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**ECE 5724 Homework 4**

**3/15/24**

1. **Introduction**
2. **Test Generation Processes**
   1. **Unfolding Bench File**

To generate test vectors for the SSC module effectively and achieve a high fault coverage the design should have its sequential and combinational components separated. This unfolding of the circuit was done in the SSC.bench file provided to us. To unfold the circuit the sequential elements, being the flip flops, were removed from the bench file. A before and after screenshot of this process is shown in Figure 1 with the unfolded file shown on the right.

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Figure 1 – Unfolding of SSC.bench With Removal of DFF

The next step in this process was to make pseudo inputs and outputs for the module. With the removal of the flip-flops, the nets connected to the DFF need to be dealt with to avoid having floating nets. The proper way to do this would be to make them visible as inputs and outputs to allow control of them for simulating the combinational logic they are connected to. To do this the outputs of the DFF are turned into pseudo primary inputs (PPI) which allows for a testbench or simulation tool to set an input value and allow the gates connected to this net to be tested. The DFF inputs are turned into pseudo primary outputs (PPO) to allow for the gates preceding this net to be tested by simulation tools. Figure 2 demonstrates some of these PPIs and PPOs added to the bench file.

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Figure 2 – Unfolded SSC.bench PPI and PPO

* 1. **Atalanta Test Generation**
  2. **Full-Scan Insertion**

1. **Virtual Tester**