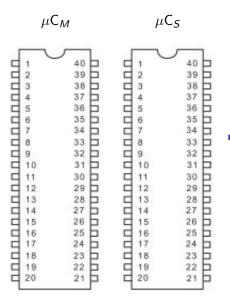
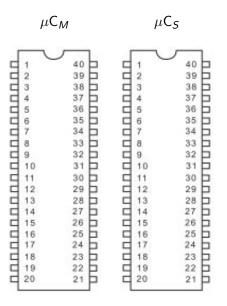
CS122A: Intermediate Embedded and Real Time Operating Systems

Jeffrey McDaniel

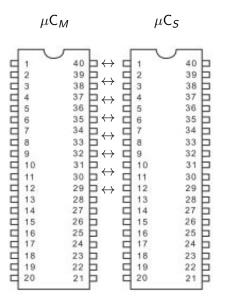
University of California, Riverside



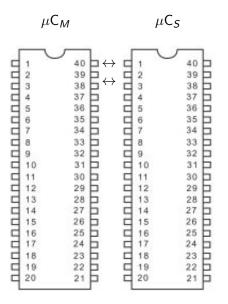
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- ► Connecting a pin for each bit of data is intractable
- Serial communication allows us to use fewer pins

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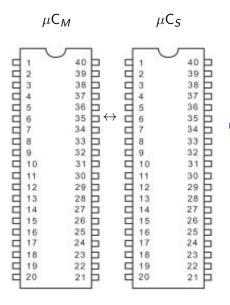
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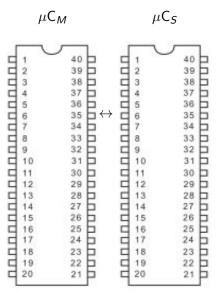
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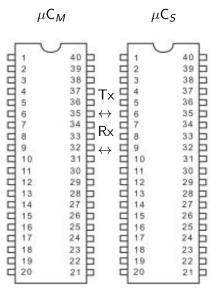
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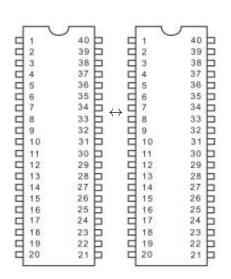


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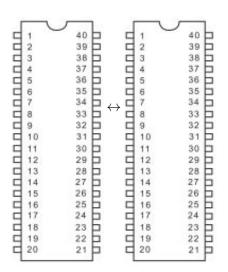
- ATMega's use Universal Asynchronous Receiver/Transmitters (UART)
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- Transmit (Tx) and Receive (Rx) over two separate pins

UART Communication $\mu C_M \qquad \mu C_S$ $T \qquad R$



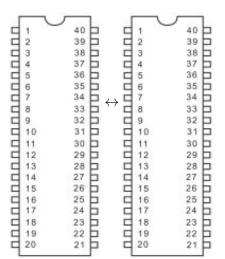
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$\begin{array}{ccc} \mathsf{UART} & \mathsf{Communication} \\ \mu \mathsf{C}_{\mathit{M}} & \mu \mathsf{C}_{\mathit{S}} \\ T & R \end{array}$



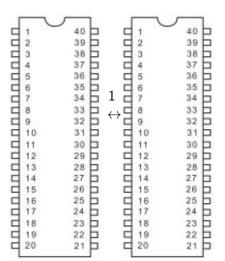
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$$\mu \mathsf{C}_M$$
 $\mu \mathsf{C}_S$ $T = 'a'$ R $\mathsf{TxReady} = 1$ $\mathsf{RxFlag} = 0$



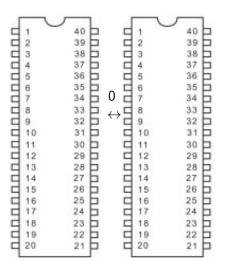
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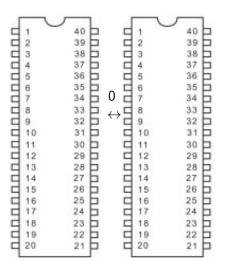
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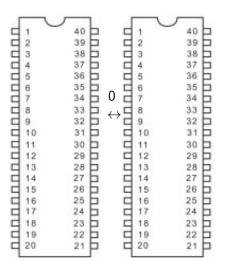
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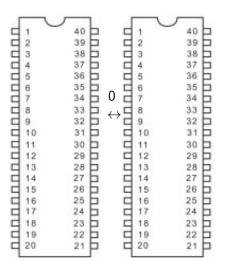
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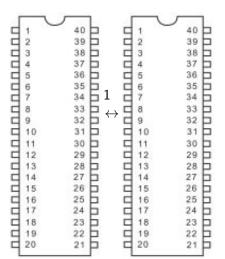
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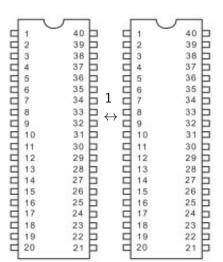
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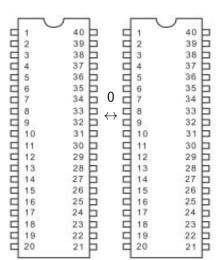
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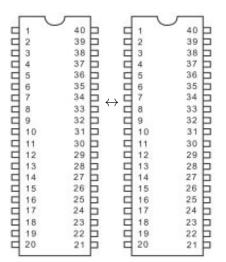
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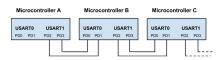
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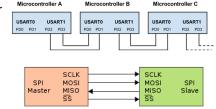
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► **SPI** is more scalable than USART

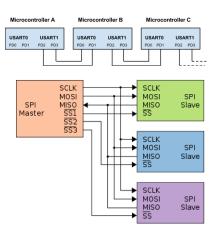
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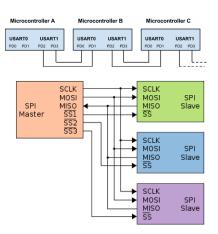
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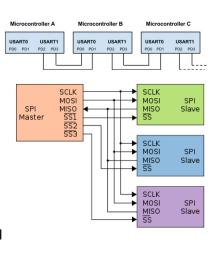
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- With 3 peripherals USART and SPI require the same number of wires
- With 4 peripherals USART requires more wires than SPI (8:7)



SPI terminology:

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- SS: Slave Select

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- 5. Master deselects SS



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- Designed to standardize connection of computer peripherals

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