DIGITAL LOGIC AND DESIGN(LAB) DA 1

NAME: UMANG AGARWAL

REG NO: 18BCE0572

Questions:

1A) Simplify ((A+B)'.(B+C)'.(A+C)')'

((A+B)'.(B+C)'.(A+C)')'

⇒ (A+B)"+(B+C)"+(A+C)"

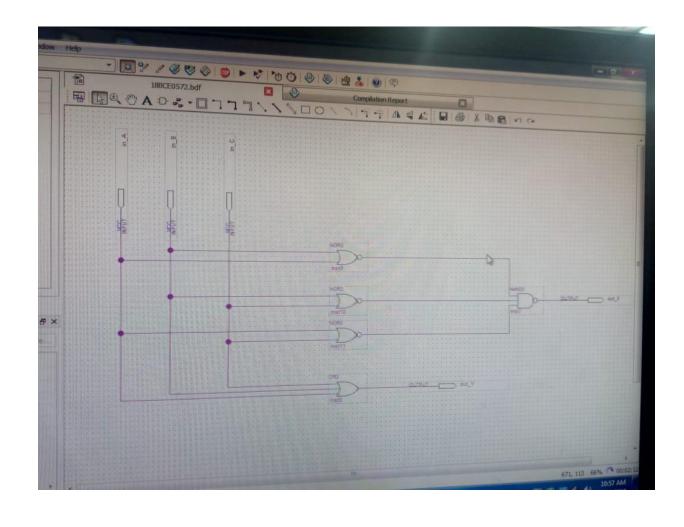
⇒ A+B+B+C+A+C

⇒ A+B+C [SIMPLIFIED FORM]

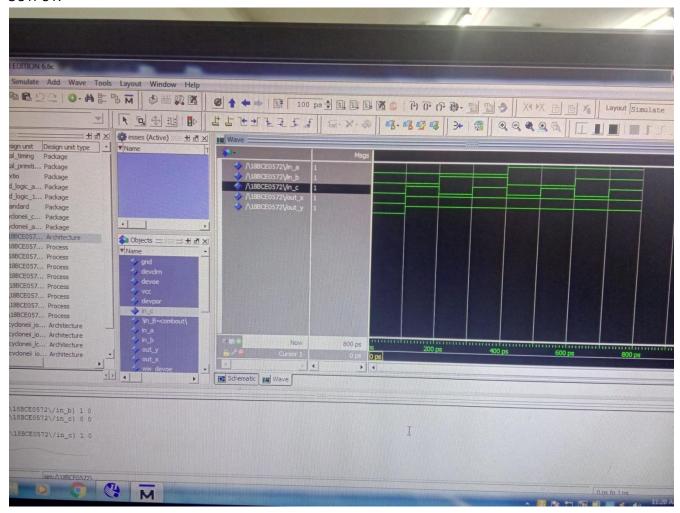
TRUTH TABLE:

А	В	С	X=((A+B)'(B+C)'(A+C)')'	Y= A+B+C
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

LOGIC CIRCUIT:



OUTPUT:



ANSWER:- Since the outputs for every input combination is the same for both X and Y which is also evident form the output screen, ((A+B)'.(B+C)'.(A+C)')' can be simplified as A+B+C

1B) Simplify (A+A'B).(B+B'C).(C+C'D)

(A+A'B).(B+B'C).(C+C'D)

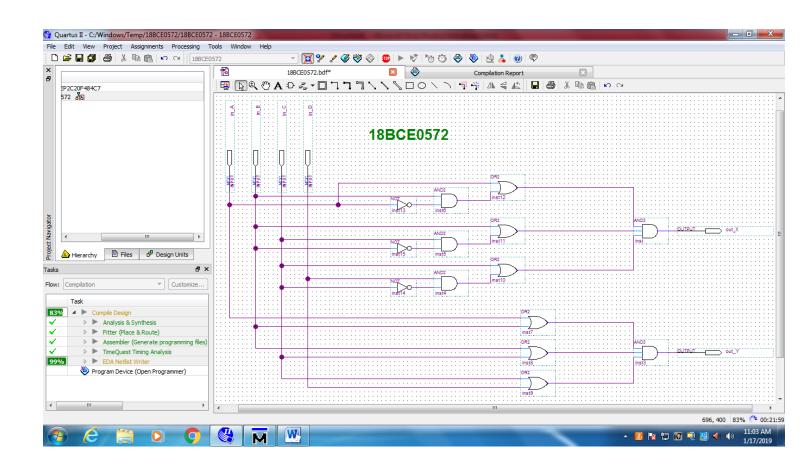
- ⇒ (A+A').(A+B).(B+B').(B+C).(C+C').(C+D)
- ⇒ (A+B).(B+C).(C+D) [SIMPLIFIED FORM]

TRUTH TABLE:

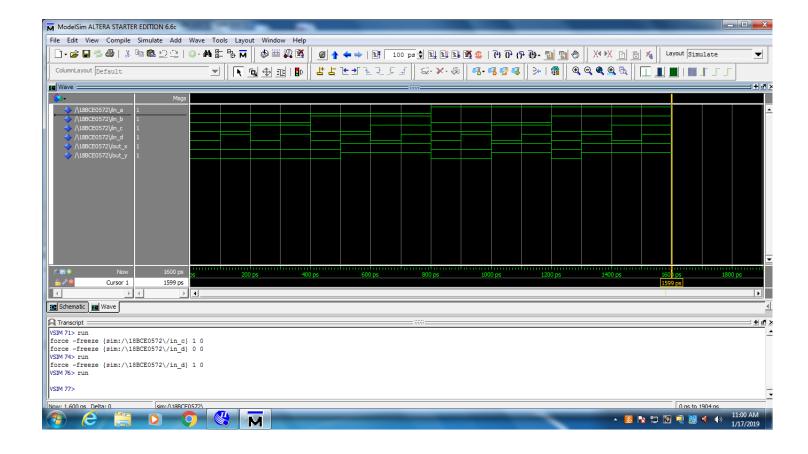
Α	В	С	D	X=(A+A'B).(B+B'C).(C+C'D)	Y=(A+B).(B+C).(C+D)
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	1	1

0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

LOGIC CIRCUIT:



OUTPUT:



ANSWER:- Since the outputs for every input combination is the same for both X and Y which is also evident form the output screen, (A+A'B).(B+B'C).(C+C'D) can be simplified as (A+B).(B+C).(C+D).

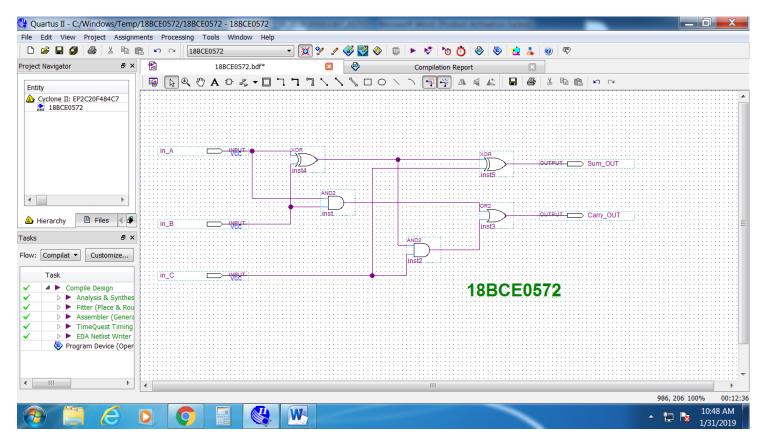
1C) Verify the full adder circuit

SUM: $A \oplus B \oplus C$ CARRY: $C.(A \oplus B) + A.B$

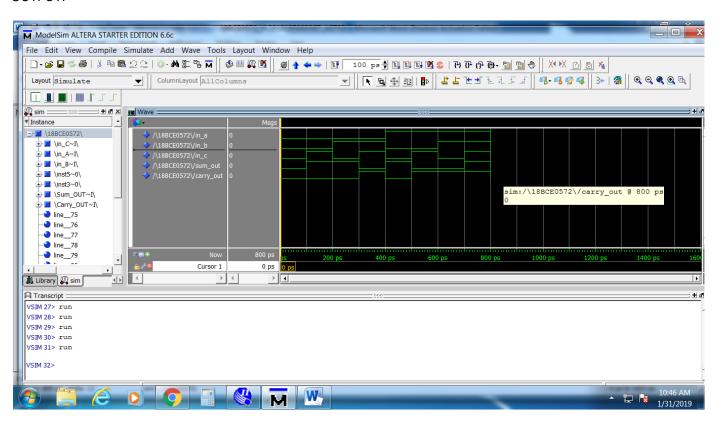
TRUTH TABLE:

A	В	С	SUM: A⊕B⊕C	CARRY: $C.(A \oplus B) + A.B$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

LOGIC CIRCUIT:



OUTPUT:



ANSWER:- Since the outputs for every input combination is the same as normal addition also shown in the output screen, the circuit for full adder is correct and has been verified.