MC68060

U4

Fan power

Default option 3V3 oscillator
(Remark: oscillator is not used with Z-turn)

Default option PCLK from Z-turn

NC
It could be necessary to terminate PCLK
for clock stability (place close to 060)

U2
XC95144XL-TQ144

_INT6 not connected on v02 (was TP1 on v02)
INT6_ARM not connected on v01 (was TP_8 on v01)
_CEAB not connected on v02 (was TP2 on v02)
_INT2 not connected on v02 (was TP3 on v02)
_040RSTO not connected on v02 (was TP4 on v02)
_BGR040 and _BTT not connected on v01 (TP_16 and TP_13, respectively)

PS_MIO12 not connected on v01 (was TP_14 on v01)
PS_MIO8 not connected on v01 (was TP_17 on v01)
PS_MIO0 not connected on v01 (was right pad of R24 on v01)

_SNOOP not connected on v02 (was TP5 on v02)
LEBUS_DMA not connected on v02 (was TP6 on v02)

SOME_CONFIG
CLOSE -> ENABLE SOME_CONFIG
OPEN -> DISABLE SOME_CONFIG
CPUCLK_RECVD not connected on v02 (was TP7 on v02)

PS_MIO13 not connected on v01 (was TP_21 on v01)

Three alternatives for voltage detection

U1B1 BU4942
U1A1 RH5VA43A
R2 10k
C400A1 NC

J1 Jumper_2_Open
4k7 R3
+3V3

R1 4k7

U3B SN74CB3T3245PW
U3A SN74CB3T3245PW
C1 100nF
+3V3

JP9 R2B 33
Default option CLK90 from Z-turn
JP10 R29 33
Default option CPUCLK from Z-turn

J2 Conn_02x07_Odd_Even
TMS TCK TDO TDI
+3V3
R4 4k7

DBG1 DBG2 DBG3

TCK TDI TDO TMS

+3V3
C2 100nF C3 100nF C4 100nF C5 100nF C6 100nF C7 100nF C8 100nF C9 100nF C10 100nF

v0.21a Changed Array Networks
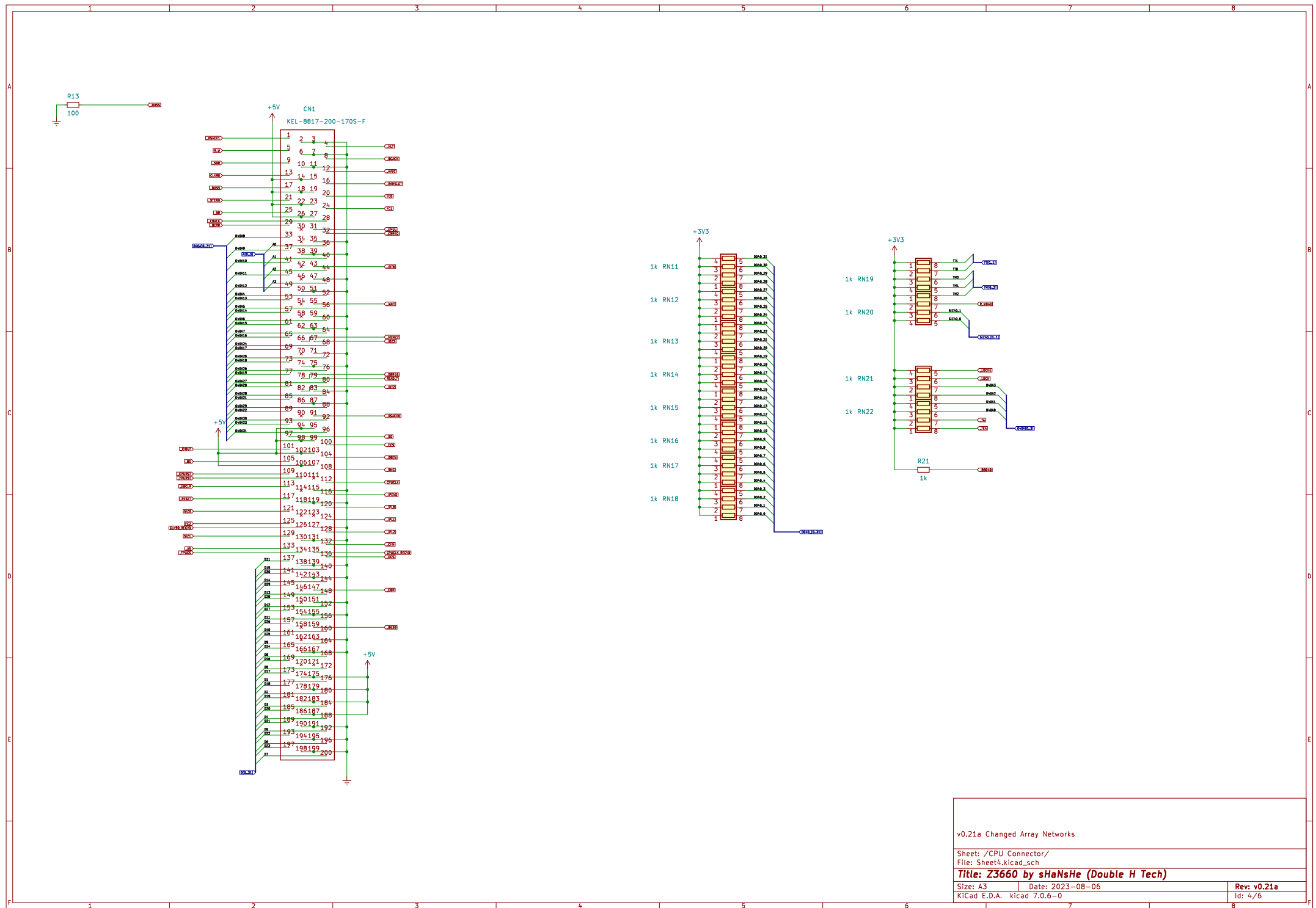
Sheet: /Bus Adapter CPLD/
File: Sheet3.kicad_sch
Title: Z3660 by sHaNsHe (Double H Tech)
Size: A3   Date: 2023-08-06   Rev: v0.21a
KiCad E.D.A. kicad 7.0.6-0   Id: 3/6

CN1
KEL-8817-200-170S-F

+5V
+3V3
+3V3

1k RN11
1k RN12
1k RN13
1k RN14
1k RN15
1k RN16
1k RN17
1k RN18

1k RN19
1k RN20
1k RN21
1k RN22

R13
100

R21
1k

NC_4 was connected to TP7 on v01, it is now PS_MIO9

PS_MIO0 -> IPL0 (not connected in v01, v02)
PS_MIO8 -> nBR_ARM (not connected in v01)
  PS_MIO8 is ARM OUT only
PS_MIO9 -> IPL1 (not connected in v01, v02???)
PS_MIO12 -> IPL2 (not connected in v01)
PS_MIO13 -> RESET_CPLD (not connected in v01)
  reset output from ARM to CPLD

MIO14 CAN'T be used for nothing useful
except maybe for ZTURN presence detector
(it is CAN RX)

PS_MIO15 -> nBG_ARM

VR1
LT1084-3.3_EXTENDED

CN3
Conn_02x40_Odd_Even

CN2
Conn_02x40_Odd_Even

U15B SN74CB3T3245PW
U16B SN74CB3T3245PW
U17B SN74CB3T3245PW
U18B SN74CB3T3245PW

U15A SN74CB3T3245PW
U16A SN74CB3T3245PW
U17A SN74CB3T3245PW
U18A SN74CB3T3245PW

U1
LTC2990

D1 LED_Small
D2 LED_Small

680 R15
1k R16

9k 0.1% R26
1k 0.1% R25
9k 0.1% R27
1k 0.1% R23
9k 0.1% R22
9k 0.1% R30
1k 0.1% R24
4k7 R17
R18 4k7

C50 100nF C51 100nF C52 100nF
C44 100nF C45 100nF C46 100nF C47 100nF C48 100nF C49 100nF
C38 100nF C39 10uF C40 10uF
C41 22uF C42 10uF C43 10uF
C53 100nF C54 100nF
C55 100nF C56 100nF
C57 100nF C58 100nF C59 100nF C60 100nF
C63 100nF

TP4 +5V
TP1 +3V3
TP8 GND
TP9 PCLK
TP10 CLK90
TP11 CPUCLK

JP5
JP4
JP12

v0.21a Changed Array Networks

Sheet: /ZTURN and 3.3V/
File: Sheet5.kicad_sch

Title: Z3660 by sHaNsHe (Double H Tech)

| Size: A4 | Date: 2023-08-06 | Rev: v0.21a |
| KiCad E.D.A. kicad 7.0.6-0 | | Id: 5/6 |

CPU and CLK

File: Sheet1.kicad_sch

ZTURN and 3.3V

File: Sheet5.kicad_sch

Bus Adapter CPLD

File: Sheet3.kicad_sch

Data Bus Buffer

File: Sheet2.kicad_sch

CPU Connector

File: Sheet4.kicad_sch