THIS IS A FLAT SCHEMATIC, NOT A HIERARCHICAL ONE. NETS USE "OFFPAGE CONNECTOR" SYMBOLS TO GO FROM PAGE TO PAGE. ON ANY PAGE, THE NUMBER OF THE CONNECTING PAGE(S) IS SHOWN IN A SMALL NUMBER BELOW THE SIGNAL NAME.

THE SCHEMATIC IS DIVIDED INTO SECTIONS OF RELATED FUNCTIONALITY. THE SECTIONS ARE:
1: NOTES AND BLOCK DIAGRAMS
2: OFF-BOARD SIGNALS (SM AND FRONT PANEL), GLOBAL CLOCKING
3: POWER SOURCES AND CONTROLS
4: I2C CONTROLS
5: FPGA#1 POWER AND SIGNAL (NON-MGT)
6: FPGA#2 POWER AND SIGNAL (NON-MGT)
7: FPGA#1 GTY TRANSCEIVERS (MOSTLY FIREFLY)
8: FPGA#2 GTY TRANSCEIVERS (MOSTLY FIREFLY)
9: BETWEEN-FPGA GTY TRANSCEIVERS

These are some general signal naming conventions:

1) Signals connected to the FPGAs contain either "F1" or "F2".

2) Signals connected to the Service Module contain "SM".

3) Signals connected to the Front Panel contain "FP".

4) Signal names starting with “PG” are “Power Good” signals from power modules.

5) Signal names starting with “EN” are “Enable” signals to turn on power modules.

6) GTY reference clock names indicate FPGA followed by side (F1L, F1R, F2L, F2R), then the reference clock (R0 or R1), finishing with the sequence order (1 thru 7).

7) Power source names start with "V_", then the voltage with the letter "V" as a decimal point. (V_3V3 is a 3.3 volt source)

8) The MCU I/Os are 3.3 volt and the FPGA I/Os are 1.8 volt. Level shifters are used for the conversion. Signal names on the FPGA side are prefaced with "lov" (low voltage) and signals on the MCU side are prefaced with "hiv" (high voltage).

TO DO:

THIS DESIGN INCLUDES FPGA CONFIGURATION MEMORIES. WE SHOULD STILL VERIFY THAT PROGRAMMING AND BOOTING WORK ON CMv1.

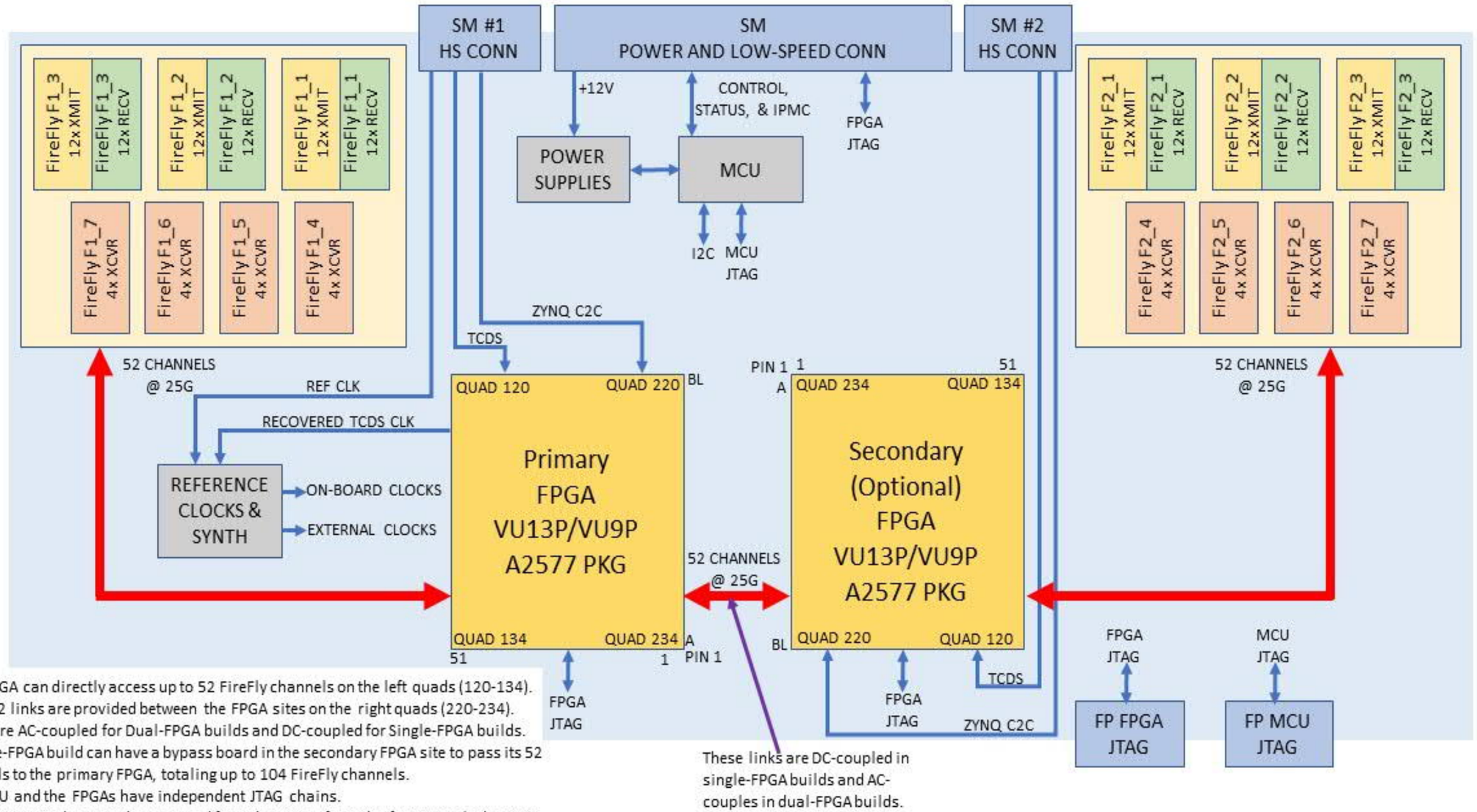
IF THE FPGA IS NOT INSTALLED, THEN "FPGA_DONE" WILL ALWAYS BE HIGH, AND THE LED WILL ALWAYS BE LIT. THIS IS UNINTENDED AND UNDESIRABLE. CONSIDER ELIMINATING THE FPGA DONE LED.

VERIFY PROPER RESISTOR VALUES FOR ALL LGA80D CONFIGURATIONS.

ADD MORE GENERIC PAIRS BETWEEN THE TWO FPGAS.

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.01: NOTES		
Size	Document Number: 6089-119	Rev: A
Date: Monday, February 22, 2021	Sheet 1 of 80	

Apollo CM Dual A2577: Block Diagram



Notes:

- Each FPGA can directly access up to 52 FireFly channels on the left quads (120-134).
- Up to 52 links are provided between the FPGA sites on the right quads (220-234). These are AC-coupled for Dual-FPGA builds and DC-coupled for Single-FPGA builds.
- A single-FPGA build can have a bypass board in the secondary FPGA site to pass its 52 channels to the primary FPGA, totaling up to 104 FireFly channels.
- The MCU and the FPGAs have independent JTAG chains.
- The FPGA JTAG chain can be accessed from the SM or from the front panel. The MCU JTAG only has front panel access. The MCU code can be change from an SM serial port.
- The recovered TCDS clock is only available from the primary FPGA.

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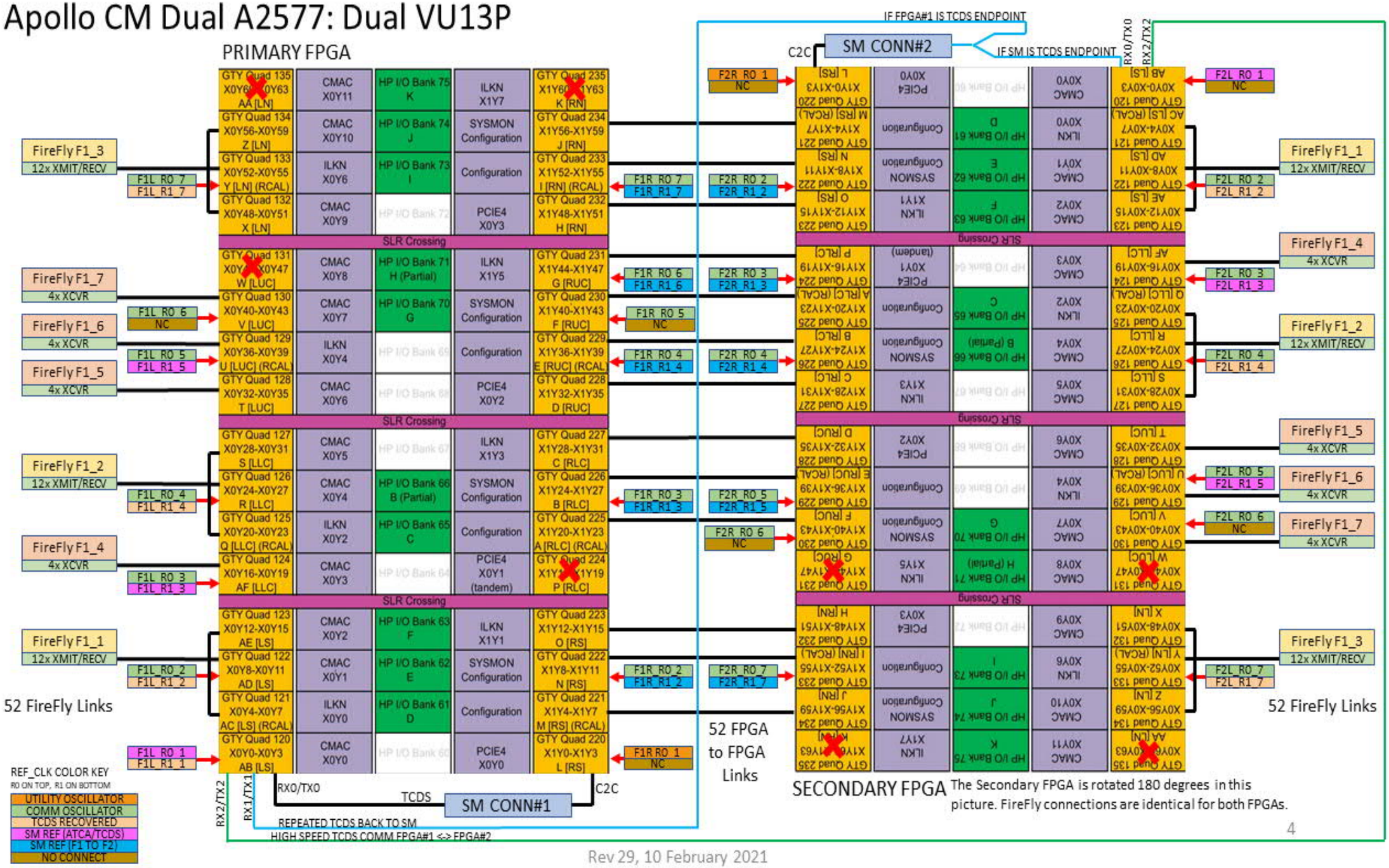
APOLLO CM W/ DUAL A2577, MK1		
Title: 1.02: BLOCK DIAGRAM		
Size	Document Number: 6089-119	Rev: A
Date: Wednesday, February 17, 2021	Sheet 2 of 80	

Apollo CM Dual A2577: Dual VU13P

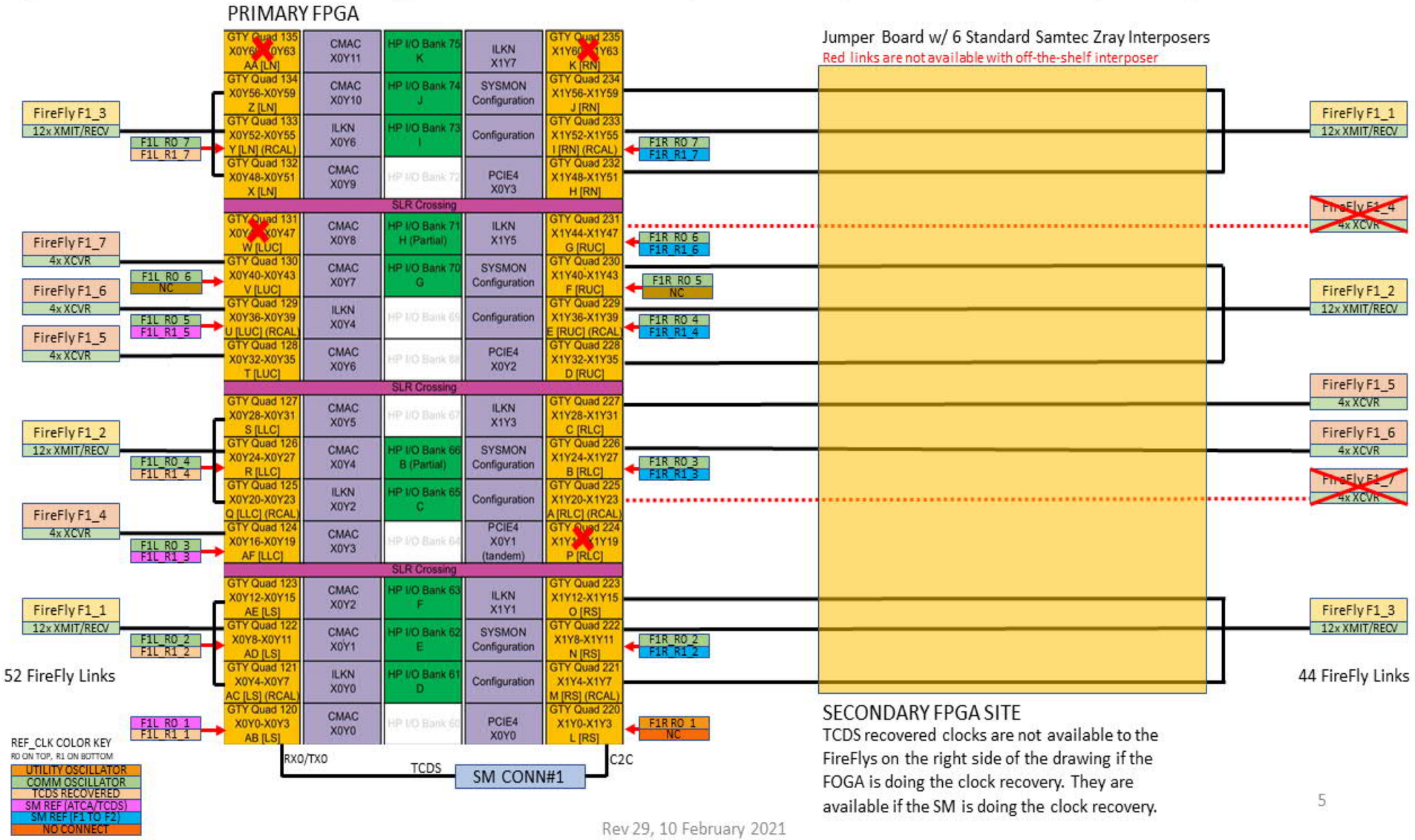


4

Rev 29, 10 February 2021

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.03: DUAL VU13P		
Size	Document Number: 6089-119	Rev: A
Date: Wednesday, February 17, 2021	Sheet 3 of 80	

Apollo CM Dual A2577: Single VU13P with Jumper Board (off-the-self Interposers)



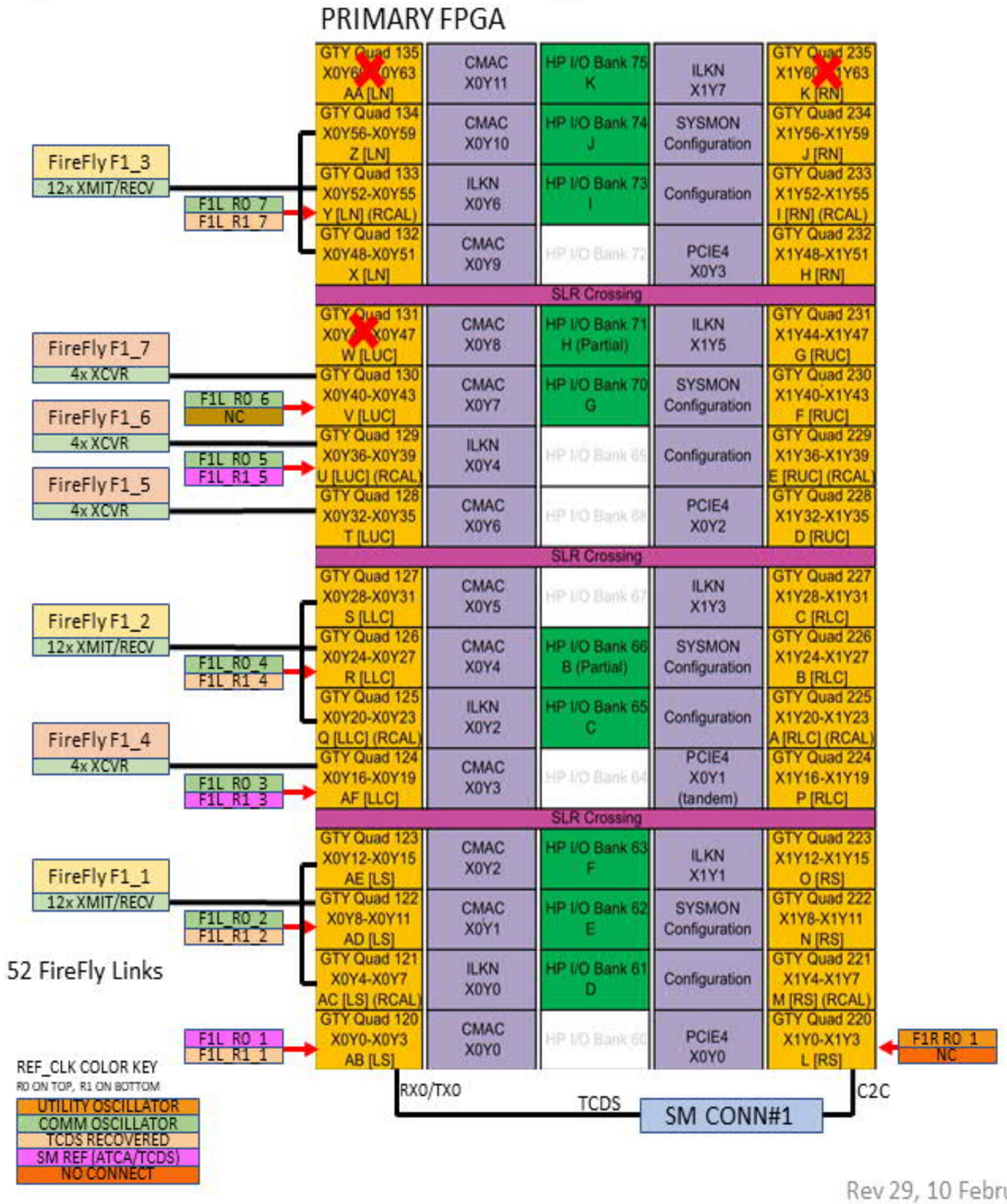
SECONDARY FPGA SITE

TCDS recovered clocks are not available to the FireFlys on the right side of the drawing if the FOGA is doing the clock recovery. They are available if the SM is doing the clock recovery.

Rev 29, 10 February 2021

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.04: SINGLE VU13P AND JUMPER		
Size	Document Number: 6089-119	Rev: A
Date: Wednesday, February 17, 2021	Sheet 4 of 80	

Apollo CM Dual A2577: Single VU13P



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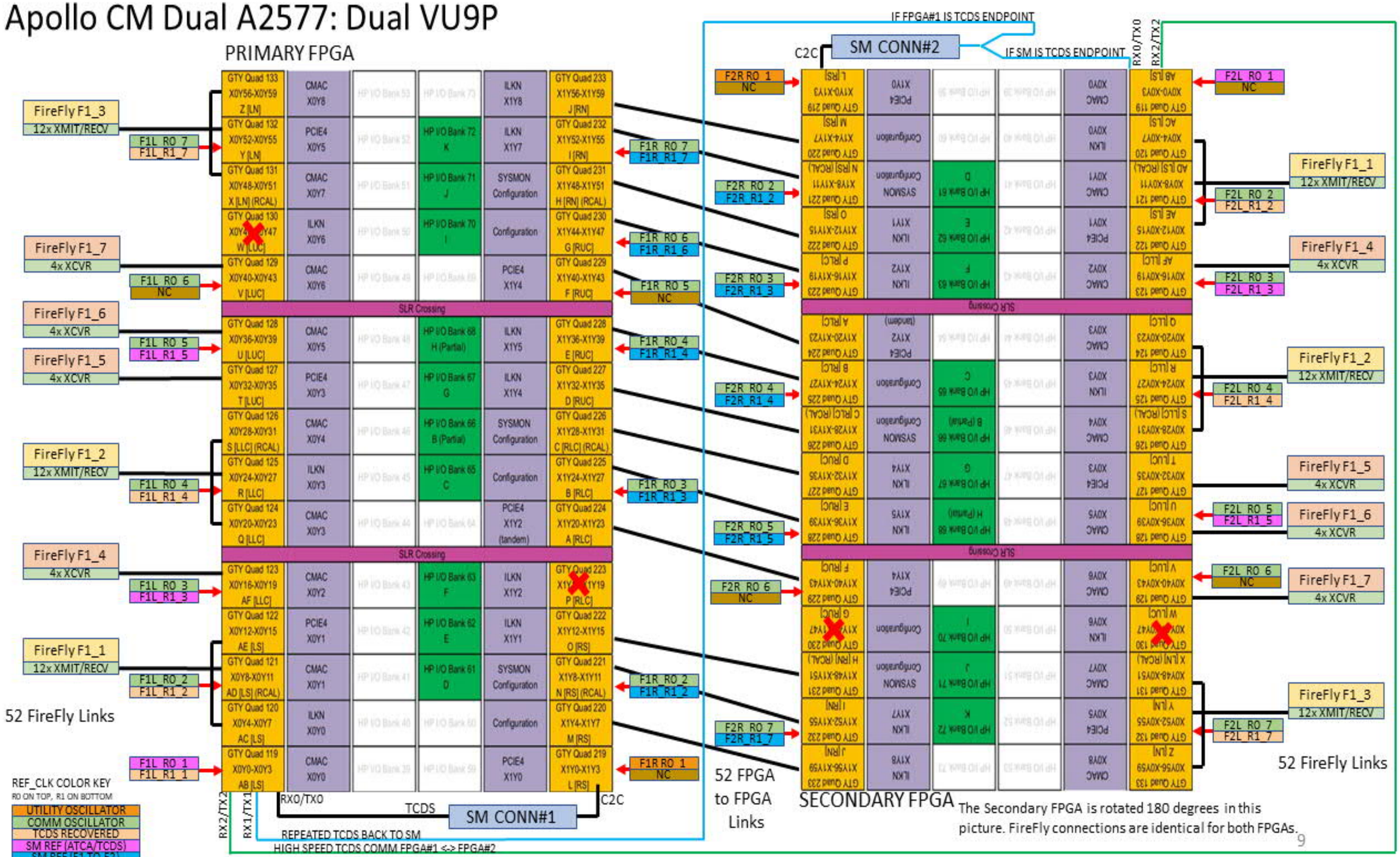
Rev 29, 10 February 2021

APOLLO CM W/ DUAL A2577, MK1			
Title: 1.05: SINGLE VU13P			
Size	Document Number: 6089-119		Rev: A
Date: Wednesday, February 17, 2021	Sheet 5 of 80		

Apollo CM Dual A2577: Dual VU9P



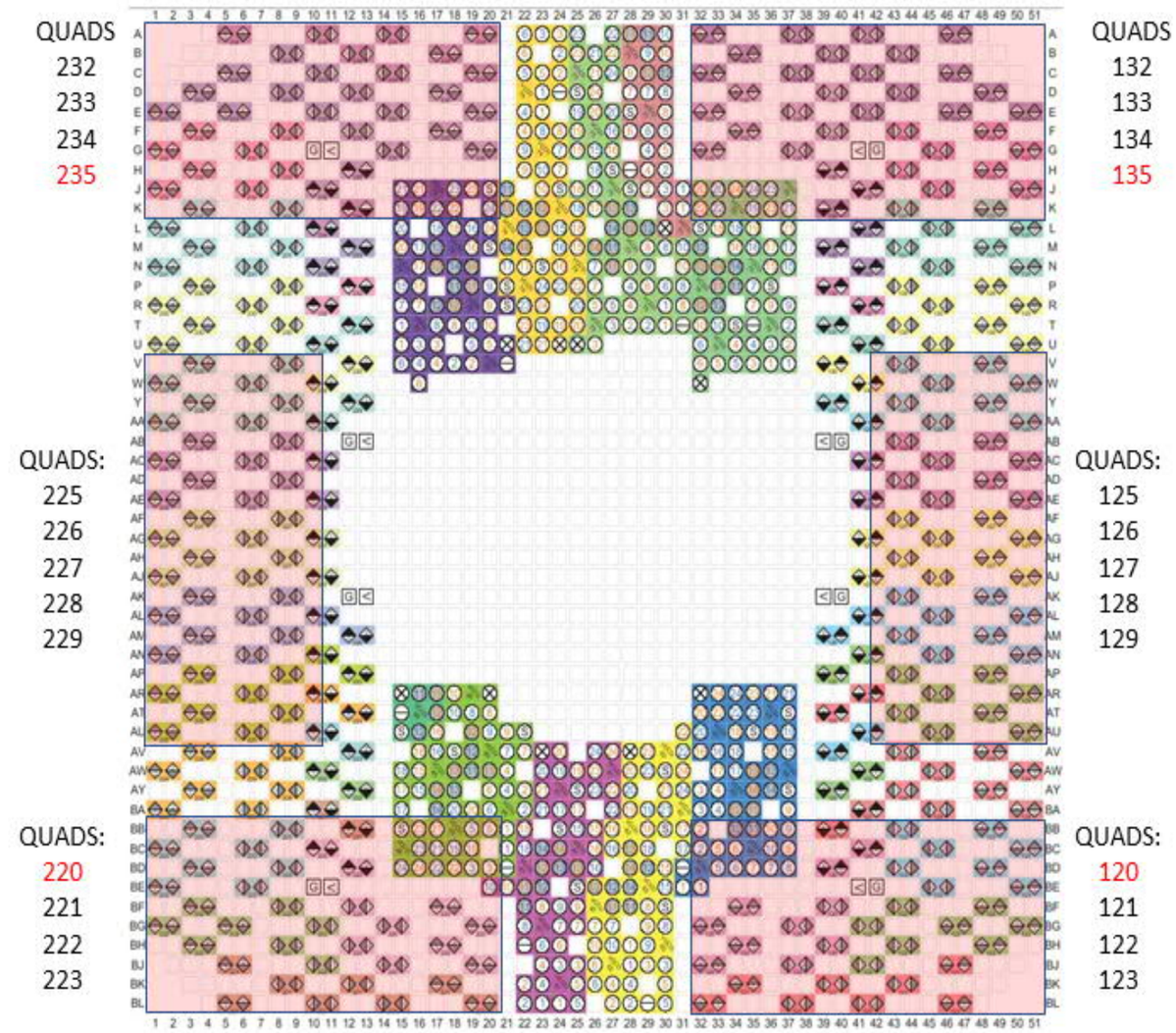
Rev 29, 10 February 2021

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.06: DUAL VU9P		
Size	Document Number: 6089-119	Rev: A
Date: Wednesday, February 17, 2021	Sheet 6 of 80	

Apollo CM Dual A2577: 6 Interposer proof of principle

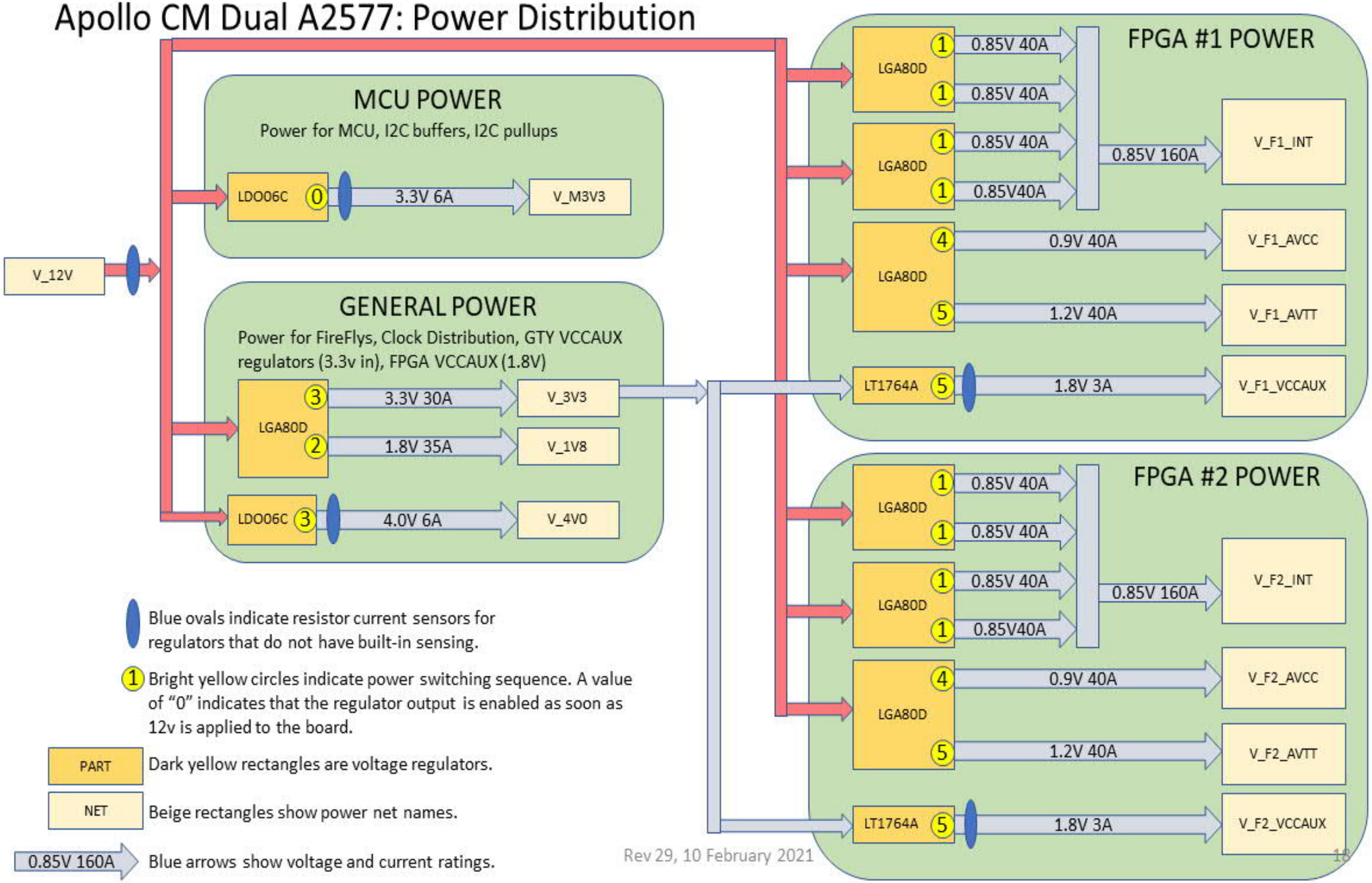
Diagram shows interposer location and available quads when 6 10x20 interposers are used to connect the jumper board.

Only quads numbered in black will be routed on the initial version. Quads numbered in red, while accessible to the interposers, will not be routed on the jumper board.



APOLLO CM W/ DUAL A2577, MK1		
Title: 1.07: SIX 10X20 INTERPOSERS		
Size	Document Number: 6089-119	Rev: A
Date: Wednesday, February 17, 2021	Sheet 7 of 80	

Apollo CM Dual A2577: Power Distribution



Blue ovals indicate resistor current sensors for regulators that do not have built-in sensing.

(1) Bright yellow circles indicate power switching sequence. A value of "0" indicates that the regulator output is enabled as soon as 12v is applied to the board.

PART — Dark yellow rectangles are voltage regulators.

NET — Beige rectangles show power net names.

0.85V 160A — Blue arrows show voltage and current ratings.

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APOLLO CM W/ DUAL A2577, MK1		
Title: 1.08: POWER		
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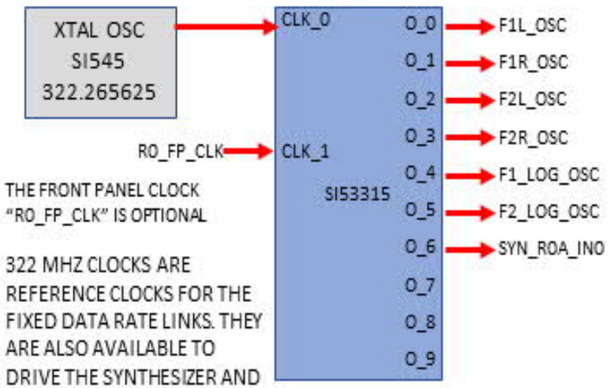
Apollo CM Dual A2577: On-Board Clock Sources

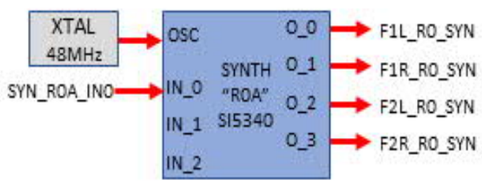
Oscillator Clocks / Reference Clock 0 (R0) Distribution

200 MHZ CLOCKS ARE UTILITY CLOCKS FOR THE FPGA LOGIC AND REFERENCE CLOCKS FOR THE SM C2C LINKS

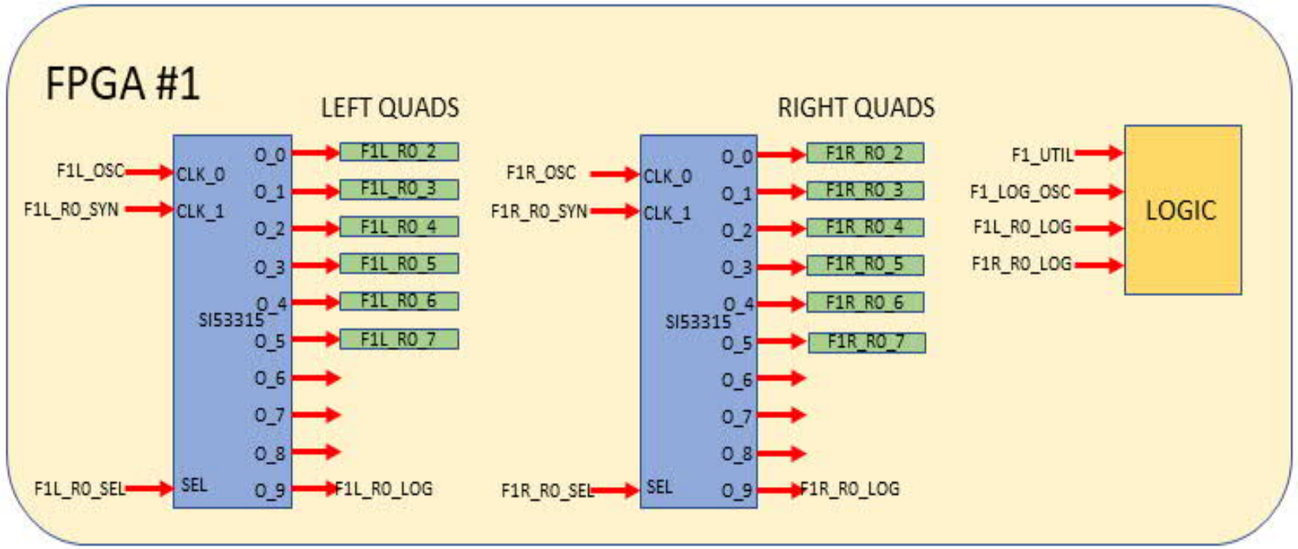


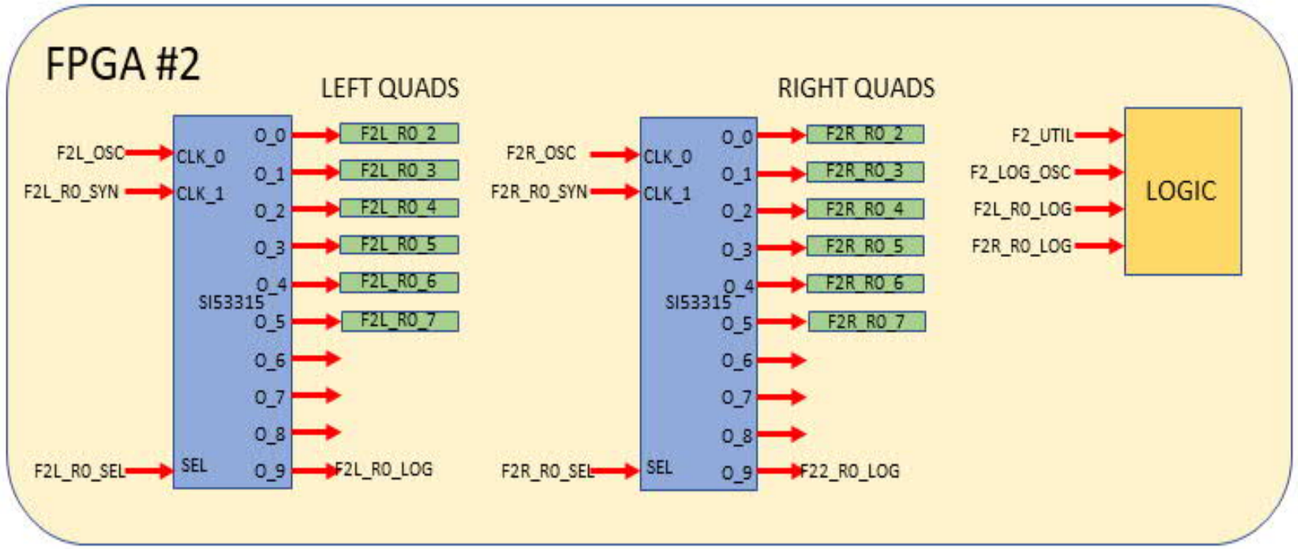
THE FRONT PANEL CLOCK "R0_FP_CLK" IS OPTIONAL

322 MHZ CLOCKS ARE REFERENCE CLOCKS FOR THE FIXED DATA RATE LINKS. THEY ARE ALSO AVAILABLE TO DRIVE THE SYNTHESIZER AND THE FPGA LOGIC.



THE REFERENCE CLOCK 0 SYNTHESIZER CAN BE DRIVEN BY A LOCAL OSCILLATOR OR THE FIXED DATA RATE OSCILLATOR (AND FRONT PANEL INPUT) FANOUT.

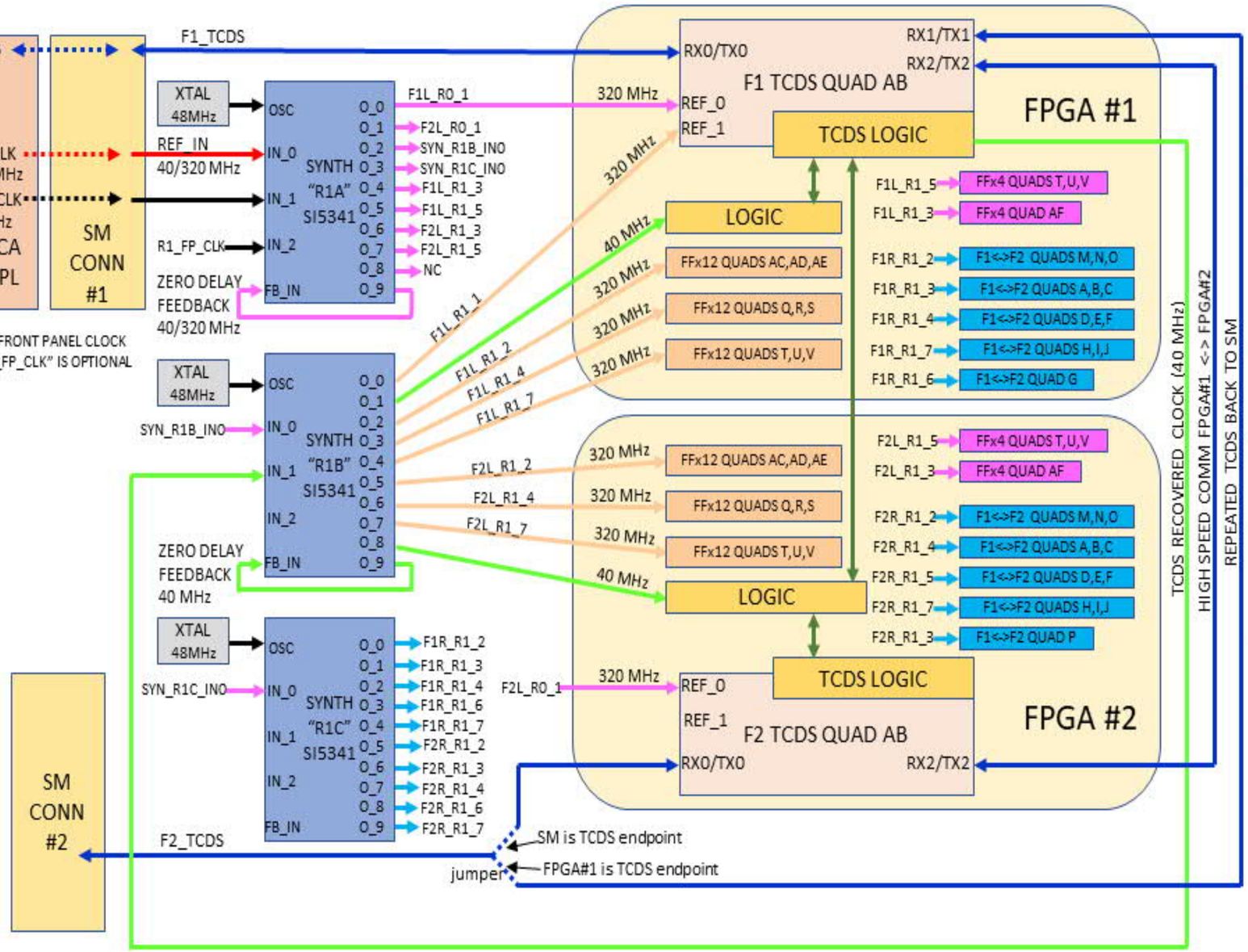




APOLLO CM W/ DUAL A2577, MK1		
Title: 1.09: ON-BOARD OSCILLATOR CLOCKS		
Size	Document Number: 6089-119	Rev: A
Date: Wednesday, February 17, 2021	Sheet 9 of 80	

Apollo CM Dual A2577: External Clock Sources

ATCA Clock and TCDS Clock/Data



GBIT CLOCK/DATA COMBINED

LHC REFERENCE CLOCK

If the SM is not the TCDS endpoint, then this is a 320 MHz clock passed directly from the ATCA backplane. If the SM is the TCDS endpoint, then this is the 40 MHz clock recovered from the backplane TCDS signal. In either case, the frequency of this clock changes when the LHC is ramping.

320 MHz REF CLOCK

If the top synthesizer is using the clock on "IN_0", then these 320 MHz clocks all have zero phase offset relative to the incoming LHC REFERENCE CLOCK signal.

40 MHz TCDS RECOVERED CLOCK

This clock is recovered from the incoming TCDS signal. The TCDS LOGIC synchronizes this clock to the bunch crossing. It also adjusts the phase to compensate for distribution delay changes. It will always maintain a fixed phase relative to the bunch crossing. The frequency also varies during filling. This clock is made available to the logic in the FPGAs for synchronizing operations.

320 MHz TCDS RECOVERED CLOCK

These clocks drive the detector-facing FireFly devices, as well as the quad that sends the outgoing TCDS signal back to the SM. They track the TCDS RECOVERED CLOCK.

FPGA TO FPGA R1 CLOCK

These clocks drive the R1 reference for the FPGA quads that connect to the other FPGA. The frequency follows the 320 MHz REF CLOCK.

TTC/TTS DATA/CONTROL

These signals contain clocks/data/control extracted from the incoming TCDS signal (TTC) or destined for the outgoing TCDS signal (TTS). They are used within each FPGA, and can also pass from one FPGA to the other.

OTHER CLOCKS

These include the 40 MHz LHC clock and the outputs of various crystal oscillators. These can be used for testing or for adding flexibility to the synthesizer outputs.

GTY QUADS

FFx12 QUADS	12-lane FireFlys. For the IT-DTC, these will be detector facing.
FFx4 QUADS	4-lane FireFlys.
F1<->F2 QUADS	Connections between the two FPGAs. These will be FireFly links in the case of a single FPGA with jumpers at the secondary FPGA site.
TCDS QUAD	Dedicated for TCDS function.

Rev 29, 10 February 2021

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.10: EXTERNAL CLOCKS		
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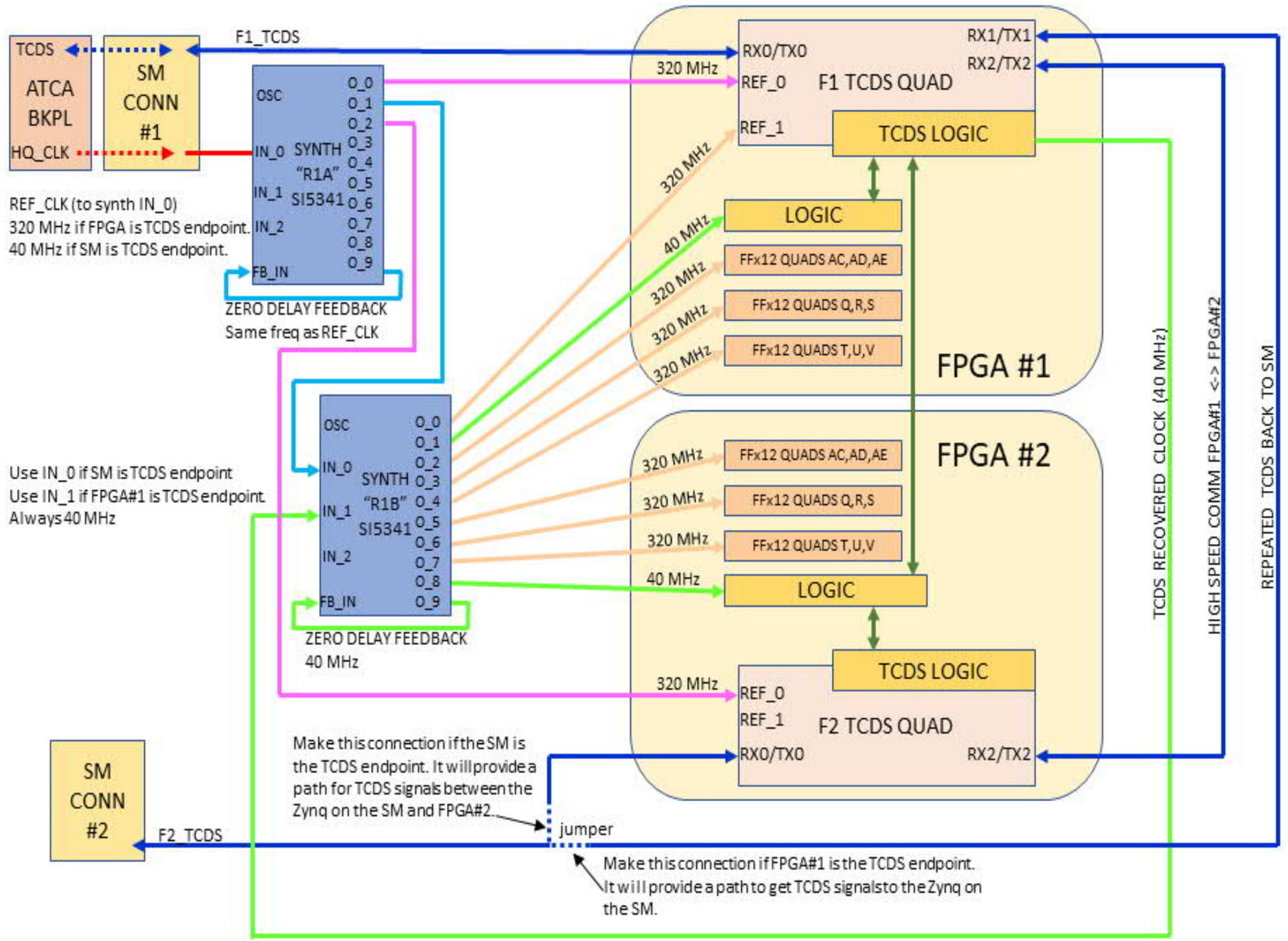
Apollo CM Dual A2577: TCDS Simplified

ATCA Clock and TCDS Clock/Data



GBIT CLOCK/DATA COMBINED

REFERENCE CLOCK

If FPGA#1 is the TCDS endpoint, then this is a 320 MHz clock passed directly from the ATCA backplane.
If the SM is the TCDS endpoint, then this is the 40 MHz clock recovered from the backplane TCDS signal.
In either case, the frequency of this clock changes when the LHC is ramping.

320 MHz REF CLOCK

These 320 MHz clocks all have zero phase offset relative to the incoming REFERENCE_CLOCK signal.

40 MHz TCDS RECOVERED CLOCK

This clock is recovered from the incoming TCDS signal. The TCDS LOGIC synchronizes this clock to the bunch crossing. It also adjusts the phase to compensate for distribution delay changes. It will always maintain a fixed phase relative to the bunch crossing. The frequency also varies during filling. This clock is made available to the logic in the FPGAs for synchronizing operations.

320 MHz TCDS RECOVERED CLOCK

These clocks drive the detector-facing FireFly devices, as well as the quad that sends the outgoing TCDS signal back to the SM. They track the TCDS RECOVERED CLOCK.

TTC/TTS DATA/CONTROL

These signals contain clocks/data/control extracted from the incoming TCDS signal (TTC) or destined for the outgoing TCDS signal (TTS). They are used within each FPGA, and can also pass from one FPGA to the other.

GTY QUADS

FFx12 QUADS — 12-lane FireFlys. For the IT-DTC, these will be detector facing.

TCDS QUAD — Dedicated for TCDS function.

Rev 29, 10 February 2021

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.11: TCDS SIMPLIFIED		
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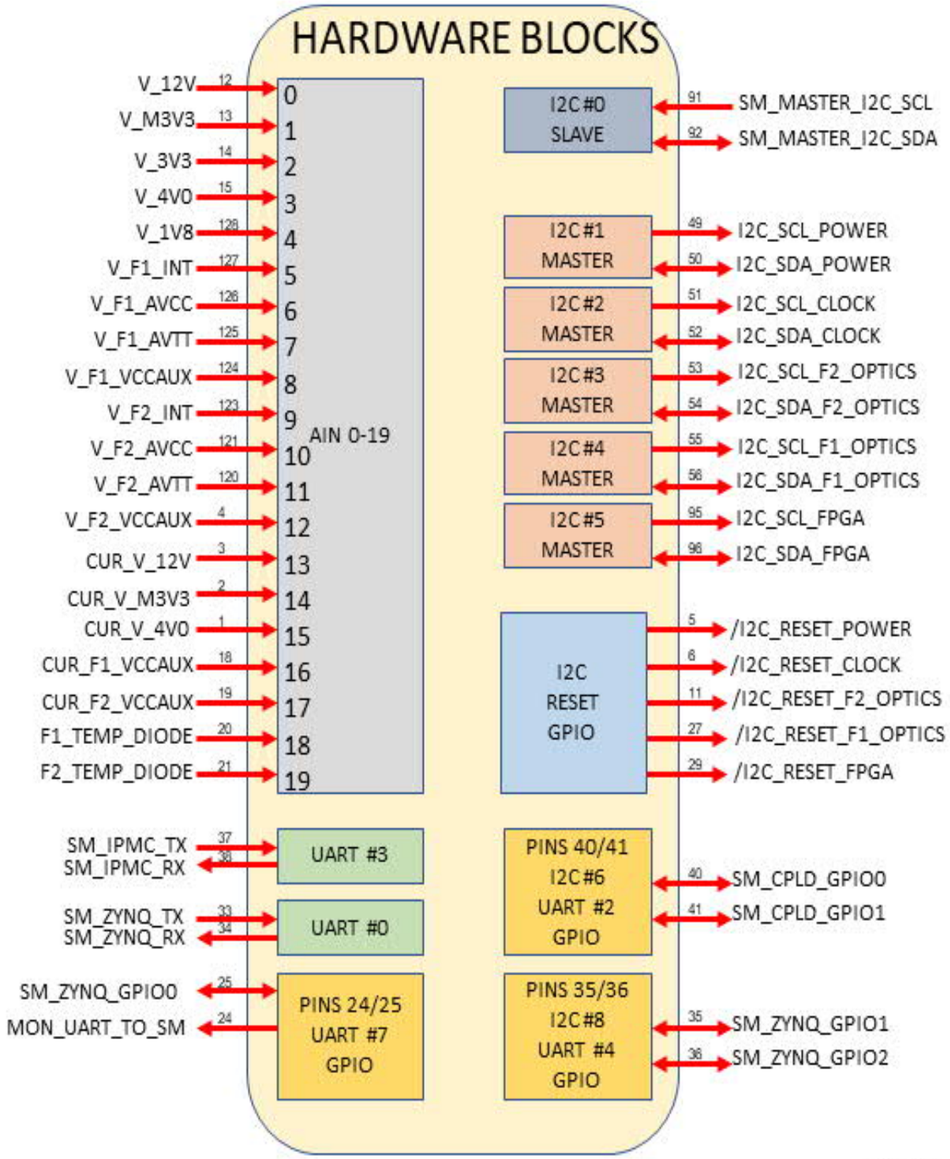
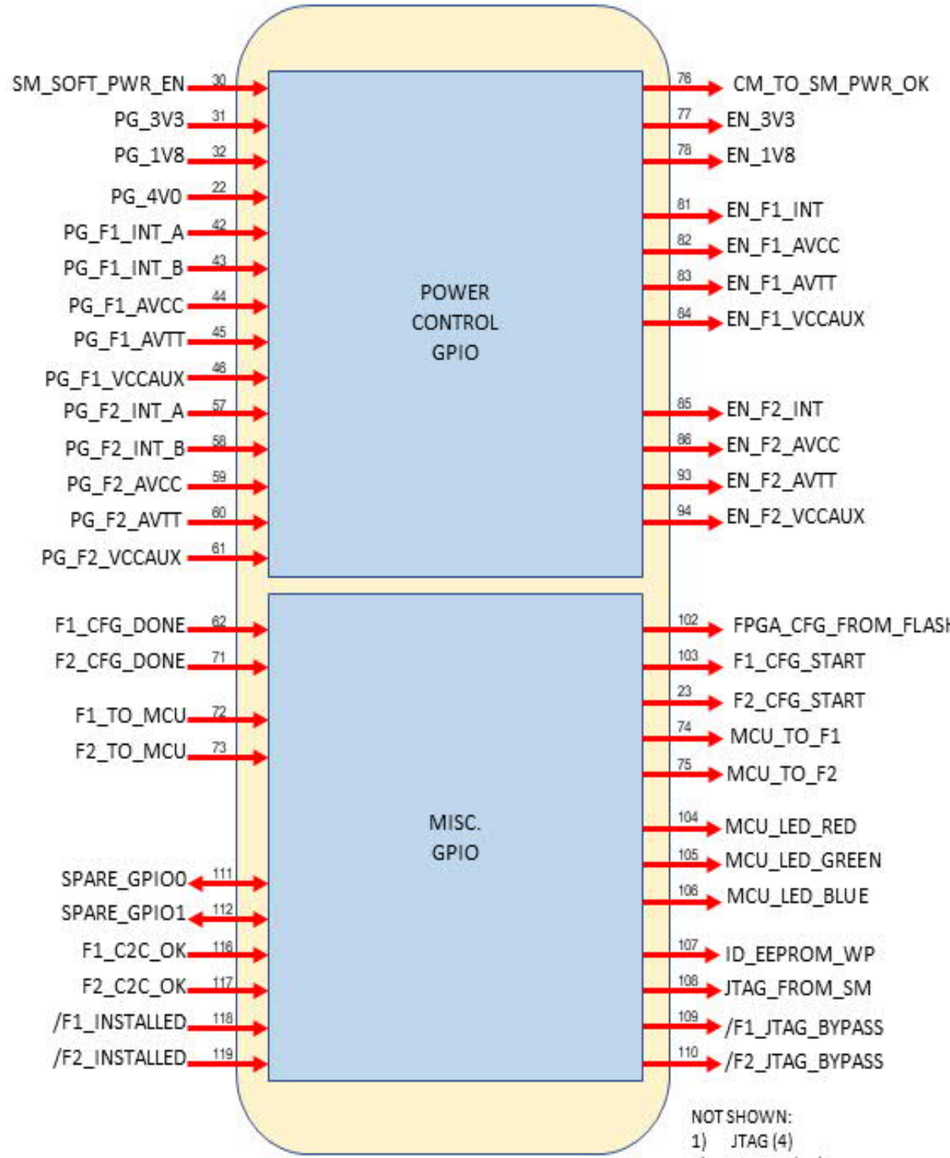
Apollo CM Dual A2577: MCU Connections and Internal Resources

1) Connect a non-SYSMON FPGA I2C block for user use
2) Consider a single I2C for optics





NOT SHOWN:
1) JTAG (4)
2) POWER (23)
3) CLOCKING (4)
4) CONTROL (3)

Rev 30, 18 February 2021

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.12: MCU I/O AND INTERNALS		
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2.01: SM POWER CONNECTOR

THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. RESISTANCE OF 1 MILLIOHMS AND A CURRENT OF 25 AMPS WILL PRODUCE A VOLTAGE OF 25MILLIVOLTS. THE SENSE AMPLIFIER HAS A GAIN OF 100, YIELDING 2.5 VOLTS AT 25 AMPS. THIS EQUALS 300 WATTS.

U214 INA240A3-Q1: IN+ (8), IN- (1), REF1 (7, GND), REF2 (3, GND), OUT (5) → CUR_V_12V 31, NC (4) → GND, VCC (6) → V_M3V3, GND (2) → GND; V_M3V3 → C2030 0.1 UF 0402 → GND

12V_INPUT → S1 → R1103 0.001 (S2) → V_12V

V_12V
R = 0.001 OHM
GAIN = 100 V/V
SCALE = 10 AMPS PER VOLT

THE "POWER_OK" SIGNAL WILL BE ASSERTED WHEN THE MCU HAS FINISHED TURNING ON ALL FPGA POWER SUPPLIES, AND THEY ARE ALL GOOD.

R1122 270 0603 → D8 LED GREEN → V_3V3

POWER OK LED

Q30 FET_N_1.8V: 1 → R1123 47K 0603 → GND; 2 → GND; 3 → R1122

IF THE SERVICE BLADE HAS I2C PULLUP RESISTORS, THEN THESE RESISTORS SHOULD BE A LARGE VALUE, JUST SUFFICIENT TO HOLD THE CONTROLLER INPUTS HIGH.

IF THE SERVICE BLADE DOES NOT HAVE I2C PULLUP RESISTORS, THEN THESE NEED TO BE AN APPROPRIATE VALUE FOR I2C OPERATION.

V_M3V3 → R1124 2.2K 0603 → R1125 2.2K 0603

MCU UART

THIS CONNECTOR IS FOR A STANDALONE USB-TO-UART CABLE. SEE DIGIKEY 768-1015 (FTDI TTL-232R-3V3). THE FACTORY CONNECTOR NEEDS TO BE REPLACED WITH A 6-PIN 2MM PLUG.

THIS SHOULD ONLY BE USED WHEN THE CM IS NOT MATED TO AN SM.

J24 CON6: 1 → GND; 2; 3 → V_M3V3; 4; 5 → GND; 6

J17 CON4: 1, 2, 3, 4 → GND

BENCHTOP POWER INLET

P1 ET60T-D02-3-08-000

P1			
PWR_GOOD	1-1	1	CM_TO_SM_PWR_OK
TMS	1-2	2	SM_JTAG_TMS 15
TDO	1-3	3	SM_JTAG_TDO 15
TX_IPMC	1-4	4	R726 0 0603 — SM_IPMC_TX
TX_ZYNQ	1-5	5	R728 0 0603 — SM_ZYNQ_TX
SENSE_SDA	1-6	6	SM_MASTER_I2C_SDA
PWR_EN	1-7	7	SM_SOFT_PWR_EN
FPGA_GPIO0	1-8	8	SM_ZYNQ_GPIO0
FPGA_GPIO1	2-1	9	R1104 270 0603 — SM_ZYNQ_GPIO1
GND_LOGIC	2-2	10	GND
GND_LOGIC	2-3	11	GND
FPGA_GPIO2	2-4	12	R1105 270 0603 — SM_ZYNQ_GPIO2
GND_LOGIC	2-5	13	GND
CPLD_GPIO0	2-6	14	R1106 270 0603 — SM_CPLD_GPIO0
GND_LOGIC	2-7	15	GND
CPLD_GPIO1	2-8	16	R1107 270 0603 — SM_CPLD_GPIO1
EN	3-1	17	SM_TO_CM_PWR_EN 16
TCK	3-2	18	SM_JTAG_TCK 15
TDI	3-3	19	SM_JTAG_TDI 15
RX_IPMC	3-4	20	R727 0 0603 — SM_IPMC_RX
RX_ZYNQ	3-5	21	R729 0 0603 — SM_ZYNQ_RX
SENSE_SCL	3-6	22	SM_MASTER_I2C_SCL
MON_RX	3-7	23	MON_UART_TO_SM
/PS_RST	3-8	24	

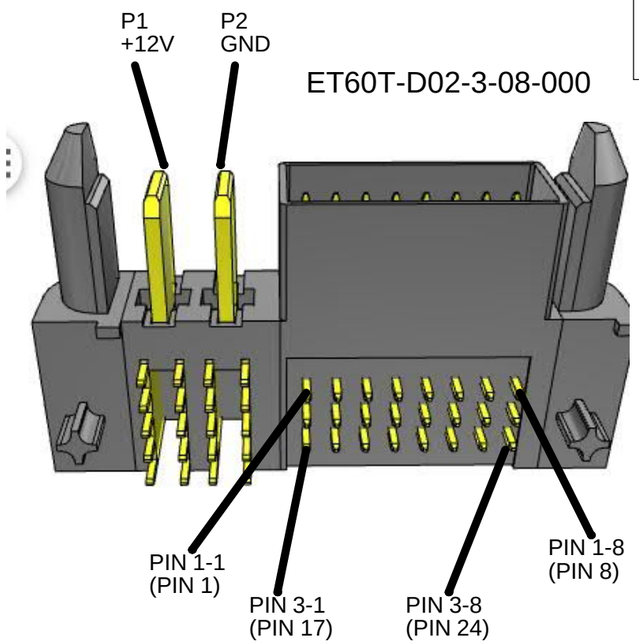
THESE ARE THE SIGNAL NAMES ON THE SMv2

/PS_RST IS NOT USED IN THIS DESIGN

P1 GND → P2-1 … P2-10

U540-8 TM4C1290NCPDT_NEW

PM2	76	CM_TO_SM_PWR_OK
UART0_RX(PA0)	33	SM_IPMC_TX
UART3_RX(PB0)	37	SM_ZYNQ_TX
I2C_SDA0	92	SM_MASTER_I2C_SDA
PH1	30	SM_SOFT_PWR_EN
UART7_RX(PA2)	25	SM_ZYNQ_GPIO0
PA2	35	SM_ZYNQ_GPIO1
PA3	36	SM_ZYNQ_GPIO2
PA6	40	SM_CPLD_GPIO0
PA7	41	SM_CPLD_GPIO1
UART0_TX(PA1)	34	SM_IPMC_RX
UART3_TX(PB1)	38	SM_ZYNQ_RX
I2C_SCL0	91	SM_MASTER_I2C_SCL
UART7_TX(PA3)	24	MON_UART_TO_SM



ZERO-OHM RESISTORS ON PIN 4 AND PIN 20 ARE PLACED ADJACENT TO EACH OTHER. IF "TX" AND "RX" NEED TO BE SWAPPED, REMOVE AND ROTATE THE JUMPERS BY 90 DEGREES.

THE SAME IS TRUE FOR THE RESISTORS ON PIN 5 AND PIN 21.

IN ROW 2, PINS 1, 4, 6, AND 8 ARE "GND" ON SMv1. A CMv2 BOARD MUST BE ABLE TO TOLERATE A HARD GND CONNECTION ON THESE PINS IN CASE IT IS CONNECTED TO AN SMv1.

IF THE MCU IS DRIVING AN OUTPUT HIGH, AND THE SIGNAL IS SHORTED TO GND, A 270 OHM RESISTOR WILL LIMIT THE CURRENT TO 12 MA. THE RESISTOR POWER WILL BE 0.04 WATTS.

TM4C1290 I2C ADDRESS:
ASSIGN A SLAVE ADDRESS TO THIS DEVICE BY WRITING A VALUE INTO THE "I2CSOAR" REGISTER.

TM4C SLAVE I2C ADDR = 0X40

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.01: SM POWER CONNECTOR		
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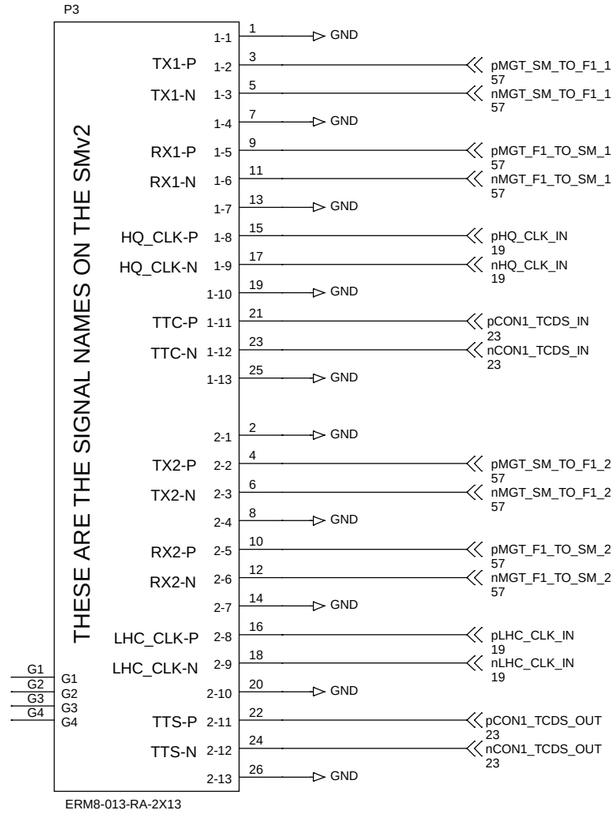
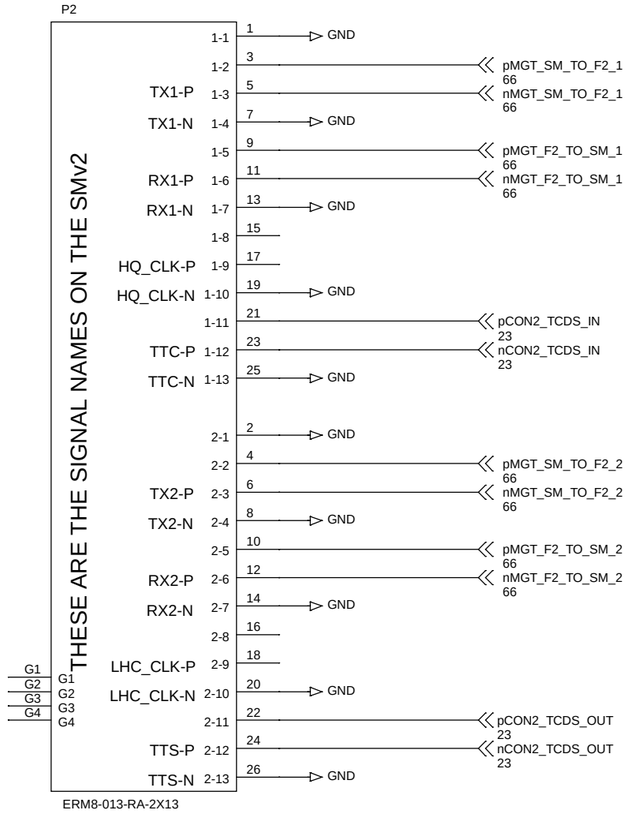
2.02: SM HIGH SPEED CONNECTORS

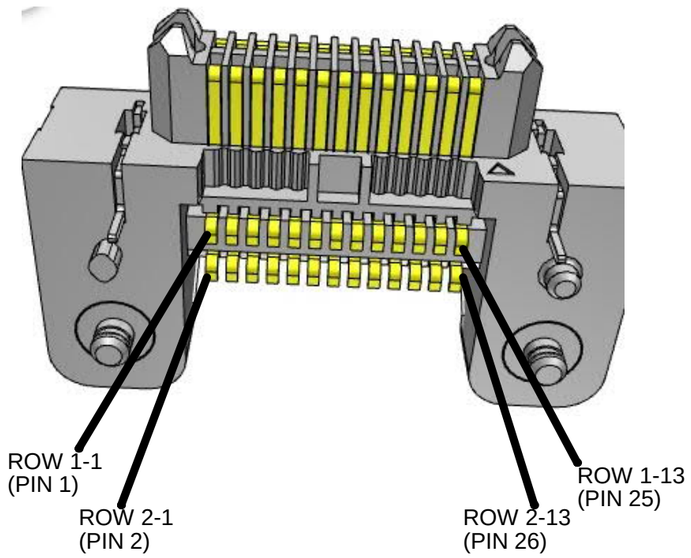
THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. AC COUPLING CAPACITORS ARE ASSUMED TO BE ON THE SM.

FPGA#1 AND BACKPLANE CLOCK SIGNALS



FPGA#2 SIGNALS





ERM8-013-01-L-D-RA-DS

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.02: SM HIGH SPEED CONNECTORS		
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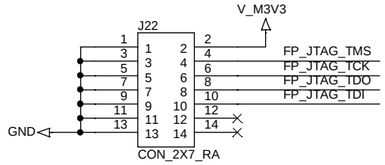
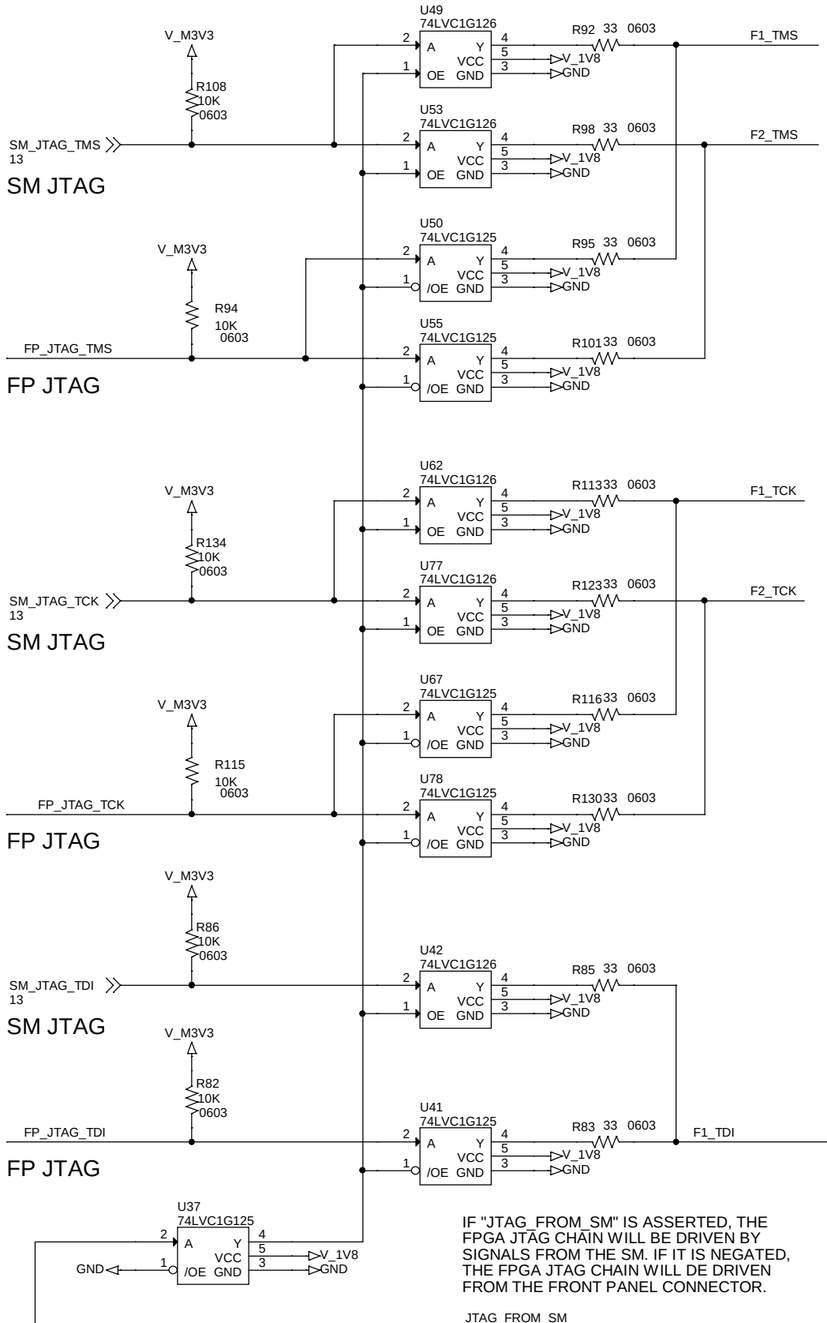
2.03: MCU AND FPGA JTAG

THE FPGA JTAG REFERENCE IS 3.3 VOLTS.



FRONT PANEL
FPGA JTAG



IF "JTAG_FROM_SM" IS ASSERTED, THE FPGA JTAG CHAIN WILL BE DRIVEN BY SIGNALS FROM THE SM. IF IT IS NEGATED, THE FPGA JTAG CHAIN WILL DE DRIVEN FROM THE FRONT PANEL CONNECTOR.

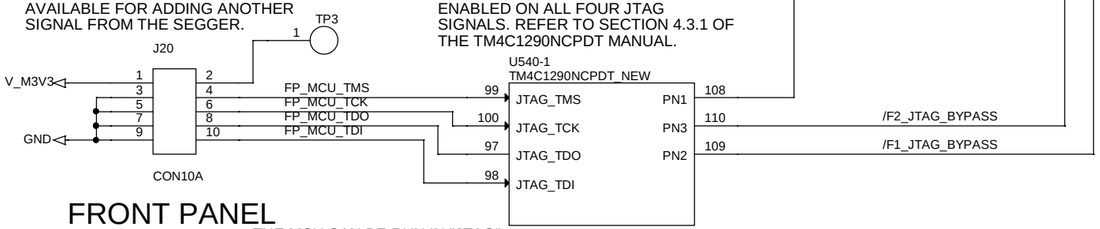
JTAG_FROM_SM

THE TEST POINT ON PIN 2 IS AVAILABLE FOR ADDING ANOTHER SIGNAL FROM THE SEGGER.

THE MCU HAS INTERNAL PULLUPS ENABLED ON ALL FOUR JTAG SIGNALS. REFER TO SECTION 4.3.1 OF THE TM4C1290NCPDT MANUAL.

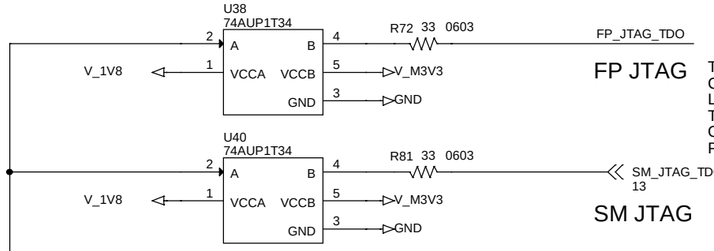
THE MCU CONNECTOR ON THE FRONT PANEL IS A 10-PIN 50-MIL PITCH CONNECTOR. A SEGGER MODEL 8.06.28 "50-MIL 10-PIN PATCH ADAPTER" IS USED AT THE PROGRAMMER.

THE MCU JTAG REFERENCE IS 3.3 VOLTS.

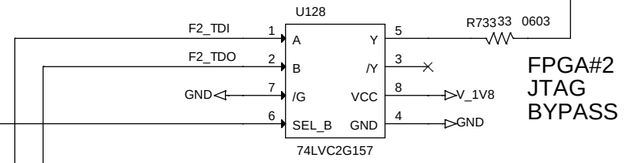


FRONT PANEL
MCU JTAG

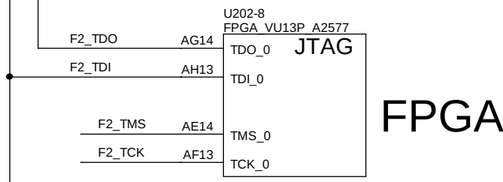
THE MCU CAN BE RUN IN "JTAG" MODE OR "ARM SWD" MODE.



THESE VOLTAGE TRANSLATORS CONVERT THE 1.8 VOLT LOGIC LEVEL FROM THE LAST FPGA TO THE 3.3 VOLT LOGIC LEVEL USED ON THE SM OR THE EXTERNAL PROGRAMMER.

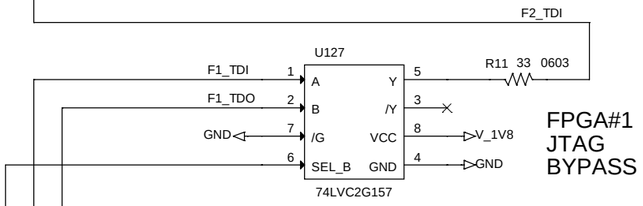


FPGA#2
JTAG
BYPASS

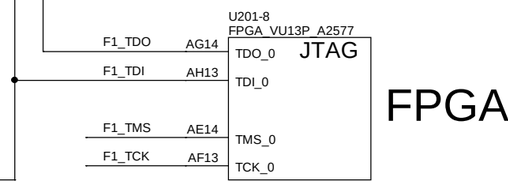


FPGA#2

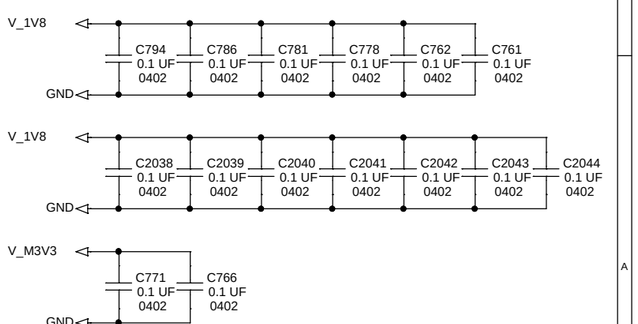
F2_TDI



FPGA#1
JTAG
BYPASS



FPGA#1



APOLLO CM W/ DUAL A2577, MK1

Title: 2.03: MCU AND FPGA JTAG

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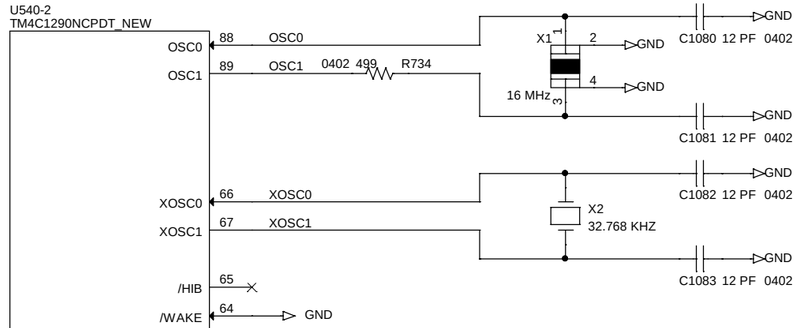
2.04: MCU I/O AND POWER

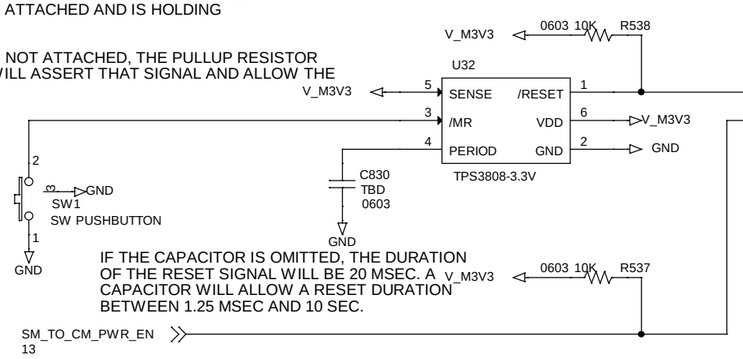


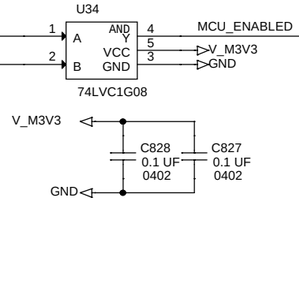
AS PER TABLE 25.7 OF THE TM4C1290 MANUAL, THE UNUSED "/WAKE" PIN GET TIED TO GND AND "/HIB" IS NC.

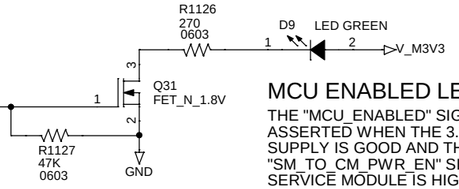
THE ACTIVE-LO "/RESET" INPUT WILL BE ASSERTED WHEN ANY OF THE FOLLOWING ARE TRUE:
1) POWER HAS JUST BEEN APPLIED
2) THE FRONT-PANEL RESET SWITCH HAS BEEN ACTIVATED
3) THE SERVICE MODULE IS ATTACHED AND IS HOLDING "SM_TO_CM_PWR_EN" LO.

IF THE SERVICE MODULE IS NOT ATTACHED, THE PULLUP RESISTOR ON"SM_TO_CM_PWR_EN" WILL ASSERT THAT SIGNAL AND ALLOW THE BOARD TO POWER UP.

FRONT PANEL RESET



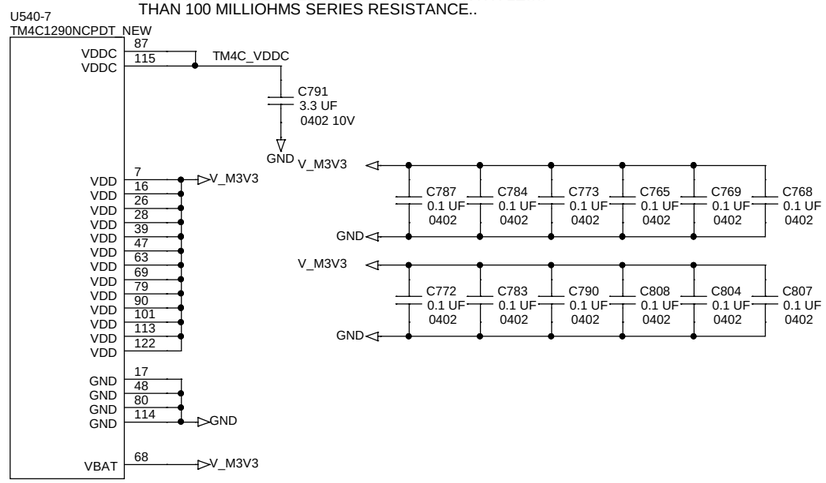




MCU ENABLED LED

THE "MCU_ENABLED" SIGNAL WILL BE ASSERTED WHEN THE 3.3V MANAGEMENT SUPPLY IS GOOD AND THE "SM_TO_CM_PWR_EN" SIGNAL FROM THE SERVICE MODULE IS HIGH.

AS PER TABLE 26.15 OF THE TM4C1290 MANUAL, THE "VDDC" PINS GET TIED TOGETHER AND CONNECTED TO A CAPACITOR BETWEEN 2.5 UF AND 4 UF WITH LESS THAN 100 MILLIOHMS SERIES RESISTANCE..



AS PER TABLE 25.7 OF THE TM4C1290 MANUAL, THE UNUSED "VBAT" PIN GET TIED TO VDD.

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Title: 2.04: MCU I/O AND POWER		
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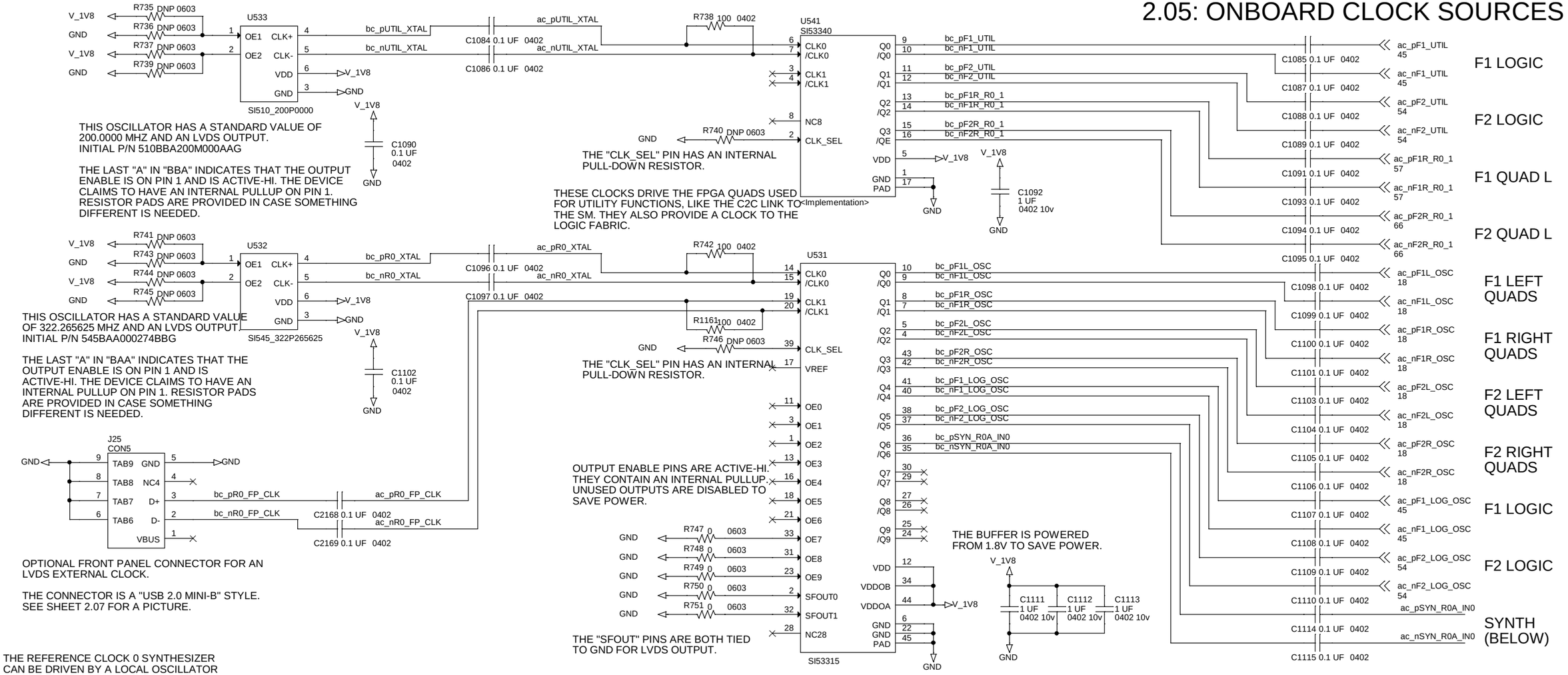
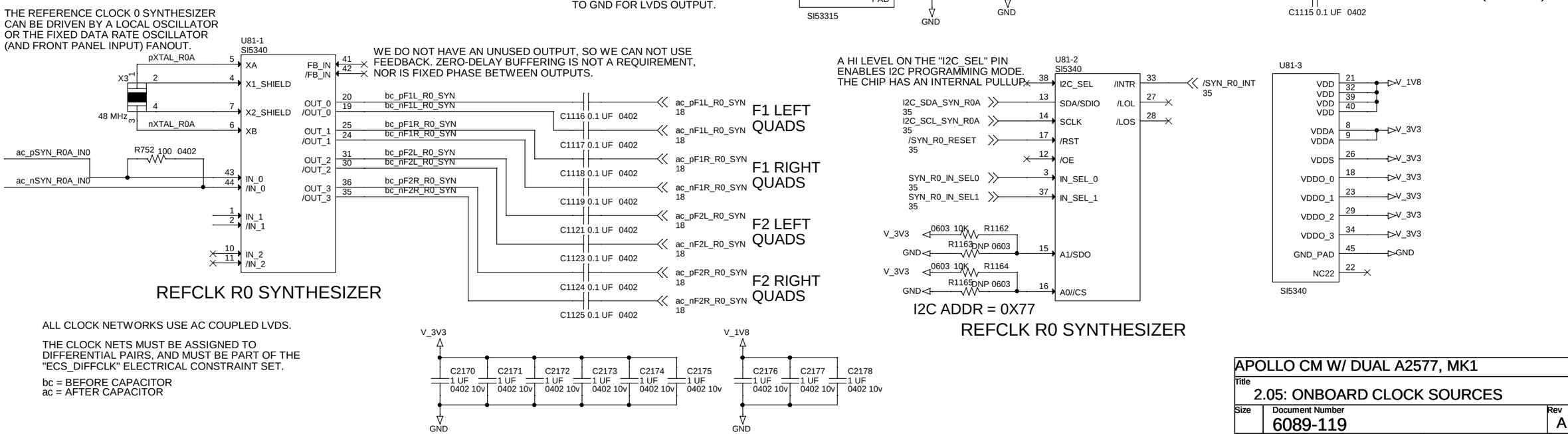
2.05: ONBOARD CLOCK SOURCES





APOLLO CM W/ DUAL A2577, MK1	
Title	2.05: ONBOARD CLOCK SOURCES
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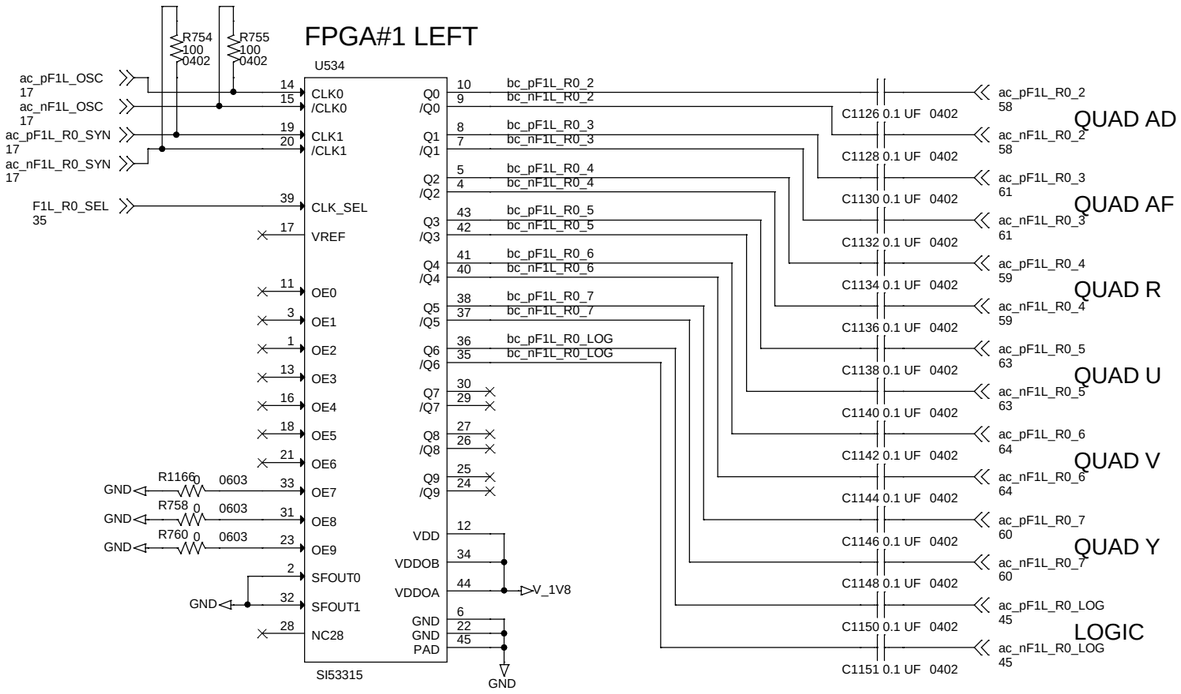
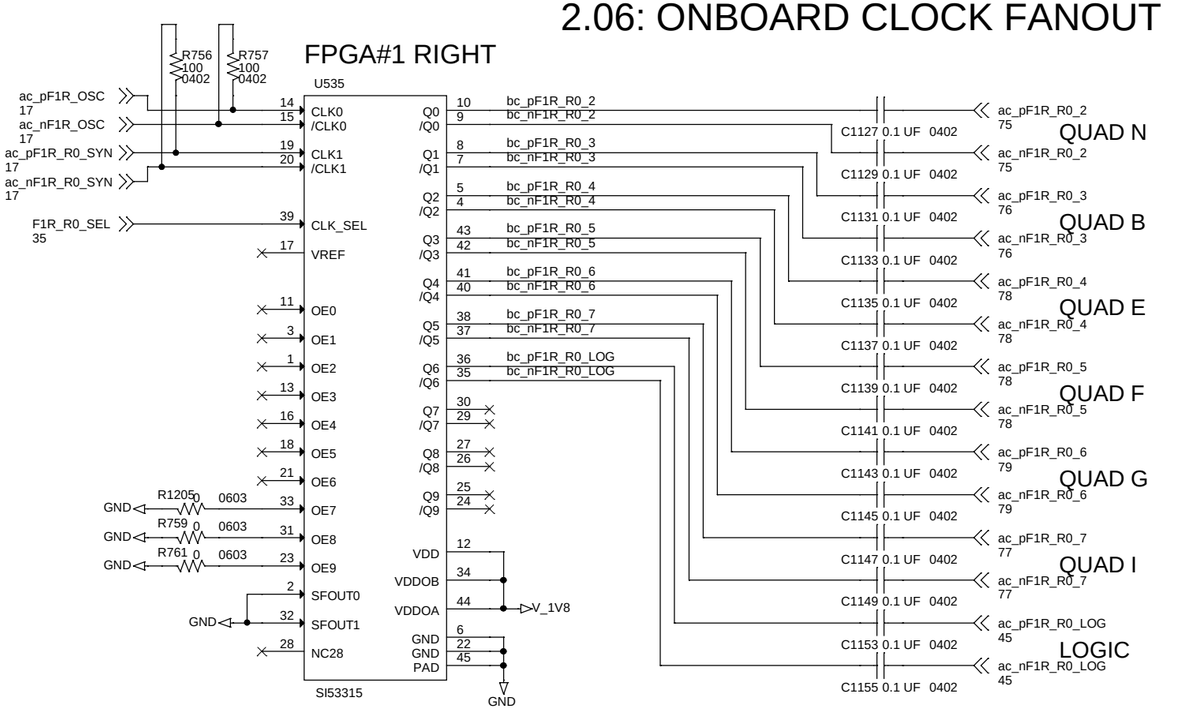
2.06: ONBOARD CLOCK FANOUT

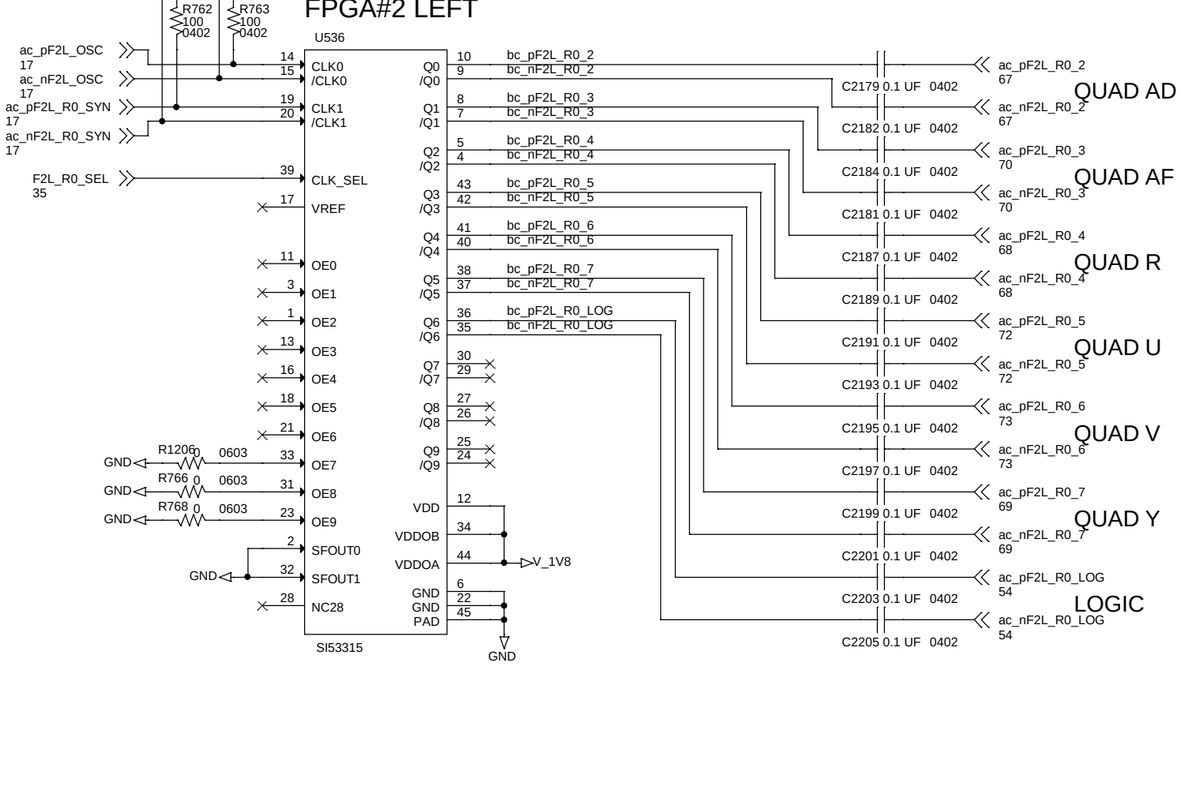
FPGA#1 LEFT



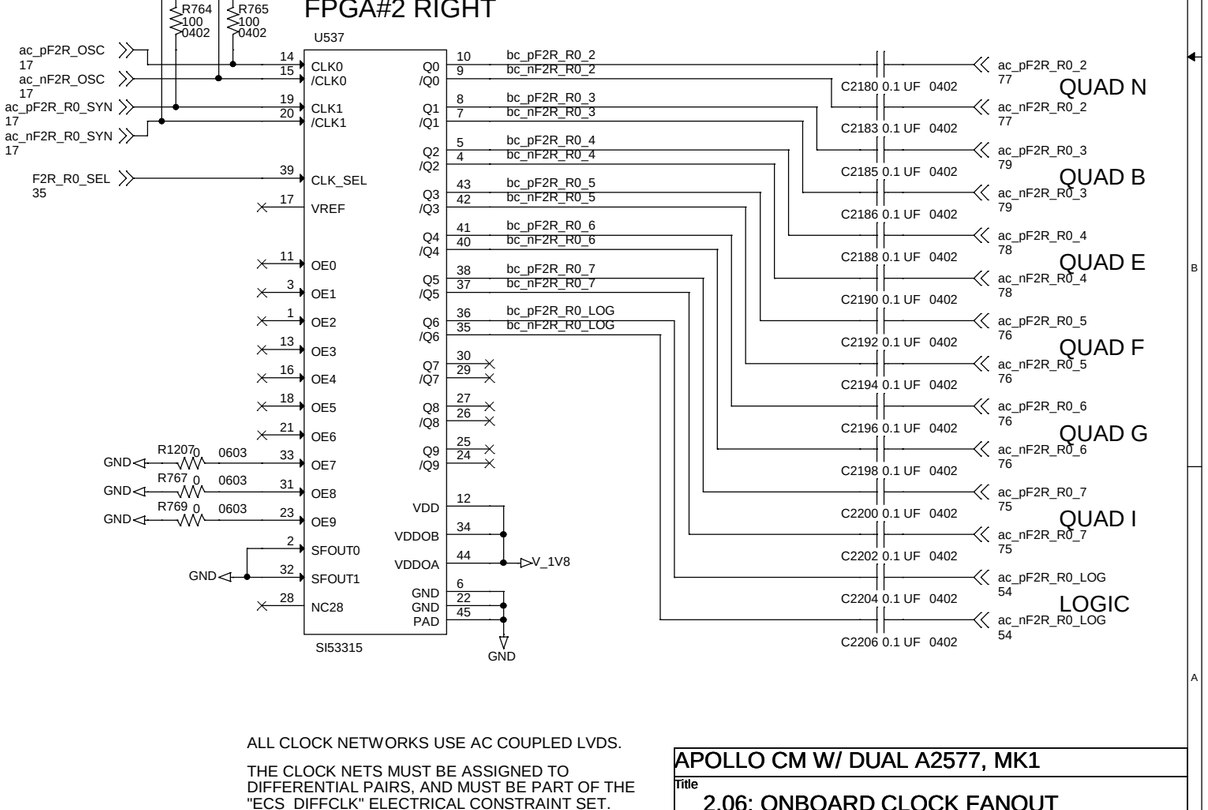
FPGA#1 RIGHT



FPGA#2 LEFT



FPGA#2 RIGHT



ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1

Title: 2.06: ONBOARD CLOCK FANOUT

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2.07: EXTERNAL REFCLK SYNTH R1A

U599-1
SI5341

X4 48 MHz
pXTAL_R1A → 8 XA
2 → 7 X1_SHIELD
4 → 10 X2_SHIELD
nXTAL_R1A → 9 XB

IF THE HQ_CLK OF LHC_CLK IS AC-COUPLED ON THE SM, USE ZERO-OHM RESISTORS ON THESE CAPACITOR PADS.

HQ_CLK

320 MHZ IF FPGA#1 IS TCDS ENDPOINT.
40 MHZ IF SM IS TCDS ENDPOINT

pHQ_CLK_IN 14 → ac_pHQ_CLK_IN → C2209 0.1 UF 0402 → R1167 100 0402 → 63 IN_0
nHQ_CLK_IN 14 → ac_nHQ_CLK_IN → C2213 0.1 UF 0402 → 64 /IN_0

LHC_CLK

ALWAYS 40 MHZ

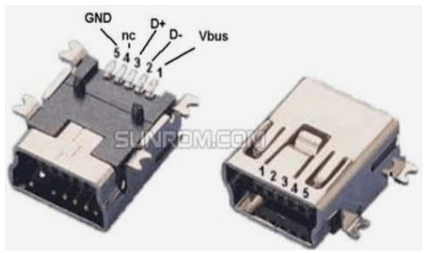
pLHC_CLK_IN 14 → ac_pLHC_CLK_IN → C2216 0.1 UF 0402 → R1168 100 0402 → 1 IN_1
nLHC_CLK_IN 14 → ac_nLHC_CLK_IN → C2218 0.1 UF 0402 → 2 /IN_1

J26
CON5

GND	9 TAB9	GND 5	GND
	8 TAB8	NC4 4	
bc_pR1_FP_CLK	7 TAB7	D+ 3	ac_pR1_FP_CLK → C2221 0.1 UF 0402 → R1169 100 0402 → 14 IN_2
bc_nR1_FP_CLK	6 TAB6	D- 2	ac_nR1_FP_CLK → C2223 0.1 UF 0402 → 15 /IN_2
		VBUS 1	

OPTIONAL FRONT PANEL CONNECTOR FOR AN LVDS EXTERNAL CLOCK.

THE CONNECTOR IS A "USB 2.0 MINI-B" STYLE.



ZERO-DELAY FEEDBACK
320 MHZ IF FPGA#1 IS TCDS ENDPOINT.
40 MHZ IF SM IS TCDS ENDPOINT

ac_pR1A_FB → C2229 0.1 UF 0402 → R1170 100 0402 → 61 FB_IN
ac_nR1A_FB → C2230 0.1 UF 0402 → 62 /FB_IN

U599-1 SI5341			
OUT_0	24	bc_pF1L_R0_1 → C2210 0.1 UF 0402	ac_pF1L_R0_1 23
/OUT_0	23	bc_nF1L_R0_1 → C2207 0.1 UF 0402	ac_nF1L_R0_1 23
OUT_1	28	bc_pF2L_R0_1 → C2211 0.1 UF 0402	ac_pF2L_R0_1 23
/OUT_1	27	bc_nF2L_R0_1 → C2208 0.1 UF 0402	ac_nF2L_R0_1 23
OUT_2	31	bc_pSYN_R1B_IN0 → C2212 0.1 UF 0402	ac_pSYN_R1B_IN0 20
/OUT_2	30	bc_nSYN_R1B_IN0 → C2214 0.1 UF 0402	ac_nSYN_R1B_IN0 20
OUT_3	35	bc_pSYN_R1C_IN0 → C2215 0.1 UF 0402	ac_pSYN_R1C_IN0 21
/OUT_3	34	bc_nSYN_R1C_IN0 → C2217 0.1 UF 0402	ac_nSYN_R1C_IN0 21
OUT_4	38	bc_pF1L_R1_3 → C2219 0.1 UF 0402	ac_pF1L_R1_3 61
/OUT_4	37	bc_nF1L_R1_3 → C2220 0.1 UF 0402	ac_nF1L_R1_3 61
OUT_5	42	bc_pF1L_R1_5 → C2222 0.1 UF 0402	ac_pF1L_R1_5 63
/OUT_5	41	bc_nF1L_R1_5 → C2224 0.1 UF 0402	ac_nF1L_R1_5 63
OUT_6	45	bc_pF2L_R1_3 → C2225 0.1 UF 0402	ac_pF2L_R1_3 70
/OUT_6	44	bc_nF2L_R1_3 → C2226 0.1 UF 0402	ac_nF2L_R1_3 70
OUT_7	51	bc_pF2L_R1_5 → C2227 0.1 UF 0402	ac_pF2L_R1_5 72
/OUT_7	50	bc_nF2L_R1_5 → C2228 0.1 UF 0402	ac_nF2L_R1_5 72
OUT_8	54		
/OUT_8	53		
OUT_9	59	bc_pR1A_FB	
/OUT_9	58	bc_nR1A_FB	

F1 QUAD AB (TCDS QUAD)

F2 QUAD AB (TCDS QUAD)

SYN R1B IN0

SYN R1C IN0

F1 QUAD AF

F1 QUAD U (T,U,V)

F2 QUAD AF

F2 QUAD U (T,U,V)

A HI LEVEL ON THE "I2C_SEL" PIN ENABLES I2C PROGRAMMING MODE. THE CHIP HAS AN INTERNAL PULLUP.

U599-2

	39 I2C_SEL	/INTR 12	/SYN_R1A_INT 35
I2C_SDA_SYN_R1A 35	18 SDA/SDIO	/LOL 47	
I2C_SCL_SYN_R1A 35	16 SCLK		
/SYN_R1A_RESET 35	6 /RST		
	11 /OE		
SYN_R1A_IN_SEL0 35	3 IN_SEL_0		
SYN_R1A_IN_SEL1 35	4 IN_SEL_1		
	48 FINC		
	25 FDEC		
	5 /SYNC		

V_M3V3 → 0603 10K R1171 → A1/SDO 17
GND → R1172 DNP 0603 → A1/SDO 17
V_M3V3 → 0603 10K R1173 → A0//CS 19
GND → R1174 DNP 0603 → A0//CS 19

I2C ADDR = 0X77

SI5341

U599-3

VDD	32	V_1V8
VDD	46	V_1V8
VDD	60	V_1V8
VDDA	13	V_3V3
VDDO_0	22	V_1V8
VDDO_1	26	
VDDO_2	29	
VDDO_3	33	
VDDO_4	36	
VDDO_5	40	
VDDO_6	43	
VDDO_7	49	
VDDO_8	52	
VDDO_9	57	
GND_PAD	65	GND
NC20	20	
NC21	21	
NC55	55	
NC56	56	

SI5341

V_3V3 → C2231 1 UF 0402 10v → GND

PLACE 3V3 BYPASS CAPS NEAR PIN 13

V_1V8 → C2232 1 UF 0402 10v, C2233 1 UF 0402 10v, C2234 1 UF 0402 10v, C2235 1 UF 0402 10v, C2236 1 UF 0402 10v, C2237 1 UF 0402 10v, C2238 1 UF 0402 10v, C2239 1 UF 0402 10v → GND

TWO 1V8 BYPASS CAPS ALONG EACH EDGE

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1

Title: 2.07: EXTERNAL REFCLK SYNTH R1A

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2.08: EXTERNAL REFCLK SYNTH R1B

U597-1
SI5341

pXTAL_R1B → 8 XA
X5 (48 MHz): 2 → 7 X1_SHIELD; 4 → 10 X2_SHIELD
nXTAL_R1B → 9 XB

SYN R1B IN0

ac_pSYN_R1B_IN0 (19) → R1175 100 0402 → 63 IN_0
ac_nSYN_R1B_IN0 (19) → 64 /IN_0

TCDS RECOVERED CLOCK
ALWAYS 40 MHZ

bc_pF1_TCDS_REC_CLK (45) → C2247 0.1 UF 0402 → ac_pF1_TCDS_REC_CLK → R1176 100 0402 → 1 IN_1
bc_nF1_TCDS_REC_CLK (45) → C2249 0.1 UF 0402 → ac_nF1_TCDS_REC_CLK → 2 /IN_1

14 IN_2
15 /IN_2

ZERO-DELAY FEEDBACK
320 MHZ IF FPGA#1 IS TCDS ENDPOINT.
40 MHZ IF SM IS TCDS ENDPOINT

ac_pR1b_FB → C2260 0.1 UF 0402 → R1177 100 0402 → 61 FB_IN
ac_nR1b_FB → C2261 0.1 UF 0402 → 62 /FB_IN

OUT_0	24	bc_pF1L_R1_1	C2240 0.1 UF 0402	ac_pF1L_R1_1	23
/OUT_0	23	bc_nF1L_R1_1	C2241 0.1 UF 0402	ac_nF1L_R1_1	23
OUT_1	28	bc_pF1_TCDS40_IN	C2242 0.1 UF 0402	ac_pF1_TCDS40_IN	45
/OUT_1	27	bc_nF1_TCDS40_IN	C2243 0.1 UF 0402	ac_nF1_TCDS40_IN	45
OUT_2	31	bc_pF1L_R1_2	C2244 0.1 UF 0402	ac_pF1L_R1_2	58
/OUT_2	30	bc_nF1L_R1_2	C2245 0.1 UF 0402	ac_nF1L_R1_2	58
OUT_3	35	bc_pF1L_R1_4	C2246 0.1 UF 0402	ac_pF1L_R1_4	59
/OUT_3	34	bc_nF1L_R1_4	C2248 0.1 UF 0402	ac_nF1L_R1_4	59
OUT_4	38	bc_pF1L_R1_7	C2250 0.1 UF 0402	ac_pF1L_R1_7	60
/OUT_4	37	bc_nF1L_R1_7	C2251 0.1 UF 0402	ac_nF1L_R1_7	60
OUT_5	42	bc_pF2_TCDS40_IN	C2252 0.1 UF 0402	ac_pF2_TCDS40_IN	54
/OUT_5	41	bc_nF2_TCDS40_IN	C2253 0.1 UF 0402	ac_nF2_TCDS40_IN	54
OUT_6	45	bc_pF2L_R1_2	C2254 0.1 UF 0402	ac_pF2L_R1_2	67
/OUT_6	44	bc_nF2L_R1_2	C2255 0.1 UF 0402	ac_nF2L_R1_2	67
OUT_7	51	bc_pF2L_R1_4	C2256 0.1 UF 0402	ac_pF2L_R1_4	68
/OUT_7	50	bc_nF2L_R1_4	C2257 0.1 UF 0402	ac_nF2L_R1_4	68
OUT_8	54	bc_pF2L_R1_7	C2258 0.1 UF 0402	ac_pF2L_R1_7	69
/OUT_8	53	bc_nF2L_R1_7	C2259 0.1 UF 0402	ac_nF2L_R1_7	69
OUT_9	59	bc_pR1b_FB			
/OUT_9	58	bc_nR1b_FB			

F1 QUAD AB
(TCDS QUAD)

F1 LOGIC
TCDS 40MHZ INPUT

F1 QUAD AD (AC,AD,AE)

F1 QUAD Q (Q,R,S)

F1 QUAD U (T,U,V)

F2 LOGIC
TCDS 40MHZ INPUT

F2 QUAD AD (AC,AD,AE)

F2 QUAD Q (Q,R,S)

F2 QUAD U (T,U,V)

A HI LEVEL ON THE "I2C_SEL" PIN
ENABLES I2C PROGRAMMING MODE.
THE CHIP HAS AN INTERNAL PULLUP.

U597-2

39	I2C_SEL	/INTR	12 → /SYN_R1B_INT (35)
I2C_SDA_SYN_R1B (35) 18	SDA/SDIO	/LOL	47
I2C_SCL_SYN_R1B (35) 16	SCLK		
/SYN_R1B_RESET (35) 6	/RST		
11	/OE		
SYN_R1B_IN_SEL0 (35) 3	IN_SEL_0		
SYN_R1B_IN_SEL1 (35) 4	IN_SEL_1		
48	FINC		
25	FDEC		
5	/SYNC		

V_3V3 → 0603 10K R1178 → A1/SDO 17
GND → R1179 DNP 0603 → A1/SDO 17
V_3V3 → 0603 10K R1180 → A0//CS 19
GND → R1181 DNP 0603 → A0//CS 19

I2C ADDR = 0X77

SI5341

U597-3

VDD	32	V_1V8
VDD	46	
VDD	60	
VDDA	13	V_3V3
VDDO_0	22	V_1V8
VDDO_1	26	
VDDO_2	29	
VDDO_3	33	
VDDO_4	36	
VDDO_5	40	
VDDO_6	43	
VDDO_7	49	
VDDO_8	52	
VDDO_9	57	
GND_PAD	65	GND
NC20	20	
NC21	21	
NC55	55	
NC56	56	

SI5341

V_3V3 → C2262 1 UF 0402 10v → GND

PLACE 3V3 BYPASS CAPS NEAR PIN 13

V_1V8 → C2263 1 UF 0402 10v, C2264 1 UF 0402 10v, C2265 1 UF 0402 10v, C2266 1 UF 0402 10v, C2267 1 UF 0402 10v, C2268 1 UF 0402 10v, C2269 1 UF 0402 10v, C2270 1 UF 0402 10v → GND

TWO 1V8 BYPASS CAPS ALONG EACH EDGE

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1			
Title: 2.08: EXTERNAL REFCLK SYNTH R1B			
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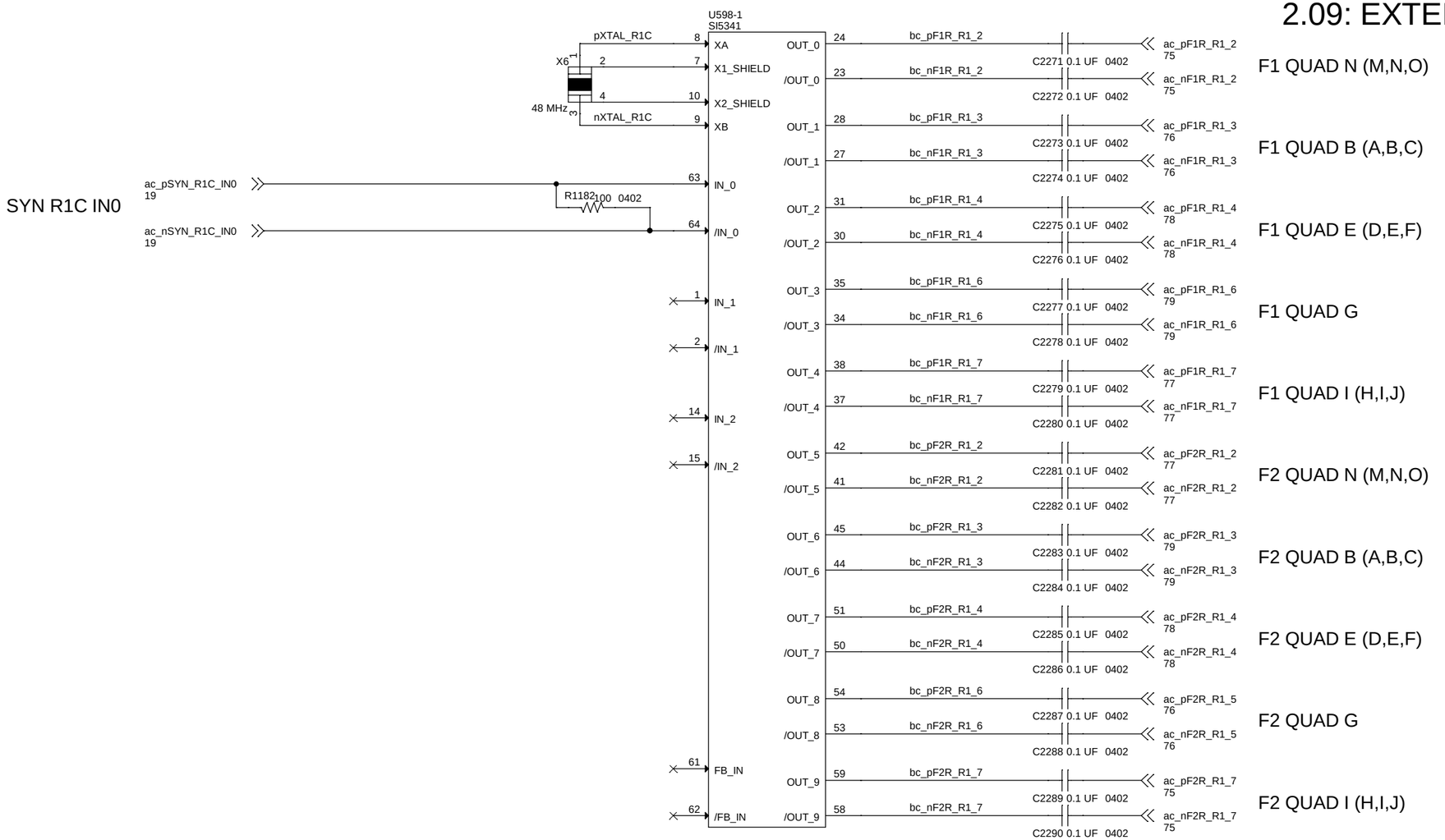
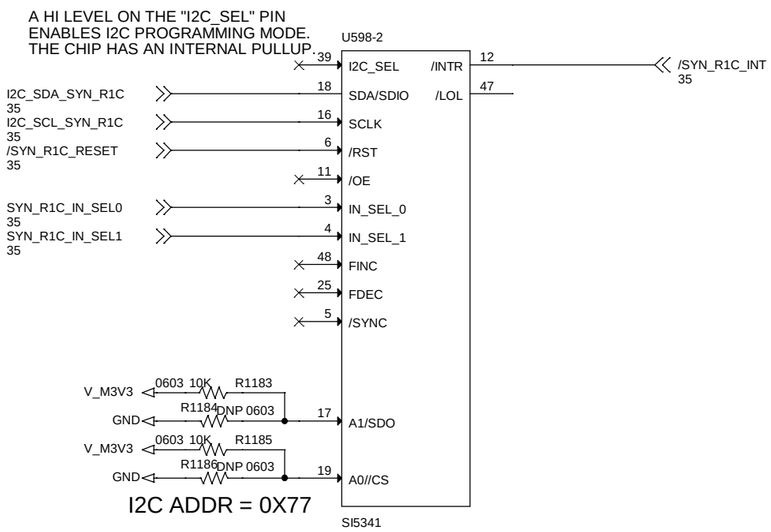
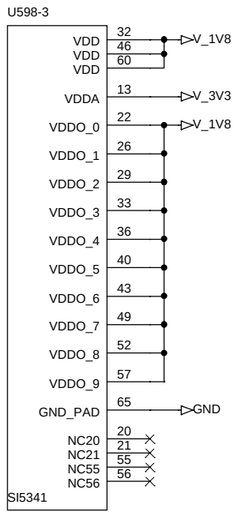
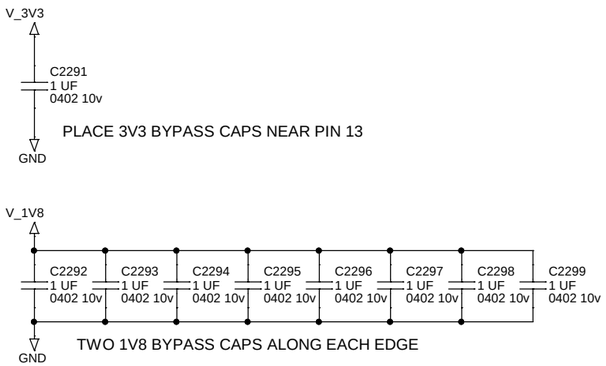
2.09: EXTERNAL REFCLK SYNTH R1C









ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.09: EXTERNAL REFCLK SYNTH R1C		
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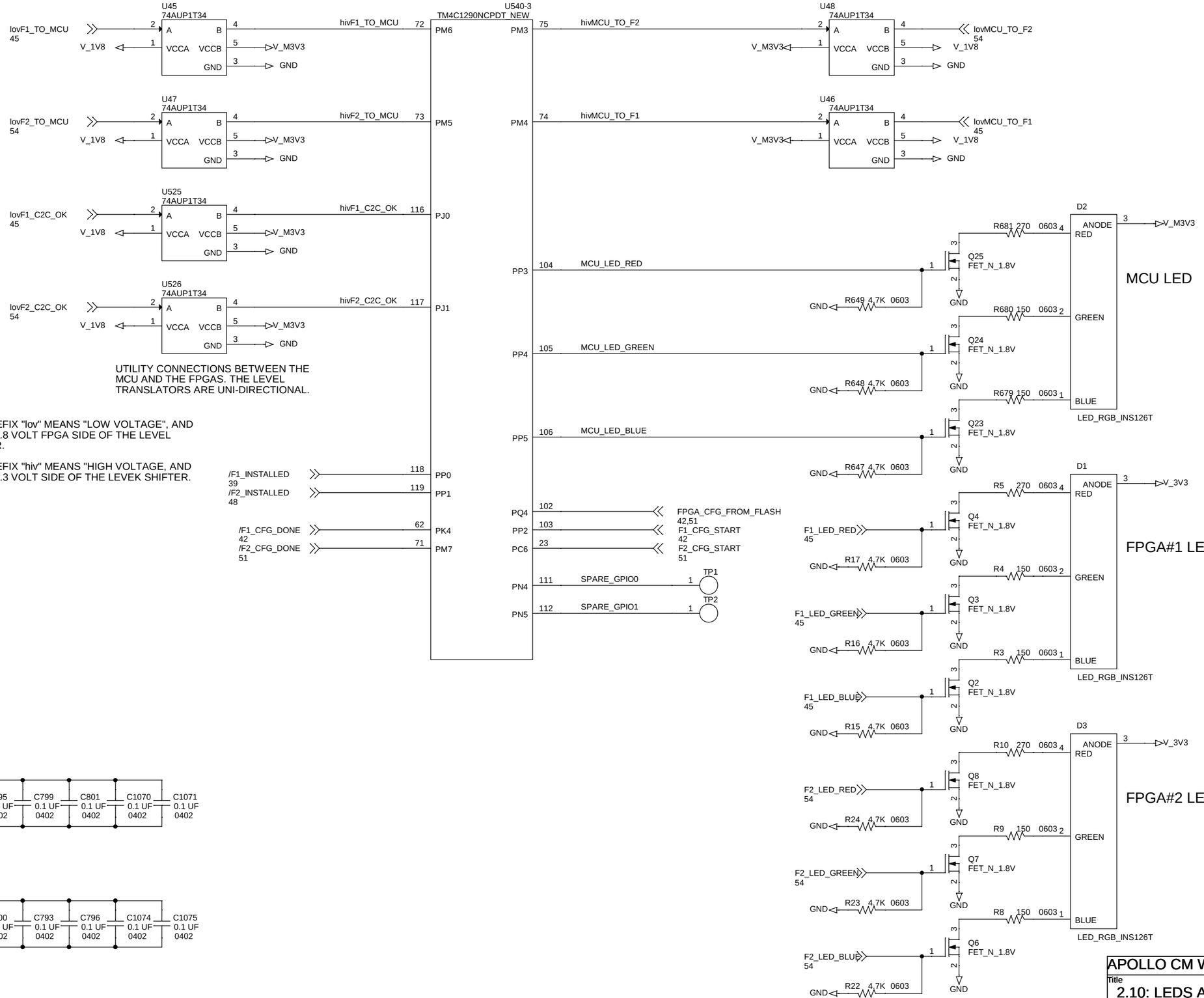
2.10: LEDS AND LEVEL SHIFTERS



APOLLO CM W/ DUAL A2577, MK1		
Title: 2.10: LEDS AND LEVEL SHIFTERS		
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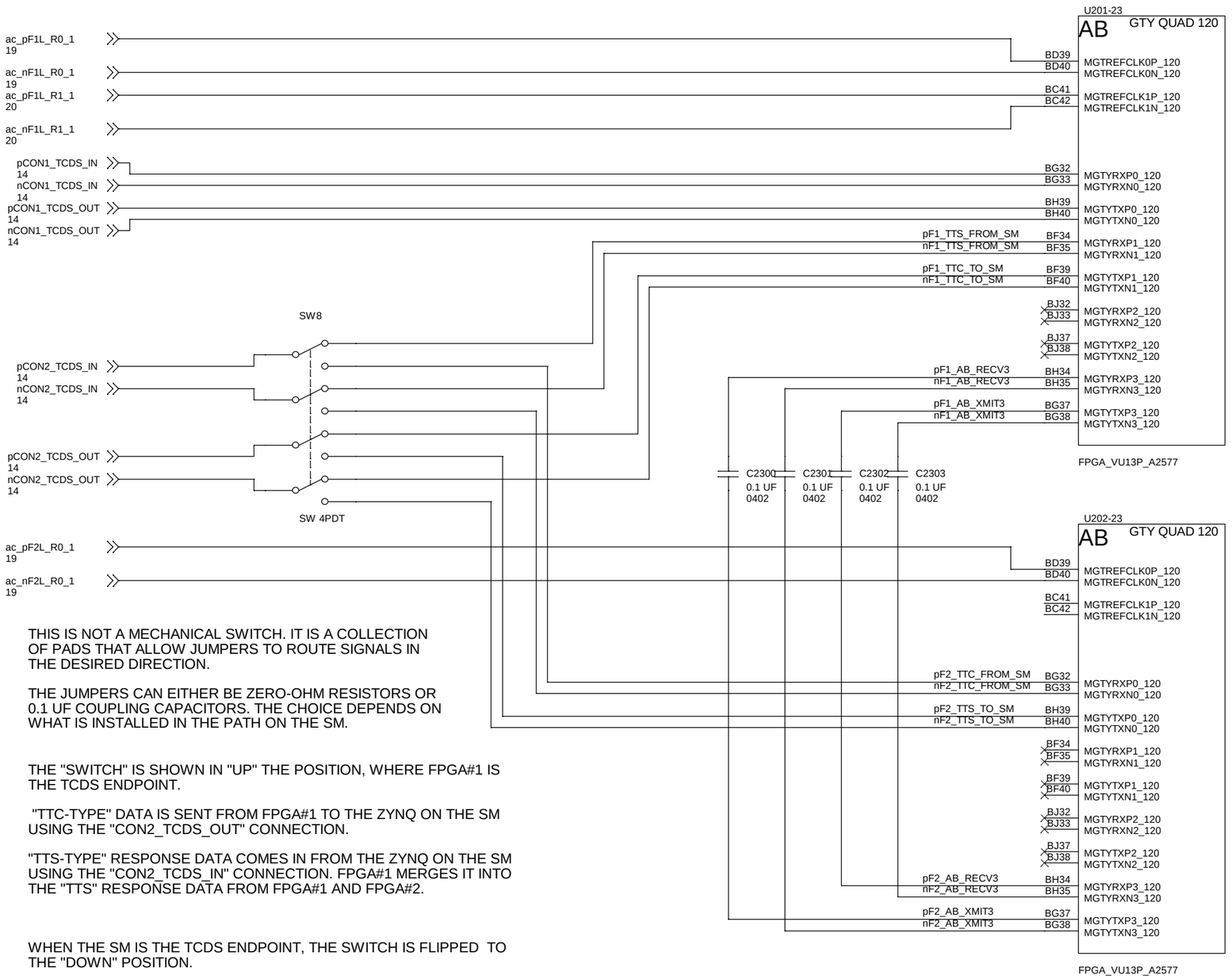
2.11: FPGA#1 AND FPGA#2 TCDS QUADS AB

THESE QUADS ARE DEDICATED TO TCDS SIGNALS. TCDS NETS COME FROM THE SERVICE BOARD HIGH SPEED CONNECTORS

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.



FPGA#1

FPGA#2

THIS IS NOT A MECHANICAL SWITCH. IT IS A COLLECTION OF PADS THAT ALLOW JUMPERS TO ROUTE SIGNALS IN THE DESIRED DIRECTION.

THE JUMPERS CAN EITHER BE ZERO-OHM RESISTORS OR 0.1 UF COUPLING CAPACITORS. THE CHOICE DEPENDS ON WHAT IS INSTALLED IN THE PATH ON THE SM.

THE "SWITCH" IS SHOWN IN "UP" THE POSITION, WHERE FPGA#1 IS THE TCDS ENDPOINT.

"TTC-TYPE" DATA IS SENT FROM FPGA#1 TO THE ZYNQ ON THE SM USING THE "CON2_TCDS_OUT" CONNECTION.

"TTS-TYPE" RESPONSE DATA COMES IN FROM THE ZYNQ ON THE SM USING THE "CON2_TCDS_IN" CONNECTION. FPGA#1 MERGES IT INTO THE "TTS" RESPONSE DATA FROM FPGA#1 AND FPGA#2.

WHEN THE SM IS THE TCDS ENDPOINT, THE SWITCH IS FLIPPED TO THE "DOWN" POSITION.

"TTC-TYPE" DATA COMES IN FROM THE ZYNQ ON THE SM USING THE "CON2_TCDS_IN" CONNECTION AND IS ROUTED TO FPGA#2.

"TTS-TYPE" DATA FROM FPGA#2 IS SENT TO THE ZYNQ ON THE SM USING THE "CON2_TCDS_OUT" CONNECTION.

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.11: FPGA#1 AND FPGA#2 TCDS QUADS AB		
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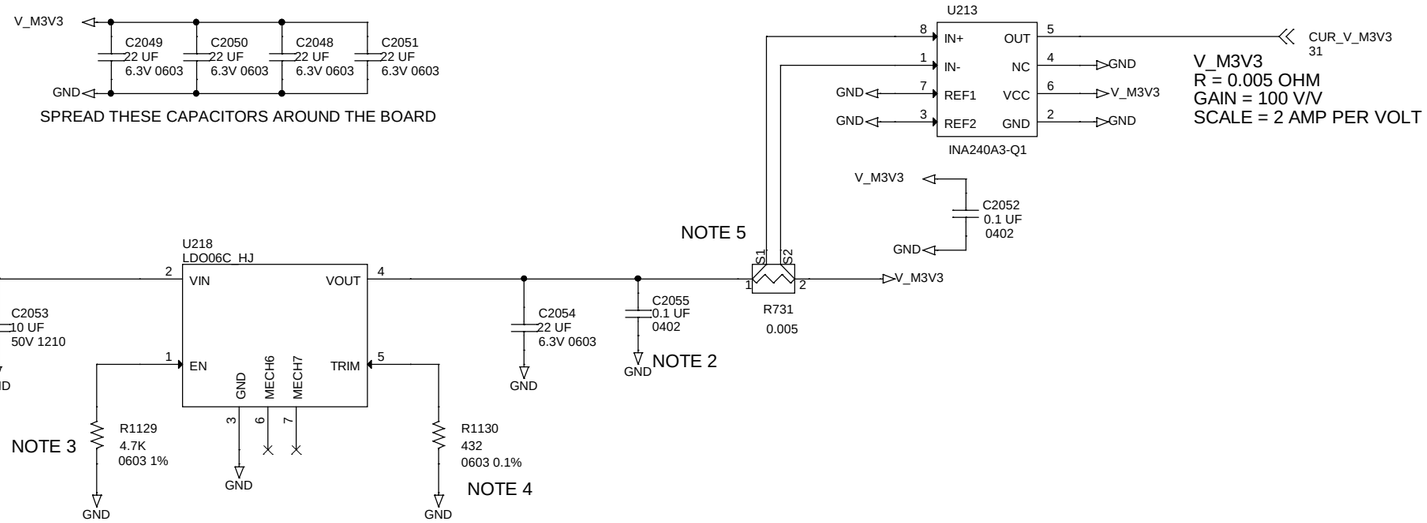
3.01: POWER MANAGEMENT M3V3



GENERAL NOTES:

V_M3V3 IS THE "MANAGEMENT" POWER. IT PROVIDES POWER TO THE POWER SEQUENCING CIRCUIT. IT IS ALWAYS ON WHEN +12V IS SUPPLIED TO THE BOARD.

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

NOTES:

NOTE 1 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL INPUT CAPACITORS.

NOTE 2 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL OUTPUT CAPACITORS.

NOTE 3 UNDERVOLTAGE LOCKOUT RESISTOR
R = 14.81 * (6.81 / ((6.81*Ven) - 18.16))
A 4.7K RESISTOR GIVES 5.8 VOLTS MINIMUM TURNON VOLTAGE

NOTE 4 OUTPUT SETPOINT RESISTOR
R = 1.182 / (VOUT - 0.591)
FOR 3.3 VOLTS, R = 436 OHMS (IF R=432 THEN V=3.327)

NOTE 5 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 5 MILLIOHMS AND A CURRENT OF 5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LDO06C REGULATOR IS RATED FOR 6 AMPS. IF MORE THAN 5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 5 MILLIOHMS.

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.01: POWER MANAGEMENT M3V3		
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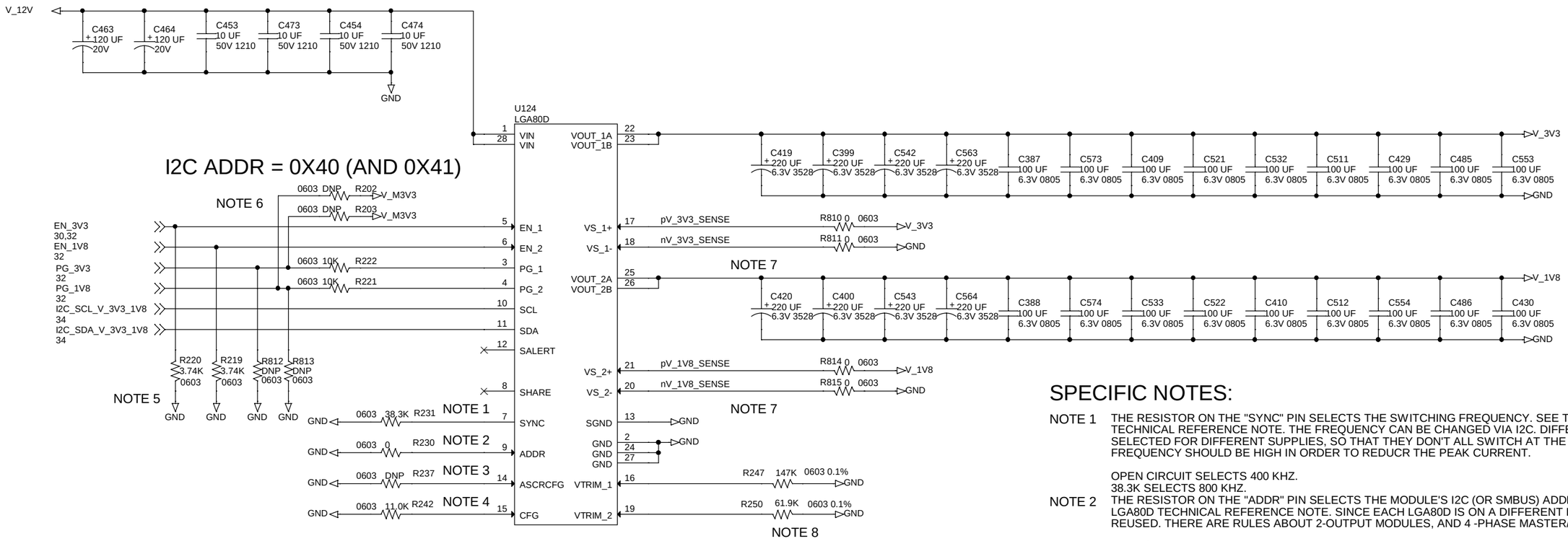
3.02: POWER GLOBAL 3.3V AND 1.8V



SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME. FOR 3.3V, THE FREQUENCY SHOULD BE HIGH IN ORDER TO REDUCR THE PEAK CURRENT.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=11K SELECTS 2-OUTPUT @ 35A(avg)/45A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

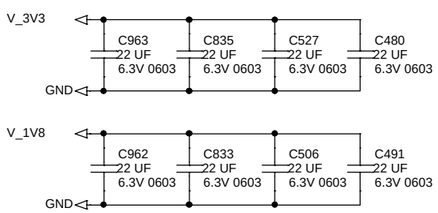
NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 147K FOR 3.3V
RSET = 61.9K FOR 1.8V

NOTE 9 SPREAD THESE CAPACITORS AROUND THE BOARD



NOTE 9

GENERAL NOTES:

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.02: POWER GLOBAL 3.3V AND 1.8V		
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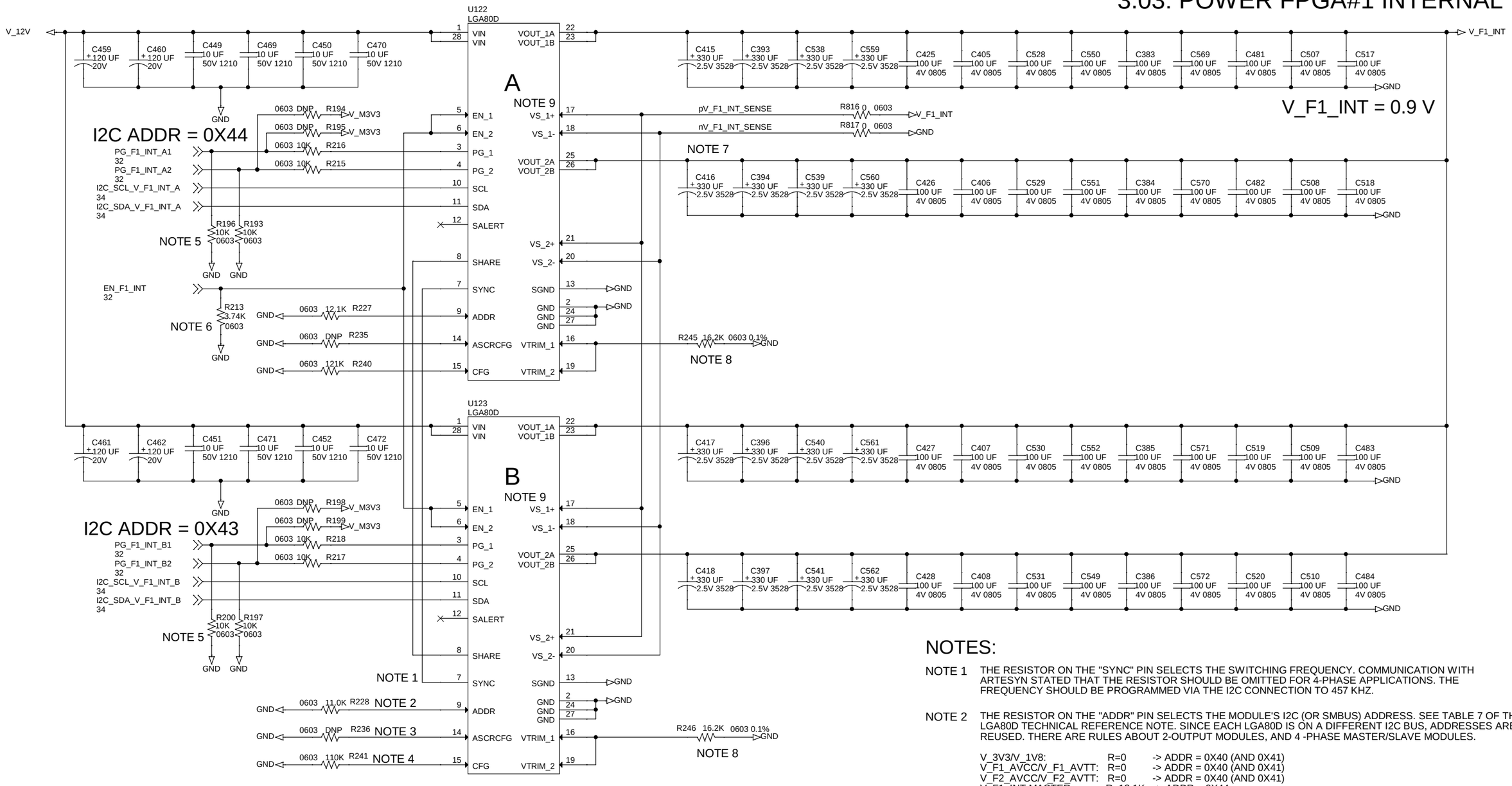
3.03: POWER FPGA#1 INTERNAL



NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. COMMUNICATION WITH ARTESYN STATED THAT THE RESISTOR SHOULD BE OMITTED FOR 4-PHASE APPLICATIONS. THE FREQUENCY SHOULD BE PROGRAMMED VIA THE I2C CONNECTION TO 457 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 10K.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 110K ON THE MASTER AND 121K ON THE SLAVE FOR 4-PHASE @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 16.2K FOR 0.85V

NOTE 9 THE MASTER IS LABELED "A".
THE SLAVE IS LABELED "B".

NOTE 10 PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.03: POWER FPGA#1 INTERNAL		
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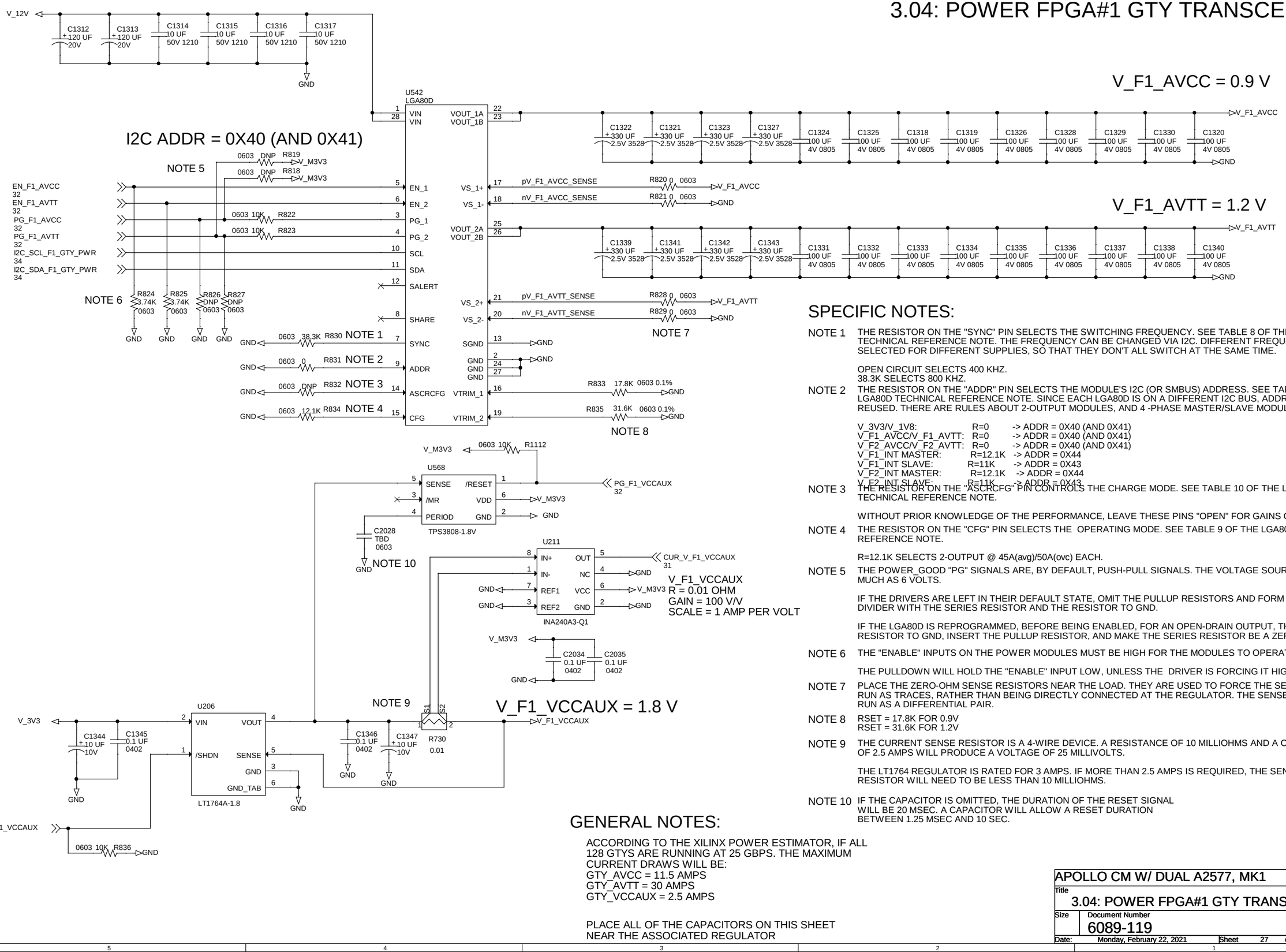
3.04: POWER FPGA#1 GTY TRANSCEIVER



SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=12.1K SELECTS 2-OUTPUT @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 17.8K FOR 0.9V
RSET = 31.6K FOR 1.2V

NOTE 9 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 10 MILLIOHMS AND A CURRENT OF 2.5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LT1764 REGULATOR IS RATED FOR 3 AMPS. IF MORE THAN 2.5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 10 MILLIOHMS.

NOTE 10 IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

GENERAL NOTES:

ACCORDING TO THE XILINX POWER ESTIMATOR, IF ALL 128 GTYS ARE RUNNING AT 25 GBPS. THE MAXIMUM CURRENT DRAWS WILL BE:
GTY_AVCC = 11.5 AMPS
GTY_AVTT = 30 AMPS
GTY_VCCAUX = 2.5 AMPS

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.04: POWER FPGA#1 GTY TRANSCEIVER		
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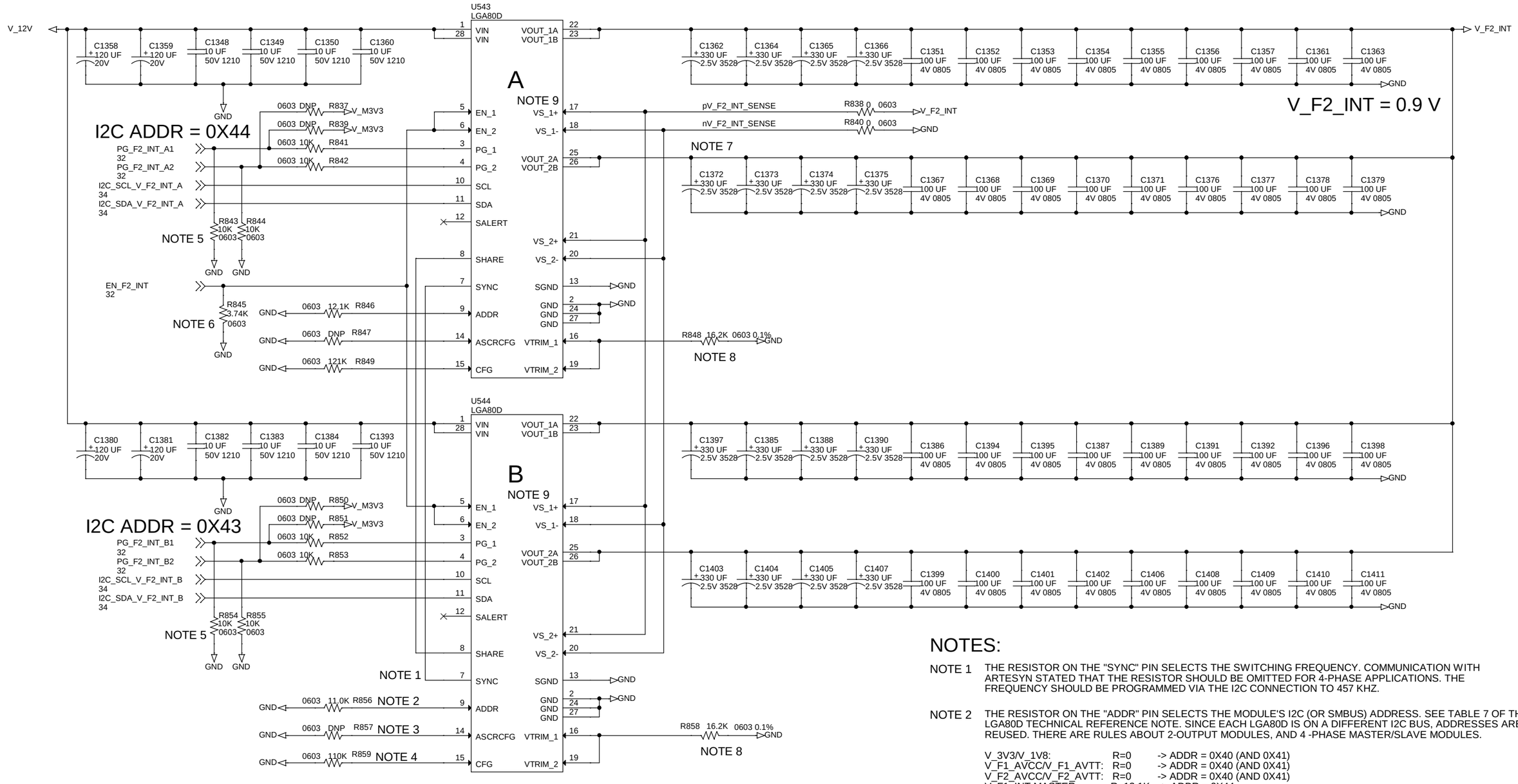
3.05: POWER FPGA#2 INTERNAL



NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. COMMUNICATION WITH ARTESYN STATED THAT THE RESISTOR SHOULD BE OMITTED FOR 4-PHASE APPLICATIONS. THE FREQUENCY SHOULD BE PROGRAMMED VIA THE I2C CONNECTION TO 457 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 10K.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 110K ON THE MASTER AND 121K ON THE SLAVE FOR 4-PHASE @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

NOTE 6 IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER. THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

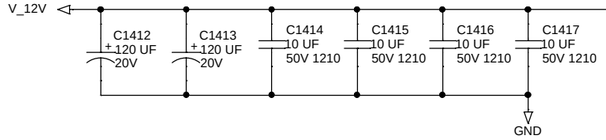
NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

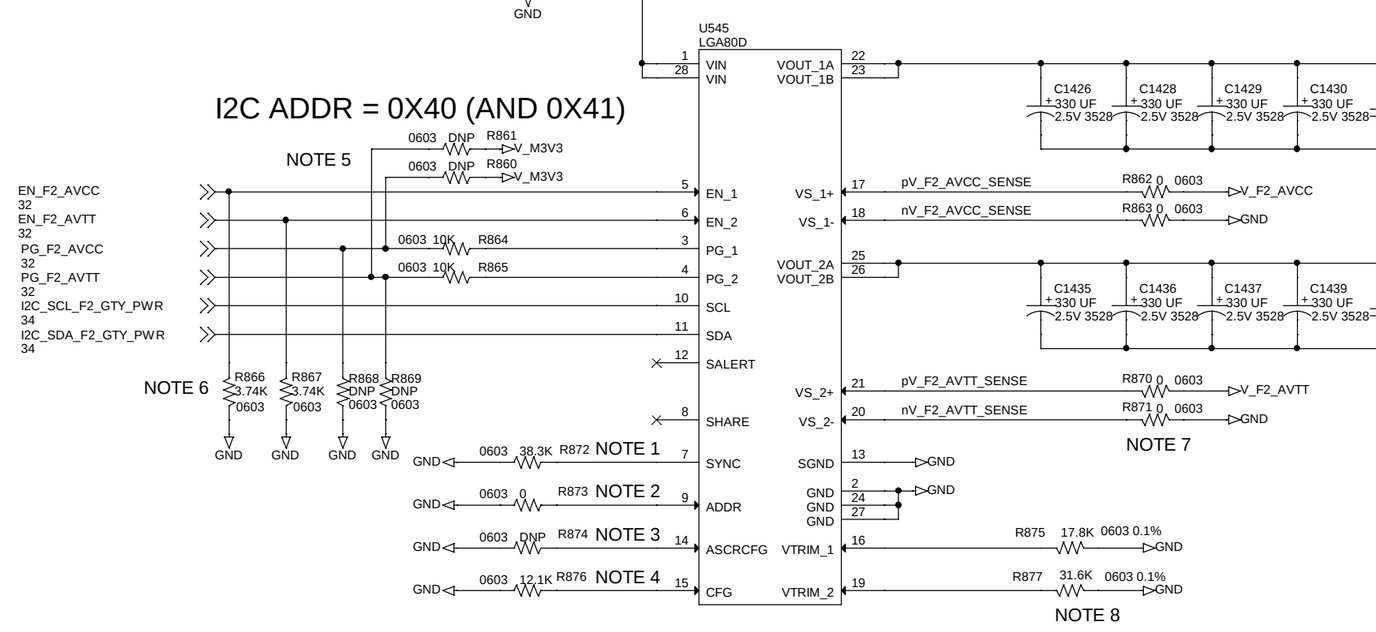
NOTE 8 RSET = 16.2K FOR 0.85V

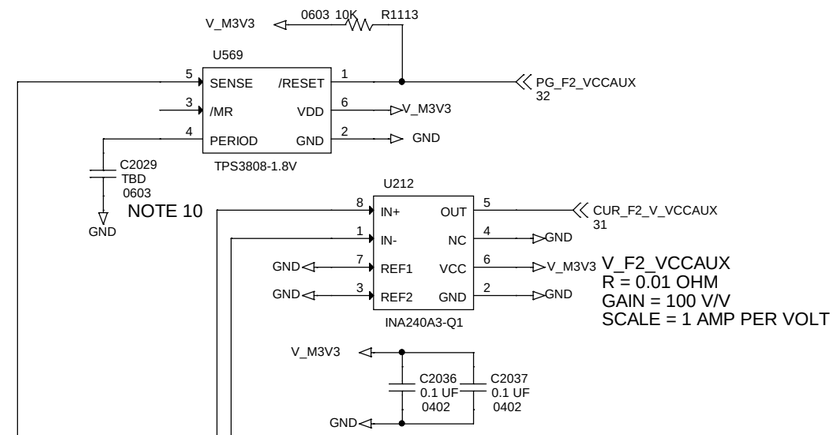
NOTE 9 THE MASTER IS LABELED "A".
THE SLAVE IS LABELED "B".

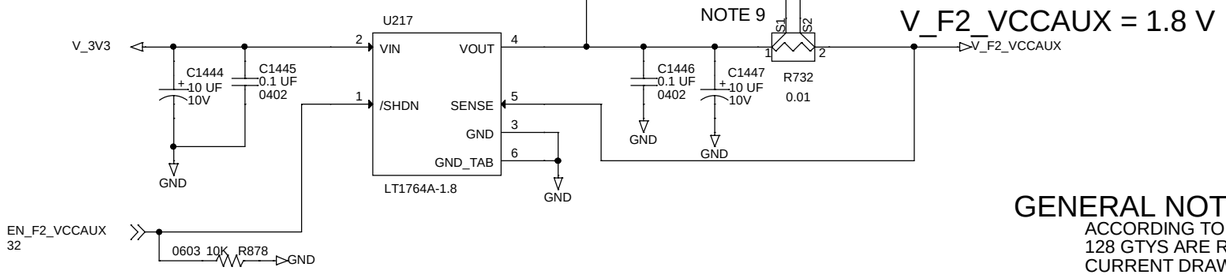
APOLLO CM W/ DUAL A2577, MK1			
Title: 3.05: POWER FPGA#2 INTERNAL			
Size	Document Number: 6089-119		Rev: A
Date: Wednesday, February 17, 2021	Sheet 28 of 80		

3.06: POWER FPGA#2 GTY TRANSCEIVER









SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=12.1K SELECTS 2-OUTPUT @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 17.8K FOR 0.9V
RSET = 31.6K FOR 1.2V

NOTE 9 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 10 MILLIOHMS AND A CURRENT OF 2.5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LT1764 REGULATOR IS RATED FOR 3 AMPS. IF MORE THAN 2.5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 10 MILLIOHMS.

NOTE 10 IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

GENERAL NOTES:

ACCORDING TO THE XILINX POWER ESTIMATOR, IF ALL 128 GTYS ARE RUNNING AT 25 GBPS. THE MAXIMUM CURRENT DRAWS WILL BE:
GTY_AVCC = 11.5 AMPS
GTY_AVTT = 30 AMPS
GTY_VCCAUX = 2.5 AMPS

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.06: POWER FPGA#2 GTY TRANSCEIVER		
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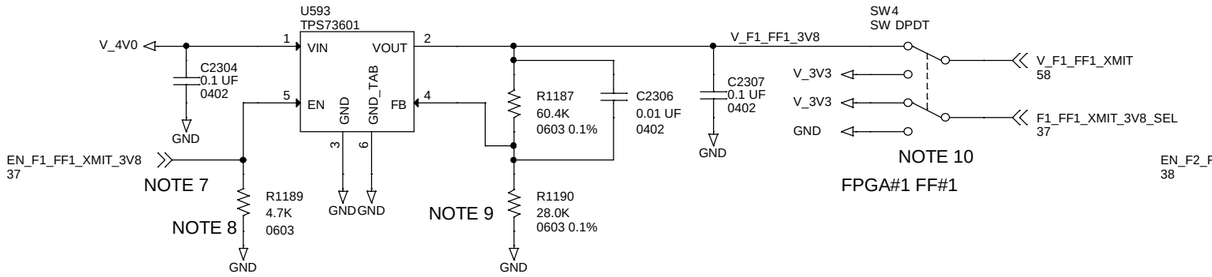
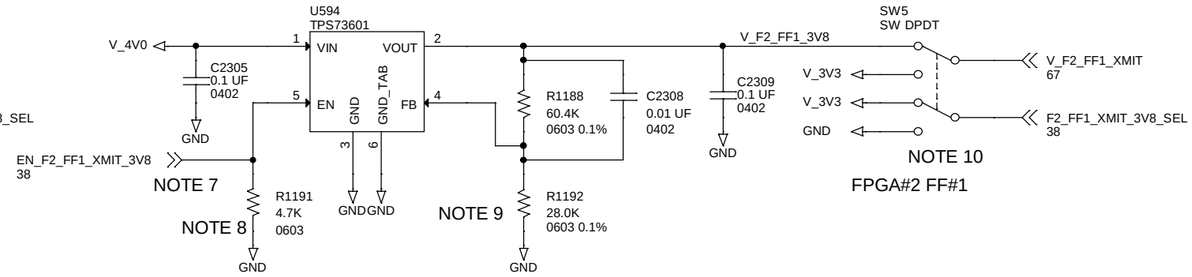
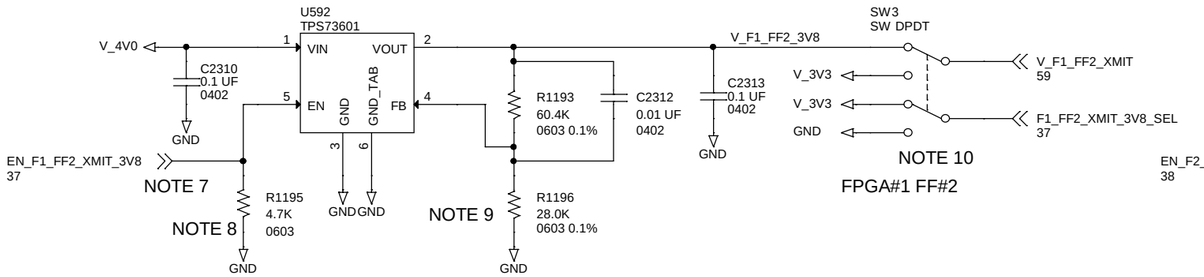
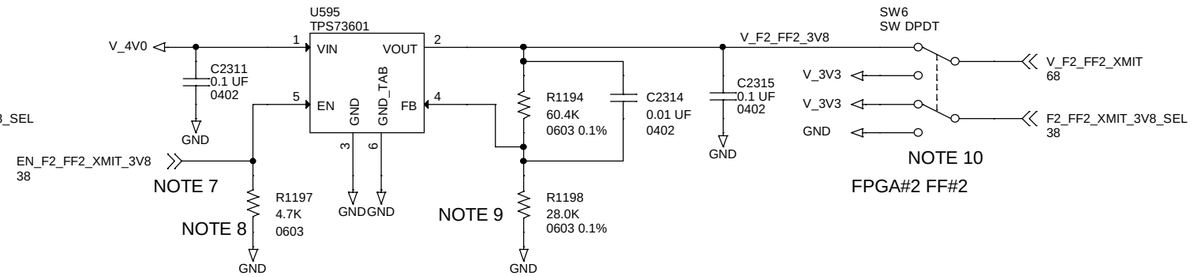
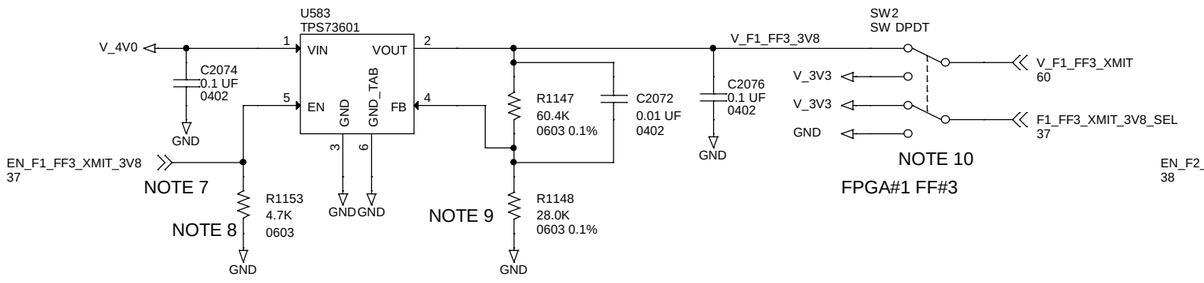
3.07: POWER FOR FF X12 XMIT

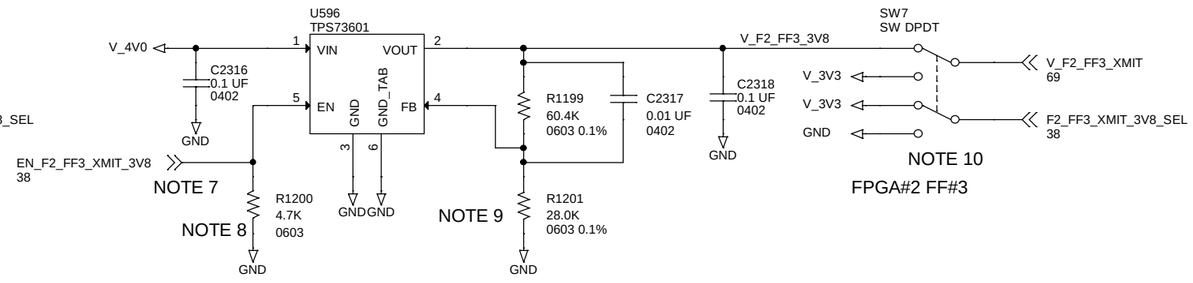




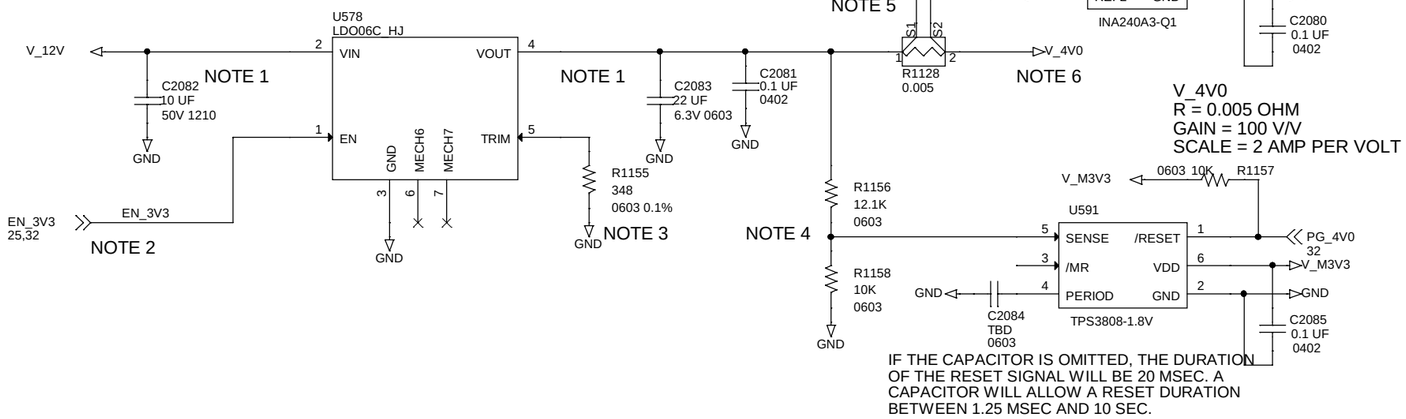








V_4V0 IS USED TO SUPPLY THE 3.8 VOLT REGULATORS FOR THE 12-LANE FIREFLY TRANSMITTERS.



NOTE 1 THE LDO06C DOES NOT REQUIRE ANY EXTERNAL INPUT OR OUTPUT CAPACITORS.

NOTE 2 THE LDO06C IS ENABLED AT THE SAME TIME AS THE BOARD-WIDE 3.3V SUPPLY.

NOTE 3 LDO06C OUTPUT SETPOINT RESISTOR
R = 1.182 / (VOUT - 0.591)
FOR 4.0 VOLTS, R=347 OHMS

NOTE 4 THE MONITORING CHIP EXPECTS 1.8 VOLTS AT THE INPUT, SO THE 4.0 VOLTS IS DIVIDED.

NOTE 5 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 5 MILLIOHMS AND A CURRENT OF 5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LDO06C REGULATOR IS RATED FOR 6 AMPS. IF MORE THAN 5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 5 MILLIOHMS.

NOTE 6 V_4V0 IS ONLY CONNECTED ONTHIS PAGE, EXCEPT FOR MEASURING BY THE MCU ADC.

NOTE 7 THE TPS73601 REGULATOR SHOULD NOT BE ENABLED UNTIL THE FIREFLY TRANSMITTER TYPE HAS BEEN DETERMINED AND THE VOLTAGE SWITCH IS FOUND TO BE IN THE CORRECT POSITION.

NOTE 8 PULLDOWNS ARE NEEDED ON THE CONTROL INPUTS, SINCE THE I2C DRIVER DEVICES NEED TO BE CONFIGURED AS OUTPUTS BEFORE THEY CAN CONTOL THE LOGIC LEVEL. THE I2C DRIVERS HAVE A BUILT-IN 100K PULLUP.

NOTE 9 THE TPS73601 OUTPUT VOLTAGE IS CALCULATED BY:
VOUT = 1.204 * ((Rtop+Rbot)/Rbot)
IF Rtop = 60.4k AND Rbot=28K, THEN VOUT = 3.8 V

NOTE 10 THE SWITCH IS SHOWN IN THE POSITION TO PROVIDE 3.8 VOLTS TO THE FIREFLY TRANSMITTER. THE "*_3V8_SEL" SIGNAL WILL BE HIGH.

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.07: POWER FOR FF X12 XMIT		
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Date: Wednesday, February 17, 2021	Sheet 30 of 80	

3.08: VOLT, CUR, TEMP MEASURE

TEST POINTS TO
MEASURE VOLTAGES

THE 12 VOLT SUPPLY
LEVEL IS DIVIDED BY 6

THE M3.3 VOLT SUPPLY
LEVEL IS DIVIDED BY 2

THE 3.3 VOLT SUPPLY
LEVEL IS DIVIDED BY 2

THE 4.0 VOLT SUPPLY
LEVEL IS DIVIDED BY 2

U540-5
TM4C1290NCPDT_NEW

THE VALUE OF "MCU_VREFA" SETS THE VOLTAGE THAT WILL CORRESPOND TO THE ADC FULL SCALE VALUE OF 4095. THE MINIMUM VOLTAGE IS 2.4 VOLTS.

THIS DESIGN USES 2.5 VOLTS FOR FULL SCALE.

U576
LT1790-2.5V

THE ANTI-ALIASING CUTOFF FREQUENCY IS 15.9 KHZ

A 16 MHZ ADC CLOCK PROVIDES A SAMPLING RATE OF 1 MEGA-SAMPLES PER SECOND. IF ALL 20 ADC CHANNELS ARE USED, THE SAMPLE RATE PER CHANNEL IS 50 KILO-SAMPLES PER SECOND, AND THE NYQUIST FREQUENCY IS 25 KHZ.

THE MAXIMUM SOURCE IMPEDANCE FEEDING THE ADC INPUTS IS 500 OHMS.

APOLLO CM W/ DUAL A2577, MK1	
Title	3.08: VOLT, CUR, TEMP MEASURE
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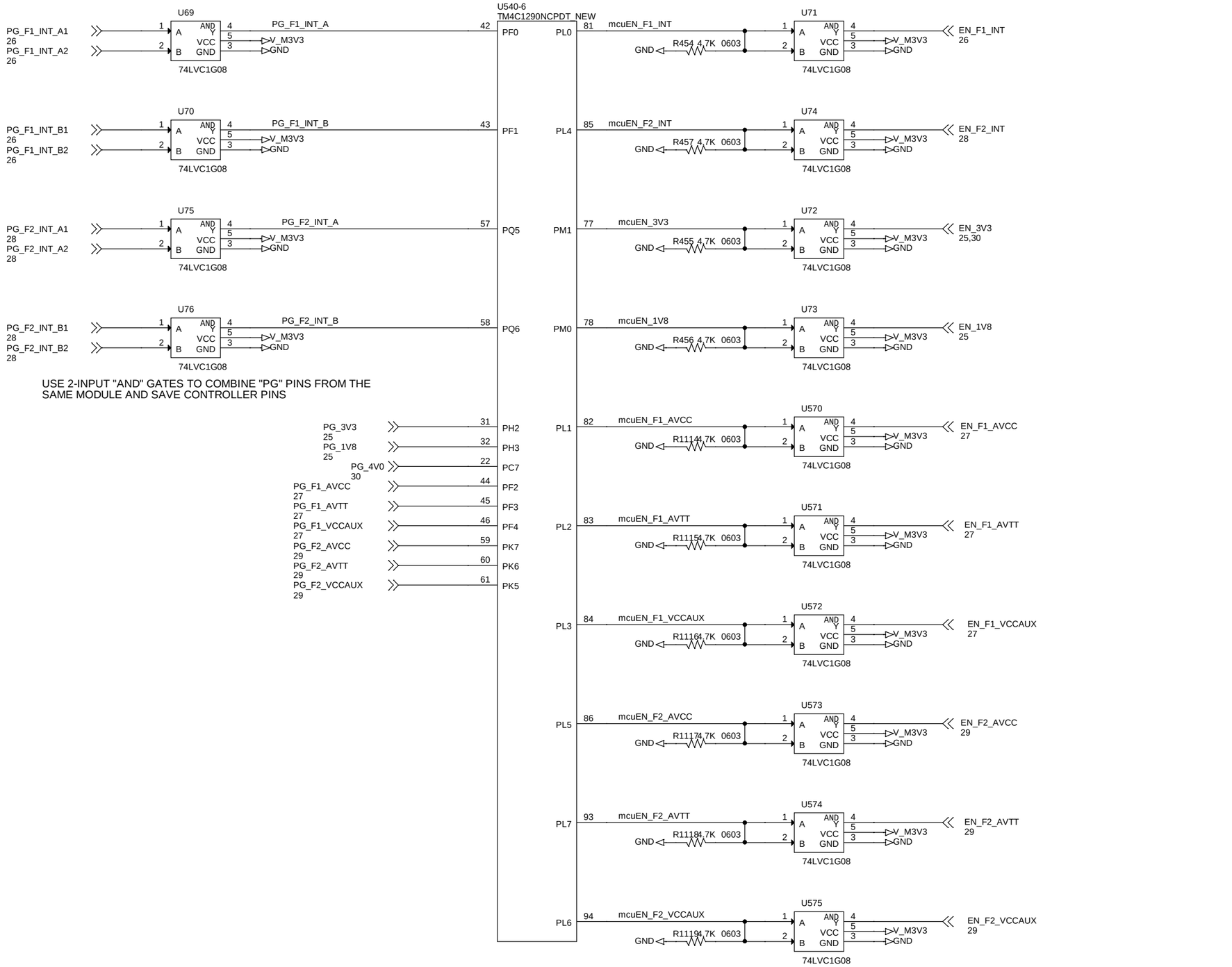
3.09: POWER CONTROL



USE 2-INPUT "AND" GATES TO COMBINE "PG" PINS FROM THE SAME MODULE AND SAVE CONTROLLER PINS

THE ACTIVE-HI "ENABLE" SIGNALS WILL ONLY BE ASSERTED WHEN V_M3V3 IS PRESENT AND THE CONTROLLER OUTPUT IS HIGH. OTHERWISE, PULLDOWN RESISTORS ON THE GATE INPUT AND THE POWER MODULE INPUT WILL KEEP THE ENABLE SIGNALS LOW.

APOLLO CM W/ DUAL A2577, MK1			
Title: 3.09: POWER CONTROL			
Size	Document Number: 6089-119		Rev: A
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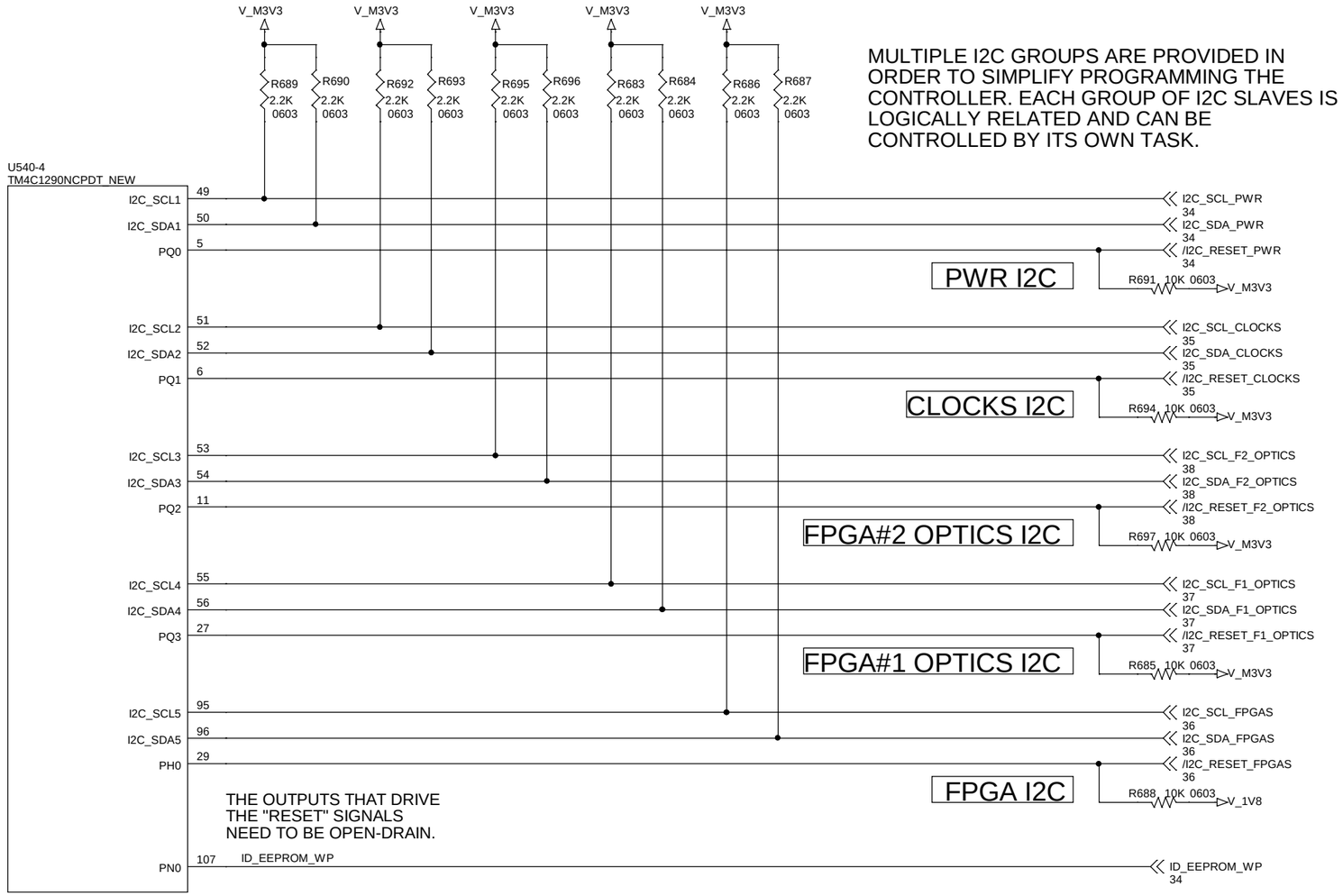
4.01: I2C CONTROLLER



APOLLO CM W/ DUAL A2577, MK1		
Title: 4.01: I2C CONTROLLER		
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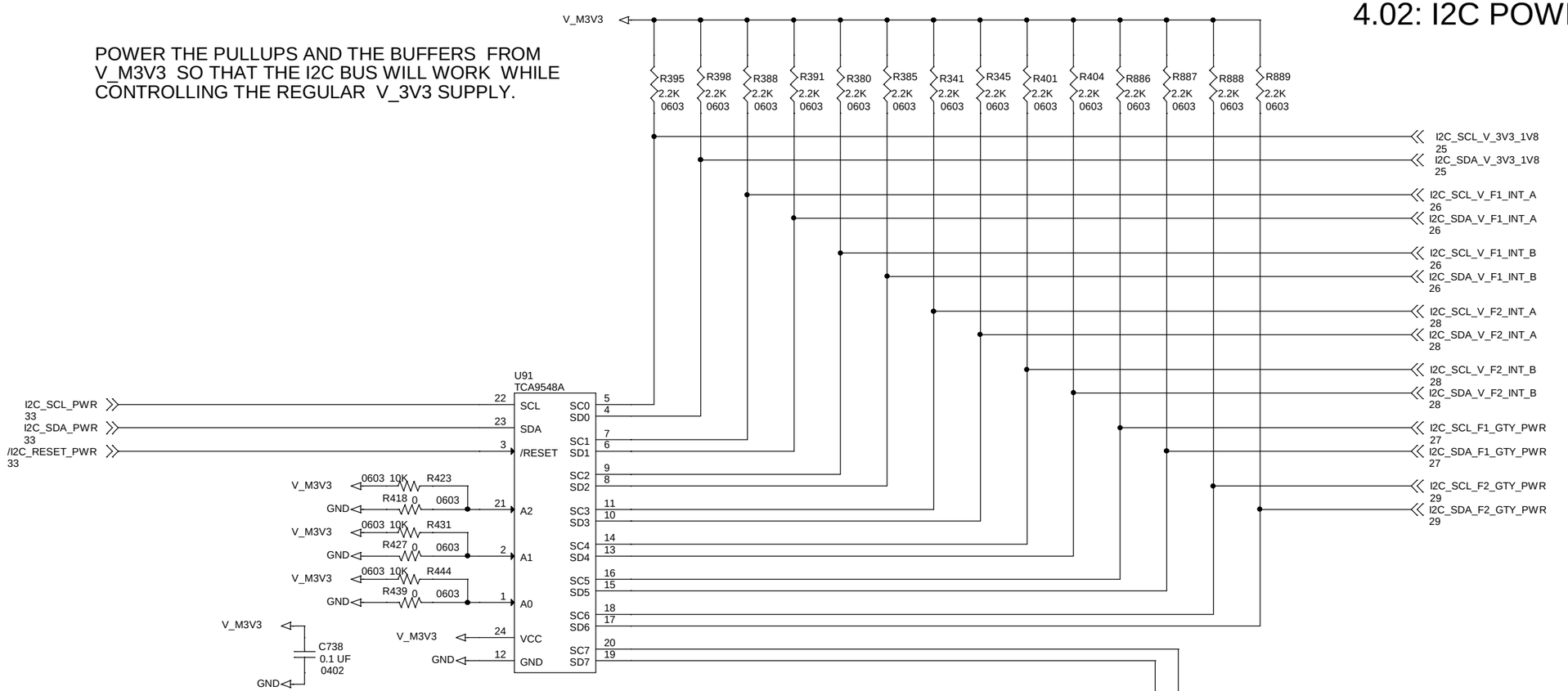
4.02: I2C POWER CONTROL

POWER THE PULLUPS AND THE BUFFERS FROM V_M3V3 SO THAT THE I2C BUS WILL WORK WHILE CONTROLLING THE REGULAR V_3V3 SUPPLY.



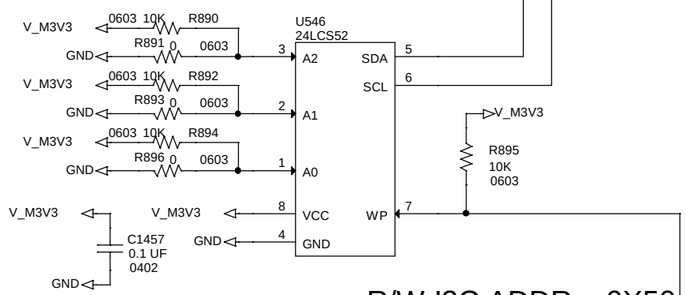
I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

THIS EEPROM IS FOR STORING UNCHANGING INFORMATION, LIKE SERIAL NUMBERS OR OTHER BOARD IDENTIFIERS.



24LCS52 I2C ADDRESS:
READ OR WRITE
1 0 1 0 A2 A1 A0
RANGE: 0X50 TO 0X57
WRITE-PROTECT REGISTER
0 1 1 0 A2 A1 A0

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

R/W I2C ADDR = 0X50

WP I2C ADDR = 0X30

ID_EEPROM_WP 33

APOLLO CM W/ DUAL A2577, MK1		
Title: 4.02: I2C POWER CONTROL		
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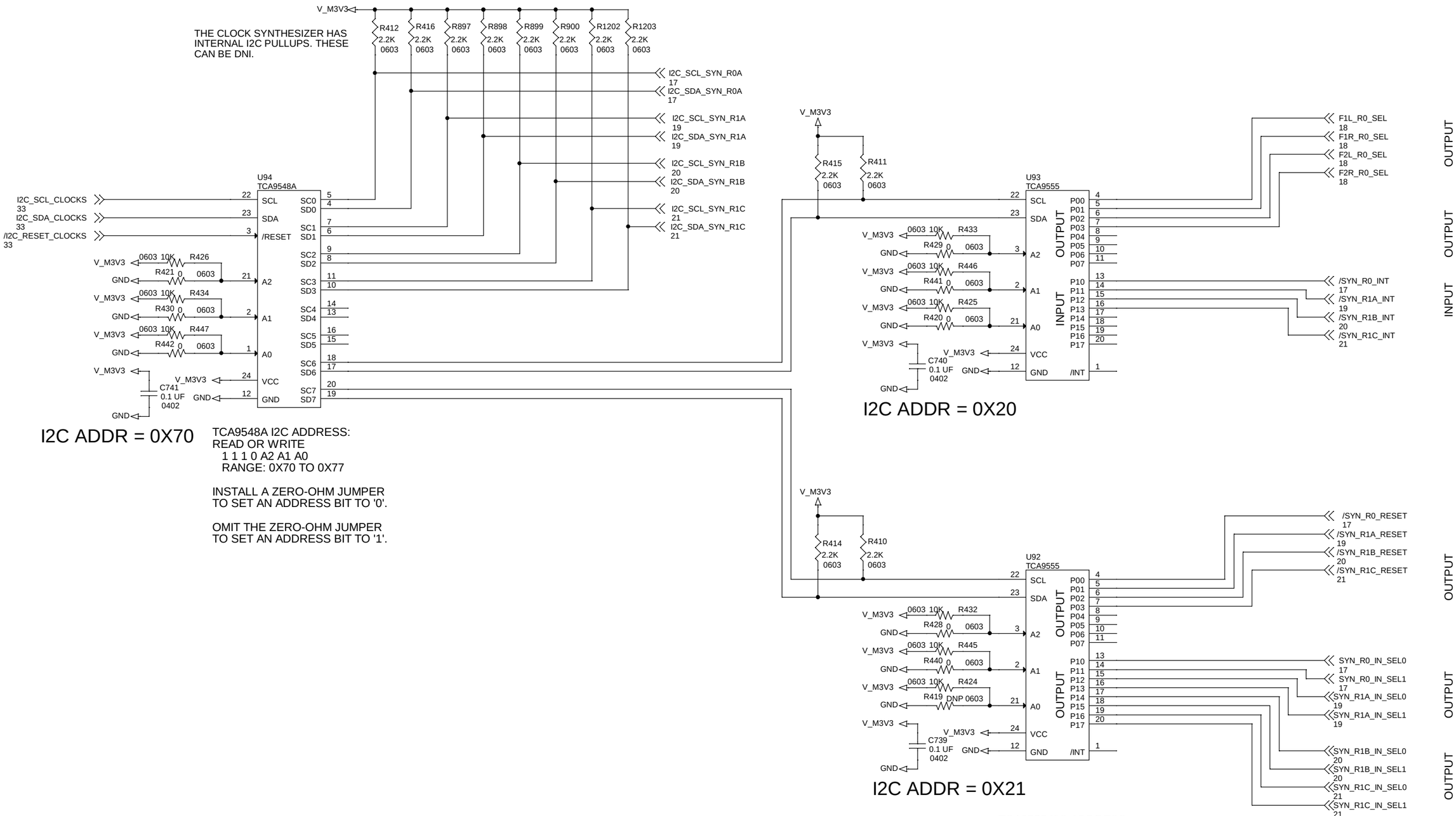
4.03: I2C CLOCK CONTROL



APOLLO CM W/ DUAL A2577, MK1		
Title: 4.03: I2C CLOCK CONTROL		
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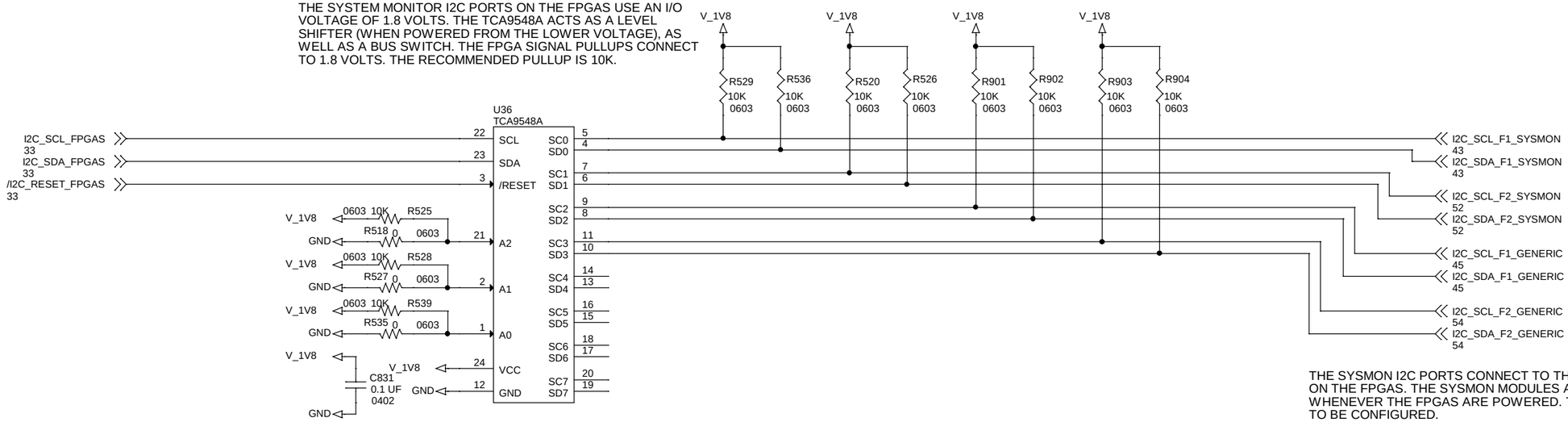
4.04: I2C FPGA INTERNALS

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER (WHEN POWERED FROM THE LOWER VOLTAGE), AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS. THE RECOMMENDED PULLUP IS 10K.



I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

THE SYSMON I2C PORTS CONNECT TO THE SYSMON MODULE PINS ON THE FPGAS. THE SYSMON MODULES ARE AVAILABLE WHENEVER THE FPGAS ARE POWERED. THE FPGAS DO NOT HAVE TO BE CONFIGURED.

THE GENERIC I2C PORTS CONNECT TO I2C MODULES THAT ARE LOADED AS PART OF THE CONFIGURATION PROCESS. THEY ARE NOT AVAILABLE BEFORE THE FPGA HAS BEEN CONFIGURED.

THE GENERIC MODULES HAVE MORE CAPABILITY THAN THE SYSMON MODULES.

A2	A1	A0	I2C BUS SLAVE ADDRESS
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

APOLLO CM W/ DUAL A2577, MK1

Title: 4.04: I2C FPGA INTERNALS

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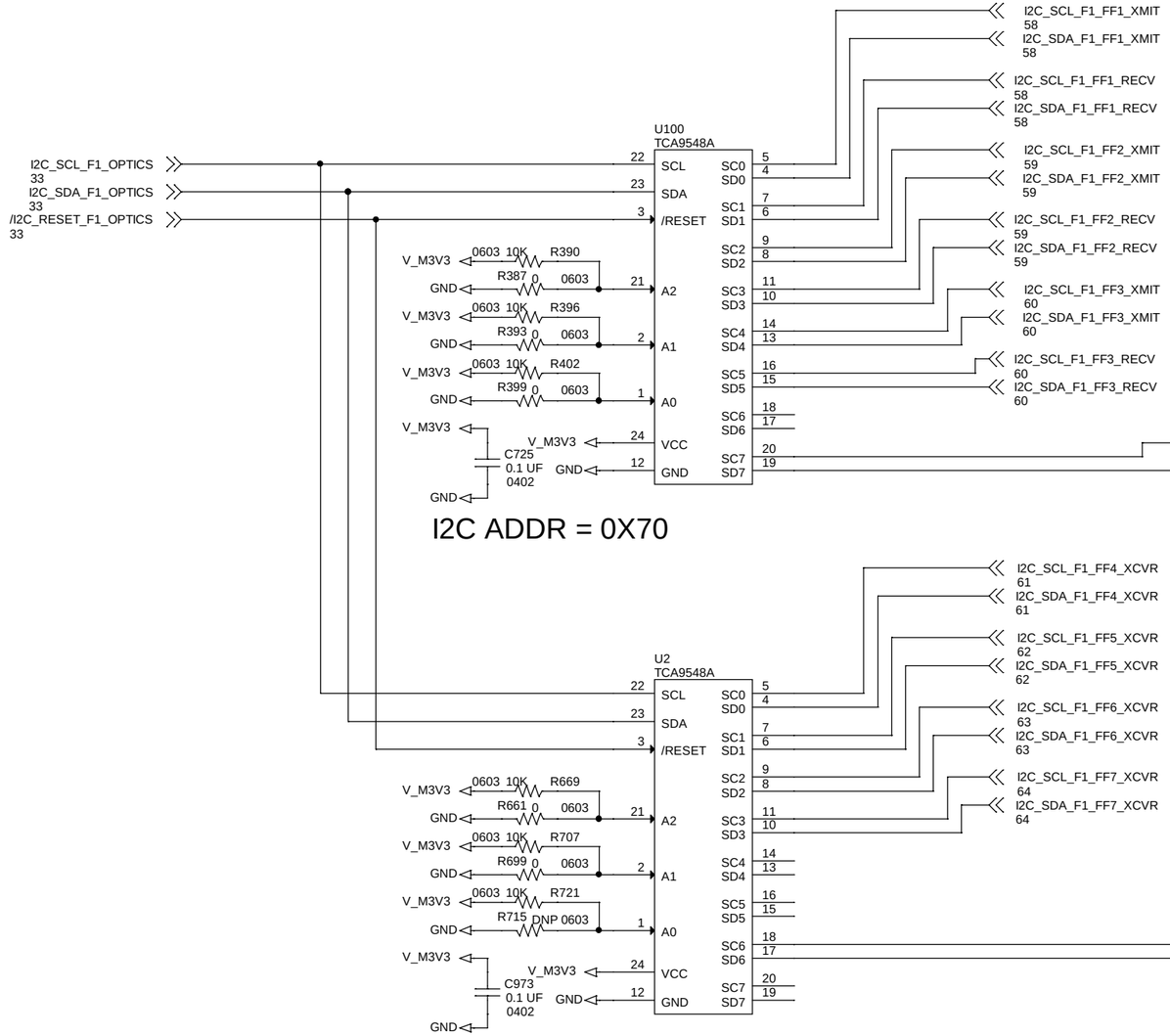
4.05: I2C FPGA#1 OPTICS



I2C ADDR = 0X70

I2C ADDR = 0X20

I2C ADDR = 0X71

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

I2C ADDR = 0X21

TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

APOLLO CM W/ DUAL A2577, MK1		
Title: 4.05: I2C FPGA#1 OPTICS		
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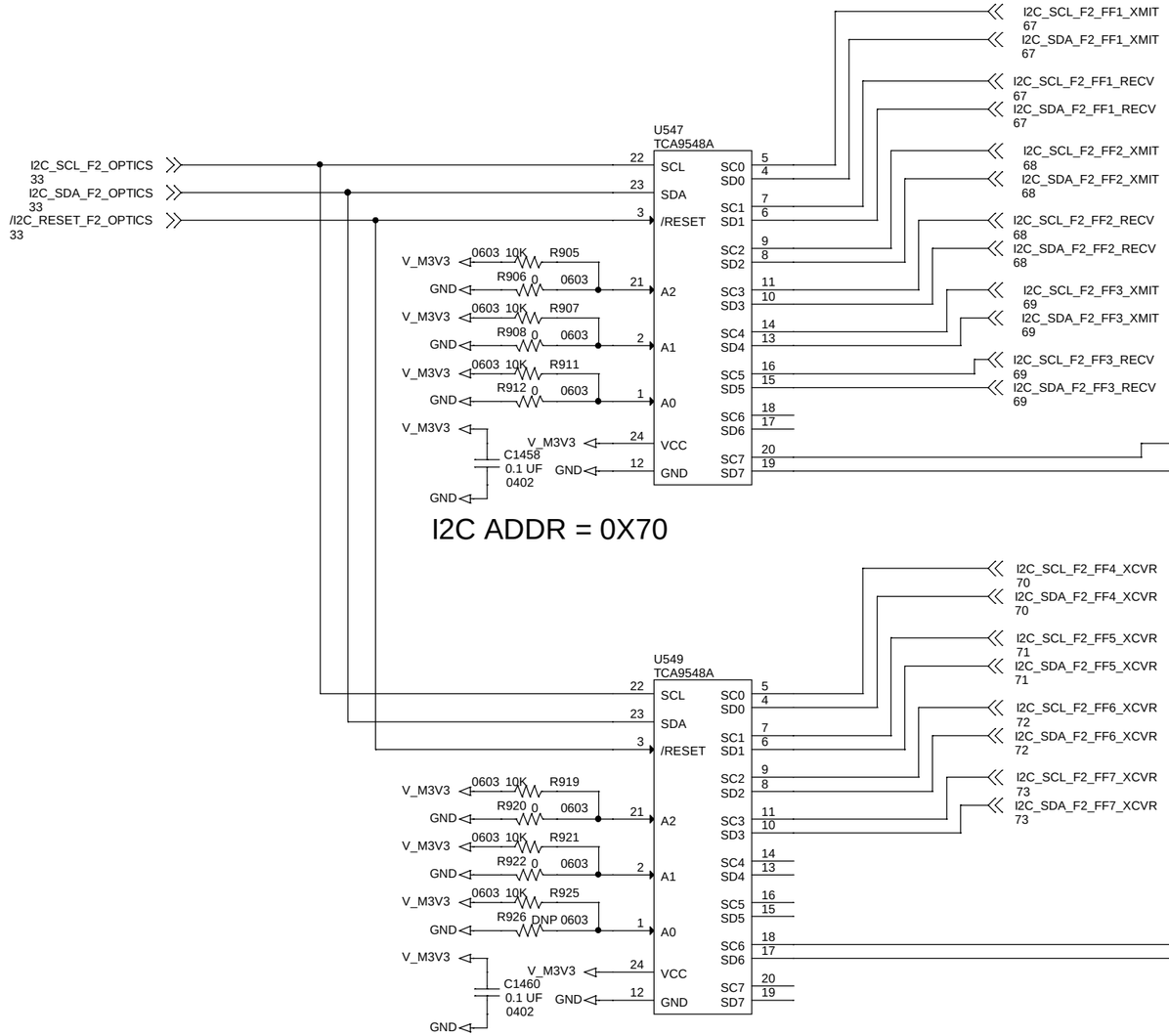
4.06: I2C FPGA#2 OPTICS



I2C ADDR = 0X70

I2C ADDR = 0X20

I2C ADDR = 0X71

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

I2C ADDR = 0X21

TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

APOLLO CM W/ DUAL A2577, MK1		
Title: 4.06: I2C FPGA#2 OPTICS		
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5.01: FPGA#1 GND

U201-1 FPGA_VU13P_A2577

A13	GND	GND	AE12
A16	GND	GND	AE16
A17	GND	GND	AE18
A18	GND	GND	AE20
A21	GND	GND	AE22
A26	GND	GND	AE24
A31	GND	GND	AE26
A34	GND	GND	AE28
A35	GND	GND	AE3
A36	GND	GND	AE30
A39	GND	GND	AE32
A4	GND	GND	AE34
A43	GND	GND	AE36
A45	GND	GND	AE38
A48	GND	GND	AE4
A7	GND	GND	AE40
A9	GND	GND	AE43
AA12	GND	GND	AE47
AA14	GND	GND	AE48
AA16	GND	GND	AE49
AA18	GND	GND	AE5
AA20	GND	GND	AE9
AA22	GND	GND	AF1
AA24	GND	GND	AF10
AA26	GND	GND	AF12
AA28	GND	GND	AF15
AA3	GND	GND	AF17
AA30	GND	GND	AF19
AA32	GND	GND	AF2
AA34	GND	GND	AF21
AA36	GND	GND	AF23
AA38	GND	GND	AF25
AA4	GND	GND	AF27
AA40	GND	GND	AF29
AA43	GND	GND	AF31
AA47	GND	GND	AF33
AA48	GND	GND	AF35
AA49	GND	GND	AF37
AA5	GND	GND	AF39
AA9	GND	GND	AF40
AB1	GND	GND	AF42
AB10	GND	GND	AF45
AB15	GND	GND	AF47
AB17	GND	GND	AF5
AB19	GND	GND	AF50
AB2	GND	GND	AF51
AB21	GND	GND	AF7
AB23	GND	GND	AG12
AB25	GND	GND	AG16
AB27	GND	GND	AG20
AB29	GND	GND	AG22
AB31	GND	GND	AG24
AB33	GND	GND	AG26
AB35	GND	GND	AG28
AB37	GND	GND	AG3
AB38	GND	GND	AG30
AB42	GND	GND	AG32
AB45	GND	GND	AG34
AB47	GND	GND	AG36
AB5	GND	GND	AG38
AB50	GND	GND	AG4
AB51	GND	GND	AG40
AB7	GND	GND	AG44
AC14	GND	GND	AG47
AC16	GND	GND	AG48
AC18	GND	GND	AG49
AC20	GND	GND	AG5
AC22	GND	GND	AG8
AC24	GND	GND	AH1
AC26	GND	GND	AH11
AC28	GND	GND	AH12
AC3	GND	GND	AH15
AC30	GND	GND	AH17
AC32	GND	GND	AH2
AC34	GND	GND	AH21
AC36	GND	GND	AH23
AC38	GND	GND	AH25
AC39	GND	GND	AH27
AC4	GND	GND	AH29
AC44	GND	GND	AH31
AC47	GND	GND	AH33
AC48	GND	GND	AH35
AC49	GND	GND	AH37
AC5	GND	GND	AH39
AC8	GND	GND	AH40
AD1	GND	GND	AH41
AD11	GND	GND	AH46
AD12	GND	GND	AH47
AD15	GND	GND	AH5
AD17	GND	GND	AH50
AD19	GND	GND	AH51
AD2	GND	GND	AH6
AD21	GND	GND	AJ14
AD23	GND	GND	AJ16
AD25	GND	GND	AJ20
AD27	GND	GND	AJ22
AD29	GND	GND	AJ24
AD31	GND	GND	AJ26
AD33	GND	GND	AJ28
AD35	GND	GND	AJ3
AD37	GND	GND	AJ30
AD39	GND	GND	AJ32
AD40	GND	GND	AJ34
AD41	GND	GND	AJ36
AD46	GND	GND	AJ38
AD47	GND	GND	AJ39
AD5	GND	GND	AJ47
AD50	GND	GND	AJ43
AD51	GND	GND	AJ48
AD6	GND	GND	AJ4

GND GND

U201-2 FPGA_VU13P_A2577

AJ49	GND	GND	AP42
AJ5	GND	GND	AP45
AJ9	GND	GND	AP47
AK1	GND	GND	AP5
AK10	GND	GND	AP50
AK15	GND	GND	AP51
AK17	GND	GND	AP7
AK2	GND	GND	AR12
AK21	GND	GND	AR14
AK23	GND	GND	AR22
AK25	GND	GND	AR24
AK27	GND	GND	AR26
AK29	GND	GND	AR28
AK31	GND	GND	AR3
AK33	GND	GND	AR30
AK35	GND	GND	AR38
AK37	GND	GND	AR4
AK38	GND	GND	AR40
AK42	GND	GND	AR44
AK45	GND	GND	AR47
AK47	GND	GND	AR48
AK5	GND	GND	AR49
AK50	GND	GND	AR5
AK51	GND	GND	AR8
AK7	GND	GND	AT1
AL12	GND	GND	AT11
AL14	GND	GND	AT2
AL16	GND	GND	AT21
AL18	GND	GND	AT23
AL20	GND	GND	AT25
AL22	GND	GND	AT27
AL24	GND	GND	AT29
AL26	GND	GND	AT31
AL28	GND	GND	AT38
AL3	GND	GND	AT41
AL30	GND	GND	AT46
AL32	GND	GND	AT47
AL34	GND	GND	AT5
AL36	GND	GND	AT50
AL38	GND	GND	AT51
AL4	GND	GND	AT6
AL40	GND	GND	AU13
AL44	GND	GND	AU14
AL47	GND	GND	AU18
AL48	GND	GND	AU24
AL49	GND	GND	AU26
AL5	GND	GND	AU28
AL8	GND	GND	AU3
AM1	GND	GND	AU30
AM11	GND	GND	AU38
AM15	GND	GND	AU39
AM17	GND	GND	AU4
AM19	GND	GND	AU43
AM2	GND	GND	AU47
AM21	GND	GND	AU48
AM23	GND	GND	AU49
AM25	GND	GND	AU5
AM27	GND	GND	AU9
AM29	GND	GND	AV1
AM31	GND	GND	AV10
AM33	GND	GND	AV15
AM35	GND	GND	AV2
AM37	GND	GND	AV25
AM38	GND	GND	AV35
AM41	GND	GND	AV38
AM46	GND	GND	AV42
AM47	GND	GND	AV45
AM5	GND	GND	AV47
AM50	GND	GND	AV5
AM51	GND	GND	AV50
AM6	GND	GND	AV51
AN12	GND	GND	AV7
AN14	GND	GND	AW12
AN16	GND	GND	AW14
AN18	GND	GND	AW22
AN20	GND	GND	AW3
AN22	GND	GND	AW32
AN24	GND	GND	AW38
AN26	GND	GND	AW4
AN28	GND	GND	AW40
AN3	GND	GND	AW44
AN30	GND	GND	AW47
AN32	GND	GND	AW48
AN34	GND	GND	AW49
AN36	GND	GND	AW5
AN38	GND	GND	AW8
AN4	GND	GND	AY1
AN40	GND	GND	AY11
AN43	GND	GND	AY19
AN47	GND	GND	AY2
AN48	GND	GND	AY29
AN49	GND	GND	AY38
AN5	GND	GND	AY41
AN9	GND	GND	AY46
AP1	GND	GND	AY47
AP10	GND	GND	AY5
AP15	GND	GND	AY50
AP17	GND	GND	AY51
AP19	GND	GND	AY6
AP2	GND	GND	B10
AP21	GND	GND	B14
AP23	GND	GND	B16
AP25	GND	GND	B19
AP27	GND	GND	B20
AP29	GND	GND	B21
AP31	GND	GND	B23
AP33	GND	GND	B3
AP35	GND	GND	B31
AP37	GND	GND	B32
AP38	GND	GND	B33

GND GND

U201-3 FPGA_VU13P_A2577

B36	GND	GND	BG12
B38	GND	GND	BG16
B4	GND	GND	BG17
B42	GND	GND	BG18
B45	GND	GND	BG21
B46	GND	GND	BG28
B47	GND	GND	BG3
B48	GND	GND	BG31
B49	GND	GND	BG34
B5	GND	GND	BG35
B6	GND	GND	BG36
B7	GND	GND	BG4
BA12	GND	GND	BG40
BA14	GND	GND	BG44
BA16	GND	GND	BG45
BA26	GND	GND	BG48
BA3	GND	GND	BG49
BA36	GND	GND	BG7
BA38	GND	GND	BG8
BA4	GND	GND	BH1
BA40	GND	GND	BH11
BA43	GND	GND	BH15
BA47	GND	GND	BH16
BA48	GND	GND	BH19
BA49	GND	GND	BH2
BA5	GND	GND	BH20
BA9	GND	GND	BH21
BB1	GND	GND	BH25
BB10	GND	GND	BH31
BB2	GND	GND	BH32
BB23	GND	GND	BH33
BB33	GND	GND	BH36
BB38	GND	GND	BH37
BB42	GND	GND	BH41
BB45	GND	GND	BH45
BB47	GND	GND	BH46
BB5	GND	GND	BH47
BB50	GND	GND	BH5
BB51	GND	GND	BH50
BB7	GND	GND	BH51
BC12	GND	GND	BH6
BC14	GND	GND	BH7
BC20	GND	GND	BJ13
BC3	GND	GND	BJ16
BC30	GND	GND	BJ17
BC38	GND	GND	BJ18
BC4	GND	GND	BJ2
BC40	GND	GND	BJ21
BC44	GND	GND	BJ22
BC47	GND	GND	BJ3
BC48	GND	GND	BJ31
BC49	GND	GND	BJ34
BC5	GND	GND	BJ35
BC8	GND	GND	BJ36
BD1	GND	GND	BJ39
BD11	GND	GND	BJ4
BD14	GND	GND	BJ43
BD2	GND	GND	BJ45
BD27	GND	GND	BJ48
BD38	GND	GND	BJ49
BD41	GND	GND	BJ50
BD46	GND	GND	BJ7
BD47	GND	GND	BJ9
BD5	GND	GND	BK10
BD50	GND	GND	BK14
BD51	GND	GND	BK16
BD6	GND	GND	BK19
BE12	GND	GND	BK20
BE14	GND	GND	BK21
BE15	GND	GND	BK29
BE16	GND	GND	BK3
BE17	GND	GND	BK31
BE18	GND	GND	BK32
BE19	GND	GND	BK33
BE24	GND	GND	BK36
BE3	GND	GND	BK38
BE33	GND	GND	BK4
BE34	GND	GND	BK42
BE35	GND	GND	BK45
BE36	GND	GND	BK46
BE37	GND	GND	BK47
BE38	GND	GND	BK48
BE4	GND	GND	BK49
BE40	GND	GND	BK5
BE43	GND	GND	BK6
BE47	GND	GND	BK7
BE48	GND	GND	BL12
BE49	GND	GND	BL16
BE5	GND	GND	BL17
BE9	GND	GND	BL18
BF1	GND	GND	BL21
BF10	GND	GND	BL26
BF16	GND	GND	BL31
BF19	GND	GND	BL34
BF2	GND	GND	BL35
BF20	GND	GND	BL36
BF21	GND	GND	BL4
BF31	GND	GND	BL40
BF32	GND	GND	BL44
BF33	GND	GND	BL45
BF36	GND	GND	BL48
BF42	GND	GND	BL7
BF45	GND	GND	BL8
BF46	GND	GND	C12
BF47	GND	GND	C16
BF5	GND	GND	C17
BF50	GND	GND	C18
BF51	GND	GND	C2
BF6	GND	GND	C21
BF7	GND	GND	C3

GND GND

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C31	GND	GND	H35
C34	GND	GND	H36
C35	GND	GND	H37
C36	GND	GND	H38
C4	GND	GND	H41
C40	GND	GND	H46
C44	GND	GND	H47
C45	GND	GND	H5
C48	GND	GND	H50
C49	GND	GND	H51
C50	GND	GND	H6
C7	GND	GND	J12
C8	GND	GND	J14
D1	GND	GND	J22
D11	GND	GND	J3
D15	GND	GND	J38
D16	GND	GND	J4
D19	GND	GND	J40
D2	GND	GND	J43
D20	GND	GND	J47
D21	GND	GND	J48
D27	GND	GND	J49
D31	GND	GND	J5
D32	GND	GND	J9
D33	GND	GND	K1
D36	GND	GND	K10
D37	GND	GND	K14
D41	GND	GND	K19
D45	GND	GND	K2
D46	GND	GND	K29
D47	GND	GND	K38
D5	GND	GND	K42
D50	GND	GND	K45
D51	GND	GND	K47
D6	GND	GND	K5
D7	GND	GND	K50
E12	GND	GND	K51
E16	GND	GND	K7
E17	GND	GND	L12
E18	GND	GND	L14
E21	GND	GND	L16
E24	GND	GND	L26
E3	GND	GND	L3
E31	GND	GND	L36
E34	GND	GND	L38
E35	GND	GND	L4
E36	GND	GND	L40
E39	GND	GND	L44
E4	GND	GND	L47
E43	GND	GND	L48
E45	GND	GND	L49
E48	GND	GND	L5
E49	GND	GND	L8
E7	GND	GND	M1
E9	GND	GND	M11
F1	GND	GND	M2
F10	GND	GND	M23
F14	GND	GND	M33
F16	GND	GND	M38
F19	GND	GND	M41
F2	GND	GND	M46
F20	GND	GND	M47
F21	GND	GND	M5
F31	GND	GND	M50
F32	GND	GND	M51
F33	GND	GND	M6
F36	GND	GND	N13
F38	GND	GND	N14
F42	GND	GND	N20
F45	GND	GND	N3
F46	GND	GND	N30
F47	GND	GND	N38
F5	GND	GND	N39
F50	GND	GND	N4
F51	GND	GND	N43
F6	GND	GND	N47
F7	GND	GND	N48
G12	GND	GND	N49
G16	GND	GND	N5
G18	GND	GND	N9
G21	GND	GND	P1
G28	GND	GND	P10
G3	GND	GND	P17
G31	GND	GND	P2
G34	GND	GND	P27
G36	GND	GND	P37
G4	GND	GND	P38
G40	GND	GND	P42
G44	GND	GND	P45
G47	GND	GND	P47
G48	GND	GND	P5
G49	GND	GND	P50
G5	GND	GND	P51
G8	GND	GND	P7
H1	GND	GND	R12
H11	GND	GND	R14
H14	GND	GND	R24
H15	GND	GND	R3
H16	GND	GND	R34
H17	GND	GND	R38
H18	GND	GND	R4
H19	GND	GND	R40
H2	GND	GND	R44
H20	GND	GND	R47
H21	GND	GND	R48
H25	GND	GND	R49
H31	GND	GND	R5
H32	GND	GND	R8
H33	GND	GND	T1
H34	GND	GND	T11

GND GND

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T2	GND
T21	GND
T38	GND
T41	GND
T46	GND
T47	GND
T5	GND
T50	GND
T51	GND
T6	GND
U13	GND
U14	GND
U18	GND
U28	GND
U3	GND
U30	GND
U38	GND
U39	GND
U4	GND
U43	GND
U47	GND
U48	GND
U49	GND
U5	GND
U9	GND
V1	GND
V10	GND
V2	GND
V23	GND
V25	GND
V27	GND
V29	GND
V31	GND
V38	GND
V42	GND
V45	GND
V47	GND
V5	GND
V50	GND
V51	GND
V7	GND
W12	GND
W14	GND
W18	GND
W20	GND
W22	GND
W24	GND
W26	GND
W28	GND
W3	GND
W30	GND
W34	GND
W36	GND
W38	GND
W4	GND
W40	GND
W44	GND
W47	GND
W48	GND
W49	GND
W5	GND
W8	GND
Y1	GND
Y11	GND
Y15	GND
Y17	GND
Y19	GND
Y2	GND
Y21	GND
Y23	GND
Y25	GND
Y27	GND
Y29	GND
Y31	GND
Y33	GND
Y35	GND
Y37	GND
Y38	GND
Y41	GND
Y46	GND
Y47	GND
Y5	GND
Y50	GND
Y51	GND

GND

R1120 10K 0603

V_M3V3

GND Y6 /F1_INSTALLED 22

IF THE FPGA IS INSTALLED, THEN THE ACTIVE-LO "/F1_INSTALLED" SIGNAL WILL BE PULLED TO GND. IF THE FPGA IS NOT INSTALLED, THE SIGNAL WILL BE HI.

ANY FPGA GND PIN CAN BE USED.

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Title: 5.01: FPGA#1 GND

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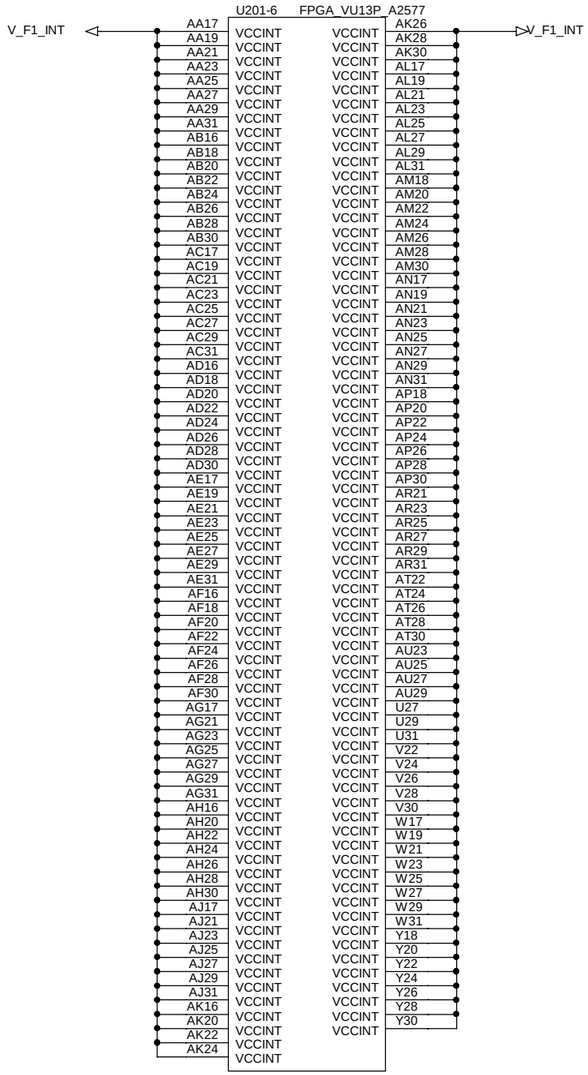
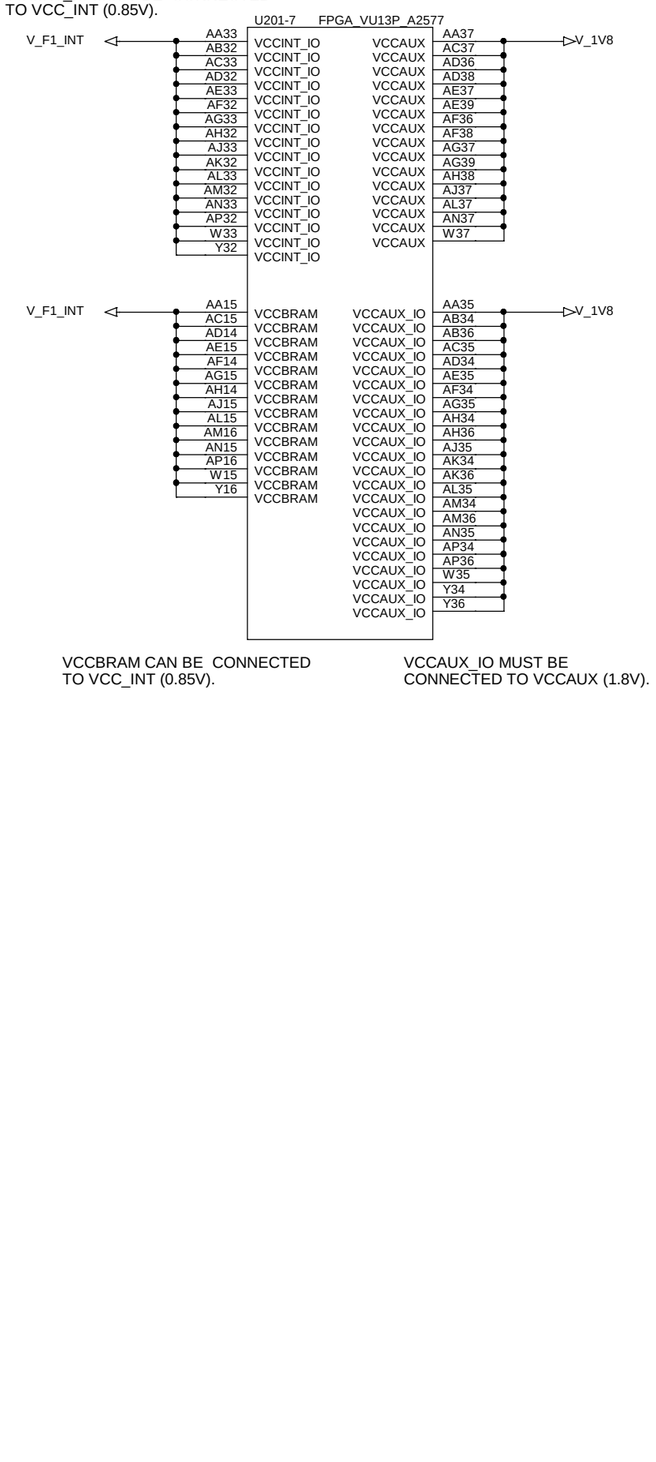
5.02: FPGA#1 POWER INTERNAL

VCCINT MUST BE 0.85V.

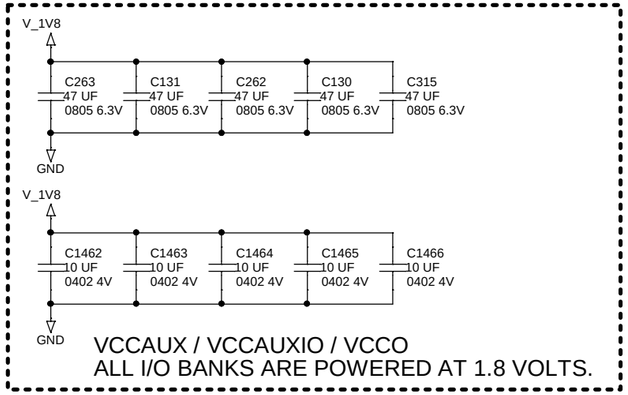


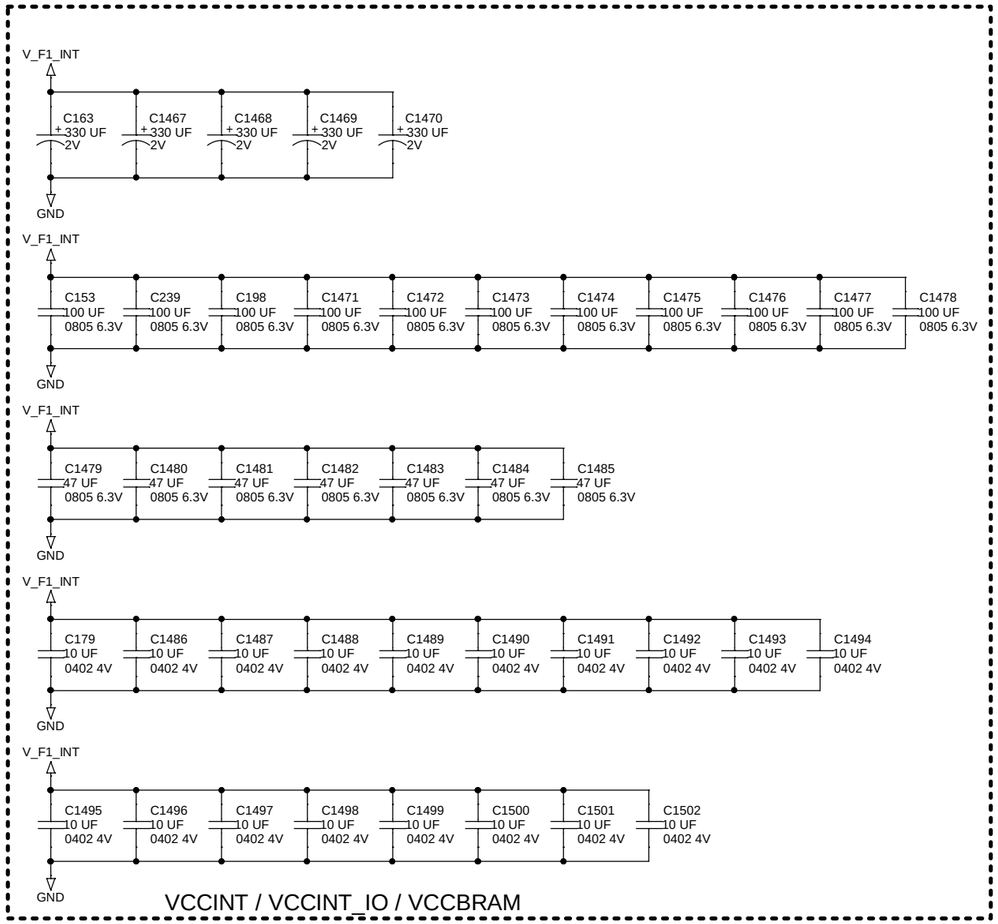
VCCINT_IO MUST BE CONNECTED TO VCC_INT (0.85V).



VCCBRAM CAN BE CONNECTED TO VCC_INT (0.85V).

VCCAUX_IO MUST BE CONNECTED TO VCCAUX (1.8V).





BYPASS CAPACITOR VALUES AND QUANTITIES FROM "UG583 UltraScale Architecture PCB Design"

APOLLO CM W/ DUAL A2577, MK1		
Title: 5.02: FPGA#1 POWER INTERNAL		
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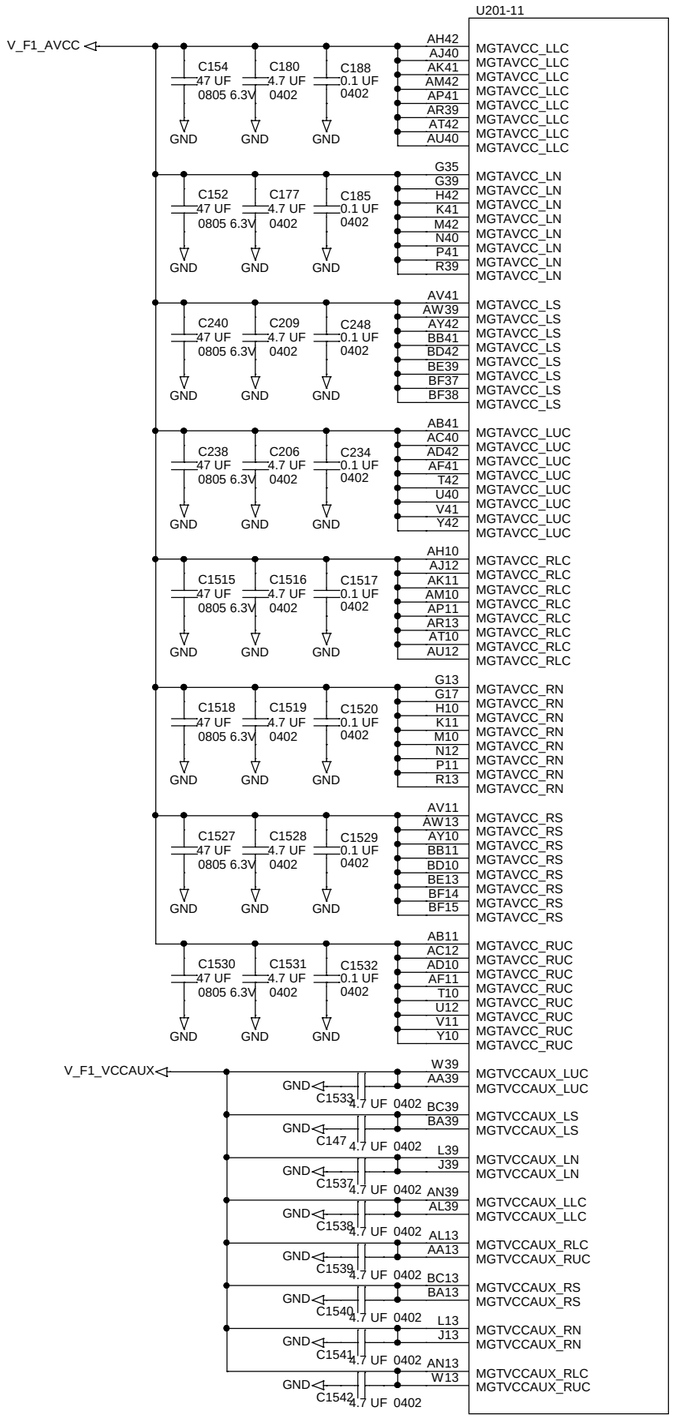
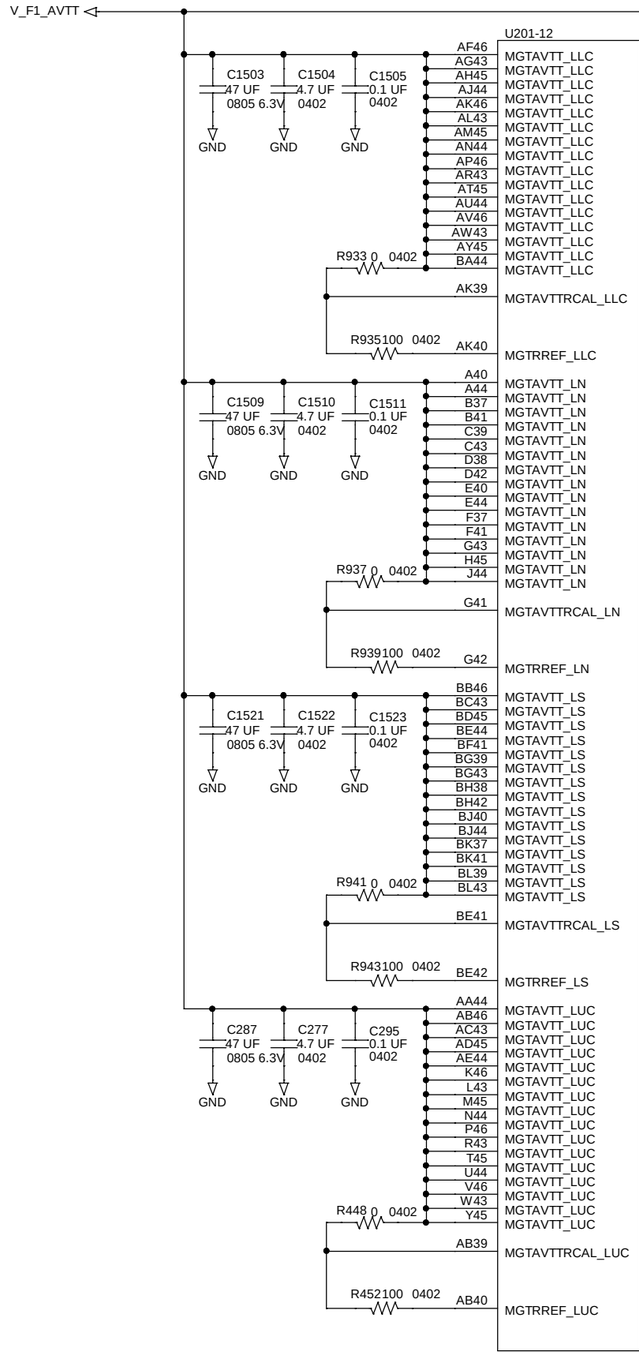
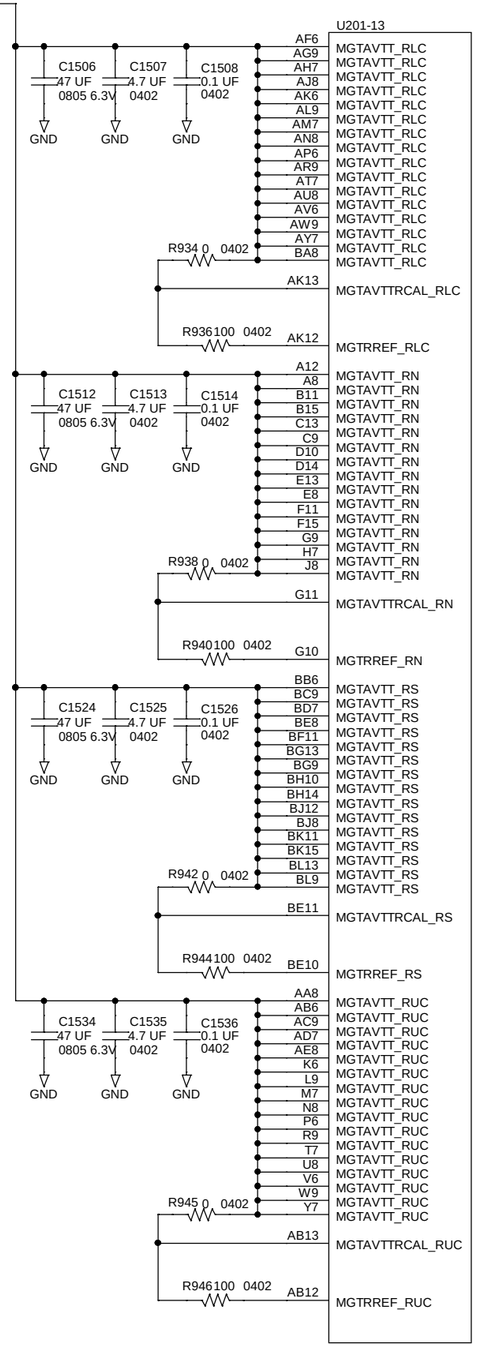
5.03: FPGA#1 GTY TRANSCEIVER POWER







REFER TO THE GTY USER GUIDE FOR DETAILS ON TRACE ROUTING FOR THE MGTRREF RESISTOR.

PLACE CAPACITORS AND RESISTORS THAT ARE ON THIS SHEET NEAR THE BGA PINS.

APOLLO CM W/ DUAL A2577, MK1		
Title: 5.03: FPGA#1 GTY TRANSCEIVER POWER		
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5.04: FPGA#1 CONFIGURATION

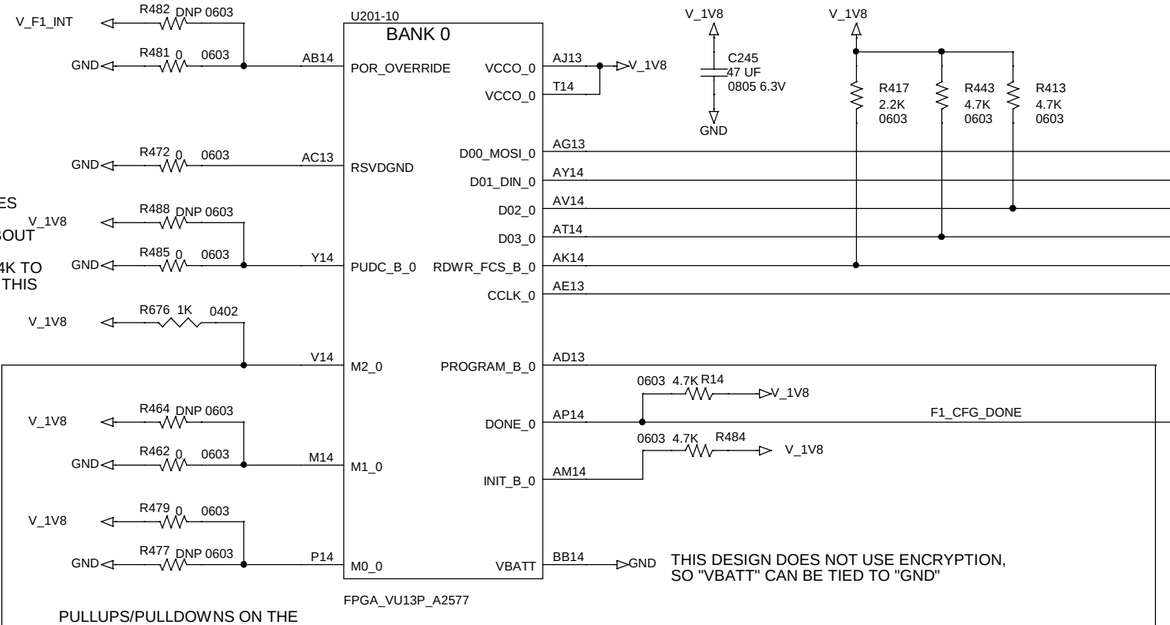
MUST BE TIED TO "VCCINT" OR "GND". DO NOT CONNECT TO "VCCO_0". CONNECT TO "GND" FOR STANDARD POR DELAY.

THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

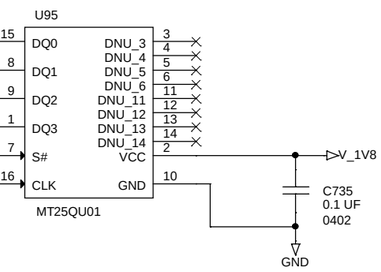
M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

PULLUPS/PULLDOWNS ON THE BOOT MODE CONFIGURATION INPUTS MUST BE 1K OR LESS.

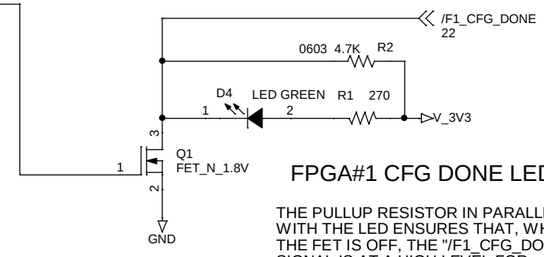


QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
VU9P 641,272,864
VU13P 906,547,008



FPGA#1 CFG DONE LED

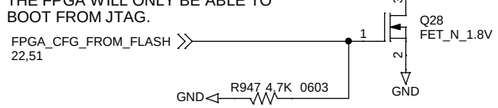


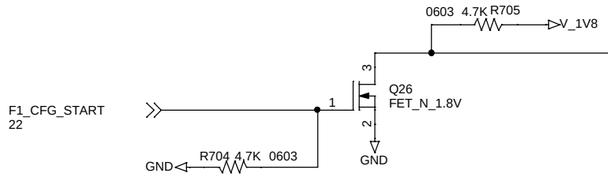
THE PULLUP RESISTOR IN PARALLEL WITH THE LED ENSURES THAT, WHEN THE FET IS OFF, THE "/F1_CFG_DONE" SIGNAL IS AT A HIGH LEVEL FOR FEEDING THE MCU.

FOR LED CURRENT OF 5 MA, THE FORWARD VOLTAGE DROP IS 1.95V. USE 270 OHM RESISTOR.

IF THE FPGA IS NOT INSTALLED, THEN "CFG_DONE" WILL ALWAYS BE HIGH, AND THE LED WILL ALWAYS BE LIT. THIS IS UNINTENDED AND UNDESIRABLE. CONSIDER ELIMINATING THE FPGA DONE LED,OR ADD A GATE.

WHEN "FPGA_CFG_FROM_FLASH" IS ASSERTED (HIGH), THE FPGA WILL BE ABLE TO BOOT FROM THE FLASH MEMORY. WHEN IT IS NEGATED (LOW), THE FPGA WILL ONLY BE ABLE TO BOOT FROM JTAG.





THE FPGA CAN BE REPROGRAMMED BY PULSING "F1_CFG_START" FROM THE MCU.

APOLLO CM W/ DUAL A2577, MK1			
Title: 5.04: FPGA#1 CONFIGURATION			
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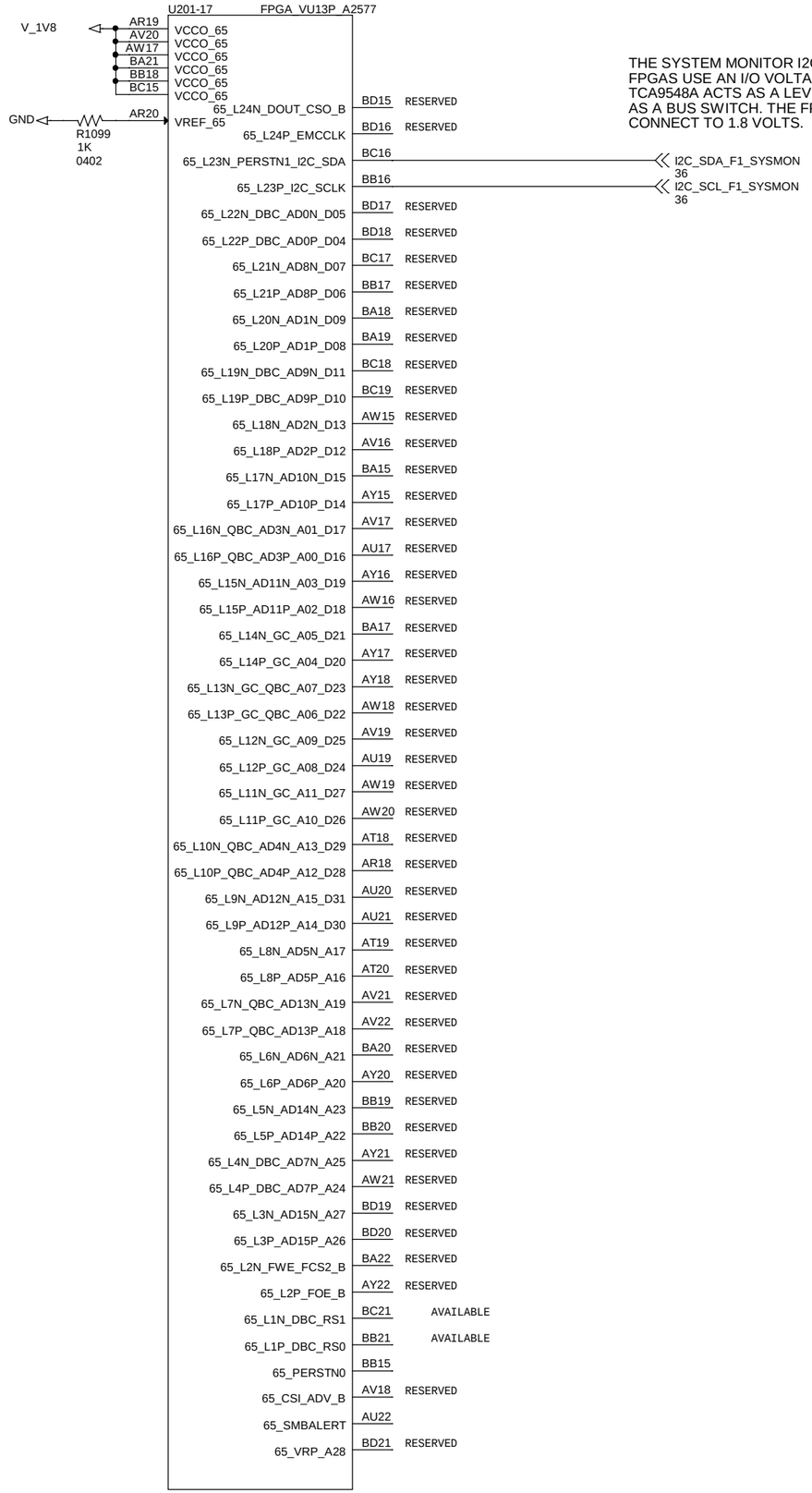
5.05: F1 BANK 65



THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

APOLLO CM W/ DUAL A2577, MK1		
Title: 5.05: F1 BANK 65		
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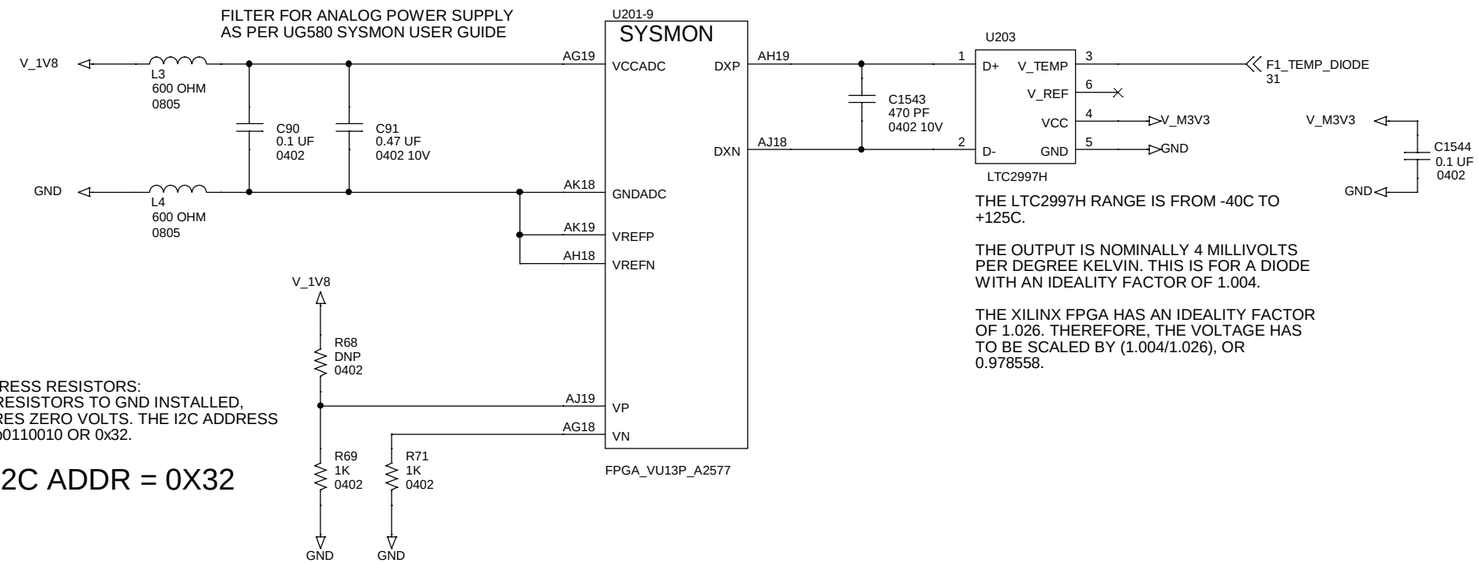
5.06: FPGA#1 SYSTEM MONITOR

FOR THE VU9P, THE MASTER SLR INDEX IS SLR1, AND THE SLAVE SLR INDEX ARE SLR0 AND SLR2.

FOR THE VU13P, THE MASTER SLR INDEX IS SLR1, AND THE SLAVE SLR INDEX ARE SLR0, SLR2, AND SLR3.

ONLY THE MASTER SLR IS ACCESSABLE FROM THE I2C CONNECTIONS.



APOLLO CM W/ DUAL A2577, MK1		
Title: 5.06: FPGA#1 SYSTEM MONITOR		
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5.07 F1 UTILITY BANKS

F1 LOGIC
TCDS 40MHZ INPUT

ac_nF1_TCDS40_IN 20
ac_pF1_TCDS40_IN 20

nF1F2_SPARE0 54
pF1F2_SPARE0 54
nF1F2_SPARE2 54
pF1F2_SPARE2 54
nF1F2_SPARE5 54
pF1F2_SPARE5 54
nF1F2_SPARE4 54
pF1F2_SPARE4 54
nF1F2_SPARE8 54
pF1F2_SPARE8 54
nF1F2_SPARE9 54
pF1F2_SPARE9 54

F1_LED_BLUE 22
F1_LED_RED 22
F1_LED_GREEN 22

bc_nF1_TCDS_REC_CLK 20
bc_pF1_TCDS_REC_CLK 20

nF1F2_SPARE11 54
pF1F2_SPARE11 54
nF1F2_SPARE12 54
pF1F2_SPARE12 54
nF1F2_SPARE7 54
pF1F2_SPARE7 54
nF1F2_SPARE3 54
pF1F2_SPARE3 54
nF1F2_SPARE1 54
pF1F2_SPARE1 54
nF1F2_SPARE10 54
pF1F2_SPARE10 54

nF1F2_SPARE6 54
pF1F2_SPARE6 54

GND — R1100 240 0402

U201-21

H23	IO_L10N_T1U_N7_QBC_AD4N_74	VCCO_74	D22
J23	IO_L10P_T1U_N6_QBC_AD4P_74	VCCO_74	G23
J21	IO_L11N_T1U_N9_GC_74	VCCO_74	K24
K21	IO_L11P_T1U_N8_GC_74	VCCO_74	L21
K22	IO_L12N_T1U_N11_GC_74	VCCO_74	N25
K23	IO_L12P_T1U_N10_GC_74	VCCO_74	P22
L22	IO_L13N_T2L_N1_GC_QBC_74		
L23	IO_L13P_T2L_N0_GC_QBC_74	VREF_74	U24
M21	IO_L14N_T2L_N3_GC_74		
M22	IO_L14P_T2L_N2_GC_74		
L24	IO_L15N_T2L_N5_AD11N_74		
M25	IO_L15P_T2L_N4_AD11P_74		
M24	IO_L16N_T2U_N7_QBC_AD3N_74		
N24	IO_L16P_T2U_N6_QBC_AD3P_74		
N21	IO_L17N_T2U_N9_AD10N_74		
N22	IO_L17P_T2U_N8_AD10P_74		
K25	IO_L18N_T2U_N11_AD2N_74		
L25	IO_L18P_T2U_N10_AD2P_74		
T23	IO_L19N_T3L_N1_DBC_AD9N_74		
T24	IO_L19P_T3L_N0_DBC_AD9P_74		
D23	IO_L1N_T0L_N1_DBC_74		
E23	IO_L1P_T0L_N0_DBC_74		
R25	IO_L20N_T3L_N3_AD1N_74		
T25	IO_L20P_T3L_N2_AD1P_74		
U22	IO_L21N_T3L_N5_AD8N_74		
U23	IO_L21P_T3L_N4_AD8P_74		
P24	IO_L22N_T3U_N7_DBC_AD0N_74		
P25	IO_L22P_T3U_N6_DBC_AD0P_74		
R22	IO_L23N_T3U_N9_74		
T22	IO_L23P_T3U_N8_74		
P23	IO_L24N_T3U_N11_74		
R23	IO_L24P_T3U_N10_74		
B24	IO_L2N_T0L_N3_74		
C24	IO_L2P_T0L_N2_74		
A23	IO_L3N_T0L_N5_AD15N_74		
A24	IO_L3P_T0L_N4_AD15P_74		
E22	IO_L4N_T0U_N7_DBC_AD7N_74		
F22	IO_L4P_T0U_N6_DBC_AD7P_74		
C22	IO_L5N_T0U_N9_AD14N_74		
C23	IO_L5P_T0U_N8_AD14P_74		
A22	IO_L6N_T0U_N11_AD6N_74		
B22	IO_L6P_T0U_N10_AD6P_74		
G24	IO_L7N_T1L_N1_QBC_AD13N_74		
H24	IO_L7P_T1L_N0_QBC_AD13P_74		
F23	IO_L8N_T1L_N3_AD5N_74		
F24	IO_L8P_T1L_N2_AD5P_74		
G22	IO_L9N_T1L_N5_AD12N_74		
H22	IO_L9P_T1L_N4_AD12P_74		
D24	IO_T0U_N12_VRP_74		
J24	IO_T1U_N12_74		
N23	IO_T2U_N12_74		
P21	IO_T3U_N12_74		

FPGA_VU13P_A2577

V_1V8

R1098 1K 0402

GND

ac_nF1L_R0_LOG 18
ac_pF1L_R0_LOG 18
ac_nF1R_R0_LOG 18
ac_pF1R_R0_LOG 18
ac_nF1_LOG_OSC 17
ac_pF1_LOG_OSC 17
ac_nF1_UTIL 17
ac_pF1_UTIL 17

THESE ARE LOGIC-CIRCUIT CLOCKS SOURCED FROM AN ON-BOARD OSCILLATOR, EITHER DIRECTLY OR THROUGH A SYNTHESIZER. THEY MUST BE CONNECTED TO A GLOBAL CLOCK INPUT.

lovF1_TO_MCU 22
lovMCU_TO_F1 22
lovF1_C2C_OK 22

I2C_SCL_F1_GENERIC 36
I2C_SDA_F1_GENERIC 36

VERIFY THAT A GENERIC I2C BUS CAN BE CONNECTED HERE.

U201-18

T33	IO_L10N_T1U_N7_QBC_AD4N_70	VCCO_70	J37
T32	IO_L10P_T1U_N6_QBC_AD4P_70	VCCO_70	K34
P34	IO_L11N_T1U_N9_GC_70	VCCO_70	N35
P33	IO_L11P_T1U_N8_GC_70	VCCO_70	P32
R33	IO_L12N_T1U_N11_GC_70	VCCO_70	T36
R32	IO_L12P_T1U_N10_GC_70	VCCO_70	U33
M32	IO_L13N_T2L_N1_GC_QBC_70		
N32	IO_L13P_T2L_N0_GC_QBC_70	VREF_70	W32
N34	IO_L14N_T2L_N3_GC_70		
N33	IO_L14P_T2L_N2_GC_70		
N37	IO_L15N_T2L_N5_AD11N_70		
N36	IO_L15P_T2L_N4_AD11P_70		
M35	IO_L16N_T2U_N7_QBC_AD3N_70		
M34	IO_L16P_T2U_N6_QBC_AD3P_70		
M37	IO_L17N_T2U_N9_AD10N_70		
M36	IO_L17P_T2U_N8_AD10P_70		
L34	IO_L18N_T2U_N11_AD2N_70		
L33	IO_L18P_T2U_N10_AD2P_70		
K35	IO_L19N_T3L_N1_DBC_AD9N_70		
L35	IO_L19P_T3L_N0_DBC_AD9P_70		
V37	IO_L1N_T0L_N1_DBC_70		
V36	IO_L1P_T0L_N0_DBC_70		
J33	IO_L20N_T3L_N3_AD1N_70		
J32	IO_L20P_T3L_N2_AD1P_70		
K37	IO_L21N_T3L_N5_AD8N_70		
L37	IO_L21P_T3L_N4_AD8P_70		
K33	IO_L22N_T3U_N7_DBC_AD0N_70		
K32	IO_L22P_T3U_N6_DBC_AD0P_70		
J36	IO_L23N_T3U_N9_70		
K36	IO_L23P_T3U_N8_70		
J35	IO_L24N_T3U_N11_70		
J34	IO_L24P_T3U_N10_70		
T37	IO_L2N_T0L_N3_70		
U37	IO_L2P_T0L_N2_70		
U36	IO_L3N_T0L_N5_AD15N_70		
V35	IO_L3P_T0L_N4_AD15P_70		
U35	IO_L4N_T0U_N7_DBC_AD7N_70		
U34	IO_L4P_T0U_N6_DBC_AD7P_70		
V34	IO_L5N_T0U_N9_AD14N_70		
V33	IO_L5P_T0U_N8_AD14P_70		
U32	IO_L6N_T0U_N11_AD6N_70		
V32	IO_L6P_T0U_N10_AD6P_70		
P35	IO_L7N_T1L_N1_QBC_AD13N_70		
R35	IO_L7P_T1L_N0_QBC_AD13P_70		
P31	IO_L8N_T1L_N3_AD5N_70		
R31	IO_L8P_T1L_N2_AD5P_70		
R37	IO_L9N_T1L_N5_AD12N_70		
R36	IO_L9P_T1L_N4_AD12P_70		
T35	IO_T0U_N12_VRP_70		
T34	IO_T1U_N12_70		
P36	IO_T2U_N12_70		
L32	IO_T3U_N12_70		

FPGA_VU13P_A2577

V_1V8

THE "F1F2_SPARE" SIGNALS ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "F1F2_SPARE0" AND "F1F2_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE FPGA

APOLLO CM W/ DUAL A2577, MK1

Title: 5.07 F1 UTILITY BANKS

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5.08 FPGA#1 TEST CONNECTOR

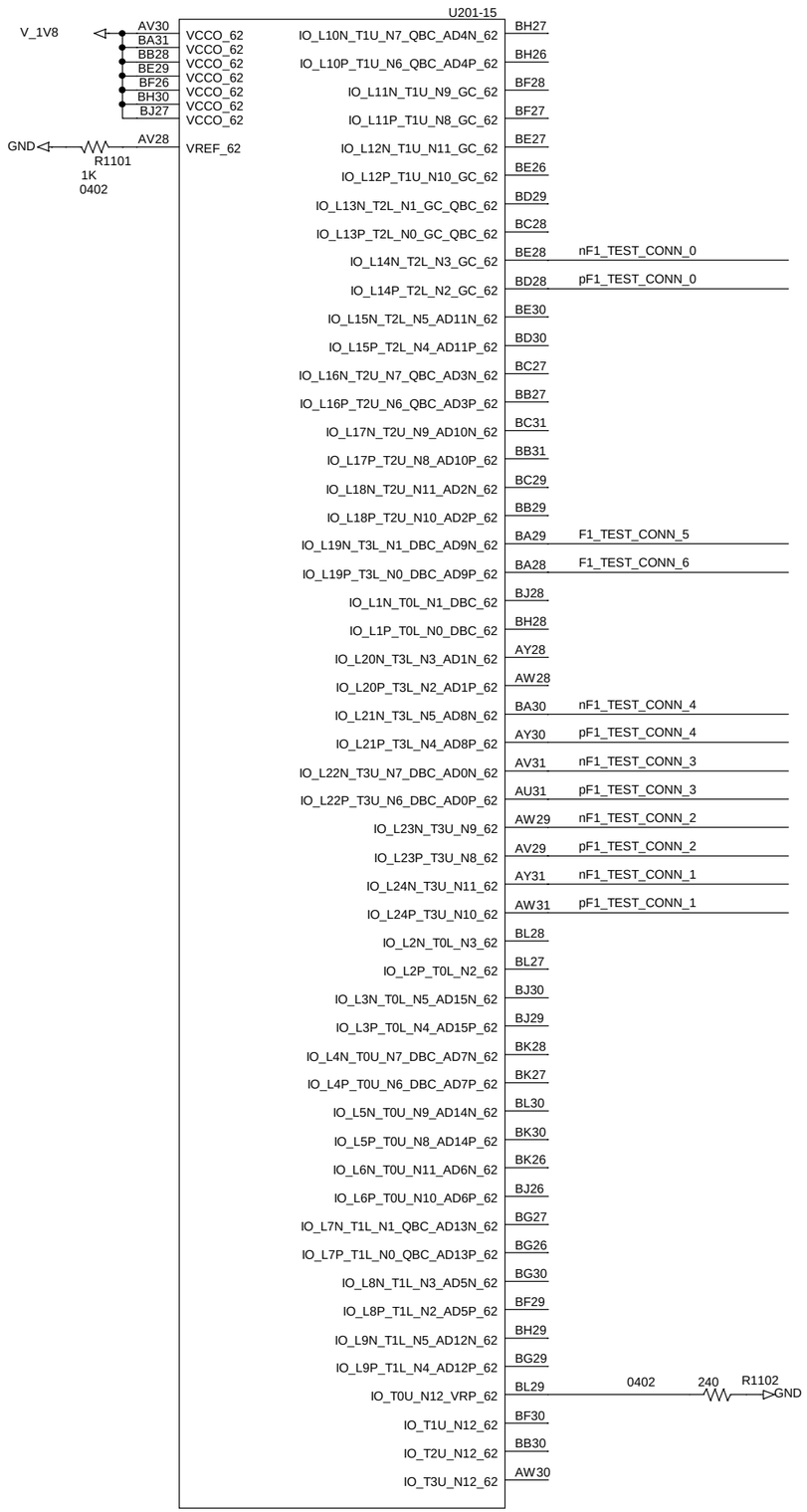
THIS CONNECTOR IS LOCATED ON THE FRONT PANEL. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

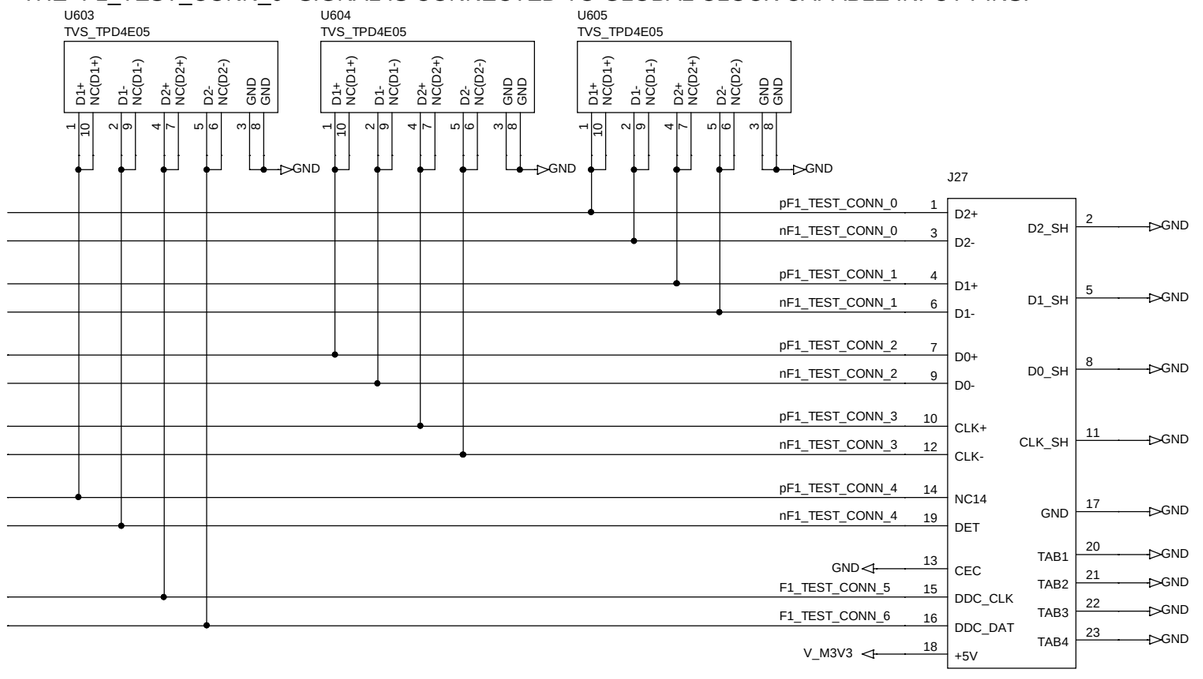
TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

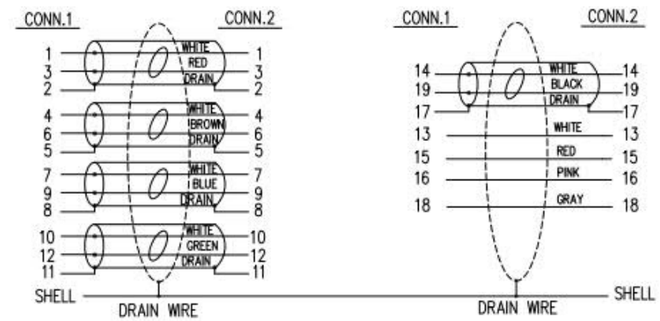
THE "F1_TEST_CONN_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.

THESE SIGNALS MAY BE ASSIGNED TO DIFFERENT PINS OR A DIFFERENT BLOCK DURING LAYOUT TO SIMPLIFY ROUTING. KEEP FPGA CLOCK INPUTS ON "GC" PINS.





PIN ASSIGNMENT



APOLLO CM W/ DUAL A2577, MK1		
Title: 5.08 FPGA#1 TEST CONNECTOR		
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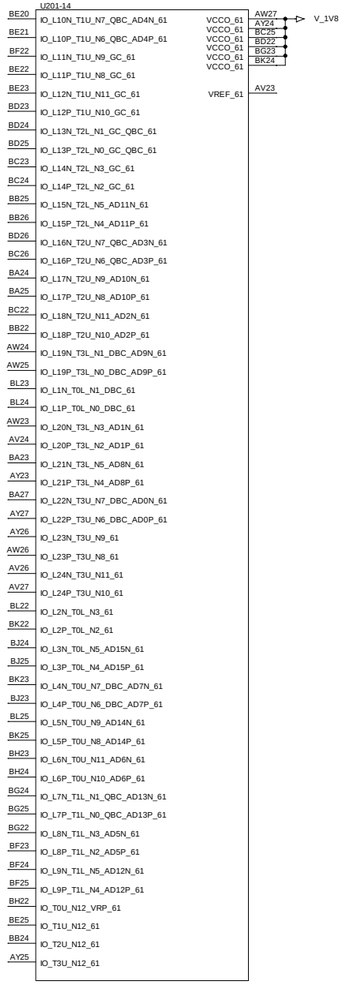
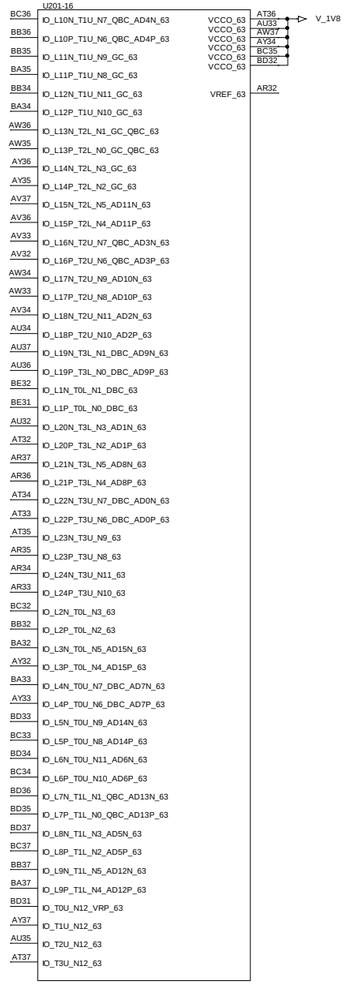
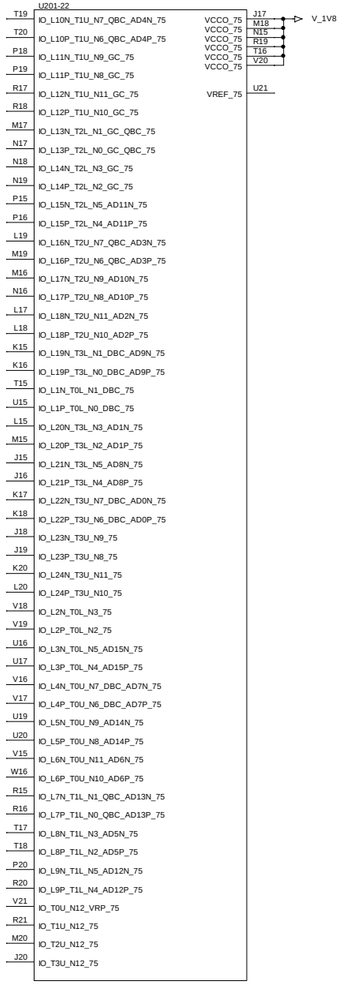
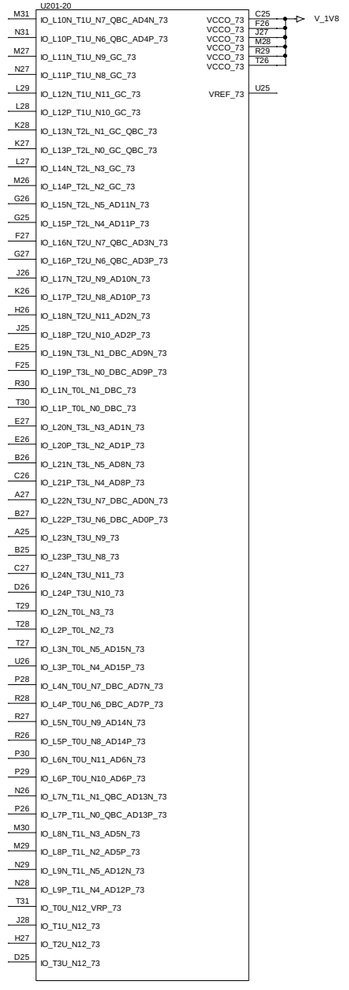
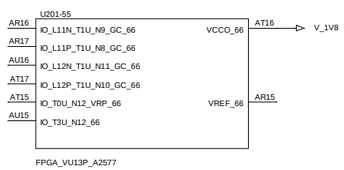
5.99: F1 UNUSED BLOCKS

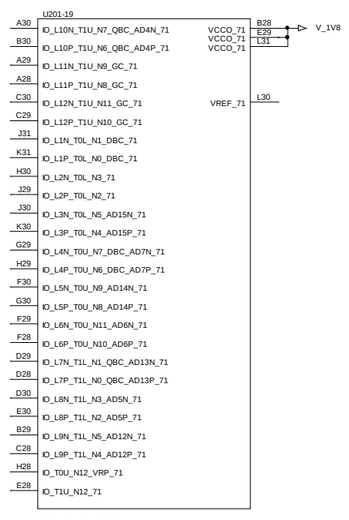












F1 UNUSED BLOCKS

APOLLO CM W/ DUAL A2577, MK1		
Title: 5.99: F1 UNUSED BLOCKS		
Size	Document Number: 6089-119	Rev: A
Date: Wednesday, February 17, 2021	Sheet 47 of 80	

6.01: FPGA#2 GND

U202-1 FPGA_VU13P_A2577

A13	GND	GND	AE12
A16	GND	GND	AE16
A17	GND	GND	AE18
A18	GND	GND	AE20
A21	GND	GND	AE22
A26	GND	GND	AE24
A31	GND	GND	AE26
A34	GND	GND	AE28
A35	GND	GND	AE3
A36	GND	GND	AE30
A39	GND	GND	AE32
A4	GND	GND	AE34
A43	GND	GND	AE36
A45	GND	GND	AE38
A48	GND	GND	AE4
A7	GND	GND	AE40
A9	GND	GND	AE43
AA12	GND	GND	AE47
AA14	GND	GND	AE48
AA16	GND	GND	AE49
AA18	GND	GND	AE5
AA20	GND	GND	AE9
AA22	GND	GND	AF1
AA24	GND	GND	AF10
AA26	GND	GND	AF12
AA28	GND	GND	AF15
AA3	GND	GND	AF17
AA30	GND	GND	AF19
AA32	GND	GND	AF2
AA34	GND	GND	AF21
AA36	GND	GND	AF23
AA38	GND	GND	AF25
AA4	GND	GND	AF27
AA40	GND	GND	AF29
AA43	GND	GND	AF31
AA47	GND	GND	AF33
AA48	GND	GND	AF35
AA49	GND	GND	AF37
AA5	GND	GND	AF39
AA9	GND	GND	AF40
AB1	GND	GND	AF42
AB10	GND	GND	AF45
AB15	GND	GND	AF47
AB17	GND	GND	AF5
AB19	GND	GND	AF50
AB2	GND	GND	AF51
AB21	GND	GND	AF7
AB23	GND	GND	AG12
AB25	GND	GND	AG16
AB27	GND	GND	AG20
AB29	GND	GND	AG22
AB31	GND	GND	AG24
AB33	GND	GND	AG26
AB35	GND	GND	AG28
AB37	GND	GND	AG3
AB38	GND	GND	AG30
AB42	GND	GND	AG32
AB45	GND	GND	AG34
AB47	GND	GND	AG36
AB5	GND	GND	AG38
AB50	GND	GND	AG4
AB51	GND	GND	AG40
AB7	GND	GND	AG44
AC14	GND	GND	AG47
AC16	GND	GND	AG48
AC18	GND	GND	AG49
AC20	GND	GND	AG5
AC22	GND	GND	AG8
AC24	GND	GND	AH1
AC26	GND	GND	AH11
AC28	GND	GND	AH12
AC3	GND	GND	AH15
AC30	GND	GND	AH17
AC32	GND	GND	AH2
AC34	GND	GND	AH21
AC36	GND	GND	AH23
AC38	GND	GND	AH25
AC39	GND	GND	AH27
AC4	GND	GND	AH29
AC44	GND	GND	AH31
AC47	GND	GND	AH33
AC48	GND	GND	AH35
AC49	GND	GND	AH37
AC5	GND	GND	AH39
AC8	GND	GND	AH40
AD1	GND	GND	AH41
AD11	GND	GND	AH46
AD12	GND	GND	AH47
AD15	GND	GND	AH5
AD17	GND	GND	AH50
AD19	GND	GND	AH51
AD2	GND	GND	AH6
AD21	GND	GND	AJ14
AD23	GND	GND	AJ16
AD25	GND	GND	AJ20
AD27	GND	GND	AJ22
AD29	GND	GND	AJ24
AD31	GND	GND	AJ26
AD33	GND	GND	AJ28
AD35	GND	GND	AJ3
AD37	GND	GND	AJ30
AD39	GND	GND	AJ32
AD40	GND	GND	AJ34
AD41	GND	GND	AJ36
AD46	GND	GND	AJ38
AD47	GND	GND	AJ39
AD5	GND	GND	AJ47
AD50	GND	GND	AJ43
AD51	GND	GND	AJ48
AD6	GND	GND	AJ4

GND GND

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AJ49	GND	GND	AP42
AJ5	GND	GND	AP45
AJ9	GND	GND	AP47
AK1	GND	GND	AP5
AK10	GND	GND	AP50
AK15	GND	GND	AP51
AK17	GND	GND	AP7
AK2	GND	GND	AR12
AK21	GND	GND	AR14
AK23	GND	GND	AR22
AK25	GND	GND	AR24
AK27	GND	GND	AR26
AK29	GND	GND	AR28
AK31	GND	GND	AR3
AK33	GND	GND	AR30
AK35	GND	GND	AR38
AK37	GND	GND	AR4
AK38	GND	GND	AR40
AK42	GND	GND	AR44
AK45	GND	GND	AR47
AK47	GND	GND	AR48
AK5	GND	GND	AR49
AK50	GND	GND	AR5
AK51	GND	GND	AR8
AK7	GND	GND	AT1
AL12	GND	GND	AT11
AL14	GND	GND	AT2
AL16	GND	GND	AT21
AL18	GND	GND	AT23
AL20	GND	GND	AT25
AL22	GND	GND	AT27
AL24	GND	GND	AT29
AL26	GND	GND	AT31
AL28	GND	GND	AT38
AL3	GND	GND	AT41
AL30	GND	GND	AT46
AL32	GND	GND	AT47
AL34	GND	GND	AT5
AL36	GND	GND	AT50
AL38	GND	GND	AT51
AL4	GND	GND	AT6
AL40	GND	GND	AU13
AL44	GND	GND	AU14
AL47	GND	GND	AU18
AL48	GND	GND	AU24
AL49	GND	GND	AU26
AL5	GND	GND	AU28
AL8	GND	GND	AU3
AM1	GND	GND	AU30
AM11	GND	GND	AU38
AM15	GND	GND	AU39
AM17	GND	GND	AU4
AM19	GND	GND	AU43
AM2	GND	GND	AU47
AM21	GND	GND	AU48
AM23	GND	GND	AU49
AM25	GND	GND	AU5
AM27	GND	GND	AU9
AM29	GND	GND	AV1
AM31	GND	GND	AV10
AM33	GND	GND	AV15
AM35	GND	GND	AV2
AM37	GND	GND	AV25
AM38	GND	GND	AV35
AM41	GND	GND	AV38
AM46	GND	GND	AV42
AM47	GND	GND	AV45
AM5	GND	GND	AV47
AM50	GND	GND	AV5
AM51	GND	GND	AV50
AM6	GND	GND	AV51
AN12	GND	GND	AV7
AN14	GND	GND	AW12
AN16	GND	GND	AW14
AN18	GND	GND	AW22
AN20	GND	GND	AW3
AN22	GND	GND	AW32
AN24	GND	GND	AW38
AN26	GND	GND	AW4
AN28	GND	GND	AW40
AN3	GND	GND	AW44
AN30	GND	GND	AW47
AN32	GND	GND	AW48
AN34	GND	GND	AW49
AN36	GND	GND	AW5
AN38	GND	GND	AW8
AN4	GND	GND	AY1
AN40	GND	GND	AY11
AN43	GND	GND	AY19
AN47	GND	GND	AY2
AN48	GND	GND	AY29
AN49	GND	GND	AY38
AN5	GND	GND	AY41
AN9	GND	GND	AY46
AP1	GND	GND	AY47
AP10	GND	GND	AY5
AP15	GND	GND	AY50
AP17	GND	GND	AY51
AP19	GND	GND	AY6
AP2	GND	GND	B10
AP21	GND	GND	B14
AP23	GND	GND	B16
AP25	GND	GND	B19
AP27	GND	GND	B20
AP29	GND	GND	B21
AP31	GND	GND	B23
AP33	GND	GND	B3
AP35	GND	GND	B31
AP37	GND	GND	B32
AP38	GND	GND	B33

GND GND

U202-3 FPGA_VU13P_A2577

B36	GND	GND	BG12
B38	GND	GND	BG16
B4	GND	GND	BG17
B42	GND	GND	BG18
B45	GND	GND	BG21
B46	GND	GND	BG28
B47	GND	GND	BG3
B48	GND	GND	BG31
B49	GND	GND	BG34
B5	GND	GND	BG35
B6	GND	GND	BG36
B7	GND	GND	BG4
BA12	GND	GND	BG40
BA14	GND	GND	BG44
BA16	GND	GND	BG45
BA26	GND	GND	BG48
BA3	GND	GND	BG49
BA36	GND	GND	BG7
BA38	GND	GND	BG8
BA4	GND	GND	BH1
BA40	GND	GND	BH11
BA43	GND	GND	BH15
BA47	GND	GND	BH16
BA48	GND	GND	BH19
BA49	GND	GND	BH2
BA5	GND	GND	BH20
BA9	GND	GND	BH21
BB1	GND	GND	BH25
BB10	GND	GND	BH31
BB2	GND	GND	BH32
BB23	GND	GND	BH33
BB33	GND	GND	BH36
BB38	GND	GND	BH37
BB42	GND	GND	BH41
BB45	GND	GND	BH45
BB47	GND	GND	BH46
BB5	GND	GND	BH47
BB50	GND	GND	BH5
BB51	GND	GND	BH50
BB7	GND	GND	BH51
BC12	GND	GND	BH6
BC14	GND	GND	BH7
BC20	GND	GND	BJ13
BC3	GND	GND	BJ16
BC30	GND	GND	BJ17
BC38	GND	GND	BJ18
BC4	GND	GND	BJ2
BC40	GND	GND	BJ21
BC44	GND	GND	BJ22
BC47	GND	GND	BJ3
BC48	GND	GND	BJ31
BC49	GND	GND	BJ34
BC5	GND	GND	BJ35
BC8	GND	GND	BJ36
BD1	GND	GND	BJ39
BD11	GND	GND	BJ4
BD14	GND	GND	BJ43
BD2	GND	GND	BJ45
BD27	GND	GND	BJ48
BD38	GND	GND	BJ49
BD41	GND	GND	BJ50
BD46	GND	GND	BJ7
BD47	GND	GND	BJ9
BD5	GND	GND	BK10
BD50	GND	GND	BK14
BD51	GND	GND	BK16
BD6	GND	GND	BK19
BE12	GND	GND	BK20
BE14	GND	GND	BK21
BE15	GND	GND	BK29
BE16	GND	GND	BK3
BE17	GND	GND	BK31
BE18	GND	GND	BK32
BE19	GND	GND	BK33
BE24	GND	GND	BK36
BE3	GND	GND	BK38
BE33	GND	GND	BK4
BE34	GND	GND	BK42
BE35	GND	GND	BK45
BE36	GND	GND	BK46
BE37	GND	GND	BK47
BE38	GND	GND	BK48
BE4	GND	GND	BK49
BE40	GND	GND	BK5
BE43	GND	GND	BK6
BE47	GND	GND	BK7
BE48	GND	GND	BL12
BE49	GND	GND	BL16
BE5	GND	GND	BL17
BE9	GND	GND	BL18
BF1	GND	GND	BL21
BF10	GND	GND	BL26
BF16	GND	GND	BL31
BF19	GND	GND	BL34
BF2	GND	GND	BL35
BF20	GND	GND	BL36
BF21	GND	GND	BL4
BF31	GND	GND	BL40
BF32	GND	GND	BL44
BF33	GND	GND	BL45
BF36	GND	GND	BL48
BF42	GND	GND	BL7
BF45	GND	GND	BL8
BF46	GND	GND	C12
BF47	GND	GND	C16
BF5	GND	GND	C17
BF50	GND	GND	C18
BF51	GND	GND	C2
BF6	GND	GND	C21
BF7	GND	GND	C3

GND GND

U202-4 FPGA_VU13P_A2577

C31	GND	GND	H35
C34	GND	GND	H36
C35	GND	GND	H37
C36	GND	GND	H38
C4	GND	GND	H41
C40	GND	GND	H46
C44	GND	GND	H47
C45	GND	GND	H5
C48	GND	GND	H50
C49	GND	GND	H51
C50	GND	GND	H6
C7	GND	GND	J12
C8	GND	GND	J14
D1	GND	GND	J22
D11	GND	GND	J3
D15	GND	GND	J38
D16	GND	GND	J4
D19	GND	GND	J40
D2	GND	GND	J43
D20	GND	GND	J47
D21	GND	GND	J48
D27	GND	GND	J49
D31	GND	GND	J5
D32	GND	GND	J9
D33	GND	GND	K1
D36	GND	GND	K10
D37	GND	GND	K14
D41	GND	GND	K19
D45	GND	GND	K2
D46	GND	GND	K29
D47	GND	GND	K38
D5	GND	GND	K42
D50	GND	GND	K45
D51	GND	GND	K47
D6	GND	GND	K5
D7	GND	GND	K50
E12	GND	GND	K51
E16	GND	GND	K7
E17	GND	GND	L12
E18	GND	GND	L14
E21	GND	GND	L16
E24	GND	GND	L26
E3	GND	GND	L3
E31	GND	GND	L36
E34	GND	GND	L38
E35	GND	GND	L4
E36	GND	GND	L40
E39	GND	GND	L44
E4	GND	GND	L47
E43	GND	GND	L48
E45	GND	GND	L49
E48	GND	GND	L5
E49	GND	GND	L8
E7	GND	GND	M1
E9	GND	GND	M11
F1	GND	GND	M2
F10	GND	GND	M23
F14	GND	GND	M33
F16	GND	GND	M38
F19	GND	GND	M41
F2	GND	GND	M46
F20	GND	GND	M47
F21	GND	GND	M5
F31	GND	GND	M50
F32	GND	GND	M51
F33	GND	GND	M6
F36	GND	GND	N13
F38	GND	GND	N14
F42	GND	GND	N20
F45	GND	GND	N3
F46	GND	GND	N30
F47	GND	GND	N38
F5	GND	GND	N39
F50	GND	GND	N4
F51	GND	GND	N43
F6	GND	GND	N47
F7	GND	GND	N48
G12	GND	GND	N49
G16	GND	GND	N5
G18	GND	GND	N9
G21	GND	GND	P1
G28	GND	GND	P10
G3	GND	GND	P17
G31	GND	GND	P2
G34	GND	GND	P27
G36	GND	GND	P37
G4	GND	GND	P38
G40	GND	GND	P42
G44	GND	GND	P45
G47	GND	GND	P47
G48	GND	GND	P5
G49	GND	GND	P50
G5	GND	GND	P51
G8	GND	GND	P7
H1	GND	GND	R12
H11	GND	GND	R14
H14	GND	GND	R24
H15	GND	GND	R3
H16	GND	GND	R34
H17	GND	GND	R38
H18	GND	GND	R4
H19	GND	GND	R40
H2	GND	GND	R44
H20	GND	GND	R47
H21	GND	GND	R48
H25	GND	GND	R49
H31	GND	GND	R5
H32	GND	GND	R8
H33	GND	GND	T1
H34	GND	GND	T11

GND GND

U202-5 FPGA_VU13P_A2577

T2	GND
T21	GND
T38	GND
T41	GND
T46	GND
T47	GND
T5	GND
T50	GND
T51	GND
T6	GND
U13	GND
U14	GND
U18	GND
U28	GND
U3	GND
U30	GND
U38	GND
U39	GND
U4	GND
U43	GND
U47	GND
U48	GND
U49	GND
U5	GND
U9	GND
V1	GND
V10	GND
V2	GND
V23	GND
V25	GND
V27	GND
V29	GND
V31	GND
V38	GND
V42	GND
V45	GND
V47	GND
V5	GND
V50	GND
V51	GND
V7	GND
W12	GND
W14	GND
W18	GND
W20	GND
W22	GND
W24	GND
W26	GND
W28	GND
W3	GND
W30	GND
W34	GND
W36	GND
W38	GND
W4	GND
W40	GND
W44	GND
W47	GND
W48	GND
W49	GND
W5	GND
W8	GND
Y1	GND
Y11	GND
Y15	GND
Y17	GND
Y19	GND
Y2	GND
Y21	GND
Y23	GND
Y25	GND
Y27	GND
Y29	GND
Y31	GND
Y33	GND
Y35	GND
Y37	GND
Y38	GND
Y41	GND
Y46	GND
Y47	GND
Y5	GND
Y50	GND
Y51	GND

GND

R1121 10K 0603

V_M3V3

GND Y6

/F2_INSTALLED
22

IF THE FPGA IS INSTALLED, THEN THE ACTIVE-LO "/F2_INSTALLED" SIGNAL WILL BE PULLED TO GND. IF THE FPGA IS NOT INSTALLED, THE SIGNAL WILL BE HI.

ANY FPGA GND PIN CAN BE USED.

APOLLO CM W/ DUAL A2577, MK1

Title
6.01: FPGA#2 GND

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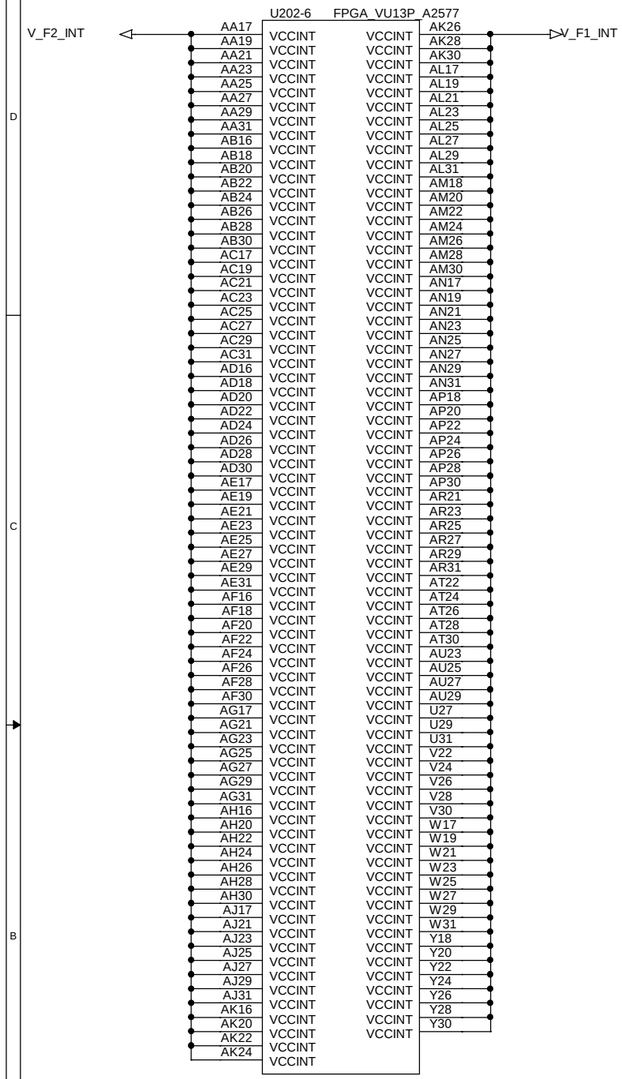
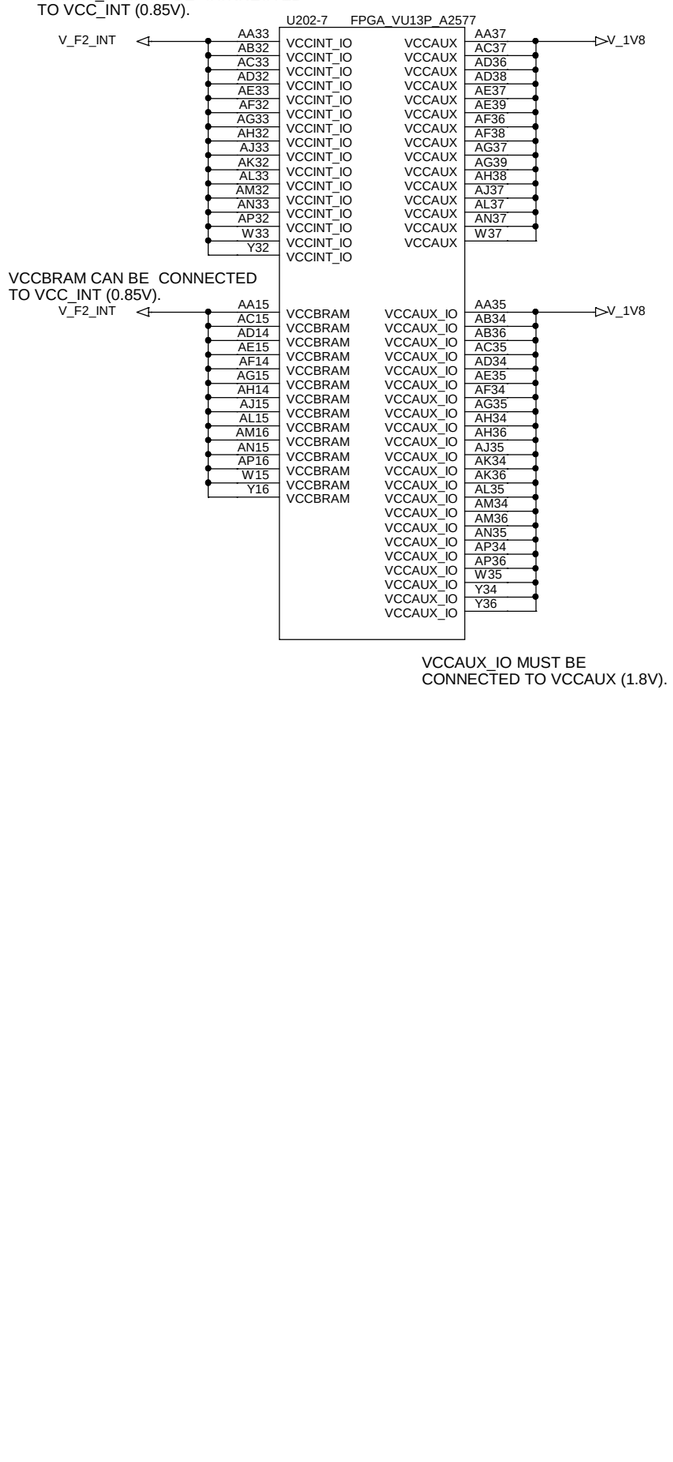
6.02: FPGA#2 POWER INTERNAL

VCCINT MUST BE 0.85V.

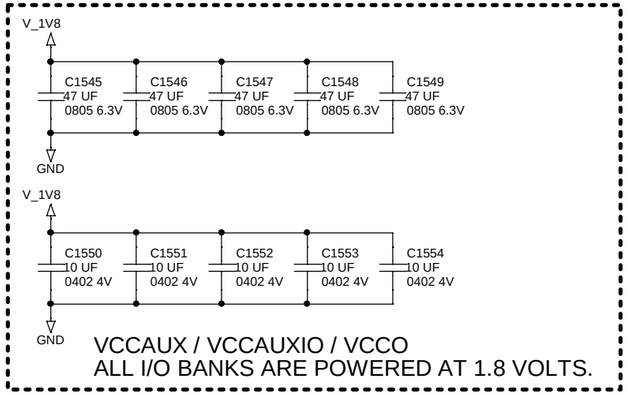


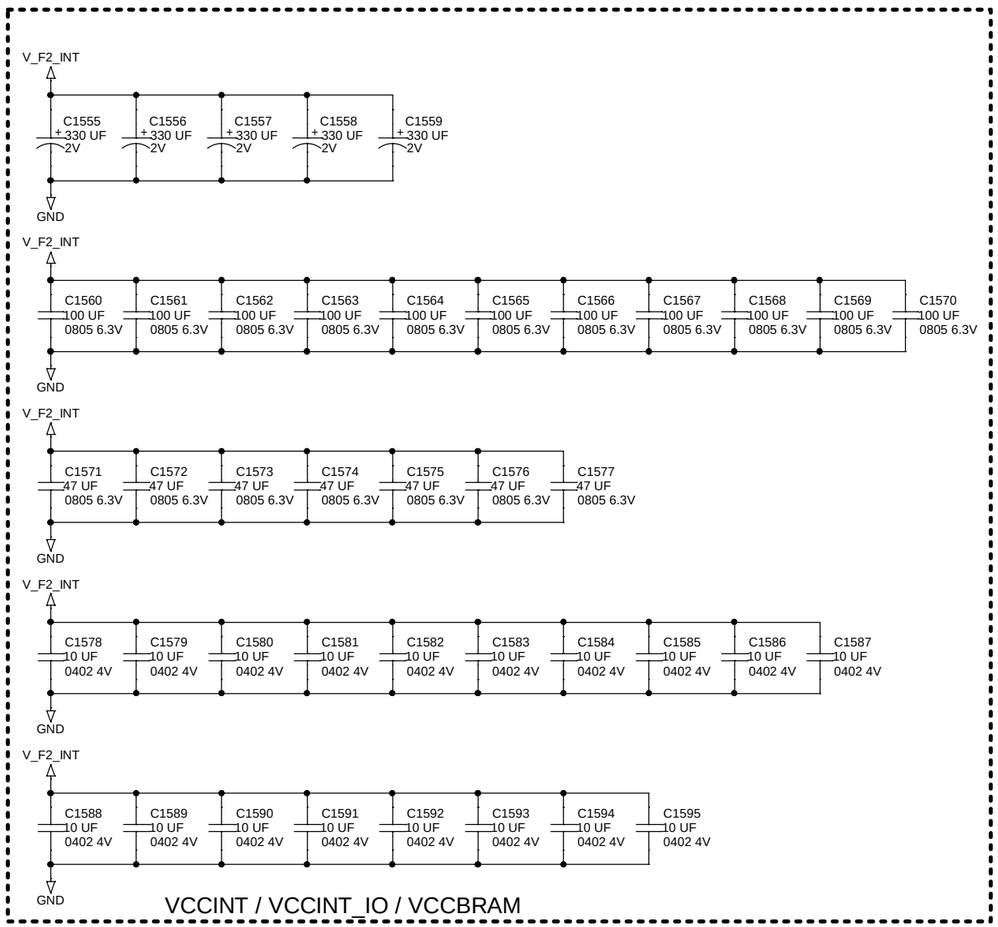
VCCINT_IO MUST BE CONNECTED TO VCC_INT (0.85V).

VCCBRAM CAN BE CONNECTED TO VCC_INT (0.85V).



VCCAUX_IO MUST BE CONNECTED TO VCCAUX (1.8V).





BYPASS CAPACITOR VALUES AND QUANTITIES FROM "UG583 UltraScale Architecture PCB Design"

APOLLO CM W/ DUAL A2577, MK1		
Title: 6.02: FPGA#2 POWER INTERNAL		
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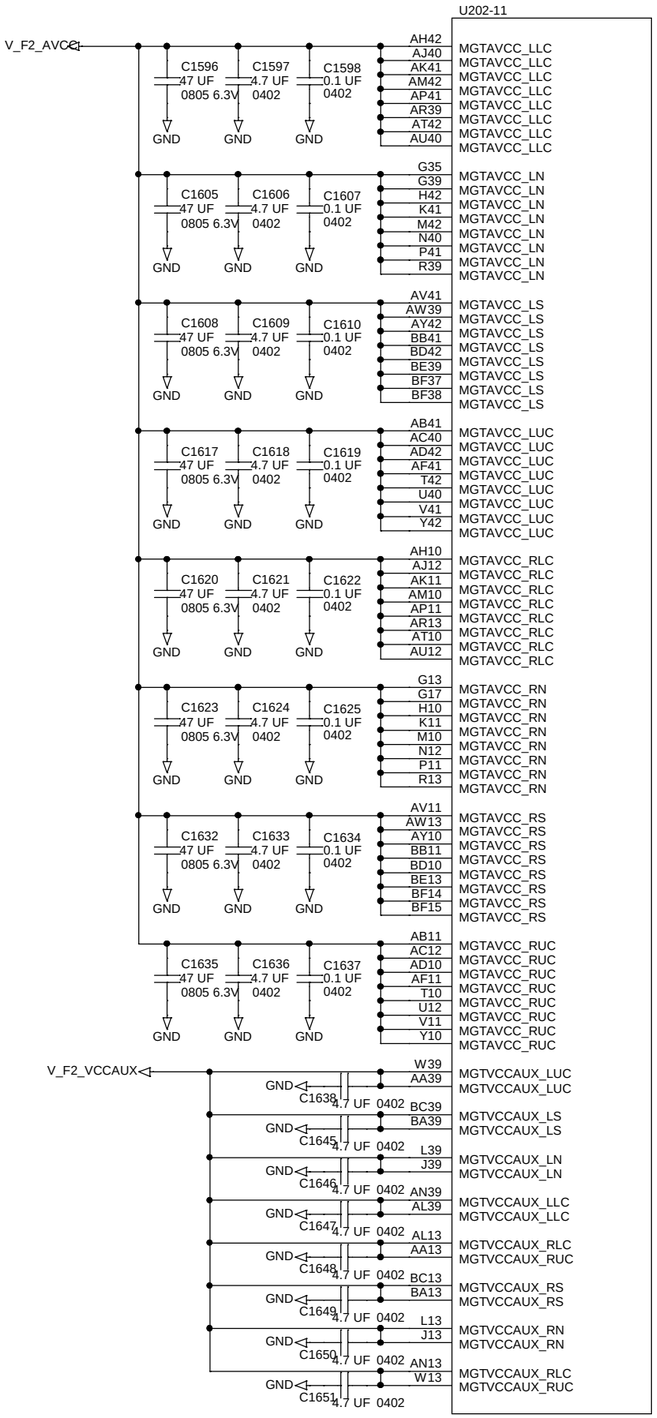
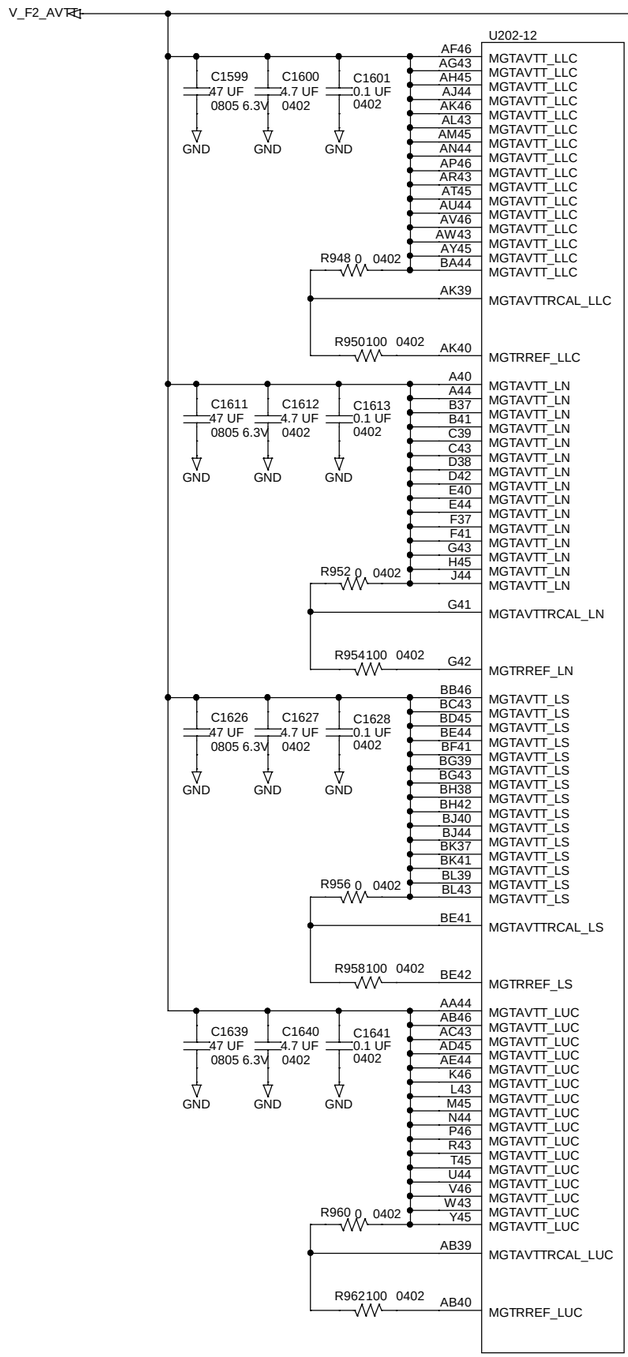
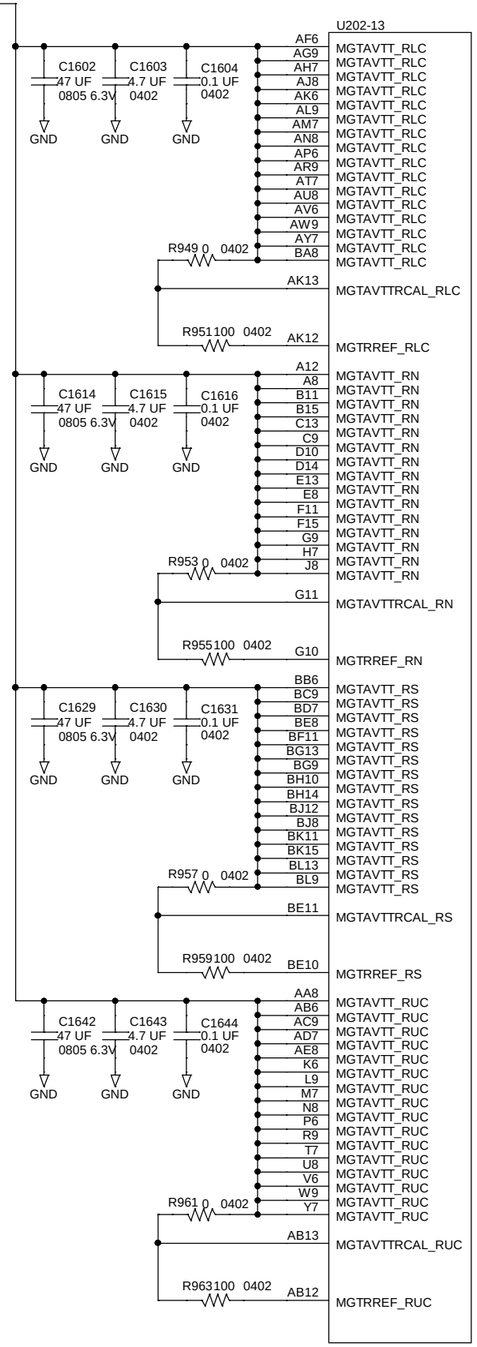
6.03: FPGA#2 GTY TRANSCEIVER POWER







REFER TO THE GTY USER GUIDE FOR DETAILS ON TRACE ROUTING FOR THE MGTRREF RESISTOR.

PLACE CAPACITORS AND RESISTORS THAT ARE ON THIS SHEET NEAR THE BGA PINS.

APOLLO CM W/ DUAL A2577, MK1		
Title: 6.03: FPGA#2 GTY TRANSCEIVER POWER		
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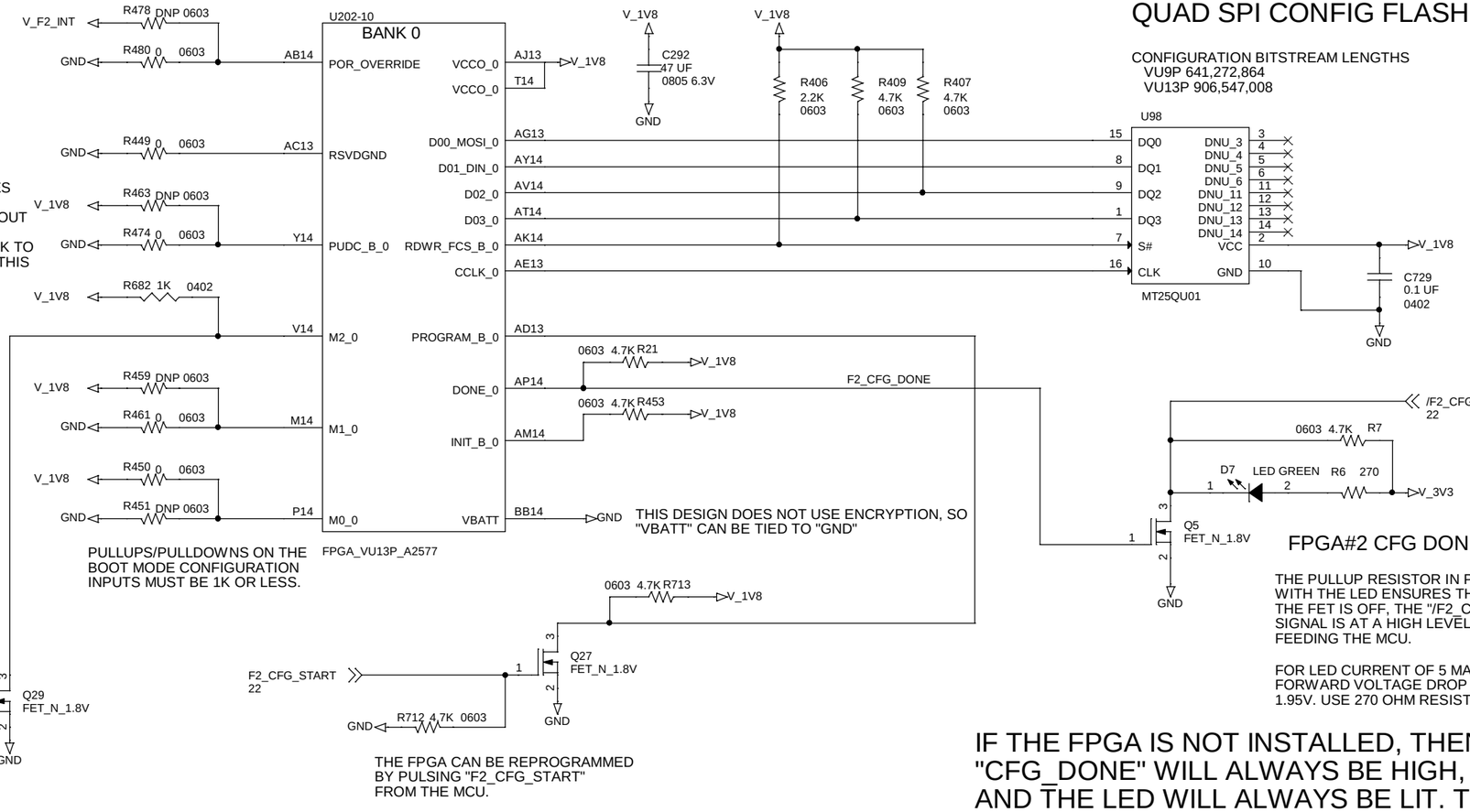
6.04: FPGA#2 CONFIGURATION

MUST BE TIED TO "VCCINT" OR "GND". DO NOT CONNECT TO "VCCO_0". CONNECT TO "GND" FOR STANDARD POR DELAY.

THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.



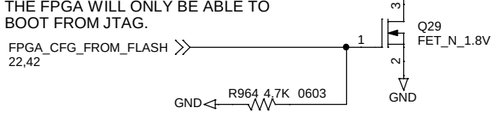
QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
VU9P 641,272,864
VU13P 906,547,008

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

PULLUPS/PULLDOWNS ON THE BOOT MODE CONFIGURATION INPUTS MUST BE 1K OR LESS.

WHEN "FPGA_CFG_FROM_FLASH" IS ASSERTED (HIGH), THE FPGA WILL BE ABLE TO BOOT FROM THE FLASH MEMORY. WHEN IT IS NEGATED (LOW), THE FPGA WILL ONLY BE ABLE TO BOOT FROM JTAG.



THE FPGA CAN BE REPROGRAMMED BY PULSING "F2_CFG_START" FROM THE MCU.

FPGA#2 CFG DONE LED

THE PULLUP RESISTOR IN PARALLEL WITH THE LED ENSURES THAT, WHEN THE FET IS OFF, THE "/F2_CFG_DONE" SIGNAL IS AT A HIGH LEVEL FOR FEEDING THE MCU.

FOR LED CURRENT OF 5 MA, THE FORWARD VOLTAGE DROP IS 1.95V. USE 270 OHM RESISTOR.

IF THE FPGA IS NOT INSTALLED, THEN "CFG_DONE" WILL ALWAYS BE HIGH, AND THE LED WILL ALWAYS BE LIT. THIS IS UNINTENDED AND UNDESIRABLE. CONSIDER ELIMINATING THE FPGA DONE LED,OR ADD A GATE.

APOLLO CM W/ DUAL A2577, MK1		
Title: 6.04: FPGA#2 CONFIGURATION		
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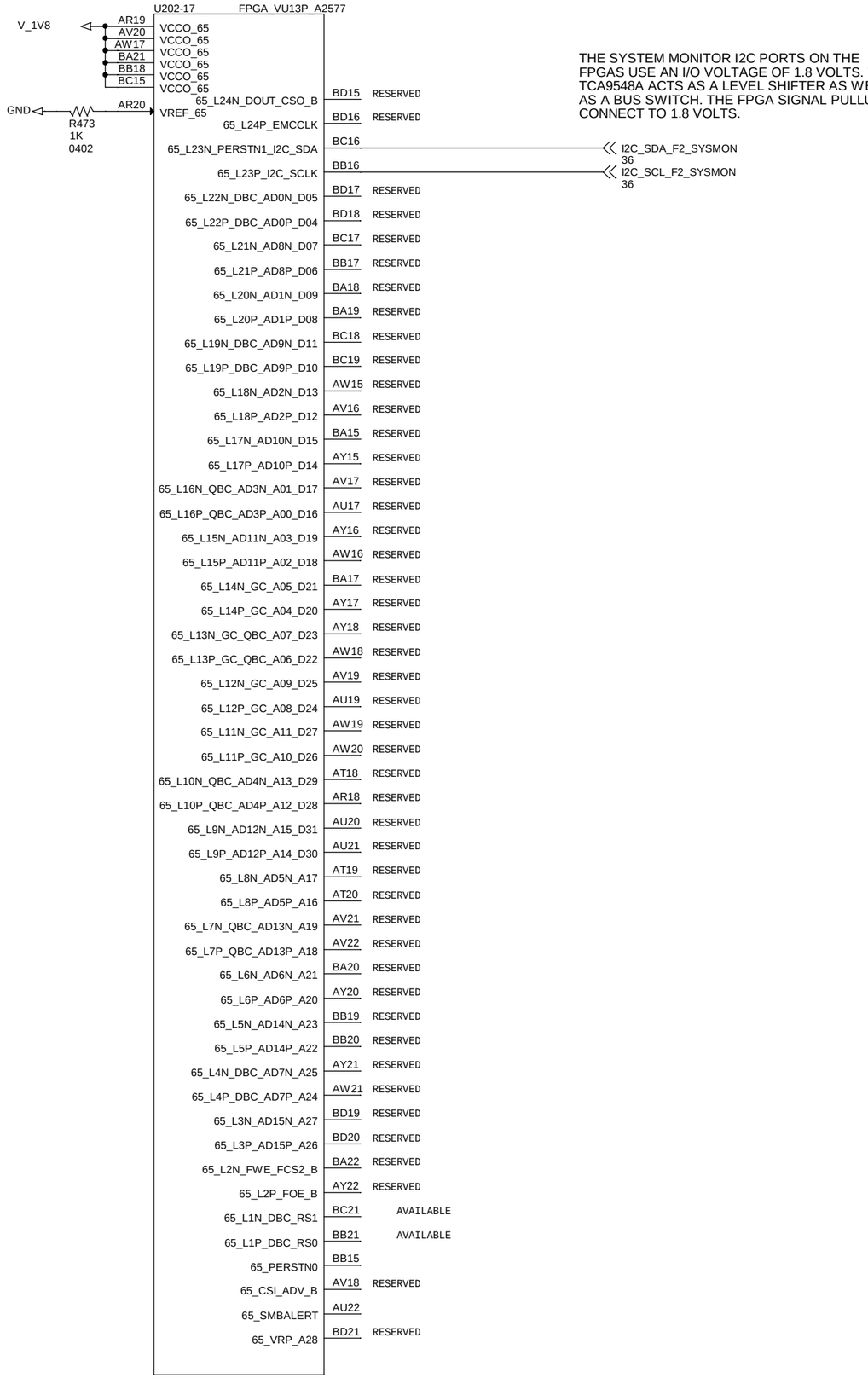
6.05: F2 BANK 65



THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

APOLLO CM W/ DUAL A2577, MK1

Title: 6.05: F2 BANK 65		
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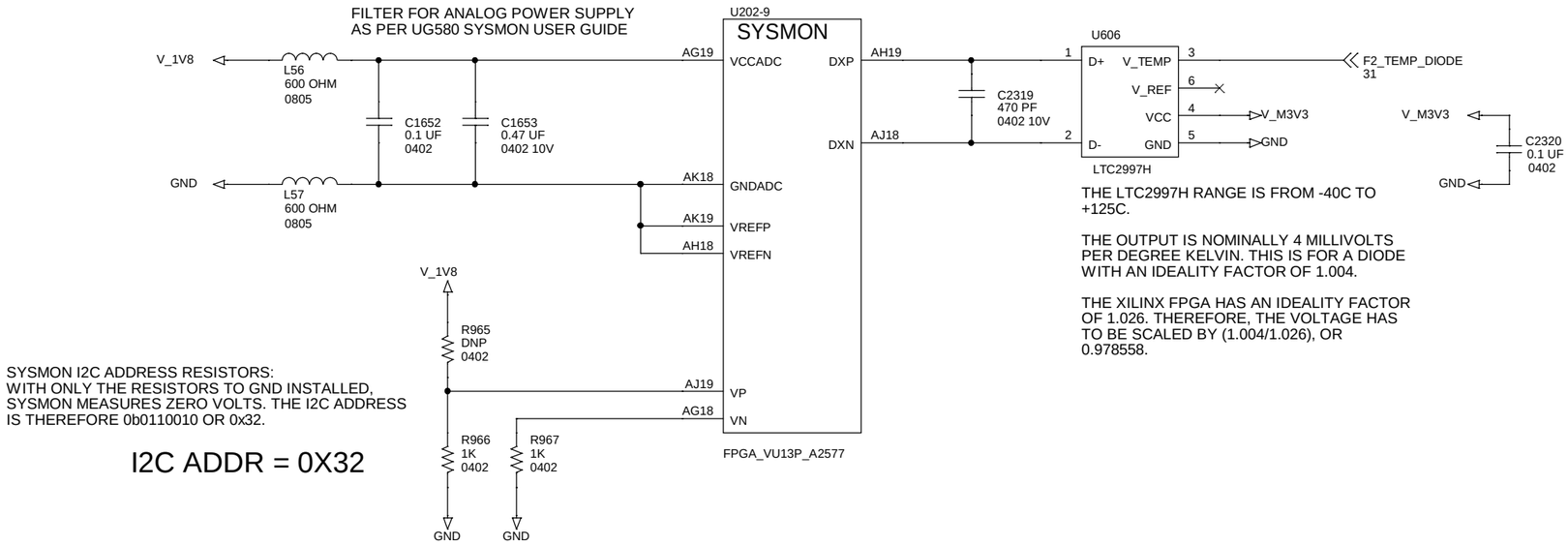
6.06: FPGA#2 SYSTEM MONITOR



APOLLO CM W/ DUAL A2577, MK1			
Title: 6.06: FPGA#2 SYSTEM MONITOR			
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6.07 F2 UTILITY BANKS

F2 LOGIC
TCDS 40MHZ INPUT

ac_nF2_TCDS40_IN 20
ac_pF2_TCDS40_IN 20

THIS IS THE 40 MHZ RECOVERED TCDS CLOCK. THE CLOCK FROM FPGA#2 IS NOT USED ANYWHERE, BUT THE PINS ARE RESERVED. THE "DNP" RESISTOR PADS GIVE THE NETS TWO CONNECTIONS.

THESE ARE LOGIC-CIRCUIT CLOCKS SOURCED FROM AN ON-BOARD OSCILLATOR, EITHER DIRECTLY OR THROUGH A SYNTHESIZER. THEY MUST BE CONNECTED TO A GLOBAL CLOCK INPUT.

VERIFY THAT A GENERIC I2C BUS CAN BE CONNECTED HERE.

THE "F1F2_SPARE" SIGNALS ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "F1F2_SPARE0" AND "F1F2_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE FPGA

U202-21

H23	IO_L10N_T1U_N7_QBC_AD4N_74	VCCO_74	D22
J23	IO_L10P_T1U_N6_QBC_AD4P_74	VCCO_74	G23
J21	IO_L11N_T1U_N9_GC_74	VCCO_74	K24
K21	IO_L11P_T1U_N8_GC_74	VCCO_74	L21
K22	IO_L12N_T1U_N11_GC_74	VCCO_74	N25
K23	IO_L12P_T1U_N10_GC_74	VCCO_74	P22
L22	IO_L13N_T2L_N1_GC_QBC_74		
L23	IO_L13P_T2L_N0_GC_QBC_74	VREF_74	U24
M21	IO_L14N_T2L_N3_GC_74		
M22	IO_L14P_T2L_N2_GC_74		
L24	IO_L15N_T2L_N5_AD11N_74		
M25	IO_L15P_T2L_N4_AD11P_74		
M24	IO_L16N_T2U_N7_QBC_AD3N_74		
N24	IO_L16P_T2U_N6_QBC_AD3P_74		
N21	IO_L17N_T2U_N9_AD10N_74		
N22	IO_L17P_T2U_N8_AD10P_74		
K25	IO_L18N_T2U_N11_AD2N_74		
L25	IO_L18P_T2U_N10_AD2P_74		
T23	IO_L19N_T3L_N1_DBC_AD9N_74		
T24	IO_L19P_T3L_N0_DBC_AD9P_74		
D23	IO_L1N_T0L_N1_DBC_74		
E23	IO_L1P_T0L_N0_DBC_74		
R25	IO_L20N_T3L_N3_AD1N_74		
T25	IO_L20P_T3L_N2_AD1P_74		
U22	IO_L21N_T3L_N5_AD8N_74		
U23	IO_L21P_T3L_N4_AD8P_74		
P24	IO_L22N_T3U_N7_DBC_AD0N_74		
P25	IO_L22P_T3U_N6_DBC_AD0P_74		
R22	IO_L23N_T3U_N9_74		
T22	IO_L23P_T3U_N8_74		
P23	IO_L24N_T3U_N11_74		
R23	IO_L24P_T3U_N10_74		
B24	IO_L2N_T0L_N3_74		
C24	IO_L2P_T0L_N2_74		
A23	IO_L3N_T0L_N5_AD15N_74		
A24	IO_L3P_T0L_N4_AD15P_74		
E22	IO_L4N_T0U_N7_DBC_AD7N_74		
F22	IO_L4P_T0U_N6_DBC_AD7P_74		
C22	IO_L5N_T0U_N9_AD14N_74		
C23	IO_L5P_T0U_N8_AD14P_74		
A22	IO_L6N_T0U_N11_AD6N_74		
B22	IO_L6P_T0U_N10_AD6P_74		
G24	IO_L7N_T1L_N1_QBC_AD13N_74		
H24	IO_L7P_T1L_N0_QBC_AD13P_74		
F23	IO_L8N_T1L_N3_AD5N_74		
F24	IO_L8P_T1L_N2_AD5P_74		
G22	IO_L9N_T1L_N5_AD12N_74		
H22	IO_L9P_T1L_N4_AD12P_74		
D24	IO_T0U_N12_VRP_74		
J24	IO_T1U_N12_74		
N23	IO_T2U_N12_74		
P21	IO_T3U_N12_74		

VCCO_74 = V_1V8

VREF_74 = U24 — R475 1K 0402 — GND

0603 DNP R1204

bc_nF2_TCDS_REC_CLK
bc_pF2_TCDS_REC_CLK

nF1F2_SPARE0 45
pF1F2_SPARE0 45
nF1F2_SPARE2 45
pF1F2_SPARE2 45
nF1F2_SPARE5 45
pF1F2_SPARE5 45
nF1F2_SPARE4 45
pF1F2_SPARE4 45
nF1F2_SPARE8 45
pF1F2_SPARE8 45
nF1F2_SPARE9 45
pF1F2_SPARE9 45
nF1F2_SPARE11 45
pF1F2_SPARE11 45
nF1F2_SPARE12 45
pF1F2_SPARE12 45
nF1F2_SPARE7 45
pF1F2_SPARE7 45
nF1F2_SPARE3 45
pF1F2_SPARE3 45
nF1F2_SPARE1 45
pF1F2_SPARE1 45
nF1F2_SPARE10 45
pF1F2_SPARE10 45
nF1F2_SPARE6 45
pF1F2_SPARE6 45

F2_LED_BLUE 22
F2_LED_RED 22
F2_LED_GREEN 22

GND — R89 240 0402

FPGA_VU13P_A2577

U202-18

T33	IO_L10N_T1U_N7_QBC_AD4N_70	VCCO_70	J37
T32	IO_L10P_T1U_N6_QBC_AD4P_70	VCCO_70	K34
P34	IO_L11N_T1U_N9_GC_70	VCCO_70	N35
P33	IO_L11P_T1U_N8_GC_70	VCCO_70	P32
R33	IO_L12N_T1U_N11_GC_70	VCCO_70	T36
R32	IO_L12P_T1U_N10_GC_70	VCCO_70	U33
M32	IO_L13N_T2L_N1_GC_QBC_70		
N32	IO_L13P_T2L_N0_GC_QBC_70	VREF_70	W32
N34	IO_L14N_T2L_N3_GC_70		
N33	IO_L14P_T2L_N2_GC_70		
N37	IO_L15N_T2L_N5_AD11N_70		
N36	IO_L15P_T2L_N4_AD11P_70		
M35	IO_L16N_T2U_N7_QBC_AD3N_70		
M34	IO_L16P_T2U_N6_QBC_AD3P_70		
M37	IO_L17N_T2U_N9_AD10N_70		
M36	IO_L17P_T2U_N8_AD10P_70		
L34	IO_L18N_T2U_N11_AD2N_70		
L33	IO_L18P_T2U_N10_AD2P_70		
K35	IO_L19N_T3L_N1_DBC_AD9N_70		
L35	IO_L19P_T3L_N0_DBC_AD9P_70		
V37	IO_L1N_T0L_N1_DBC_70		
V36	IO_L1P_T0L_N0_DBC_70		
J33	IO_L20N_T3L_N3_AD1N_70		
J32	IO_L20P_T3L_N2_AD1P_70		
K37	IO_L21N_T3L_N5_AD8N_70		
L37	IO_L21P_T3L_N4_AD8P_70		
K33	IO_L22N_T3U_N7_DBC_AD0N_70		
K32	IO_L22P_T3U_N6_DBC_AD0P_70		
J36	IO_L23N_T3U_N9_70		
K36	IO_L23P_T3U_N8_70		
J35	IO_L24N_T3U_N11_70		
J34	IO_L24P_T3U_N10_70		
T37	IO_L2N_T0L_N3_70		
U37	IO_L2P_T0L_N2_70		
U36	IO_L3N_T0L_N5_AD15N_70		
V35	IO_L3P_T0L_N4_AD15P_70		
U35	IO_L4N_T0U_N7_DBC_AD7N_70		
U34	IO_L4P_T0U_N6_DBC_AD7P_70		
V34	IO_L5N_T0U_N9_AD14N_70		
V33	IO_L5P_T0U_N8_AD14P_70		
U32	IO_L6N_T0U_N11_AD6N_70		
V32	IO_L6P_T0U_N10_AD6P_70		
P35	IO_L7N_T1L_N1_QBC_AD13N_70		
R35	IO_L7P_T1L_N0_QBC_AD13P_70		
P31	IO_L8N_T1L_N3_AD5N_70		
R31	IO_L8P_T1L_N2_AD5P_70		
R37	IO_L9N_T1L_N5_AD12N_70		
R36	IO_L9P_T1L_N4_AD12P_70		
T35	IO_T0U_N12_VRP_70		
T34	IO_T1U_N12_70		
P36	IO_T2U_N12_70		
L32	IO_T3U_N12_70		

VCCO_70 = V_1V8

ac_nF2L_R0_LOG 18
ac_pF2L_R0_LOG 18
ac_nF2R_R0_LOG 18
ac_pF2R_R0_LOG 18
ac_nF2_LOG_OSC 17
ac_pF2_LOG_OSC 17
ac_nF2_UTIL 17
ac_pF2_UTIL 17

lovF2_TO_MCU 22
lovMCU_TO_F2 22
lovF2_C2C_OK 22

I2C_SCL_F2_GENERIC 36
I2C_SDA_F2_GENERIC 36

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APOLLO CM W/ DUAL A2577, MK1	
Title: 6.07 F2 UTILITY BANKS	
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6.08 FPGA#2 TEST CONNECTOR

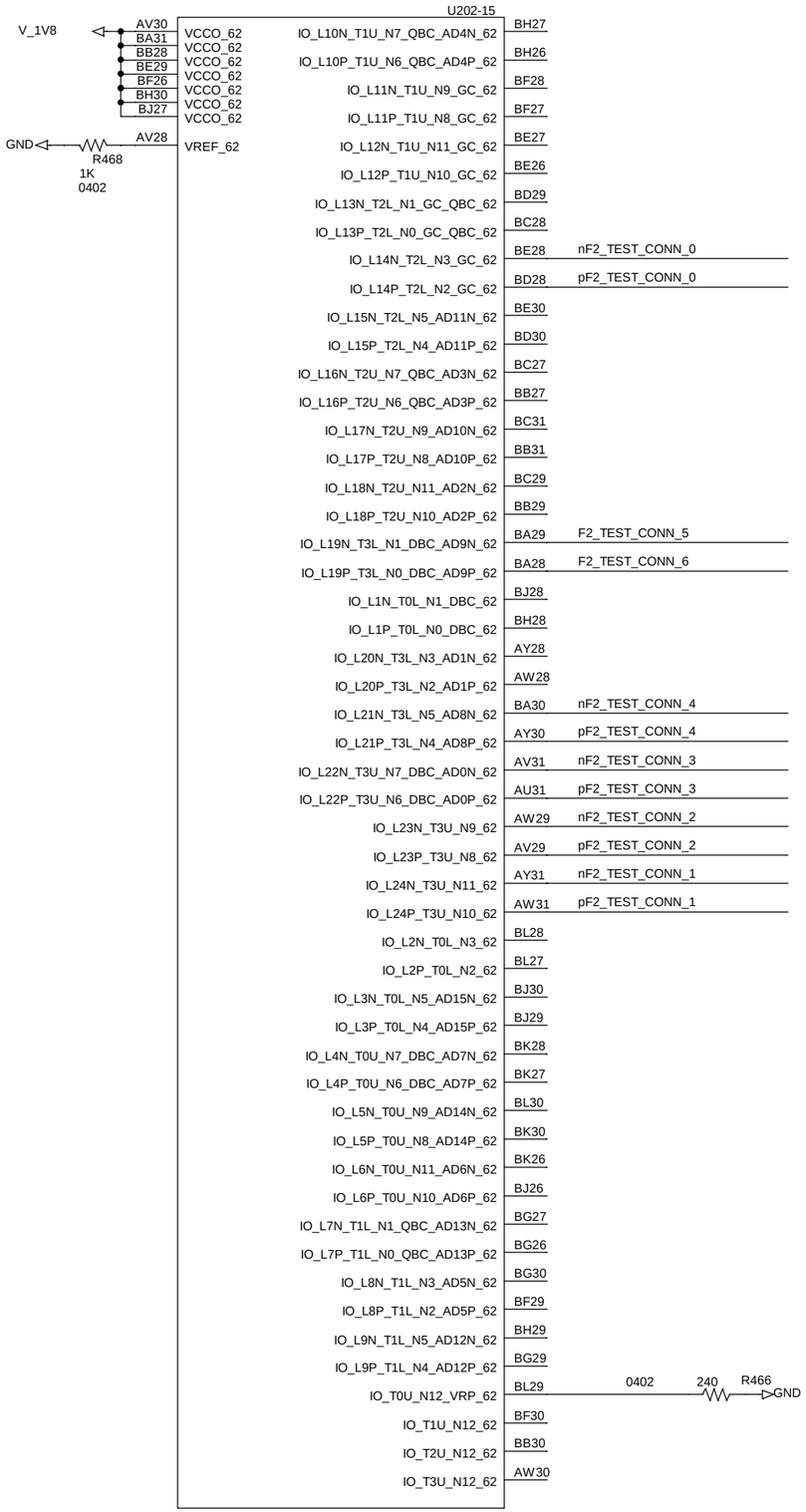
THIS CONNECTOR IS LOCATED ON THE FRONT PANEL. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

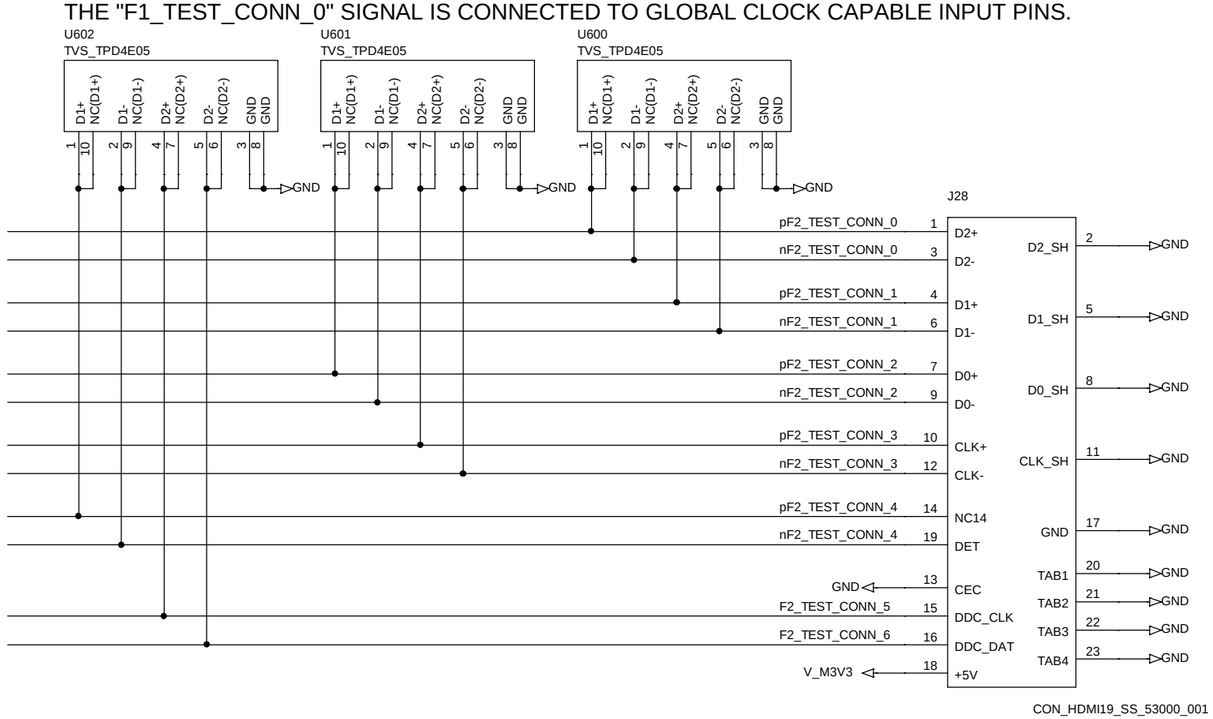
TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "F1_TEST_CONN_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.

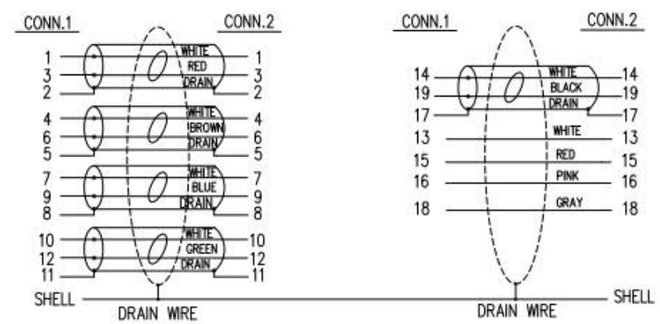
THESE SIGNALS MAY BE ASSIGNED TO DIFFERENT PINS OR A DIFFERENT BLOCK DURING LAYOUT TO SIMPLIFY ROUTING. KEEP FPGA CLOCK INPUTS ON "GC" PINS.





CON_HDMI19_SS_53000_001

PIN ASSIGNMENT



APOLLO CM W/ DUAL A2577, MK1		
Title: 6.08 FPGA#2 TEST CONNECTOR		
Size	Document Number: 6089-119	Rev: A
Date: Wednesday, February 17, 2021	Sheet 55 of 80	

U202-14

BE20	IO_L10N_T1U_N7_QBC_AD4N_61	VCCO_61	AW27	V_1V8
BE21	IO_L10P_T1U_N6_QBC_AD4P_61	VCCO_61	AY24	
BF22	IO_L11N_T1U_N9_GC_61	VCCO_61	BC25	
BE22	IO_L11P_T1U_N8_GC_61	VCCO_61	BD22	
BE23	IO_L12N_T1U_N11_GC_61	VCCO_61	BG23	
BD23	IO_L12P_T1U_N10_GC_61	VCCO_61	BK24	
BD24	IO_L13N_T2L_N1_GC_QBC_61	VREF_61	AV23	
BD25	IO_L13P_T2L_N0_GC_QBC_61			
BC23	IO_L14N_T2L_N3_GC_61			
BC24	IO_L14P_T2L_N2_GC_61			
BB25	IO_L15N_T2L_N5_AD11N_61			
BB26	IO_L15P_T2L_N4_AD11P_61			
BD26	IO_L16N_T2U_N7_QBC_AD3N_61			
BC26	IO_L16P_T2U_N6_QBC_AD3P_61			
BA24	IO_L17N_T2U_N9_AD10N_61			
BA25	IO_L17P_T2U_N8_AD10P_61			
BC22	IO_L18N_T2U_N11_AD2N_61			
BB22	IO_L18P_T2U_N10_AD2P_61			
AW24	IO_L19N_T3L_N1_DBC_AD9N_61			
AW25	IO_L19P_T3L_N0_DBC_AD9P_61			
BL23	IO_L1N_T0L_N1_DBC_61			
BL24	IO_L1P_T0L_N0_DBC_61			
AW23	IO_L20N_T3L_N3_AD1N_61			
AV24	IO_L20P_T3L_N2_AD1P_61			
BA23	IO_L21N_T3L_N5_AD8N_61			
AY23	IO_L21P_T3L_N4_AD8P_61			
BA27	IO_L22N_T3U_N7_DBC_AD0N_61			
AY27	IO_L22P_T3U_N6_DBC_AD0P_61			
AY26	IO_L23N_T3U_N9_61			
AW26	IO_L23P_T3U_N8_61			
AV26	IO_L24N_T3U_N11_61			
AV27	IO_L24P_T3U_N10_61			
BL22	IO_L2N_T0L_N3_61			
BK22	IO_L2P_T0L_N2_61			
BJ24	IO_L3N_T0L_N5_AD15N_61			
BJ25	IO_L3P_T0L_N4_AD15P_61			
BK23	IO_L4N_T0U_N7_DBC_AD7N_61			
BJ23	IO_L4P_T0U_N6_DBC_AD7P_61			
BL25	IO_L5N_T0U_N9_AD14N_61			
BK25	IO_L5P_T0U_N8_AD14P_61			
BH23	IO_L6N_T0U_N11_AD6N_61			
BH24	IO_L6P_T0U_N10_AD6P_61			
BG24	IO_L7N_T1L_N1_QBC_AD13N_61			
BG25	IO_L7P_T1L_N0_QBC_AD13P_61			
BG22	IO_L8N_T1L_N3_AD5N_61			
BF23	IO_L8P_T1L_N2_AD5P_61			
BF24	IO_L9N_T1L_N5_AD12N_61			
BF25	IO_L9P_T1L_N4_AD12P_61			
BH22	IO_T0U_N12_VRP_61			
BE25	IO_T1U_N12_61			
BB24	IO_T2U_N12_61			
AY25	IO_T3U_N12_61			

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U202-16

BC36	IO_L10N_T1U_N7_QBC_AD4N_63	VCCO_63	AT36	V_1V8
BB36	IO_L10P_T1U_N6_QBC_AD4P_63	VCCO_63	AU33	
BB35	IO_L11N_T1U_N9_GC_63	VCCO_63	AW37	
BA35	IO_L11P_T1U_N8_GC_63	VCCO_63	AY34	
BB34	IO_L12N_T1U_N11_GC_63	VCCO_63	BC35	
BA34	IO_L12P_T1U_N10_GC_63	VCCO_63	BD32	
AW36	IO_L13N_T2L_N1_GC_QBC_63	VREF_63	AR32	
AW35	IO_L13P_T2L_N0_GC_QBC_63			
AY36	IO_L14N_T2L_N3_GC_63			
AY35	IO_L14P_T2L_N2_GC_63			
AV37	IO_L15N_T2L_N5_AD11N_63			
AV36	IO_L15P_T2L_N4_AD11P_63			
AV33	IO_L16N_T2U_N7_QBC_AD3N_63			
AV32	IO_L16P_T2U_N6_QBC_AD3P_63			
AW34	IO_L17N_T2U_N9_AD10N_63			
AW33	IO_L17P_T2U_N8_AD10P_63			
AV34	IO_L18N_T2U_N11_AD2N_63			
AU34	IO_L18P_T2U_N10_AD2P_63			
AU37	IO_L19N_T3L_N1_DBC_AD9N_63			
AU36	IO_L19P_T3L_N0_DBC_AD9P_63			
BE32	IO_L1N_T0L_N1_DBC_63			
BE31	IO_L1P_T0L_N0_DBC_63			
AU32	IO_L20N_T3L_N3_AD1N_63			
AT32	IO_L20P_T3L_N2_AD1P_63			
AR37	IO_L21N_T3L_N5_AD8N_63			
AR36	IO_L21P_T3L_N4_AD8P_63			
AT34	IO_L22N_T3U_N7_DBC_AD0N_63			
AT33	IO_L22P_T3U_N6_DBC_AD0P_63			
AT35	IO_L23N_T3U_N9_63			
AR35	IO_L23P_T3U_N8_63			
AR34	IO_L24N_T3U_N11_63			
AR33	IO_L24P_T3U_N10_63			
BC32	IO_L2N_T0L_N3_63			
BB32	IO_L2P_T0L_N2_63			
BA32	IO_L3N_T0L_N5_AD15N_63			
AY32	IO_L3P_T0L_N4_AD15P_63			
BA33	IO_L4N_T0U_N7_DBC_AD7N_63			
AY33	IO_L4P_T0U_N6_DBC_AD7P_63			
BD33	IO_L5N_T0U_N9_AD14N_63			
BC33	IO_L5P_T0U_N8_AD14P_63			
BD34	IO_L6N_T0U_N11_AD6N_63			
BC34	IO_L6P_T0U_N10_AD6P_63			
BD36	IO_L7N_T1L_N1_QBC_AD13N_63			
BD35	IO_L7P_T1L_N0_QBC_AD13P_63			
BD37	IO_L8N_T1L_N3_AD5N_63			
BC37	IO_L8P_T1L_N2_AD5P_63			
BB37	IO_L9N_T1L_N5_AD12N_63			
BA37	IO_L9P_T1L_N4_AD12P_63			
BD31	IO_T0U_N12_VRP_63			
AY37	IO_T1U_N12_63			
AU35	IO_T2U_N12_63			
AT37	IO_T3U_N12_63			

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U202-22

T19	IO_L10N_T1U_N7_QBC_AD4N_75	VCCO_75	J17	V_1V8
T20	IO_L10P_T1U_N6_QBC_AD4P_75	VCCO_75	M18	
P18	IO_L11N_T1U_N9_GC_75	VCCO_75	N15	
P19	IO_L11P_T1U_N8_GC_75	VCCO_75	R19	
R17	IO_L12N_T1U_N11_GC_75	VCCO_75	T16	
R18	IO_L12P_T1U_N10_GC_75	VREF_75	V20	
M17	IO_L13N_T2L_N1_GC_QBC_75		U21	
N17	IO_L13P_T2L_N0_GC_QBC_75			
N18	IO_L14N_T2L_N3_GC_75			
N19	IO_L14P_T2L_N2_GC_75			
P15	IO_L15N_T2L_N5_AD11N_75			
P16	IO_L15P_T2L_N4_AD11P_75			
L19	IO_L16N_T2U_N7_QBC_AD3N_75			
M19	IO_L16P_T2U_N6_QBC_AD3P_75			
M16	IO_L17N_T2U_N9_AD10N_75			
N16	IO_L17P_T2U_N8_AD10P_75			
L17	IO_L18N_T2U_N11_AD2N_75			
L18	IO_L18P_T2U_N10_AD2P_75			
K15	IO_L19N_T3L_N1_DBC_AD9N_75			
K16	IO_L19P_T3L_N0_DBC_AD9P_75			
T15	IO_L1N_T0L_N1_DBC_75			
U15	IO_L1P_T0L_N0_DBC_75			
L15	IO_L20N_T3L_N3_AD1N_75			
M15	IO_L20P_T3L_N2_AD1P_75			
J15	IO_L21N_T3L_N5_AD8N_75			
J16	IO_L21P_T3L_N4_AD8P_75			
K17	IO_L22N_T3U_N7_DBC_AD0N_75			
K18	IO_L22P_T3U_N6_DBC_AD0P_75			
J18	IO_L23N_T3U_N9_75			
J19	IO_L23P_T3U_N8_75			
K20	IO_L24N_T3U_N11_75			
L20	IO_L24P_T3U_N10_75			
V18	IO_L2N_T0L_N3_75			
V19	IO_L2P_T0L_N2_75			
U16	IO_L3N_T0L_N5_AD15N_75			
U17	IO_L3P_T0L_N4_AD15P_75			
V16	IO_L4N_T0U_N7_DBC_AD7N_75			
V17	IO_L4P_T0U_N6_DBC_AD7P_75			
U19	IO_L5N_T0U_N9_AD14N_75			
U20	IO_L5P_T0U_N8_AD14P_75			
V15	IO_L6N_T0U_N11_AD6N_75			
W16	IO_L6P_T0U_N10_AD6P_75			
R15	IO_L7N_T1L_N1_QBC_AD13N_75			
R16	IO_L7P_T1L_N0_QBC_AD13P_75			
T17	IO_L8N_T1L_N3_AD5N_75			
T18	IO_L8P_T1L_N2_AD5P_75			
P20	IO_L9N_T1L_N5_AD12N_75			
R20	IO_L9P_T1L_N4_AD12P_75			
V21	IO_T0U_N12_VRP_75			
R21	IO_T1U_N12_75			
M20	IO_T2U_N12_75			
J20	IO_T3U_N12_75			

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U202-20

M31	IO_L10N_T1U_N7_QBC_AD4N_73	VCCO_73	C25	V_1V8
N31	IO_L10P_T1U_N6_QBC_AD4P_73	VCCO_73	F26	
M27	IO_L11N_T1U_N9_GC_73	VCCO_73	J27	
N27	IO_L11P_T1U_N8_GC_73	VCCO_73	M28	
L29	IO_L12N_T1U_N11_GC_73	VCCO_73	R29	
L28	IO_L12P_T1U_N10_GC_73	VCCO_73	T26	
K28	IO_L13N_T2L_N1_GC_QBC_73	VREF_73	U25	
K27	IO_L13P_T2L_N0_GC_QBC_73			
L27	IO_L14N_T2L_N3_GC_73			
M26	IO_L14P_T2L_N2_GC_73			
G26	IO_L15N_T2L_N5_AD11N_73			
G25	IO_L15P_T2L_N4_AD11P_73			
F27	IO_L16N_T2U_N7_QBC_AD3N_73			
G27	IO_L16P_T2U_N6_QBC_AD3P_73			
J26	IO_L17N_T2U_N9_AD10N_73			
K26	IO_L17P_T2U_N8_AD10P_73			
H26	IO_L18N_T2U_N11_AD2N_73			
J25	IO_L18P_T2U_N10_AD2P_73			
E25	IO_L19N_T3L_N1_DBC_AD9N_73			
F25	IO_L19P_T3L_N0_DBC_AD9P_73			
R30	IO_L1N_T0L_N1_DBC_73			
T30	IO_L1P_T0L_N0_DBC_73			
E27	IO_L20N_T3L_N3_AD1N_73			
E26	IO_L20P_T3L_N2_AD1P_73			
B26	IO_L21N_T3L_N5_AD8N_73			
C26	IO_L21P_T3L_N4_AD8P_73			
A27	IO_L22N_T3U_N7_DBC_AD0N_73			
B27	IO_L22P_T3U_N6_DBC_AD0P_73			
A25	IO_L23N_T3U_N9_73			
B25	IO_L23P_T3U_N8_73			
C27	IO_L24N_T3U_N11_73			
D26	IO_L24P_T3U_N10_73			
T29	IO_L2N_T0L_N3_73			
T28	IO_L2P_T0L_N2_73			
T27	IO_L3N_T0L_N5_AD15N_73			
U26	IO_L3P_T0L_N4_AD15P_73			
P28	IO_L4N_T0U_N7_DBC_AD7N_73			
R28	IO_L4P_T0U_N6_DBC_AD7P_73			
R27	IO_L5N_T0U_N9_AD14N_73			
R26	IO_L5P_T0U_N8_AD14P_73			
P30	IO_L6N_T0U_N11_AD6N_73			
P29	IO_L6P_T0U_N10_AD6P_73			
N26	IO_L7N_T1L_N1_QBC_AD13N_73			
P26	IO_L7P_T1L_N0_QBC_AD13P_73			
M30	IO_L8N_T1L_N3_AD5N_73			
M29	IO_L8P_T1L_N2_AD5P_73			
N29	IO_L9N_T1L_N5_AD12N_73			
N28	IO_L9P_T1L_N4_AD12P_73			
T31	IO_T0U_N12_VRP_73			
J28	IO_T1U_N12_73			
H27	IO_T2U_N12_73			
D25	IO_T3U_N12_73			

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U202-55

AR16	IO_L11N_T1U_N9_GC_66	VCCO_66	AT16	V_1V8
AR17	IO_L11P_T1U_N8_GC_66	VREF_66	AR15	
AU16	IO_L12N_T1U_N11_GC_66			
AT17	IO_L12P_T1U_N10_GC_66			
AT15	IO_T0U_N12_VRP_66			
AU15	IO_T3U_N12_66			

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U202-19

A30	IO_L10N_T1U_N7_QBC_AD4N_71	VCCO_71	B28	V_1V8
B30	IO_L10P_T1U_N6_QBC_AD4P_71	VCCO_71	E29	
A29	IO_L11N_T1U_N9_GC_71	VCCO_71	L31	
A28	IO_L11P_T1U_N8_GC_71	VREF_71	L30	
C30	IO_L12N_T1U_N11_GC_71			
C29	IO_L12P_T1U_N10_GC_71			
J31	IO_L1N_T0L_N1_DBC_71			
K31	IO_L1P_T0L_N0_DBC_71			
H30	IO_L2N_T0L_N3_71			
J29	IO_L2P_T0L_N2_71			
J30	IO_L3N_T0L_N5_AD15N_71			
K30	IO_L3P_T0L_N4_AD15P_71			
G29	IO_L4N_T0U_N7_DBC_AD7N_71			
H29	IO_L4P_T0U_N6_DBC_AD7P_71			
F30	IO_L5N_T0U_N9_AD14N_71			
G30	IO_L5P_T0U_N8_AD14P_71			
F29	IO_L6N_T0U_N11_AD6N_71			
F28	IO_L6P_T0U_N10_AD6P_71			
D29	IO_L7N_T1L_N1_QBC_AD13N_71			
D28	IO_L7P_T1L_N0_QBC_AD13P_71			
D30	IO_L8N_T1L_N3_AD5N_71			
E30	IO_L8P_T1L_N2_AD5P_71			
B29	IO_L9N_T1L_N5_AD12N_71			
C28	IO_L9P_T1L_N4_AD12P_71			
H28	IO_T0U_N12_VRP_71			
E28	IO_T1U_N12_71			

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F2 UNUSED BLOCKS

APOLLO CM W/ DUAL A2577, MK1

Title: 6.99: F2 UNUSED BLOCKS

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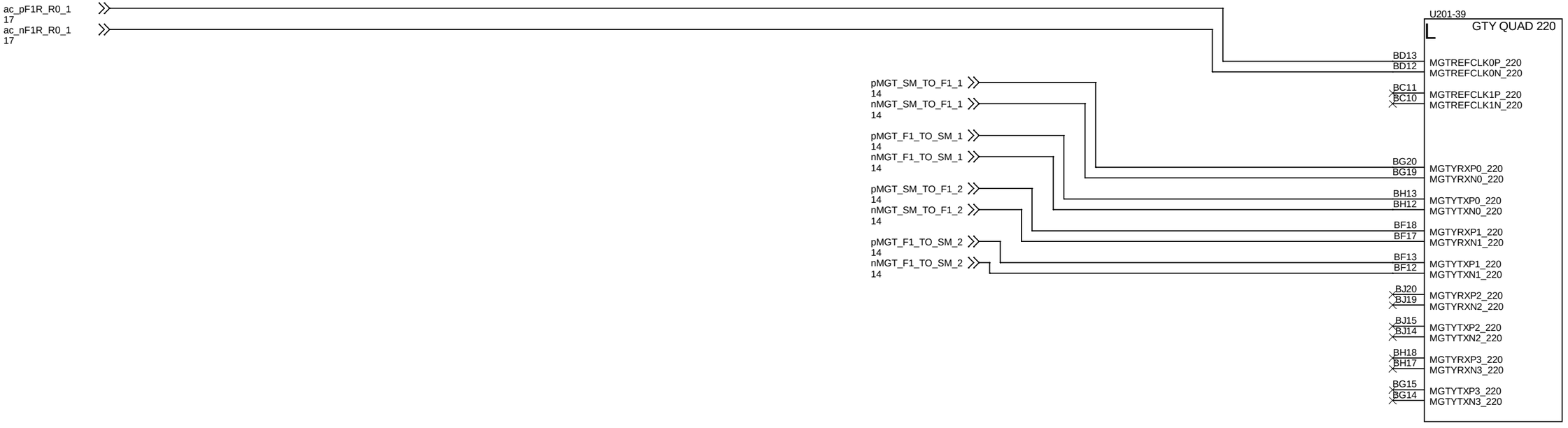
7.01: FPGA#1 SM C2C ON QUAD L

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



APOLLO CM W/ DUAL A2577, MK1		
Title: 7.01: FPGA#1 SM C2C ON QUAD L		
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7.02: FPGA#1 FF#1 X12 ON QUADS AC AD AE

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_2 18
ac_nF1L_R0_2 18
ac_pF1L_R1_2 20
ac_nF1L_R1_2 20

V_M3V3
R968 3.3K 0603
R969 3.3K 0603
R970 2.2K 0603
R971 2.2K 0603

U551-1 FIREFLY_XMIT_X12 FIREFLY XMIT X12

/F1_FF_RESET 37,58,59,60,61,62,63,64
I2C_SDA_F1_FF1_XMIT 37
I2C_SCL_F1_FF1_XMIT 37
/F1_FF1_XMIT_INT 37
/F1_FF1_XMIT_PRESENT 37
V_3V3
V_F1_FF1_XMIT 30

6 /RESET G1 G2
7 SDA
8 SCL
4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.8/3.3V >=25G 3.8V <=16G 3.3V
9 RSVD
2 GND

C2086 +-22 UF 0603 6.3V
C2087 0.1 UF 0402
C2088 +-22 UF 0603 6.3V
C2089 0.1 UF 0402
L103 1.0 UH 1008
C2090 +-22 UF 0603 6.3V
C2091 0.1 UF 0402
C2092 +-22 UF 0603 6.3V
C2093 0.1 UF 0402
L104 1.0 UH 1008

<Implementation>

U551-2 FIREFLY_XMIT_X12 FIREFLY XMIT X12

GND_B19 A19, GND_A19
GND_B16 B16, A16
GND_B13 B13, A13
GND_B10 B10, A10
GND_B7 B7, A7
GND_B4 B4, A4
GND_B1 B1, A1

0P 18 pF1_FF1_XMIT0
0N 17 nF1_FF1_XMIT0
1P 18 pF1_FF1_XMIT1
1N 17 nF1_FF1_XMIT1
2P 15 pF1_FF1_XMIT2
2N 14 nF1_FF1_XMIT2
3P 15 pF1_FF1_XMIT3
3N 14 nF1_FF1_XMIT3
4P 12 pF1_FF1_XMIT4
4N 11 nF1_FF1_XMIT4
5P 12 pF1_FF1_XMIT5
5N 11 nF1_FF1_XMIT5
6P 9 pF1_FF1_XMIT6
6N 8 nF1_FF1_XMIT6
7P 9 pF1_FF1_XMIT7
7N 8 nF1_FF1_XMIT7
8P 6 pF1_FF1_XMIT8
8N 5 nF1_FF1_XMIT8
9P 6 pF1_FF1_XMIT9
9N 5 nF1_FF1_XMIT9
10P 3 pF1_FF1_XMIT10
10N 2 nF1_FF1_XMIT10
11P 3 pF1_FF1_XMIT11
11N 2 nF1_FF1_XMIT11

GND 1 GND 2 /A83
GND 3 GND 4 /A84
GND 1 GND 2 /A85
GND 3 GND 4 /A86
GND 1 GND 2 /A87
GND 3 GND 4 /A88

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U201-24 AC GTY QUAD 121

BB39 BB40 MGTREFCLK0P_121 MGTREFCLK0N_121
BA41 BA42 MGTREFCLK1P_121 MGTREFCLK1N_121

pF1_FF1_RECV0 BK34 MGTYRXP0_121
nF1_FF1_RECV0 BK35 MGTYRXN0_121
pF1_FF1_XMIT0 BL37 MGTYTXP0_121
nF1_FF1_XMIT0 BL38 MGTYTXN0_121
pF1_FF1_RECV1 BL32 MGTYRXP1_121
nF1_FF1_RECV1 BL33 MGTYRXN1_121
pF1_FF1_XMIT1 BK39 MGTYTXP1_121
nF1_FF1_XMIT1 BK40 MGTYTXN1_121
pF1_FF1_RECV2 BL46 MGTYRXP2_121
nF1_FF1_RECV2 BL47 MGTYRXN2_121
pF1_FF1_XMIT2 BL41 MGTYTXP2_121
nF1_FF1_XMIT2 BL42 MGTYTXN2_121
pF1_FF1_RECV3 BJ46 MGTYRXP3_121
nF1_FF1_RECV3 BJ47 MGTYRXN3_121
pF1_FF1_XMIT3 BK43 MGTYTXP3_121
nF1_FF1_XMIT3 BK44 MGTYTXN3_121

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U201-25 AD GTY QUAD 122

AY39 AY40 MGTREFCLK0P_122 MGTREFCLK0N_122
AW41 AW42 MGTREFCLK1P_122 MGTREFCLK1N_122

pF1_FF1_RECV4 BH48 MGTYRXP0_122
nF1_FF1_RECV4 BH49 MGTYRXN0_122
pF1_FF1_XMIT4 BG41 MGTYTXP0_122
nF1_FF1_XMIT4 BG42 MGTYTXN0_122
pF1_FF1_RECV5 BG50 MGTYRXP1_122
nF1_FF1_RECV5 BG51 MGTYRXN1_122
pF1_FF1_XMIT5 BJ41 MGTYTXP1_122
nF1_FF1_XMIT5 BJ42 MGTYTXN1_122
pF1_FF1_RECV6 BG46 MGTYRXP2_122
nF1_FF1_RECV6 BG47 MGTYRXN2_122
pF1_FF1_XMIT6 BH43 MGTYTXP2_122
nF1_FF1_XMIT6 BH44 MGTYTXN2_122
pF1_FF1_RECV7 BF48 MGTYRXP3_122
nF1_FF1_RECV7 BF49 MGTYRXN3_122
pF1_FF1_XMIT7 BF43 MGTYTXP3_122
nF1_FF1_XMIT7 BF44 MGTYTXN3_122

FPGA_VU13P_A2577

V_M3V3
R972 3.3K 0603
R973 3.3K 0603
R974 2.2K 0603
R975 2.2K 0603

U559-1 FIREFLY_RECV_X12 FIREFLY RECV X12

/F1_FF_RESET 37,58,59,60,61,62,63,64
I2C_SDA_F1_FF1_RECV 37
I2C_SCL_F1_FF1_RECV 37
/F1_FF1_RECV_INT 37
/F1_FF1_RECV_PRESENT 37
V_3V3

6 /RESET G1 G2
7 SDA
8 SCL
4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.3V
9 RSVD
2 GND

C2096 +-22 UF 0603 6.3V
C2097 0.1 UF 0402
C2094 +-22 UF 0603 6.3V
C2095 0.1 UF 0402
L105 1.0 UH 1008
C2098 +-22 UF 0603 6.3V
C2099 0.1 UF 0402
L106 1.0 UH 1008

<Implementation>

U559-2 FIREFLY_RECV_X12 FIREFLY RECV X12

GND_B19 A19, GND_A19
GND_B16 B16, A16
GND_B13 B13, A13
GND_B10 B10, A10
GND_B7 B7, A7
GND_B4 B4, A4
GND_B1 B1, A1

0P 18 pF1_FF1_RECV0
0N 17 nF1_FF1_RECV0
1P 18 pF1_FF1_RECV1
1N 17 nF1_FF1_RECV1
2P 15 pF1_FF1_RECV2
2N 14 nF1_FF1_RECV2
3P 15 pF1_FF1_RECV3
3N 14 nF1_FF1_RECV3
4P 12 pF1_FF1_RECV4
4N 11 nF1_FF1_RECV4
5P 12 pF1_FF1_RECV5
5N 11 nF1_FF1_RECV5
6P 9 pF1_FF1_RECV6
6N 8 nF1_FF1_RECV6
7P 9 pF1_FF1_RECV7
7N 8 nF1_FF1_RECV7
8P 6 pF1_FF1_RECV8
8N 5 nF1_FF1_RECV8
9P 6 pF1_FF1_RECV9
9N 5 nF1_FF1_RECV9
10P 3 pF1_FF1_RECV10
10N 2 nF1_FF1_RECV10
11P 3 pF1_FF1_RECV11
11N 2 nF1_FF1_RECV11

GND 1 GND 2 /A90
GND 3 GND 4 /A91
GND 1 GND 2 /A92
GND 3 GND 4 /A93
GND 1 GND 2 /A94

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

U201-26 AE GTY QUAD 123

AV39 AV40 MGTREFCLK0P_123 MGTREFCLK0N_123
AU41 AU42 MGTREFCLK1P_123 MGTREFCLK1N_123

pF1_FF1_RECV8 BE50 MGTYRXP0_123
nF1_FF1_RECV8 BE51 MGTYRXN0_123
pF1_FF1_XMIT8 BE45 MGTYTXP0_123
nF1_FF1_XMIT8 BE46 MGTYTXN0_123
pF1_FF1_RECV9 BD48 MGTYRXP1_123
nF1_FF1_RECV9 BD49 MGTYRXN1_123
pF1_FF1_XMIT9 BD43 MGTYTXP1_123
nF1_FF1_XMIT9 BD44 MGTYTXN1_123
pF1_FF1_RECV10 BC50 MGTYRXP2_123
nF1_FF1_RECV10 BC51 MGTYRXN2_123
pF1_FF1_XMIT10 BC45 MGTYTXP2_123
nF1_FF1_XMIT10 BC46 MGTYTXN2_123
pF1_FF1_RECV11 BB48 MGTYRXP3_123
nF1_FF1_RECV11 BB49 MGTYRXN3_123
pF1_FF1_XMIT11 BB43 MGTYTXP3_123
nF1_FF1_XMIT11 BB44 MGTYTXN3_123

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ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

APOLLO CM W/ DUAL A2577, MK1

Title: 7.02: FPGA#1 FF#1 X12 ON QUADS AC AD AE

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7.03: FPGA#1 FF#2 X12 ON QUADS Q R S

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_4 18
ac_nF1L_R0_4 18
ac_pF1L_R1_4 20
ac_nF1L_R1_4 20

V_M3V3 — R976 3.3K 0603 — R977 3.3K 0603 — R978 2.2K 0603 — R979 2.2K 0603

U552-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

/F1_FF_RESET 37,58,59,60,61,62,63,64 → /RESET (G1, G2 → GND)
I2C_SDA_F1_FF2_XMIT 37 → SDA
I2C_SCL_F1_FF2_XMIT 37 → SCL
GND → /SELECT
/F1_FF2_XMIT_INT 37 → /INT
/F1_FF2_XMIT_PRESENT 37 → /PRESENT
V_3V3 → 3.3V
V_F1_FF2_XMIT 30 → 3.8/3.3V (>=25G 3.8V, <=16G 3.3V)
RSVD
GND

V_3V3 filter: C2100 22 UF 0603 6.3V; C2101 0.1 UF 0402; L107 1.0 UH 1008; C2102 22 UF 0603 6.3V; C2103 0.1 UF 0402
V_F1_FF2_XMIT filter: C2104 22 UF 0603 6.3V; C2105 0.1 UF 0402; L108 1.0 UH 1008; C2106 22 UF 0603 6.3V; C2107 0.1 UF 0402

<Implementation>

U552-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

B19 GND_B19 / A19 GND_A19	0P / 0N	B18 / B17	pF1_FF2_XMIT0 / nF1_FF2_XMIT0
	1P / 1N	A18 / A17	pF1_FF2_XMIT1 / nF1_FF2_XMIT1
B16 GND_B16 / A16 GND_A16	2P / 2N	B15 / B14	pF1_FF2_XMIT2 / nF1_FF2_XMIT2
	3P / 3N	A15 / A14	pF1_FF2_XMIT3 / nF1_FF2_XMIT3
B13 GND_B13 / A13 GND_A13	4P / 4N	B12 / B11	pF1_FF2_XMIT4 / nF1_FF2_XMIT4
	5P / 5N	A12 / A11	pF1_FF2_XMIT5 / nF1_FF2_XMIT5
B10 GND_B10 / A10 GND_A10	6P / 6N	B9 / B8	pF1_FF2_XMIT6 / nF1_FF2_XMIT6
	7P / 7N	A9 / A8	pF1_FF2_XMIT7 / nF1_FF2_XMIT7
B7 GND_B7 / A7 GND_A7	8P / 8N	B6 / B5	pF1_FF2_XMIT8 / nF1_FF2_XMIT8
	9P / 9N	A6 / A5	pF1_FF2_XMIT9 / nF1_FF2_XMIT9
B4 GND_B4 / A4 GND_A4	10P / 10N	B3 / B2	pF1_FF2_XMIT10 / nF1_FF2_XMIT10
B1 GND_B1 / A1 GND_A1	11P / 11N	A3 / A2	pF1_FF2_XMIT11 / nF1_FF2_XMIT11

GND — 3 4 1 G1 2 G2 — A95 A96 A97 A98 A99 A100

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U201-28 Q — GTY QUAD 125

	AP39 / AP40	MGTREFCLK0P_125 / MGTREFCLK0N_125
	AN41 / AN42	MGTREFCLK1P_125 / MGTREFCLK1N_125
pF1_FF2_RECV0 / nF1_FF2_RECV0	AU50 / AU51	MGTYRXP0_125 / MGTYRXN0_125
pF1_FF2_XMIT0 / nF1_FF2_XMIT0	AU45 / AU46	MGTYTXP0_125 / MGTYTXN0_125
pF1_FF2_RECV1 / nF1_FF2_RECV1	AT48 / AT49	MGTYRXP1_125 / MGTYRXN1_125
pF1_FF2_XMIT1 / nF1_FF2_XMIT1	AT43 / AT44	MGTYTXP1_125 / MGTYTXN1_125
pF1_FF2_RECV2 / nF1_FF2_RECV2	AR50 / AR51	MGTYRXP2_125 / MGTYRXN2_125
pF1_FF2_XMIT2 / nF1_FF2_XMIT2	AR45 / AR46	MGTYTXP2_125 / MGTYTXN2_125
pF1_FF2_RECV3 / nF1_FF2_RECV3	AP48 / AP49	MGTYRXP3_125 / MGTYRXN3_125
pF1_FF2_XMIT3 / nF1_FF2_XMIT3	AP43 / AP44	MGTYTXP3_125 / MGTYTXN3_125

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U201-29 R — GTY QUAD 126

	AM39 / AM40	MGTREFCLK0P_126 / MGTREFCLK0N_126
	AL41 / AL42	MGTREFCLK1P_126 / MGTREFCLK1N_126
pF1_FF2_RECV4 / nF1_FF2_RECV4	AN50 / AN51	MGTYRXP0_126 / MGTYRXN0_126
pF1_FF2_XMIT4 / nF1_FF2_XMIT4	AN45 / AN46	MGTYTXP0_126 / MGTYTXN0_126
pF1_FF2_RECV5 / nF1_FF2_RECV5	AM48 / AM49	MGTYRXP1_126 / MGTYRXN1_126
pF1_FF2_XMIT5 / nF1_FF2_XMIT5	AM43 / AM44	MGTYTXP1_126 / MGTYTXN1_126
pF1_FF2_RECV6 / nF1_FF2_RECV6	AL50 / AL51	MGTYRXP2_126 / MGTYRXN2_126
pF1_FF2_XMIT6 / nF1_FF2_XMIT6	AL45 / AL46	MGTYTXP2_126 / MGTYTXN2_126
pF1_FF2_RECV7 / nF1_FF2_RECV7	AK48 / AK49	MGTYRXP3_126 / MGTYRXN3_126
pF1_FF2_XMIT7 / nF1_FF2_XMIT7	AK43 / AK44	MGTYTXP3_126 / MGTYTXN3_126

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V_M3V3 — R980 3.3K 0603 — R981 3.3K 0603 — R982 2.2K 0603 — R983 2.2K 0603

U560-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

/F1_FF_RESET 37,58,59,60,61,62,63,64 → /RESET (G1, G2 → GND)
I2C_SDA_F1_FF2_RECV 37 → SDA
I2C_SCL_F1_FF2_RECV 37 → SCL
GND → /SELECT
/F1_FF2_RECV_INT 37 → /INT
/F1_FF2_RECV_PRESENT 37 → /PRESENT
V_3V3 → 3.3V
3.3V
RSVD
GND

V_3V3 filter: C2108 22 UF 0603 6.3V; C2109 0.1 UF 0402; L109 1.0 UH 1008; C2110 22 UF 0603 6.3V; C2111 0.1 UF 0402
3.3V filter: L110 1.0 UH 1008; C2112 22 UF 0603 6.3V; C2113 0.1 UF 0402

<Implementation>

U560-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

B19 GND_B19 / A19 GND_A19	0P / 0N	A18 / A17	pF1_FF2_RECV0 / nF1_FF2_RECV0
	1P / 1N	B18 / B17	pF1_FF2_RECV1 / nF1_FF2_RECV1
B16 GND_B16 / A16 GND_A16	2P / 2N	A15 / A14	pF1_FF2_RECV2 / nF1_FF2_RECV2
	3P / 3N	B15 / B14	pF1_FF2_RECV3 / nF1_FF2_RECV3
B13 GND_B13 / A13 GND_A13	4P / 4N	A12 / A11	pF1_FF2_RECV4 / nF1_FF2_RECV4
	5P / 5N	B12 / B11	pF1_FF2_RECV5 / nF1_FF2_RECV5
B10 GND_B10 / A10 GND_A10	6P / 6N	A9 / A8	pF1_FF2_RECV6 / nF1_FF2_RECV6
	7P / 7N	B9 / B8	pF1_FF2_RECV7 / nF1_FF2_RECV7
B7 GND_B7 / A7 GND_A7	8P / 8N	A6 / A5	pF1_FF2_RECV8 / nF1_FF2_RECV8
	9P / 9N	B6 / B5	pF1_FF2_RECV9 / nF1_FF2_RECV9
B4 GND_B4 / A4 GND_A4	10P / 10N	A3 / A2	pF1_FF2_RECV10 / nF1_FF2_RECV10
B1 GND_B1 / A1 GND_A1	11P / 11N	B3 / B2	pF1_FF2_RECV11 / nF1_FF2_RECV11

GND — 3 4 1 G1 2 G2 — A101 A102 A103 A104 A105 A106

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U201-30 S — GTY QUAD 127

	AJ41 / AJ42	MGTREFCLK0P_127 / MGTREFCLK0N_127
	AG41 / AG42	MGTREFCLK1P_127 / MGTREFCLK1N_127
pF1_FF2_RECV8 / nF1_FF2_RECV8	AJ50 / AJ51	MGTYRXP0_127 / MGTYRXN0_127
pF1_FF2_XMIT8 / nF1_FF2_XMIT8	AJ45 / AJ46	MGTYTXP0_127 / MGTYTXN0_127
pF1_FF2_RECV9 / nF1_FF2_RECV9	AH48 / AH49	MGTYRXP1_127 / MGTYRXN1_127
pF1_FF2_XMIT9 / nF1_FF2_XMIT9	AH43 / AH44	MGTYTXP1_127 / MGTYTXN1_127
pF1_FF2_RECV10 / nF1_FF2_RECV10	AG50 / AG51	MGTYRXP2_127 / MGTYRXN2_127
pF1_FF2_XMIT10 / nF1_FF2_XMIT10	AG45 / AG46	MGTYTXP2_127 / MGTYTXN2_127
pF1_FF2_RECV11 / nF1_FF2_RECV11	AF48 / AF49	MGTYRXP3_127 / MGTYRXN3_127
pF1_FF2_XMIT11 / nF1_FF2_XMIT11	AF43 / AF44	MGTYTXP3_127 / MGTYTXN3_127

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ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1	
Title	7.03: FPGA#1 FF#2 X12 ON QUADS Q R S
Size	Document Number 6089-119 Rev A
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7.04: FPGA#1 FF#3 X12 ON QUADS X Y Z

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_7 18
ac_nF1L_R0_7 18
ac_pF1L_R1_7 20
ac_nF1L_R1_7 20

V_M3V3

R984 3.3K 0603
R985 3.3K 0603
R986 2.2K 0603
R987 2.2K 0603

/F1_FF_RESET 37,58,59,60,61,62,63,64
I2C_SDA_F1_FF3_XMIT 37
I2C_SCL_F1_FF3_XMIT 37
/F1_FF3_XMIT_INT 37
/F1_FF3_XMIT_PRESENT 37
V_3V3
V_F1_FF3_XMIT 30

C2114 +22 UF 0603 6.3V
C2115 0.1 UF 0402
C2116 +22 UF 0603 6.3V
C2117 0.1 UF 0402
L111 1.0 UH 1008
C2118 +22 UF 0603 6.3V
C2119 0.1 UF 0402
C2120 0.1 UF 0402
C2121 +22 UF 0603 6.3V
L112 1.0 UH 1008

U553-1
FIREFLY_XMIT_X12
FIREFLY XMIT X12

/RESET
SDA
SCL
/SELECT
/INT
/PRESENT
3.3V
3.8/3.3V >=25G 3.8V <=16G 3.3V
RSVD
GND
G1
G2
<Implementation>

U553-2
FIREFLY_XMIT_X12
FIREFLY XMIT X12

B19	GND_B19	0P	B18	pF1_FF3_XMIT0
A19	GND_A19	0N	B17	nF1_FF3_XMIT0
		1P	A18	pF1_FF3_XMIT1
		1N	A17	nF1_FF3_XMIT1
B16	GND_B16	2P	B15	pF1_FF3_XMIT2
A16	GND_A16	2N	B14	nF1_FF3_XMIT2
		3P	A15	pF1_FF3_XMIT3
		3N	A14	nF1_FF3_XMIT3
B13	GND_B13	4P	B12	pF1_FF3_XMIT4
A13	GND_A13	4N	B11	nF1_FF3_XMIT4
		5P	A12	pF1_FF3_XMIT5
		5N	A11	nF1_FF3_XMIT5
B10	GND_B10	6P	B9	pF1_FF3_XMIT6
A10	GND_A10	6N	B8	nF1_FF3_XMIT6
		7P	A9	pF1_FF3_XMIT7
		7N	A8	nF1_FF3_XMIT7
B7	GND_B7	8P	B6	pF1_FF3_XMIT8
A7	GND_A7	8N	B5	nF1_FF3_XMIT8
		9P	A6	pF1_FF3_XMIT9
		9N	A5	nF1_FF3_XMIT9
B4	GND_B4	10P	B3	pF1_FF3_XMIT10
A4	GND_A4	10N	B2	nF1_FF3_XMIT10
		11P	A3	pF1_FF3_XMIT11
		11N	A2	nF1_FF3_XMIT11
B1	GND_B1			
A1	GND_A1			

GND
GND_A107
GND_A108
GND_A109
GND_A110
GND_A111
GND_A112

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U201-35
X
GTY QUAD 132

	R41	MGTREFCLK0P_132
	R42	MGTREFCLK0N_132
	P39	MGTREFCLK1P_132
	P40	MGTREFCLK1N_132
pF1_FF3_RECV0	J50	MGTYRXP0_132
nF1_FF3_RECV0	J51	MGTYRXN0_132
pF1_FF3_XMIT0	J45	MGTYTXP0_132
nF1_FF3_XMIT0	J46	MGTYTXN0_132
pF1_FF3_RECV1	H48	MGTYRXP1_132
nF1_FF3_RECV1	H49	MGTYRXN1_132
pF1_FF3_XMIT1	H43	MGTYTXP1_132
nF1_FF3_XMIT1	H44	MGTYTXN1_132
pF1_FF3_RECV2	G50	MGTYRXP2_132
nF1_FF3_RECV2	G51	MGTYRXN2_132
pF1_FF3_XMIT2	G45	MGTYTXP2_132
nF1_FF3_XMIT2	G46	MGTYTXN2_132
pF1_FF3_RECV3	F48	MGTYRXP3_132
nF1_FF3_RECV3	F49	MGTYRXN3_132
pF1_FF3_XMIT3	F43	MGTYTXP3_132
nF1_FF3_XMIT3	F44	MGTYTXN3_132

FPGA_VU13P_A2577

U201-36
Y
GTY QUAD 133

	N41	MGTREFCLK0P_133
	N42	MGTREFCLK0N_133
	M39	MGTREFCLK1P_133
	M40	MGTREFCLK1N_133
pF1_FF3_RECV4	E50	MGTYRXP0_133
nF1_FF3_RECV4	E51	MGTYRXN0_133
pF1_FF3_XMIT4	D43	MGTYTXP0_133
nF1_FF3_XMIT4	D44	MGTYTXN0_133
pF1_FF3_RECV5	D48	MGTYRXP1_133
nF1_FF3_RECV5	D49	MGTYRXN1_133
pF1_FF3_XMIT5	B43	MGTYTXP1_133
nF1_FF3_XMIT5	B44	MGTYTXN1_133
pF1_FF3_RECV6	E46	MGTYRXP2_133
nF1_FF3_RECV6	E47	MGTYRXN2_133
pF1_FF3_XMIT6	C41	MGTYTXP2_133
nF1_FF3_XMIT6	C42	MGTYTXN2_133
pF1_FF3_RECV7	C46	MGTYRXP3_133
nF1_FF3_RECV7	C47	MGTYRXN3_133
pF1_FF3_XMIT7	E41	MGTYTXP3_133
nF1_FF3_XMIT7	E42	MGTYTXN3_133

FPGA_VU13P_A2577

V_M3V3

R988 3.3K 0603
R989 3.3K 0603
R990 2.2K 0603
R991 2.2K 0603

/F1_FF_RESET 37,58,59,60,61,62,63,64
I2C_SDA_F1_FF3_RECV 37
I2C_SCL_F1_FF3_RECV 37
/F1_FF3_RECV_INT 37
/F1_FF3_RECV_PRESENT 37
V_3V3

C2122 +22 UF 0603 6.3V
C2123 0.1 UF 0402
C2124 +22 UF 0603 6.3V
C2125 0.1 UF 0402
L113 1.0 UH 1008
C2126 +22 UF 0603 6.3V
C2127 0.1 UF 0402
L114 1.0 UH 1008

U561-1
FIREFLY_RECV_X12
FIREFLY RECV X12

/RESET
SDA
SCL
/SELECT
/INT
/PRESENT
3.3V
3.3V
RSVD
GND
G1
G2
<Implementation>

U561-2
FIREFLY_RECV_X12
FIREFLY RECV X12

B19	GND_B19	0P	A18	pF1_FF3_RECV0
A19	GND_A19	0N	A17	nF1_FF3_RECV0
		1P	B18	pF1_FF3_RECV1
		1N	B17	nF1_FF3_RECV1
B16	GND_B16	2P	A15	pF1_FF3_RECV2
A16	GND_A16	2N	A14	nF1_FF3_RECV2
		3P	B15	pF1_FF3_RECV3
		3N	B14	nF1_FF3_RECV3
B13	GND_B13	4P	A12	pF1_FF3_RECV4
A13	GND_A13	4N	A11	nF1_FF3_RECV4
		5P	B12	pF1_FF3_RECV5
		5N	B11	nF1_FF3_RECV5
B10	GND_B10	6P	A9	pF1_FF3_RECV6
A10	GND_A10	6N	A8	nF1_FF3_RECV6
		7P	B9	pF1_FF3_RECV7
		7N	B8	nF1_FF3_RECV7
B7	GND_B7	8P	A6	pF1_FF3_RECV8
A7	GND_A7	8N	A5	nF1_FF3_RECV8
		9P	B6	pF1_FF3_RECV9
		9N	B5	nF1_FF3_RECV9
B4	GND_B4	10P	A3	pF1_FF3_RECV10
A4	GND_A4	10N	A2	nF1_FF3_RECV10
		11P	B3	pF1_FF3_RECV11
		11N	B2	nF1_FF3_RECV11
B1	GND_B1			
A1	GND_A1			

GND
GND_A113
GND_A114
GND_A115
GND_A116
GND_A117
GND_A118

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U201-37
Z
GTY QUAD 134

	L41	MGTREFCLK0P_134
	L42	MGTREFCLK0N_134
	K39	MGTREFCLK1P_134
	K40	MGTREFCLK1N_134
pF1_FF3_RECV8	A46	MGTYRXP0_134
nF1_FF3_RECV8	A47	MGTYRXN0_134
pF1_FF3_XMIT8	A41	MGTYTXP0_134
nF1_FF3_XMIT8	A42	MGTYTXN0_134
pF1_FF3_RECV9	A32	MGTYRXP1_134
nF1_FF3_RECV9	A33	MGTYRXN1_134
pF1_FF3_XMIT9	B39	MGTYTXP1_134
nF1_FF3_XMIT9	B40	MGTYTXN1_134
pF1_FF3_RECV10	B34	MGTYRXP2_134
nF1_FF3_RECV10	B35	MGTYRXN2_134
pF1_FF3_XMIT10	A37	MGTYTXP2_134
nF1_FF3_XMIT10	A38	MGTYTXN2_134
pF1_FF3_RECV11	C32	MGTYRXP3_134
nF1_FF3_RECV11	C33	MGTYRXN3_134
pF1_FF3_XMIT11	C37	MGTYTXP3_134
nF1_FF3_XMIT11	C38	MGTYTXN3_134

FPGA_VU13P_A2577

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1			
Title: 7.04: FPGA#1 FF#3 X12 ON QUADS X Y Z			
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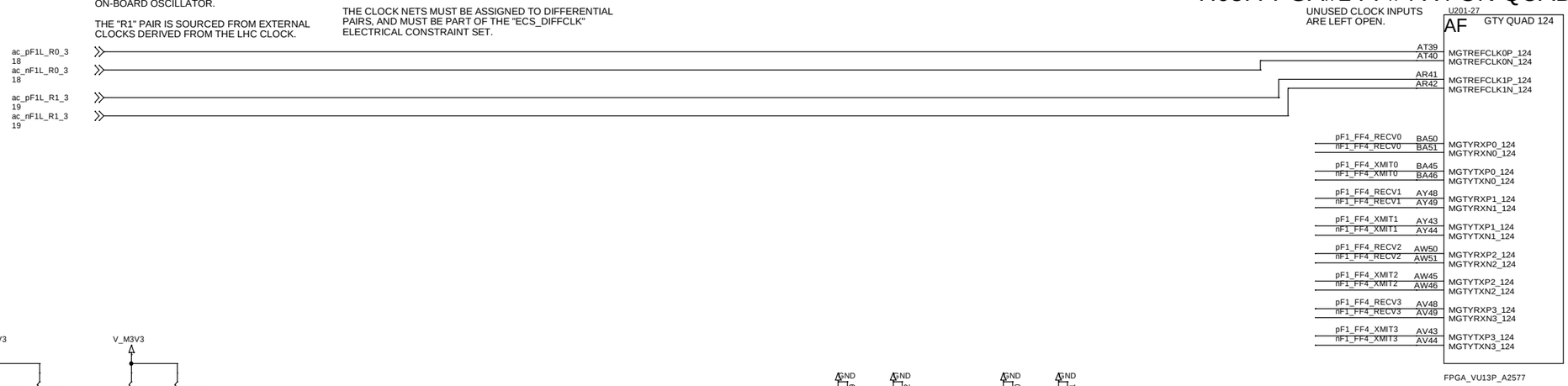
7.05: FPGA#1 FF#4 X4 ON QUAD AF

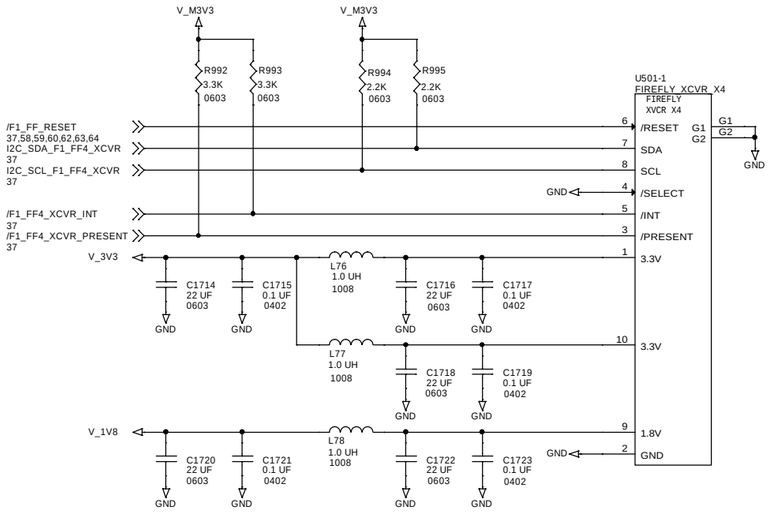
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

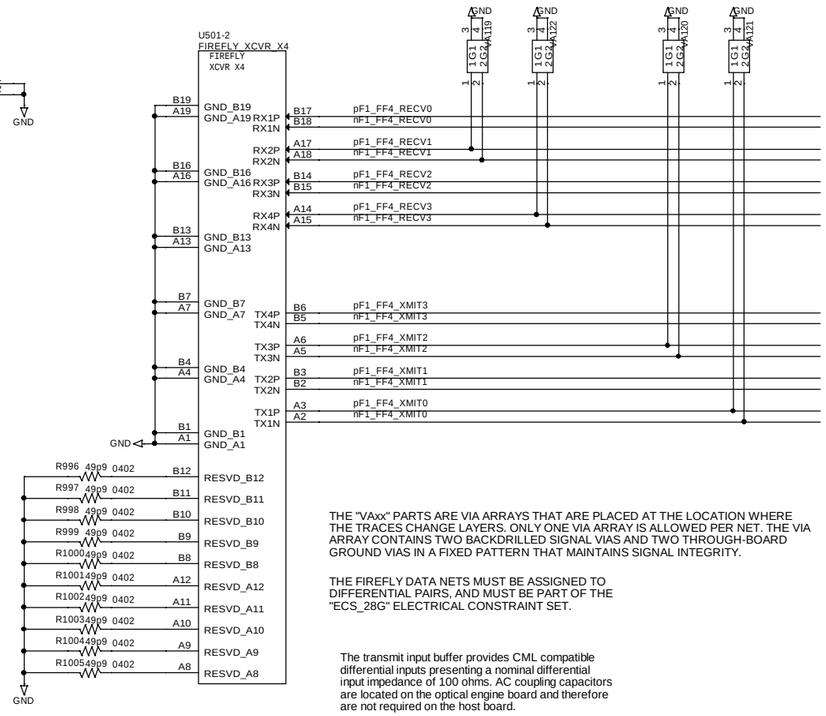
THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.







THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1		
Title: 7.05: FPGA#1 FF#4 X4 ON QUAD AF		
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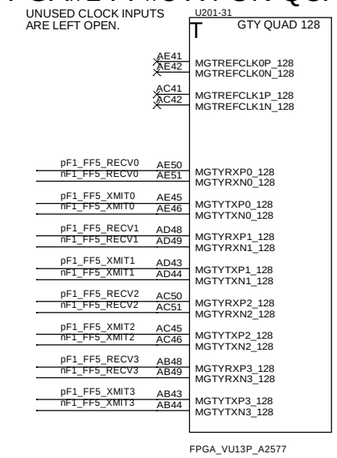
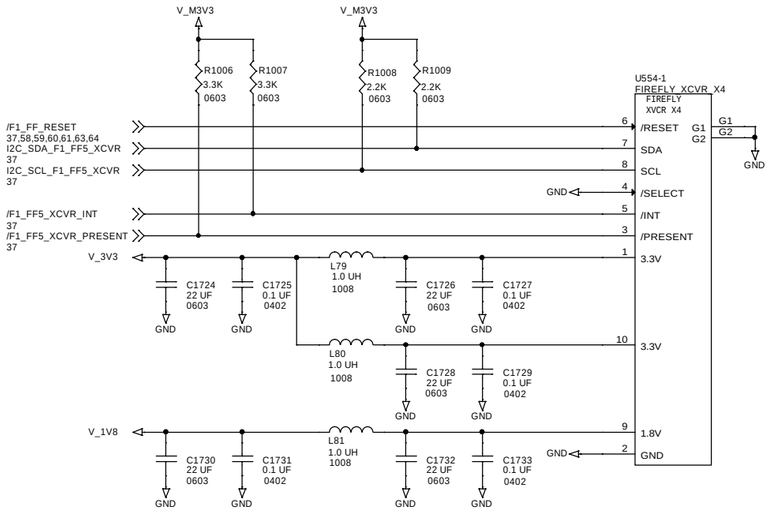
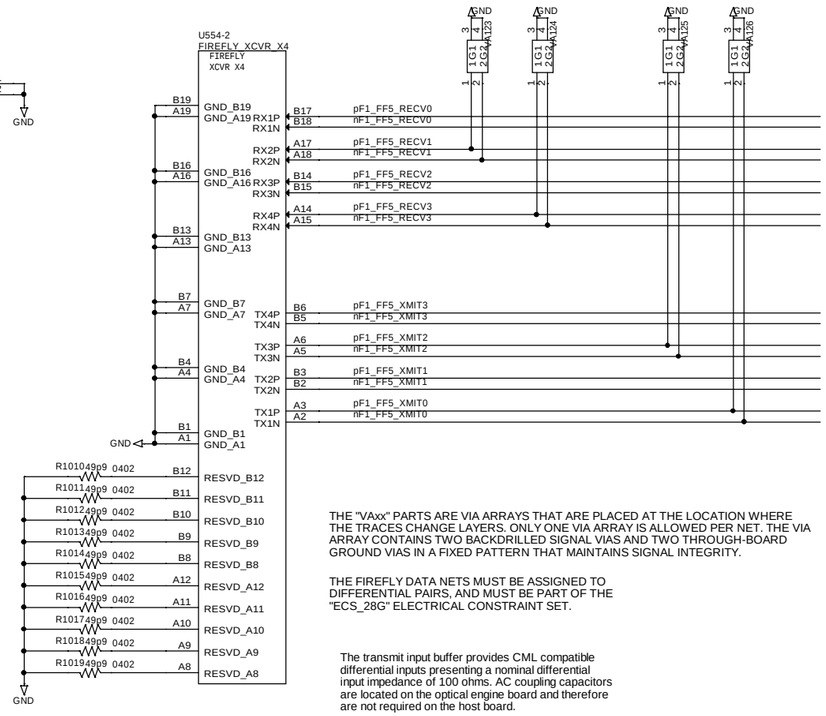
7.06: FPGA#1 FF#5 X4 ON QUAD T

UNUSED CLOCK INPUTS
ARE LEFT OPEN.



FPGA_VU13P_A2577





THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1			
Title: 7.06: FPGA#1 FF#5 X4 ON QUAD T			
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7.07: FPGA#1 FF#6 X4 ON QUAD U

ac_pF1L_R0_5 18
ac_nF1L_R0_5 18
ac_pF1L_R1_5 19
ac_nF1L_R1_5 19

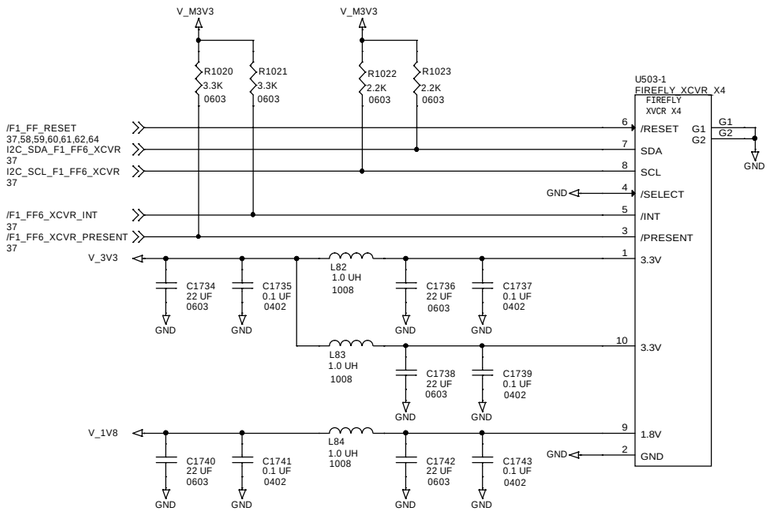
F1 QUAD U (T,U,V)

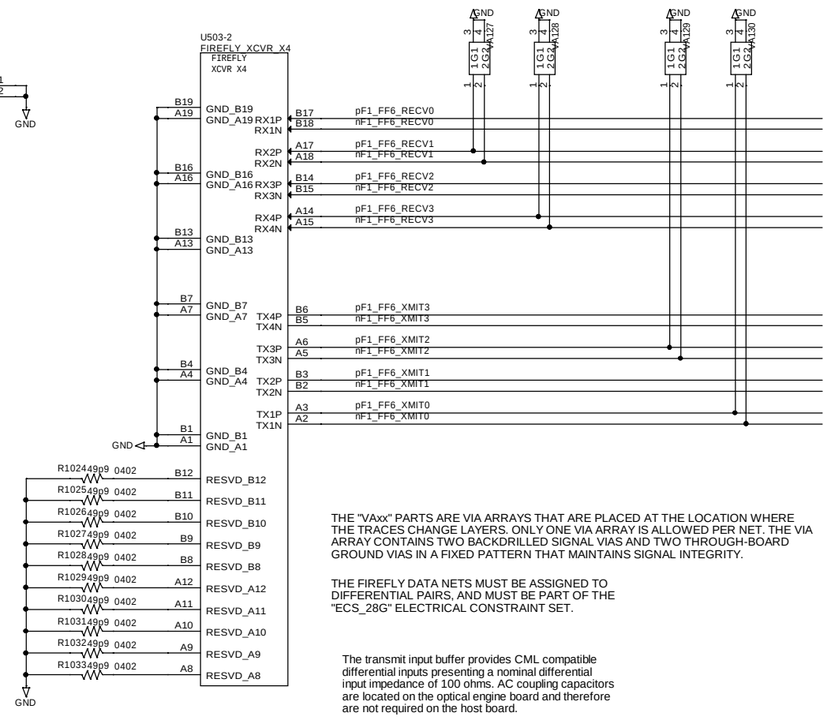
UNUSED CLOCK INPUTS ARE LEFT OPEN.

U201-32
U
GTY QUAD 129

	AA41	
	AA42	MGTREFCLK0P_129
		MGTREFCLK0N_129
	Y39	
	Y40	MGTREFCLK1P_129
		MGTREFCLK1N_129
pF1_FF6_RECV0	AA50	MGTYRXP0_129
nF1_FF6_RECV0	AA51	MGTYRXN0_129
pF1_FF6_XMIT0	AA45	MGTYTXP0_129
nF1_FF6_XMIT0	AA46	MGTYTXN0_129
pF1_FF6_RECV1	Y48	MGTYRXP1_129
nF1_FF6_RECV1	Y49	MGTYRXN1_129
pF1_FF6_XMIT1	Y43	MGTYTXP1_129
nF1_FF6_XMIT1	Y44	MGTYTXN1_129
pF1_FF6_RECV2	W50	MGTYRXP2_129
nF1_FF6_RECV2	W51	MGTYRXN2_129
pF1_FF6_XMIT2	W45	MGTYTXP2_129
nF1_FF6_XMIT2	W46	MGTYTXN2_129
pF1_FF6_RECV3	V48	MGTYRXP3_129
nF1_FF6_RECV3	V49	MGTYRXN3_129
pF1_FF6_XMIT3	V43	MGTYTXP3_129
nF1_FF6_XMIT3	V44	MGTYTXN3_129

FPGA_VU13P_A2577





THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1		
Title: 7.07: FPGA#1 FF#6 X4 ON QUAD U		
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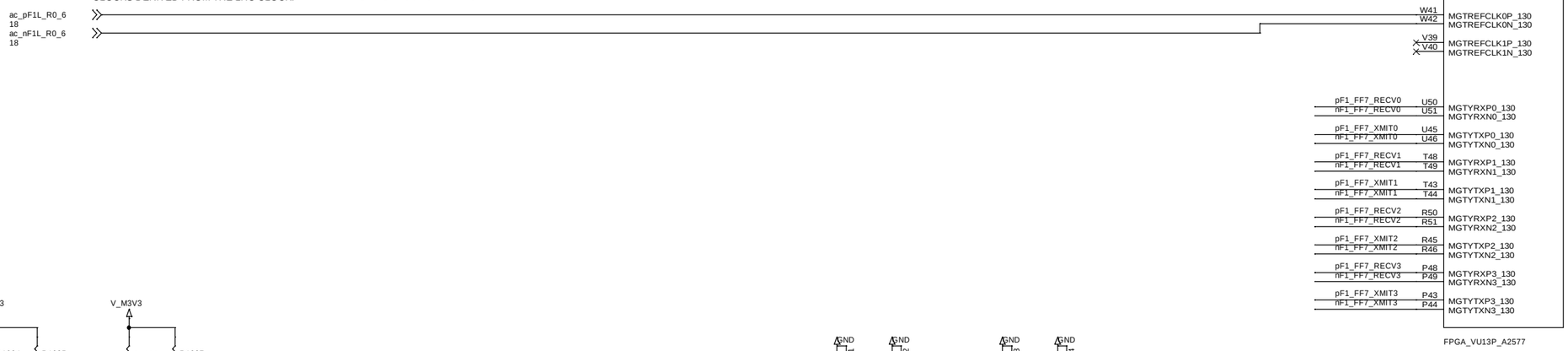
7.08: FPGA#1 FF#7 X4 ON QUAD V

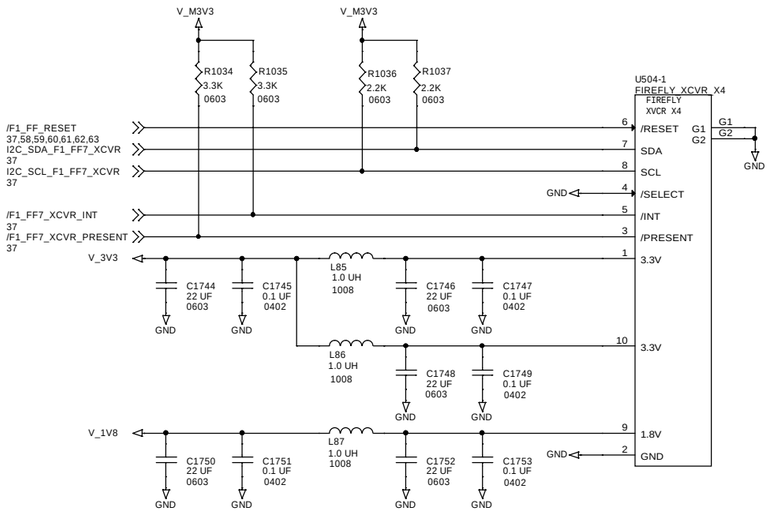
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

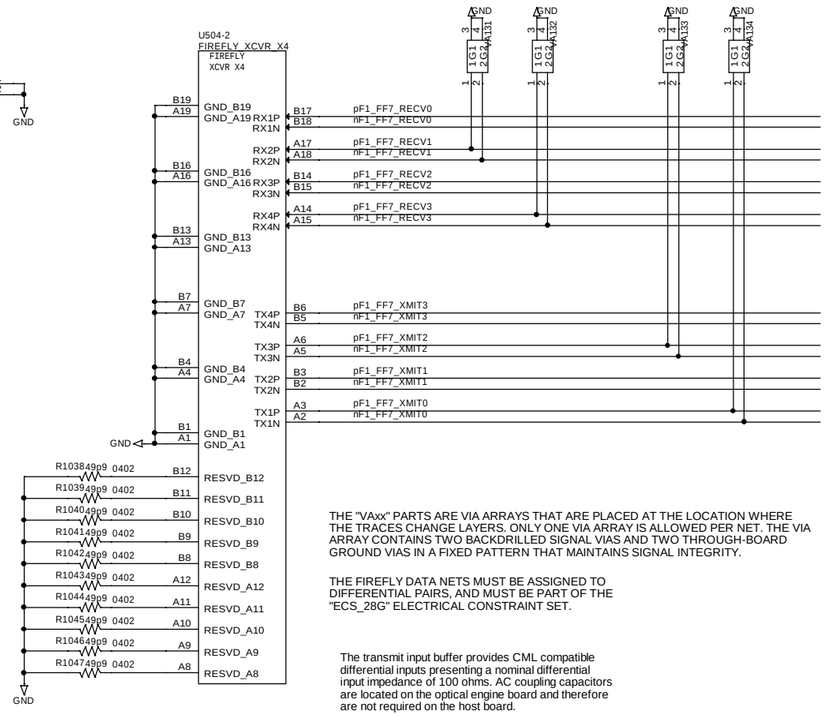
THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1		
Title: 7.08: FPGA#1 FF#7 X4 ON QUAD V		
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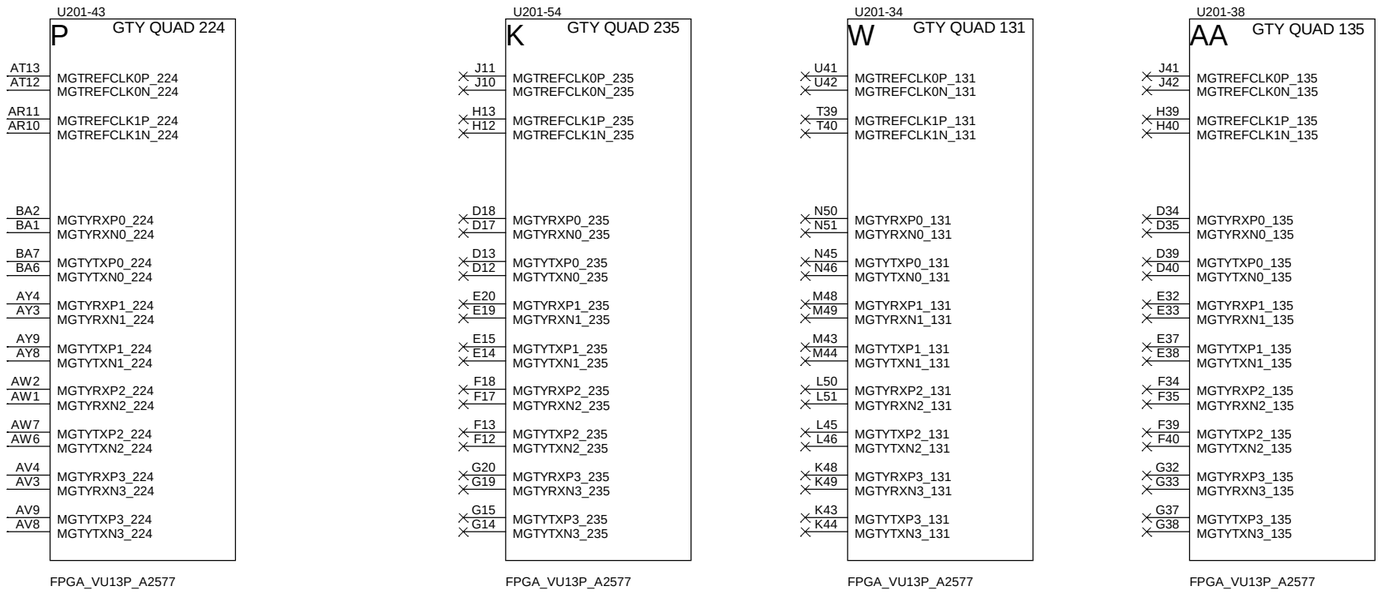
7.09: FPGA#1 UNUSED QUADS K, P, W, AA



APOLLO CM W/ DUAL A2577, MK1		
Title: 7.09: FPGA#1 UNUSED QUADS K, P, W, AA		
Size	Document Number: 6089-119	Rev: A
Date: Wednesday, February 17, 2021	Sheet 65 of 80	

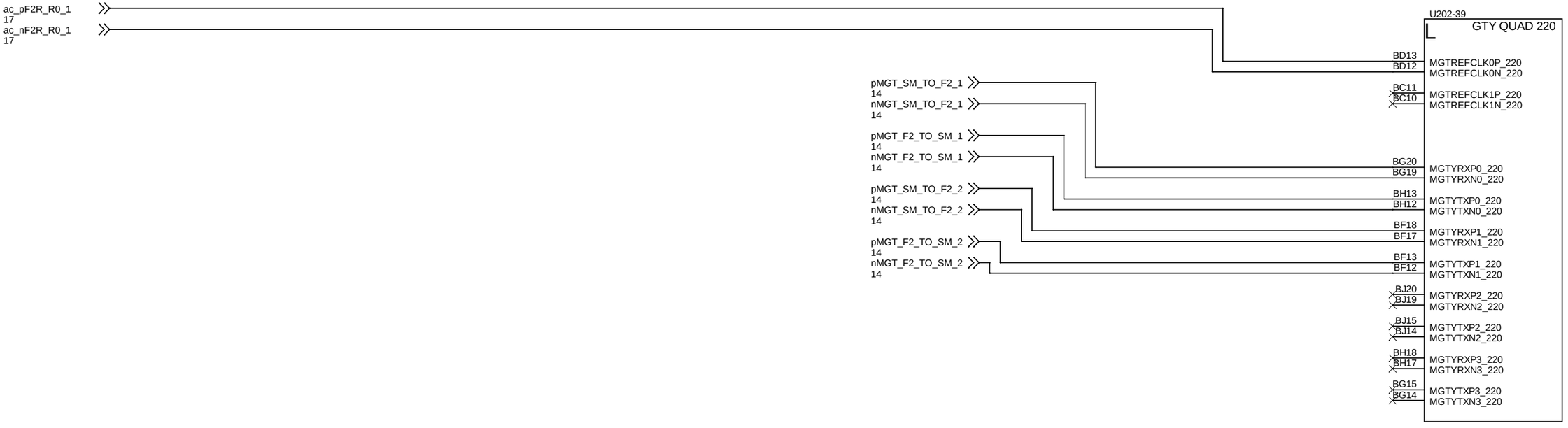
8.01: FPGA#2 SM C2C ON QUAD L

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



APOLLO CM W/ DUAL A2577, MK1

Title		
8.01: FPGA#2 SM C2C ON QUAD L		
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8.02: FPGA#2 FF#1 X12 ON QUADS AC AD AE

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF2L_R0_2 18
ac_nF2L_R0_2 18
ac_pF2L_R1_2 20
ac_nF2L_R1_2 20

V_M3V3
R1048 3.3K 0603
R1049 3.3K 0603
R1050 2.2K 0603
R1051 2.2K 0603

U555-1 FIREFLY_XMIT_X12 FIREFLY XMIT X12

/F2_FF_RESET 38,67,68,69,70,71,72,73
I2C_SDA_F2_FF1_XMIT 38
I2C_SCL_F2_FF1_XMIT 38
/F2_FF1_XMIT_INT 38
/F2_FF1_XMIT_PRESENT 38

6 /RESET G1 G2 → GND
7 SDA
8 SCL
GND 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.8/3.3V >=25G 3.8V <=16G 3.3V
9 RSVD
GND 2 GND

V_3V3
C2128 +22 UF 0603 6.3V
C1755 0.1 UF 0402
L88 1.0 UH 1008
C2129 +22 UF 0603 6.3V
C1757 0.1 UF 0402

V_F2_FF1_XMIT 30
C2130 +22 UF 0603 6.3V
C2131 0.1 UF 0402
L115 1.0 UH 1008
C2132 +22 UF 0603 6.3V
C2133 0.1 UF 0402

<Implementation>

U555-2 FIREFLY_XMIT_X12 FIREFLY XMIT X12

B19 A19	GND_B19 GND_A19	0P 0N	B18 B17	pF2_FF1_XMIT0 nF2_FF1_XMIT0
A18 A17	pF2_FF1_XMIT1 nF2_FF1_XMIT1	1P 1N		
B16 A16	GND_B16 GND_A16	2P 2N	B15 B14	pF2_FF1_XMIT2 nF2_FF1_XMIT2
A15 A14	pF2_FF1_XMIT3 nF2_FF1_XMIT3	3P 3N		
B13 A13	GND_B13 GND_A13	4P 4N	B12 B11	pF2_FF1_XMIT4 nF2_FF1_XMIT4
A12 A11	pF2_FF1_XMIT5 nF2_FF1_XMIT5	5P 5N		
B10 A10	GND_B10 GND_A10	6P 6N	B9 B8	pF2_FF1_XMIT6 nF2_FF1_XMIT6
A9 A8	pF2_FF1_XMIT7 nF2_FF1_XMIT7	7P 7N		
B7 A7	GND_B7 GND_A7	8P 8N	B6 B5	pF2_FF1_XMIT8 nF2_FF1_XMIT8
A6 A5	pF2_FF1_XMIT9 nF2_FF1_XMIT9	9P 9N		
B4 A4	GND_B4 GND_A4	10P 10N	B3 B2	pF2_FF1_XMIT10 nF2_FF1_XMIT10
A3 A2	pF2_FF1_XMIT11 nF2_FF1_XMIT11	11P 11N		
B1 A1	GND_B1 GND_A1			

GND → 1 GA135 2 GA136 3 GA137 4 GA138 5 GA139 6 GA140

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U202-24 AC GTY QUAD 121

BB39 BB40		MGTREFCLK0P_121 MGTREFCLK0N_121
BA41 BA42		MGTREFCLK1P_121 MGTREFCLK1N_121
pF2_FF1_RECV0 nF2_FF1_RECV0	BK34 BK35	MGTYRXP0_121 MGTYRXN0_121
pF2_FF1_XMIT0 nF2_FF1_XMIT0	BL37 BL38	MGTYTXP0_121 MGTYTXN0_121
pF2_FF1_RECV1 nF2_FF1_RECV1	BL32 BL33	MGTYRXP1_121 MGTYRXN1_121
pF2_FF1_XMIT1 nF2_FF1_XMIT1	BK39 BK40	MGTYTXP1_121 MGTYTXN1_121
pF2_FF1_RECV2 nF2_FF1_RECV2	BL46 BL47	MGTYRXP2_121 MGTYRXN2_121
pF2_FF1_XMIT2 nF2_FF1_XMIT2	BL41 BL42	MGTYTXP2_121 MGTYTXN2_121
pF2_FF1_RECV3 nF2_FF1_RECV3	BJ46 BJ47	MGTYRXP3_121 MGTYRXN3_121
pF2_FF1_XMIT3 nF2_FF1_XMIT3	BK43 BK44	MGTYTXP3_121 MGTYTXN3_121

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U202-25 AD GTY QUAD 122

AY39 AY40		MGTREFCLK0P_122 MGTREFCLK0N_122
AW41 AW42		MGTREFCLK1P_122 MGTREFCLK1N_122
pF2_FF1_RECV4 nF2_FF1_RECV4	BH48 BH49	MGTYRXP0_122 MGTYRXN0_122
pF2_FF1_XMIT4 nF2_FF1_XMIT4	BG41 BG42	MGTYTXP0_122 MGTYTXN0_122
pF2_FF1_RECV5 nF2_FF1_RECV5	BG50 BG51	MGTYRXP1_122 MGTYRXN1_122
pF2_FF1_XMIT5 nF2_FF1_XMIT5	BJ41 BJ42	MGTYTXP1_122 MGTYTXN1_122
pF2_FF1_RECV6 nF2_FF1_RECV6	BG46 BG47	MGTYRXP2_122 MGTYRXN2_122
pF2_FF1_XMIT6 nF2_FF1_XMIT6	BH43 BH44	MGTYTXP2_122 MGTYTXN2_122
pF2_FF1_RECV7 nF2_FF1_RECV7	BF48 BF49	MGTYRXP3_122 MGTYRXN3_122
pF2_FF1_XMIT7 nF2_FF1_XMIT7	BF43 BF44	MGTYTXP3_122 MGTYTXN3_122

FPGA_VU13P_A2577

V_M3V3
R1052 3.3K 0603
R1053 3.3K 0603
R1054 2.2K 0603
R1055 2.2K 0603

U562-1 FIREFLY_RECV_X12 FIREFLY RECV X12

/F2_FF_RESET 38,67,68,69,70,71,72,73
I2C_SDA_F2_FF1_RECV 38
I2C_SCL_F2_FF1_RECV 38
/F2_FF1_RECV_INT 38
/F2_FF1_RECV_PRESENT 38

6 /RESET G1 G2 → GND
7 SDA
8 SCL
GND 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.3V
9 RSVD
GND 2 GND

V_3V3
C2137 +22 UF 0603 6.3V
C2134 0.1 UF 0402
L116 1.0 UH 1008
C2135 +22 UF 0603 6.3V
C2136 0.1 UF 0402

L117 1.0 UH 1008
C2138 +22 UF 0603 6.3V
C2139 0.1 UF 0402

<Implementation>

U562-2 FIREFLY_RECV_X12 FIREFLY RECV X12

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17	pF2_FF1_RECV0 nF2_FF1_RECV0
B18 B17	pF2_FF1_RECV1 nF2_FF1_RECV1	1P 1N		
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14	pF2_FF1_RECV2 nF2_FF1_RECV2
B15 B14	pF2_FF1_RECV3 nF2_FF1_RECV3	3P 3N		
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11	pF2_FF1_RECV4 nF2_FF1_RECV4
B12 B11	pF2_FF1_RECV5 nF2_FF1_RECV5	5P 5N		
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8	pF2_FF1_RECV6 nF2_FF1_RECV6
B9 B8	pF2_FF1_RECV7 nF2_FF1_RECV7	7P 7N		
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5	pF2_FF1_RECV8 nF2_FF1_RECV8
B6 B5	pF2_FF1_RECV9 nF2_FF1_RECV9	9P 9N		
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2	pF2_FF1_RECV10 nF2_FF1_RECV10
B3 B2	pF2_FF1_RECV11 nF2_FF1_RECV11	11P 11N		
B1 A1	GND_B1 GND_A1			

GND → 1 GA141 2 GA142 3 GA143 4 GA144 5 GA145 6 GA146

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U202-26 AE GTY QUAD 123

AV39 AV40		MGTREFCLK0P_123 MGTREFCLK0N_123
AU41 AU42		MGTREFCLK1P_123 MGTREFCLK1N_123
pF2_FF1_RECV8 nF2_FF1_RECV8	BE50 BE51	MGTYRXP0_123 MGTYRXN0_123
pF2_FF1_XMIT8 nF2_FF1_XMIT8	BE45 BE46	MGTYTXP0_123 MGTYTXN0_123
pF2_FF1_RECV9 nF2_FF1_RECV9	BD48 BD49	MGTYRXP1_123 MGTYRXN1_123
pF2_FF1_XMIT9 nF2_FF1_XMIT9	BD43 BD44	MGTYTXP1_123 MGTYTXN1_123
pF2_FF1_RECV10 nF2_FF1_RECV10	BC50 BC51	MGTYRXP2_123 MGTYRXN2_123
pF2_FF1_XMIT10 nF2_FF1_XMIT10	BC45 BC46	MGTYTXP2_123 MGTYTXN2_123
pF2_FF1_RECV11 nF2_FF1_RECV11	BB48 BB49	MGTYRXP3_123 MGTYRXN3_123
pF2_FF1_XMIT11 nF2_FF1_XMIT11	BB43 BB44	MGTYTXP3_123 MGTYTXN3_123

FPGA_VU13P_A2577

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1

Title: 8.02: FPGA#2 FF#1 X12 ON QUADS AC AD AE

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8.03: FPGA#2 FF#2 X12 ON QUADS Q R S

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF2L_R0_4 18
ac_nF2L_R0_4 18
ac_pF2L_R1_4 20
ac_nF2L_R1_4 20

U106-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

/F2_FF_RESET 38,67,68,69,70,71,72,73
I2C_SDA_F2_FF2_XMIT 38
I2C_SCL_F2_FF2_XMIT 38
/F2_FF2_XMIT_INT 38
/F2_FF2_XMIT_PRESENT 38
V_F2_FF2_XMIT 30

R268 3.3K 0603 · R267 3.3K 0603 · R265 2.2K 0603 · R266 2.2K 0603

/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.8/3.3V (>=25G 3.8V <=166 3.3V), RSVD, GND

C2140 22 UF 0603 6.3V · C2141 0.1 UF 0402 · C2142 22 UF 0603 6.3V · C2143 0.1 UF 0402
L118 1.0 UH 1008 · L119 1.0 UH 1008
C2144 22 UF 0603 6.3V · C2145 0.1 UF 0402 · C2146 22 UF 0603 6.3V · C2147 0.1 UF 0402

U106-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

B19 GND_B19 / A19 GND_A19	0P / 0N	B18 pF2_FF2_XMIT0	B17 nF2_FF2_XMIT0
		A18 pF2_FF2_XMIT1	A17 nF2_FF2_XMIT1
B16 GND_B16 / A16 GND_A16	1P / 1N	B15 pF2_FF2_XMIT2	B14 nF2_FF2_XMIT2
	2P / 2N	A15 pF2_FF2_XMIT3	A14 nF2_FF2_XMIT3
B13 GND_B13 / A13 GND_A13	3P / 3N	B12 pF2_FF2_XMIT4	B11 nF2_FF2_XMIT4
	4P / 4N	A12 pF2_FF2_XMIT5	A11 nF2_FF2_XMIT5
B10 GND_B10 / A10 GND_A10	5P / 5N	B9 pF2_FF2_XMIT6	B8 nF2_FF2_XMIT6
	6P / 6N	A9 pF2_FF2_XMIT7	A8 nF2_FF2_XMIT7
B7 GND_B7 / A7 GND_A7	7P / 7N	B6 pF2_FF2_XMIT8	B5 nF2_FF2_XMIT8
	8P / 8N	A6 pF2_FF2_XMIT9	A5 nF2_FF2_XMIT9
B4 GND_B4 / A4 GND_A4	9P / 9N	B3 pF2_FF2_XMIT10	B2 nF2_FF2_XMIT10
	10P / 10N	A3 pF2_FF2_XMIT11	A2 nF2_FF2_XMIT11
B1 GND_B1 / A1 GND_A1	11P / 11N		

GND_A77 · GND_A78 · GND_A79 · GND_A80 · GND_A81 · GND_A82

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U202-28 Q — GTY QUAD 125

	AP39 / AP40	MGTREFCLK0P_125 / MGTREFCLK0N_125
	AN41 / AN42	MGTREFCLK1P_125 / MGTREFCLK1N_125
pF2_FF2_RECV0 / nF2_FF2_RECV0	AU50 / AU51	MGTYRXP0_125 / MGTYRXN0_125
pF2_FF2_XMIT0 / nF2_FF2_XMIT0	AU45 / AU46	MGTYTXP0_125 / MGTYTXN0_125
pF2_FF2_RECV1 / nF2_FF2_RECV1	AT48 / AT49	MGTYRXP1_125 / MGTYRXN1_125
pF2_FF2_XMIT1 / nF2_FF2_XMIT1	AT43 / AT44	MGTYTXP1_125 / MGTYTXN1_125
pF2_FF2_RECV2 / nF2_FF2_RECV2	AR50 / AR51	MGTYRXP2_125 / MGTYRXN2_125
pF2_FF2_XMIT2 / nF2_FF2_XMIT2	AR45 / AR46	MGTYTXP2_125 / MGTYTXN2_125
pF2_FF2_RECV3 / nF2_FF2_RECV3	AP48 / AP49	MGTYRXP3_125 / MGTYRXN3_125
pF2_FF2_XMIT3 / nF2_FF2_XMIT3	AP43 / AP44	MGTYTXP3_125 / MGTYTXN3_125

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U202-29 R — GTY QUAD 126

	AM39 / AM40	MGTREFCLK0P_126 / MGTREFCLK0N_126
	AL41 / AL42	MGTREFCLK1P_126 / MGTREFCLK1N_126
pF2_FF2_RECV4 / nF2_FF2_RECV4	AN50 / AN51	MGTYRXP0_126 / MGTYRXN0_126
pF2_FF2_XMIT4 / nF2_FF2_XMIT4	AN45 / AN46	MGTYTXP0_126 / MGTYTXN0_126
pF2_FF2_RECV5 / nF2_FF2_RECV5	AM48 / AM49	MGTYRXP1_126 / MGTYRXN1_126
pF2_FF2_XMIT5 / nF2_FF2_XMIT5	AM43 / AM44	MGTYTXP1_126 / MGTYTXN1_126
pF2_FF2_RECV6 / nF2_FF2_RECV6	AL50 / AL51	MGTYRXP2_126 / MGTYRXN2_126
pF2_FF2_XMIT6 / nF2_FF2_XMIT6	AL45 / AL46	MGTYTXP2_126 / MGTYTXN2_126
pF2_FF2_RECV7 / nF2_FF2_RECV7	AK48 / AK49	MGTYRXP3_126 / MGTYRXN3_126
pF2_FF2_XMIT7 / nF2_FF2_XMIT7	AK43 / AK44	MGTYTXP3_126 / MGTYTXN3_126

FPGA_VU13P_A2577

U107-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

/F2_FF_RESET 38,67,68,69,70,71,72,73
I2C_SDA_F2_FF2_RECV 38
I2C_SCL_F2_FF2_RECV 38
/F2_FF2_RECV_INT 38
/F2_FF2_RECV_PRESENT 38

R272 3.3K 0603 · R271 3.3K 0603 · R269 2.2K 0603 · R270 2.2K 0603

/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.3V, RSVD, GND

C2148 22 UF 0603 6.3V · C2149 0.1 UF 0402 · C2150 22 UF 0603 6.3V · C2151 0.1 UF 0402
L120 1.0 UH 1008 · L121 1.0 UH 1008
C2152 22 UF 0603 6.3V · C2153 0.1 UF 0402

U107-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

B19 GND_B19 / A19 GND_A19	0P / 0N	A18 pF2_FF2_RECV0	A17 nF2_FF2_RECV0
		B18 pF2_FF2_RECV1	B17 nF2_FF2_RECV1
B16 GND_B16 / A16 GND_A16	1P / 1N	A15 pF2_FF2_RECV2	A14 nF2_FF2_RECV2
	2P / 2N	B15 pF2_FF2_RECV3	B14 nF2_FF2_RECV3
B13 GND_B13 / A13 GND_A13	3P / 3N	A12 pF2_FF2_RECV4	A11 nF2_FF2_RECV4
	4P / 4N	B12 pF2_FF2_RECV5	B11 nF2_FF2_RECV5
B10 GND_B10 / A10 GND_A10	5P / 5N	A9 pF2_FF2_RECV6	A8 nF2_FF2_RECV6
	6P / 6N	B9 pF2_FF2_RECV7	B8 nF2_FF2_RECV7
B7 GND_B7 / A7 GND_A7	7P / 7N	A6 pF2_FF2_RECV8	A5 nF2_FF2_RECV8
	8P / 8N	B6 pF2_FF2_RECV9	B5 nF2_FF2_RECV9
B4 GND_B4 / A4 GND_A4	9P / 9N	A3 pF2_FF2_RECV10	A2 nF2_FF2_RECV10
	10P / 10N	B3 pF2_FF2_RECV11	B2 nF2_FF2_RECV11
B1 GND_B1 / A1 GND_A1	11P / 11N		

GND_A147 · GND_A148 · GND_A149 · GND_A150 · GND_A151 · GND_A152

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U202-30 S — GTY QUAD 127

	AJ41 / AJ42	MGTREFCLK0P_127 / MGTREFCLK0N_127
	AG41 / AG42	MGTREFCLK1P_127 / MGTREFCLK1N_127
pF2_FF2_RECV8 / nF2_FF2_RECV8	AJ50 / AJ51	MGTYRXP0_127 / MGTYRXN0_127
pF2_FF2_XMIT8 / nF2_FF2_XMIT8	AJ45 / AJ46	MGTYTXP0_127 / MGTYTXN0_127
pF2_FF2_RECV9 / nF2_FF2_RECV9	AH48 / AH49	MGTYRXP1_127 / MGTYRXN1_127
pF2_FF2_XMIT9 / nF2_FF2_XMIT9	AH43 / AH44	MGTYTXP1_127 / MGTYTXN1_127
pF2_FF2_RECV10 / nF2_FF2_RECV10	AG50 / AG51	MGTYRXP2_127 / MGTYRXN2_127
pF2_FF2_XMIT10 / nF2_FF2_XMIT10	AG45 / AG46	MGTYTXP2_127 / MGTYTXN2_127
pF2_FF2_RECV11 / nF2_FF2_RECV11	AF48 / AF49	MGTYRXP3_127 / MGTYRXN3_127
pF2_FF2_XMIT11 / nF2_FF2_XMIT11	AF43 / AF44	MGTYTXP3_127 / MGTYTXN3_127

FPGA_VU13P_A2577

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1	
Title	8.03: FPGA#2 FF#2 X12 ON QUADS Q R S
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8.04: FPGA#2 FF#3 X12 ON QUADS X Y Z

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF2L_R0_7 18
ac_nF2L_R0_7 18
ac_pF2L_R1_7 20
ac_nF2L_R1_7 20

V_M3V3
R260 3.3K 0603
R259 3.3K 0603
R257 2.2K 0603
R258 2.2K 0603

U104-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

/F2_FF_RESET 38,67,68,69,70,71,72,73
I2C_SDA_F2_FF3_XMIT 38
I2C_SCL_F2_FF3_XMIT 38
/F2_FF3_XMIT_INT 38
/F2_FF3_XMIT_PRESENT 38
V_3V3
V_F2_FF3_XMIT 30

C2154 22 UF 0603 6.3V
C2155 0.1 UF 0402
L122 1.0 UH 1008
C2156 22 UF 0603 6.3V
C2157 0.1 UF 0402
C2158 22 UF 0603 6.3V
C2159 0.1 UF 0402
L123 1.0 UH 1008
C2160 22 UF 0603 6.3V
C2161 0.1 UF 0402

/RESET G1 G2 GND
SDA
SCL
/SELECT
/INT
/PRESENT
3.3V
3.8/3.3V >=256 3.8V <=166 3.3V
RSVD
GND
<Implementation>

U104-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

B19 A19	GND_B19 GND_A19	0P 0N	B18 B17	pF2_FF3_XMIT0 nF2_FF3_XMIT0
		1P 1N	A18 A17	pF2_FF3_XMIT1 nF2_FF3_XMIT1
B16 A16	GND_B16 GND_A16	2P 2N	B15 B14	pF2_FF3_XMIT2 nF2_FF3_XMIT2
		3P 3N	A15 A14	pF2_FF3_XMIT3 nF2_FF3_XMIT3
B13 A13	GND_B13 GND_A13	4P 4N	B12 B11	pF2_FF3_XMIT4 nF2_FF3_XMIT4
		5P 5N	A12 A11	pF2_FF3_XMIT5 nF2_FF3_XMIT5
B10 A10	GND_B10 GND_A10	6P 6N	B9 B8	pF2_FF3_XMIT6 nF2_FF3_XMIT6
		7P 7N	A9 A8	pF2_FF3_XMIT7 nF2_FF3_XMIT7
B7 A7	GND_B7 GND_A7	8P 8N	B6 B5	pF2_FF3_XMIT8 nF2_FF3_XMIT8
		9P 9N	A6 A5	pF2_FF3_XMIT9 nF2_FF3_XMIT9
B4 A4	GND_B4 GND_A4	10P 10N	B3 B2	pF2_FF3_XMIT10 nF2_FF3_XMIT10
		11P 11N	A3 A2	pF2_FF3_XMIT11 nF2_FF3_XMIT11
B1 A1	GND_B1 GND_A1			

GND 3 1 G1 2 G2 A154 / A155 / A156 / A157

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U202-35 X — GTY QUAD 132

R41 R42		MGTREFCLK0P_132 MGTREFCLK0N_132
P39 P40		MGTREFCLK1P_132 MGTREFCLK1N_132
pF2_FF3_RECV0 nF2_FF3_RECV0	J50 J51	MGTYRXP0_132 MGTYRXN0_132
pF2_FF3_XMIT0 nF2_FF3_XMIT0	J45 J46	MGTYTXP0_132 MGTYTXN0_132
pF2_FF3_RECV1 nF2_FF3_RECV1	H48 H49	MGTYRXP1_132 MGTYRXN1_132
pF2_FF3_XMIT1 nF2_FF3_XMIT1	H43 H44	MGTYTXP1_132 MGTYTXN1_132
pF2_FF3_RECV2 nF2_FF3_RECV2	G50 G51	MGTYRXP2_132 MGTYRXN2_132
pF2_FF3_XMIT2 nF2_FF3_XMIT2	G45 G46	MGTYTXP2_132 MGTYTXN2_132
pF2_FF3_RECV3 nF2_FF3_RECV3	F48 F49	MGTYRXP3_132 MGTYRXN3_132
pF2_FF3_XMIT3 nF2_FF3_XMIT3	F43 F44	MGTYTXP3_132 MGTYTXN3_132

FPGA_VU13P_A2577

U202-36 Y — GTY QUAD 133

N41 N42		MGTREFCLK0P_133 MGTREFCLK0N_133
M39 M40		MGTREFCLK1P_133 MGTREFCLK1N_133
pF2_FF3_RECV4 nF2_FF3_RECV4	E50 E51	MGTYRXP0_133 MGTYRXN0_133
pF2_FF3_XMIT4 nF2_FF3_XMIT4	D43 D44	MGTYTXP0_133 MGTYTXN0_133
pF2_FF3_RECV5 nF2_FF3_RECV5	D48 D49	MGTYRXP1_133 MGTYRXN1_133
pF2_FF3_XMIT5 nF2_FF3_XMIT5	B43 B44	MGTYTXP1_133 MGTYTXN1_133
pF2_FF3_RECV6 nF2_FF3_RECV6	E46 E47	MGTYRXP2_133 MGTYRXN2_133
pF2_FF3_XMIT6 nF2_FF3_XMIT6	C41 C42	MGTYTXP2_133 MGTYTXN2_133
pF2_FF3_RECV7 nF2_FF3_RECV7	C46 C47	MGTYRXP3_133 MGTYRXN3_133
pF2_FF3_XMIT7 nF2_FF3_XMIT7	E41 E42	MGTYTXP3_133 MGTYTXN3_133

FPGA_VU13P_A2577

V_M3V3
R264 3.3K 0603
R263 3.3K 0603
R261 2.2K 0603
R262 2.2K 0603

U105-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

/F2_FF_RESET 38,67,68,69,70,71,72,73
I2C_SDA_F2_FF3_RECV 38
I2C_SCL_F2_FF3_RECV 38
/F2_FF3_RECV_INT 38
/F2_FF3_RECV_PRESENT 38
V_3V3

C2162 22 UF 0603 6.3V
C2163 0.1 UF 0402
L124 1.0 UH 1008
C2164 22 UF 0603 6.3V
C2165 0.1 UF 0402
L125 1.0 UH 1008
C2166 22 UF 0603 6.3V
C2167 0.1 UF 0402

/RESET G1 G2 GND
SDA
SCL
/SELECT
/INT
/PRESENT
3.3V
3.3V
RSVD
GND
<Implementation>

U105-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17	pF2_FF3_RECV0 nF2_FF3_RECV0
		1P 1N	B18 B17	pF2_FF3_RECV1 nF2_FF3_RECV1
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14	pF2_FF3_RECV2 nF2_FF3_RECV2
		3P 3N	B15 B14	pF2_FF3_RECV3 nF2_FF3_RECV3
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11	pF2_FF3_RECV4 nF2_FF3_RECV4
		5P 5N	B12 B11	pF2_FF3_RECV5 nF2_FF3_RECV5
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8	pF2_FF3_RECV6 nF2_FF3_RECV6
		7P 7N	B9 B8	pF2_FF3_RECV7 nF2_FF3_RECV7
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5	pF2_FF3_RECV8 nF2_FF3_RECV8
		9P 9N	B6 B5	pF2_FF3_RECV9 nF2_FF3_RECV9
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2	pF2_FF3_RECV10 nF2_FF3_RECV10
		11P 11N	B3 B2	pF2_FF3_RECV11 nF2_FF3_RECV11
B1 A1	GND_B1 GND_A1			

GND 3 1 G1 2 G2 A159 / A160 / A161 / A162 / A163 / A164

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U202-37 Z — GTY QUAD 134

L41 L42		MGTREFCLK0P_134 MGTREFCLK0N_134
K39 K40		MGTREFCLK1P_134 MGTREFCLK1N_134
pF2_FF3_RECV8 nF2_FF3_RECV8	A46 A47	MGTYRXP0_134 MGTYRXN0_134
pF2_FF3_XMIT8 nF2_FF3_XMIT8	A41 A42	MGTYTXP0_134 MGTYTXN0_134
pF2_FF3_RECV9 nF2_FF3_RECV9	A32 A33	MGTYRXP1_134 MGTYRXN1_134
pF2_FF3_XMIT9 nF2_FF3_XMIT9	B39 B40	MGTYTXP1_134 MGTYTXN1_134
pF2_FF3_RECV10 nF2_FF3_RECV10	B34 B35	MGTYRXP2_134 MGTYRXN2_134
pF2_FF3_XMIT10 nF2_FF3_XMIT10	A37 A38	MGTYTXP2_134 MGTYTXN2_134
pF2_FF3_RECV11 nF2_FF3_RECV11	C32 C33	MGTYRXP3_134 MGTYRXN3_134
pF2_FF3_XMIT11 nF2_FF3_XMIT11	C37 C38	MGTYTXP3_134 MGTYTXN3_134

FPGA_VU13P_A2577

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1

Title: 8.04: FPGA#2 FF#3 X12 ON QUADS X Y Z

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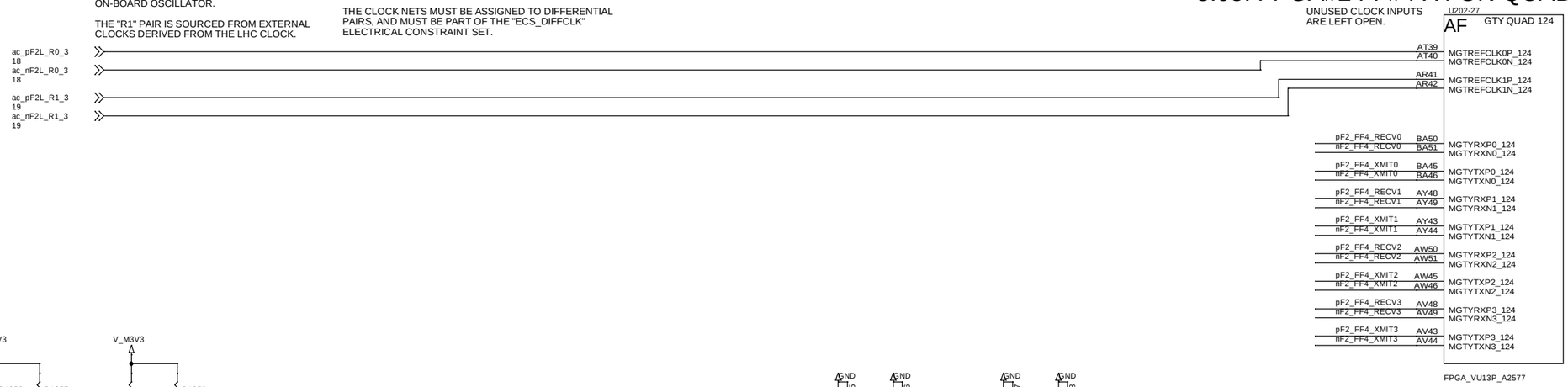
8.05: FPGA#2 FF#4 X4 ON QUAD AF

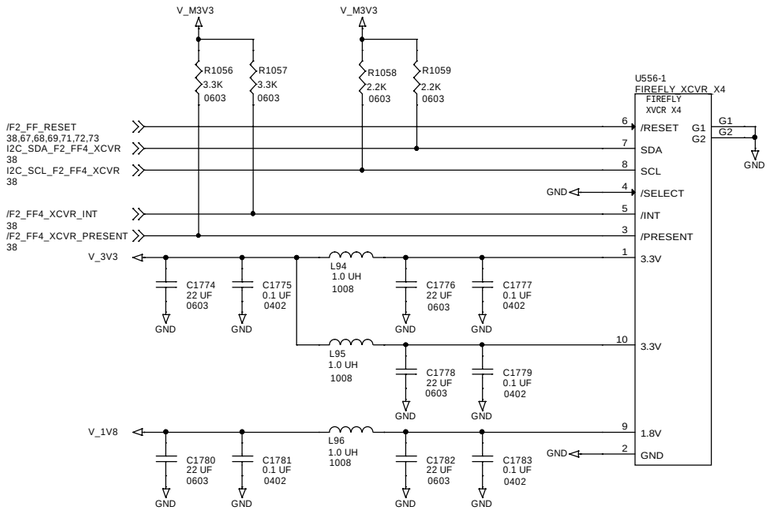
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

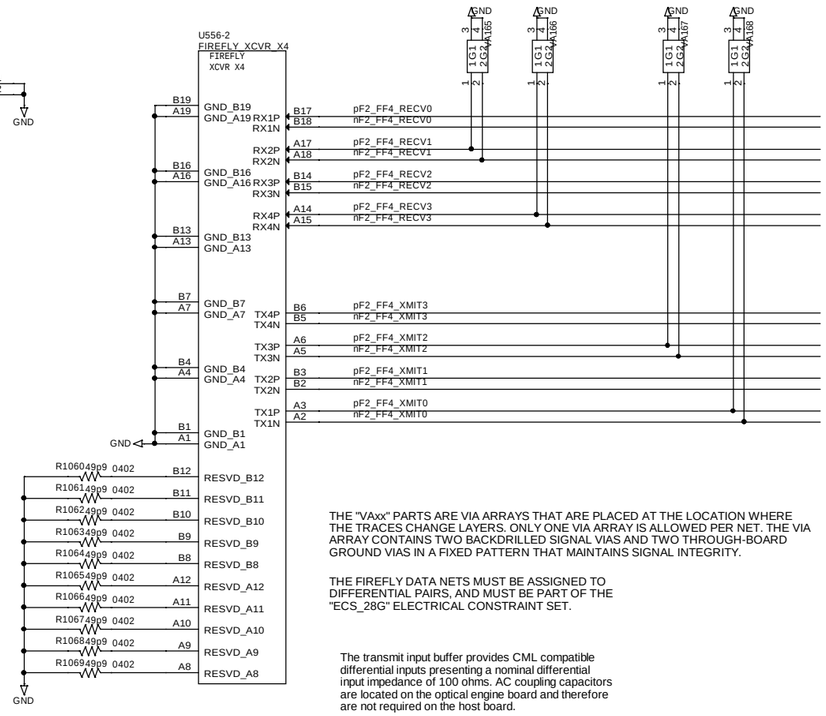
THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.







THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1		
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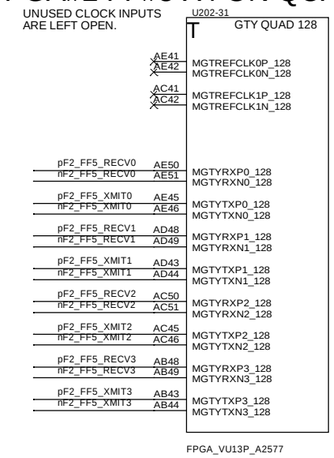
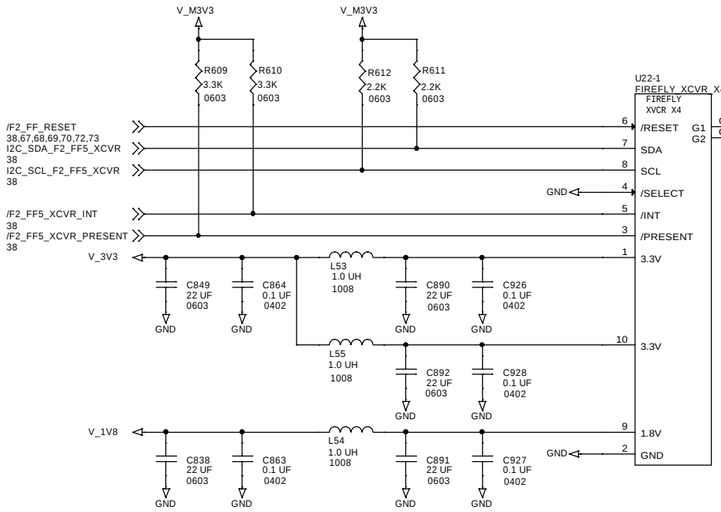
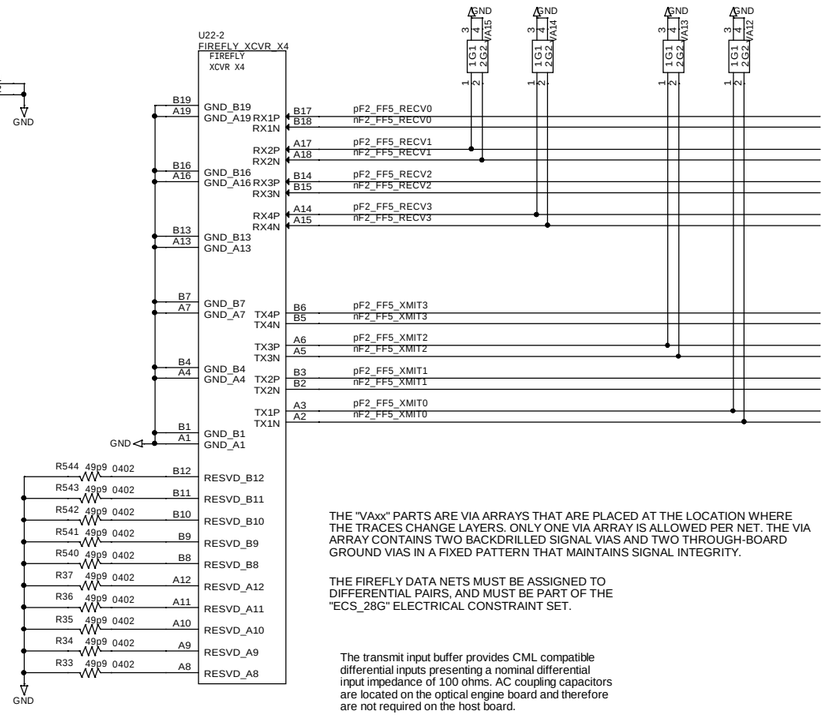
8.06: FPGA#2 FF#5 X4 ON QUAD T

UNUSED CLOCK INPUTS
ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1		
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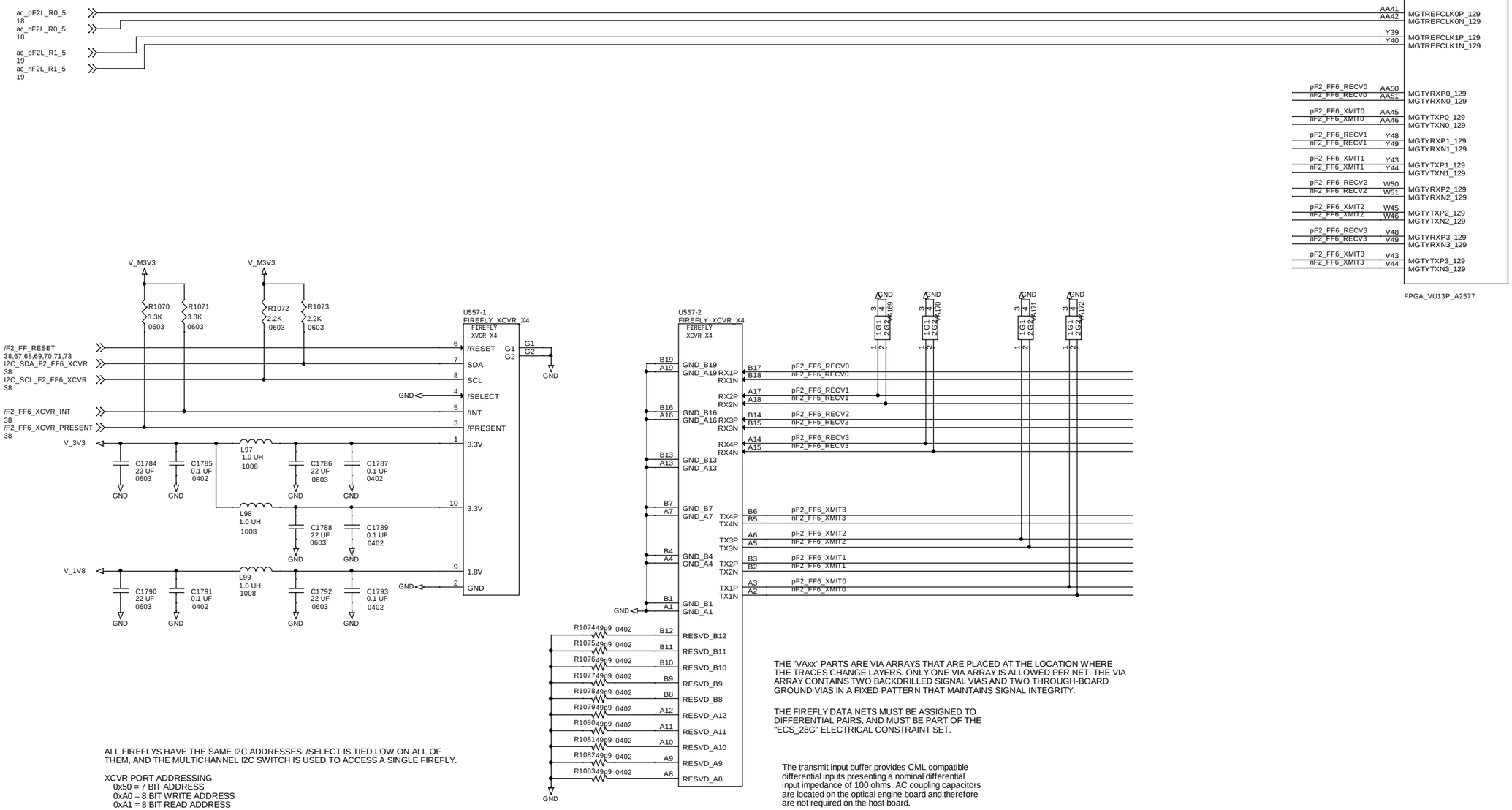
8.07: FPGA#2 FF#6 X4 ON QUAD U

UNUSED CLOCK INPUTS
ARE LEFT OPEN.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

APOLLO CM W/ DUAL A2577, MK1

Title: 8.07: FPGA#2 FF#6 X4 ON QUAD U

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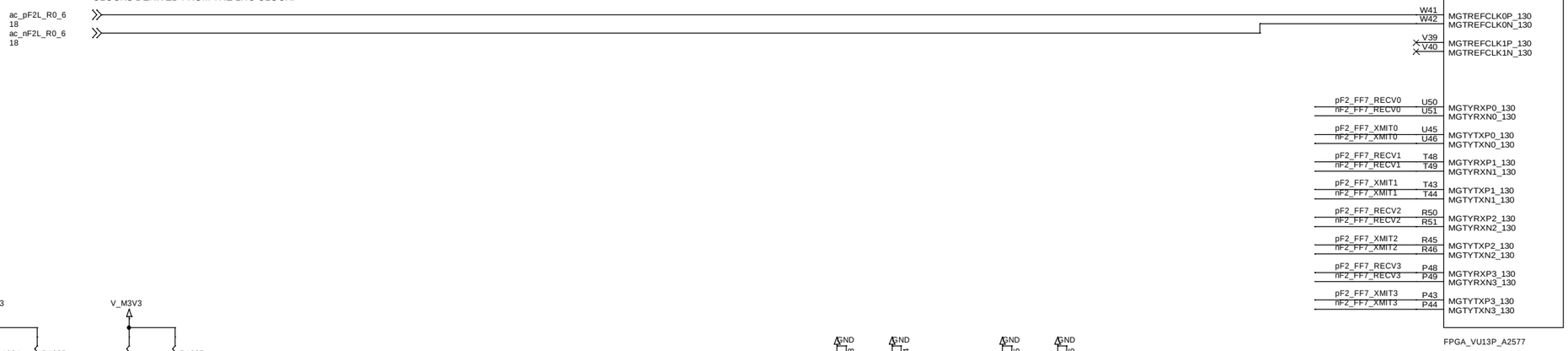
8.08: FPGA#2 FF#7 X4 ON QUAD V

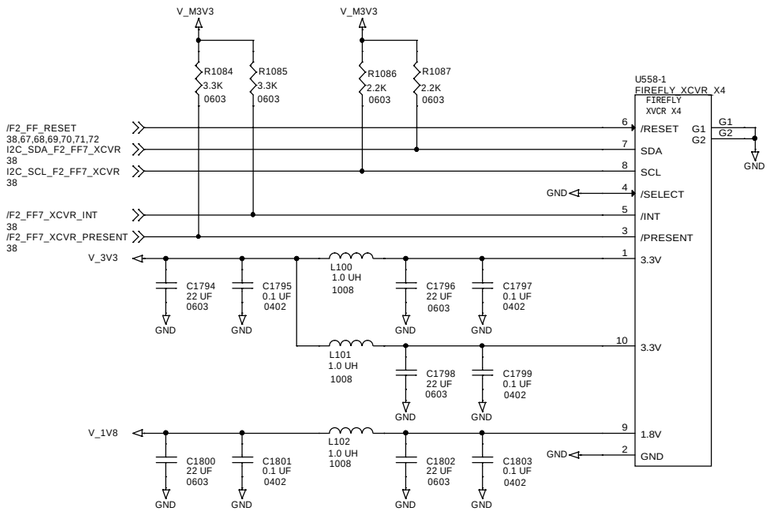
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

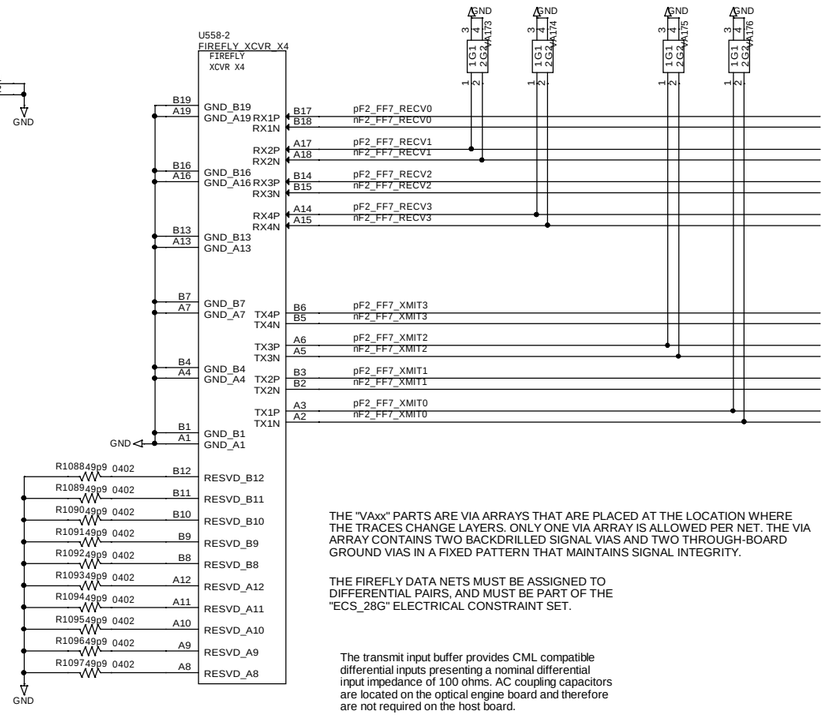
THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

APOLLO CM W/ DUAL A2577, MK1			
Title: 8.08: FPGA#2 FF#7 X4 ON QUAD V			
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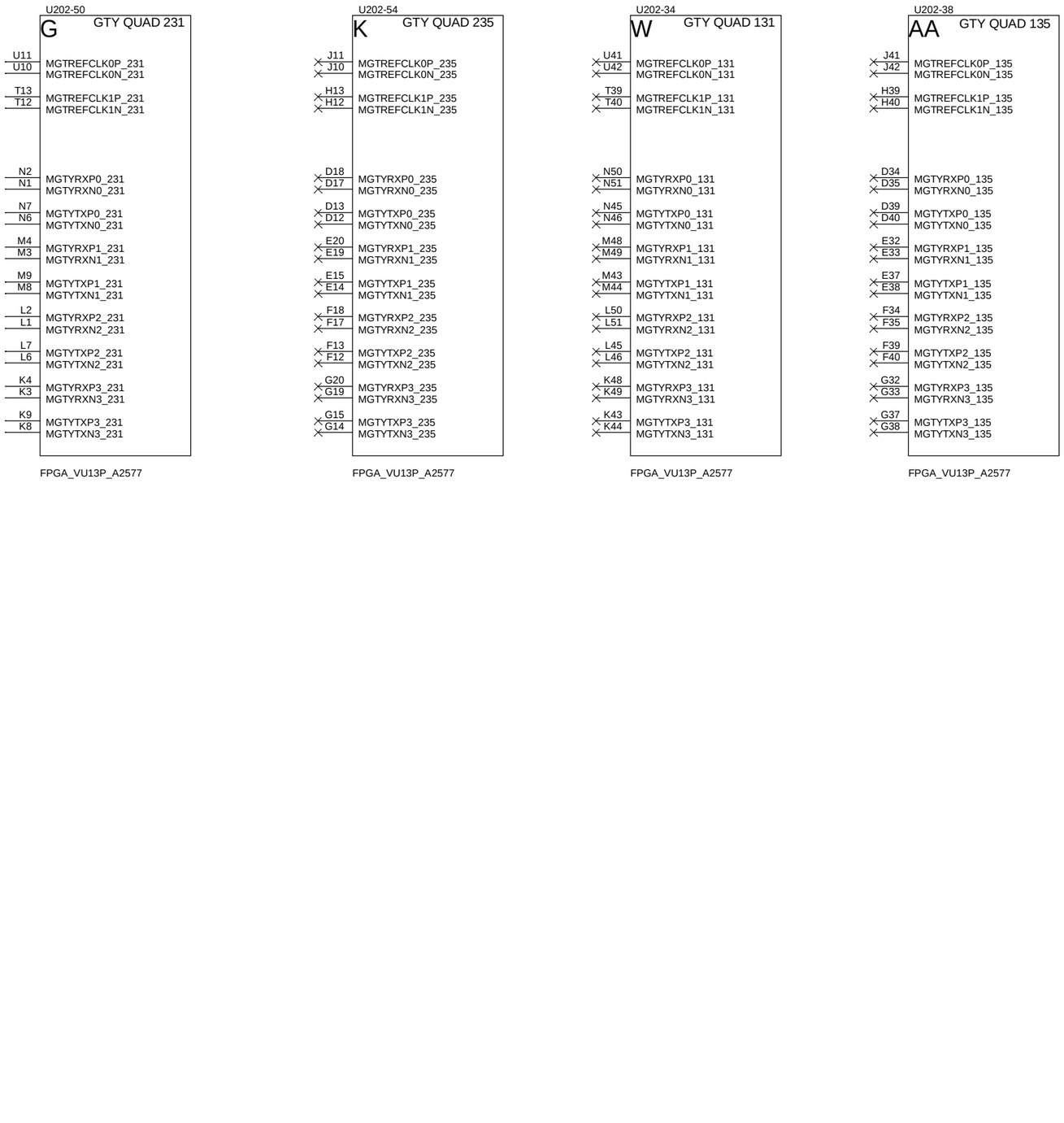
8.09: FPGA#2 UNUSED QUADS G, K, W, AA



APOLLO CM W/ DUAL A2577, MK1		
Title: 8.09: FPGA#2 UNUSED QUADS G, K, W, AA		
Size	Document Number: 6089-119	Rev: A
Date: Wednesday, February 17, 2021	Sheet 74 of 80	

9.01: F1 QUADS M, N, O TO F2 QUADS J, I, H

FPGA#1

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

FPGA#2

U201-40
GTY QUAD 221 M

MGTREFCLK0P_221	BB13	
MGTREFCLK0N_221	BB12	
MGTREFCLK1P_221	BA11	
MGTREFCLK1N_221	BA10	
MGTYRXP0_221	BK18	pF1_M_RECV0
MGTYRXN0_221	BK17	nF1_M_RECV0
MGTYTXP0_221	BL15	pF1_M_XMIT0
MGTYTXN0_221	BL14	nF1_M_XMIT0
MGTYRXP1_221	BL20	pF1_M_RECV1
MGTYRXN1_221	BL19	nF1_M_RECV1
MGTYTXP1_221	BK13	pF1_M_XMIT1
MGTYTXN1_221	BK12	nF1_M_XMIT1
MGTYRXP2_221	BL6	pF1_M_RECV2
MGTYRXN2_221	BL5	nF1_M_RECV2
MGTYTXP2_221	BL11	pF1_M_XMIT2
MGTYTXN2_221	BL10	nF1_M_XMIT2
MGTYRXP3_221	BJ6	pF1_M_RECV3
MGTYRXN3_221	BJ5	nF1_M_RECV3
MGTYTXP3_221	BK9	pF1_M_XMIT3
MGTYTXN3_221	BK8	nF1_M_XMIT3

FPGA_VU13P_A2577

U201-41
GTY QUAD 222 N

MGTREFCLK0P_222	AY13	ac_pF1R_R0_2 18
MGTREFCLK0N_222	AY12	ac_nF1R_R0_2 18
MGTREFCLK1P_222	AW11	ac_pF1R_R1_2 21
MGTREFCLK1N_222	AW10	ac_nF1R_R1_2 21
MGTYRXP0_222	BH4	pF1_N_RECV0
MGTYRXN0_222	BH3	nF1_N_RECV0
MGTYTXP0_222	BG11	pF1_N_XMIT0
MGTYTXN0_222	BG10	nF1_N_XMIT0
MGTYRXP1_222	BG2	pF1_N_RECV1
MGTYRXN1_222	BG1	nF1_N_RECV1
MGTYTXP1_222	BJ11	pF1_N_XMIT1
MGTYTXN1_222	BJ10	nF1_N_XMIT1
MGTYRXP2_222	BG6	pF1_N_RECV2
MGTYRXN2_222	BG5	nF1_N_RECV2
MGTYTXP2_222	BH9	pF1_N_XMIT2
MGTYTXN2_222	BH8	nF1_N_XMIT2
MGTYRXP3_222	BF4	pF1_N_RECV3
MGTYRXN3_222	BF3	nF1_N_RECV3
MGTYTXP3_222	BF9	pF1_N_XMIT3
MGTYTXN3_222	BF8	nF1_N_XMIT3

FPGA_VU13P_A2577

U201-42
GTY QUAD 223 O

MGTREFCLK0P_223	AV13	
MGTREFCLK0N_223	AV12	
MGTREFCLK1P_223	AU11	
MGTREFCLK1N_223	AU10	
MGTYRXP0_223	BE2	pF1_O_RECV0
MGTYRXN0_223	BE1	nF1_O_RECV0
MGTYTXP0_223	BE7	pF1_O_XMIT0
MGTYTXN0_223	BE6	nF1_O_XMIT0
MGTYRXP1_223	BD4	pF1_O_RECV1
MGTYRXN1_223	BD3	nF1_O_RECV1
MGTYTXP1_223	BD9	pF1_O_XMIT1
MGTYTXN1_223	BD8	nF1_O_XMIT1
MGTYRXP2_223	BC2	pF1_O_RECV2
MGTYRXN2_223	BC1	nF1_O_RECV2
MGTYTXP2_223	BC7	pF1_O_XMIT2
MGTYTXN2_223	BC6	nF1_O_XMIT2
MGTYRXP3_223	BB4	pF1_O_RECV3
MGTYRXN3_223	BB3	nF1_O_RECV3
MGTYTXP3_223	BB9	pF1_O_XMIT3
MGTYTXN3_223	BB8	nF1_O_XMIT3

FPGA_VU13P_A2577

pF1_M_RECV0	C1804 0.1 UF 0402	pF2_J_XMIT0	
pF1_M_RECV1	C1805 0.1 UF 0402	pF2_J_XMIT1	
pF1_M_RECV2	C1807 0.1 UF 0402	pF2_J_XMIT2	
pF1_M_RECV3	C1809 0.1 UF 0402	pF2_J_XMIT3	
	C1811 0.1 UF 0402		
	C1813 0.1 UF 0402		
	C1815 0.1 UF 0402		
	C1817 0.1 UF 0402		

pF1_M_XMIT0	0402 0.1 UF C1806	pF2_J_RECV0	
pF1_M_XMIT1	0402 0.1 UF C1808	pF2_J_RECV1	
pF1_M_XMIT2	0402 0.1 UF C1810	pF2_J_RECV2	
pF1_M_XMIT3	0402 0.1 UF C1812	pF2_J_RECV3	
	0402 0.1 UF C1814		
	0402 0.1 UF C1816		
	0402 0.1 UF C1818		
	0402 0.1 UF C1819		

U202-53
GTY QUAD 234 J

L11	MGTREFCLK0P_234	
L10	MGTREFCLK0N_234	
K13	MGTREFCLK1P_234	
K12	MGTREFCLK1N_234	
A6	MGTYRXP0_234	pF2_J_RECV0
A5	MGTYRXN0_234	nF2_J_RECV0
A11	MGTYTXP0_234	pF2_J_XMIT0
A10	MGTYTXN0_234	nF2_J_XMIT0
A20	MGTYRXP1_234	pF2_J_RECV1
A19	MGTYRXN1_234	nF2_J_RECV1
B13	MGTYTXP1_234	pF2_J_XMIT1
B12	MGTYTXN1_234	nF2_J_XMIT1
B18	MGTYRXP2_234	pF2_J_RECV2
B17	MGTYRXN2_234	nF2_J_RECV2
A15	MGTYTXP2_234	pF2_J_XMIT2
A14	MGTYTXN2_234	nF2_J_XMIT2
C20	MGTYRXP3_234	pF2_J_RECV3
C19	MGTYRXN3_234	nF2_J_RECV3
C15	MGTYTXP3_234	pF2_J_XMIT3
C14	MGTYTXN3_234	nF2_J_XMIT3

FPGA_VU13P_A2577

U202-52
GTY QUAD 233 I

ac_pF2R_R0_7 18		
ac_nF2R_R0_7 18	N11	MGTREFCLK0P_233
	N10	MGTREFCLK0N_233
ac_pF2R_R1_7 21	M13	MGTREFCLK1P_233
ac_nF2R_R1_7 21	M12	MGTREFCLK1N_233
E2	MGTYRXP0_233	pF2_I_RECV0
E1	MGTYRXN0_233	nF2_I_RECV0
D9	MGTYTXP0_233	pF2_I_XMIT0
D8	MGTYTXN0_233	nF2_I_XMIT0
D4	MGTYRXP1_233	pF2_I_RECV1
D3	MGTYRXN1_233	nF2_I_RECV1
B9	MGTYTXP1_233	pF2_I_XMIT1
B8	MGTYTXN1_233	nF2_I_XMIT1
E6	MGTYRXP2_233	pF2_I_RECV2
E5	MGTYRXN2_233	nF2_I_RECV2
C11	MGTYTXP2_233	pF2_I_XMIT2
C10	MGTYTXN2_233	nF2_I_XMIT2
C6	MGTYRXP3_233	pF2_I_RECV3
C5	MGTYRXN3_233	nF2_I_RECV3
E11	MGTYTXP3_233	pF2_I_XMIT3
E10	MGTYTXN3_233	nF2_I_XMIT3

FPGA_VU13P_A2577

pF1_N_RECV0	C1820 0.1 UF 0402	pF2_I_XMIT0	
pF1_N_RECV1	C1821 0.1 UF 0402	pF2_I_XMIT1	
pF1_N_RECV2	C1823 0.1 UF 0402	pF2_I_XMIT2	
pF1_N_RECV3	C1825 0.1 UF 0402	pF2_I_XMIT3	
	C1827 0.1 UF 0402		
	C1829 0.1 UF 0402		
	C1831 0.1 UF 0402		
	C1833 0.1 UF 0402		

pF1_N_XMIT0	0402 0.1 UF C1822	pF2_I_RECV0	
pF1_N_XMIT1	0402 0.1 UF C1824	pF2_I_RECV1	
pF1_N_XMIT2	0402 0.1 UF C1826	pF2_I_RECV2	
pF1_N_XMIT3	0402 0.1 UF C1828	pF2_I_RECV3	
	0402 0.1 UF C1830		
	0402 0.1 UF C1832		
	0402 0.1 UF C1834		
	0402 0.1 UF C1835		

pF1_O_RECV0	C1836 0.1 UF 0402	pF2_H_XMIT0	
pF1_O_RECV1	C1837 0.1 UF 0402	pF2_H_XMIT1	
pF1_O_RECV2	C1839 0.1 UF 0402	pF2_H_XMIT2	
pF1_O_RECV3	C1841 0.1 UF 0402	pF2_H_XMIT3	
	C1843 0.1 UF 0402		
	C1845 0.1 UF 0402		
	C1847 0.1 UF 0402		
	C1849 0.1 UF 0402		

pF1_O_XMIT0	0402 0.1 UF C1838	pF2_H_RECV0	
pF1_O_XMIT1	0402 0.1 UF C1840	pF2_H_RECV1	
pF1_O_XMIT2	0402 0.1 UF C1842	pF2_H_RECV2	
pF1_O_XMIT3	0402 0.1 UF C1844	pF2_H_RECV3	
	0402 0.1 UF C1846		
	0402 0.1 UF C1848		
	0402 0.1 UF C1850		
	0402 0.1 UF C1851		

U202-51
GTY QUAD 232 H

R11	MGTREFCLK0P_232	
R10	MGTREFCLK0N_232	
P13	MGTREFCLK1P_232	
P12	MGTREFCLK1N_232	
J2	MGTYRXP0_232	pF2_H_RECV0
J1	MGTYRXN0_232	nF2_H_RECV0
J7	MGTYTXP0_232	pF2_H_XMIT0
J6	MGTYTXN0_232	nF2_H_XMIT0
H4	MGTYRXP1_232	pF2_H_RECV1
H3	MGTYRXN1_232	nF2_H_RECV1
H9	MGTYTXP1_232	pF2_H_XMIT1
H8	MGTYTXN1_232	nF2_H_XMIT1
G2	MGTYRXP2_232	pF2_H_RECV2
G1	MGTYRXN2_232	nF2_H_RECV2
G7	MGTYTXP2_232	pF2_H_XMIT2
G6	MGTYTXN2_232	nF2_H_XMIT2
F4	MGTYRXP3_232	pF2_H_RECV3
F3	MGTYRXN3_232	nF2_H_RECV3
F9	MGTYTXP3_232	pF2_H_XMIT3
F8	MGTYTXN3_232	nF2_H_XMIT3

FPGA_VU13P_A2577

APOLLO CM W/ DUAL A2577, MK1

Title: 9.01: F1 QUADS M, N, O TO F2 QUADS J, I, H

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9.02: F1 QUADS A, B, C TO F2 QUADS F, E, D

FPGA#1

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

FPGA#2

U201-44
GTY QUAD 225 A

MGTREFCLK0P_225	AP13	
MGTREFCLK0N_225	AP12	
MGTREFCLK1P_225	AN11	
MGTREFCLK1N_225	AN10	
MGTYRXP0_225	AU2	pF1_A_RECV0
MGTYRXN0_225	AU1	nF1_A_RECV0
MGTYTXP0_225	AU7	pF1_A_XMIT0
MGTYTXN0_225	AU6	nF1_A_XMIT0
MGTYRXP1_225	AT4	pF1_A_RECV1
MGTYRXN1_225	AT3	nF1_A_RECV1
MGTYTXP1_225	AT9	pF1_A_XMIT1
MGTYTXN1_225	AT8	nF1_A_XMIT1
MGTYRXP2_225	AR2	pF1_A_RECV2
MGTYRXN2_225	AR1	nF1_A_RECV2
MGTYTXP2_225	AR7	pF1_A_XMIT2
MGTYTXN2_225	AR6	nF1_A_XMIT2
MGTYRXP3_225	AP4	pF1_A_RECV3
MGTYRXN3_225	AP3	nF1_A_RECV3
MGTYTXP3_225	AP9	pF1_A_XMIT3
MGTYTXN3_225	AP8	nF1_A_XMIT3

FPGA_VU13P_A2577

U202-49
F GTY QUAD 230

ac_pF2R_R0_6 18	W11	
ac_nF2R_R0_6 18	W10	
	V13	MGTREFCLK0P_230
	V12	MGTREFCLK0N_230
		MGTREFCLK1P_230
		MGTREFCLK1N_230
pF2_F_RECV0	U2	MGTYRXP0_230
nF2_F_RECV0	U1	MGTYRXN0_230
pF2_F_XMIT0	U7	MGTYTXP0_230
nF2_F_XMIT0	U6	MGTYTXN0_230
pF2_F_RECV1	T4	MGTYRXP1_230
nF2_F_RECV1	T3	MGTYRXN1_230
pF2_F_XMIT1	T9	MGTYTXP1_230
nF2_F_XMIT1	T8	MGTYTXN1_230
pF2_F_RECV2	R2	MGTYRXP2_230
nF2_F_RECV2	R1	MGTYRXN2_230
pF2_F_XMIT2	R7	MGTYTXP2_230
nF2_F_XMIT2	R6	MGTYTXN2_230
pF2_F_RECV3	P4	MGTYRXP3_230
nF2_F_RECV3	P3	MGTYRXN3_230
pF2_F_XMIT3	P9	MGTYTXP3_230
nF2_F_XMIT3	P8	MGTYTXN3_230

FPGA_VU13P_A2577

pF1_A_RECV0	C1852 0.1 UF 0402	pF2_F_XMIT0	pF1_A_XMIT0	0402 0.1 UF C1854 pF2_F_RECV0
nF1_A_RECV0	C1853 0.1 UF 0402	nF2_F_XMIT0	nF1_A_XMIT0	0402 0.1 UF C1856 nF2_F_RECV0
pF1_A_RECV1	C1855 0.1 UF 0402	pF2_F_XMIT1	pF1_A_XMIT1	0402 0.1 UF C1858 pF2_F_RECV1
nF1_A_RECV1	C1857 0.1 UF 0402	nF2_F_XMIT1	nF1_A_XMIT1	0402 0.1 UF C1860 nF2_F_RECV1
pF1_A_RECV2	C1859 0.1 UF 0402	pF2_F_XMIT2	pF1_A_XMIT2	0402 0.1 UF C1862 pF2_F_RECV2
nF1_A_RECV2	C1861 0.1 UF 0402	nF2_F_XMIT2	nF1_A_XMIT2	0402 0.1 UF C1864 nF2_F_RECV2
pF1_A_RECV3	C1863 0.1 UF 0402	pF2_F_XMIT3	pF1_A_XMIT3	0402 0.1 UF C1866 pF2_F_RECV3
nF1_A_RECV3	C1865 0.1 UF 0402	nF2_F_XMIT3	nF1_A_XMIT3	0402 0.1 UF C1867 nF2_F_RECV3

U201-45
GTY QUAD 226 B

MGTREFCLK0P_226	AM13	ac_pF1R_R0_3 18
MGTREFCLK0N_226	AM12	ac_nF1R_R0_3 18
MGTREFCLK1P_226	AL11	ac_pF1R_R1_3 21
MGTREFCLK1N_226	AL10	ac_nF1R_R1_3 21
MGTYRXP0_226	AN2	pF1_B_RECV0
MGTYRXN0_226	AN1	nF1_B_RECV0
MGTYTXP0_226	AN7	pF1_B_XMIT0
MGTYTXN0_226	AN6	nF1_B_XMIT0
MGTYRXP1_226	AM4	pF1_B_RECV1
MGTYRXN1_226	AM3	nF1_B_RECV1
MGTYTXP1_226	AM9	pF1_B_XMIT1
MGTYTXN1_226	AM8	nF1_B_XMIT1
MGTYRXP2_226	AL2	pF1_B_RECV2
MGTYRXN2_226	AL1	nF1_B_RECV2
MGTYTXP2_226	AL7	pF1_B_XMIT2
MGTYTXN2_226	AL6	nF1_B_XMIT2
MGTYRXP3_226	AK4	pF1_B_RECV3
MGTYRXN3_226	AK3	nF1_B_RECV3
MGTYTXP3_226	AK9	pF1_B_XMIT3
MGTYTXN3_226	AK8	nF1_B_XMIT3

FPGA_VU13P_A2577

U202-48
E GTY QUAD 229

ac_pF2R_R0_5 18	AA11	
ac_nF2R_R0_5 18	AA10	
ac_pF2R_R1_5 21	Y13	
ac_nF2R_R1_5 21	Y12	
		MGTREFCLK0P_229
		MGTREFCLK0N_229
		MGTREFCLK1P_229
		MGTREFCLK1N_229
pF2_E_RECV0	AA2	MGTYRXP0_229
nF2_E_RECV0	AA1	MGTYRXN0_229
pF2_E_XMIT0	AA7	MGTYTXP0_229
nF2_E_XMIT0	AA6	MGTYTXN0_229
pF2_E_RECV1	Y4	MGTYRXP1_229
nF2_E_RECV1	Y3	MGTYRXN1_229
pF2_E_XMIT1	Y9	MGTYTXP1_229
nF2_E_XMIT1	Y8	MGTYTXN1_229
pF2_E_RECV2	W2	MGTYRXP2_229
nF2_E_RECV2	W1	MGTYRXN2_229
pF2_E_XMIT2	W7	MGTYTXP2_229
nF2_E_XMIT2	W6	MGTYTXN2_229
pF2_E_RECV3	V4	MGTYRXP3_229
nF2_E_RECV3	V3	MGTYRXN3_229
pF2_E_XMIT3	V9	MGTYTXP3_229
nF2_E_XMIT3	V8	MGTYTXN3_229

FPGA_VU13P_A2577

pF1_B_RECV0	C1868 0.1 UF 0402	pF2_E_XMIT0	pF1_B_XMIT0	0402 0.1 UF C1870 pF2_E_RECV0
nF1_B_RECV0	C1869 0.1 UF 0402	nF2_E_XMIT0	nF1_B_XMIT0	0402 0.1 UF C1872 nF2_E_RECV0
pF1_B_RECV1	C1871 0.1 UF 0402	pF2_E_XMIT1	pF1_B_XMIT1	0402 0.1 UF C1874 pF2_E_RECV1
nF1_B_RECV1	C1873 0.1 UF 0402	nF2_E_XMIT1	nF1_B_XMIT1	0402 0.1 UF C1876 nF2_E_RECV1
pF1_B_RECV2	C1875 0.1 UF 0402	pF2_E_XMIT2	pF1_B_XMIT2	0402 0.1 UF C1878 pF2_E_RECV2
nF1_B_RECV2	C1877 0.1 UF 0402	nF2_E_XMIT2	nF1_B_XMIT2	0402 0.1 UF C1880 nF2_E_RECV2
pF1_B_RECV3	C1879 0.1 UF 0402	pF2_E_XMIT3	pF1_B_XMIT3	0402 0.1 UF C1882 pF2_E_RECV3
nF1_B_RECV3	C1881 0.1 UF 0402	nF2_E_XMIT3	nF1_B_XMIT3	0402 0.1 UF C1883 nF2_E_RECV3

U201-46
GTY QUAD 227 C

MGTREFCLK0P_227	AJ11	
MGTREFCLK0N_227	AJ10	
MGTREFCLK1P_227	AG11	
MGTREFCLK1N_227	AG10	
MGTYRXP0_227	AJ2	pF1_C_RECV0
MGTYRXN0_227	AJ1	nF1_C_RECV0
MGTYTXP0_227	AJ7	pF1_C_XMIT0
MGTYTXN0_227	AJ6	nF1_C_XMIT0
MGTYRXP1_227	AH4	pF1_C_RECV1
MGTYRXN1_227	AH3	nF1_C_RECV1
MGTYTXP1_227	AH9	pF1_C_XMIT1
MGTYTXN1_227	AH8	nF1_C_XMIT1
MGTYRXP2_227	AG2	pF1_C_RECV2
MGTYRXN2_227	AG1	nF1_C_RECV2
MGTYTXP2_227	AG7	pF1_C_XMIT2
MGTYTXN2_227	AG6	nF1_C_XMIT2
MGTYRXP3_227	AF4	pF1_C_RECV3
MGTYRXN3_227	AF3	nF1_C_RECV3
MGTYTXP3_227	AF9	pF1_C_XMIT3
MGTYTXN3_227	AF8	nF1_C_XMIT3

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U202-47
D GTY QUAD 228

	AE11	MGTREFCLK0P_228
	AE10	MGTREFCLK0N_228
	AC11	MGTREFCLK1P_228
	AC10	MGTREFCLK1N_228
pF2_D_RECV0	AE2	MGTYRXP0_228
nF2_D_RECV0	AE1	MGTYRXN0_228
pF2_D_XMIT0	AE7	MGTYTXP0_228
nF2_D_XMIT0	AE6	MGTYTXN0_228
pF2_D_RECV1	AD4	MGTYRXP1_228
nF2_D_RECV1	AD3	MGTYRXN1_228
pF2_D_XMIT1	AD9	MGTYTXP1_228
nF2_D_XMIT1	AD8	MGTYTXN1_228
pF2_D_RECV2	AC2	MGTYRXP2_228
nF2_D_RECV2	AC1	MGTYRXN2_228
pF2_D_XMIT2	AC7	MGTYTXP2_228
nF2_D_XMIT2	AC6	MGTYTXN2_228
pF2_D_RECV3	AB4	MGTYRXP3_228
nF2_D_RECV3	AB3	MGTYRXN3_228
pF2_D_XMIT3	AB9	MGTYTXP3_228
nF2_D_XMIT3	AB8	MGTYTXN3_228

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pF1_C_RECV0	C1884 0.1 UF 0402	pF2_D_XMIT0	pF1_C_XMIT0	0402 0.1 UF C1886 pF2_D_RECV0
nF1_C_RECV0	C1885 0.1 UF 0402	nF2_D_XMIT0	nF1_C_XMIT0	0402 0.1 UF C1888 nF2_D_RECV0
pF1_C_RECV1	C1887 0.1 UF 0402	pF2_D_XMIT1	pF1_C_XMIT1	0402 0.1 UF C1890 pF2_D_RECV1
nF1_C_RECV1	C1889 0.1 UF 0402	nF2_D_XMIT1	nF1_C_XMIT1	0402 0.1 UF C1892 nF2_D_RECV1
pF1_C_RECV2	C1891 0.1 UF 0402	pF2_D_XMIT2	pF1_C_XMIT2	0402 0.1 UF C1894 pF2_D_RECV2
nF1_C_RECV2	C1893 0.1 UF 0402	nF2_D_XMIT2	nF1_C_XMIT2	0402 0.1 UF C1896 nF2_D_RECV2
pF1_C_RECV3	C1895 0.1 UF 0402	pF2_D_XMIT3	pF1_C_XMIT3	0402 0.1 UF C1898 pF2_D_RECV3
nF1_C_RECV3	C1897 0.1 UF 0402	nF2_D_XMIT3	nF1_C_XMIT3	0402 0.1 UF C1899 nF2_D_RECV3

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Title: 9.02: F1 QUADS A, B, C TO F2 QUADS F, E, D

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9.03: F1 QUADS H, I, J TO F2 QUADS O, N, M

FPGA#1

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

FPGA#2

U201-51
GTY QUAD 232 H

MGTREFCLK0P_232	R11	
MGTREFCLK0N_232	R10	
MGTREFCLK1P_232	P13	
MGTREFCLK1N_232	P12	
MGTYRXP0_232	J2	pF1_H_RECV0
MGTYRXN0_232	J1	nF1_H_RECV0
MGTYTXP0_232	J7	pF1_H_XMIT0
MGTYTXN0_232	J6	nF1_H_XMIT0
MGTYRXP1_232	H4	pF1_H_RECV1
MGTYRXN1_232	H3	nF1_H_RECV1
MGTYTXP1_232	H9	pF1_H_XMIT1
MGTYTXN1_232	H8	nF1_H_XMIT1
MGTYRXP2_232	G2	pF1_H_RECV2
MGTYRXN2_232	G1	nF1_H_RECV2
MGTYTXP2_232	G7	pF1_H_XMIT2
MGTYTXN2_232	G6	nF1_H_XMIT2
MGTYRXP3_232	F4	pF1_H_RECV3
MGTYRXN3_232	F3	nF1_H_RECV3
MGTYTXP3_232	F9	pF1_H_XMIT3
MGTYTXN3_232	F8	nF1_H_XMIT3

FPGA_VU13P_A2577

U201-52
GTY QUAD 233 I

MGTREFCLK0P_233	N11	ac_pF1R_R0_7 18
MGTREFCLK0N_233	N10	ac_nF1R_R0_7 18
MGTREFCLK1P_233	M13	ac_pF1R_R1_7 21
MGTREFCLK1N_233	M12	ac_nF1R_R1_7 21
MGTYRXP0_233	E2	pF1_I_RECV0
MGTYRXN0_233	E1	nF1_I_RECV0
MGTYTXP0_233	D9	pF1_I_XMIT0
MGTYTXN0_233	D8	nF1_I_XMIT0
MGTYRXP1_233	D4	pF1_I_RECV1
MGTYRXN1_233	D3	nF1_I_RECV1
MGTYTXP1_233	B9	pF1_I_XMIT1
MGTYTXN1_233	B8	nF1_I_XMIT1
MGTYRXP2_233	E6	pF1_I_RECV2
MGTYRXN2_233	E5	nF1_I_RECV2
MGTYTXP2_233	C11	pF1_I_XMIT2
MGTYTXN2_233	C10	nF1_I_XMIT2
MGTYRXP3_233	C6	pF1_I_RECV3
MGTYRXN3_233	C5	nF1_I_RECV3
MGTYTXP3_233	E11	pF1_I_XMIT3
MGTYTXN3_233	E10	nF1_I_XMIT3

FPGA_VU13P_A2577

U201-53
GTY QUAD 234 J

MGTREFCLK0P_234	L11	
MGTREFCLK0N_234	L10	
MGTREFCLK1P_234	K13	
MGTREFCLK1N_234	K12	
MGTYRXP0_234	A6	pF1_J_RECV0
MGTYRXN0_234	A5	nF1_J_RECV0
MGTYTXP0_234	A11	pF1_J_XMIT0
MGTYTXN0_234	A10	nF1_J_XMIT0
MGTYRXP1_234	A20	pF1_J_RECV1
MGTYRXN1_234	A19	nF1_J_RECV1
MGTYTXP1_234	B13	pF1_J_XMIT1
MGTYTXN1_234	B12	nF1_J_XMIT1
MGTYRXP2_234	B18	pF1_J_RECV2
MGTYRXN2_234	B17	nF1_J_RECV2
MGTYTXP2_234	A15	pF1_J_XMIT2
MGTYTXN2_234	A14	nF1_J_XMIT2
MGTYRXP3_234	C20	pF1_J_RECV3
MGTYRXN3_234	C19	nF1_J_RECV3
MGTYTXP3_234	C15	pF1_J_XMIT3
MGTYTXN3_234	C14	nF1_J_XMIT3

FPGA_VU13P_A2577

pF1_H_RECV0 / nF1_H_RECV0 — C1900 0.1 UF 0402 — pF2_O_XMIT0 / nF2_O_XMIT0
C1901 0.1 UF 0402
pF1_H_RECV1 / nF1_H_RECV1 — C1903 0.1 UF 0402 — pF2_O_XMIT1 / nF2_O_XMIT1
C1905 0.1 UF 0402
pF1_H_RECV2 / nF1_H_RECV2 — C1907 0.1 UF 0402 — pF2_O_XMIT2 / nF2_O_XMIT2
C1909 0.1 UF 0402
pF1_H_RECV3 / nF1_H_RECV3 — C1911 0.1 UF 0402 — pF2_O_XMIT3 / nF2_O_XMIT3
C1913 0.1 UF 0402

pF1_H_XMIT0 / nF1_H_XMIT0 — 0402 0.1 UF C1902 — pF2_O_RECV0 / nF2_O_RECV0
0402 0.1 UF C1904
pF1_H_XMIT1 / nF1_H_XMIT1 — 0402 0.1 UF C1906 — pF2_O_RECV1 / nF2_O_RECV1
0402 0.1 UF C1908
pF1_H_XMIT2 / nF1_H_XMIT2 — 0402 0.1 UF C1910 — pF2_O_RECV2 / nF2_O_RECV2
0402 0.1 UF C1912
pF1_H_XMIT3 / nF1_H_XMIT3 — 0402 0.1 UF C1914 — pF2_O_RECV3 / nF2_O_RECV3
0402 0.1 UF C1915

U202-42
GTY QUAD 223 O

AV13		
AV12		MGTREFCLK0P_223
		MGTREFCLK0N_223
AU11		
AU10		MGTREFCLK1P_223
		MGTREFCLK1N_223
pF2_O_RECV0	BE2	MGTYRXP0_223
nF2_O_RECV0	BE1	MGTYRXN0_223
pF2_O_XMIT0	BE7	MGTYTXP0_223
nF2_O_XMIT0	BE6	MGTYTXN0_223
pF2_O_RECV1	BD4	MGTYRXP1_223
nF2_O_RECV1	BD3	MGTYRXN1_223
pF2_O_XMIT1	BD9	MGTYTXP1_223
nF2_O_XMIT1	BD8	MGTYTXN1_223
pF2_O_RECV2	BC2	MGTYRXP2_223
nF2_O_RECV2	BC1	MGTYRXN2_223
pF2_O_XMIT2	BC7	MGTYTXP2_223
nF2_O_XMIT2	BC6	MGTYTXN2_223
pF2_O_RECV3	BB4	MGTYRXP3_223
nF2_O_RECV3	BB3	MGTYRXN3_223
pF2_O_XMIT3	BB9	MGTYTXP3_223
nF2_O_XMIT3	BB8	MGTYTXN3_223

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U202-41
GTY QUAD 222 N

ac_pF2R_R0_2 18		
ac_nF2R_R0_2 18	AY13	
	AY12	MGTREFCLK0P_222
		MGTREFCLK0N_222
ac_pF2R_R1_2 21	AW11	
ac_nF2R_R1_2 21	AW10	MGTREFCLK1P_222
		MGTREFCLK1N_222
pF2_N_RECV0	BH4	MGTYRXP0_222
nF2_N_RECV0	BH3	MGTYRXN0_222
pF2_N_XMIT0	BG11	MGTYTXP0_222
nF2_N_XMIT0	BG10	MGTYTXN0_222
pF2_N_RECV1	BG2	MGTYRXP1_222
nF2_N_RECV1	BG1	MGTYRXN1_222
pF2_N_XMIT1	BJ11	MGTYTXP1_222
nF2_N_XMIT1	BJ10	MGTYTXN1_222
pF2_N_RECV2	BG6	MGTYRXP2_222
nF2_N_RECV2	BG5	MGTYRXN2_222
pF2_N_XMIT2	BH9	MGTYTXP2_222
nF2_N_XMIT2	BH8	MGTYTXN2_222
pF2_N_RECV3	BF4	MGTYRXP3_222
nF2_N_RECV3	BF3	MGTYRXN3_222
pF2_N_XMIT3	BF9	MGTYTXP3_222
nF2_N_XMIT3	BF8	MGTYTXN3_222

FPGA_VU13P_A2577

pF1_I_RECV0 / nF1_I_RECV0 — C1916 0.1 UF 0402 — pF2_N_XMIT0 / nF2_N_XMIT0
C1917 0.1 UF 0402
pF1_I_RECV1 / nF1_I_RECV1 — C1919 0.1 UF 0402 — pF2_N_XMIT1 / nF2_N_XMIT1
C1921 0.1 UF 0402
pF1_I_RECV2 / nF1_I_RECV2 — C1923 0.1 UF 0402 — pF2_N_XMIT2 / nF2_N_XMIT2
C1925 0.1 UF 0402
pF1_I_RECV3 / nF1_I_RECV3 — C1927 0.1 UF 0402 — pF2_N_XMIT3 / nF2_N_XMIT3
C1929 0.1 UF 0402

pF1_I_XMIT0 / nF1_I_XMIT0 — 0402 0.1 UF C1918 — pF2_N_RECV0 / nF2_N_RECV0
0402 0.1 UF C1920
pF1_I_XMIT1 / nF1_I_XMIT1 — 0402 0.1 UF C1922 — pF2_N_RECV1 / nF2_N_RECV1
0402 0.1 UF C1924
pF1_I_XMIT2 / nF1_I_XMIT2 — 0402 0.1 UF C1926 — pF2_N_RECV2 / nF2_N_RECV2
0402 0.1 UF C1928
pF1_I_XMIT3 / nF1_I_XMIT3 — 0402 0.1 UF C1930 — pF2_N_RECV3 / nF2_N_RECV3
0402 0.1 UF C1931

pF1_J_RECV0 / nF1_J_RECV0 — C1932 0.1 UF 0402 — pF2_M_XMIT0 / nF2_M_XMIT0
C1933 0.1 UF 0402
pF1_J_RECV1 / nF1_J_RECV1 — C1935 0.1 UF 0402 — pF2_M_XMIT1 / nF2_M_XMIT1
C1937 0.1 UF 0402
pF1_J_RECV2 / nF1_J_RECV2 — C1939 0.1 UF 0402 — pF2_M_XMIT2 / nF2_M_XMIT2
C1941 0.1 UF 0402
pF1_J_RECV3 / nF1_J_RECV3 — C1943 0.1 UF 0402 — pF2_M_XMIT3 / nF2_M_XMIT3
C1945 0.1 UF 0402

pF1_J_XMIT0 / nF1_J_XMIT0 — 0402 0.1 UF C1934 — pF2_M_RECV0 / nF2_M_RECV0
0402 0.1 UF C1936
pF1_J_XMIT1 / nF1_J_XMIT1 — 0402 0.1 UF C1938 — pF2_M_RECV1 / nF2_M_RECV1
0402 0.1 UF C1940
pF1_J_XMIT2 / nF1_J_XMIT2 — 0402 0.1 UF C1942 — pF2_M_RECV2 / nF2_M_RECV2
0402 0.1 UF C1944
pF1_J_XMIT3 / nF1_J_XMIT3 — 0402 0.1 UF C1946 — pF2_M_RECV3 / nF2_M_RECV3
0402 0.1 UF C1947

U202-40
GTY QUAD 221 M

BB13		
BB12		MGTREFCLK0P_221
		MGTREFCLK0N_221
BA11		
BA10		MGTREFCLK1P_221
		MGTREFCLK1N_221
pF2_M_RECV0	BK18	MGTYRXP0_221
nF2_M_RECV0	BK17	MGTYRXN0_221
pF2_M_XMIT0	BL15	MGTYTXP0_221
nF2_M_XMIT0	BL14	MGTYTXN0_221
pF2_M_RECV1	BL20	MGTYRXP1_221
nF2_M_RECV1	BL19	MGTYRXN1_221
pF2_M_XMIT1	BK13	MGTYTXP1_221
nF2_M_XMIT1	BK12	MGTYTXN1_221
pF2_M_RECV2	BL6	MGTYRXP2_221
nF2_M_RECV2	BL5	MGTYRXN2_221
pF2_M_XMIT2	BL11	MGTYTXP2_221
nF2_M_XMIT2	BL10	MGTYTXN2_221
pF2_M_RECV3	BJ6	MGTYRXP3_221
nF2_M_RECV3	BJ5	MGTYRXN3_221
pF2_M_XMIT3	BK9	MGTYTXP3_221
nF2_M_XMIT3	BK8	MGTYTXN3_221

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Title: 9.03: F1 QUADS H, I, J TO F2 QUADS O, N, M

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9.04: F1 QUADS D, E, F TO F2 QUADS C, B, A

FPGA#1

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

FPGA#2

U201-47 — GTY QUAD 228 D

MGTREFCLK0P_228	AE11	
MGTREFCLK0N_228	AE10	
MGTREFCLK1P_228	AC11	
MGTREFCLK1N_228	AC10	
MGTYRXP0_228	AE2	pF1_D_RECV0
MGTYRXN0_228	AE1	nF1_D_RECV0
MGTYTXP0_228	AE7	pF1_D_XMIT0
MGTYTXN0_228	AE6	nF1_D_XMIT0
MGTYRXP1_228	AD4	pF1_D_RECV1
MGTYRXN1_228	AD3	nF1_D_RECV1
MGTYTXP1_228	AD9	pF1_D_XMIT1
MGTYTXN1_228	AD8	nF1_D_XMIT1
MGTYRXP2_228	AC2	pF1_D_RECV2
MGTYRXN2_228	AC1	nF1_D_RECV2
MGTYTXP2_228	AC7	pF1_D_XMIT2
MGTYTXN2_228	AC6	nF1_D_XMIT2
MGTYRXP3_228	AB4	pF1_D_RECV3
MGTYRXN3_228	AB3	nF1_D_RECV3
MGTYTXP3_228	AB9	pF1_D_XMIT3
MGTYTXN3_228	AB8	nF1_D_XMIT3

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U201-48 — GTY QUAD 229 E

MGTREFCLK0P_229	AA11	ac_pF1R_R0_4 18
MGTREFCLK0N_229	AA10	ac_nF1R_R0_4 18
MGTREFCLK1P_229	Y13	ac_pF1R_R1_4 21
MGTREFCLK1N_229	Y12	ac_nF1R_R1_4 21
MGTYRXP0_229	AA2	pF1_E_RECV0
MGTYRXN0_229	AA1	nF1_E_RECV0
MGTYTXP0_229	AA7	pF1_E_XMIT0
MGTYTXN0_229	AA6	nF1_E_XMIT0
MGTYRXP1_229	Y4	pF1_E_RECV1
MGTYRXN1_229	Y3	nF1_E_RECV1
MGTYTXP1_229	Y9	pF1_E_XMIT1
MGTYTXN1_229	Y8	nF1_E_XMIT1
MGTYRXP2_229	W2	pF1_E_RECV2
MGTYRXN2_229	W1	nF1_E_RECV2
MGTYTXP2_229	W7	pF1_E_XMIT2
MGTYTXN2_229	W6	nF1_E_XMIT2
MGTYRXP3_229	V4	pF1_E_RECV3
MGTYRXN3_229	V3	nF1_E_RECV3
MGTYTXP3_229	V9	pF1_E_XMIT3
MGTYTXN3_229	V8	nF1_E_XMIT3

FPGA_VU13P_A2577

U201-49 — GTY QUAD 230 F

MGTREFCLK0P_230	W11	ac_pF1R_R0_5 18
MGTREFCLK0N_230	W10	ac_nF1R_R0_5 18
MGTREFCLK1P_230	V13	
MGTREFCLK1N_230	V12	
MGTYRXP0_230	U2	pF1_F_RECV0
MGTYRXN0_230	U1	nF1_F_RECV0
MGTYTXP0_230	U7	pF1_F_XMIT0
MGTYTXN0_230	U6	nF1_F_XMIT0
MGTYRXP1_230	T4	pF1_F_RECV1
MGTYRXN1_230	T3	nF1_F_RECV1
MGTYTXP1_230	T9	pF1_F_XMIT1
MGTYTXN1_230	T8	nF1_F_XMIT1
MGTYRXP2_230	R2	pF1_F_RECV2
MGTYRXN2_230	R1	nF1_F_RECV2
MGTYTXP2_230	R7	pF1_F_XMIT2
MGTYTXN2_230	R6	nF1_F_XMIT2
MGTYRXP3_230	P4	pF1_F_RECV3
MGTYRXN3_230	P3	nF1_F_RECV3
MGTYTXP3_230	P9	pF1_F_XMIT3
MGTYTXN3_230	P8	nF1_F_XMIT3

FPGA_VU13P_A2577

U202-46 — GTY QUAD 227 C

MGTREFCLK0P_227	AJ11	
MGTREFCLK0N_227	AJ10	
MGTREFCLK1P_227	AG11	
MGTREFCLK1N_227	AG10	
MGTYRXP0_227	AJ2	pF2_C_RECV0
MGTYRXN0_227	AJ1	nF2_C_RECV0
MGTYTXP0_227	AJ7	pF2_C_XMIT0
MGTYTXN0_227	AJ6	nF2_C_XMIT0
MGTYRXP1_227	AH4	pF2_C_RECV1
MGTYRXN1_227	AH3	nF2_C_RECV1
MGTYTXP1_227	AH9	pF2_C_XMIT1
MGTYTXN1_227	AH8	nF2_C_XMIT1
MGTYRXP2_227	AG2	pF2_C_RECV2
MGTYRXN2_227	AG1	nF2_C_RECV2
MGTYTXP2_227	AG7	pF2_C_XMIT2
MGTYTXN2_227	AG6	nF2_C_XMIT2
MGTYRXP3_227	AF4	pF2_C_RECV3
MGTYRXN3_227	AF3	nF2_C_RECV3
MGTYTXP3_227	AF9	pF2_C_XMIT3
MGTYTXN3_227	AF8	nF2_C_XMIT3

FPGA_VU13P_A2577

U202-45 — GTY QUAD 226 B

ac_pF2R_R0_4 18		
ac_nF2R_R0_4 18	AM13	
	AM12	MGTREFCLK0P_226
ac_pF2R_R1_4 21		MGTREFCLK0N_226
ac_nF2R_R1_4 21	AL11	
	AL10	MGTREFCLK1P_226
		MGTREFCLK1N_226
MGTYRXP0_226	AN2	pF2_B_RECV0
MGTYRXN0_226	AN1	nF2_B_RECV0
MGTYTXP0_226	AN7	pF2_B_XMIT0
MGTYTXN0_226	AN6	nF2_B_XMIT0
MGTYRXP1_226	AM4	pF2_B_RECV1
MGTYRXN1_226	AM3	nF2_B_RECV1
MGTYTXP1_226	AM9	pF2_B_XMIT1
MGTYTXN1_226	AM8	nF2_B_XMIT1
MGTYRXP2_226	AL2	pF2_B_RECV2
MGTYRXN2_226	AL1	nF2_B_RECV2
MGTYTXP2_226	AL7	pF2_B_XMIT2
MGTYTXN2_226	AL6	nF2_B_XMIT2
MGTYRXP3_226	AK4	pF2_B_RECV3
MGTYRXN3_226	AK3	nF2_B_RECV3
MGTYTXP3_226	AK9	pF2_B_XMIT3
MGTYTXN3_226	AK8	nF2_B_XMIT3

FPGA_VU13P_A2577

U202-44 — GTY QUAD 225 A

MGTREFCLK0P_225	AP13	
MGTREFCLK0N_225	AP12	
MGTREFCLK1P_225	AN11	
MGTREFCLK1N_225	AN10	
MGTYRXP0_225	AU2	pF2_A_RECV0
MGTYRXN0_225	AU1	nF2_A_RECV0
MGTYTXP0_225	AU7	pF2_A_XMIT0
MGTYTXN0_225	AU6	nF2_A_XMIT0
MGTYRXP1_225	AT4	pF2_A_RECV1
MGTYRXN1_225	AT3	nF2_A_RECV1
MGTYTXP1_225	AT9	pF2_A_XMIT1
MGTYTXN1_225	AT8	nF2_A_XMIT1
MGTYRXP2_225	AR2	pF2_A_RECV2
MGTYRXN2_225	AR1	nF2_A_RECV2
MGTYTXP2_225	AR7	pF2_A_XMIT2
MGTYTXN2_225	AR6	nF2_A_XMIT2
MGTYRXP3_225	AP4	pF2_A_RECV3
MGTYRXN3_225	AP3	nF2_A_RECV3
MGTYTXP3_225	AP9	pF2_A_XMIT3
MGTYTXN3_225	AP8	nF2_A_XMIT3

FPGA_VU13P_A2577

pF1_D_RECV0	C1948 0.1 UF 0402		pF2_C_XMIT0
nF1_D_RECV0	C1949 0.1 UF 0402		nF2_C_XMIT0
pF1_D_RECV1	C1951 0.1 UF 0402		pF2_C_XMIT1
nF1_D_RECV1	C1953 0.1 UF 0402		nF2_C_XMIT1
pF1_D_RECV2	C1955 0.1 UF 0402		pF2_C_XMIT2
nF1_D_RECV2	C1957 0.1 UF 0402		nF2_C_XMIT2
pF1_D_RECV3	C1959 0.1 UF 0402		pF2_C_XMIT3
nF1_D_RECV3	C1961 0.1 UF 0402		nF2_C_XMIT3
pF1_D_XMIT0	0402 0.1 UF C1950		pF2_C_RECV0
nF1_D_XMIT0	0402 0.1 UF C1952		nF2_C_RECV0
pF1_D_XMIT1	0402 0.1 UF C1954		pF2_C_RECV1
nF1_D_XMIT1	0402 0.1 UF C1956		nF2_C_RECV1
pF1_D_XMIT2	0402 0.1 UF C1958		pF2_C_RECV2
nF1_D_XMIT2	0402 0.1 UF C1960		nF2_C_RECV2
pF1_D_XMIT3	0402 0.1 UF C1962		pF2_C_RECV3
nF1_D_XMIT3	0402 0.1 UF C1963		nF2_C_RECV3
pF1_E_RECV0	C1964 0.1 UF 0402		pF2_B_XMIT0
nF1_E_RECV0	C1965 0.1 UF 0402		nF2_B_XMIT0
pF1_E_RECV1	C1967 0.1 UF 0402		pF2_B_XMIT1
nF1_E_RECV1	C1969 0.1 UF 0402		nF2_B_XMIT1
pF1_E_RECV2	C1971 0.1 UF 0402		pF2_B_XMIT2
nF1_E_RECV2	C1973 0.1 UF 0402		nF2_B_XMIT2
pF1_E_RECV3	C1975 0.1 UF 0402		pF2_B_XMIT3
nF1_E_RECV3	C1977 0.1 UF 0402		nF2_B_XMIT3
pF1_E_XMIT0	0402 0.1 UF C1966		pF2_B_RECV0
nF1_E_XMIT0	0402 0.1 UF C1968		nF2_B_RECV0
pF1_E_XMIT1	0402 0.1 UF C1970		pF2_B_RECV1
nF1_E_XMIT1	0402 0.1 UF C1972		nF2_B_RECV1
pF1_E_XMIT2	0402 0.1 UF C1974		pF2_B_RECV2
nF1_E_XMIT2	0402 0.1 UF C1976		nF2_B_RECV2
pF1_E_XMIT3	0402 0.1 UF C1978		pF2_B_RECV3
nF1_E_XMIT3	0402 0.1 UF C1979		nF2_B_RECV3
pF1_F_RECV0	C1980 0.1 UF 0402		pF2_A_XMIT0
nF1_F_RECV0	C1981 0.1 UF 0402		nF2_A_XMIT0
pF1_F_RECV1	C1983 0.1 UF 0402		pF2_A_XMIT1
nF1_F_RECV1	C1985 0.1 UF 0402		nF2_A_XMIT1
pF1_F_RECV2	C1987 0.1 UF 0402		pF2_A_XMIT2
nF1_F_RECV2	C1989 0.1 UF 0402		nF2_A_XMIT2
pF1_F_RECV3	C1991 0.1 UF 0402		pF2_A_XMIT3
nF1_F_RECV3	C1993 0.1 UF 0402		nF2_A_XMIT3
pF1_F_XMIT0	0402 0.1 UF C1982		pF2_A_RECV0
nF1_F_XMIT0	0402 0.1 UF C1984		nF2_A_RECV0
pF1_F_XMIT1	0402 0.1 UF C1986		pF2_A_RECV1
nF1_F_XMIT1	0402 0.1 UF C1988		nF2_A_RECV1
pF1_F_XMIT2	0402 0.1 UF C1990		pF2_A_RECV2
nF1_F_XMIT2	0402 0.1 UF C1992		nF2_A_RECV2
pF1_F_XMIT3	0402 0.1 UF C1994		pF2_A_RECV3
nF1_F_XMIT3	0402 0.1 UF C1995		nF2_A_RECV3

APOLLO CM W/ DUAL A2577, MK1	
Title	9.04: F1 QUADS D, E, F TO F2 QUADS C, B, A
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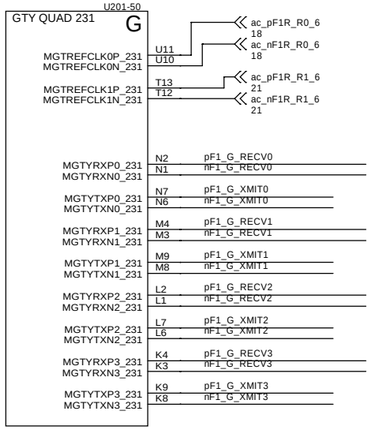
9.05: F1 QUAD G TO F2 QUAD P

FPGA#1

U201-50

GTY QUAD 231 G



FPGA_VU13P_A2577

UNUSED CLOCK INPUTS ARE LEFT OPEN.

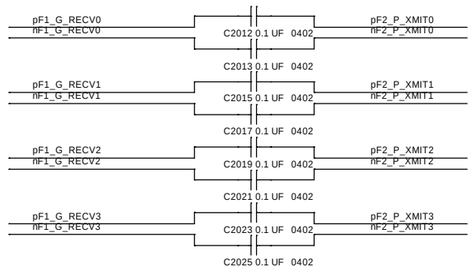
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

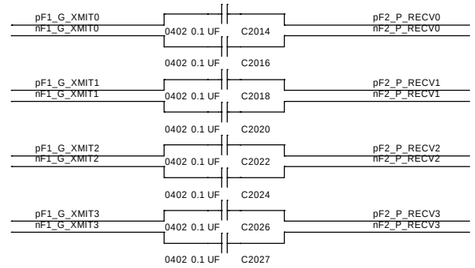
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

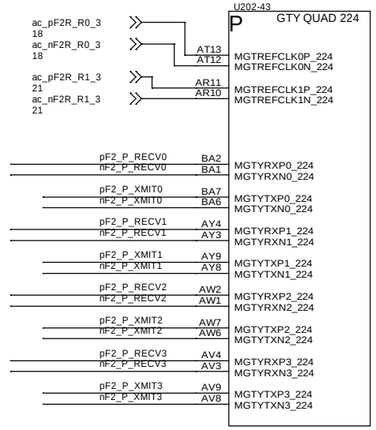




FPGA#2

U202-43

GTY QUAD 224 P



FPGA_VU13P_A2577

APOLLO CM W/ DUAL A2577, MK1

Title: 9.05: F1 QUAD G TO F2 QUAD P

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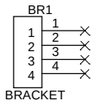
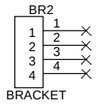
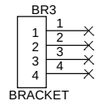
THESE SHAPES DEFINE MECHANICAL OBJECTS
THAT SHOULD BE IN THE BILL OF MATERIALS.

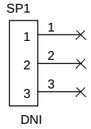


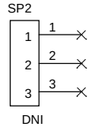




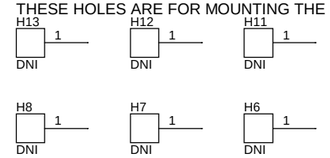
BRACKETS FOR SUPPORTING
A SUB-FRONT PANEL

THESE SHAPES DEFINE HOLES AND KEEPOUT
AREAS FOR THE SPLICE PLATES.

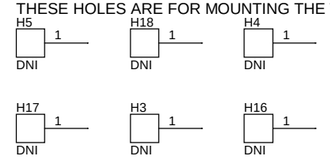




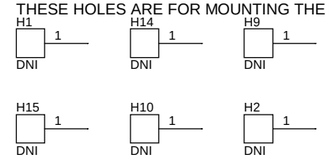
THESE HOLES ARE FOR MOUNTING THE FIREFLY HEATSINKS



THESE HOLES ARE FOR MOUNTING THE TOP COVER



THESE HOLES ARE FOR MOUNTING THE BOTTOM COVER



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