

Instructions for using Clock Builder PRO with the Apollo CMv2

This is initially written for an SI5341. Differences for an SI5395 will be accounted for later.

Step 1 – For the device ID register contents, enter the 8-character string consisting of the synthesizer name [one of R0A, R0B, R1A, R1B, R1C], followed by a lowercase “v”, then a 4 digit revision number [in the example “R0Av0001”]. This string will appear later in file names.

In the design notes block, enter a line like the one shown below. It should contain the schematic drawing number and revision [in the example “6089-119-RevA”] and the schematic sheet number where the associated device can be found [in the example :schematic sheet 2.06”].

Press “Next”

CB New Si5341 Project - ClockBuilder Pro

ClockBuilder Pro v4.1 **SKYWORKS**

Step 1 of 10 - Design ID & Notes ▼ Configuring Si5341ABCD Rev D

Design ID
The device has 8 registers, DESIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuration/revision identifier.

Design ID: (optional; max 8 characters)
The string you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN_ID7.

Padding Mode: ☒ **NULL Padded**
If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padded with 0x00 bytes (aka NULL character).
☐ **Space Padded**
If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padded with 0x20 bytes (space character).

Design Notes
Enter anything you want here. The text is stored in your project file and included in design reports and custom part number datasheet addendums. While the text is word wrapped in reports, you can use newlines to start a new paragraph.

Synthesizer for Apollo CMv2, 6089-119-RevA, schematic sheet 2.06

< Back Next > Finish Cancel

Step 2 – The SI5341 only comes with Device Revision “D”.

Press “Next”.

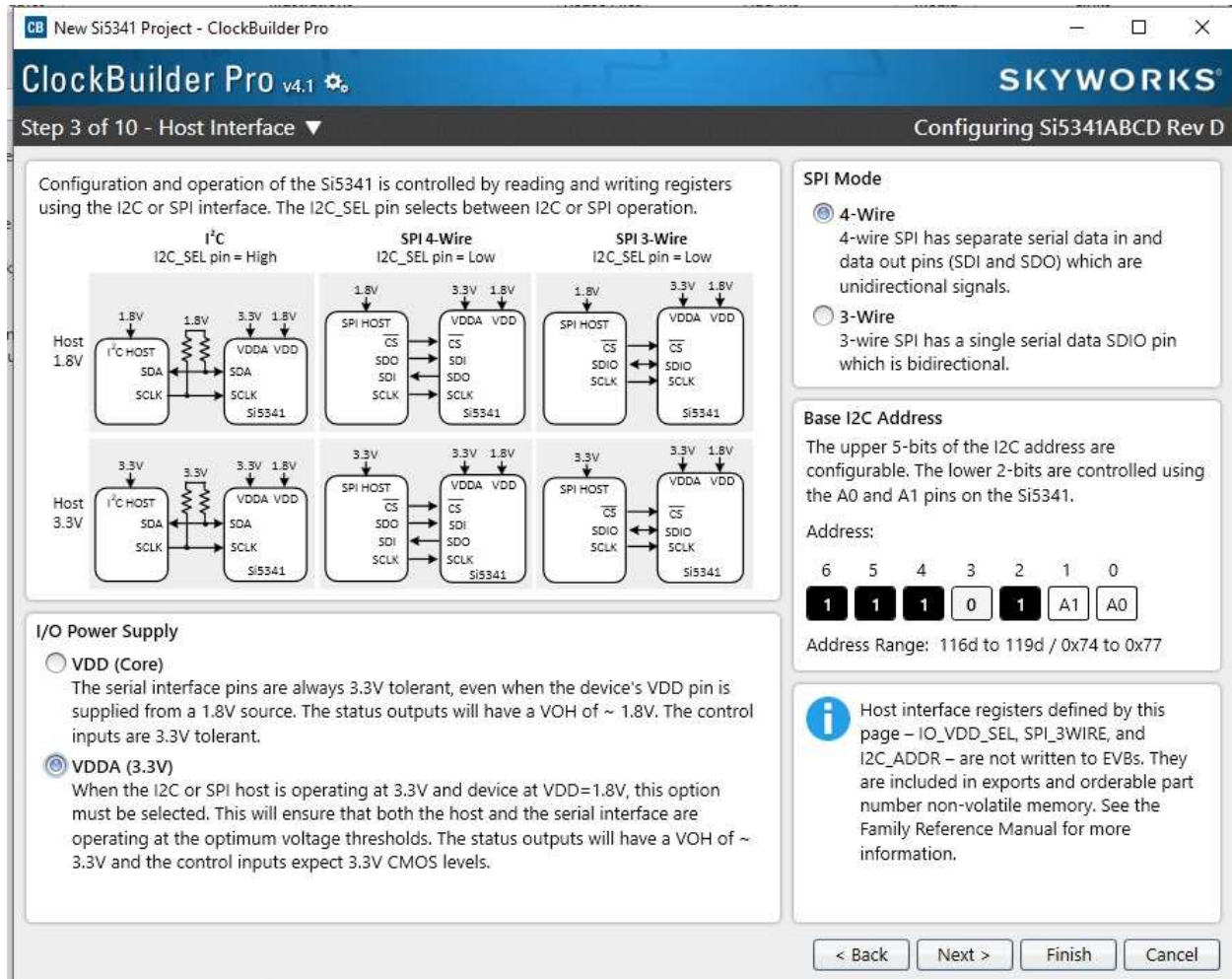
The screenshot shows the ClockBuilder Pro v4.1.1 software interface. The title bar indicates 'New Si5341 Project - ClockBuilder Pro'. The main header displays 'ClockBuilder Pro v4.1.1' and the 'SKYWORKS' logo. The progress bar shows 'Step 2 of 10 - Device Revision'. The right side of the header indicates 'Configuring Si5341ABCD Rev D'.

On the left, the 'Device Revision' is set to 'D' in a dropdown menu. The right panel contains the following text and list:

Select the device revision for your Si5341 design. This revision will be used in the following scenarios:

- Create an Orderable Part Number (OPN) for the selected device revision
- Export device configuration registers to program a device in-system, where the in-system DUT has the selected device revision
- Change the configuration of an Evaluation Board
- Use the field programmer to update the configuration of a Si5341 that has the selected device version

At the bottom right, there are four buttons: '< Back', 'Next >', 'Finish', and 'Cancel'.



Step 4 – Generally chose one input for a design and leave all other inputs unused, even if there is a signal that is potentially available. Live switching is not usually needed. For instance, all five synthesizers have a 48 MHz crystal connected to the XA/XB pins. The R0A synthesizer also has a 322.265625 oscillator connected to the IN0 pins, and an output from the R0B synthesizer connected to the IN1 pins. This design will just use the 322.265625 MHz oscillator. In the “Mode” column for IN0 select “Enabled” from the popup window. Set the frequency to 322.265625 MHz. Be sure to indicate “MHz” in the value.

Four of the five synthesizers have wiring in place to support “Zero Delay Mode”. If it is available, and the application warrants using it, check the “Enable Zero Delay Mode” box and select the output that is connected for ZDM. ZDM is not available for the crystal input. For synthesizer R0A, it is not necessary when using the oscillator on IN_0, but may be desirable when using the R0B output on IN_1.

If you wanted to use the crystal instead, then select “Crystal Mode” for the XA/XB input and disable the other inputs. Disable ZDM as well, otherwise an error will be indicated.

Press “Next”.

Input Clock Modes and Frequencies

Input	Mode	Frequency
XA/XB	Unused	N/A
IN0	Enabled	322.265625 MHz
IN1	Unused	N/A
IN2	Unused	N/A

Zero Delay Mode (ZDM)

☒ Enable Zero Delay Mode

External Feedback Output: OUT9

Important Notes About Zero Delay Mode (ZDM):

- ZDM is optional. It is intended for applications that require a controlled minimum delay between the selected input and outputs.
- For optimal ZDM operation and performance, tie the FB_IN clock pins to the OUT9 output clock pins.
- Although any one of the output clocks can be fed back to the FB_IN pins, using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay (typically 100 ps). OUT9 is strongly recommended by Skyworks.

Block Diagram:

The diagram illustrates the clock input options and the Zero Delay Mode (ZDM) configuration. It shows the IN_SEL[1:0] input, the IN0, IN1, and IN2 inputs, and the XA/XB input options. The XA/XB input options include the OSC (Oscillator) and the External Reference Clock Input Mode. The ZDM section shows the FB_IN input and the P_fb divider. The output is labeled OUT9.

Frequency Plan Valid **Design OK** **Typical Pd 660 mW, Tj 37 °C**

Navigation: < Back Next > Finish Cancel

Step 5 – For this design, only one input clock is defined and input clock selection is not used.

If input clock selection is needed, the board is designed to support using the “IN_SEL[1:0]” pins. These pins are driven from I2C registers that appear on schematic sheet 4.03. These registers will power-up with all zeroes on the outputs, so the power-up selection will be the 48 MHz crystal (even if it not enabled).

The input clock selection can also be done from a register.

Press “Next”.

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Step 5 of 10 - Input Clock Selection ▼ Configuring Si5341ABCD Rev D

Because you have only defined one input clock, input clock selection does not need to be configured.

Manual Clock Select Mode

☒ **Register**
Use the input select register via serial interface to select the input clock.
Power on Default:

☐ **Pins**
Use the IN_SEL[1:0] pins to select the input clock.

Input clock selection can be made manually using the IN_SEL[1:0] pins or with an input select register using the serial interface. A device register selects input selection as pin selectable or register selectable. When the zero delay mode is enabled, IN3 becomes the feedback input and is not available for selection as a clock input.

Frequency Plan Valid Design OK Typical Pd 660 mW, Tj 37 °C

< Back Next > Finish Cancel

Step 6 – Enable the outputs that are both connected and will be used by selecting “Enabled (Powered-up with Output Enabled)” in the “Mode” column.

For boards with only FPGA#1 populated, outputs to FPGA#2 should be left disabled. This will both save power and minimize electrical noise. The 100 ohm terminators are internal to the FPGA and are not present if the FPGA is not installed, so the signal will reflect and ring on the PCB traces.

For boards with only FPGA#1 populated and no jumper board in the FPGA#2 site, outputs to the right side of FPGA#1 should be left disabled. This will save power. [Verify that this is true for TCDS signals.]

Some outputs connect to other synthesizers and will only be used under special circumstances. Leave them disabled until needed. This will save power.

The “Disabled State” for each output can be left at “Stop Low”.

The “Format” for each output should be set to “LVDS 1.8 V”.

Enter the desired frequency for each enabled output. Be sure to indicate “MHz” in the value.

If ZDM is being used, pick the “N0” manual assignment in the “N Divider/DCO/ZDM” column.

Press “Next”.

Output	Mode	Disabled State	Format	Frequency	N Divider / DCO / ZDM
OUT0	Unused	N/A	N/A	N/A	N/A
OUT1	Unused	N/A	N/A	N/A	N/A
OUT2	Enabled	Stop Low	LVDS 1.8 V	322.2656... MHz [322 + 17/64 MHz]	N0...
OUT3	Enabled	Stop Low	LVDS 1.8 V	322.2656... MHz [322 + 17/64 MHz]	N0...
OUT4	Unused	N/A	N/A	N/A	N/A
OUT5	Unused	N/A	N/A	N/A	N/A
OUT6	Unused	N/A	N/A	N/A	N/A
OUT7	Unused	N/A	N/A	N/A	N/A
OUT8	Unused	N/A	N/A	N/A	N/A
OUT9	ZDM	Stop Low	LVDS 1.8 V	ZDM (322.265625 MHz)	N0...

Frequency Plan Valid Design OK Typical Pd 660 mW, Tj 37 °C

< Back Next > Finish Cancel

Step 7 – This project does not use “DCO Mode”

Press “Next”.

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Step 7 of 10 - DCO (Digitally Controlled Oscillator) ▼

Configuring Si5341ABCD Rev D

Mode: ☒ Frequency Increment/Decrement via FINC/FDEC Register & Pin Control
☐ Write to Divider Registers Directly

Nx	DCO Enable	Desired Step Size	Range ?	Initial Step Size	Output	Frequency	Initial Step Size
N0	<input type="checkbox"/>	1 ppm	± 200 ppm	---	OUT2 OUT3 OUT9	322.2656... MHz 322.2656... MHz 322.2656... MHz	---
N1	<input type="checkbox"/>	1 ppm	± 200 ppm			No Outputs	
N2	<input type="checkbox"/>	1 ppm	± 200 ppm			No Outputs	
N3	<input type="checkbox"/>	1 ppm	± 200 ppm			No Outputs	
N4	<input type="checkbox"/>	1 ppm	± 200 ppm			No Outputs	

DCO Report ...

Overview

DCO mode is designed for small , glitchless frequency changes. A [short introductory video](#) is available. The [Family Reference Manual](#) and [AN959](#) has more detailed technical information.

FINC/FDEC Mode

Output frequencies are adjustable in pre-defined steps defined by frequency step words (FSW). The frequency adjustments are initiated using the frequency increment (FINC) or decrement (FDEC) device registers or pins.

$$F_{out} = \frac{F_{vco} * N_{x_DEN}}{(N_{x_NUM} \pm n * N_{x_FSTEPW}) * R_y}$$

The N_FSTEP_MSK register controls whether all or a sub-set of Nx dividers are incremented or decremented. Any DCO enabled Nx divider will be included in FINC/FDEC by CBPro. Your host can change this in-system via I2C/SPI.

Register Direct Write Mode

In this mode, the host directly writes the Nx_NUM register value to set a new output frequency for all output(s) on an Nx divider.

$$F_{out} = \frac{F_{vco} * N_{x_DEN}}{N_{x_NUM} * R_y}$$

The host writes the Nx_UPDATE register to cause the change to take effect.

Frequency Plan Valid

Design OK

Typical Pd 660 mW, Tj 37 °C

< Back

Next >

Finish

Cancel

Step 8 – Unless otherwise known, the frequency planner should be instructed to maximize the number of low jitter outputs.

Press “Next”.

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Step 8 of 10 - Configure Frequency Planner ▼ Configuring Si5341ABCD Rev D

☒ **Maximize the number of low jitter outputs**
CBPro will select the frequency plan with the most number of outputs on an integer N divider.

☐ **Select one output as lowest jitter**
CBPro will ensure that the selected output is on an integer N divider. Where possible, other outputs that are even common multiple related will be placed on the same divider, within the bounds of any manual N divider assignment you have configured.

Output:

The ClockBuilder Pro frequency planner tries a variety of possible VCO frequencies and divider values to compute your frequency plan. You can modify the criteria used to select the best frequency plan.

Other factors may still be weighted higher than the options to the left depending on device configuration and revision.

These settings will have no effect when using the CBProFOTF1 Command Line Tool to do Frequency-On-The-Fly (FOTF). The FOTF tool will optimize for lowest jitter across all plans.

Frequency Plan Valid Design OK Typical Pd 660 mW, Tj 37 °C

< Back **Next >** Finish Cancel

Step 9 – Unless otherwise known, the LOS (Loss Of Signal) values should be left as is.

Press “Next”.

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ClockBuilder Pro v4.1 ⚙

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Step 9 of 10 - LOS (Loss of Signal) ▼

Configuring Si5341ABCD Rev D

LOS Detect

Thresholds for assert and de-assert of LOS are specified in number of corresponding clock cycles at the input to the phase detector, which is the input clock divided by it's P divider. This is translated to a time based on the frequency of the corresponding phase detector input clock.

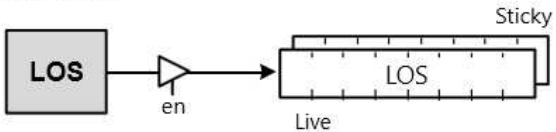
Input Clock	Assert Threshold ?	De-Assert Threshold ?	Validation Time ?
IN0	4,000	4,000	100 ms
IN1	N/A	N/A	N/A
IN2	N/A	N/A	N/A
FB_IN	4,000	4,000	100 ms

XA/XB Threshold and validation times are not configurable for LOS on XA/XB

The loss of signal monitor measures the period of each phase detector input clock cycle to detect phase irregularities or missing clock edges.

Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors.

The LOS status for each of the monitors is accessible by reading a status register.



Frequency Plan Valid

Design OK

Typical Pd 660 mW, Tj 37 °C

< Back

Next >

Finish

Cancel

Step 10 – The interrupt output pin is connected to an I2C registers that appear on schematic sheet 4.03. It will not actually generate an interrupt. It will be available for polling by the MCU.

Use the default settings unless something different is desired.

Press “Next”.

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ClockBuilder Pro v4.1

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Step 10 of 10 - Interrupt Pin ▼

Configuring Si5341ABCD Rev D

INTR Config - Define What Alert Conditions Should Assert $\overline{\text{INTR}}$

LOSREF_FLG ?

LOSXAXB_FLG ☒ ?

(IN0) LOS_FLG[0] ☒ ?

(IN1) LOS_FLG[1] ☐ ?

(IN2) LOS_FLG[2] ☐ ?

(FB_IN) LOS_FLG[3] ☒ ?

LOS

LOL_FLG ?

SMBUS_TIMEOUT_FLG ?

SYSINCAL_FLG ?

$\overline{\text{INTR}}$

The interrupt pin (INTR) indicates a change in state in a configurable group of status registers. Most status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTR pin is reset by clearing the sticky status registers.

When you check a status condition in the editor, you are indicating that you want that signal to contribute to INTR. Note that there are some conditions that will always contribute to INTR: loss of XA/XB signal and system calibration in progress. Mouse over the ? icons to learn more.

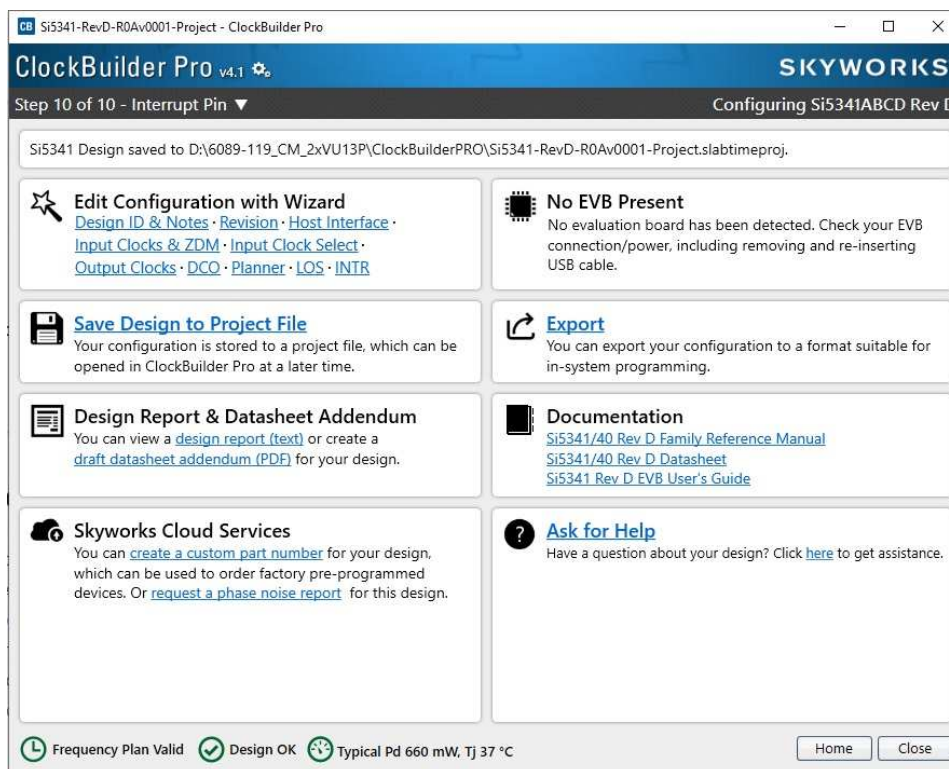
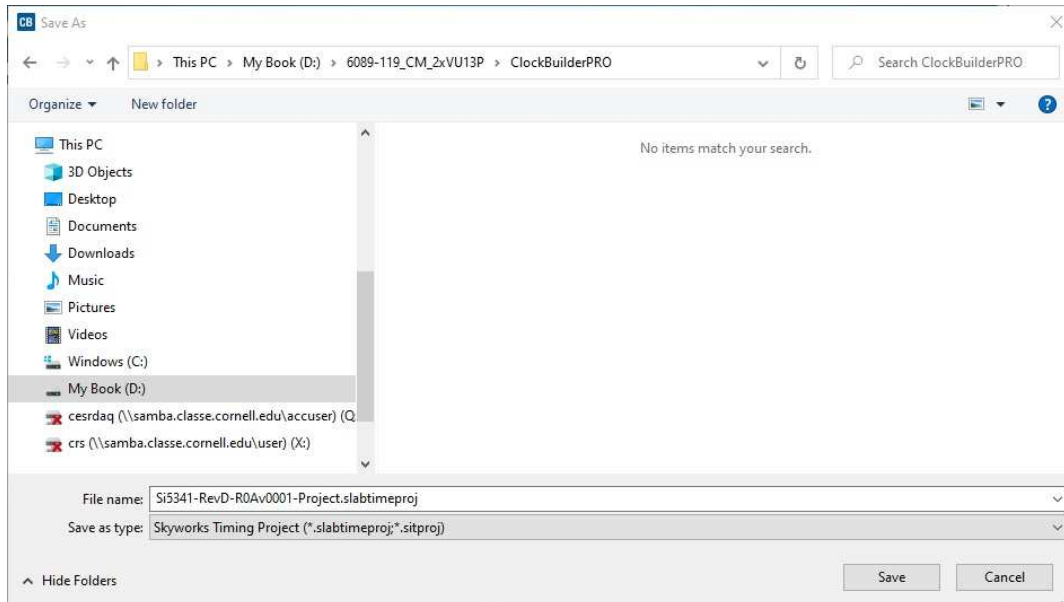
Frequency Plan Valid Design OK Typical Pd 660 mW, Tj 37 °C

< Back Next > Finish Cancel

Step 11 - The design dashboard will appear after step 10.

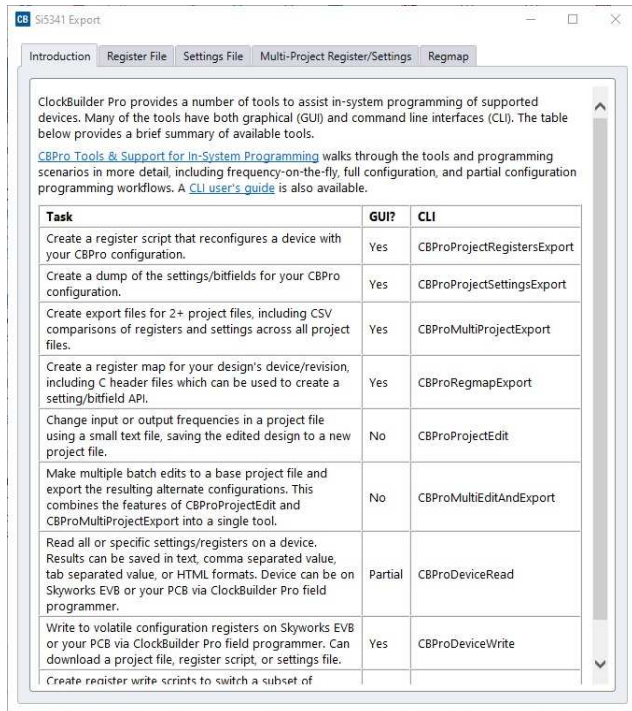
After making any changes, save the design to a project file. The name of the project file should reflect the “Design ID” entered in step 1.

Press “Save”. The design dashboard will reappear with a confirmation message.



Step 12 – Export a configuration file that can be downloaded to the hardware. Select “Export” on the dashboard.

In the popup “export” window, select the “Register File” tab.



Under the register file tab, select “C Code Header File”. Check the box for “Include pre- and post-...”. Press “Save to File”. It will be saved as a “.h” file.

