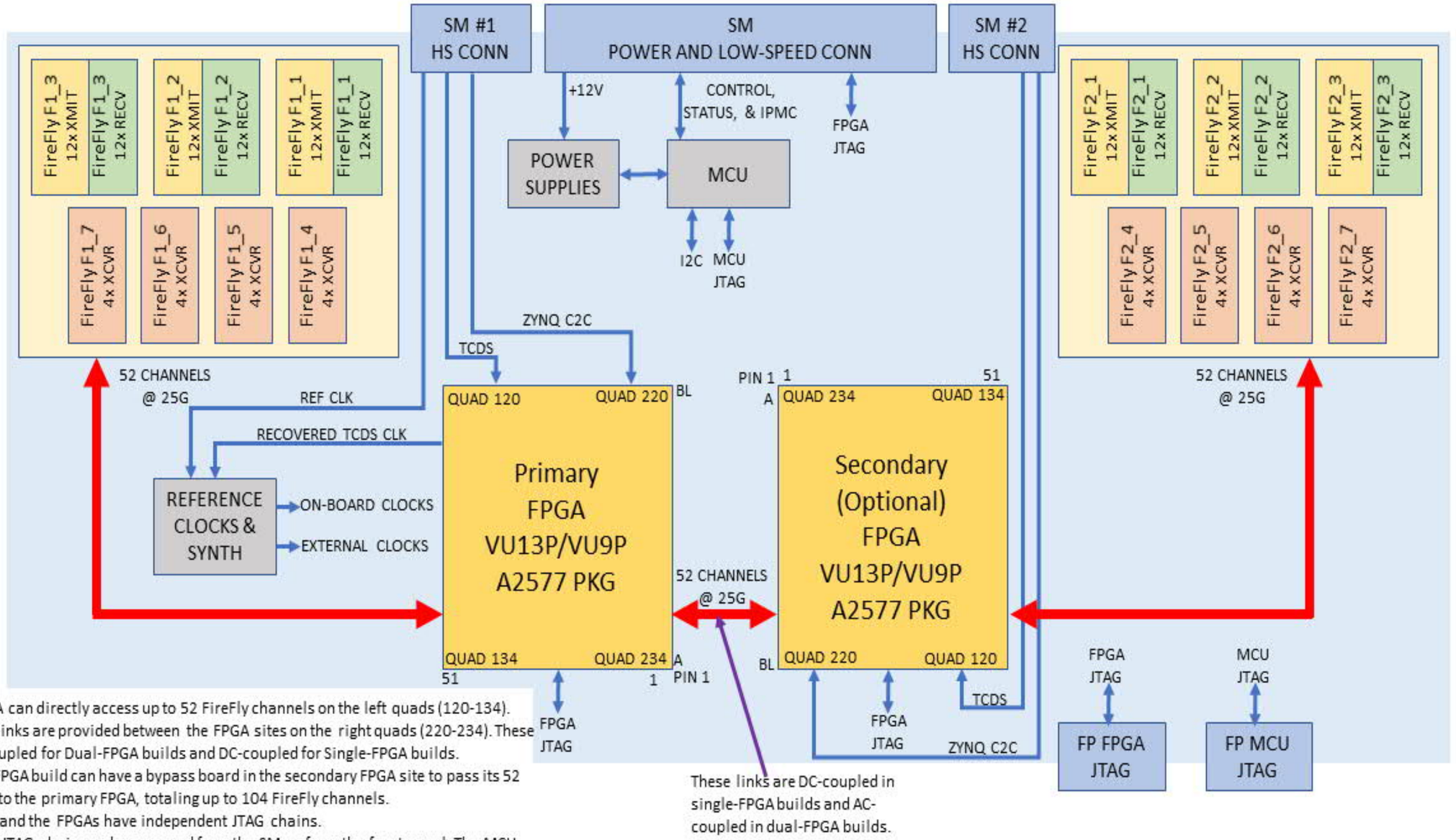
Apollo CM Dual A2577: Block Diagram



Notes:

- Each FPGA can directly access up to 52 FireFly channels on the left quads (120-134).
- Up to 52 links are provided between the FPGA sites on the right quads (220-234). These are AC-coupled for Dual-FPGA builds and DC-coupled for Single-FPGA builds.
- A single-FPGA build can have a bypass board in the secondary FPGA site to pass its 52 channels to the primary FPGA, totaling up to 104 FireFly channels.
- The MCU and the FPGAs have independent JTAG chains.
- The FPGA JTAG chain can be accessed from the SM or from the front panel. The MCU JTAG only has front panel access. The MCU code can be changed from an SM serial port.
- The recovered TCDS clock is only available from the primary FPGA.

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.02: BLOCK DIAGRAM		
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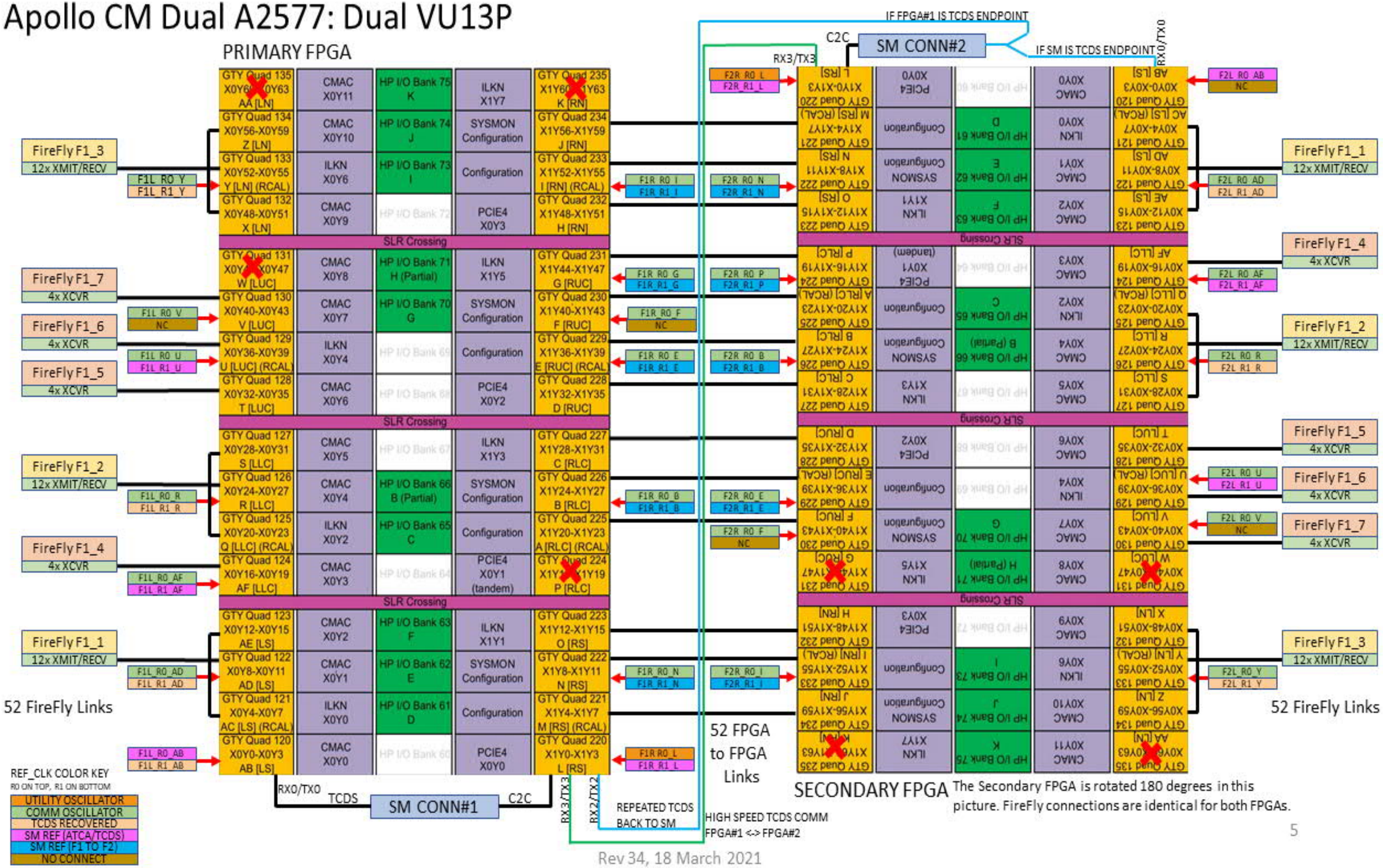
Apollo CM Dual A2577: Dual VU13P



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APOLLO CM W/ DUAL A2577, MK1				
Title: 1.03: DUAL VU13P				
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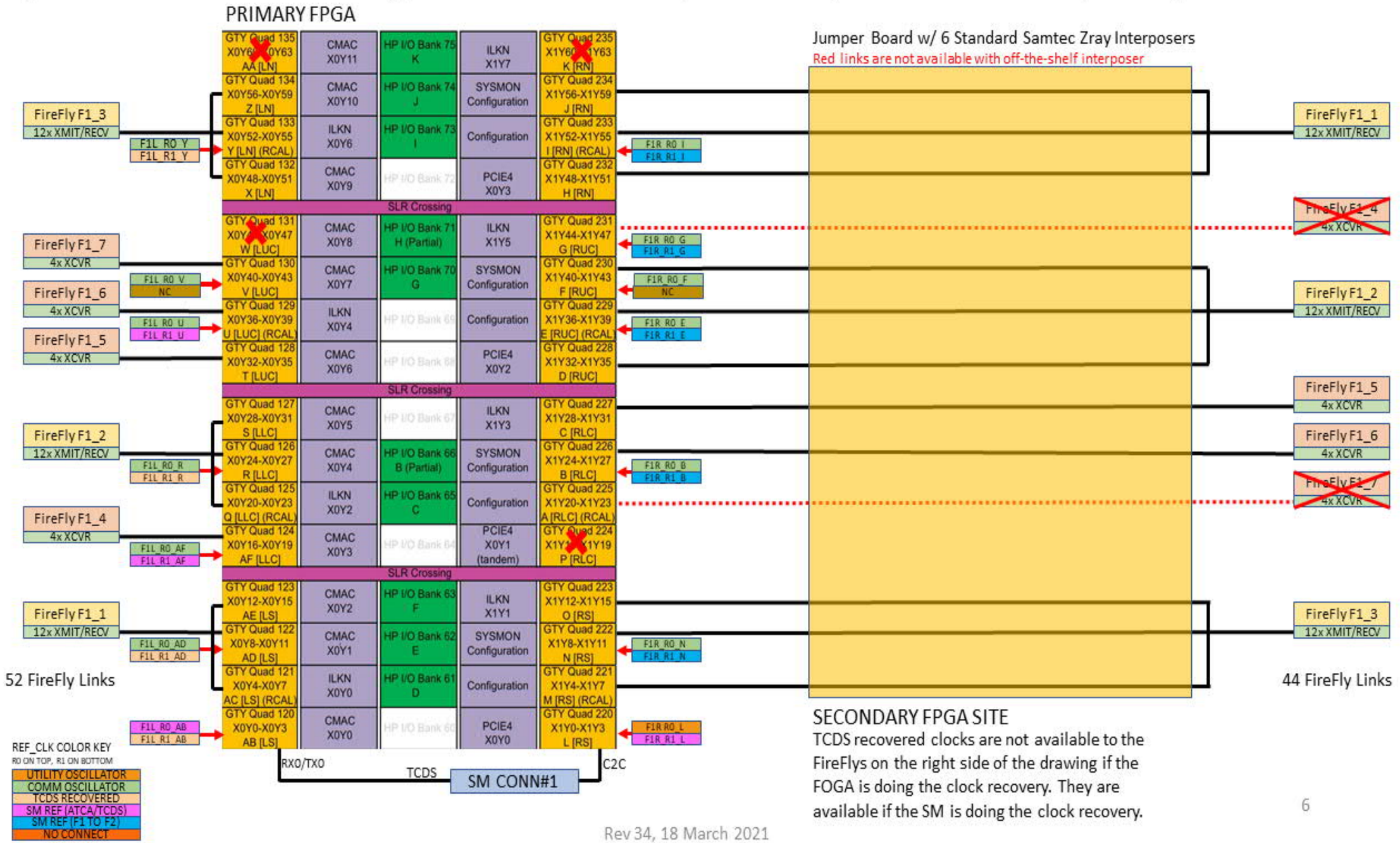
Apollo CM Dual A2577: Single VU13P with Jumper Board (off-the-self Interposers)



APOLLO CM W/ DUAL A2577, MK1		
Title: 1.04: SINGLE VU13P AND JUMPER		
Size	Document Number: 6089-119	Rev: A
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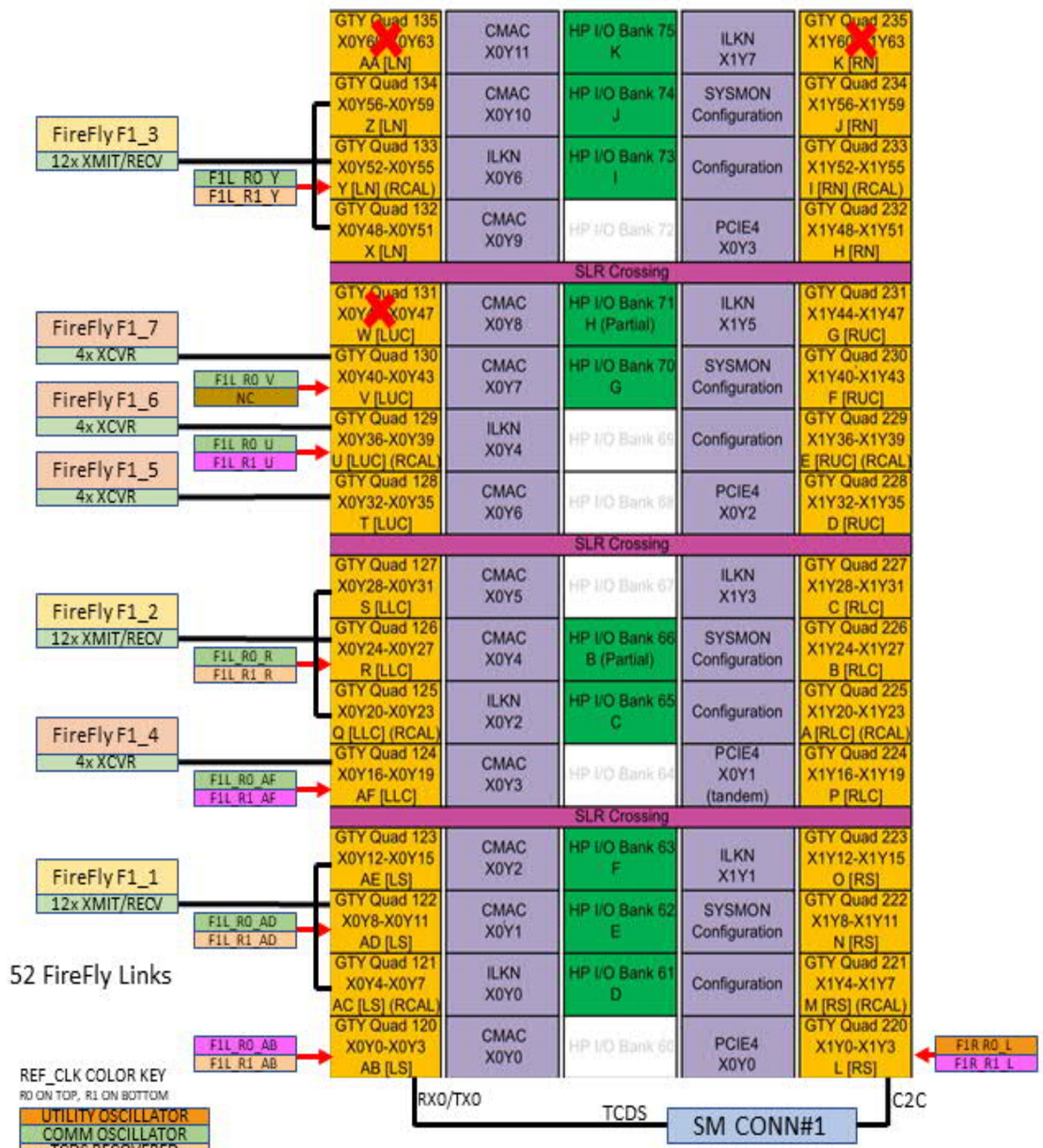
Apollo CM Dual A2577: Single VU13P



7

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APOLLO CM W/ DUAL A2577, MK1		
Title: 1.05: SINGLE VU13P		
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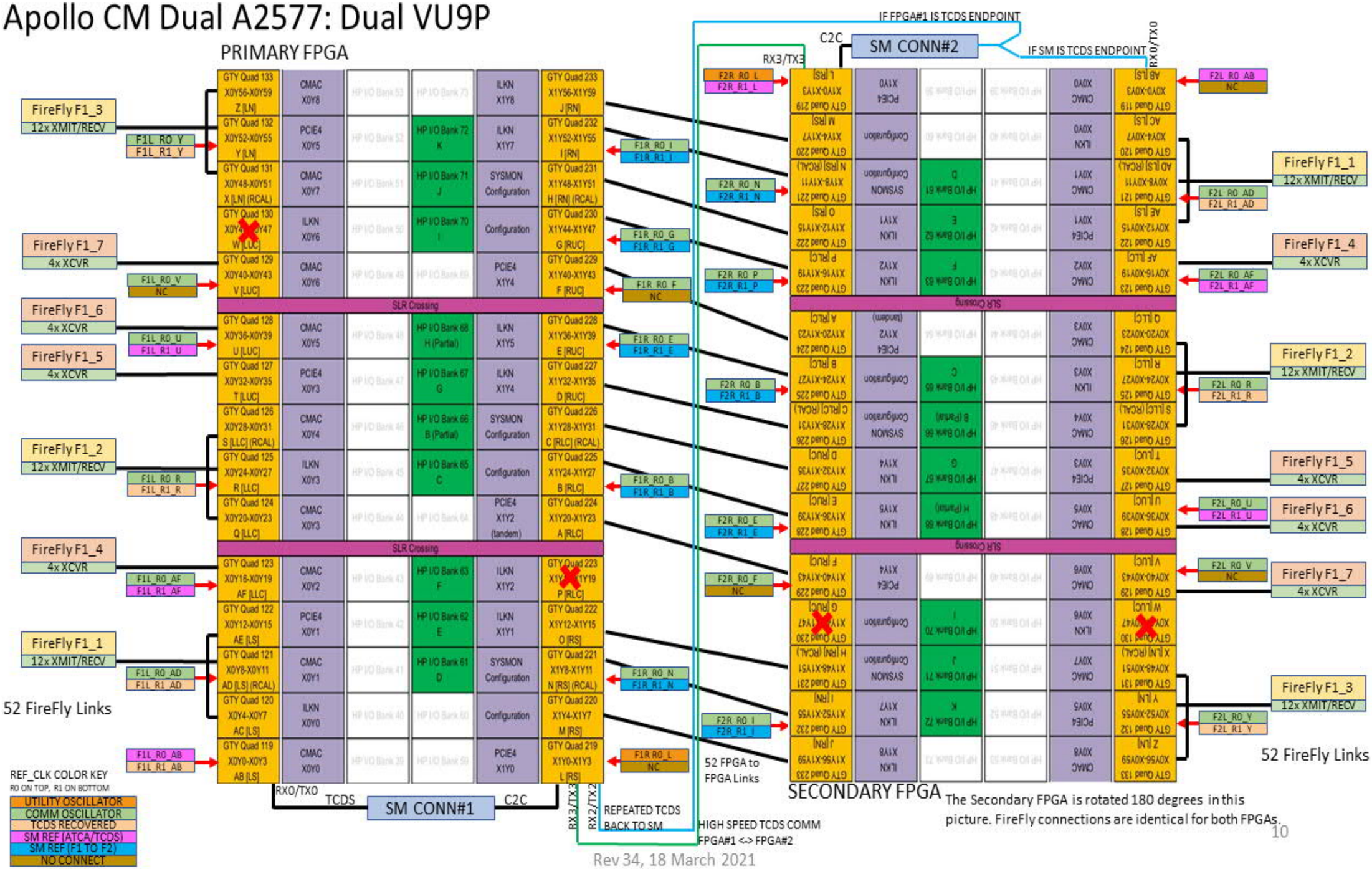
Apollo CM Dual A2577: Dual VU9P



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APOLLO CM W/ DUAL A2577, MK1			
Title: 1.06: DUAL VU9P			
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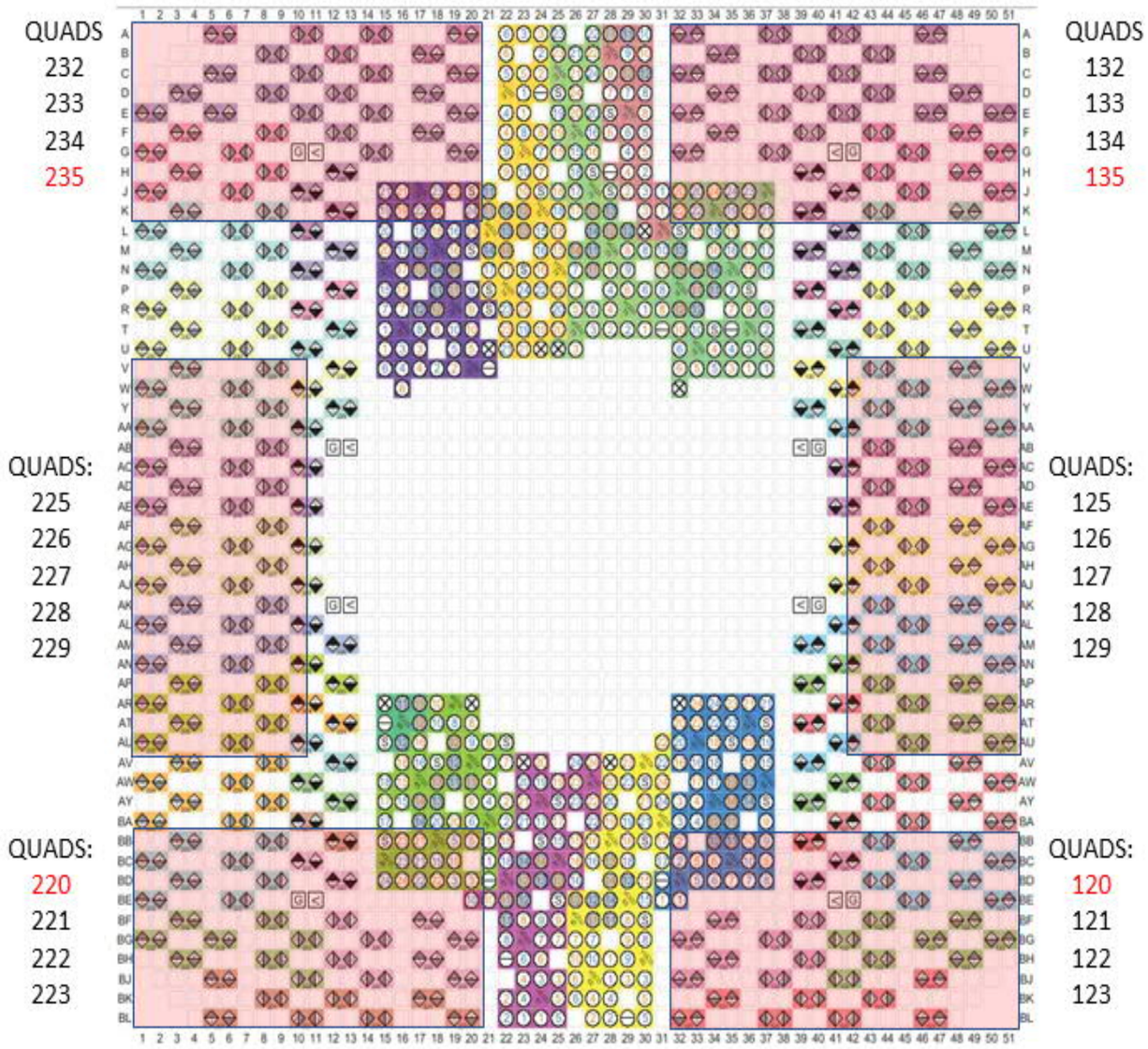
Apollo CM Dual A2577: 6 Interposer proof of principle

Diagram shows interposer location and available quads when 6 10x20 interposers are used to connect the jumper board.

Only quads numbered in black will be routed on the initial version. Quads numbered in red, while accessible to the interposers, will not be routed on the jumper board.



APOLLO CM W/ DUAL A2577, MK1		
Title: 1.07: SIX 10X20 INTERPOSERS		
Size	Document Number: 6089-119	Rev: A
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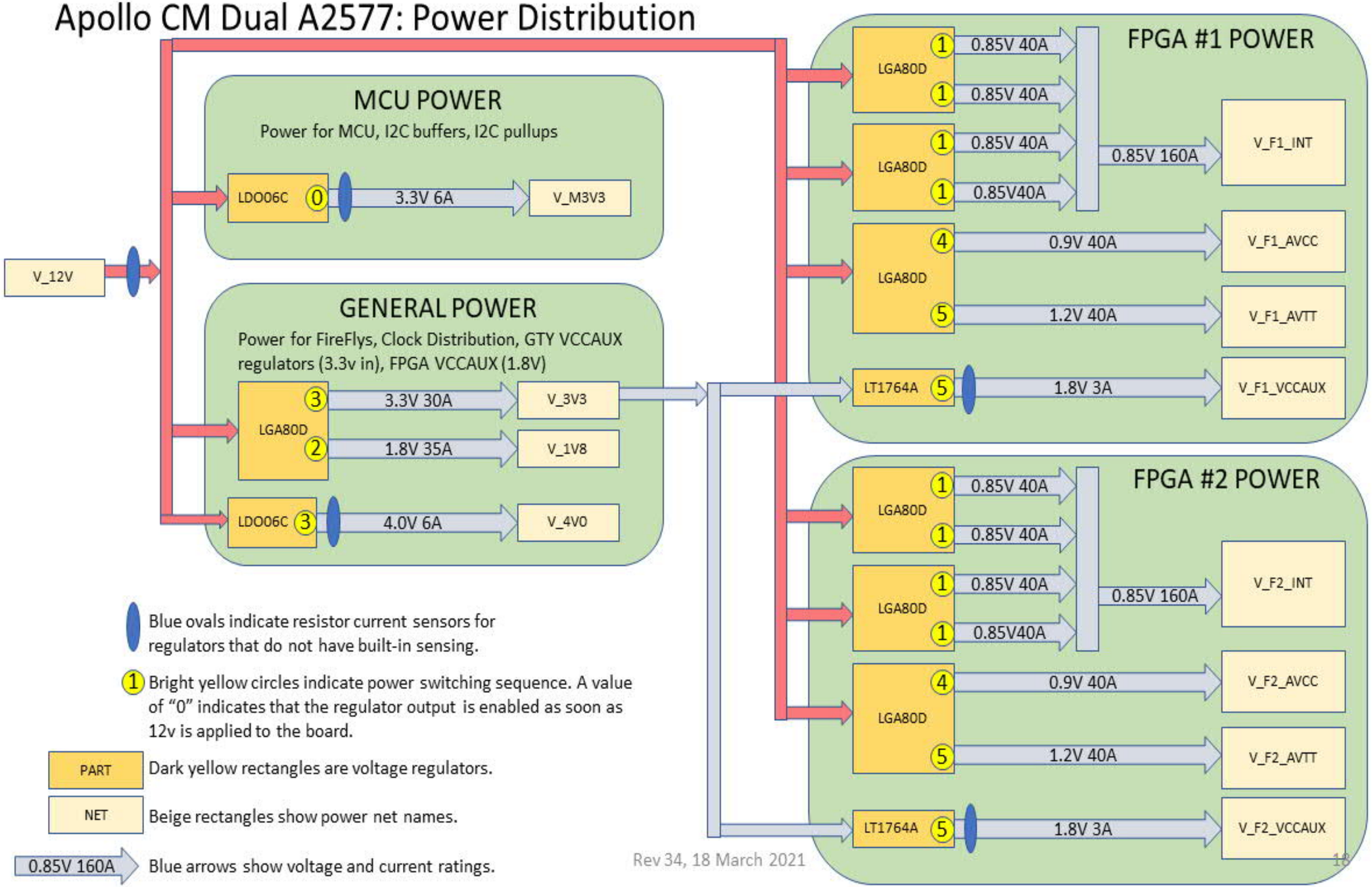
Apollo CM Dual A2577: Power Distribution



Blue ovals indicate resistor current sensors for regulators that do not have built-in sensing.

(1) Bright yellow circles indicate power switching sequence. A value of "0" indicates that the regulator output is enabled as soon as 12v is applied to the board.

PART — Dark yellow rectangles are voltage regulators.

NET — Beige rectangles show power net names.

0.85V 160A — Blue arrows show voltage and current ratings.

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APOLLO CM W/ DUAL A2577, MK1		
Title: 1.08: POWER		
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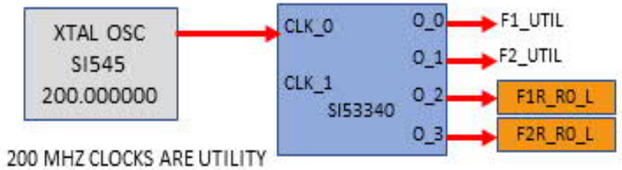
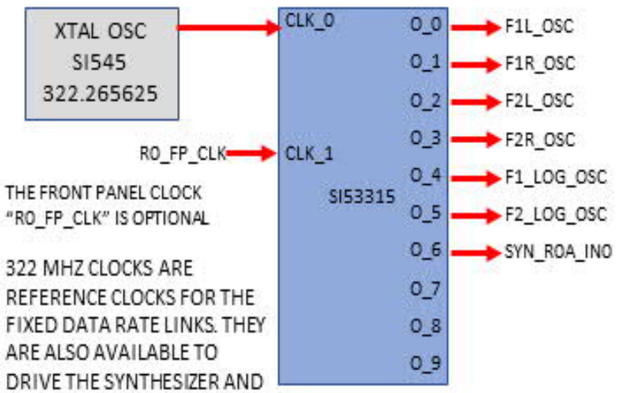
Apollo CM Dual A2577: On-Board Clock Sources

Oscillator Clocks / Reference Clock 0 (R0) Distribution

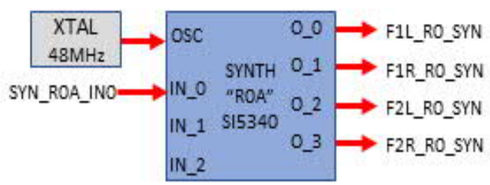


200 MHZ CLOCKS ARE UTILITY CLOCKS FOR THE FPGA LOGIC AND REFERENCE CLOCKS FOR THE SM C2C LINKS

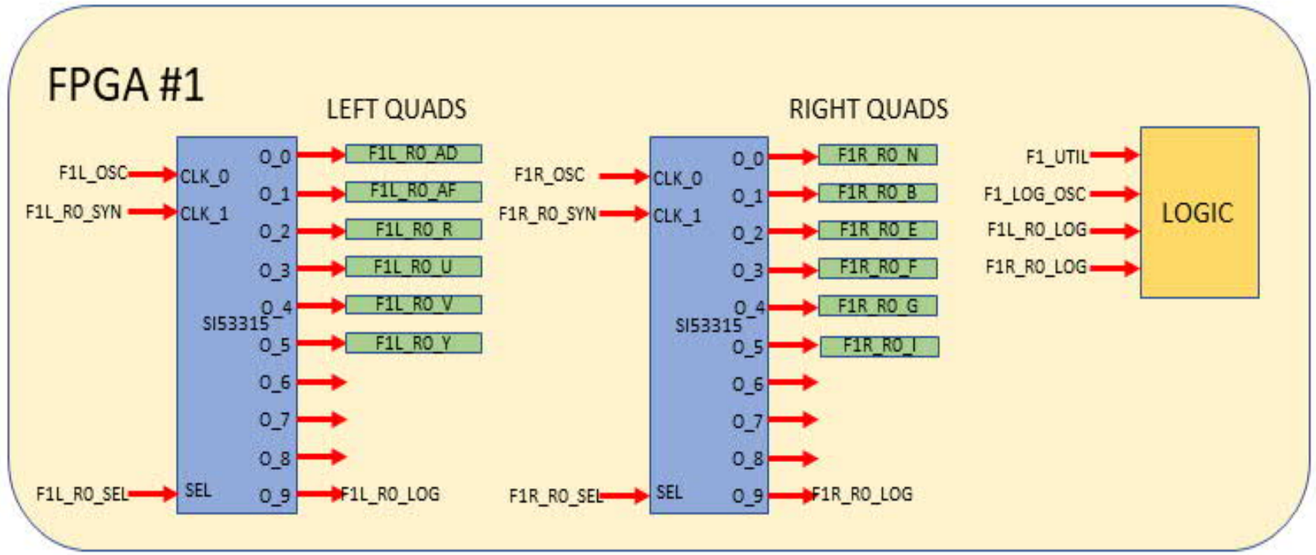


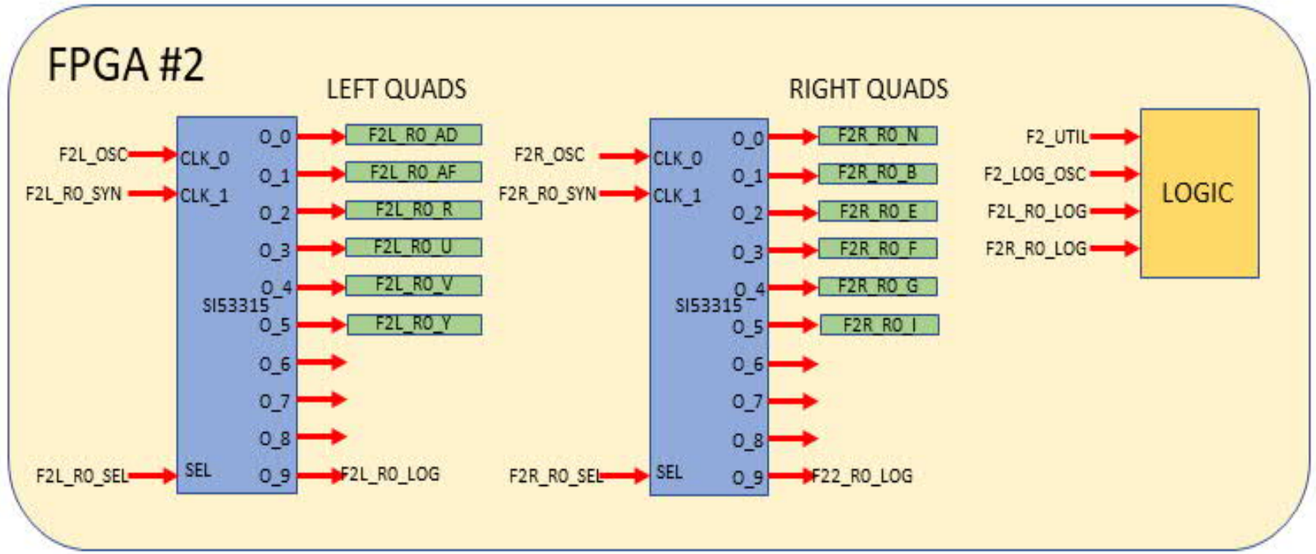
THE FRONT PANEL CLOCK "R0_FP_CLK" IS OPTIONAL

322 MHZ CLOCKS ARE REFERENCE CLOCKS FOR THE FIXED DATA RATE LINKS. THEY ARE ALSO AVAILABLE TO DRIVE THE SYNTHESIZER AND THE FPGA LOGIC.



THE REFERENCE CLOCK 0 SYNTHESIZER CAN BE DRIVEN BY A LOCAL OSCILLATOR OR THE FIXED DATA RATE OSCILLATOR (AND FRONT PANEL INPUT) FANOUT.





APOLLO CM W/ DUAL A2577, MK1		
Title: 1.09: ON-BOARD OSCILLATOR CLOCKS		
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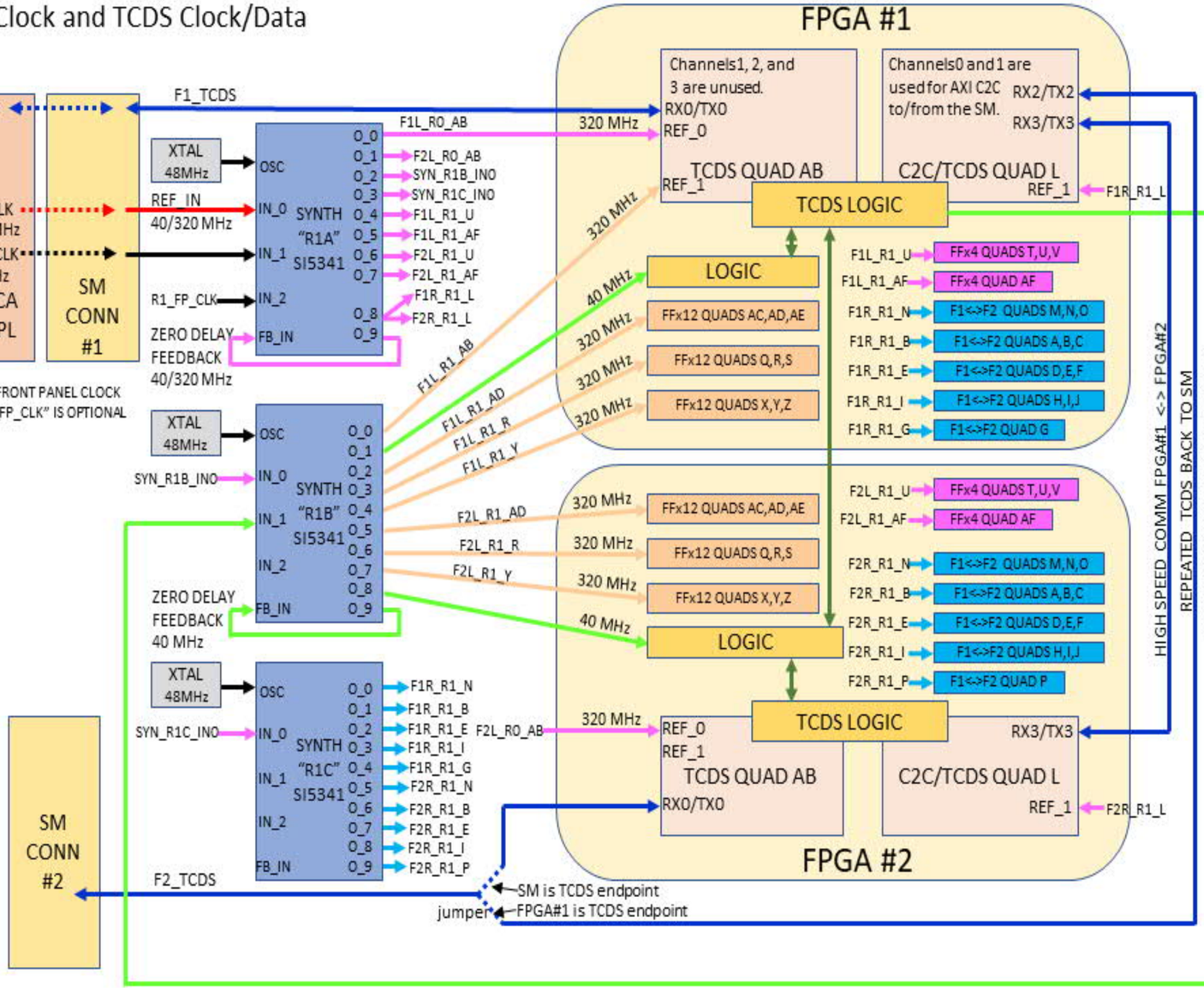
Apollo CM Dual A2577: External Clock Sources

ATCA Clock and TCDS Clock/Data



GBIT CLOCK/DATA COMBINED

LHC REFERENCE CLOCK

If the SM is not the TCDS endpoint, then this is a 320 MHz clock passed directly from the ATCA backplane. If the SM is the TCDS endpoint, then this is the 40 MHz clock recovered from the backplane TCDS signal. In either case, the frequency of this clock changes when the LHC is ramping.

320 MHz REF CLOCK

If the top synthesizer is using the clock on "IN_0", then these 320 MHz clocks all have zero phase offset relative to the incoming LHC REFERENCE CLOCK signal.

40 MHz TCDS RECOVERED CLOCK

This clock is recovered from the incoming TCDS signal. The TCDS LOGIC synchronizes this clock to the bunch crossing. It also adjusts the phase to compensate for distribution delay changes. It will always maintain a fixed phase relative to the bunch crossing. The frequency also varies during filling. This clock is made available to the logic in the FPGAs for synchronizing operations.

320 MHz TCDS RECOVERED CLOCK

These clocks drive the detector-facing FireFly devices, as well as the quad that sends the outgoing TCDS signal back to the SM. They track the TCDS RECOVERED CLOCK.

FPGA TO FPGA R1 CLOCK

These clocks drive the R1 reference for the FPGA quads that connect to the other FPGA. The frequency follows the 320 MHz REF CLOCK.

TTC/TTS DATA/CONTROL

These signals contain clocks/data/control extracted from the incoming TCDS signal (TTC) or destined for the outgoing TCDS signal (TTS). They are used within each FPGA, and can also pass from one FPGA to the other.

OTHER CLOCKS

These include the 40 MHz LHC clock and the outputs of various crystal oscillators. These can be used for testing or for adding flexibility to the synthesizer outputs.

GTY QUADS

FFx12 QUADS	12-lane FireFlys. For the IT-DTC, these will be detector facing.
FFx4 QUADS	4-lane FireFlys.
F1<->F2 QUADS	Connections between the two FPGAs. These will be FireFly links in the case of a single FPGA with jumpers at the secondary FPGA site.
TCDS QUAD	Dedicated for TCDS function.

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APOLLO CM W/ DUAL A2577, MK1		
Title: 1.10: EXTERNAL CLOCKS		
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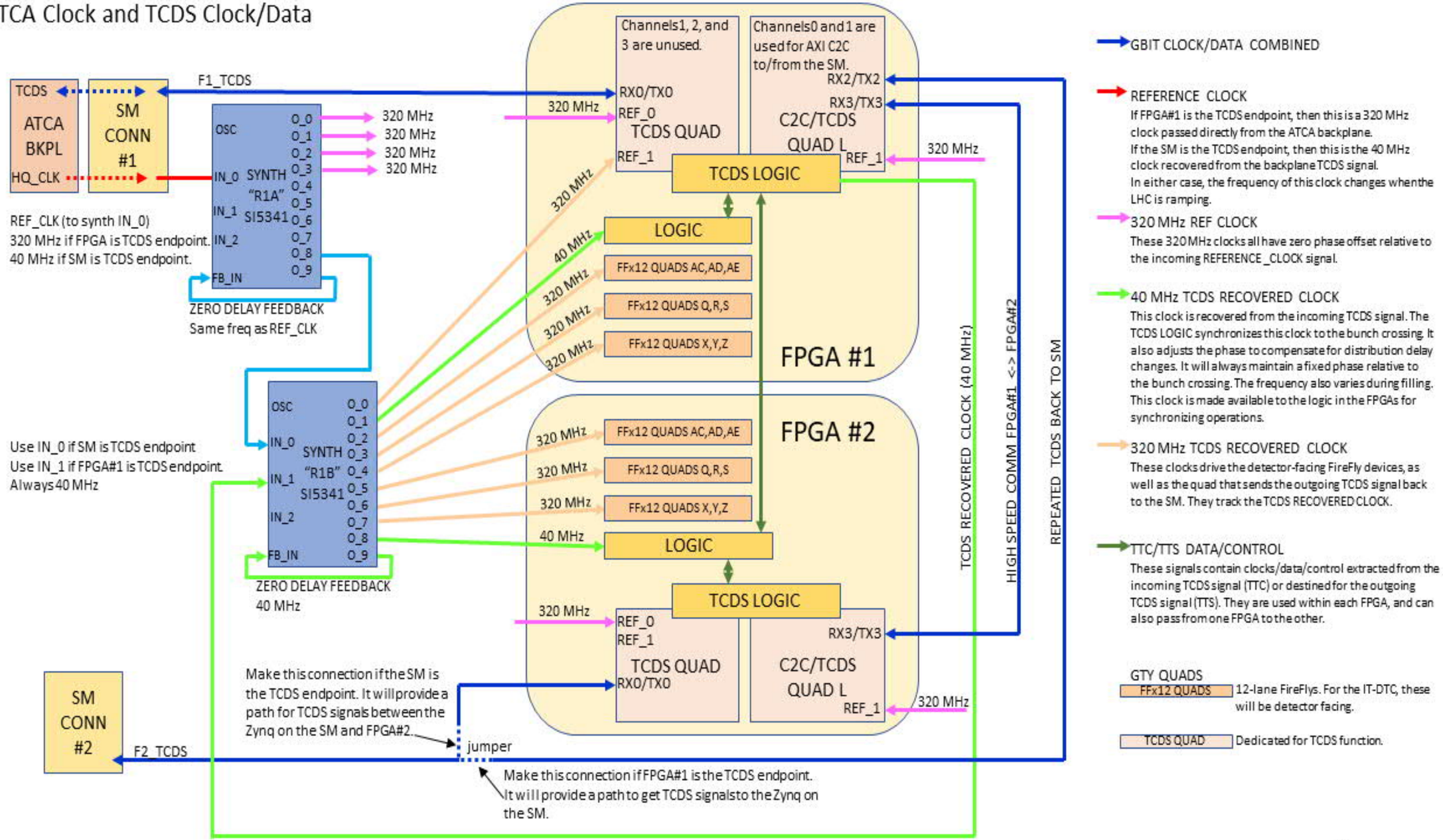
Apollo CM Dual A2577: TCDS Simplified

ATCA Clock and TCDS Clock/Data



GBIT CLOCK/DATA COMBINED

REFERENCE CLOCK

If FPGA#1 is the TCDS endpoint, then this is a 320 MHz clock passed directly from the ATCA backplane.
If the SM is the TCDS endpoint, then this is the 40 MHz clock recovered from the backplane TCDS signal.
In either case, the frequency of this clock changes when the LHC is ramping.

320 MHz REF CLOCK

These 320 MHz clocks all have zero phase offset relative to the incoming REFERENCE_CLOCK signal.

40 MHz TCDS RECOVERED CLOCK

This clock is recovered from the incoming TCDS signal. The TCDS LOGIC synchronizes this clock to the bunch crossing. It also adjusts the phase to compensate for distribution delay changes. It will always maintain a fixed phase relative to the bunch crossing. The frequency also varies during filling. This clock is made available to the logic in the FPGAs for synchronizing operations.

320 MHz TCDS RECOVERED CLOCK

These clocks drive the detector-facing FireFly devices, as well as the quad that sends the outgoing TCDS signal back to the SM. They track the TCDS RECOVERED CLOCK.

TTC/TTS DATA/CONTROL

These signals contain clocks/data/control extracted from the incoming TCDS signal (TTC) or destined for the outgoing TCDS signal (TTS). They are used within each FPGA, and can also pass from one FPGA to the other.

GTY QUADS

FFx12 QUADS	12-lane FireFlys. For the IT-DTC, these will be detector facing.
TCDS QUAD	Dedicated for TCDS function.

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APOLLO CM W/ DUAL A2577, MK1		
Title: 1.11: TCDS SIMPLIFIED		
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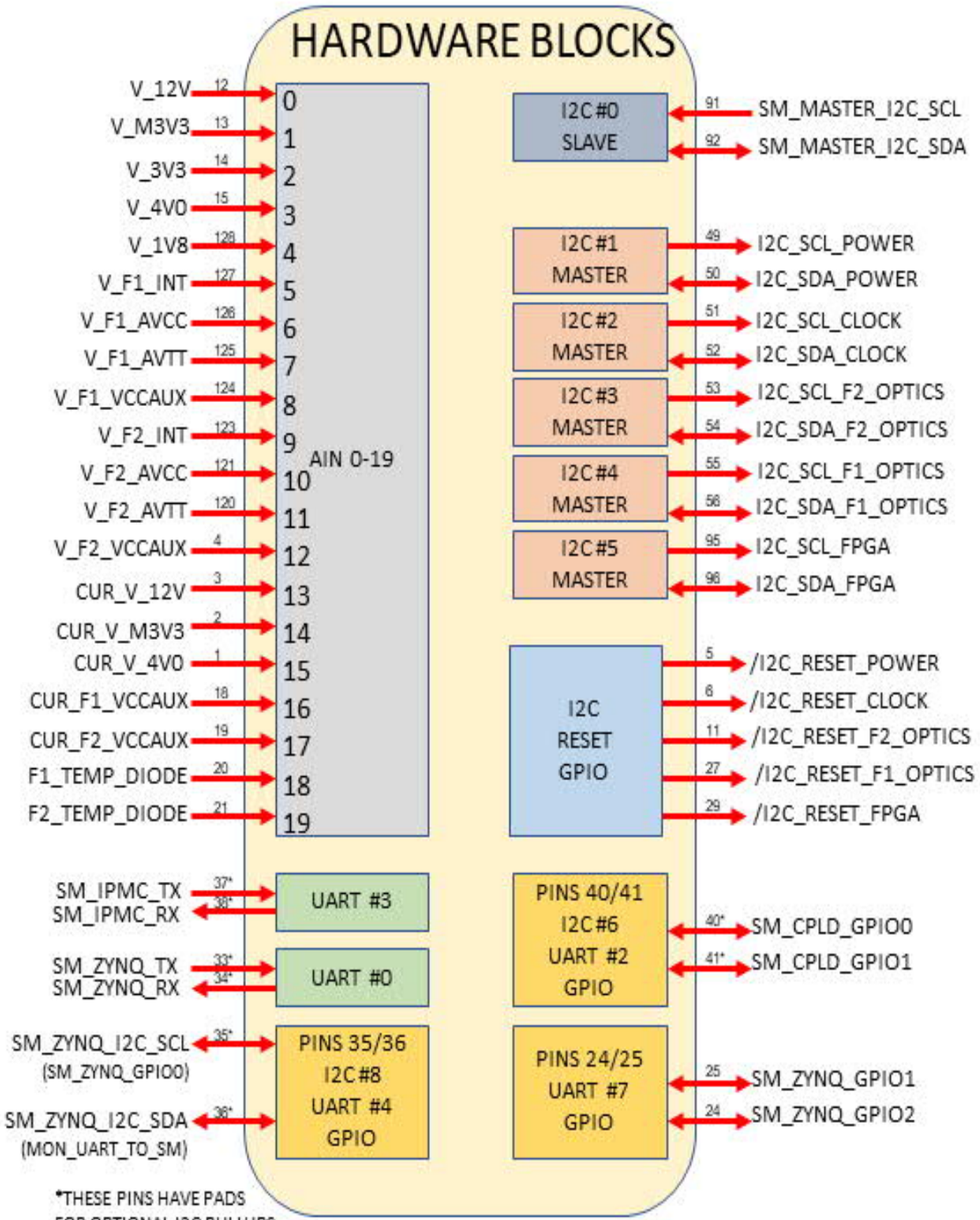
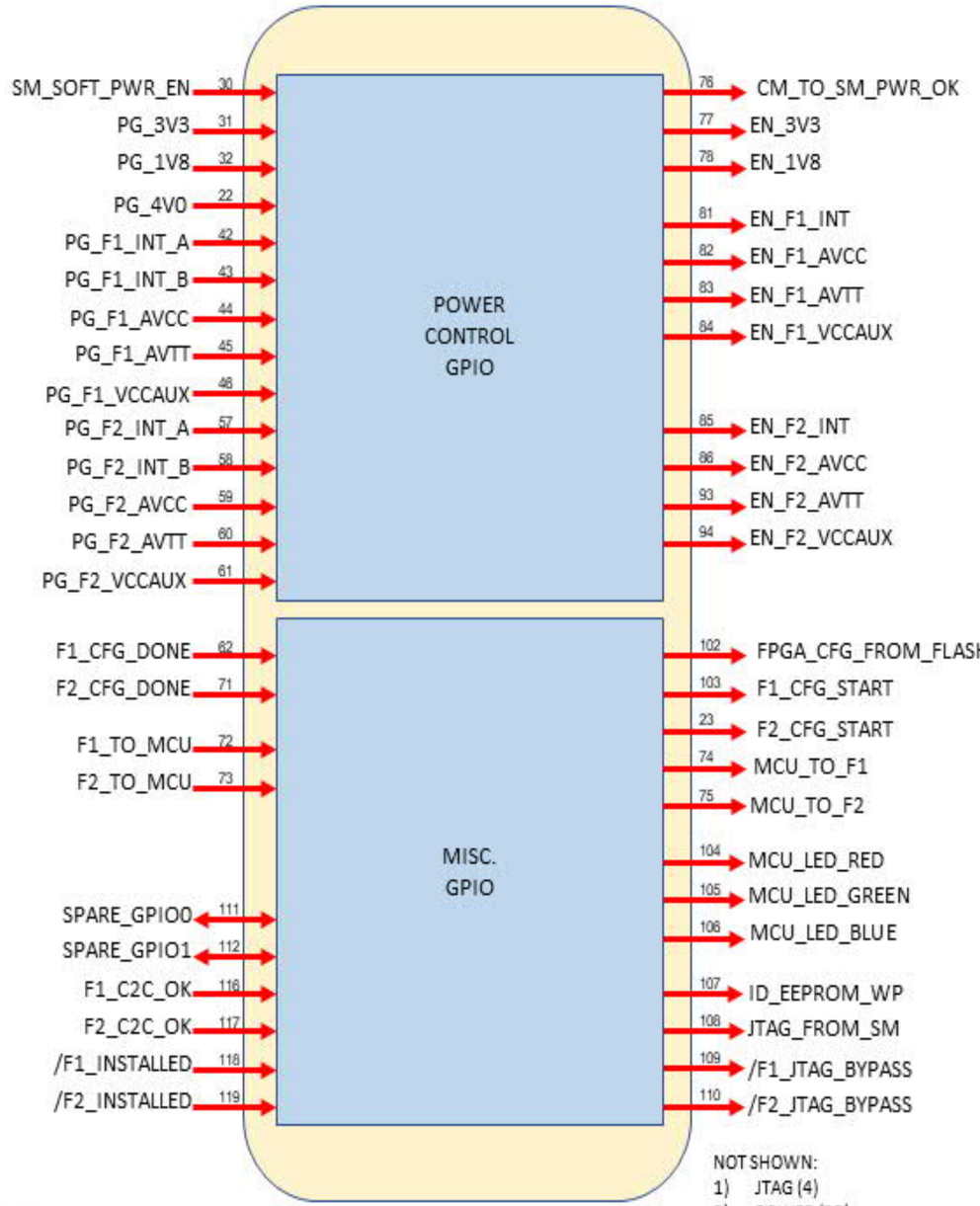
Apollo CM Dual A2577: MCU Connections and Internal Resources

1) Connect a non-SYSMON FPGA I2C block for user use
2) Consider a single I2C for optics





NOT SHOWN:
1) JTAG (4)
2) POWER (28)
3) CLOCKING (4)
4) CONTROL (3)

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APOLLO CM W/ DUAL A2577, MK1			
Title: 1.12: MCU I/O AND INTERNALS			
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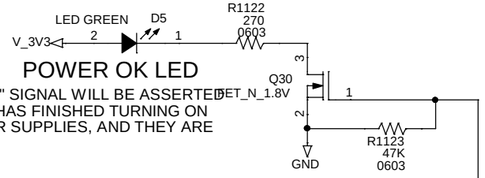
2.01: SM POWER AND CONTROL CONNECTOR

POWER OK LED

THE "POWER_OK" SIGNAL WILL BE ASSERTED WHEN THE MCU HAS FINISHED TURNING ON ALL FPGA POWER SUPPLIES, AND THEY ARE ALL GOOD.



I2C0 IS A SLAVE INTERFACE. IT IS CONNECTED TO THE IPMC ON THE SM.

I2C8 CAN BE A MASTER OR A SLAVE. IT IS USED TO GET MONITORING DATA INTO THE ZYNQ. ON CMv1, THIS IS THE UART#4 PATH. IT IS CONNECTED TO THE ZYNQ ON THE SM.

I2C6 IS AVAILABLE FOR FUTURE USE. IT IS CONNECTED TO THE CPLD ON THE SM. PULLUPS ARE NOT INSTALLED.

THE I2C7 PINS ARE INITIALLY USED FOR UART#3 CONNECTIONS TO THE IPMC ON THE SM. PULLUPS ARE NOT INSTALLED.

THE I2C9 PINS ARE INITIALLY USED FOR UART#0 CONNECTIONS TO THE ZYNQ ON THE SM.THIS PROVIDES A BOOTLOADER FUNCTION FOR THE MCU. PULLUPS ARE NOT INSTALLED.

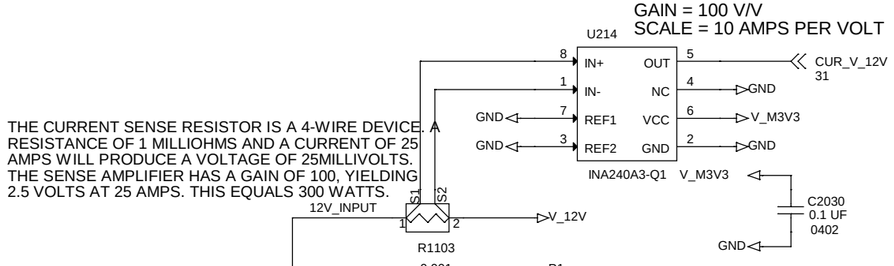
IF THE SERVICE BLADE HAS I2C PULLUP RESISTORS, THEN THESE RESISTORS SHOULD BE A LARGE VALUE, JUST SUFFICIENT TO HOLD THE CONTROLLER INPUTS HIGH. IF THE SERVICE BLADE DOES NOT HAVE I2C PULLUP RESISTORS, THEN THESE NEED TO BE AN APPROPRIATE VALUE FOR I2C OPERATION.

TM4C SLAVE I2C ADDR = 0X40

TM4C1290 I2C ADDRESS:
ASSIGN A SLAVE ADDRESS TO THIS DEVICE BY WRITING A VALUE INTO THE "I2CSOAR" REGISTER.

V_12V
R = 0.001 OHM
GAIN = 100 V/V
SCALE = 10 AMPS PER VOLT

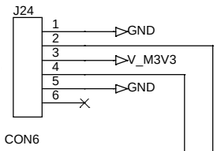
THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 1 MILLIOHMS AND A CURRENT OF 25 AMPS WILL PRODUCE A VOLTAGE OF 25MILLIVOLTS. THE SENSE AMPLIFIER HAS A GAIN OF 100, YIELDING 2.5 VOLTS AT 25 AMPS. THIS EQUALS 300 WATTS.



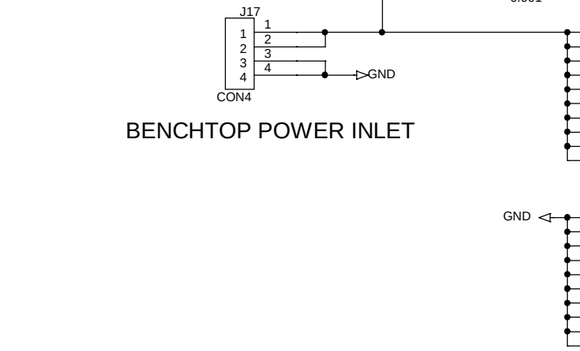
THIS CONNECTOR IS FOR A STANDALONE USB-TO-UART CABLE. SEE DIGIKEY 768-1015 (FTDI TTL-232R-3V3). THE FACTORY CONNECTOR NEEDS TO BE REPLACED WITH A 6-PIN 2MM PLUG.

THIS SHOULD ONLY BE USED WHEN THE CM IS NOT MATED TO AN SM.

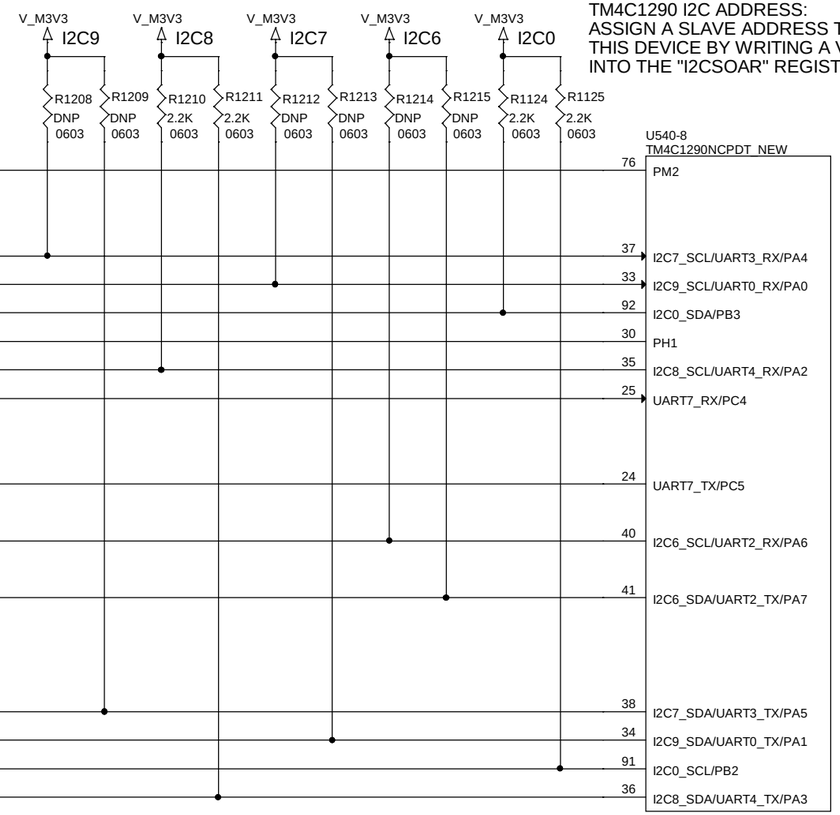
MCU UART



BENCHTOP POWER INLET



/PS_RST IS NOT USED IN THIS DESIGN

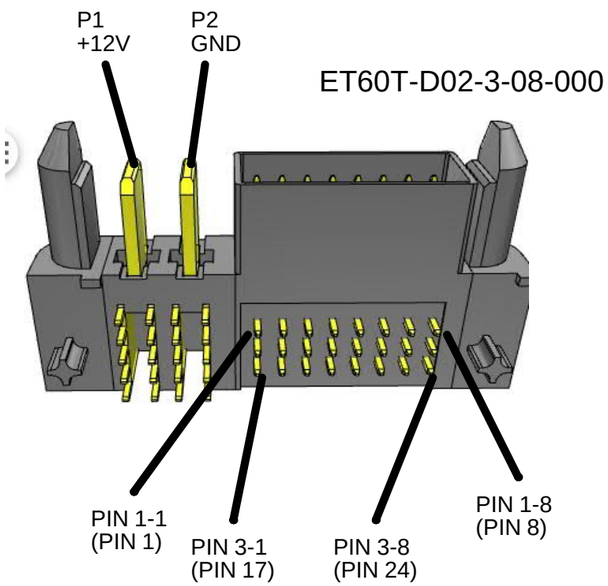


ZERO-OHM RESISTORS ON PIN 4 AND PIN 20 ARE PLACED ADJACENT TO EACH OTHER. IF "TX" AND "RX" NEED TO BE SWAPPED, REMOVE AND ROTATE THE JUMPERS BY 90 DEGREES.

THE SAME IS TRUE FOR THE RESISTORS ON PIN 5 AND PIN 21.

IN ROW 2, PINS 1, 4, 6, AND 8 ARE "GND" ON SMv1. A CMv2 BOARD MUST BE ABLE TO TOLERATE A HARD GND CONNECTION ON THESE PINS IN CASE IT IS CONNECTED TO AN SMv1.

IF THE MCU IS DRIVING AN OUTPUT HIGH, AND THE SIGNAL IS SHORTED TO GND, A 270 OHM RESISTOR WILL LIMIT THE CURRENT TO 12 MA. THE RESISTOR POWER WILL BE 0.04 WATTS.



APOLLO CM W/ DUAL A2577, MK1

Title: 2.01: SM POWER AND CONTROL CONNECTOR

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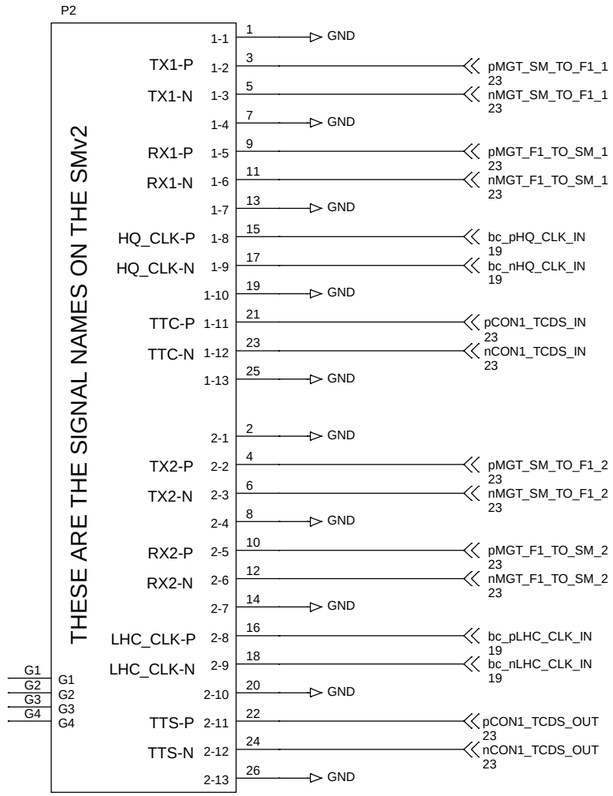
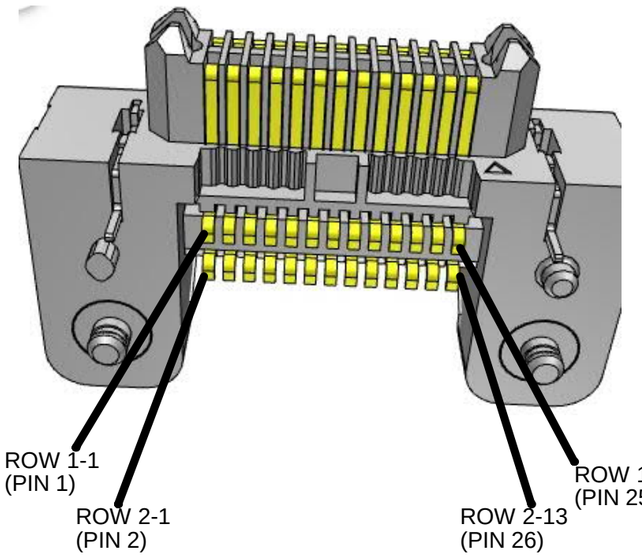
2.02: SM HIGH SPEED CONNECTORS

THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. AC COUPLING CAPACITORS ARE ASSUMED TO BE ON THE SM.

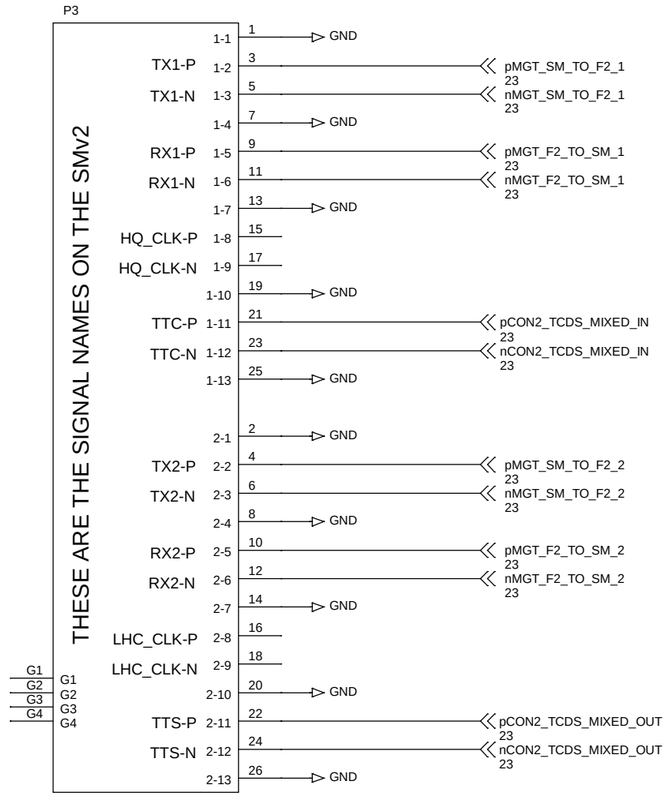
FPGA#1 AND BACKPLANE CLOCK SIGNALS





ERM8-013-01-L-D-RA-DS

FPGA#2 SIGNALS



THE TCDS SIGNALS ON HIGH SPEED CONNECTOR #2 ARE LABELED "MIXED" BECAUSE THEY CAN EITHER BE REGULAR TCDS SIGNALS WHEN THE SM IS THE TCDS ENDPOINT, OR THEY CAN BE REPEATED TCDS SIGNALS WHEN FPGA#1 IS THE TCDS ENDPOINT.

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.02: SM HIGH SPEED CONNECTORS		
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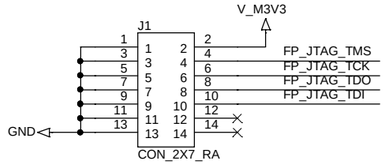
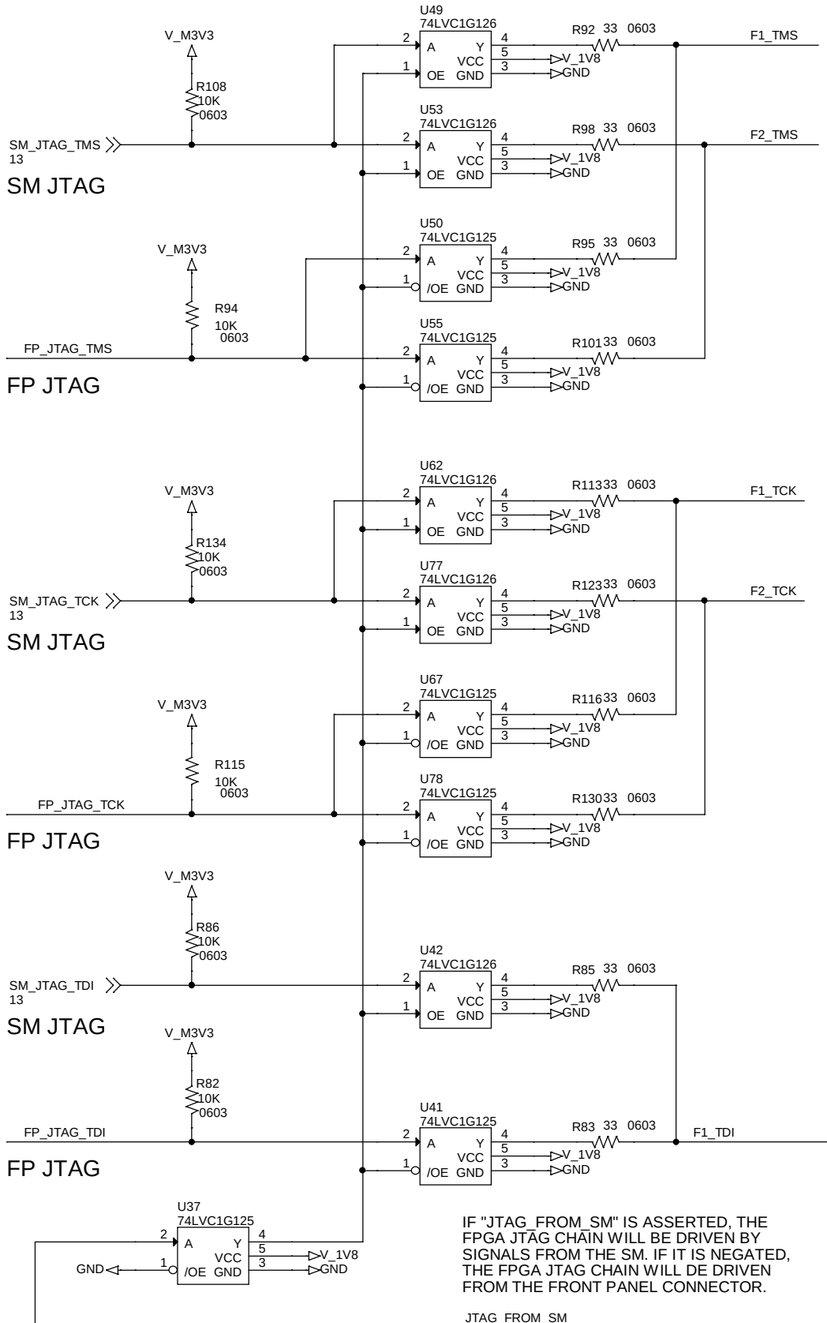
2.03: MCU AND FPGA JTAG

THE FPGA JTAG REFERENCE IS 3.3 VOLTS.



FRONT PANEL
FPGA JTAG



IF "JTAG_FROM_SM" IS ASSERTED, THE FPGA JTAG CHAIN WILL BE DRIVEN BY SIGNALS FROM THE SM. IF IT IS NEGATED, THE FPGA JTAG CHAIN WILL DE DRIVEN FROM THE FRONT PANEL CONNECTOR.

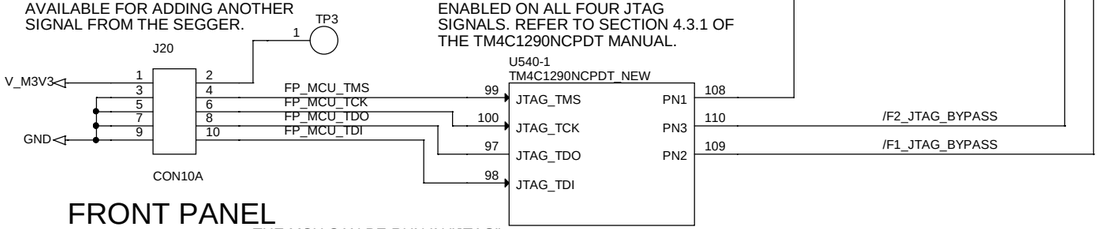
JTAG_FROM_SM

THE TEST POINT ON PIN 2 IS AVAILABLE FOR ADDING ANOTHER SIGNAL FROM THE SEGGER.

THE MCU HAS INTERNAL PULLUPS ENABLED ON ALL FOUR JTAG SIGNALS. REFER TO SECTION 4.3.1 OF THE TM4C1290NCPDT MANUAL.

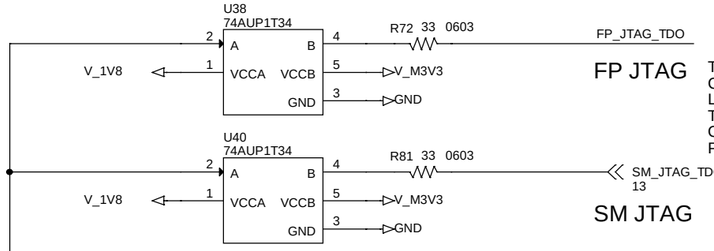
THE MCU CONNECTOR ON THE FRONT PANEL IS A 10-PIN 50-MIL PITCH CONNECTOR. A SEGGER MODEL 8.06.28 "50-MIL 10-PIN PATCH ADAPTER" IS USED AT THE PROGRAMMER.

THE MCU JTAG REFERENCE IS 3.3 VOLTS.



FRONT PANEL
MCU JTAG

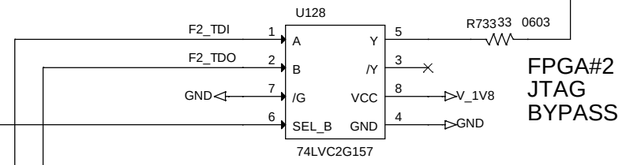
THE MCU CAN BE RUN IN "JTAG" MODE OR "ARM SWD" MODE.



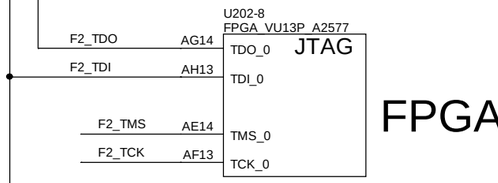
FP JTAG

SM JTAG

THESE VOLTAGE TRANSLATORS CONVERT THE 1.8 VOLT LOGIC LEVEL FROM THE LAST FPGA TO THE 3.3 VOLT LOGIC LEVEL USED ON THE SM OR THE EXTERNAL PROGRAMMER.

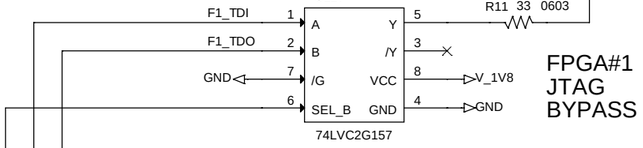


FPGA#2
JTAG
BYPASS

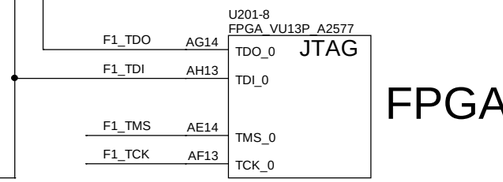


FPGA#2

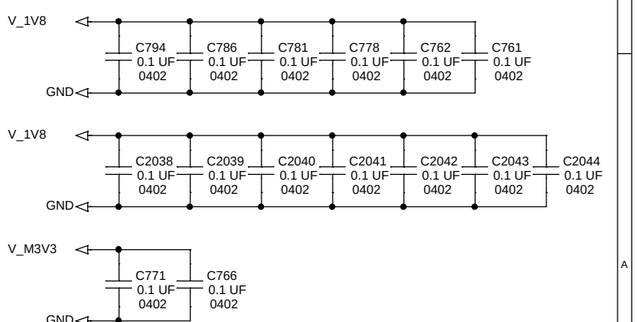
F2_TDI



FPGA#1
JTAG
BYPASS



FPGA#1



APOLLO CM W/ DUAL A2577, MK1

Title: 2.03: MCU AND FPGA JTAG

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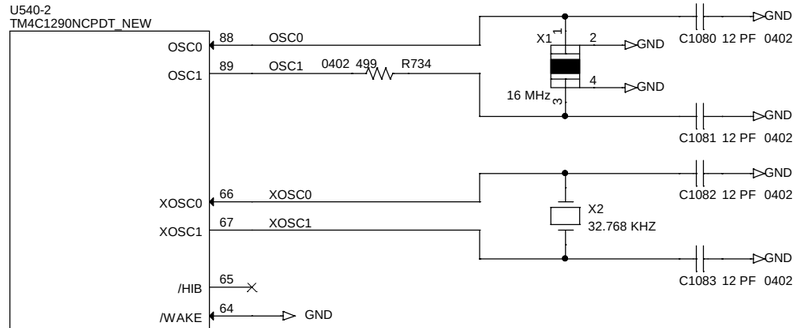
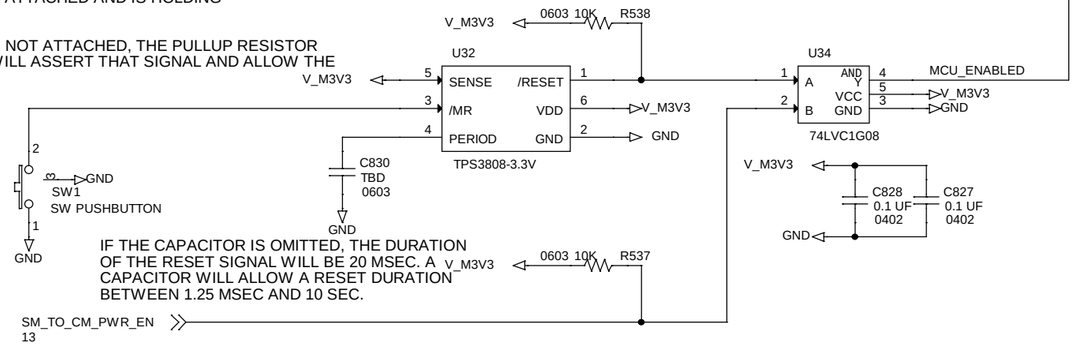
2.04: MCU I/O AND POWER

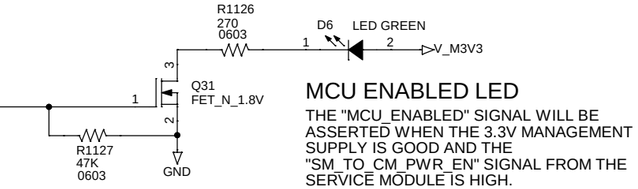


AS PER TABLE 25.7 OF THE TM4C1290 MANUAL, THE UNUSED "/WAKE" PIN GET TIED TO GND AND "/HIB" IS NC.

THE ACTIVE-LO "/RESET" INPUT WILL BE ASSERTED WHEN ANY OF THE FOLLOWING ARE TRUE:
1) POWER HAS JUST BEEN APPLIED
2) THE FRONT-PANEL RESET SWITCH HAS BEEN ACTIVATED
3) THE SERVICE MODULE IS ATTACHED AND IS HOLDING "SM_TO_CM_PWR_EN" LO.

IF THE SERVICE MODULE IS NOT ATTACHED, THE PULLUP RESISTOR ON"SM_TO_CM_PWR_EN" WILL ASSERT THAT SIGNAL AND ALLOW THE BOARD TO POWER UP.

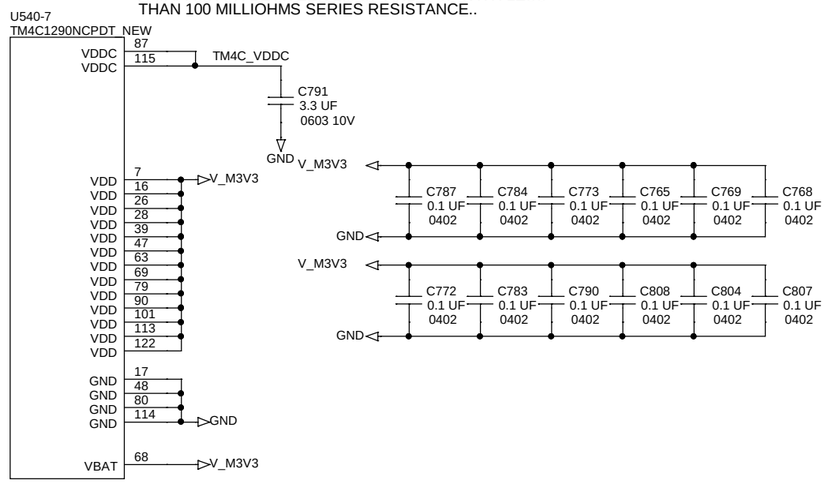




MCU ENABLED LED

THE "MCU_ENABLED" SIGNAL WILL BE ASSERTED WHEN THE 3.3V MANAGEMENT SUPPLY IS GOOD AND THE "SM_TO_CM_PWR_EN" SIGNAL FROM THE SERVICE MODULE IS HIGH.

AS PER TABLE 26.15 OF THE TM4C1290 MANUAL, THE "VDDC" PINS GET TIED TOGETHER AND CONNECTED TO A CAPACITOR BETWEEN 2.5 UF AND 4 UF WITH LESS THAN 100 MILLIOHMS SERIES RESISTANCE..



AS PER TABLE 25.7 OF THE TM4C1290 MANUAL, THE UNUSED "VBAT" PIN GET TIED TO VDD.

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.04: MCU I/O AND POWER		
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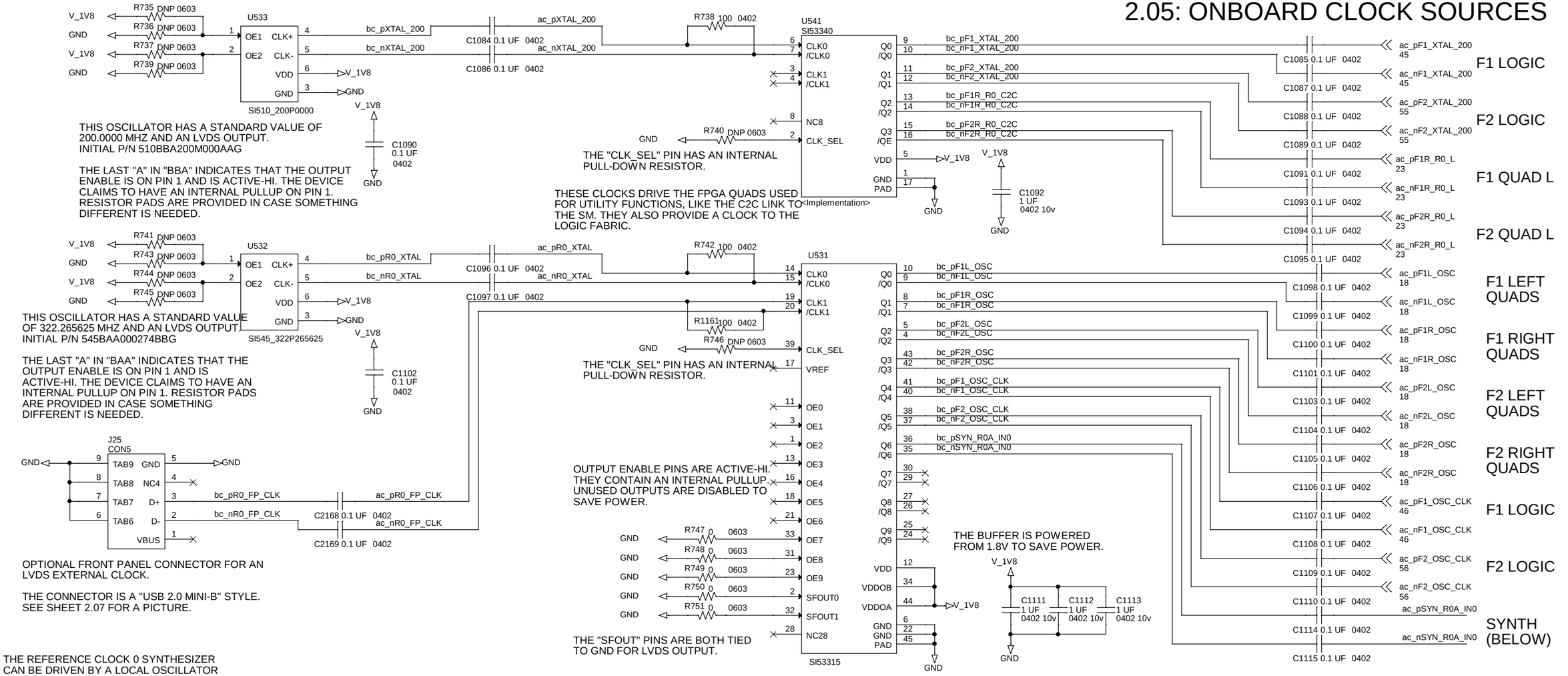
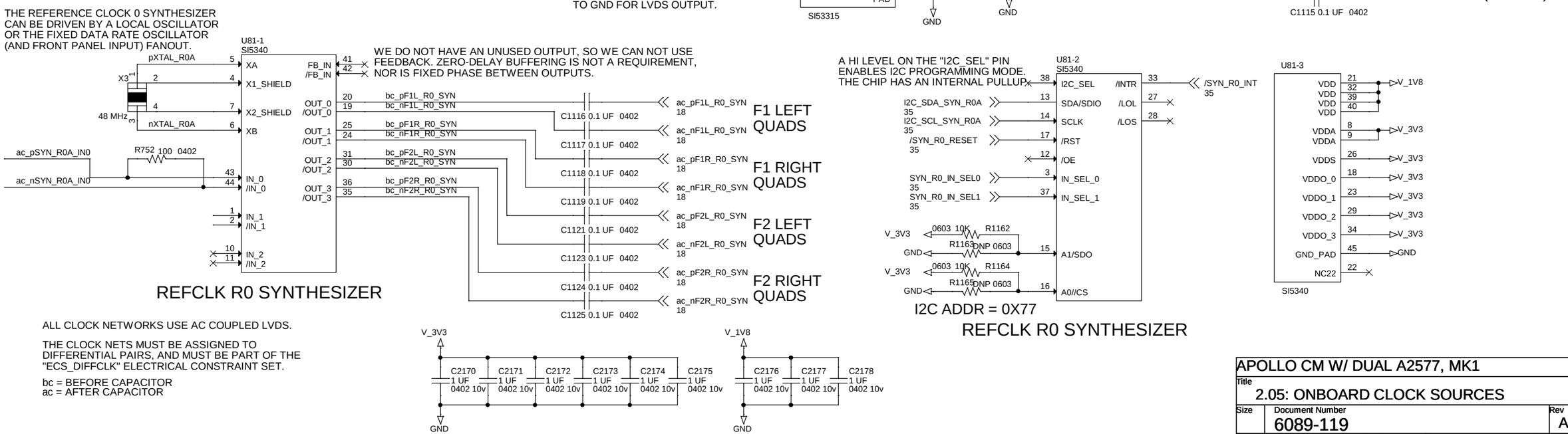
2.05: ONBOARD CLOCK SOURCES





APOLLO CM W/ DUAL A2577, MK1	
Title	2.05: ONBOARD CLOCK SOURCES
Size	Document Number 6089-119 Rev A
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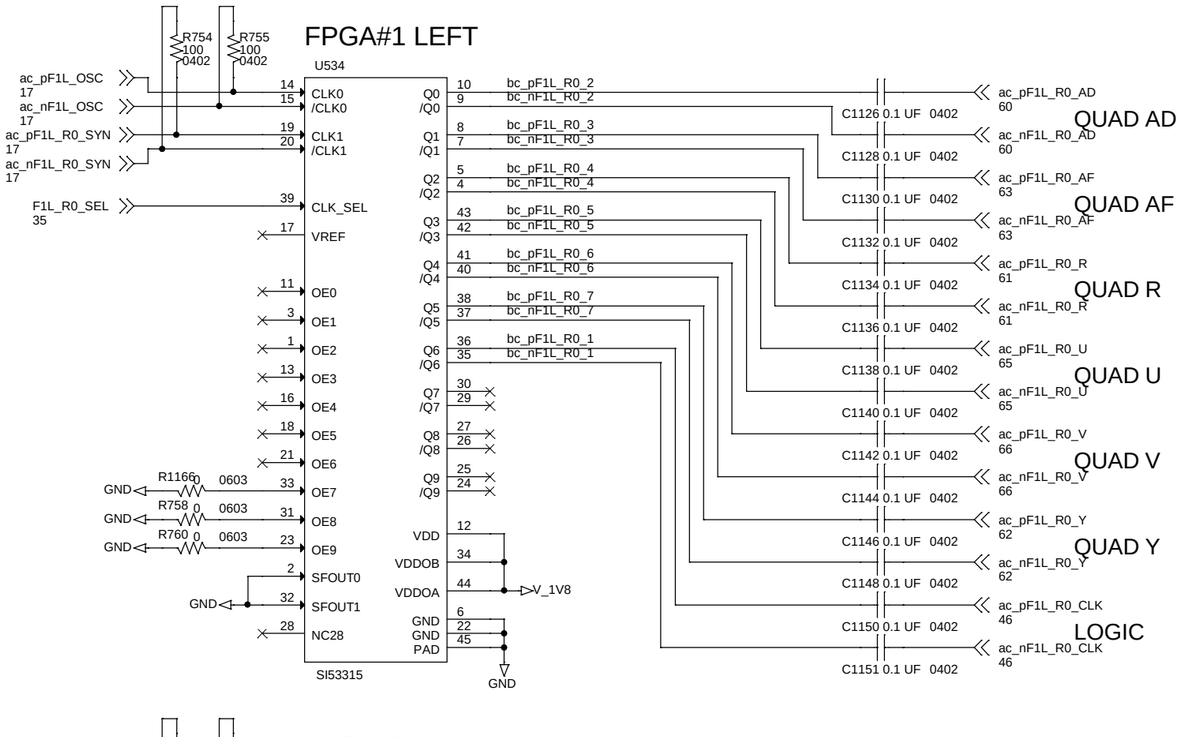
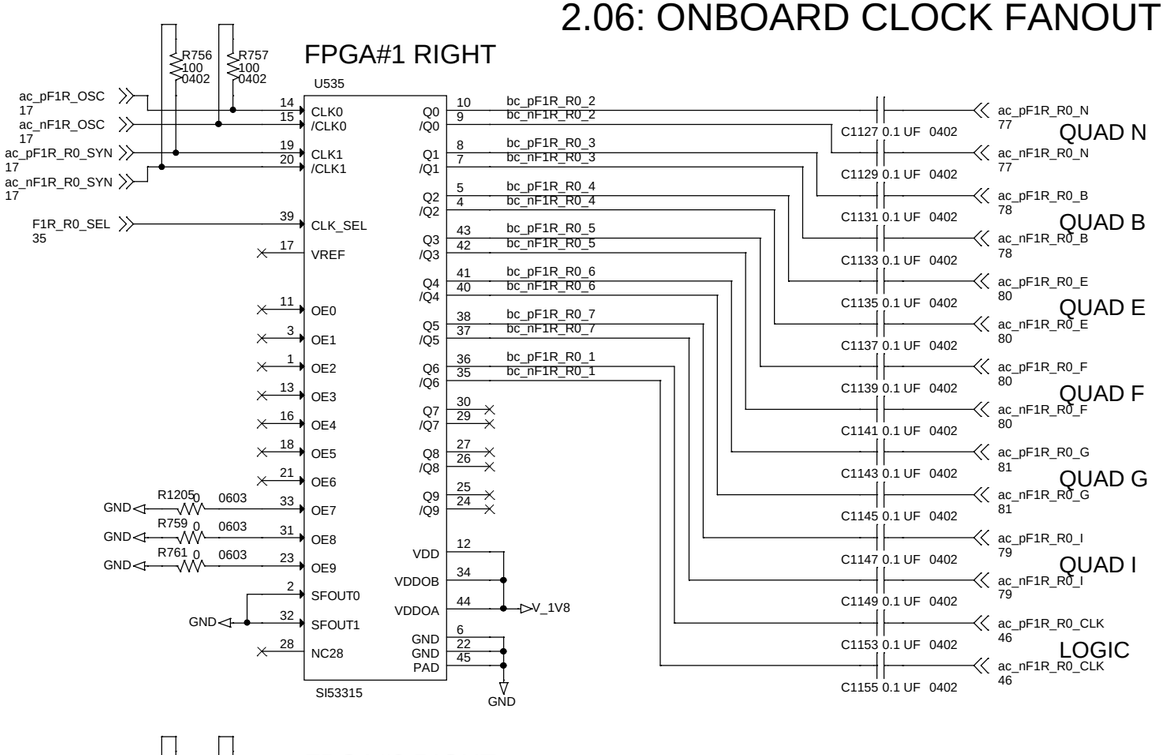
2.06: ONBOARD CLOCK FANOUT

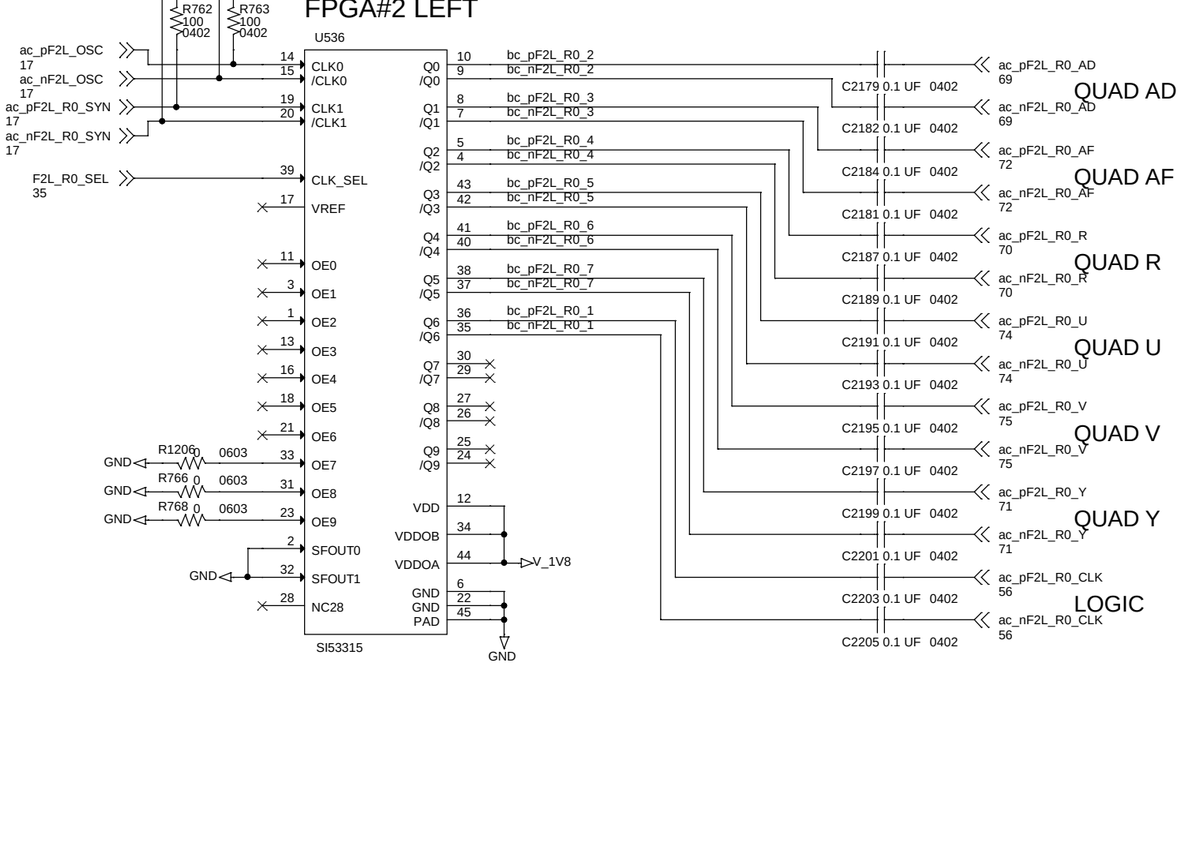
FPGA#1 LEFT



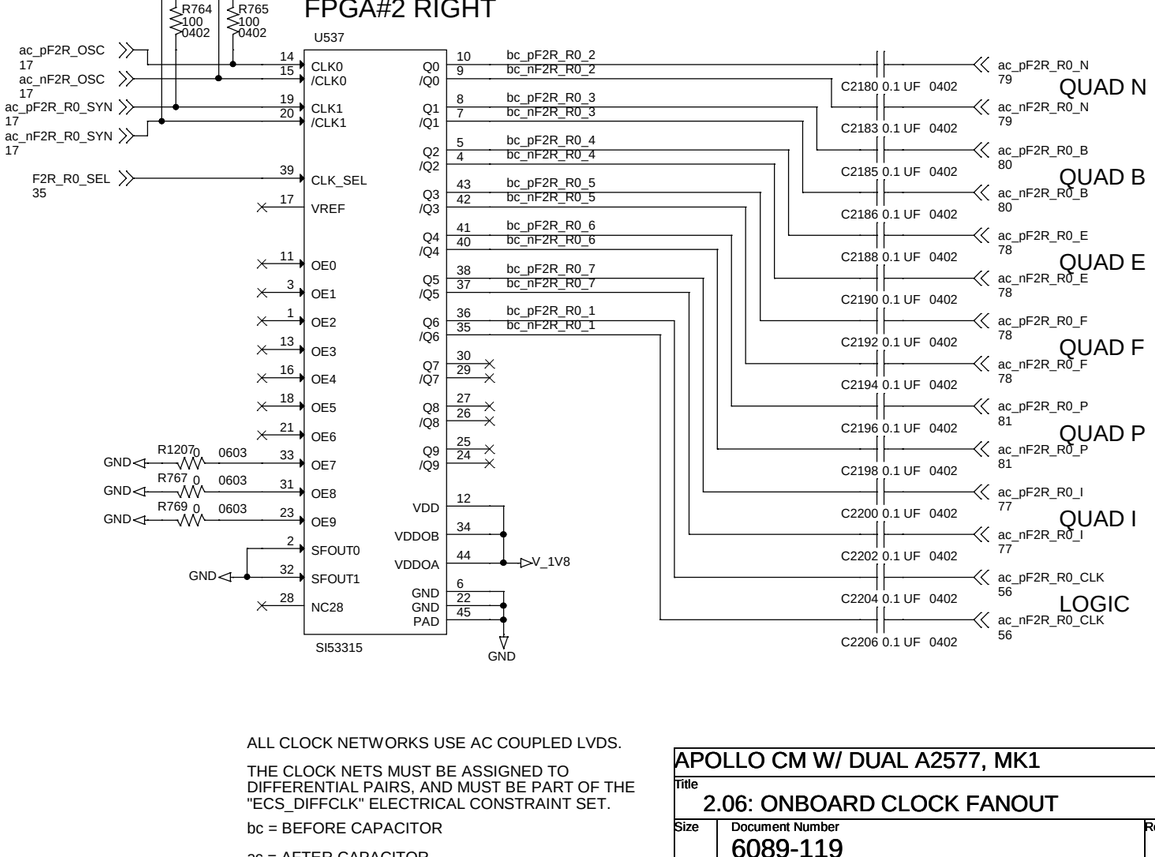
FPGA#1 RIGHT



FPGA#2 LEFT



FPGA#2 RIGHT



ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.06: ONBOARD CLOCK FANOUT		
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2.07: EXTERNAL REFCLK SYNTH R1A

U599-1
SI5341

pXTAL_R1A → XA (8)
nXTAL_R1A → XB (9)
X4: 48 MHz, pins 1, 2, 3, 4
X1_SHIELD (7)
X2_SHIELD (10)

IF THE HQ_CLK OR LHC_CLK IS AC-COUPLED ON THE SM, USE ZERO-OHM RESISTORS ON THESE CAPACITOR PADS.

HQ_CLK

320 MHZ IF FPGA#1 IS TCDS ENDPOINT.
40 MHZ IF SM IS TCDS ENDPOINT

bc_pHQ_CLK_IN 14 → C2209 0.1 UF 0402 → ac_pHQ_CLK_IN → R1167 100 0402 → IN_0 (63)
bc_nHQ_CLK_IN 14 → C2213 0.1 UF 0402 → ac_nHQ_CLK_IN → /IN_0 (64)

LHC_CLK

ALWAYS 40 MHZ

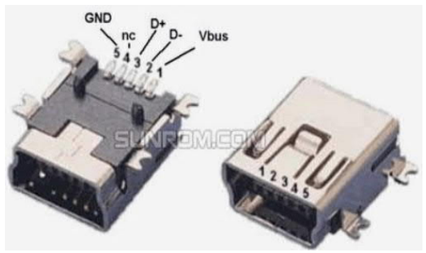
bc_pLHC_CLK_IN 14 → C2216 0.1 UF 0402 → ac_pLHC_CLK_IN → R1168 100 0402 → IN_1 (1)
bc_nLHC_CLK_IN 14 → C2218 0.1 UF 0402 → ac_nLHC_CLK_IN → /IN_1 (2)

J26
CON5

GND (9) TAB9 GND (5) → GND
(8) TAB8 NC4 (4) → X
(7) TAB7 D+ (3) → bc_pR1_FP_CLK → C2221 0.1 UF 0402 → ac_pR1_FP_CLK → R1169 100 0402 → IN_2 (14)
(6) TAB6 D- (2) → bc_nR1_FP_CLK → C2223 0.1 UF 0402 → ac_nR1_FP_CLK → /IN_2 (15)
VBUS (1) → X

OPTIONAL FRONT PANEL CONNECTOR FOR AN LVDS EXTERNAL CLOCK.

THE CONNECTOR IS A "USB 2.0 MINI-B" STYLE.



ZERO-DELAY FEEDBACK
320 MHZ IF FPGA#1 IS TCDS ENDPOINT.
40 MHZ IF SM IS TCDS ENDPOINT

ac_pR1A_FB → C2229 0.1 UF 0402 → R1170 100 0402 → FB_IN (61)
ac_nR1A_FB → C2230 0.1 UF 0402 → /FB_IN (62)

A HI LEVEL ON THE "I2C_SEL" PIN ENABLES I2C PROGRAMMING MODE. THE CHIP HAS AN INTERNAL PULLUP.

U599-2

I2C_SEL (39) → /INTR (12) → /SYN_R1A_INT 35
SDA/SDIO (18) ← I2C_SDA_SYN_R1A 35
SCLK (16) ← I2C_SCL_SYN_R1A 35
/RST (6) ← /SYN_R1A_RESET 35
/OE (11) → X
IN_SEL_0 (3) ← SYN_R1A_IN_SEL0 35
IN_SEL_1 (4) ← SYN_R1A_IN_SEL1 35
FINC (48) → X
FDEC (25) → X
/SYNC (5) → X
/LOL (47) → X
A1/SDO (17) ← V_M3V3 → 0603 10K R1171 → GND; R1172 DNP 0603 → GND
A0//CS (19) ← V_M3V3 → 0603 10K R1173 → GND; R1174 DNP 0603 → GND

I2C ADDR = 0X77

SI5341

U599-3

VDD (32, 46, 60) ← V_1V8
VDDA (13) ← V_3V3
VDDO_0 (22) ← V_1V8
VDDO_1 (26)
VDDO_2 (29)
VDDO_3 (33)
VDDO_4 (36)
VDDO_5 (40)
VDDO_6 (43)
VDDO_7 (49)
VDDO_8 (52)
VDDO_9 (57)
GND_PAD (65) → GND
NC20 (20) → X
NC21 (21) → X
NC55 (55) → X
NC56 (56) → X

SI5341

OUT_0 (24)	bc_pF1L_R0_TCDS	C2210 0.1 UF 0402	ac_pF1L_R0_AB 23	F1 QUAD AB (TCDS QUAD)
/OUT_0 (23)	bc_nF1L_R0_TCDS	C2207 0.1 UF 0402	ac_nF1L_R0_AB 23	
OUT_1 (28)	bc_pF2L_R0_TCDS	C2211 0.1 UF 0402	ac_pF2L_R0_AB 23	F2 QUAD AB (TCDS QUAD)
/OUT_1 (27)	bc_nF2L_R0_TCDS	C2208 0.1 UF 0402	ac_nF2L_R0_AB 23	
OUT_2 (31)	bc_pSYN_R1B_IN0	C2212 0.1 UF 0402	ac_pSYN_R1B_IN0 20	SYN R1B IN0
/OUT_2 (30)	bc_nSYN_R1B_IN0	C2214 0.1 UF 0402	ac_nSYN_R1B_IN0 20	
OUT_3 (35)	bc_pSYN_R1C_IN0	C2215 0.1 UF 0402	ac_pSYN_R1C_IN0 21	SYN R1C IN0
/OUT_3 (34)	bc_nSYN_R1C_IN0	C2217 0.1 UF 0402	ac_nSYN_R1C_IN0 21	
OUT_4 (38)	bc_pF1L_R1_3	C2219 0.1 UF 0402	ac_pF1L_R1_AF 63	F1 QUAD AF
/OUT_4 (37)	bc_nF1L_R1_3	C2220 0.1 UF 0402	ac_nF1L_R1_AF 63	
OUT_5 (42)	bc_pF1L_R1_5	C2222 0.1 UF 0402	ac_pF1L_R1_U 65	F1 QUAD U (T,U,V)
/OUT_5 (41)	bc_nF1L_R1_5	C2224 0.1 UF 0402	ac_nF1L_R1_U 65	
OUT_6 (45)	bc_pF2L_R1_3	C2225 0.1 UF 0402	ac_pF2L_R1_AF 72	F2 QUAD AF
/OUT_6 (44)	bc_nF2L_R1_3	C2226 0.1 UF 0402	ac_nF2L_R1_AF 72	
OUT_7 (51)	bc_pF2L_R1_5	C2227 0.1 UF 0402	ac_pF2L_R1_U 74	F2 QUAD U (T,U,V)
/OUT_7 (50)	bc_nF2L_R1_5	C2228 0.1 UF 0402	ac_nF2L_R1_U 74	
OUT_8 (54)	bc_pBUF1	C2493 0.1 UF 0402	ac_pBUF1 → R1245 100 0402	
/OUT_8 (53)	bc_nBUF1	C2494 0.1 UF 0402	ac_nBUF1	
OUT_9 (59)	bc_pR1A_FB			
/OUT_9 (58)	bc_nR1A_FB			

THIS BUFFER IS NEEDED TO EXPAND THE NUMBER OF CLOCKS FROM THIS SYNTHESIZER.

U607

IN+ (1) ← R1245
IN- (2) ← GND
IN_GND (3) ← GND
OEB (19) ← GND
RSVD4 (4)
RSVD5 (5)
RSVD6 (6)
RSVD12 (12)
RSVD23 (23)
TAB (25) ← GND
VDDO0 (20)
VDDO1 (16)
VDDO2 (15)
VDDO3 (11) ← V_1V8
CLK0A (22) → bc_pF1R_R1_L → C2495 0.1 UF 0402 → ac_pF1R_R1_L 23
CLK0B (21) → bc_nF1R_R1_L → C2496 0.1 UF 0402 → ac_nF1R_R1_L 23 — F1 QUAD L (C2C/TCDS QUAD)
CLK1A (18) → bc_pF2R_R1_L → C2497 0.1 UF 0402 → ac_pF2R_R1_L 23
CLK1B (17) → bc_nF2R_R1_L → C2498 0.1 UF 0402 → ac_nF2R_R1_L 23 — F2 QUAD L (C2C/TCDS QUAD)
CLK2A (14)
CLK2B (13)
CLK3A (10)
CLK3B (9)
VIA26 (26) → GND
LOS (8)
VDD7 (7) → V_1V8
VDD24 (24)

SI5330

V_1V8 → C2504 0.1 UF 0402; C2505 0.1 UF 0402; C2506 0.1 UF 0402; C2507 0.1 UF 0402; C2508 0.1 UF 0402; C2509 0.1 UF 0402 → GND

ONE CAPACITOR NEAR EACH POWER PIN

V_1V8 → C2232 1 UF 0402 10v; C2233 1 UF 0402 10v; C2234 1 UF 0402 10v; C2235 1 UF 0402 10v; C2236 1 UF 0402 10v; C2237 1 UF 0402 10v; C2238 1 UF 0402 10v; C2239 1 UF 0402 10v → GND

TWO 1V8 BYPASS CAPS ALONG EACH EDGE

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1

Title: 2.07: EXTERNAL REFCLK SYNTH R1A

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2.08: EXTERNAL REFCLK SYNTH R1B

U597-1
SI5341

pXTAL_R1B → 8 XA
X5 (48 MHz): 2 → 7 X1_SHIELD; 4 → 10 X2_SHIELD
nXTAL_R1B → 9 XB

SYN R1B IN0
ac_pSYN_R1B_IN0 19 → 63 IN_0
R1175 100 0402
ac_nSYN_R1B_IN0 19 → 64 /IN_0

TCDS RECOVERED CLOCK
ALWAYS 40 MHZ
bc_pF1_TCDS_RECOV_CLK 44 → C2247 0.1 UF 0402 → ac_pF1_TCDS_RECOV_CLK → 1 IN_1
R1176 100 0402
bc_nF1_TCDS_RECOV_CLK 44 → C2249 0.1 UF 0402 → ac_nF1_TCDS_RECOV_CLK → 2 /IN_1

14 IN_2
15 /IN_2

ZERO-DELAY FEEDBACK
320 MHZ IF FPGA#1 IS TCDS ENDPOINT.
40 MHZ IF SM IS TCDS ENDPOINT

ac_pR1b_FB → C2260 0.1 UF 0402 → 61 FB_IN
R1177 100 0402
ac_nR1b_FB → C2261 0.1 UF 0402 → 62 /FB_IN

OUT_0	24	bc_pF1L_R1_1	C2240 0.1 UF 0402	ac_pF1L_R1_AB 23	F1 QUAD AB (TCDS QUAD)
/OUT_0	23	bc_nF1L_R1_1	C2241 0.1 UF 0402	ac_nF1L_R1_AB 23	
OUT_1	28	bc_pF1_TCDS40_CLK	C2242 0.1 UF 0402	ac_pF1_TCDS40_CLK 45	F1 LOGIC TCDS 40MHZ INPUT
/OUT_1	27	bc_nF1_TCDS40_CLK	C2243 0.1 UF 0402	ac_nF1_TCDS40_CLK 45	
OUT_2	31	bc_pF1L_R1_2	C2244 0.1 UF 0402	ac_pF1L_R1_AD 60	F1 QUAD AD (AC,AD,AE)
/OUT_2	30	bc_nF1L_R1_2	C2245 0.1 UF 0402	ac_nF1L_R1_AD 60	
OUT_3	35	bc_pF1L_R1_4	C2246 0.1 UF 0402	ac_pF1L_R1_R 61	F1 QUAD R (Q,R,S)
/OUT_3	34	bc_nF1L_R1_4	C2248 0.1 UF 0402	ac_nF1L_R1_R 61	
OUT_4	38	bc_pF1L_R1_7	C2250 0.1 UF 0402	ac_pF1L_R1_Y 62	F1 QUAD Y (X,Y,Z)
/OUT_4	37	bc_nF1L_R1_7	C2251 0.1 UF 0402	ac_nF1L_R1_Y 62	
OUT_5	42	bc_pF2_TCDS40_CLK	C2252 0.1 UF 0402	ac_pF2_TCDS40_CLK 55	F2 LOGIC TCDS 40MHZ INPUT
/OUT_5	41	bc_nF2_TCDS40_CLK	C2253 0.1 UF 0402	ac_nF2_TCDS40_CLK 55	
OUT_6	45	bc_pF2L_R1_2	C2254 0.1 UF 0402	ac_pF2L_R1_AD 69	F2 QUAD AD (AC,AD,AE)
/OUT_6	44	bc_nF2L_R1_2	C2255 0.1 UF 0402	ac_nF2L_R1_AD 69	
OUT_7	51	bc_pF2L_R1_4	C2256 0.1 UF 0402	ac_pF2L_R1_R 70	F2 QUAD R (Q,R,S)
/OUT_7	50	bc_nF2L_R1_4	C2257 0.1 UF 0402	ac_nF2L_R1_R 70	
OUT_8	54	bc_pF2L_R1_7	C2258 0.1 UF 0402	ac_pF2L_R1_Y 71	F2 QUAD Y (X,Y,Z)
/OUT_8	53	bc_nF2L_R1_7	C2259 0.1 UF 0402	ac_nF2L_R1_Y 71	
OUT_9	59	bc_pR1b_FB			
/OUT_9	58	bc_nR1b_FB			

A HI LEVEL ON THE "I2C_SEL" PIN
ENABLES I2C PROGRAMMING MODE.
THE CHIP HAS AN INTERNAL PULLUP.

U597-2
39 I2C_SEL; /INTR 12 → /SYN_R1B_INT 35
I2C_SDA_SYN_R1B 35 ↔ 18 SDA/SDIO; /LOL 47
I2C_SCL_SYN_R1B 35 → 16 SCLK
/SYN_R1B_RESET 35 → 6 /RST
11 /OE
SYN_R1B_IN_SEL0 35 → 3 IN_SEL_0
SYN_R1B_IN_SEL1 35 → 4 IN_SEL_1
48 FINC
25 FDEC
5 /SYNC

V_3V3 → 0603 10K R1178 → 17 A1/SDO
GND → R1179 DNP 0603 → 17 A1/SDO
V_3V3 → 0603 10K R1180 → 19 A0//CS
GND → R1181 DNP 0603 → 19 A0//CS

I2C ADDR = 0X77

SI5341

U597-3
VDD 32, 46, 60 → V_1V8
VDDA 13 → V_3V3
VDDO_0 22 → V_1V8
VDDO_1 26
VDDO_2 29
VDDO_3 33
VDDO_4 36
VDDO_5 40
VDDO_6 43
VDDO_7 49
VDDO_8 52
VDDO_9 57
GND_PAD 65 → GND
NC20 20
NC21 21
NC55 55
NC56 56

SI5341

V_3V3 → C2262 1 UF 0402 10v → GND

PLACE 3V3 BYPASS CAPS NEAR PIN 13

V_1V8 → C2263 1 UF 0402 10v; C2264 1 UF 0402 10v; C2265 1 UF 0402 10v; C2266 1 UF 0402 10v; C2267 1 UF 0402 10v; C2268 1 UF 0402 10v; C2269 1 UF 0402 10v; C2270 1 UF 0402 10v → GND

TWO 1V8 BYPASS CAPS ALONG EACH EDGE

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1			
Title: 2.08: EXTERNAL REFCLK SYNTH R1B			
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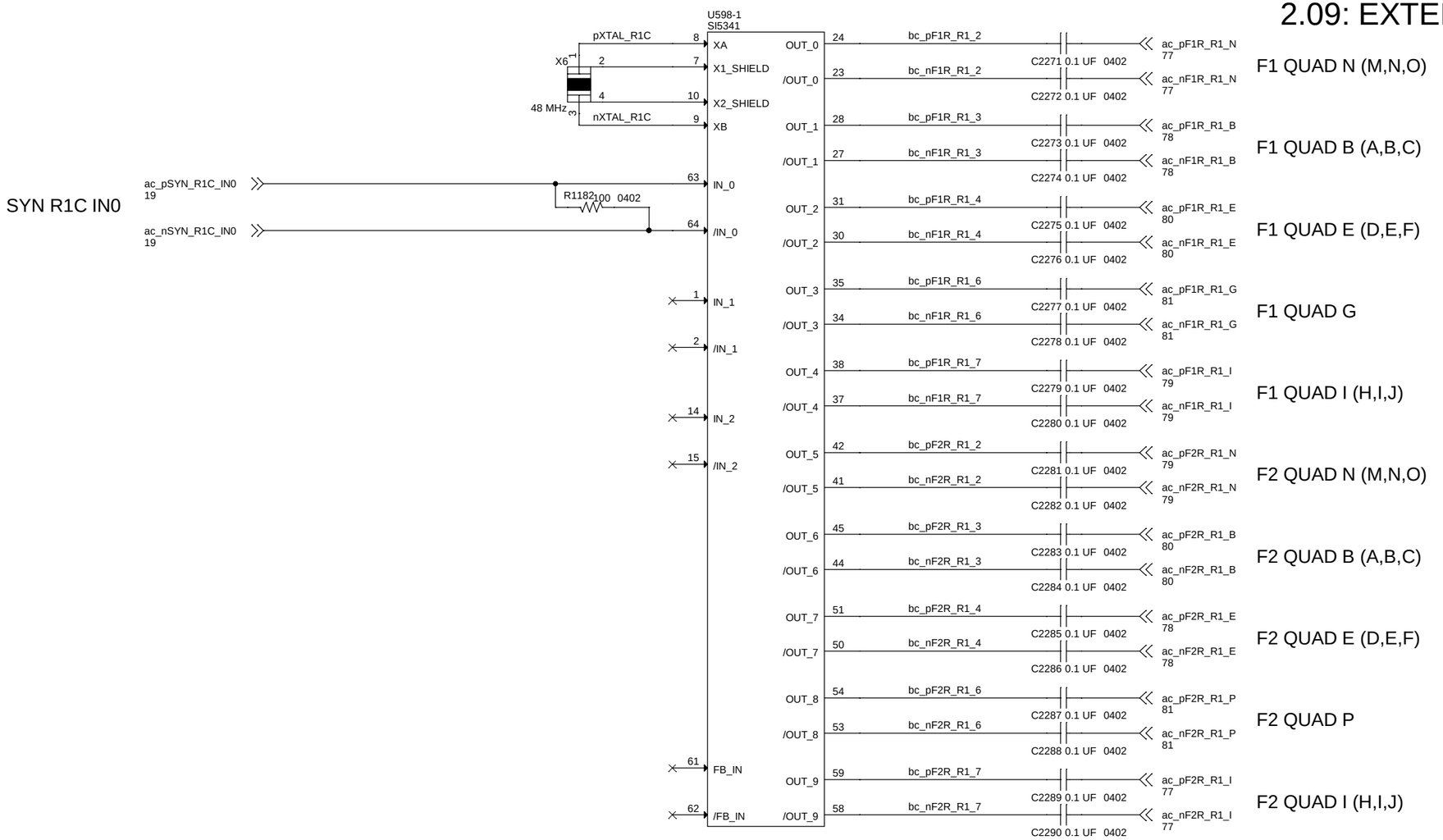
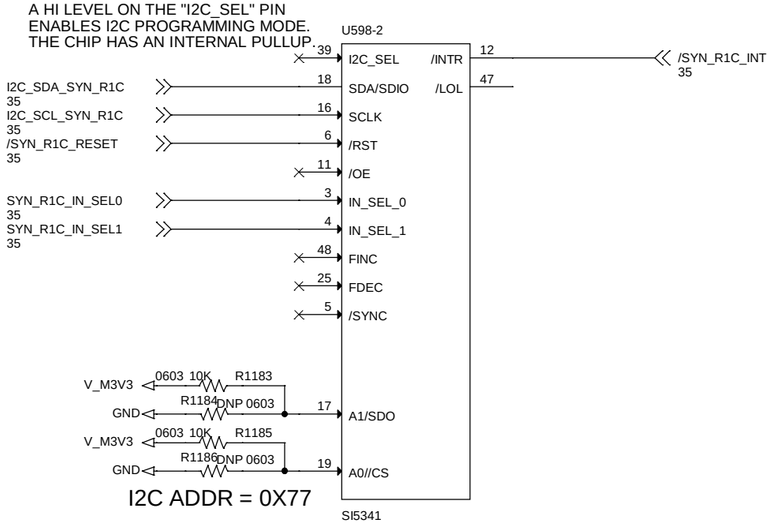
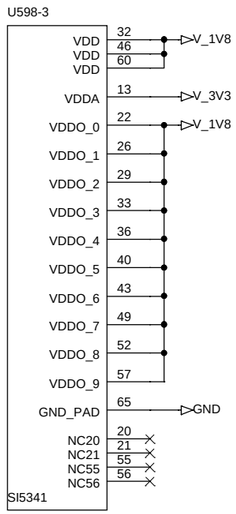
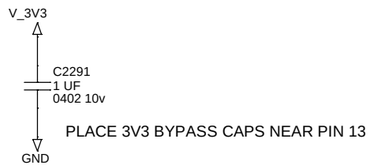
2.09: EXTERNAL REFCLK SYNTH R1C



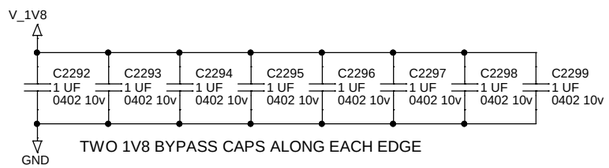
A HI LEVEL ON THE "I2C_SEL" PIN
ENABLES I2C PROGRAMMING MODE.
THE CHIP HAS AN INTERNAL PULLUP.







PLACE 3V3 BYPASS CAPS NEAR PIN 13



TWO 1V8 BYPASS CAPS ALONG EACH EDGE

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.09: EXTERNAL REFCLK SYNTH R1C		
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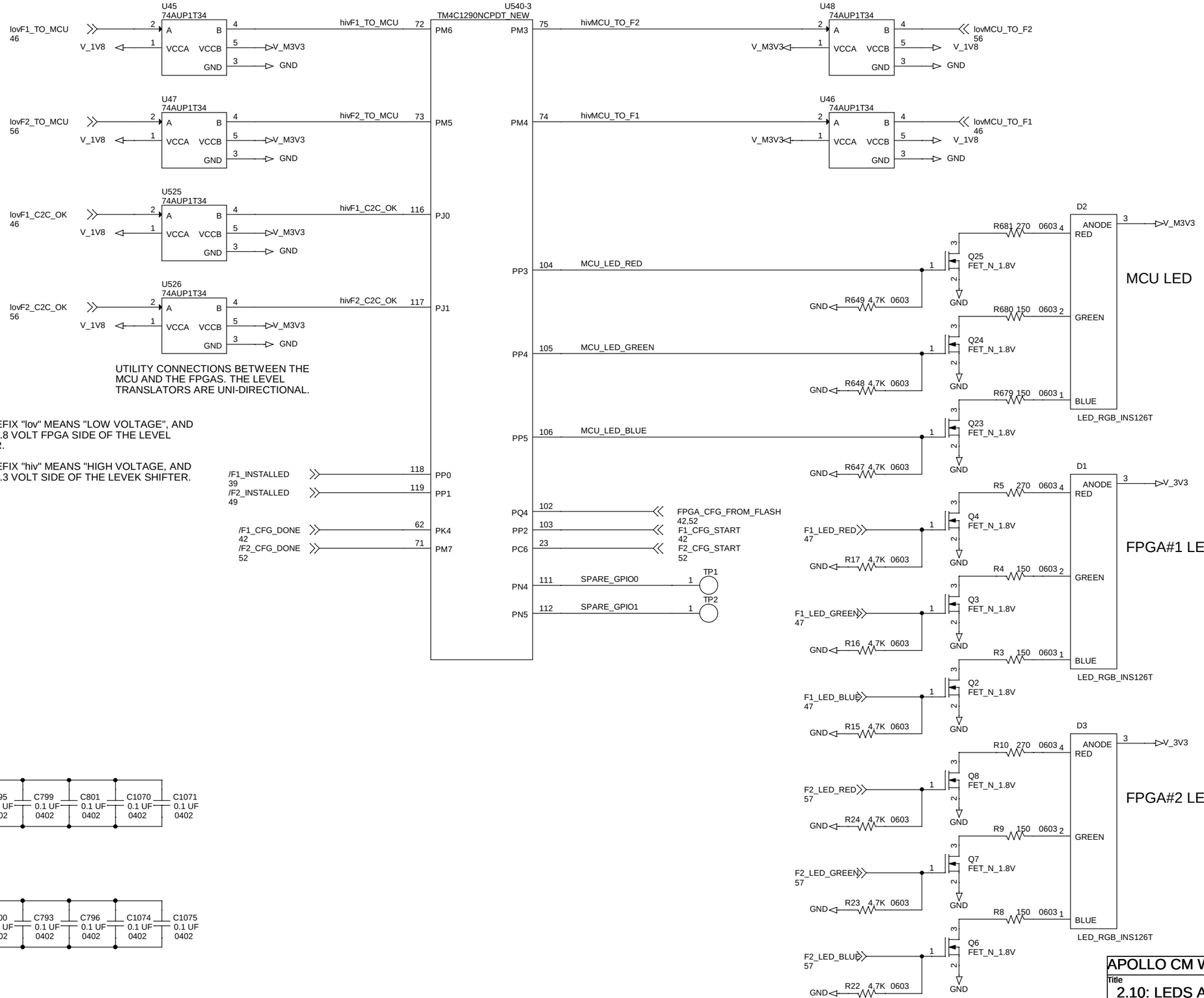
2.10: LEDS AND LEVEL SHIFTERS



APOLLO CM W/ DUAL A2577, MK1		
Title: 2.10: LEDS AND LEVEL SHIFTERS		
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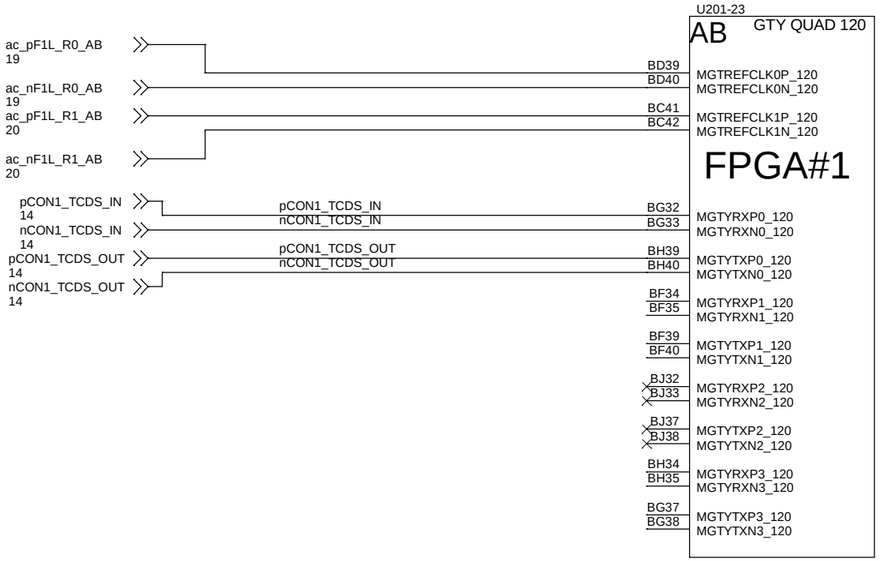
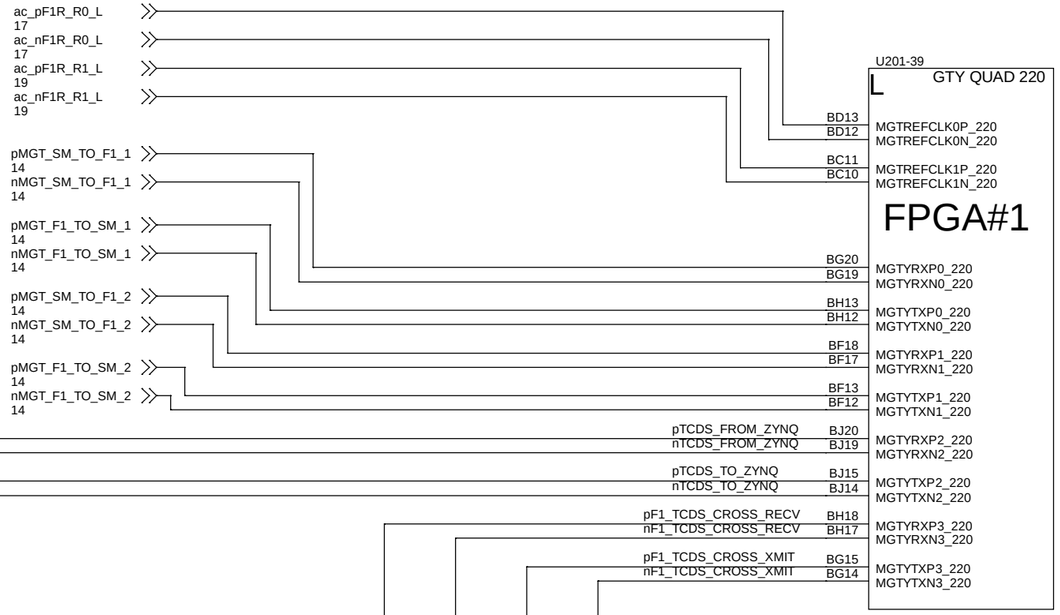
2.11: FPGA#1 AND FPGA#2 TCDS QUADS AB

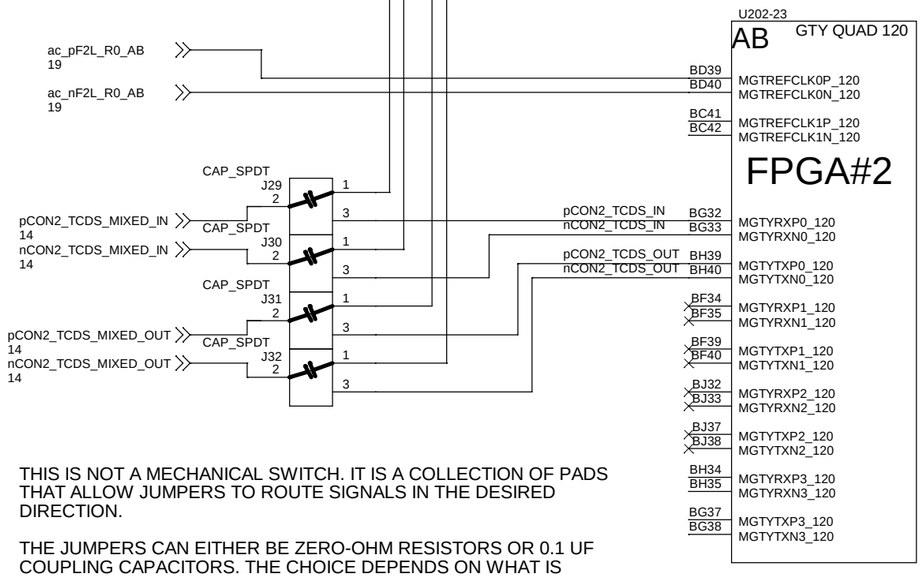
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

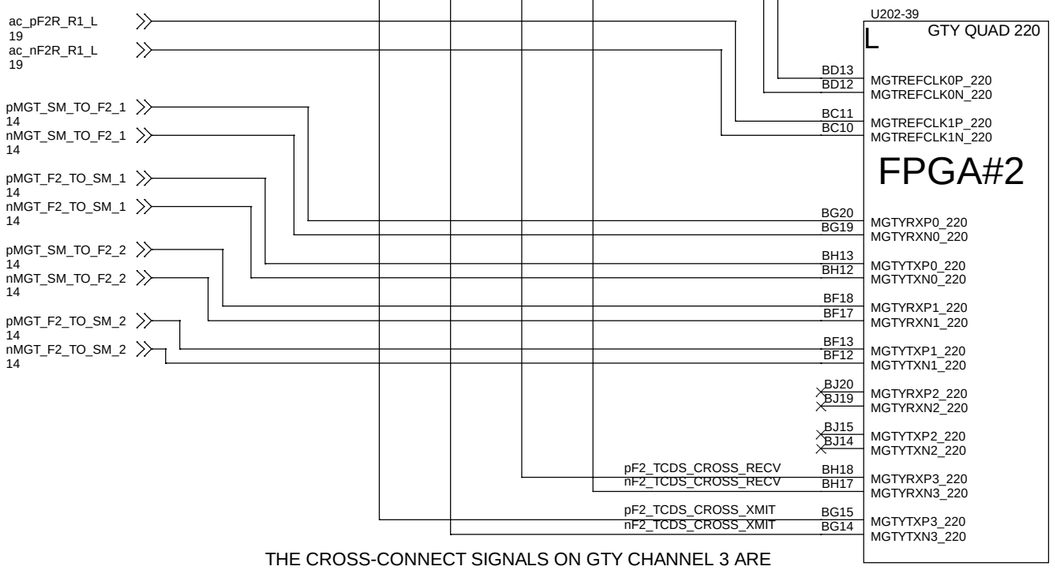
THESE QUADS ARE DEDICATED TO TCDS SIGNALS. TCDS NETS COME FROM THE SERVICE BOARD HIGH SPEED CONNECTORS





C2500 0.1 UF 0402
C2501 0.1 UF 0402
C2502 0.1 UF 0402
C2503 0.1 UF 0402





THIS IS NOT A MECHANICAL SWITCH. IT IS A COLLECTION OF PADS THAT ALLOW JUMPERS TO ROUTE SIGNALS IN THE DESIRED DIRECTION.

THE JUMPERS CAN EITHER BE ZERO-OHM RESISTORS OR 0.1 UF COUPLING CAPACITORS. THE CHOICE DEPENDS ON WHAT IS INSTALLED IN THE PATH ON THE SM.

THE "SWITCH" IS SHOWN IN "UP" THE POSITION, WHERE FPGA#1 IS THE TCDS ENDPOINT. "TTC-TYPE" DATA IS SENT FROM FPGA#1 TO THE ZYNQ ON THE SM USING THE "TCDS_TO_ZYNQ" CONNECTION. "TTS-TYPE" RESPONSE DATA COMES IN FROM THE ZYNQ ON THE SM USING THE "TCDS_FROM_ZYNQ" CONNECTION. FPGA#1 MERGES IT INTO THE "TTS" RESPONSE DATA FROM FPGA#1 AND FPGA#2.

WHEN THE SM IS THE TCDS ENDPOINT, THE SWITCH IS FLIPPED TO THE "DOWN" POSITION. "TTC-TYPE" DATA COMES IN FROM THE ZYNQ ON THE SM USING THE "CON2_TCDS_IN" CONNECTION AND IS ROUTED TO FPGA#2. "TTS-TYPE" DATA FROM FPGA#2 IS SENT TO THE ZYNQ ON THE SM USING THE "CON2_TCDS_OUT" CONNECTION.

THE CROSS-CONNECT SIGNALS ON GTY CHANNEL 3 ARE USED TO TRANSFER TCDS DATA FROM THE FPGA#1 MASTER TO THE FPGA#2 SLAVE. THEY ARE NOT USED WHEN THE ZYNQ ON THE SM IS THE TCDS ENDPOINT.

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.11: FPGA#1 AND FPGA#2 TCDS QUADS AB		
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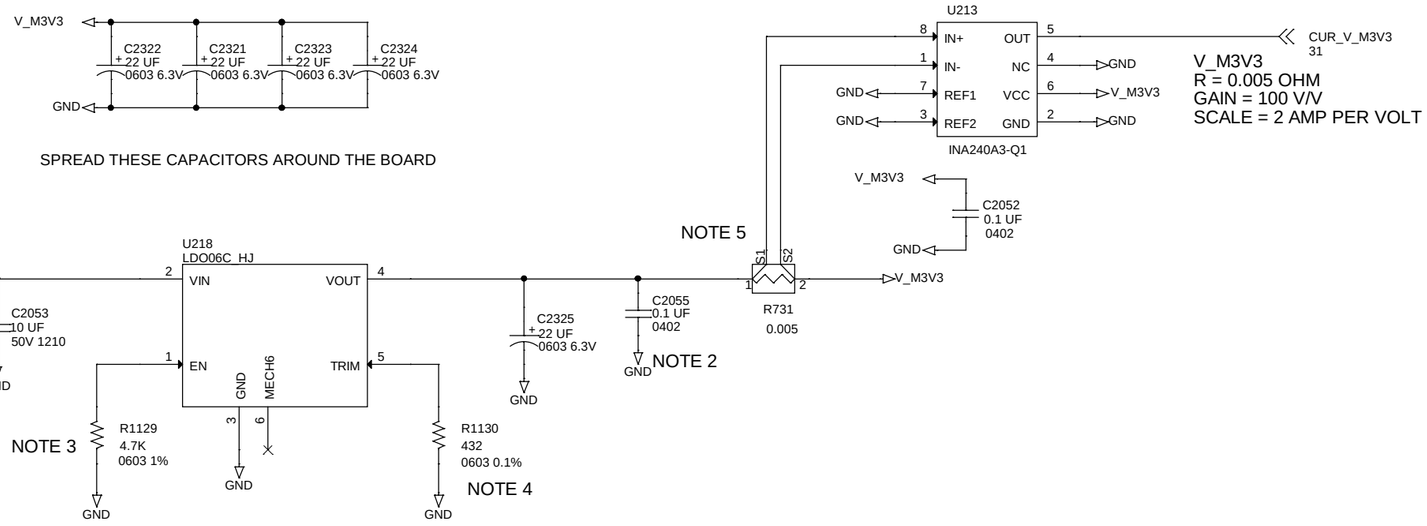
3.01: POWER MANAGEMENT M3V3



GENERAL NOTES:

V_M3V3 IS THE "MANAGEMENT" POWER. IT PROVIDES POWER TO THE POWER SEQUENCING CIRCUIT. IT IS ALWAYS ON WHEN +12V IS SUPPLIED TO THE BOARD.

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

NOTES:

NOTE 1 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL INPUT CAPACITORS.

NOTE 2 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL OUTPUT CAPACITORS.

NOTE 3 UNDERVOLTAGE LOCKOUT RESISTOR
R = 14.81 * (6.81 / ((6.81*Ven) - 18.16))
A 4.7K RESISTOR GIVES 5.8 VOLTS MINIMUM TURNON VOLTAGE

NOTE 4 OUTPUT SETPOINT RESISTOR
R = 1.182 / (VOUT - 0.591)
FOR 3.3 VOLTS, R = 436 OHMS (IF R=432 THEN V=3.327)

NOTE 5 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 5 MILLIOHMS AND A CURRENT OF 5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LDO06C REGULATOR IS RATED FOR 6 AMPS. IF MORE THAN 5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 5 MILLIOHMS.

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.01: POWER MANAGEMENT M3V3		
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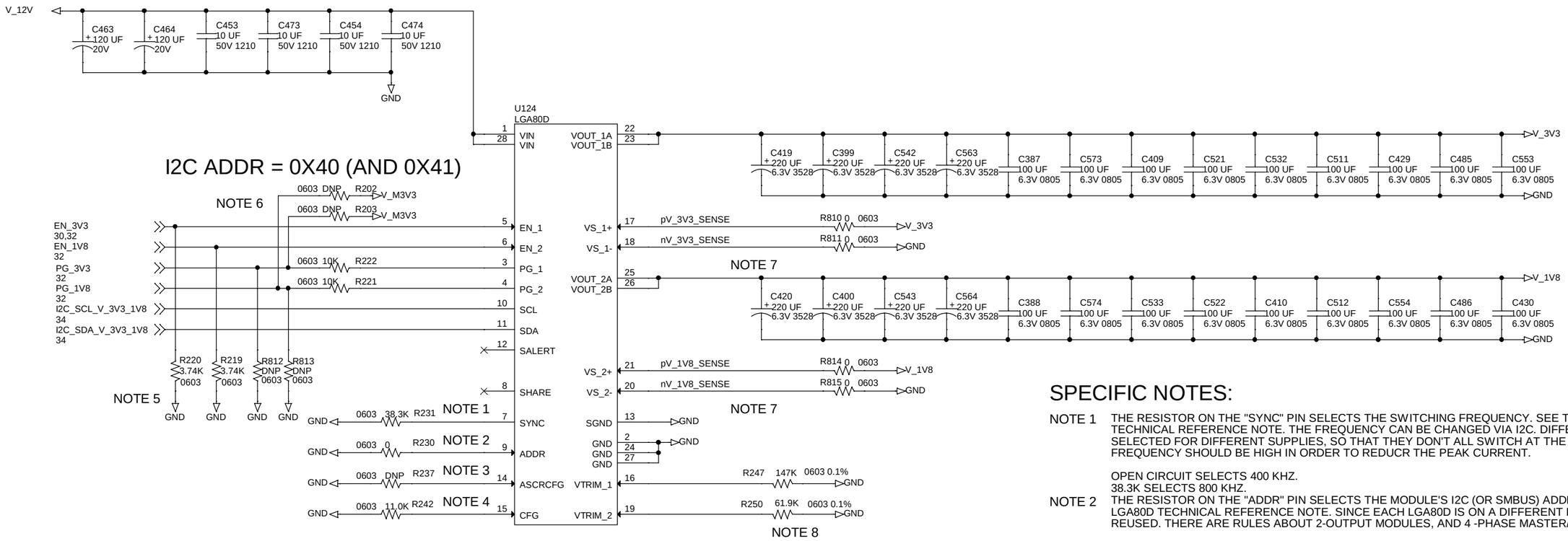
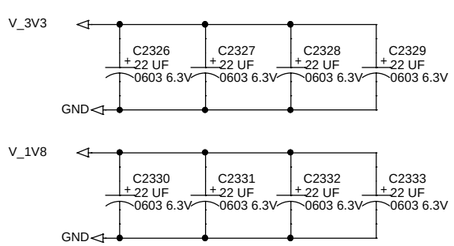
3.02: POWER GLOBAL 3.3V AND 1.8V





NOTE 9

SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME. FOR 3.3V, THE FREQUENCY SHOULD BE HIGH IN ORDER TO REDUCR THE PEAK CURRENT.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=11K SELECTS 2-OUTPUT @ 35A(avg)/45A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 147K FOR 3.3V
RSET = 61.9K FOR 1.8V

NOTE 9 SPREAD THESE CAPACITORS AROUND THE BOARD

GENERAL NOTES:

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.02: POWER GLOBAL 3.3V AND 1.8V		
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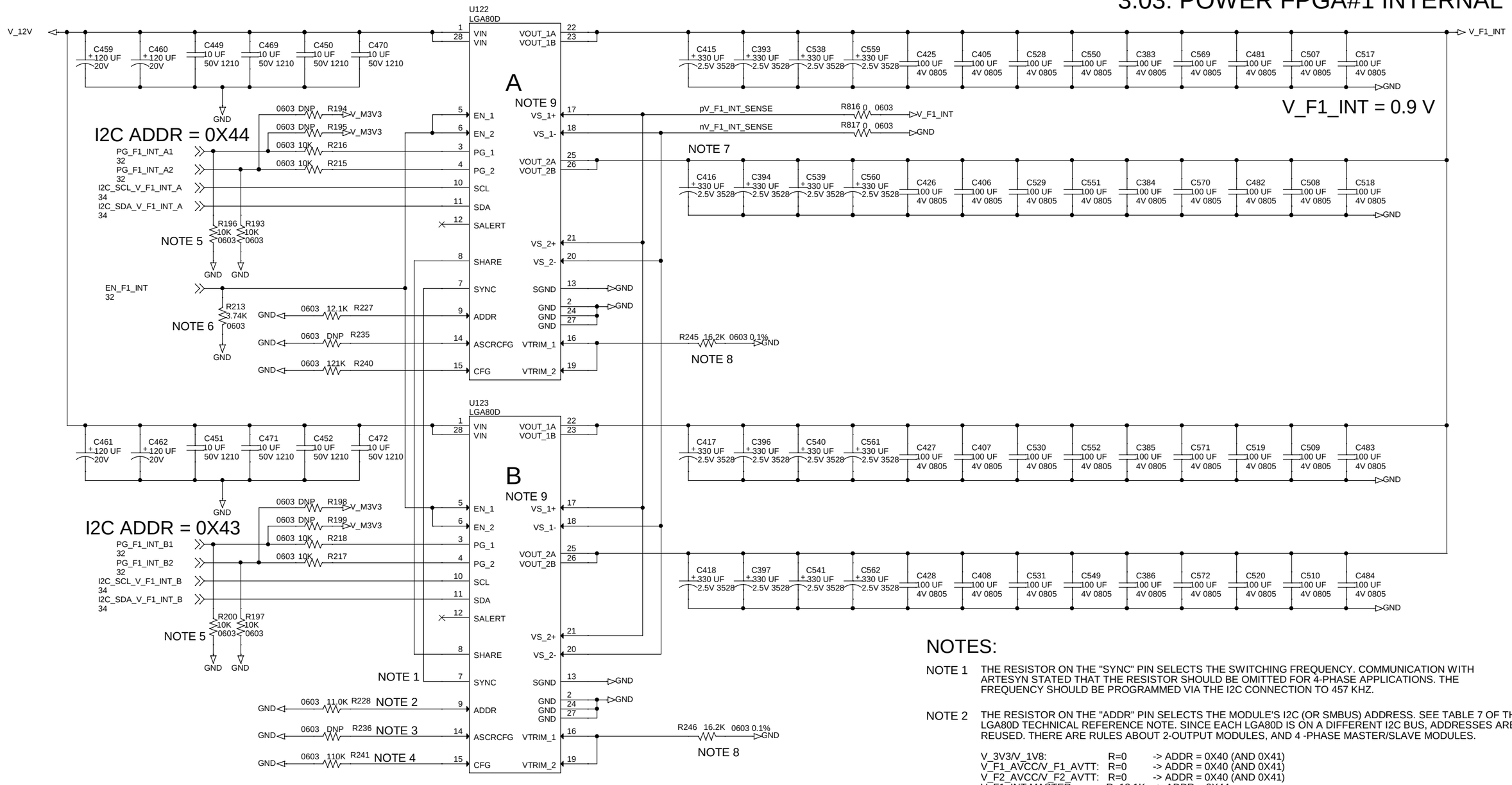
3.03: POWER FPGA#1 INTERNAL



NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 16.2K FOR 0.85V

NOTE 9 THE MASTER IS LABELED "A".
THE SLAVE IS LABELED "B".

NOTE 10 PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. COMMUNICATION WITH ARTESYN STATED THAT THE RESISTOR SHOULD BE OMITTED FOR 4-PHASE APPLICATIONS. THE FREQUENCY SHOULD BE PROGRAMMED VIA THE I2C CONNECTION TO 457 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 10K.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 110K ON THE MASTER AND 121K ON THE SLAVE FOR 4-PHASE @ 45A(avg)/50A(ovc) EACH.

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.03: POWER FPGA#1 INTERNAL		
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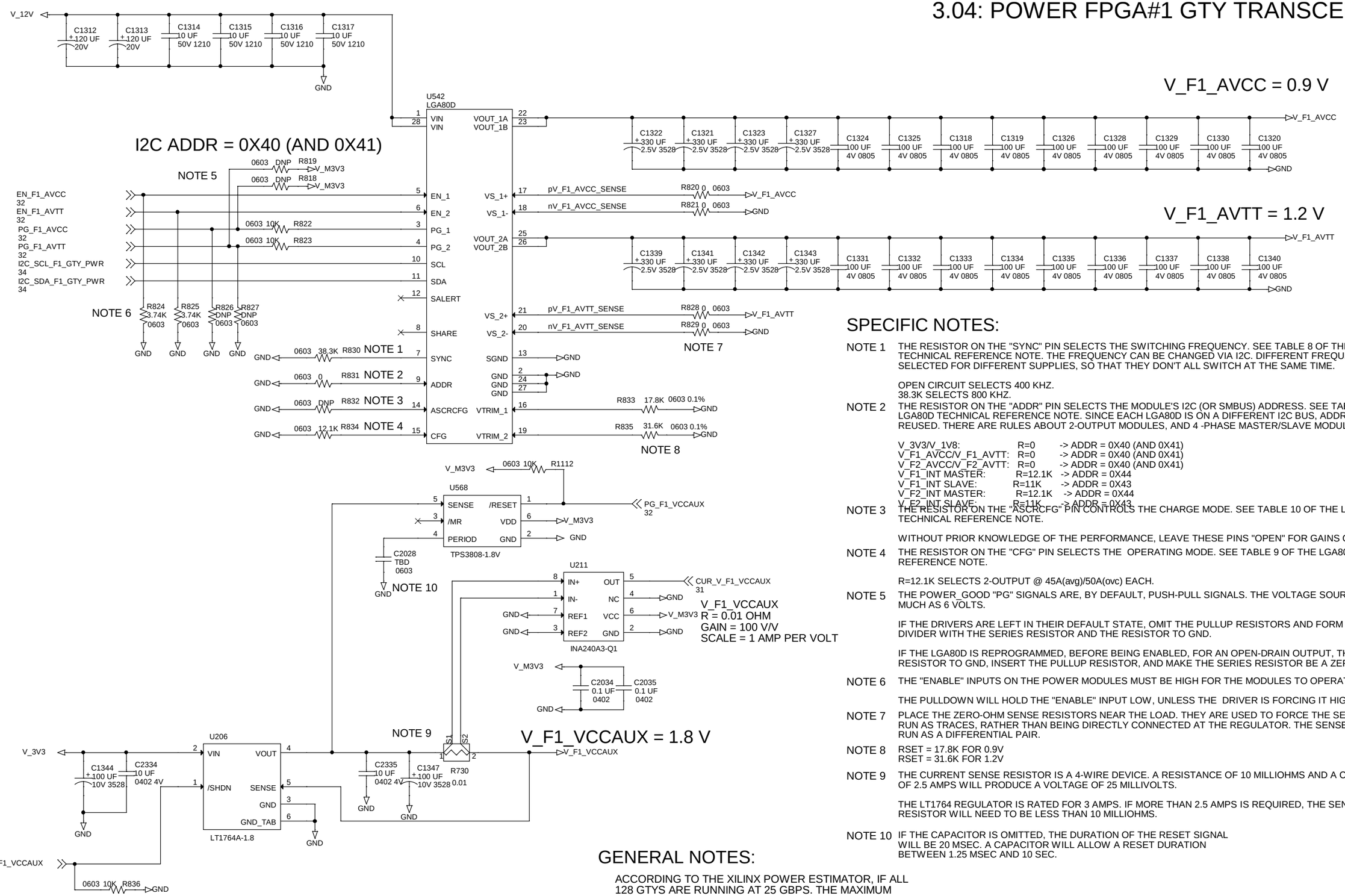
3.04: POWER FPGA#1 GTY TRANSCEIVER



SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=12.1K SELECTS 2-OUTPUT @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 17.8K FOR 0.9V
RSET = 31.6K FOR 1.2V

NOTE 9 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 10 MILLIOHMS AND A CURRENT OF 2.5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LT1764 REGULATOR IS RATED FOR 3 AMPS. IF MORE THAN 2.5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 10 MILLIOHMS.

NOTE 10 IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

GENERAL NOTES:

ACCORDING TO THE XILINX POWER ESTIMATOR, IF ALL 128 GTYS ARE RUNNING AT 25 GBPS. THE MAXIMUM CURRENT DRAWS WILL BE:
GTY_AVCC = 11.5 AMPS
GTY_AVTT = 30 AMPS
GTY_VCCAUX = 2.5 AMPS

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.04: POWER FPGA#1 GTY TRANSCEIVER		
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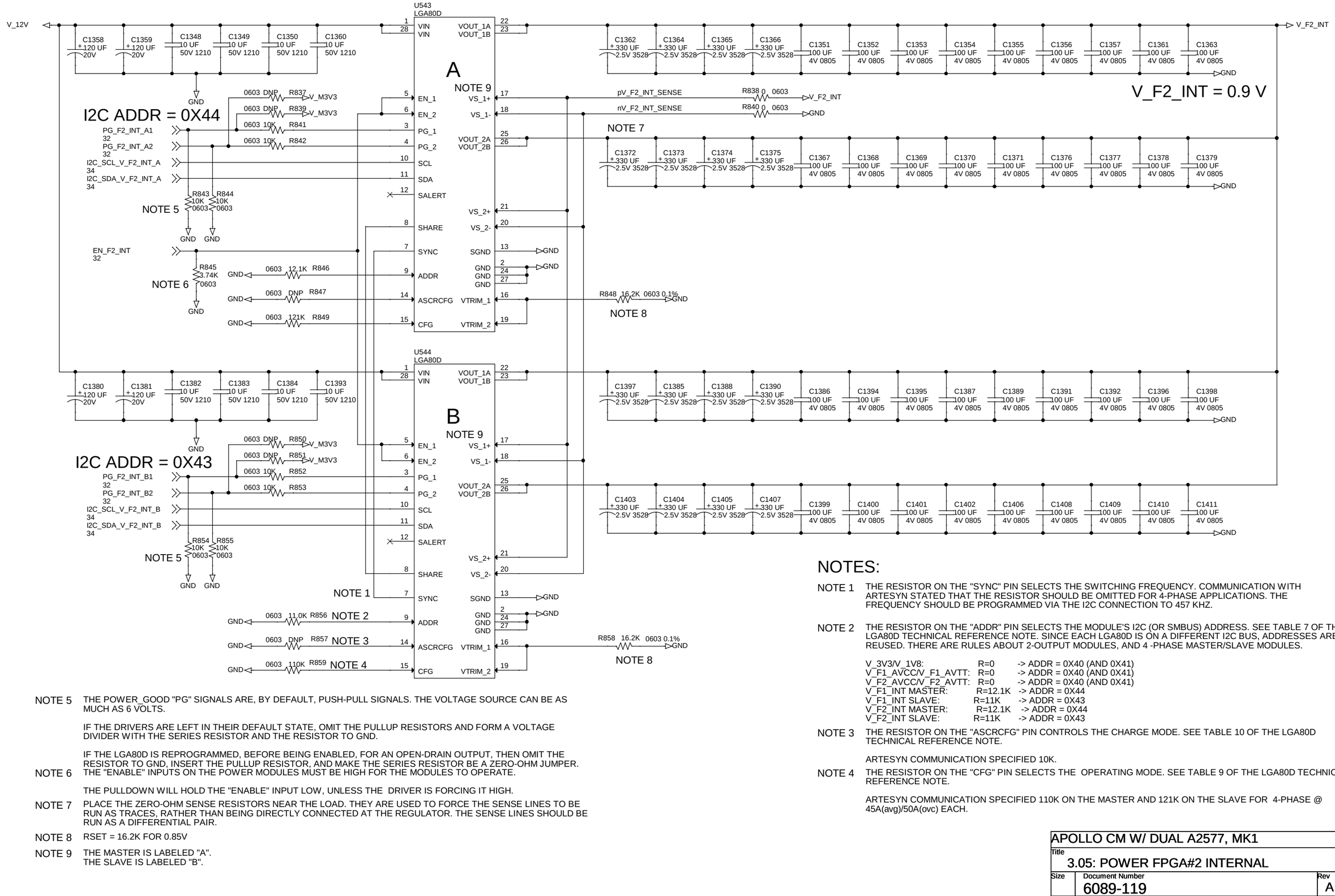
3.05: POWER FPGA#2 INTERNAL



NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 16.2K FOR 0.85V

NOTE 9 THE MASTER IS LABELED "A".
THE SLAVE IS LABELED "B".

NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. COMMUNICATION WITH ARTESYN STATED THAT THE RESISTOR SHOULD BE OMITTED FOR 4-PHASE APPLICATIONS. THE FREQUENCY SHOULD BE PROGRAMMED VIA THE I2C CONNECTION TO 457 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 10K.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 110K ON THE MASTER AND 121K ON THE SLAVE FOR 4-PHASE @ 45A(avg)/50A(ovc) EACH.

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.05: POWER FPGA#2 INTERNAL		
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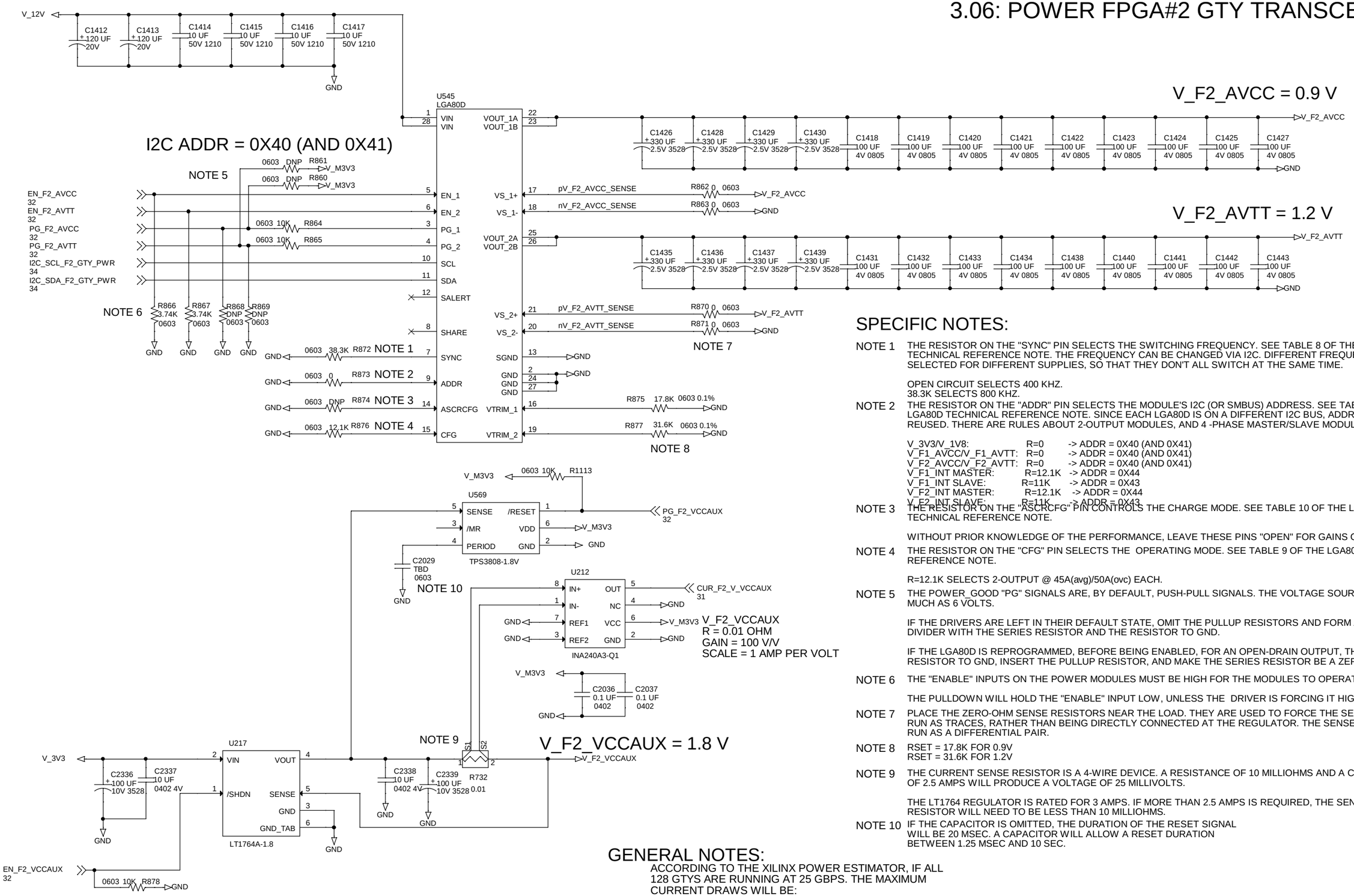
3.06: POWER FPGA#2 GTY TRANSCEIVER



SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=12.1K SELECTS 2-OUTPUT @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 17.8K FOR 0.9V
RSET = 31.6K FOR 1.2V

NOTE 9 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 10 MILLIOHMS AND A CURRENT OF 2.5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LT1764 REGULATOR IS RATED FOR 3 AMPS. IF MORE THAN 2.5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 10 MILLIOHMS.

NOTE 10 IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

GENERAL NOTES:

ACCORDING TO THE XILINX POWER ESTIMATOR, IF ALL 128 GTYS ARE RUNNING AT 25 GBPS. THE MAXIMUM CURRENT DRAWS WILL BE:
GTY_AVCC = 11.5 AMPS
GTY_AVTT = 30 AMPS
GTY_VCCAUX = 2.5 AMPS

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.06: POWER FPGA#2 GTY TRANSCEIVER		
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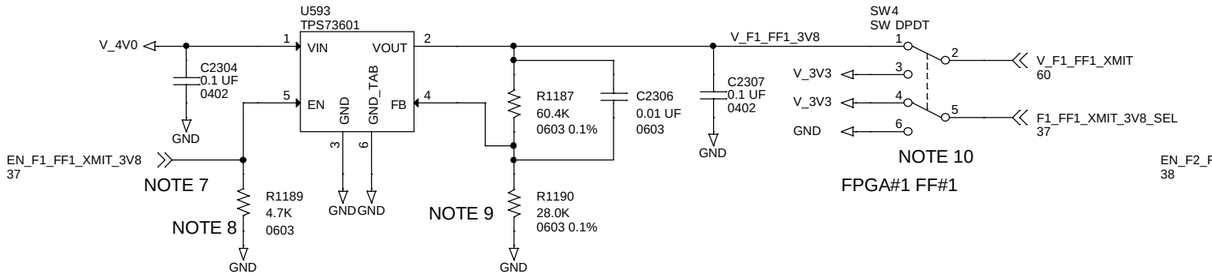
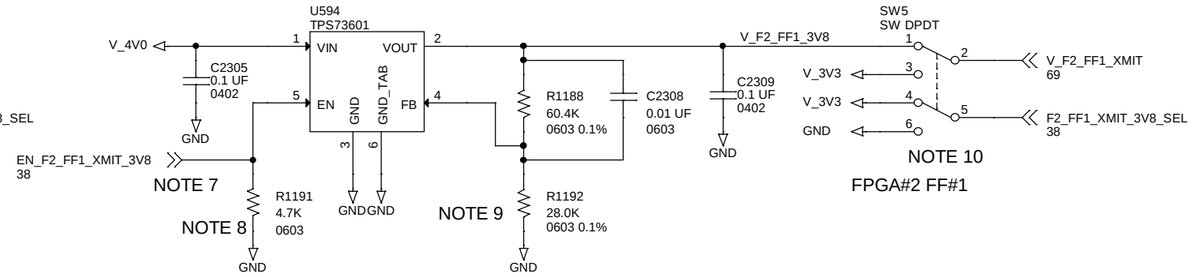
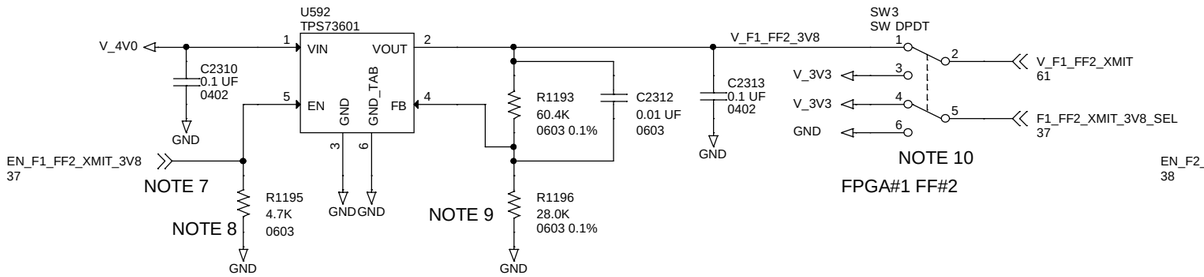
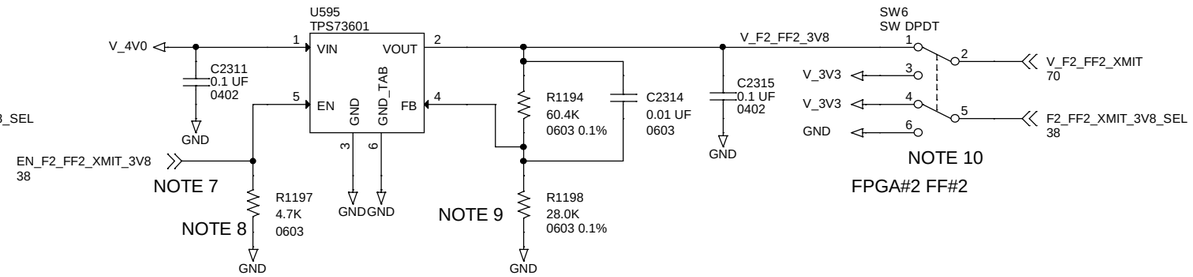
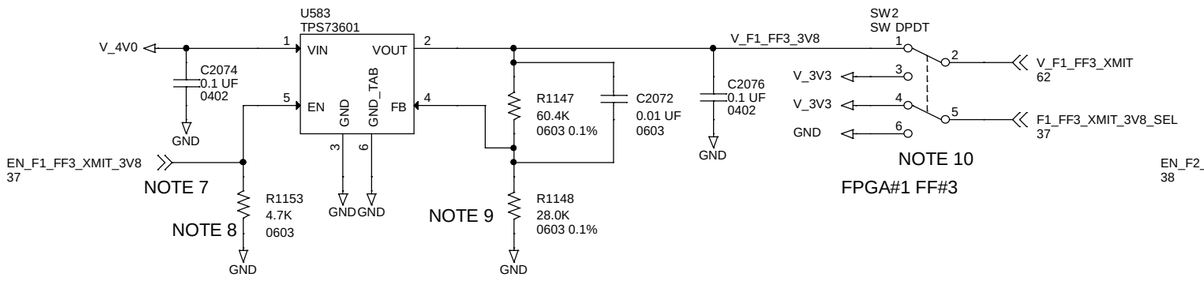
3.07: POWER FOR FF X12 XMIT

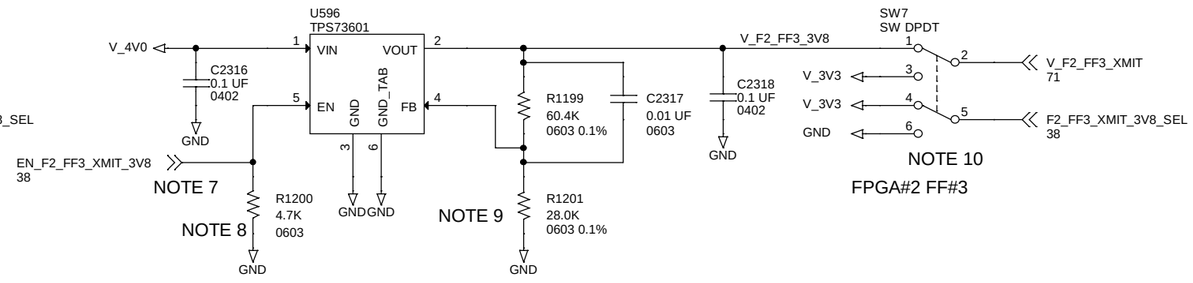




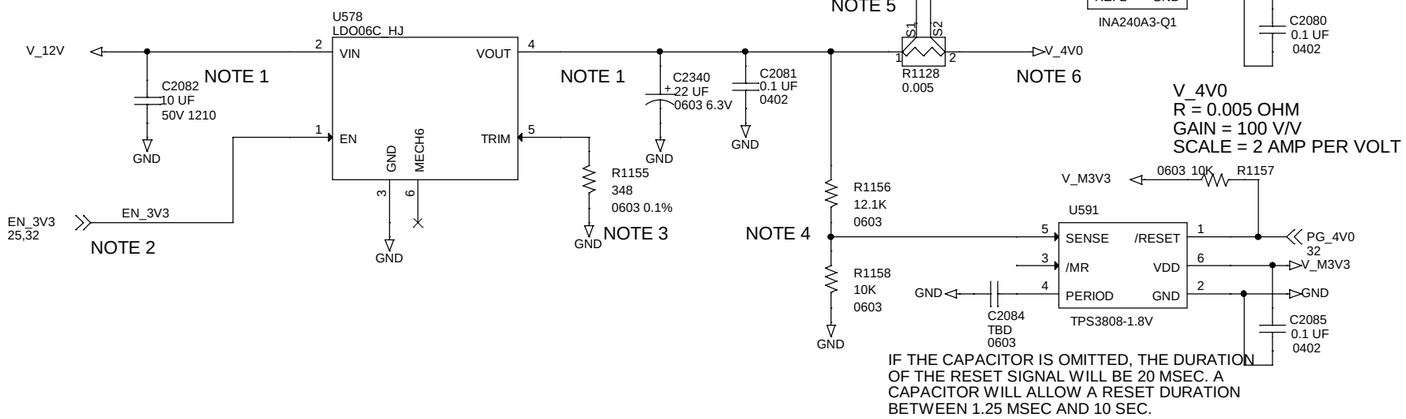








V_4V0 IS USED TO SUPPLY THE 3.8 VOLT REGULATORS FOR THE 12-LANE FIREFLY TRANSMITTERS.



NOTE 1 THE LDO06C DOES NOT REQUIRE ANY EXTERNAL INPUT OR OUTPUT CAPACITORS.

NOTE 2 THE LDO06C IS ENABLED AT THE SAME TIME AS THE BOARD-WIDE 3.3V SUPPLY.

NOTE 3 LDO06C OUTPUT SETPOINT RESISTOR
R = 1.182 / (VOUT - 0.591)
FOR 4.0 VOLTS, R=347 OHMS

NOTE 4 THE MONITORING CHIP EXPECTS 1.8 VOLTS AT THE INPUT, SO THE 4.0 VOLTS IS DIVIDED.

NOTE 5 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 5 MILLIOHMS AND A CURRENT OF 5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LDO06C REGULATOR IS RATED FOR 6 AMPS. IF MORE THAN 5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 5 MILLIOHMS.

NOTE 6 V_4V0 IS ONLY CONNECTED ONTHIS PAGE, EXCEPT FOR MEASURING BY THE MCU ADC.

NOTE 7 THE TPS73601 REGULATOR SHOULD NOT BE ENABLED UNTIL THE FIREFLY TRANSMITTER TYPE HAS BEEN DETERMINED AND THE VOLTAGE SWITCH IS FOUND TO BE IN THE CORRECT POSITION.

NOTE 8 PULLDOWNS ARE NEEDED ON THE CONTROL INPUTS, SINCE THE I2C DRIVER DEVICES NEED TO BE CONFIGURED AS OUTPUTS BEFORE THEY CAN CONTOL THE LOGIC LEVEL. THE I2C DRIVERS HAVE A BUILT-IN 100K PULLUP.

NOTE 9 THE TPS73601 OUTPUT VOLTAGE IS CALCULATED BY:
VOUT = 1.204 * ((Rtop+Rbot)/Rbot)
IF Rtop = 60.4k AND Rbot=28K, THEN VOUT = 3.8 V

NOTE 10 THE SWITCH IS SHOWN IN THE POSITION TO PROVIDE 3.8 VOLTS TO THE FIREFLY TRANSMITTER. THE "*_3V8_SEL" SIGNAL WILL BE HIGH.

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.07: POWER FOR FF X12 XMIT		
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3.08: VOLT, CUR, TEMP MEASURE

TEST POINTS TO
MEASURE VOLTAGES

THE 12 VOLT SUPPLY
LEVEL IS DIVIDED BY 6

THE M3.3 VOLT SUPPLY
LEVEL IS DIVIDED BY 2

THE 3.3 VOLT SUPPLY
LEVEL IS DIVIDED BY 2

THE 4.0 VOLT SUPPLY
LEVEL IS DIVIDED BY 2

U540-5
TM4C1290NCPDT_NEW

THE VALUE OF "MCU_VREFA" SETS THE VOLTAGE THAT WILL CORRESPOND TO THE ADC FULL SCALE VALUE OF 4095. THE MINIMUM VOLTAGE IS 2.4 VOLTS.

THIS DESIGN USES 2.5 VOLTS FOR FULL SCALE.

U576
LT1790-2.5V

THE ANTI-ALIASING CUTOFF FREQUENCY IS 15.9 KHZ

A 16 MHZ ADC CLOCK PROVIDES A SAMPLING RATE OF 1 MEGA-SAMPLES PER SECOND. IF ALL 20 ADC CHANNELS ARE USED, THE SAMPLE RATE PER CHANNEL IS 50 KILO-SAMPLES PER SECOND, AND THE NYQUIST FREQUENCY IS 25 KHZ.

THE MAXIMUM SOURCE IMPEDANCE FEEDING THE ADC INPUTS IS 500 OHMS.

APOLLO CM W/ DUAL A2577, MK1	
Title	3.08: VOLT, CUR, TEMP MEASURE
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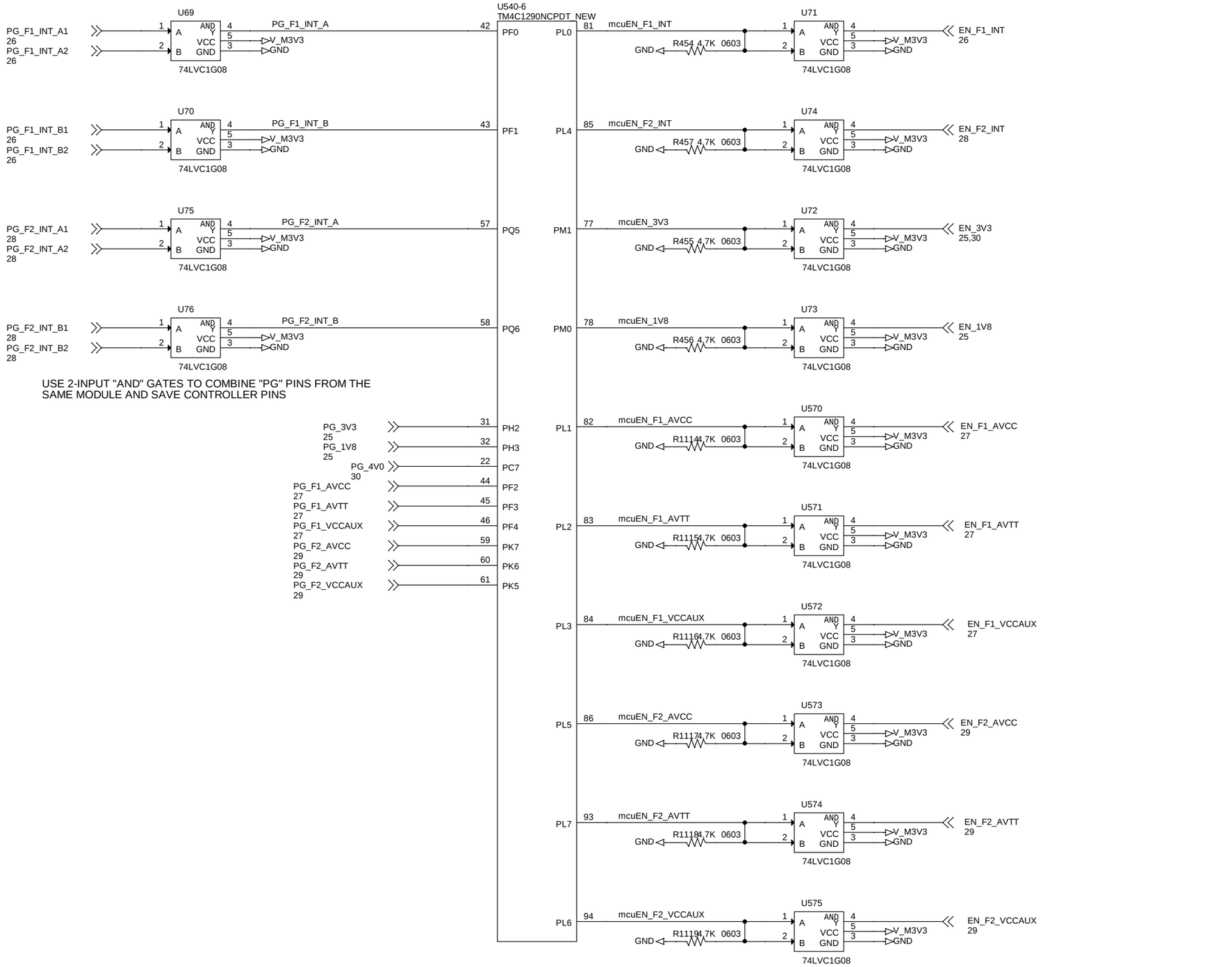
3.09: POWER CONTROL



APOLLO CM W/ DUAL A2577, MK1		
Title: 3.09: POWER CONTROL		
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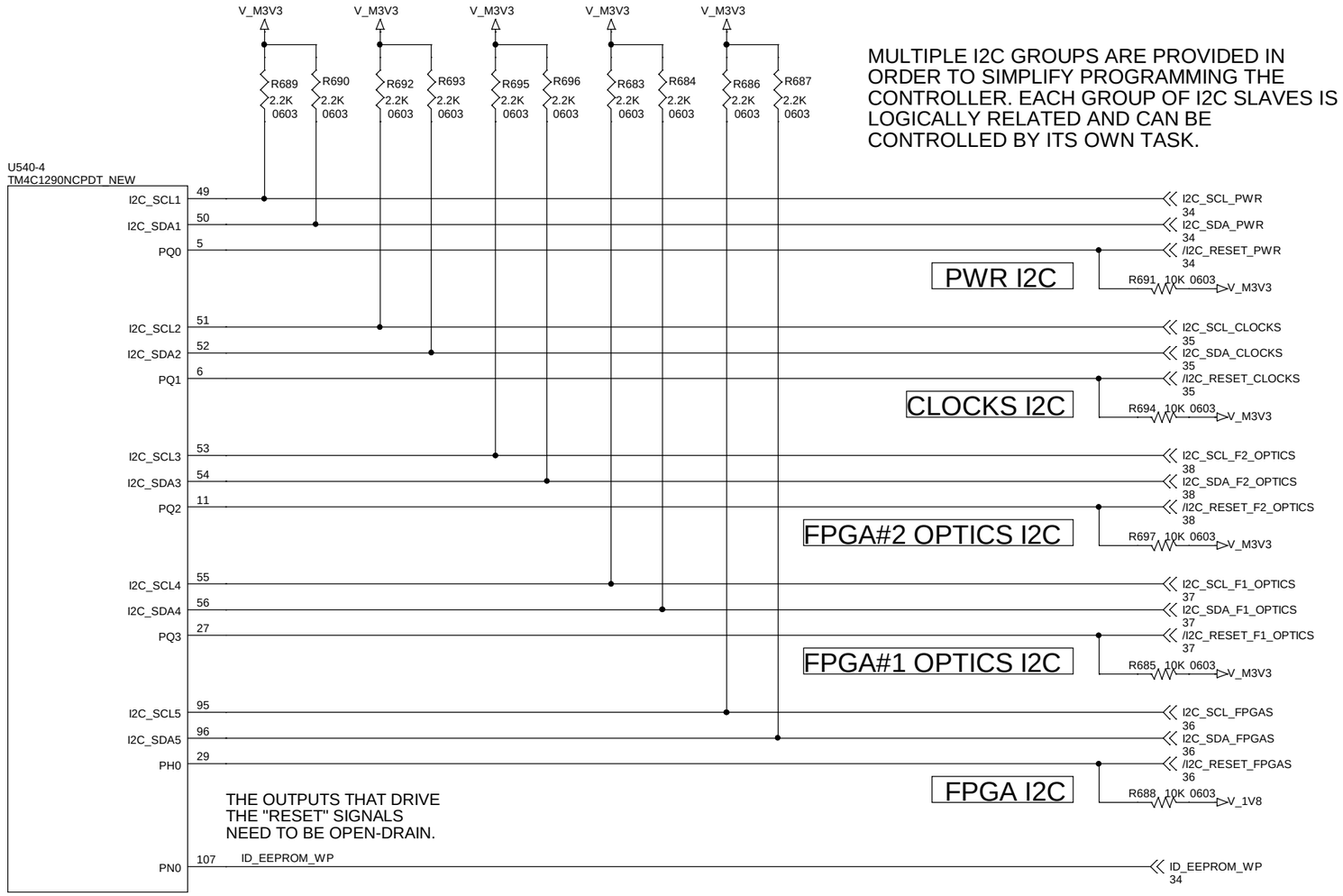
4.01: I2C CONTROLLER



MULTIPLE I2C GROUPS ARE PROVIDED IN ORDER TO SIMPLIFY PROGRAMMING THE CONTROLLER. EACH GROUP OF I2C SLAVES IS LOGICALLY RELATED AND CAN BE CONTROLLED BY ITS OWN TASK.

APOLLO CM W/ DUAL A2577, MK1			
Title: 4.01: I2C CONTROLLER			
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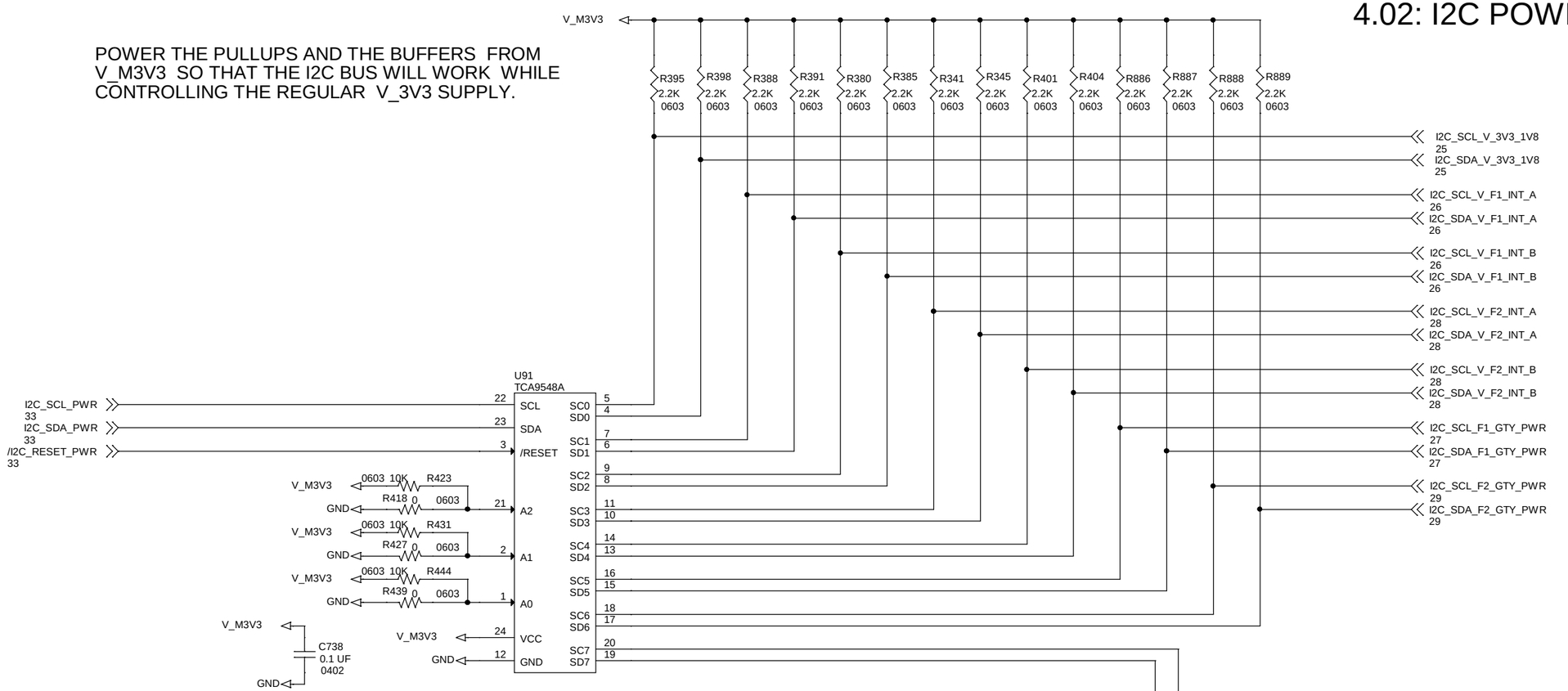
4.02: I2C POWER CONTROL

POWER THE PULLUPS AND THE BUFFERS FROM V_M3V3 SO THAT THE I2C BUS WILL WORK WHILE CONTROLLING THE REGULAR V_3V3 SUPPLY.



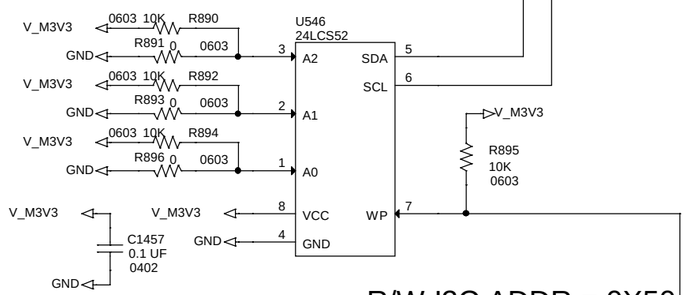
I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

THIS EEPROM IS FOR STORING UNCHANGING INFORMATION, LIKE SERIAL NUMBERS OR OTHER BOARD IDENTIFIERS.



R/W I2C ADDR = 0X50

WP I2C ADDR = 0X30

24LCS52 I2C ADDRESS:
READ OR WRITE
1 0 1 0 A2 A1 A0
RANGE: 0X50 TO 0X57
WRITE-PROTECT REGISTER
0 1 1 0 A2 A1 A0

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

ID_EEPROM_WP 33

APOLLO CM W/ DUAL A2577, MK1		
Title: 4.02: I2C POWER CONTROL		
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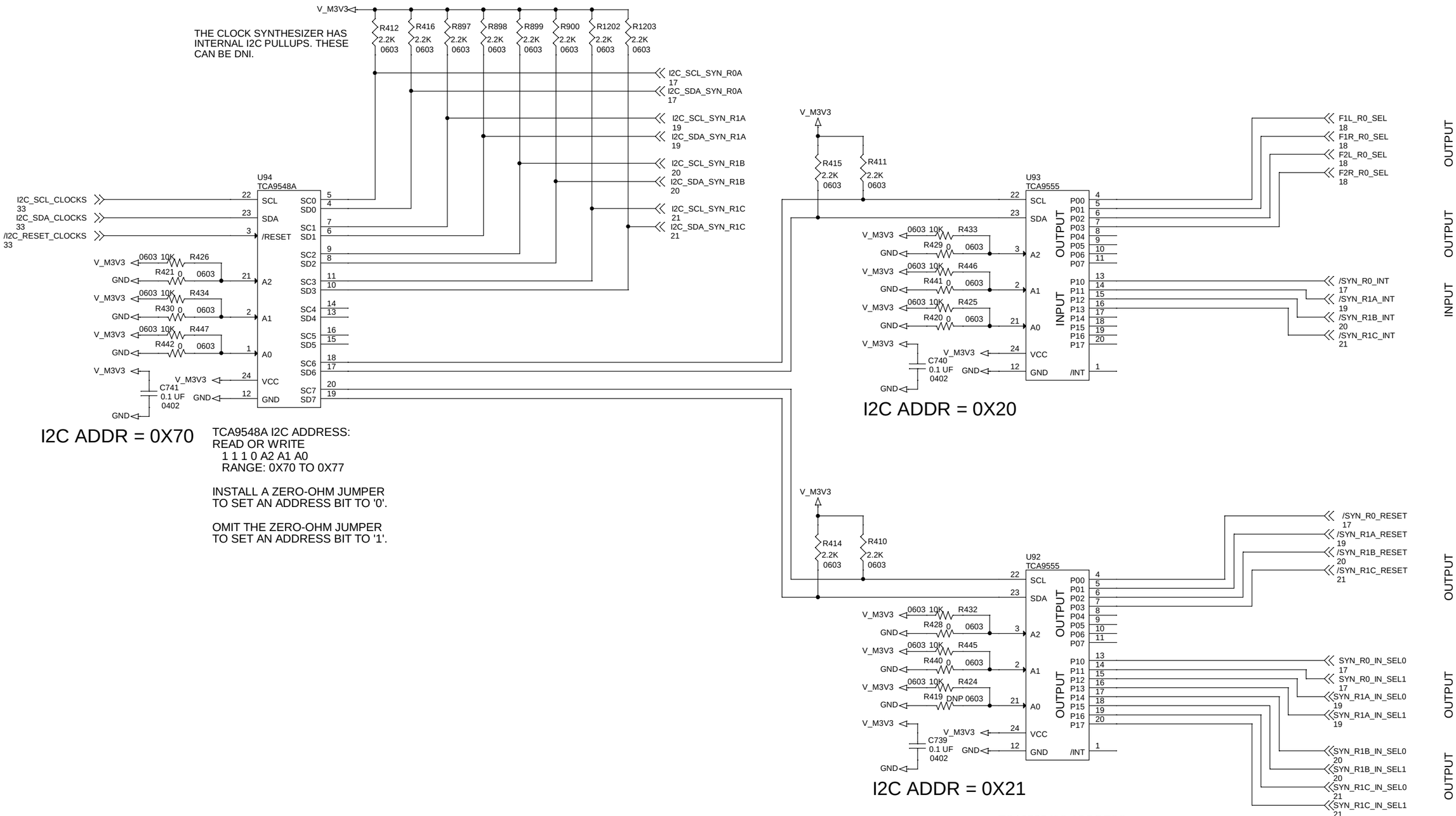
4.03: I2C CLOCK CONTROL



APOLLO CM W/ DUAL A2577, MK1		
Title: 4.03: I2C CLOCK CONTROL		
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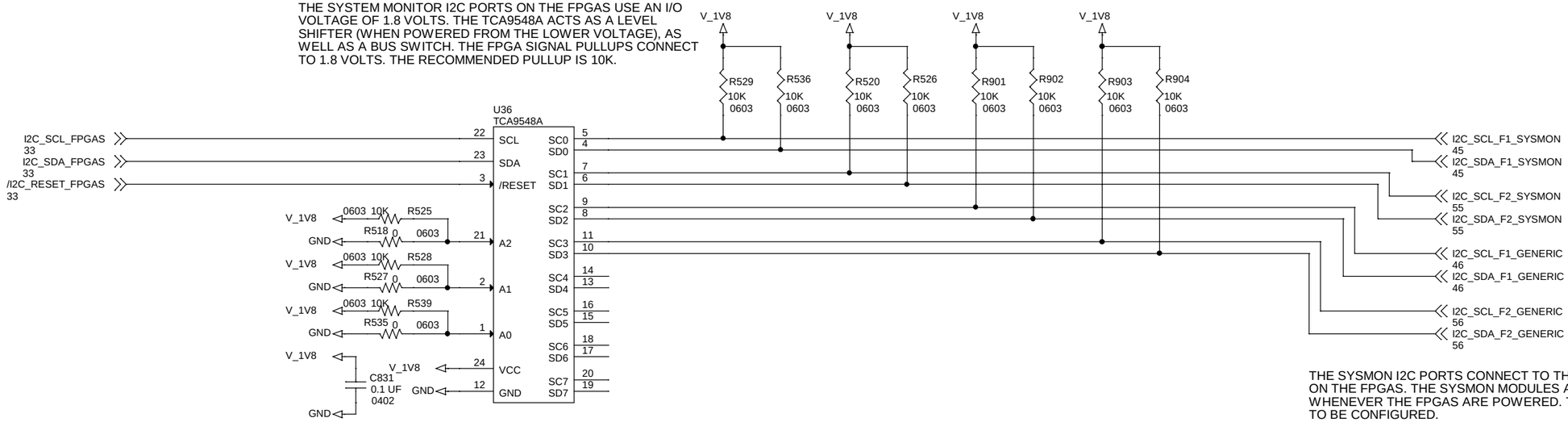
4.04: I2C FPGA INTERNALS

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER (WHEN POWERED FROM THE LOWER VOLTAGE), AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS. THE RECOMMENDED PULLUP IS 10K.



I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

THE SYSMON I2C PORTS CONNECT TO THE SYSMON MODULE PINS ON THE FPGAS. THE SYSMON MODULES ARE AVAILABLE WHENEVER THE FPGAS ARE POWERED. THE FPGAS DO NOT HAVE TO BE CONFIGURED.

THE GENERIC I2C PORTS CONNECT TO I2C MODULES THAT ARE LOADED AS PART OF THE CONFIGURATION PROCESS. THEY ARE NOT AVAILABLE BEFORE THE FPGA HAS BEEN CONFIGURED.

THE GENERIC MODULES HAVE MORE CAPABILITY THAN THE SYSMON MODULES.

A2	A1	A0	I2C BUS SLAVE ADDRESS
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

APOLLO CM W/ DUAL A2577, MK1

Title: 4.04: I2C FPGA INTERNALS

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4.05: I2C FPGA#1 OPTICS

I2C_SCL_F1_OPTICS 33
I2C_SDA_F1_OPTICS 33
/I2C_RESET_F1_OPTICS 33

U100 TCA9548A

SCL, SDA, /RESET, A2, A1, A0, VCC, GND
SC0/SD0, SC1/SD1, SC2/SD2, SC3/SD3, SC4/SD4, SC5/SD5, SC6/SD6, SC7/SD7

V_M3V3 — 0603 10K R390; R387 0 0603 — GND — A2
V_M3V3 — 0603 10K R396; R393 0 0603 — GND — A1
V_M3V3 — 0603 10K R402; R399 0 0603 — GND — A0
V_M3V3 — C725 0.1 UF 0402 — GND — VCC

I2C_SCL_F1_FF1_XMIT 60
I2C_SDA_F1_FF1_XMIT 60
I2C_SCL_F1_FF1_RECV 60
I2C_SDA_F1_FF1_RECV 60
I2C_SCL_F1_FF2_XMIT 61
I2C_SDA_F1_FF2_XMIT 61
I2C_SCL_F1_FF2_RECV 61
I2C_SDA_F1_FF2_RECV 61
I2C_SCL_F1_FF3_XMIT 62
I2C_SDA_F1_FF3_XMIT 62
I2C_SCL_F1_FF3_RECV 62
I2C_SDA_F1_FF3_RECV 62

I2C ADDR = 0X70

V_M3V3 — R383 2.2K 0603; R344 2.2K 0603

U102 TCA9555

SCL, SDA, A2, A1, A0, VCC, GND, /INT
P00, P01, P02, P03, P04, P05, P06, P07, P10, P11, P12, P13, P14, P15, P16, P17

V_M3V3 — 0603 10K R346; R342 0 0603 — GND — A2
V_M3V3 — 0603 10K R384; R379 0 0603 — GND — A1
V_M3V3 — 0603 10K R339; R337 0 0603 — GND — A0
V_M3V3 — C723 0.1 UF 0402 — GND — VCC

/F1_FF1_XMIT_INT 60
/F1_FF1_RECV_INT 60
/F1_FF2_XMIT_INT 61
/F1_FF2_RECV_INT 61
/F1_FF3_XMIT_INT 62
/F1_FF3_RECV_INT 62

/F1_FF1_XMIT_PRESENT 60
/F1_FF1_RECV_PRESENT 60
/F1_FF2_XMIT_PRESENT 61
/F1_FF2_RECV_PRESENT 61
/F1_FF3_XMIT_PRESENT 62
/F1_FF3_RECV_PRESENT 62

INPUT

I2C ADDR = 0X20

U2 TCA9548A

SCL, SDA, /RESET, A2, A1, A0, VCC, GND
SC0/SD0, SC1/SD1, SC2/SD2, SC3/SD3, SC4/SD4, SC5/SD5, SC6/SD6, SC7/SD7

V_M3V3 — 0603 10K R669; R661 0 0603 — GND — A2
V_M3V3 — 0603 10K R707; R699 0 0603 — GND — A1
V_M3V3 — 0603 10K R721; R715 DNP 0603 — GND — A0
V_M3V3 — C973 0.1 UF 0402 — GND — VCC

I2C_SCL_F1_FF4_XCVR 63
I2C_SDA_F1_FF4_XCVR 63
I2C_SCL_F1_FF5_XCVR 64
I2C_SDA_F1_FF5_XCVR 64
I2C_SCL_F1_FF6_XCVR 65
I2C_SDA_F1_FF6_XCVR 65
I2C_SCL_F1_FF7_XCVR 66
I2C_SDA_F1_FF7_XCVR 66

I2C ADDR = 0X71

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

V_M3V3 — R655 2.2K 0603; R650 2.2K 0603

U1 TCA9555

SCL, SDA, A2, A1, A0, VCC, GND, /INT
P00, P01, P02, P03, P04, P05, P06, P07, P10, P11, P12, P13, P14, P15, P16, P17

V_M3V3 — 0603 10K R706; R698 0 0603 — GND — A2
V_M3V3 — 0603 10K R720; R714 0 0603 — GND — A1
V_M3V3 — 0603 10K R668; R660 DNP 0603 — GND — A0
V_M3V3 — C972 0.1 UF 0402 — GND — VCC

/F1_FF4_XCVR_INT 63
/F1_FF5_XCVR_INT 64
/F1_FF6_XCVR_INT 65
/F1_FF7_XCVR_INT 66
/F1_FF4_XCVR_PRESENT 63
/F1_FF5_XCVR_PRESENT 64
/F1_FF6_XCVR_PRESENT 65
/F1_FF7_XCVR_PRESENT 66
/F1_FF_RESET 60,61,62,63,64,65,66
EN_F1_FF1_XMIT_3V8 30
EN_F1_FF2_XMIT_3V8 30
EN_F1_FF3_XMIT_3V8 30
F1_FF1_XMIT_3V8_SEL 30
F1_FF2_XMIT_3V8_SEL 30
F1_FF3_XMIT_3V8_SEL 30

INPUT
OUTPUT
INPUT

I2C ADDR = 0X21

TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

APOLLO CM W/ DUAL A2577, MK1		
Title: 4.05: I2C FPGA#1 OPTICS		
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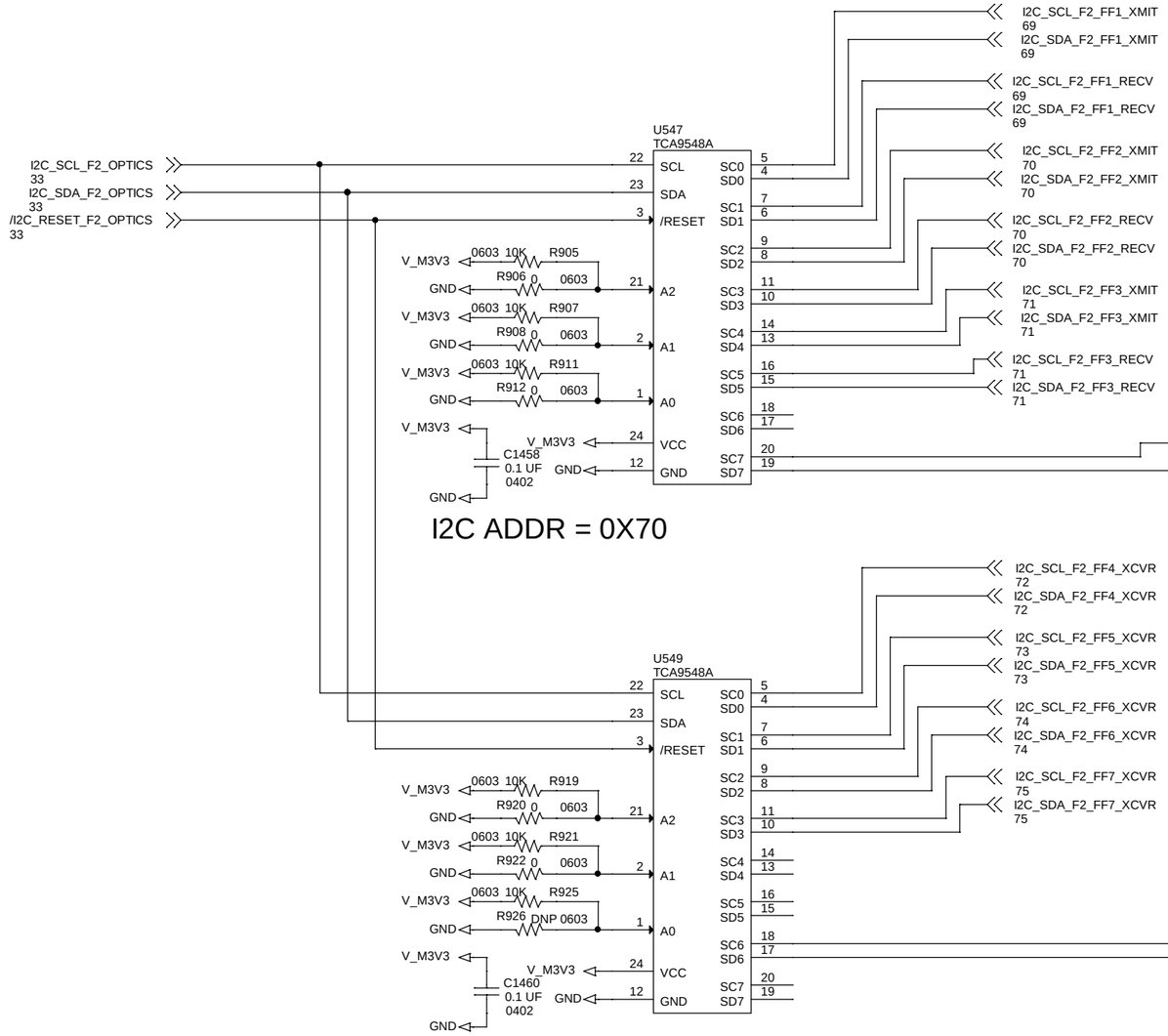
4.06: I2C FPGA#2 OPTICS



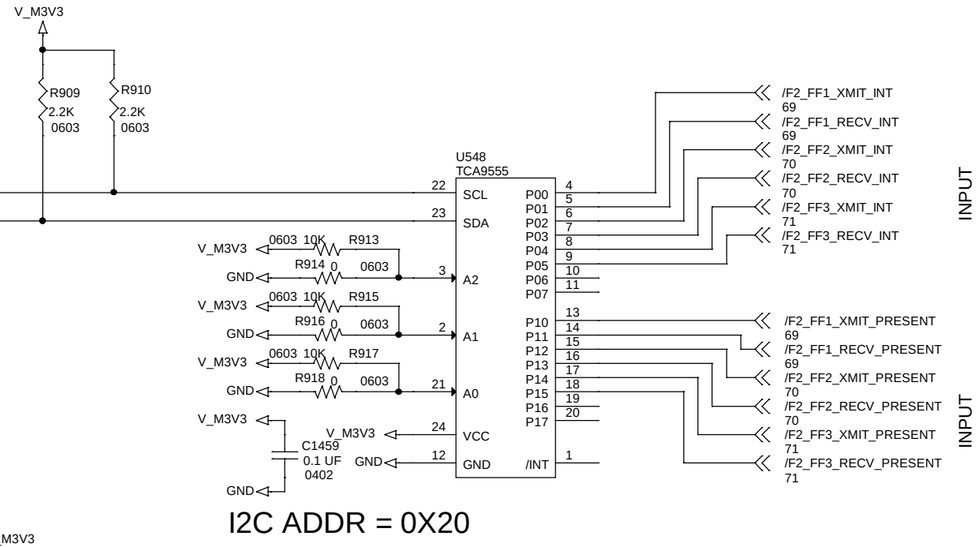
I2C ADDR = 0X70

I2C ADDR = 0X71

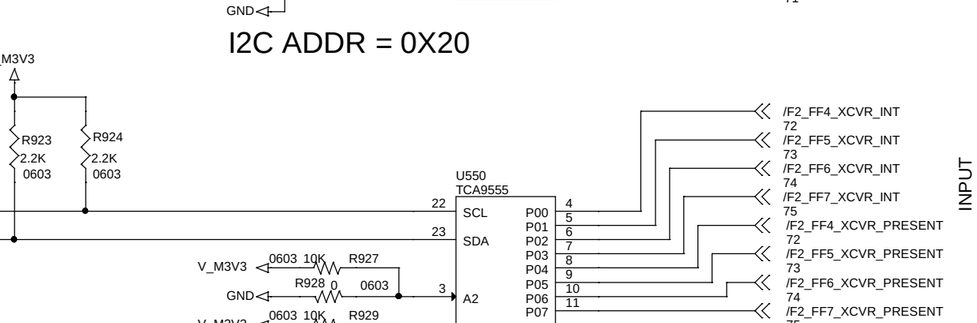
TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.



I2C ADDR = 0X20



I2C ADDR = 0X21

TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

APOLLO CM W/ DUAL A2577, MK1		
Title: 4.06: I2C FPGA#2 OPTICS		
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5.01: FPGA#1 GND

U201-1 FPGA_VU13P_A2577

A13	GND	GND	AE12
A16	GND	GND	AE16
A17	GND	GND	AE18
A18	GND	GND	AE20
A21	GND	GND	AE22
A26	GND	GND	AE24
A31	GND	GND	AE26
A34	GND	GND	AE28
A35	GND	GND	AE3
A36	GND	GND	AE30
A39	GND	GND	AE32
A4	GND	GND	AE34
A43	GND	GND	AE36
A45	GND	GND	AE38
A48	GND	GND	AE4
A7	GND	GND	AE40
A9	GND	GND	AE43
AA12	GND	GND	AE47
AA14	GND	GND	AE48
AA16	GND	GND	AE49
AA18	GND	GND	AE5
AA20	GND	GND	AE9
AA22	GND	GND	AF1
AA24	GND	GND	AF10
AA26	GND	GND	AF12
AA28	GND	GND	AF15
AA3	GND	GND	AF17
AA30	GND	GND	AF19
AA32	GND	GND	AF2
AA34	GND	GND	AF21
AA36	GND	GND	AF23
AA38	GND	GND	AF25
AA4	GND	GND	AF27
AA40	GND	GND	AF29
AA43	GND	GND	AF31
AA47	GND	GND	AF33
AA48	GND	GND	AF35
AA49	GND	GND	AF37
AA5	GND	GND	AF39
AA9	GND	GND	AF40
AB1	GND	GND	AF42
AB10	GND	GND	AF45
AB15	GND	GND	AF47
AB17	GND	GND	AF5
AB19	GND	GND	AF50
AB2	GND	GND	AF51
AB21	GND	GND	AF7
AB23	GND	GND	AG12
AB25	GND	GND	AG16
AB27	GND	GND	AG20
AB29	GND	GND	AG22
AB31	GND	GND	AG24
AB33	GND	GND	AG26
AB35	GND	GND	AG28
AB37	GND	GND	AG3
AB38	GND	GND	AG30
AB42	GND	GND	AG32
AB45	GND	GND	AG34
AB47	GND	GND	AG36
AB5	GND	GND	AG38
AB50	GND	GND	AG4
AB51	GND	GND	AG40
AB7	GND	GND	AG44
AC14	GND	GND	AG47
AC16	GND	GND	AG48
AC18	GND	GND	AG49
AC20	GND	GND	AG5
AC22	GND	GND	AG8
AC24	GND	GND	AH1
AC26	GND	GND	AH11
AC28	GND	GND	AH12
AC3	GND	GND	AH15
AC30	GND	GND	AH17
AC32	GND	GND	AH2
AC34	GND	GND	AH21
AC36	GND	GND	AH23
AC38	GND	GND	AH25
AC39	GND	GND	AH27
AC4	GND	GND	AH29
AC44	GND	GND	AH31
AC47	GND	GND	AH33
AC48	GND	GND	AH35
AC49	GND	GND	AH37
AC5	GND	GND	AH39
AC8	GND	GND	AH40
AD1	GND	GND	AH41
AD11	GND	GND	AH46
AD12	GND	GND	AH47
AD15	GND	GND	AH5
AD17	GND	GND	AH50
AD19	GND	GND	AH51
AD2	GND	GND	AH6
AD21	GND	GND	AJ14
AD23	GND	GND	AJ16
AD25	GND	GND	AJ20
AD27	GND	GND	AJ22
AD29	GND	GND	AJ24
AD31	GND	GND	AJ26
AD33	GND	GND	AJ28
AD35	GND	GND	AJ3
AD37	GND	GND	AJ30
AD39	GND	GND	AJ32
AD40	GND	GND	AJ34
AD41	GND	GND	AJ36
AD46	GND	GND	AJ38
AD47	GND	GND	AJ39
AD5	GND	GND	AJ47
AD50	GND	GND	AJ43
AD51	GND	GND	AJ48
AD6	GND	GND	AJ4

GND GND

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AJ49	GND	GND	AP42
AJ5	GND	GND	AP45
AJ9	GND	GND	AP47
AK1	GND	GND	AP5
AK10	GND	GND	AP50
AK15	GND	GND	AP51
AK17	GND	GND	AP7
AK2	GND	GND	AR12
AK21	GND	GND	AR14
AK23	GND	GND	AR22
AK25	GND	GND	AR24
AK27	GND	GND	AR26
AK29	GND	GND	AR28
AK31	GND	GND	AR3
AK33	GND	GND	AR30
AK35	GND	GND	AR38
AK37	GND	GND	AR4
AK38	GND	GND	AR40
AK42	GND	GND	AR44
AK45	GND	GND	AR47
AK47	GND	GND	AR48
AK5	GND	GND	AR49
AK50	GND	GND	AR5
AK51	GND	GND	AR8
AK7	GND	GND	AT1
AL12	GND	GND	AT11
AL14	GND	GND	AT2
AL16	GND	GND	AT21
AL18	GND	GND	AT23
AL20	GND	GND	AT25
AL22	GND	GND	AT27
AL24	GND	GND	AT29
AL26	GND	GND	AT31
AL28	GND	GND	AT38
AL3	GND	GND	AT41
AL30	GND	GND	AT46
AL32	GND	GND	AT47
AL34	GND	GND	AT5
AL36	GND	GND	AT50
AL38	GND	GND	AT51
AL4	GND	GND	AT6
AL40	GND	GND	AU13
AL44	GND	GND	AU14
AL47	GND	GND	AU18
AL48	GND	GND	AU24
AL49	GND	GND	AU26
AL5	GND	GND	AU28
AL8	GND	GND	AU3
AM1	GND	GND	AU30
AM11	GND	GND	AU38
AM15	GND	GND	AU39
AM17	GND	GND	AU4
AM19	GND	GND	AU43
AM2	GND	GND	AU47
AM21	GND	GND	AU48
AM23	GND	GND	AU49
AM25	GND	GND	AU5
AM27	GND	GND	AU9
AM29	GND	GND	AV1
AM31	GND	GND	AV10
AM33	GND	GND	AV15
AM35	GND	GND	AV2
AM37	GND	GND	AV25
AM38	GND	GND	AV35
AM41	GND	GND	AV38
AM46	GND	GND	AV42
AM47	GND	GND	AV45
AM5	GND	GND	AV47
AM50	GND	GND	AV5
AM51	GND	GND	AV50
AM6	GND	GND	AV51
AN12	GND	GND	AV7
AN14	GND	GND	AW12
AN16	GND	GND	AW14
AN18	GND	GND	AW22
AN20	GND	GND	AW3
AN22	GND	GND	AW32
AN24	GND	GND	AW38
AN26	GND	GND	AW4
AN28	GND	GND	AW40
AN3	GND	GND	AW44
AN30	GND	GND	AW47
AN32	GND	GND	AW48
AN34	GND	GND	AW49
AN36	GND	GND	AW5
AN38	GND	GND	AW8
AN4	GND	GND	AY1
AN40	GND	GND	AY11
AN43	GND	GND	AY19
AN47	GND	GND	AY2
AN48	GND	GND	AY29
AN49	GND	GND	AY38
AN5	GND	GND	AY41
AN9	GND	GND	AY46
AP1	GND	GND	AY47
AP10	GND	GND	AY5
AP15	GND	GND	AY50
AP17	GND	GND	AY51
AP19	GND	GND	AY6
AP2	GND	GND	B10
AP21	GND	GND	B14
AP23	GND	GND	B16
AP25	GND	GND	B19
AP27	GND	GND	B20
AP29	GND	GND	B21
AP31	GND	GND	B23
AP33	GND	GND	B3
AP35	GND	GND	B31
AP37	GND	GND	B32
AP38	GND	GND	B33

GND GND

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B36	GND	GND	BG12
B38	GND	GND	BG16
B4	GND	GND	BG17
B42	GND	GND	BG18
B45	GND	GND	BG21
B46	GND	GND	BG28
B47	GND	GND	BG3
B48	GND	GND	BG31
B49	GND	GND	BG34
B5	GND	GND	BG35
B6	GND	GND	BG36
B7	GND	GND	BG4
BA12	GND	GND	BG40
BA14	GND	GND	BG44
BA16	GND	GND	BG45
BA26	GND	GND	BG48
BA3	GND	GND	BG49
BA36	GND	GND	BG7
BA38	GND	GND	BG8
BA4	GND	GND	BH1
BA40	GND	GND	BH11
BA43	GND	GND	BH15
BA47	GND	GND	BH16
BA48	GND	GND	BH19
BA49	GND	GND	BH2
BA5	GND	GND	BH20
BA9	GND	GND	BH21
BB1	GND	GND	BH25
BB10	GND	GND	BH31
BB2	GND	GND	BH32
BB23	GND	GND	BH33
BB33	GND	GND	BH36
BB38	GND	GND	BH37
BB42	GND	GND	BH41
BB45	GND	GND	BH45
BB47	GND	GND	BH46
BB5	GND	GND	BH47
BB50	GND	GND	BH5
BB51	GND	GND	BH50
BB7	GND	GND	BH51
BC12	GND	GND	BH6
BC14	GND	GND	BH7
BC20	GND	GND	BJ13
BC3	GND	GND	BJ16
BC30	GND	GND	BJ17
BC38	GND	GND	BJ18
BC4	GND	GND	BJ2
BC40	GND	GND	BJ21
BC44	GND	GND	BJ22
BC47	GND	GND	BJ3
BC48	GND	GND	BJ31
BC49	GND	GND	BJ34
BC5	GND	GND	BJ35
BC8	GND	GND	BJ36
BD1	GND	GND	BJ39
BD11	GND	GND	BJ4
BD14	GND	GND	BJ43
BD2	GND	GND	BJ45
BD27	GND	GND	BJ48
BD38	GND	GND	BJ49
BD41	GND	GND	BJ50
BD46	GND	GND	BJ7
BD47	GND	GND	BJ9
BD5	GND	GND	BK10
BD50	GND	GND	BK14
BD51	GND	GND	BK16
BD6	GND	GND	BK19
BE12	GND	GND	BK20
BE14	GND	GND	BK21
BE15	GND	GND	BK29
BE16	GND	GND	BK3
BE17	GND	GND	BK31
BE18	GND	GND	BK32
BE19	GND	GND	BK33
BE24	GND	GND	BK36
BE3	GND	GND	BK38
BE33	GND	GND	BK4
BE34	GND	GND	BK42
BE35	GND	GND	BK45
BE36	GND	GND	BK46
BE37	GND	GND	BK47
BE38	GND	GND	BK48
BE4	GND	GND	BK49
BE40	GND	GND	BK5
BE43	GND	GND	BK6
BE47	GND	GND	BK7
BE48	GND	GND	BL12
BE49	GND	GND	BL16
BE5	GND	GND	BL17
BE9	GND	GND	BL18
BF1	GND	GND	BL21
BF10	GND	GND	BL26
BF16	GND	GND	BL31
BF19	GND	GND	BL34
BF2	GND	GND	BL35
BF20	GND	GND	BL36
BF21	GND	GND	BL4
BF31	GND	GND	BL40
BF32	GND	GND	BL44
BF33	GND	GND	BL45
BF36	GND	GND	BL48
BF42	GND	GND	BL7
BF45	GND	GND	BL8
BF46	GND	GND	C12
BF47	GND	GND	C16
BF5	GND	GND	C17
BF50	GND	GND	C18
BF51	GND	GND	C2
BF6	GND	GND	C21
BF7	GND	GND	C3

GND GND

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C31	GND	GND	H35
C34	GND	GND	H36
C35	GND	GND	H37
C36	GND	GND	H38
C4	GND	GND	H41
C40	GND	GND	H46
C44	GND	GND	H47
C45	GND	GND	H5
C48	GND	GND	H50
C49	GND	GND	H51
C50	GND	GND	H6
C7	GND	GND	J12
C8	GND	GND	J14
D1	GND	GND	J22
D11	GND	GND	J3
D15	GND	GND	J38
D16	GND	GND	J4
D19	GND	GND	J40
D2	GND	GND	J43
D20	GND	GND	J47
D21	GND	GND	J48
D27	GND	GND	J49
D31	GND	GND	J5
D32	GND	GND	J9
D33	GND	GND	K1
D36	GND	GND	K10
D37	GND	GND	K14
D41	GND	GND	K19
D45	GND	GND	K2
D46	GND	GND	K29
D47	GND	GND	K38
D5	GND	GND	K42
D50	GND	GND	K45
D51	GND	GND	K47
D6	GND	GND	K5
D7	GND	GND	K50
E12	GND	GND	K51
E16	GND	GND	K7
E17	GND	GND	L12
E18	GND	GND	L14
E21	GND	GND	L16
E24	GND	GND	L26
E3	GND	GND	L3
E31	GND	GND	L36
E34	GND	GND	L38
E35	GND	GND	L4
E36	GND	GND	L40
E39	GND	GND	L44
E4	GND	GND	L47
E43	GND	GND	L48
E45	GND	GND	L49
E48	GND	GND	L5
E49	GND	GND	L8
E7	GND	GND	M1
E9	GND	GND	M11
F1	GND	GND	M2
F10	GND	GND	M23
F14	GND	GND	M33
F16	GND	GND	M38
F19	GND	GND	M41
F2	GND	GND	M46
F20	GND	GND	M47
F21	GND	GND	M5
F31	GND	GND	M50
F32	GND	GND	M51
F33	GND	GND	M6
F36	GND	GND	N13
F38	GND	GND	N14
F42	GND	GND	N20
F45	GND	GND	N3
F46	GND	GND	N30
F47	GND	GND	N38
F5	GND	GND	N39
F50	GND	GND	N4
F51	GND	GND	N43
F6	GND	GND	N47
F7	GND	GND	N48
G12	GND	GND	N49
G16	GND	GND	N5
G18	GND	GND	N9
G21	GND	GND	P1
G28	GND	GND	P10
G3	GND	GND	P17
G31	GND	GND	P2
G34	GND	GND	P27
G36	GND	GND	P37
G4	GND	GND	P38
G40	GND	GND	P42
G44	GND	GND	P45
G47	GND	GND	P47
G48	GND	GND	P5
G49	GND	GND	P50
G5	GND	GND	P51
G8	GND	GND	P7
H1	GND	GND	R12
H11	GND	GND	R14
H14	GND	GND	R24
H15	GND	GND	R3
H16	GND	GND	R34
H17	GND	GND	R38
H18	GND	GND	R4
H19	GND	GND	R40
H2	GND	GND	R44
H20	GND	GND	R47
H21	GND	GND	R48
H25	GND	GND	R49
H31	GND	GND	R5
H32	GND	GND	R8
H33	GND	GND	T1
H34	GND	GND	T11

GND GND

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T2	GND
T21	GND
T38	GND
T41	GND
T46	GND
T47	GND
T5	GND
T50	GND
T51	GND
T6	GND
U13	GND
U14	GND
U18	GND
U28	GND
U3	GND
U30	GND
U38	GND
U39	GND
U4	GND
U43	GND
U47	GND
U48	GND
U49	GND
U5	GND
U9	GND
V1	GND
V10	GND
V2	GND
V23	GND
V25	GND
V27	GND
V29	GND
V31	GND
V38	GND
V42	GND
V45	GND
V47	GND
V5	GND
V50	GND
V51	GND
V7	GND
W12	GND
W14	GND
W18	GND
W20	GND
W22	GND
W24	GND
W26	GND
W28	GND
W3	GND
W30	GND
W34	GND
W36	GND
W38	GND
W4	GND
W40	GND
W44	GND
W47	GND
W48	GND
W49	GND
W5	GND
W8	GND
Y1	GND
Y11	GND
Y15	GND
Y17	GND
Y19	GND
Y2	GND
Y21	GND
Y23	GND
Y25	GND
Y27	GND
Y29	GND
Y31	GND
Y33	GND
Y35	GND
Y37	GND
Y38	GND
Y41	GND
Y46	GND
Y47	GND
Y5	GND
Y50	GND
Y51	GND

GND

R1120 10K 0603

V_M3V3

Y6

GND

/F1_INSTALLED
22

IF THE FPGA IS INSTALLED, THEN THE ACTIVE-LO "/F1_INSTALLED" SIGNAL WILL BE PULLED TO GND. IF THE FPGA IS NOT INSTALLED, THE SIGNAL WILL BE HI.

ANY FPGA GND PIN CAN BE USED.

APOLLO CM W/ DUAL A2577, MK1

Title
5.01: FPGA#1 GND

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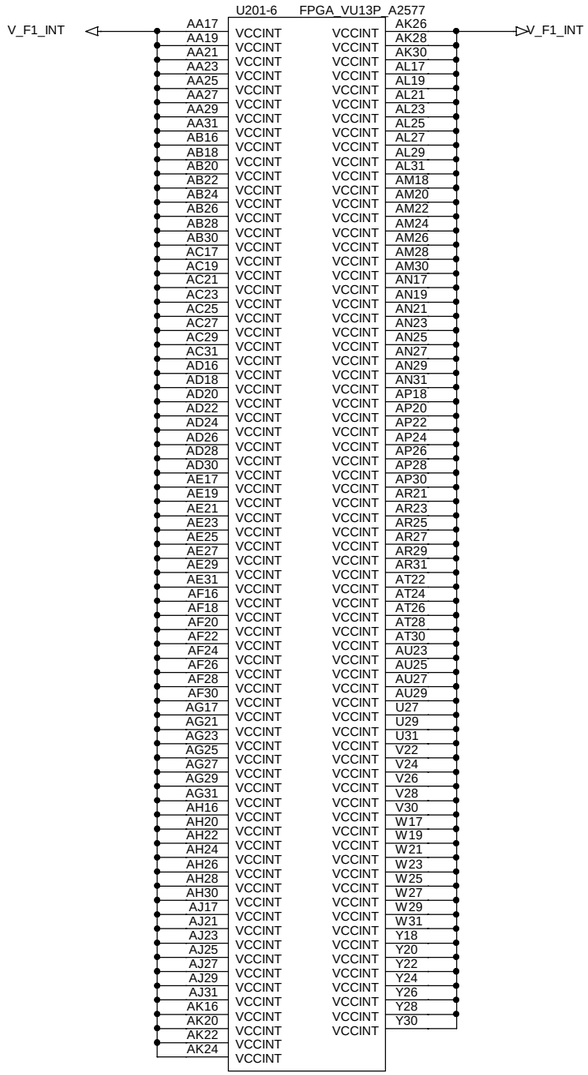
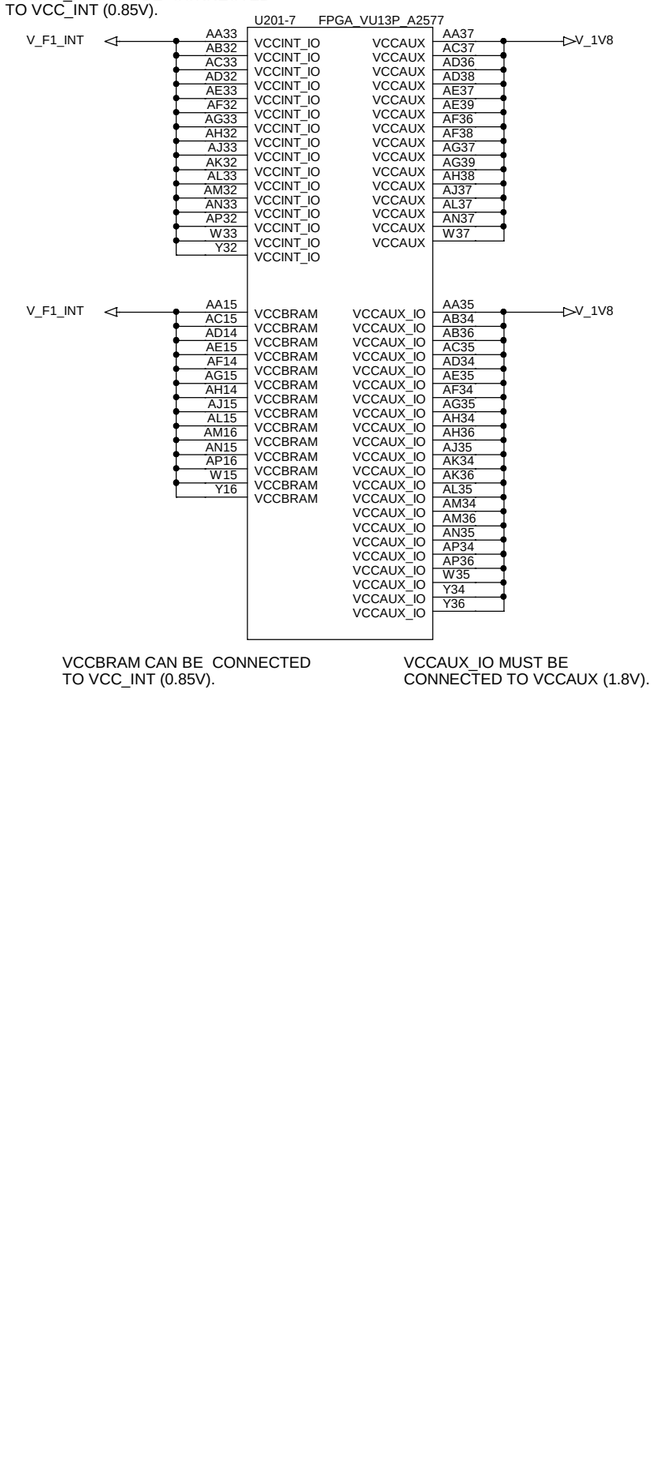
5.02: FPGA#1 POWER INTERNAL

VCCINT MUST BE 0.85V.

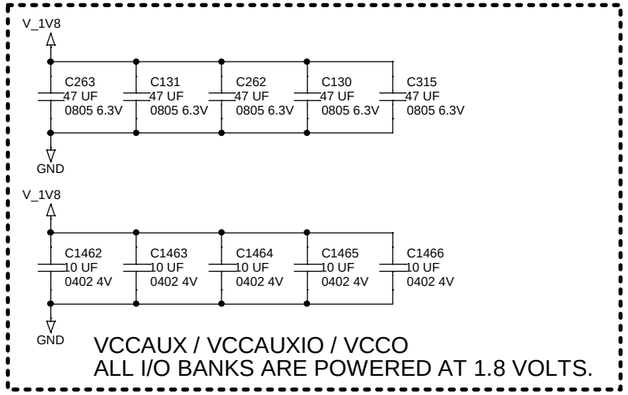


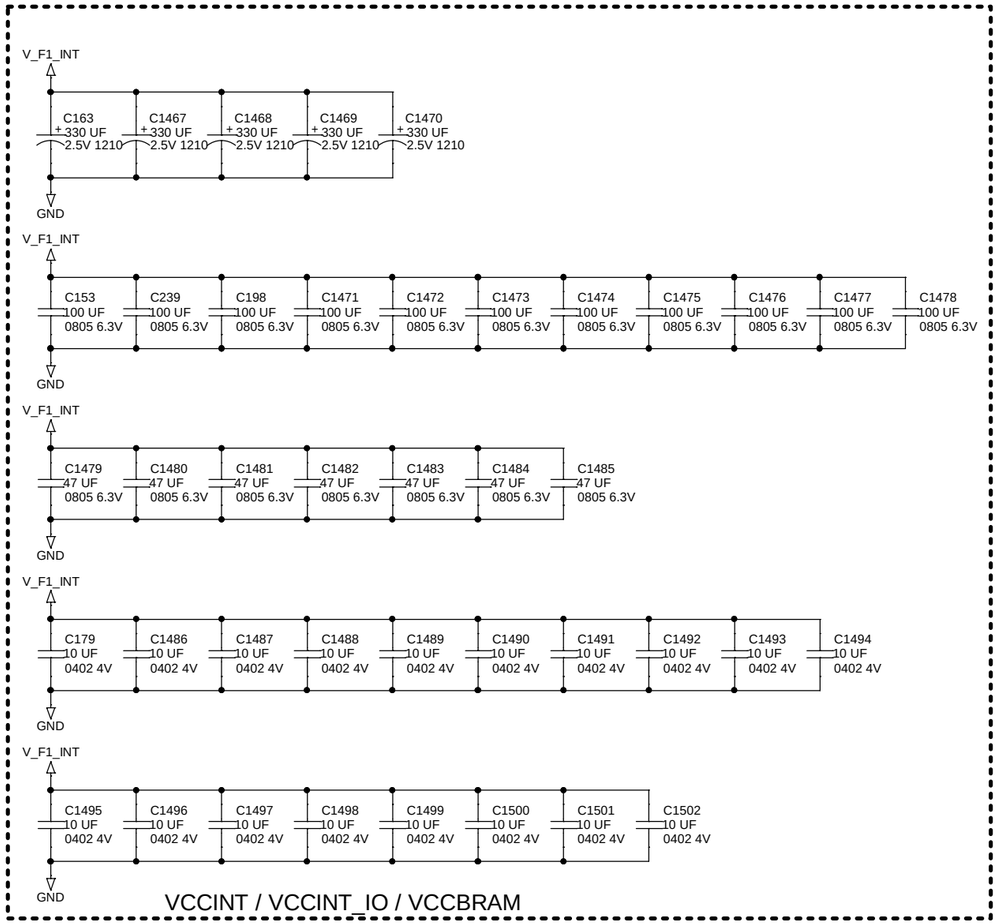
VCCINT_IO MUST BE CONNECTED TO VCC_INT (0.85V).



VCCBRAM CAN BE CONNECTED TO VCC_INT (0.85V).

VCCAUX_IO MUST BE CONNECTED TO VCCAUX (1.8V).





BYPASS CAPACITOR VALUES AND QUANTITIES FROM
"UG583 UltraScale Architecture PCB Design"

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Title: 5.02: FPGA#1 POWER INTERNAL		
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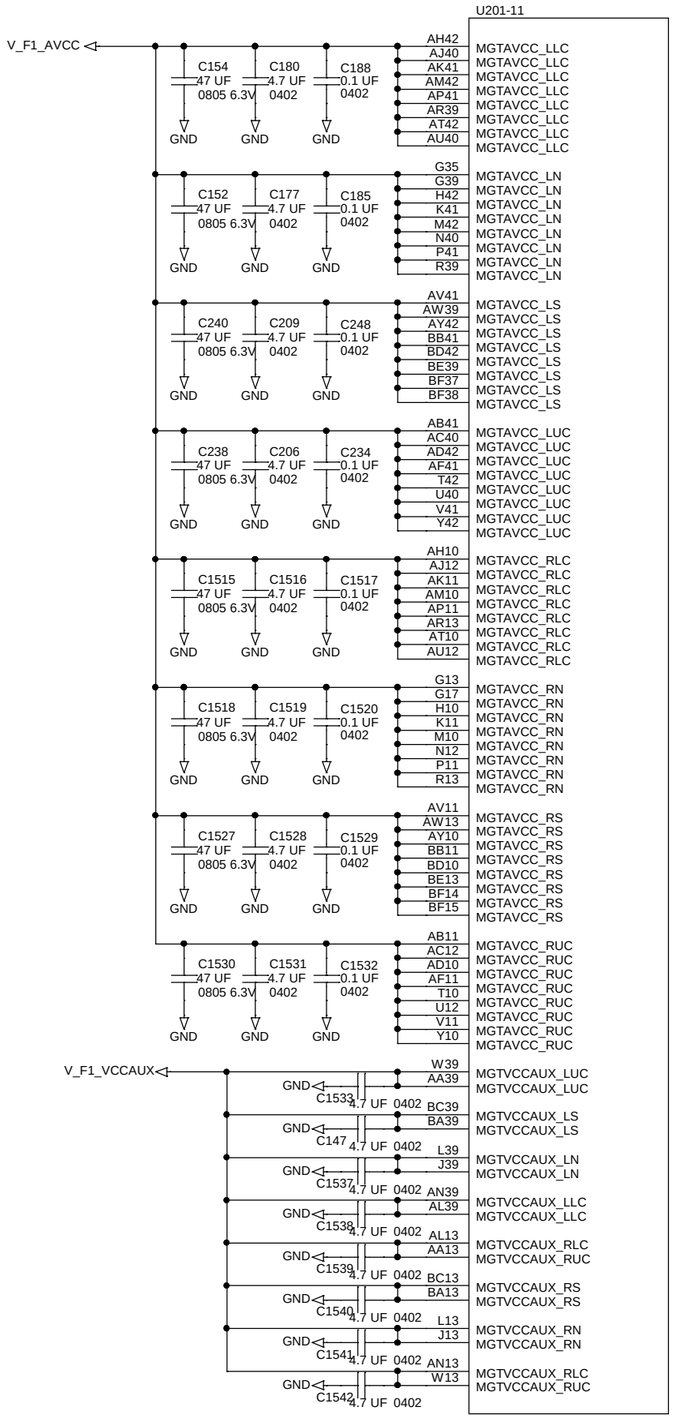
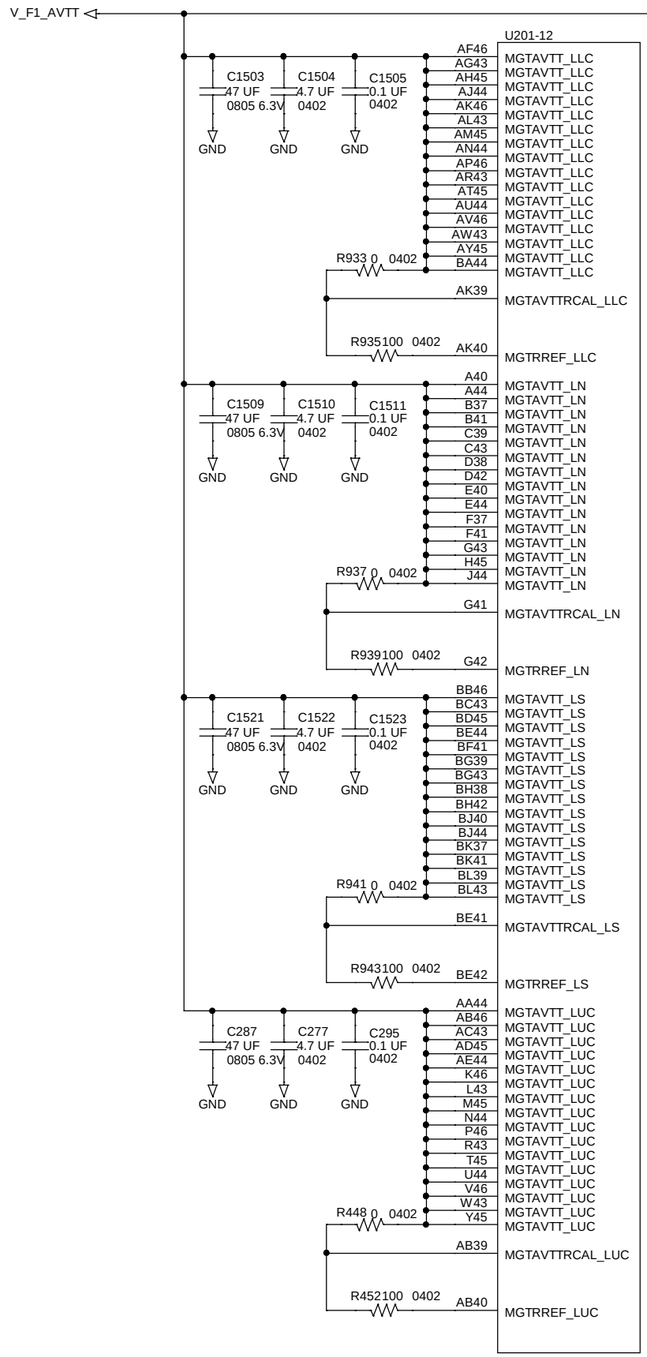
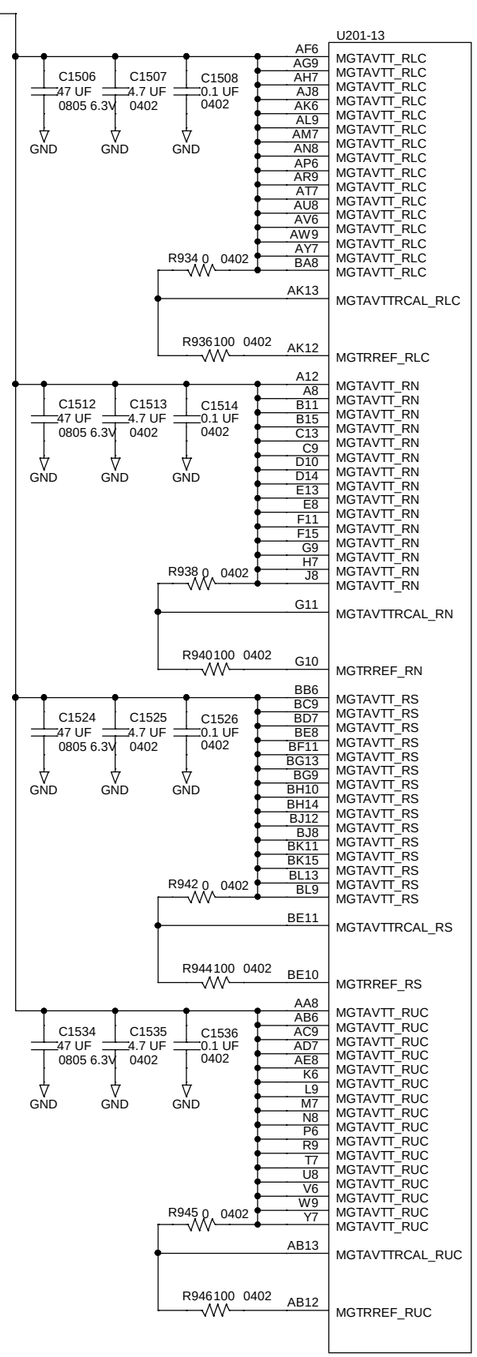
5.03: FPGA#1 GTY TRANSCEIVER POWER



FPGA_VU13P_A2577



FPGA_VU13P_A2577



FPGA_VU13P_A2577

REFER TO THE GTY USER GUIDE FOR DETAILS ON TRACE ROUTING FOR THE MGTRREF RESISTOR.

PLACE CAPACITORS AND RESISTORS THAT ARE ON THIS SHEET NEAR THE BGA PINS.

APOLLO CM W/ DUAL A2577, MK1

Title: 5.03: FPGA#1 GTY TRANSCEIVER POWER

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5.04: FPGA#1 CONFIGURATION

MUST BE TIED TO "VCCINT" OR "GND". DO NOT CONNECT TO "VCCO_0". CONNECT TO "GND" FOR STANDARD POR DELAY.

THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

PULLUPS/PULLDOWNS ON THE BOOT MODE CONFIGURATION INPUTS MUST BE 1K OR LESS.

U201-10
BANK 0
FPGA_VU13P_A2577

POR_OVERRIDE, RSVDGND, PUDC_B_0, M2_0, M1_0, M0_0, VCCO_0, VCCO_0, D00_MOSI_0, D01_DIN_0, D02_0, D03_0, RDWR_FCS_B_0, CCLK_0, PROGRAM_B_0, DONE_0, INIT_B_0, VBATT

THIS DESIGN DOES NOT USE ENCRYPTION, SO "VBATT" CAN BE TIED TO "GND"

QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
VU9P 641,272,864
VU13P 906,547,008

U95
MT25QU01
DQ0, DQ1, DQ2, DQ3, S#, CLK, VCC, GND, DNU_3, DNU_4, DNU_5, DNU_6, DNU_11, DNU_12, DNU_13, DNU_14

C245 47 UF 0805 6.3V
C735 0.1 UF 0402

F1_CFG_DONE

FPGA#1 CFG DONE LED

/F1_CFG_DONE 22
D4 LED GREEN
Q1 FET_N_1.8V

THE PULLUP RESISTOR IN PARALLEL WITH THE LED ENSURES THAT, WHEN THE FET IS OFF, THE "/F1_CFG_DONE" SIGNAL IS AT A HIGH LEVEL FOR FEEDING THE MCU.

FOR LED CURRENT OF 5 MA, THE FORWARD VOLTAGE DROP IS 1.95V. USE 270 OHM RESISTOR.

IF THE FPGA IS NOT INSTALLED, THEN "CFG_DONE" WILL ALWAYS BE HIGH, AND THE LED WILL ALWAYS BE LIT. THIS IS UNINTENDED AND UNDESIRABLE. CONSIDER ELIMINATING THE FPGA DONE LED,OR ADD A GATE.

WHEN "FPGA_CFG_FROM_FLASH" IS ASSERTED (HIGH), THE FPGA WILL BE ABLE TO BOOT FROM THE FLASH MEMORY. WHEN IT IS NEGATED (LOW), THE FPGA WILL ONLY BE ABLE TO BOOT FROM JTAG.

FPGA_CFG_FROM_FLASH 22,52
Q28 FET_N_1.8V

THE FPGA CAN BE REPROGRAMMED BY PULSING "F1_CFG_START" FROM THE MCU.

F1_CFG_START 22
Q26 FET_N_1.8V

APOLLO CM W/ DUAL A2577, MK1			
Title: 5.04: FPGA#1 CONFIGURATION			
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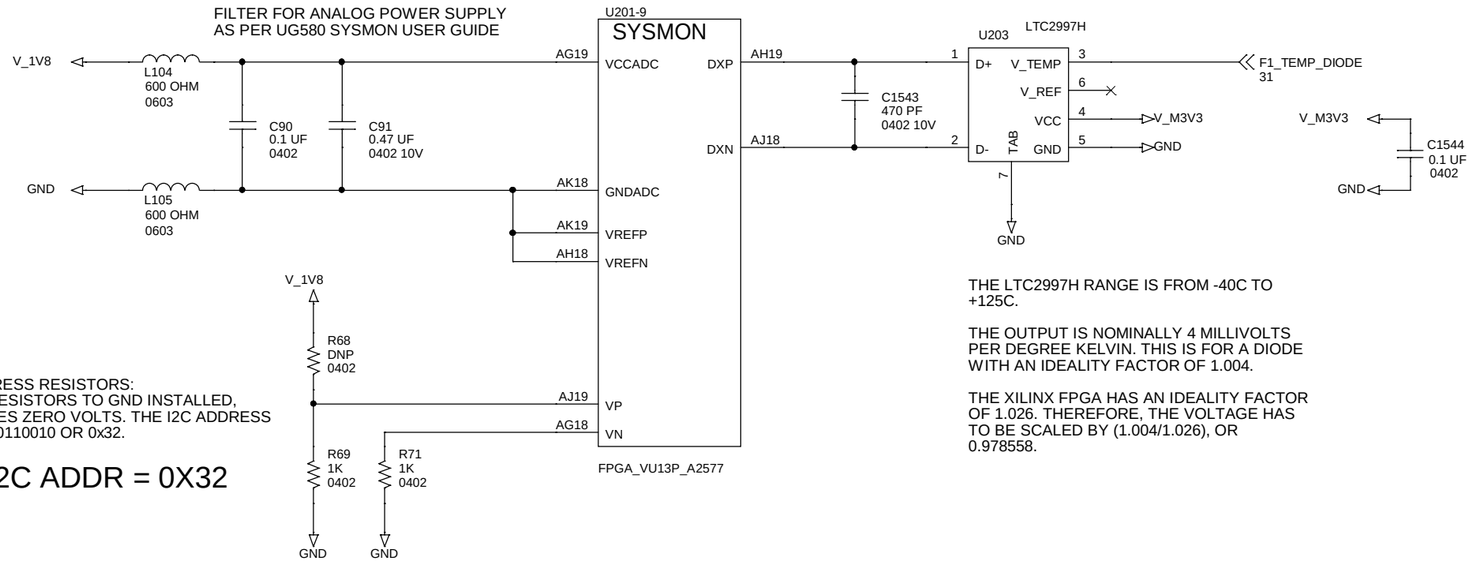
5.05: FPGA#1 SYSTEM MONITOR

FOR THE VU9P, THE MASTER SLR INDEX IS SLR1, AND THE SLAVE SLR INDEX ARE SLR0 AND SLR2.

FOR THE VU13P, THE MASTER SLR INDEX IS SLR1, AND THE SLAVE SLR INDEX ARE SLR0, SLR2, AND SLR3.

ONLY THE MASTER SLR IS ACCESSABLE FROM THE I2C CONNECTIONS.



SYSMON I2C ADDRESS RESISTORS:
WITH ONLY THE RESISTORS TO GND INSTALLED, SYSMON MEASURES ZERO VOLTS. THE I2C ADDRESS IS THEREFORE 0b0110010 OR 0x32.

I2C ADDR = 0X32

THE LTC2997H RANGE IS FROM -40C TO +125C.

THE OUTPUT IS NOMINALLY 4 MILLIVOLTS PER DEGREE KELVIN. THIS IS FOR A DIODE WITH AN IDEALITY FACTOR OF 1.004.

THE XILINX FPGA HAS AN IDEALITY FACTOR OF 1.026. THEREFORE, THE VOLTAGE HAS TO BE SCALED BY (1.004/1.026), OR 0.978558.

APOLLO CM W/ DUAL A2577, MK1		
Title: 5.05: FPGA#1 SYSTEM MONITOR		
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5.06 FPGA#1 I/O SLR0

THESE BANKS ARE NUMBERED THE SAME IN THE VU13P AND VU9P, AND THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#0 FOR THE VU13P AND SLR#0 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
D	61	61
E	62	62
F	63	63

THESE SIGNALS MAY BE ASSIGNED TO DIFFERENT PINS OR A DIFFERENT BLOCK DURING LAYOUT TO SIMPLIFY ROUTING. KEEP FPGA CLOCK INPUTS ON "GC" PINS.

U201-14

BE20 IO_L10N_T1U_N7_QBC_AD4N_61
BE21 IO_L10P_T1U_N6_QBC_AD4P_61
BF22 IO_L11N_T1U_N9_GC_61
BE22 IO_L11P_T1U_N8_GC_61
BE23 IO_L12N_T1U_N11_GC_61
BD23 IO_L12P_T1U_N10_GC_61
BD24 IO_L13N_T2L_N1_GC_QBC_61
BD25 IO_L13P_T2L_N0_GC_QBC_61
BC23 IO_L14N_T2L_N3_GC_61
BC24 IO_L14P_T2L_N2_GC_61
BB25 IO_L15N_T2L_N5_AD11N_61
BB26 IO_L15P_T2L_N4_AD11P_61
BD26 IO_L16N_T2U_N7_QBC_AD3N_61
BC26 IO_L16P_T2U_N6_QBC_AD3P_61
BA24 IO_L17N_T2U_N9_AD10N_61
BA25 IO_L17P_T2U_N8_AD10P_61
BC22 IO_L18N_T2U_N11_AD2N_61
BB22 IO_L18P_T2U_N10_AD2P_61
AW24 IO_L19N_T3L_N1_DBC_AD9N_61
AW25 IO_L19P_T3L_N0_DBC_AD9P_61
BL23 IO_L1N_T0L_N1_DBC_61
BL24 IO_L1P_T0L_N0_DBC_61
AW23 IO_L20N_T3L_N3_AD1N_61
AV24 IO_L20P_T3L_N2_AD1P_61
BA23 IO_L21N_T3L_N5_AD8N_61
AY23 IO_L21P_T3L_N4_AD8P_61
BA27 IO_L22N_T3U_N7_DBC_AD0N_61
AY27 IO_L22P_T3U_N6_DBC_AD0P_61
AY26 IO_L23N_T3U_N9_61
AW26 IO_L23P_T3U_N8_61
AV26 IO_L24N_T3U_N11_61
AV27 IO_L24P_T3U_N10_61
BL22 IO_L2N_T0L_N3_61
BK22 IO_L2P_T0L_N2_61
BJ24 IO_L3N_T0L_N5_AD15N_61
BJ25 IO_L3P_T0L_N4_AD15P_61
BK23 IO_L4N_T0U_N7_DBC_AD7N_61
BJ23 IO_L4P_T0U_N6_DBC_AD7P_61
BL25 IO_L5N_T0U_N9_AD14N_61
BK25 IO_L5P_T0U_N8_AD14P_61
BH23 IO_L6N_T0U_N11_AD6N_61
BH24 IO_L6P_T0U_N10_AD6P_61
BG24 IO_L7N_T1L_N1_QBC_AD13N_61
BG25 IO_L7P_T1L_N0_QBC_AD13P_61
BG22 IO_L8N_T1L_N3_AD5N_61
BF23 IO_L8P_T1L_N2_AD5P_61
BF24 IO_L9N_T1L_N5_AD12N_61
BF25 IO_L9P_T1L_N4_AD12P_61
BH22 IO_T0U_N12_VRP_61
BE25 IO_T1U_N12_61
BB24 IO_T2U_N12_61
AY25 IO_T3U_N12_61

VCCO_61 AW27 AY24 BC25 BD22 BG23 BK24
VREF_61 AV23

V_1V8
R1221 1K 0402 GND
R1224 240 0402 GND

FPGA_VU13P_A2577

nF1_TEST_CONN_0 48
pF1_TEST_CONN_0 48
pF1_TEST_CONN_5 48
nF1_TEST_CONN_6 48
nF1_TEST_CONN_4 48
pF1_TEST_CONN_4 48
nF1_TEST_CONN_3 48
pF1_TEST_CONN_3 48
nF1_TEST_CONN_2 48
pF1_TEST_CONN_2 48
nF1_TEST_CONN_1 48
pF1_TEST_CONN_1 48

THIS IS THE 40 MHZ RECOVERED TCDS CLOCK. USING BANK 62 KEEPS THIS INTHE SAME SLR AS THE TCDS LOGIC.

bc_nF1_TCDS_RECOV_CLK 20
bc_pF1_TCDS_RECOV_CLK 20

U201-15

BH27 IO_L10N_T1U_N7_QBC_AD4N_62
BH26 IO_L10P_T1U_N6_QBC_AD4P_62
BF28 IO_L11N_T1U_N9_GC_62
BF27 IO_L11P_T1U_N8_GC_62
BE27 IO_L12N_T1U_N11_GC_62
BE26 IO_L12P_T1U_N10_GC_62
BD29 IO_L13N_T2L_N1_GC_QBC_62
BC28 IO_L13P_T2L_N0_GC_QBC_62
BE28 IO_L14N_T2L_N3_GC_62
BD28 IO_L14P_T2L_N2_GC_62
BE30 IO_L15N_T2L_N5_AD11N_62
BD30 IO_L15P_T2L_N4_AD11P_62
BC27 IO_L16N_T2U_N7_QBC_AD3N_62
BB27 IO_L16P_T2U_N6_QBC_AD3P_62
BC31 IO_L17N_T2U_N9_AD10N_62
BB31 IO_L17P_T2U_N8_AD10P_62
BC29 IO_L18N_T2U_N11_AD2N_62
BB29 IO_L18P_T2U_N10_AD2P_62
BA29 IO_L19N_T3L_N1_DBC_AD9N_62
BA28 IO_L19P_T3L_N0_DBC_AD9P_62
BJ28 IO_L1N_T0L_N1_DBC_62
BH28 IO_L1P_T0L_N0_DBC_62
AY28 IO_L20N_T3L_N3_AD1N_62
AW28 IO_L20P_T3L_N2_AD1P_62
BA30 IO_L21N_T3L_N5_AD8N_62
AY30 IO_L21P_T3L_N4_AD8P_62
AV31 IO_L22N_T3U_N7_DBC_AD0N_62
AU31 IO_L22P_T3U_N6_DBC_AD0P_62
AW29 IO_L23N_T3U_N9_62
AV29 IO_L23P_T3U_N8_62
AY31 IO_L24N_T3U_N11_62
AW31 IO_L24P_T3U_N10_62
BL28 IO_L2N_T0L_N3_62
BL27 IO_L2P_T0L_N2_62
BJ30 IO_L3N_T0L_N5_AD15N_62
BJ29 IO_L3P_T0L_N4_AD15P_62
BK28 IO_L4N_T0U_N7_DBC_AD7N_62
BK27 IO_L4P_T0U_N6_DBC_AD7P_62
BL30 IO_L5N_T0U_N9_AD14N_62
BK30 IO_L5P_T0U_N8_AD14P_62
BK26 IO_L6N_T0U_N11_AD6N_62
BJ26 IO_L6P_T0U_N10_AD6P_62
BG27 IO_L7N_T1L_N1_QBC_AD13N_62
BG26 IO_L7P_T1L_N0_QBC_AD13P_62
BG30 IO_L8N_T1L_N3_AD5N_62
BF29 IO_L8P_T1L_N2_AD5P_62
BH29 IO_L9N_T1L_N5_AD12N_62
BG29 IO_L9P_T1L_N4_AD12P_62
BL29 IO_T0U_N12_VRP_62
BF30 IO_T1U_N12_62
BB30 IO_T2U_N12_62
AW30 IO_T3U_N12_62

VCCO_62 AV30 BA31 BB28 BE29 BF26 BH30 BJ27
VREF_62 AV28

V_1V8
R1222 1K 0402 GND
R1225 240 0402 GND

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U201-16

BC36 IO_L10N_T1U_N7_QBC_AD4N_63
BB36 IO_L10P_T1U_N6_QBC_AD4P_63
BB35 IO_L11N_T1U_N9_GC_63
BA35 IO_L11P_T1U_N8_GC_63
BB34 IO_L12N_T1U_N11_GC_63
BA34 IO_L12P_T1U_N10_GC_63
AW36 IO_L13N_T2L_N1_GC_QBC_63
AW35 IO_L13P_T2L_N0_GC_QBC_63
AY36 IO_L14N_T2L_N3_GC_63
AY35 IO_L14P_T2L_N2_GC_63
AV37 IO_L15N_T2L_N5_AD11N_63
AV36 IO_L15P_T2L_N4_AD11P_63
AV33 IO_L16N_T2U_N7_QBC_AD3N_63
AV32 IO_L16P_T2U_N6_QBC_AD3P_63
AW34 IO_L17N_T2U_N9_AD10N_63
AW33 IO_L17P_T2U_N8_AD10P_63
AV34 IO_L18N_T2U_N11_AD2N_63
AU34 IO_L18P_T2U_N10_AD2P_63
AU37 IO_L19N_T3L_N1_DBC_AD9N_63
AU36 IO_L19P_T3L_N0_DBC_AD9P_63
BE32 IO_L1N_T0L_N1_DBC_63
BE31 IO_L1P_T0L_N0_DBC_63
AU32 IO_L20N_T3L_N3_AD1N_63
AT32 IO_L20P_T3L_N2_AD1P_63
AR37 IO_L21N_T3L_N5_AD8N_63
AR36 IO_L21P_T3L_N4_AD8P_63
AT34 IO_L22N_T3U_N7_DBC_AD0N_63
AT33 IO_L22P_T3U_N6_DBC_AD0P_63
AT35 IO_L23N_T3U_N9_63
AR35 IO_L23P_T3U_N8_63
AR34 IO_L24N_T3U_N11_63
AR33 IO_L24P_T3U_N10_63
BC32 IO_L2N_T0L_N3_63
BB32 IO_L2P_T0L_N2_63
BA32 IO_L3N_T0L_N5_AD15N_63
AY32 IO_L3P_T0L_N4_AD15P_63
BA33 IO_L4N_T0U_N7_DBC_AD7N_63
AY33 IO_L4P_T0U_N6_DBC_AD7P_63
BD33 IO_L5N_T0U_N9_AD14N_63
BC33 IO_L5P_T0U_N8_AD14P_63
BD34 IO_L6N_T0U_N11_AD6N_63
BC34 IO_L6P_T0U_N10_AD6P_63
BD36 IO_L7N_T1L_N1_QBC_AD13N_63
BD35 IO_L7P_T1L_N0_QBC_AD13P_63
BD37 IO_L8N_T1L_N3_AD5N_63
BC37 IO_L8P_T1L_N2_AD5P_63
BB37 IO_L9N_T1L_N5_AD12N_63
BA37 IO_L9P_T1L_N4_AD12P_63
BD31 IO_T0U_N12_VRP_63
AY37 IO_T1U_N12_63
AU35 IO_T2U_N12_63
AT37 IO_T3U_N12_63

VCCO_63 AT36 AU33 AW37 AY34 BC35 BD32
VREF_63 AR32

V_1V8
R1223 1K 0402 GND
R1226 240 0402 GND

FPGA_VU13P_A2577

APOLLO CM W/ DUAL A2577, MK1

Title: 5.06 FPGA#1 I/O SLR0

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5.07 FPGA#1 I/O SLR1

THESE BANKS ARE NUMBERED THE SAME IN THE VU13P AND VU9P, AND THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#1 FOR THE VU13P AND SLR#1 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
C	65	65
B	66	66

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

FPGA_VU13P_A2577 U201-17

		VCCO_65	AR19
		VCCO_65	AV20
		VCCO_65	AW17
		VCCO_65	BA21
		VCCO_65	BB18
		VCCO_65	BC15
RESERVED	BD15	65_L24N_DOUT_CSO_B	
RESERVED	BD16	VREF_65	AR20
I2C_SDA_F1_SYSMON 36	BC16	65_L24P_EMCCLK	
I2C_SCL_F1_SYSMON 36	BB16	65_L23N_PERSTN1_I2C_SDA	
RESERVED	BD17	65_L23P_I2C_SCLK	
RESERVED	BD18	65_L22N_DBC_AD0N_D05	
RESERVED	BC17	65_L22P_DBC_AD0P_D04	
RESERVED	BB17	65_L21N_AD8N_D07	
RESERVED	BA18	65_L21P_AD8P_D06	
RESERVED	BA19	65_L20N_AD1N_D09	
RESERVED	BC18	65_L20P_AD1P_D08	
RESERVED	BC19	65_L19N_DBC_AD9N_D11	
RESERVED	AW15	65_L19P_DBC_AD9P_D10	
RESERVED	AV16	65_L18N_AD2N_D13	
RESERVED	BA15	65_L18P_AD2P_D12	
RESERVED	AY15	65_L17N_AD10N_D15	
RESERVED	AV17	65_L17P_AD10P_D14	
RESERVED	AU17	65_L16N_QBC_AD3N_A01_D17	
RESERVED	AY16	65_L16P_QBC_AD3P_A00_D16	
RESERVED	AW16	65_L15N_AD11N_A03_D19	
RESERVED	BA17	65_L15P_AD11P_A02_D18	
RESERVED	AY17	65_L14N_GC_A05_D21	
RESERVED	AY18	65_L14P_GC_A04_D20	
RESERVED	AW18	65_L13N_GC_QBC_A07_D23	
RESERVED	AV19	65_L13P_GC_QBC_A06_D22	
RESERVED	AU19	65_L12N_GC_A09_D25	
RESERVED	AW19	65_L12P_GC_A08_D24	
RESERVED	AW20	65_L11N_GC_A11_D27	
RESERVED	AT18	65_L11P_GC_A10_D26	
RESERVED	AR18	65_L10N_QBC_AD4N_A13_D29	
RESERVED	AU20	65_L10P_QBC_AD4P_A12_D28	
RESERVED	AU21	65_L9N_AD12N_A15_D31	
RESERVED	AT19	65_L9P_AD12P_A14_D30	
RESERVED	AT20	65_L8N_AD5N_A17	
RESERVED	AV21	65_L8P_AD5P_A16	
RESERVED	AV22	65_L7N_QBC_AD13N_A19	
RESERVED	BA20	65_L7P_QBC_AD13P_A18	
RESERVED	AY20	65_L6N_AD6N_A21	
RESERVED	BB19	65_L6P_AD6P_A20	
RESERVED	BB20	65_L5N_AD14N_A23	
RESERVED	AY21	65_L5P_AD14P_A22	
RESERVED	AW21	65_L4N_DBC_AD7N_A25	
RESERVED	BD19	65_L4P_DBC_AD7P_A24	
RESERVED	BD20	65_L3N_AD15N_A27	
RESERVED	BA22	65_L3P_AD15P_A26	
RESERVED	AY22	65_L2N_FWE_FCS2_B	
AVAILABLE	BC21	65_L2P_FOE_B	
AVAILABLE	BB21	65_L1N_DBC_RS1	
	BB15	65_L1P_DBC_RS0	
RESERVED	AV18	65_PERSTN0	
	AU22	65_CSI_ADV_B	
RESERVED	BD21	65_SMBALERT	
		65_VRP_A28	

V_1V8 — R1099 1K 0402 — GND

F1 LOGIC
TCDS 40MHZ INPUT

U201-55

ac_nF1_TCDS40_CLK 20	AR16	IO_L11N_T1U_N9_GC_66	VCCO_66 AT16
ac_pF1_TCDS40_CLK 20	AR17	IO_L11P_T1U_N8_GC_66	
ac_nF1_XTAL_200 17	AU16	IO_L12N_T1U_N11_GC_66	
ac_pF1_XTAL_200 17	AT17	IO_L12P_T1U_N10_GC_66	
GND R1243240 0402	AT15	IO_T0U_N12_VRP_66	VREF_66 AR15
	AU15	IO_T3U_N12_66	

V_1V8 — R1227 1K 0402 — GND

FPGA_VU13P_A2577

Title	APOLLO CM W/ DUAL A2577, MK1	
	5.07 FPGA#1 I/O SLR1	
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5.08: FPGA#1 I/O SLR2

THESE BANKS ARE NUMBERED DIFFERENTLY IN THE VU13P AND VU9P, BUT THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#2 FOR THE VU13P AND SLR#1 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
G	70	67
H	71	68

THESE ARE LOGIC-CIRCUIT CLOCKS SOURCED FROM AN ON-BOARD OSCILLATOR, EITHER DIRECTLY OR THROUGH A SYNTHESIZER. THEY MUST BE CONNECTED TO A GLOBAL CLOCK INPUT.

VERIFY THAT A GENERIC I2C BUS CAN BE CONNECTED HERE.

U201-18

T33	IO_L10N_T1U_N7_QBC_AD4N_70	VCCO_70	J37
T32	IO_L10P_T1U_N6_QBC_AD4P_70	VCCO_70	K34
P34	IO_L11N_T1U_N9_GC_70	VCCO_70	N35
P33	IO_L11P_T1U_N8_GC_70	VCCO_70	P32
R33	IO_L12N_T1U_N11_GC_70	VCCO_70	T36
R32	IO_L12P_T1U_N10_GC_70	VCCO_70	U33
M32	IO_L13N_T2L_N1_GC_QBC_70	VCCO_70	
N32	IO_L13P_T2L_N0_GC_QBC_70	VREF_70	W32
N34	IO_L14N_T2L_N3_GC_70		
N33	IO_L14P_T2L_N2_GC_70		
N37	IO_L15N_T2L_N5_AD11N_70		
N36	IO_L15P_T2L_N4_AD11P_70		
M35	IO_L16N_T2U_N7_QBC_AD3N_70		
M34	IO_L16P_T2U_N6_QBC_AD3P_70		
M37	IO_L17N_T2U_N9_AD10N_70		
M36	IO_L17P_T2U_N8_AD10P_70		
L34	IO_L18N_T2U_N11_AD2N_70		
L33	IO_L18P_T2U_N10_AD2P_70		
K35	IO_L19N_T3L_N1_DBC_AD9N_70		
L35	IO_L19P_T3L_N0_DBC_AD9P_70		
V37	IO_L1N_T0L_N1_DBC_70		
V36	IO_L1P_T0L_N0_DBC_70		
J33	IO_L20N_T3L_N3_AD1N_70		
J32	IO_L20P_T3L_N2_AD1P_70		
K37	IO_L21N_T3L_N5_AD8N_70		
L37	IO_L21P_T3L_N4_AD8P_70		
K33	IO_L22N_T3U_N7_DBC_AD0N_70		
K32	IO_L22P_T3U_N6_DBC_AD0P_70		
J36	IO_L23N_T3U_N9_70		
K36	IO_L23P_T3U_N8_70		
J35	IO_L24N_T3U_N11_70		
J34	IO_L24P_T3U_N10_70		
T37	IO_L2N_T0L_N3_70		
U37	IO_L2P_T0L_N2_70		
U36	IO_L3N_T0L_N5_AD15N_70		
V35	IO_L3P_T0L_N4_AD15P_70		
U35	IO_L4N_T0U_N7_DBC_AD7N_70		
U34	IO_L4P_T0U_N6_DBC_AD7P_70		
V34	IO_L5N_T0U_N9_AD14N_70		
V33	IO_L5P_T0U_N8_AD14P_70		
U32	IO_L6N_T0U_N11_AD6N_70		
V32	IO_L6P_T0U_N10_AD6P_70		
P35	IO_L7N_T1L_N1_QBC_AD13N_70		
R35	IO_L7P_T1L_N0_QBC_AD13P_70		
P31	IO_L8N_T1L_N3_AD5N_70		
R31	IO_L8P_T1L_N2_AD5P_70		
R37	IO_L9N_T1L_N5_AD12N_70		
R36	IO_L9P_T1L_N4_AD12P_70		
T35	IO_T0U_N12_VRP_70		
T34	IO_T1U_N12_70		
P36	IO_T2U_N12_70		
L32	IO_T3U_N12_70		

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U201-19

A30	IO_L10N_T1U_N7_QBC_AD4N_71	VCCO_71	B28
B30	IO_L10P_T1U_N6_QBC_AD4P_71	VCCO_71	E29
A29	IO_L11N_T1U_N9_GC_71	VCCO_71	L31
A28	IO_L11P_T1U_N8_GC_71		
C30	IO_L12N_T1U_N11_GC_71	VREF_71	L30
C29	IO_L12P_T1U_N10_GC_71		
J31	IO_L1N_T0L_N1_DBC_71		
K31	IO_L1P_T0L_N0_DBC_71		
H30	IO_L2N_T0L_N3_71		
J29	IO_L2P_T0L_N2_71		
J30	IO_L3N_T0L_N5_AD15N_71		
K30	IO_L3P_T0L_N4_AD15P_71		
G29	IO_L4N_T0U_N7_DBC_AD7N_71		
H29	IO_L4P_T0U_N6_DBC_AD7P_71		
F30	IO_L5N_T0U_N9_AD14N_71		
G30	IO_L5P_T0U_N8_AD14P_71		
F29	IO_L6N_T0U_N11_AD6N_71		
F28	IO_L6P_T0U_N10_AD6P_71		
D29	IO_L7N_T1L_N1_QBC_AD13N_71		
D28	IO_L7P_T1L_N0_QBC_AD13P_71		
D30	IO_L8N_T1L_N3_AD5N_71		
E30	IO_L8P_T1L_N2_AD5P_71		
B29	IO_L9N_T1L_N5_AD12N_71		
C28	IO_L9P_T1L_N4_AD12P_71		
H28	IO_T0U_N12_VRP_71		
E28	IO_T1U_N12_71		

FPGA_VU13P_A2577

ac_nF1L_R0_CLK	18	
ac_pF1L_R0_CLK	18	
ac_nF1R_R0_CLK	18	
ac_pF1R_R0_CLK	18	
ac_nF1_OSC_CLK	17	
ac_pF1_OSC_CLK	17	
lovF1_TO_MCU	22	
lovMCU_TO_F1	22	
lovF1_C2C_OK	22	
I2C_SCL_F1_GENERIC	36	
I2C_SDA_F1_GENERIC	36	

GND — R1228240 0402 — IO_T0U_N12_VRP_70

V_1V8

APOLLO CM W/ DUAL A2577, MK1	
Title	5.08: FPGA#1 I/O SLR2
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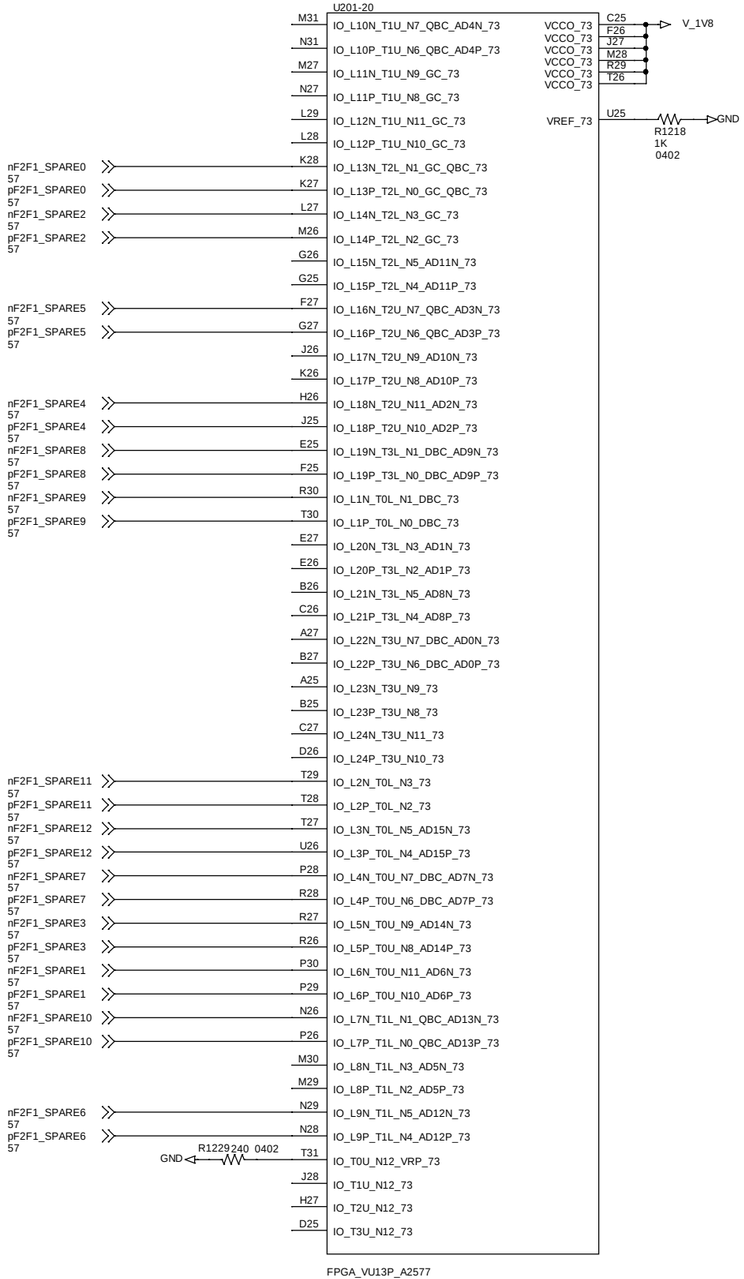
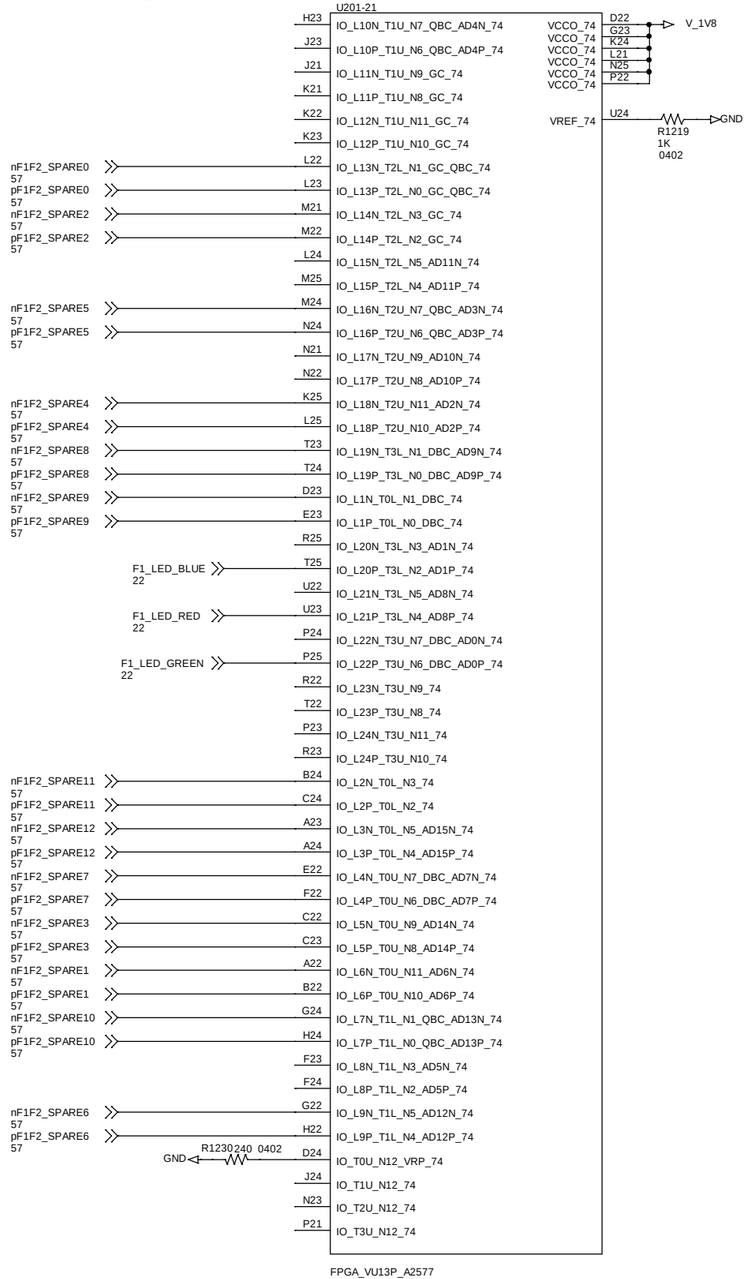
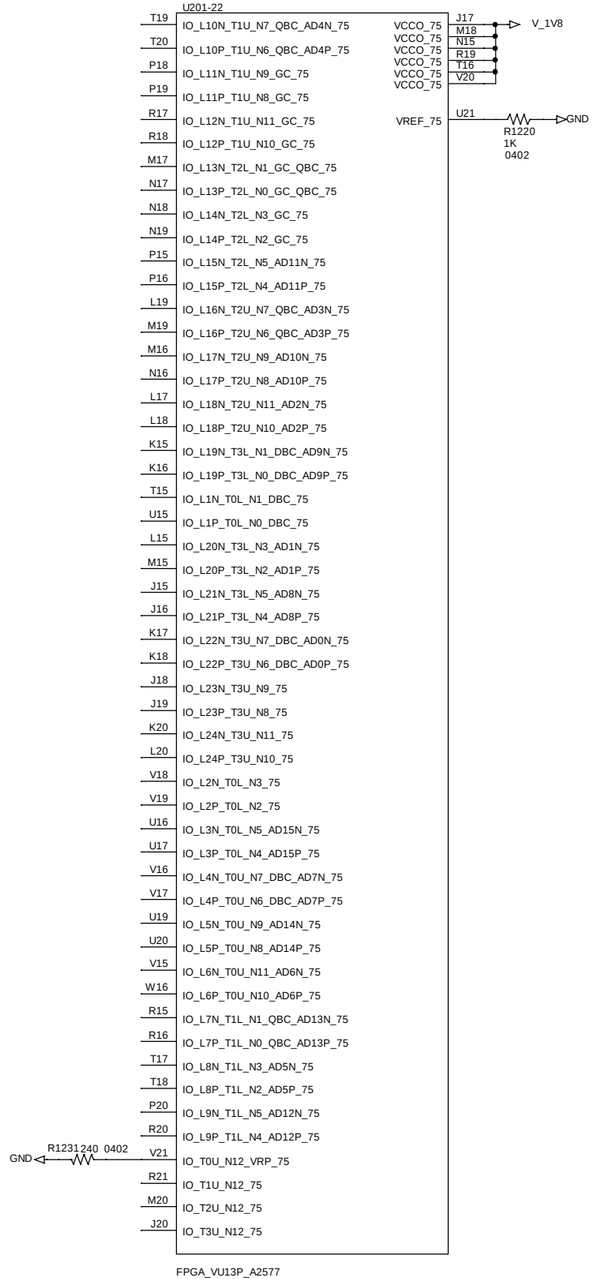
5.09: FPGA#1 I/O SLR3

THESE BANKS ARE NUMBERED DIFFERENTLY IN THE VU13P AND VU9P, BUT THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#3 FOR THE VU13P AND SLR#2 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
I	73	70
J	74	71
K	75	72







THE "F2F1_SPARE" SIGNALS ARE OUTPUTS FROM F2 AND INPUTS TO F1.
THE "F1F2_SPARE" SIGNALS ARE OUTPUTS FROM F1 AND INPUTS TO F2.
THEY ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "_SPARE0" AND "_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE FPGA

APOLLO CM W/ DUAL A2577, MK1
Title: 5.09: FPGA#1 I/O SLR3
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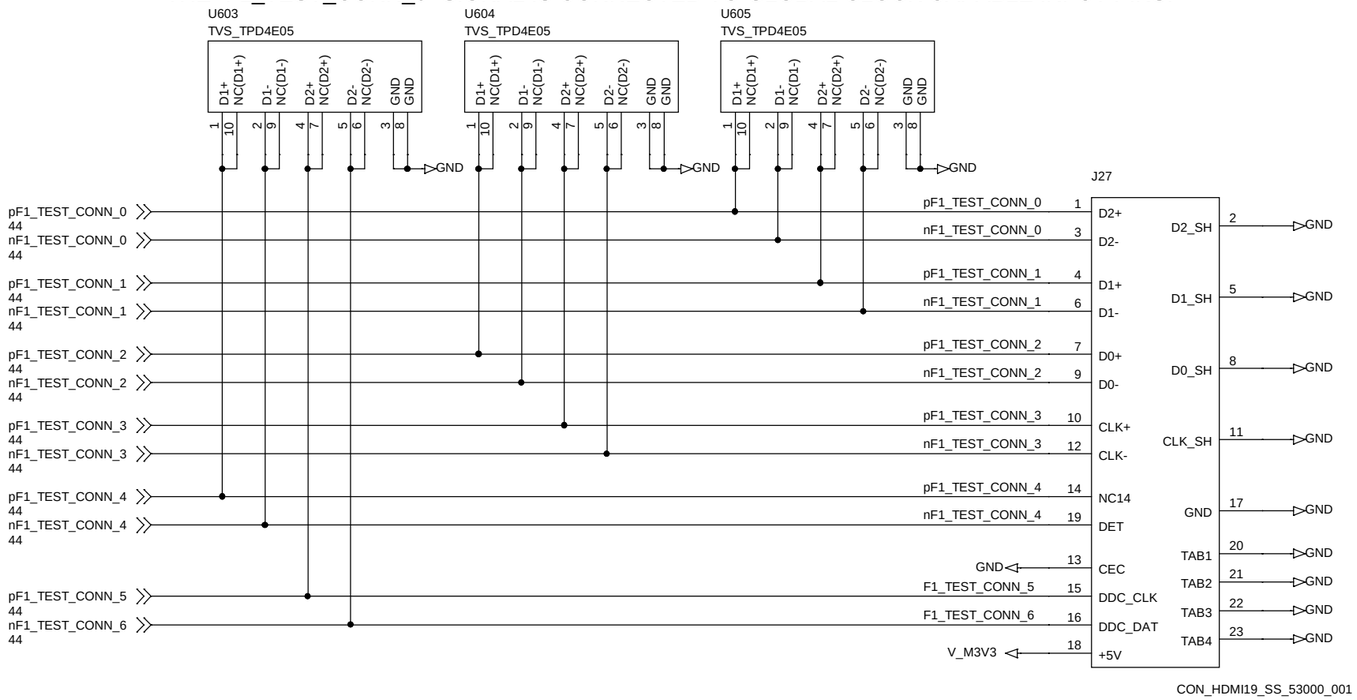
5.10: FPGA#1 TEST CONNECTOR

THIS CONNECTOR IS LOCATED ON THE FRONT PANEL. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

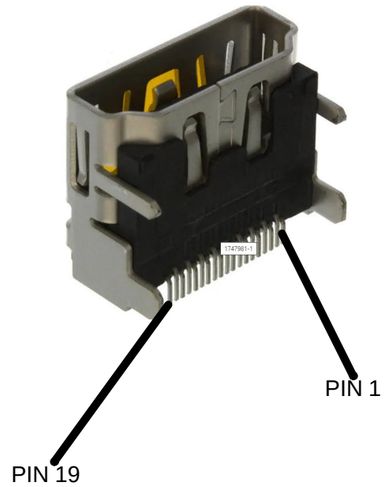
TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

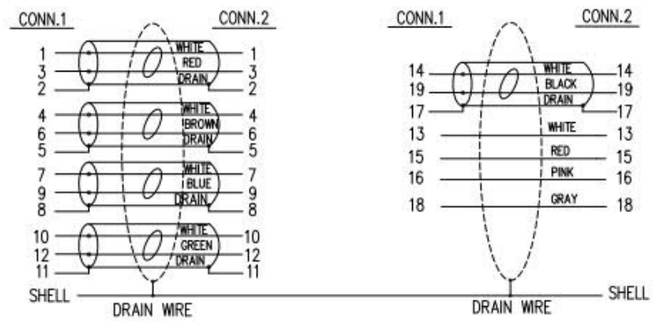
THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "F1_TEST_CONN_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.



PIN ASSIGNMENT





APOLLO CM W/ DUAL A2577, MK1		
Title: 5.10: FPGA#1 TEST CONNECTOR		
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6.01: FPGA#2 GND

U202-1 FPGA_VU13P_A2577

A13	GND	GND	AE12
A16	GND	GND	AE16
A17	GND	GND	AE18
A18	GND	GND	AE20
A21	GND	GND	AE22
A26	GND	GND	AE24
A31	GND	GND	AE26
A34	GND	GND	AE28
A35	GND	GND	AE3
A36	GND	GND	AE30
A39	GND	GND	AE32
A4	GND	GND	AE34
A43	GND	GND	AE36
A45	GND	GND	AE38
A48	GND	GND	AE4
A7	GND	GND	AE40
A9	GND	GND	AE43
AA12	GND	GND	AE47
AA14	GND	GND	AE48
AA16	GND	GND	AE49
AA18	GND	GND	AE5
AA20	GND	GND	AE9
AA22	GND	GND	AF1
AA24	GND	GND	AF10
AA26	GND	GND	AF12
AA28	GND	GND	AF15
AA3	GND	GND	AF17
AA30	GND	GND	AF19
AA32	GND	GND	AF2
AA34	GND	GND	AF21
AA36	GND	GND	AF23
AA38	GND	GND	AF25
AA4	GND	GND	AF27
AA40	GND	GND	AF29
AA43	GND	GND	AF31
AA47	GND	GND	AF33
AA48	GND	GND	AF35
AA49	GND	GND	AF37
AA5	GND	GND	AF39
AA9	GND	GND	AF40
AB1	GND	GND	AF42
AB10	GND	GND	AF45
AB15	GND	GND	AF47
AB17	GND	GND	AF5
AB19	GND	GND	AF50
AB2	GND	GND	AF51
AB21	GND	GND	AF7
AB23	GND	GND	AG12
AB25	GND	GND	AG16
AB27	GND	GND	AG20
AB29	GND	GND	AG22
AB31	GND	GND	AG24
AB33	GND	GND	AG26
AB35	GND	GND	AG28
AB37	GND	GND	AG3
AB38	GND	GND	AG30
AB42	GND	GND	AG32
AB45	GND	GND	AG34
AB47	GND	GND	AG36
AB5	GND	GND	AG38
AB50	GND	GND	AG4
AB51	GND	GND	AG40
AB7	GND	GND	AG44
AC14	GND	GND	AG47
AC16	GND	GND	AG48
AC18	GND	GND	AG49
AC20	GND	GND	AG5
AC22	GND	GND	AG8
AC24	GND	GND	AH1
AC26	GND	GND	AH11
AC28	GND	GND	AH12
AC3	GND	GND	AH15
AC30	GND	GND	AH17
AC32	GND	GND	AH2
AC34	GND	GND	AH21
AC36	GND	GND	AH23
AC38	GND	GND	AH25
AC39	GND	GND	AH27
AC4	GND	GND	AH29
AC44	GND	GND	AH31
AC47	GND	GND	AH33
AC48	GND	GND	AH35
AC49	GND	GND	AH37
AC5	GND	GND	AH39
AC8	GND	GND	AH40
AD1	GND	GND	AH41
AD11	GND	GND	AH46
AD12	GND	GND	AH47
AD15	GND	GND	AH5
AD17	GND	GND	AH50
AD19	GND	GND	AH51
AD2	GND	GND	AH6
AD21	GND	GND	AJ14
AD23	GND	GND	AJ16
AD25	GND	GND	AJ20
AD27	GND	GND	AJ22
AD29	GND	GND	AJ24
AD31	GND	GND	AJ26
AD33	GND	GND	AJ28
AD35	GND	GND	AJ3
AD37	GND	GND	AJ30
AD39	GND	GND	AJ32
AD40	GND	GND	AJ34
AD41	GND	GND	AJ36
AD46	GND	GND	AJ38
AD47	GND	GND	AJ39
AD5	GND	GND	AJ47
AD50	GND	GND	AJ43
AD51	GND	GND	AJ48
AD6	GND	GND	AJ4

GND GND

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AJ49	GND	GND	AP42
AJ5	GND	GND	AP45
AJ9	GND	GND	AP47
AK1	GND	GND	AP5
AK10	GND	GND	AP50
AK15	GND	GND	AP51
AK17	GND	GND	AP7
AK2	GND	GND	AR12
AK21	GND	GND	AR14
AK23	GND	GND	AR22
AK25	GND	GND	AR24
AK27	GND	GND	AR26
AK29	GND	GND	AR28
AK31	GND	GND	AR3
AK33	GND	GND	AR30
AK35	GND	GND	AR38
AK37	GND	GND	AR4
AK38	GND	GND	AR40
AK42	GND	GND	AR44
AK45	GND	GND	AR47
AK47	GND	GND	AR48
AK5	GND	GND	AR49
AK50	GND	GND	AR5
AK51	GND	GND	AR8
AK7	GND	GND	AT1
AL12	GND	GND	AT11
AL14	GND	GND	AT2
AL16	GND	GND	AT21
AL18	GND	GND	AT23
AL20	GND	GND	AT25
AL22	GND	GND	AT27
AL24	GND	GND	AT29
AL26	GND	GND	AT31
AL28	GND	GND	AT38
AL3	GND	GND	AT41
AL30	GND	GND	AT46
AL32	GND	GND	AT47
AL34	GND	GND	AT5
AL36	GND	GND	AT50
AL38	GND	GND	AT51
AL4	GND	GND	AT6
AL40	GND	GND	AU13
AL44	GND	GND	AU14
AL47	GND	GND	AU18
AL48	GND	GND	AU24
AL49	GND	GND	AU26
AL5	GND	GND	AU28
AL8	GND	GND	AU3
AM1	GND	GND	AU30
AM11	GND	GND	AU38
AM15	GND	GND	AU39
AM17	GND	GND	AU4
AM19	GND	GND	AU43
AM2	GND	GND	AU47
AM21	GND	GND	AU48
AM23	GND	GND	AU49
AM25	GND	GND	AU5
AM27	GND	GND	AU9
AM29	GND	GND	AV1
AM31	GND	GND	AV10
AM33	GND	GND	AV15
AM35	GND	GND	AV2
AM37	GND	GND	AV25
AM38	GND	GND	AV35
AM41	GND	GND	AV38
AM46	GND	GND	AV42
AM47	GND	GND	AV45
AM5	GND	GND	AV47
AM50	GND	GND	AV5
AM51	GND	GND	AV50
AM6	GND	GND	AV51
AN12	GND	GND	AV7
AN14	GND	GND	AW12
AN16	GND	GND	AW14
AN18	GND	GND	AW22
AN20	GND	GND	AW3
AN22	GND	GND	AW32
AN24	GND	GND	AW38
AN26	GND	GND	AW4
AN28	GND	GND	AW40
AN3	GND	GND	AW44
AN30	GND	GND	AW47
AN32	GND	GND	AW48
AN34	GND	GND	AW49
AN36	GND	GND	AW5
AN38	GND	GND	AW8
AN4	GND	GND	AY1
AN40	GND	GND	AY11
AN43	GND	GND	AY19
AN47	GND	GND	AY2
AN48	GND	GND	AY29
AN49	GND	GND	AY38
AN5	GND	GND	AY41
AN9	GND	GND	AY46
AP1	GND	GND	AY47
AP10	GND	GND	AY5
AP15	GND	GND	AY50
AP17	GND	GND	AY51
AP19	GND	GND	AY6
AP2	GND	GND	B10
AP21	GND	GND	B14
AP23	GND	GND	B16
AP25	GND	GND	B19
AP27	GND	GND	B20
AP29	GND	GND	B21
AP31	GND	GND	B23
AP33	GND	GND	B3
AP35	GND	GND	B31
AP37	GND	GND	B32
AP38	GND	GND	B33

GND GND

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B36	GND	GND	BG12
B38	GND	GND	BG16
B4	GND	GND	BG17
B42	GND	GND	BG18
B45	GND	GND	BG21
B46	GND	GND	BG28
B47	GND	GND	BG3
B48	GND	GND	BG31
B49	GND	GND	BG34
B5	GND	GND	BG35
B6	GND	GND	BG36
B7	GND	GND	BG4
BA12	GND	GND	BG40
BA14	GND	GND	BG44
BA16	GND	GND	BG45
BA26	GND	GND	BG48
BA3	GND	GND	BG49
BA36	GND	GND	BG7
BA38	GND	GND	BG8
BA4	GND	GND	BH1
BA40	GND	GND	BH11
BA43	GND	GND	BH15
BA47	GND	GND	BH16
BA48	GND	GND	BH19
BA49	GND	GND	BH2
BA5	GND	GND	BH20
BA9	GND	GND	BH21
BB1	GND	GND	BH25
BB10	GND	GND	BH31
BB2	GND	GND	BH32
BB23	GND	GND	BH33
BB33	GND	GND	BH36
BB38	GND	GND	BH37
BB42	GND	GND	BH41
BB45	GND	GND	BH45
BB47	GND	GND	BH46
BB5	GND	GND	BH47
BB50	GND	GND	BH5
BB51	GND	GND	BH50
BB7	GND	GND	BH51
BC12	GND	GND	BH6
BC14	GND	GND	BH7
BC20	GND	GND	BJ13
BC3	GND	GND	BJ16
BC30	GND	GND	BJ17
BC38	GND	GND	BJ18
BC4	GND	GND	BJ2
BC40	GND	GND	BJ21
BC44	GND	GND	BJ22
BC47	GND	GND	BJ3
BC48	GND	GND	BJ31
BC49	GND	GND	BJ34
BC5	GND	GND	BJ35
BC8	GND	GND	BJ36
BD1	GND	GND	BJ39
BD11	GND	GND	BJ4
BD14	GND	GND	BJ43
BD2	GND	GND	BJ45
BD27	GND	GND	BJ48
BD38	GND	GND	BJ49
BD41	GND	GND	BJ50
BD46	GND	GND	BJ7
BD47	GND	GND	BJ9
BD5	GND	GND	BK10
BD50	GND	GND	BK14
BD51	GND	GND	BK16
BD6	GND	GND	BK19
BE12	GND	GND	BK20
BE14	GND	GND	BK21
BE15	GND	GND	BK29
BE16	GND	GND	BK3
BE17	GND	GND	BK31
BE18	GND	GND	BK32
BE19	GND	GND	BK33
BE24	GND	GND	BK36
BE3	GND	GND	BK38
BE33	GND	GND	BK4
BE34	GND	GND	BK42
BE35	GND	GND	BK45
BE36	GND	GND	BK46
BE37	GND	GND	BK47
BE38	GND	GND	BK48
BE4	GND	GND	BK49
BE40	GND	GND	BK5
BE43	GND	GND	BK6
BE47	GND	GND	BK7
BE48	GND	GND	BL12
BE49	GND	GND	BL16
BE5	GND	GND	BL17
BE9	GND	GND	BL18
BF1	GND	GND	BL21
BF10	GND	GND	BL26
BF16	GND	GND	BL31
BF19	GND	GND	BL34
BF2	GND	GND	BL35
BF20	GND	GND	BL36
BF21	GND	GND	BL4
BF31	GND	GND	BL40
BF32	GND	GND	BL44
BF33	GND	GND	BL45
BF36	GND	GND	BL48
BF42	GND	GND	BL7
BF45	GND	GND	BL8
BF46	GND	GND	C12
BF47	GND	GND	C16
BF5	GND	GND	C17
BF50	GND	GND	C18
BF51	GND	GND	C2
BF6	GND	GND	C21
BF7	GND	GND	C3

GND GND

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C31	GND	GND	H35
C34	GND	GND	H36
C35	GND	GND	H37
C36	GND	GND	H38
C4	GND	GND	H41
C40	GND	GND	H46
C44	GND	GND	H47
C45	GND	GND	H5
C48	GND	GND	H50
C49	GND	GND	H51
C50	GND	GND	H6
C7	GND	GND	J12
C8	GND	GND	J14
D1	GND	GND	J22
D11	GND	GND	J3
D15	GND	GND	J38
D16	GND	GND	J4
D19	GND	GND	J40
D2	GND	GND	J43
D20	GND	GND	J47
D21	GND	GND	J48
D27	GND	GND	J49
D31	GND	GND	J5
D32	GND	GND	J9
D33	GND	GND	K1
D36	GND	GND	K10
D37	GND	GND	K14
D41	GND	GND	K19
D45	GND	GND	K2
D46	GND	GND	K29
D47	GND	GND	K38
D5	GND	GND	K42
D50	GND	GND	K45
D51	GND	GND	K47
D6	GND	GND	K5
D7	GND	GND	K50
E12	GND	GND	K51
E16	GND	GND	K7
E17	GND	GND	L12
E18	GND	GND	L14
E21	GND	GND	L16
E24	GND	GND	L26
E3	GND	GND	L3
E31	GND	GND	L36
E34	GND	GND	L38
E35	GND	GND	L4
E36	GND	GND	L40
E39	GND	GND	L44
E4	GND	GND	L47
E43	GND	GND	L48
E45	GND	GND	L49
E48	GND	GND	L5
E49	GND	GND	L8
E7	GND	GND	M1
E9	GND	GND	M11
F1	GND	GND	M2
F10	GND	GND	M23
F14	GND	GND	M33
F16	GND	GND	M38
F19	GND	GND	M41
F2	GND	GND	M46
F20	GND	GND	M47
F21	GND	GND	M5
F31	GND	GND	M50
F32	GND	GND	M51
F33	GND	GND	M6
F36	GND	GND	N13
F38	GND	GND	N14
F42	GND	GND	N20
F45	GND	GND	N3
F46	GND	GND	N30
F47	GND	GND	N38
F5	GND	GND	N39
F50	GND	GND	N4
F51	GND	GND	N43
F6	GND	GND	N47
F7	GND	GND	N48
G12	GND	GND	N49
G16	GND	GND	N5
G18	GND	GND	N9
G21	GND	GND	P1
G28	GND	GND	P10
G3	GND	GND	P17
G31	GND	GND	P2
G34	GND	GND	P27
G36	GND	GND	P37
G4	GND	GND	P38
G40	GND	GND	P42
G44	GND	GND	P45
G47	GND	GND	P47
G48	GND	GND	P5
G49	GND	GND	P50
G5	GND	GND	P51
G8	GND	GND	P7
H1	GND	GND	R12
H11	GND	GND	R14
H14	GND	GND	R24
H15	GND	GND	R3
H16	GND	GND	R34
H17	GND	GND	R38
H18	GND	GND	R4
H19	GND	GND	R40
H2	GND	GND	R44
H20	GND	GND	R47
H21	GND	GND	R48
H25	GND	GND	R49
H31	GND	GND	R5
H32	GND	GND	R8
H33	GND	GND	T1
H34	GND	GND	T11

GND GND

U202-5 FPGA_VU13P_A2577

T2	GND
T21	GND
T38	GND
T41	GND
T46	GND
T47	GND
T5	GND
T50	GND
T51	GND
T6	GND
U13	GND
U14	GND
U18	GND
U28	GND
U3	GND
U30	GND
U38	GND
U39	GND
U4	GND
U43	GND
U47	GND
U48	GND
U49	GND
U5	GND
U9	GND
V1	GND
V10	GND
V2	GND
V23	GND
V25	GND
V27	GND
V29	GND
V31	GND
V38	GND
V42	GND
V45	GND
V47	GND
V5	GND
V50	GND
V51	GND
V7	GND
W12	GND
W14	GND
W18	GND
W20	GND
W22	GND
W24	GND
W26	GND
W28	GND
W3	GND
W30	GND
W34	GND
W36	GND
W38	GND
W4	GND
W40	GND
W44	GND
W47	GND
W48	GND
W49	GND
W5	GND
W8	GND
Y1	GND
Y11	GND
Y15	GND
Y17	GND
Y19	GND
Y2	GND
Y21	GND
Y23	GND
Y25	GND
Y27	GND
Y29	GND
Y31	GND
Y33	GND
Y35	GND
Y37	GND
Y38	GND
Y41	GND
Y46	GND
Y47	GND
Y5	GND
Y50	GND
Y51	GND

GND

R1121 10K 0603

V_M3V3

GND Y6

/F2_INSTALLED
22

IF THE FPGA IS INSTALLED, THEN THE ACTIVE-LO "/F2_INSTALLED" SIGNAL WILL BE PULLED TO GND. IF THE FPGA IS NOT INSTALLED, THE SIGNAL WILL BE HI.

ANY FPGA GND PIN CAN BE USED.

APOLLO CM W/ DUAL A2577, MK1

Title: 6.01: FPGA#2 GND

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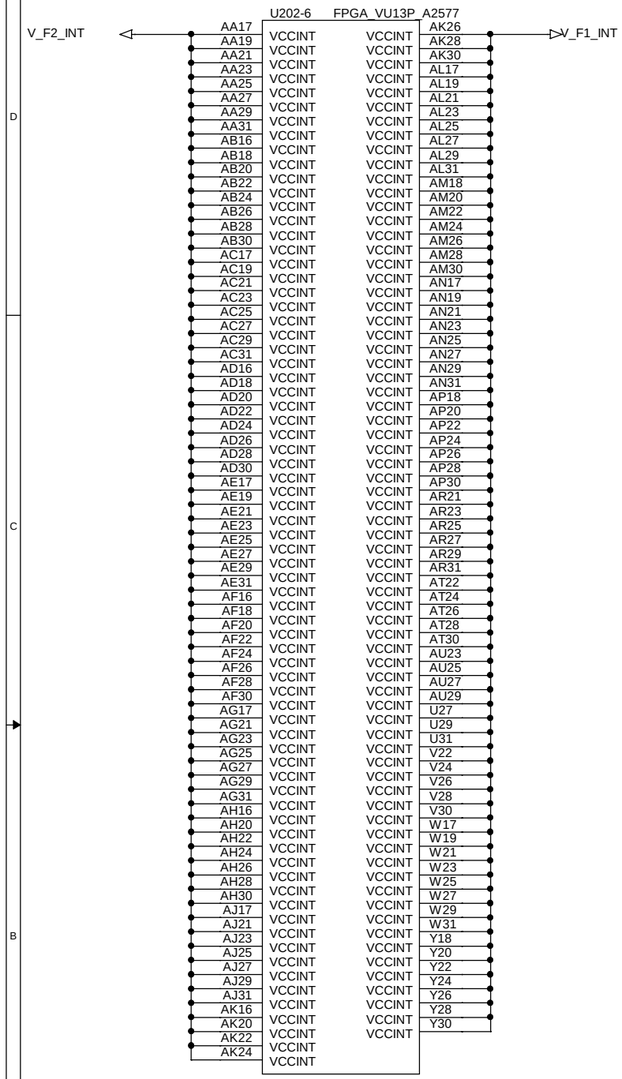
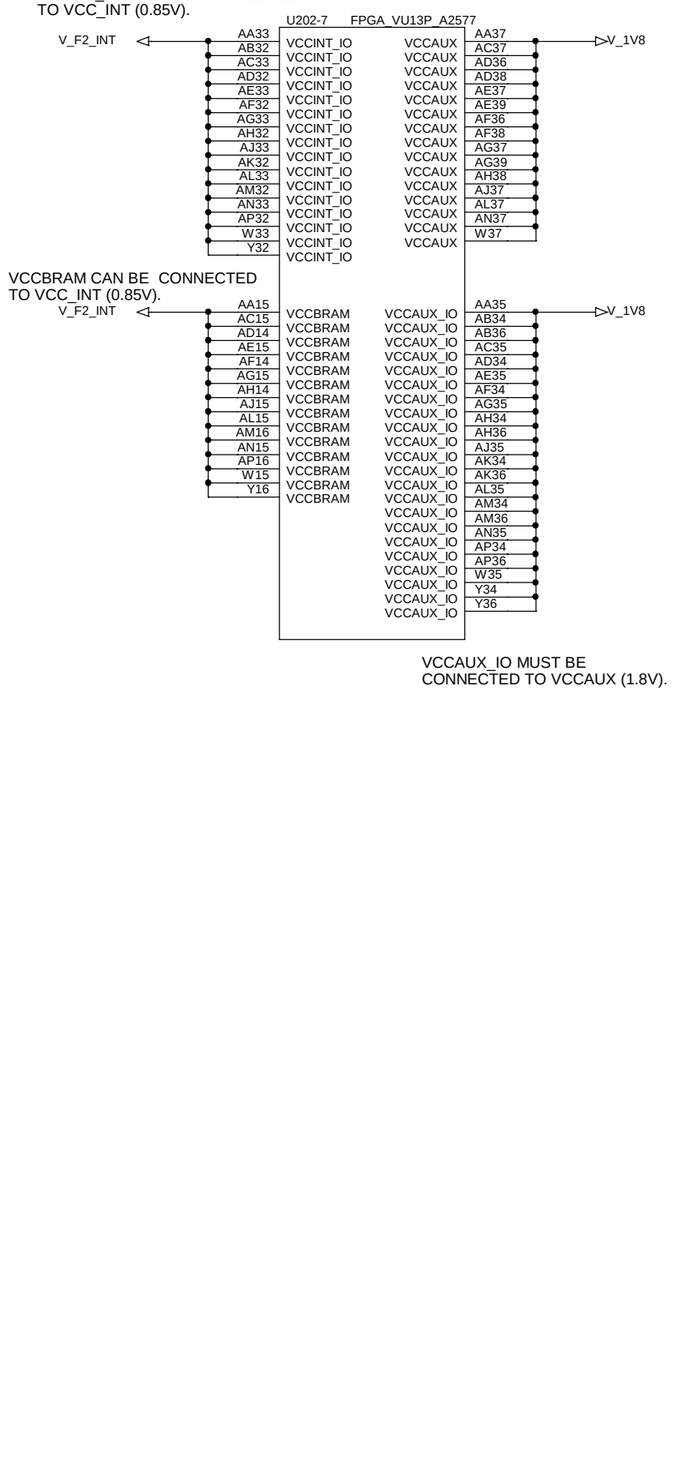
6.02: FPGA#2 POWER INTERNAL

VCCINT MUST BE 0.85V.

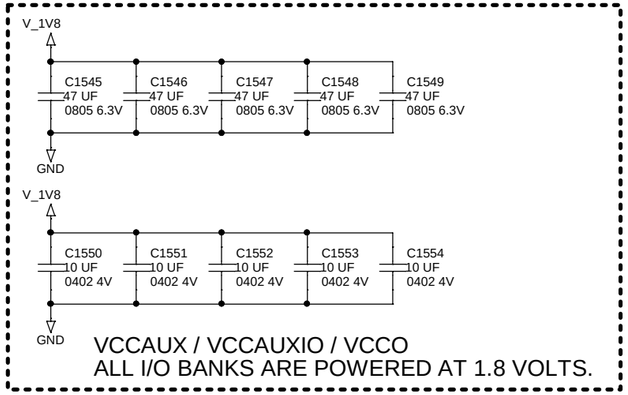


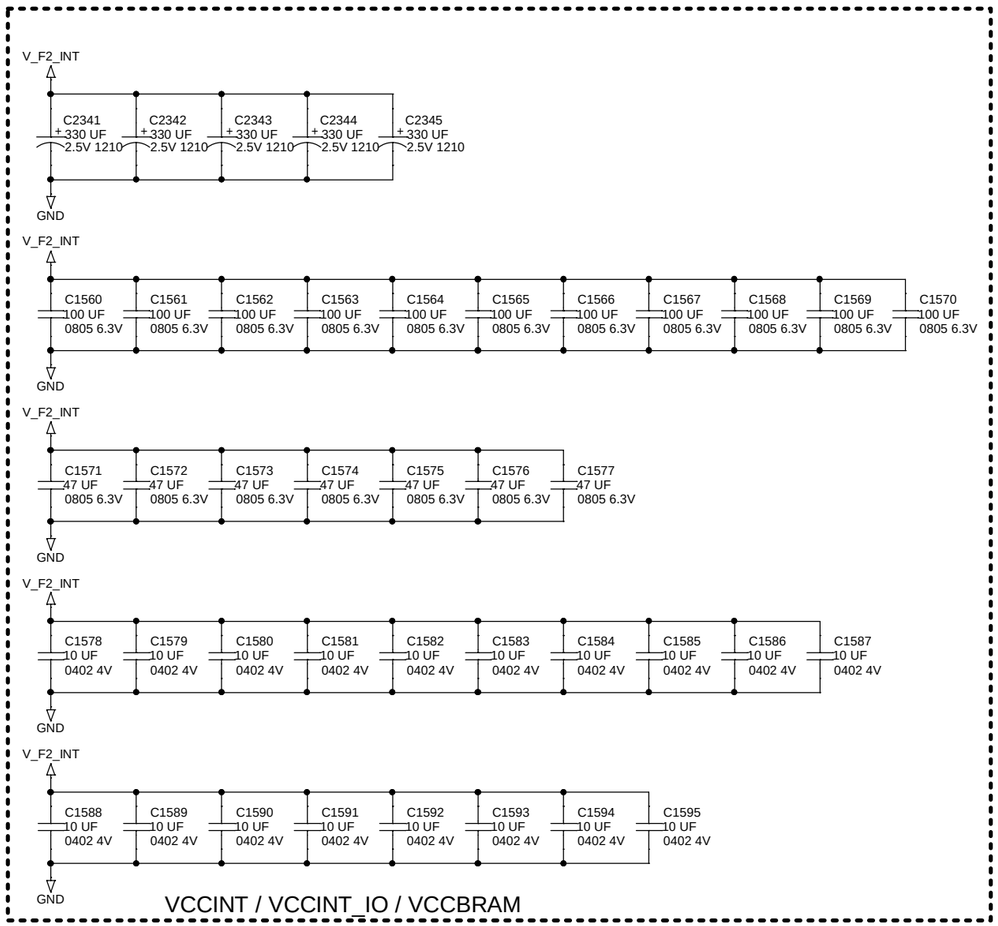
VCCINT_IO MUST BE CONNECTED TO VCC_INT (0.85V).

VCCBRAM CAN BE CONNECTED TO VCC_INT (0.85V).



VCCAUX_IO MUST BE CONNECTED TO VCCAUX (1.8V).





BYPASS CAPACITOR VALUES AND QUANTITIES FROM "UG583 UltraScale Architecture PCB Design"

APOLLO CM W/ DUAL A2577, MK1		
Title: 6.02: FPGA#2 POWER INTERNAL		
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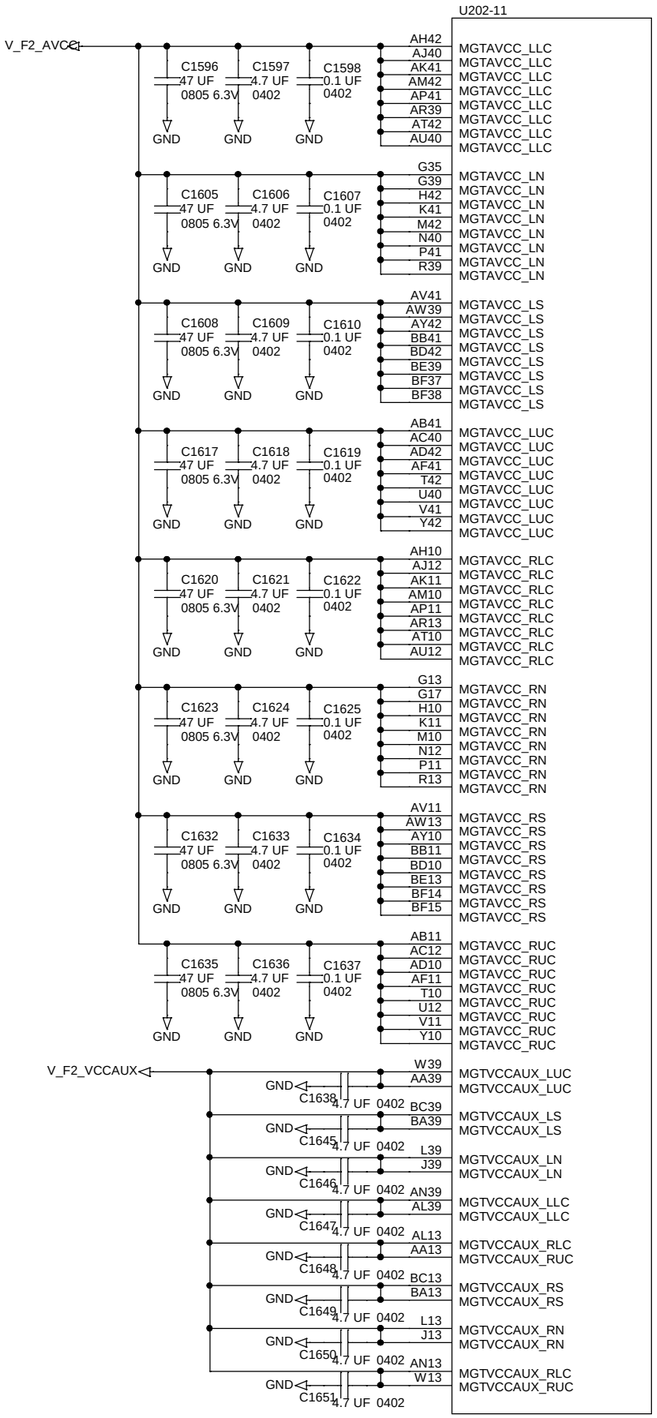
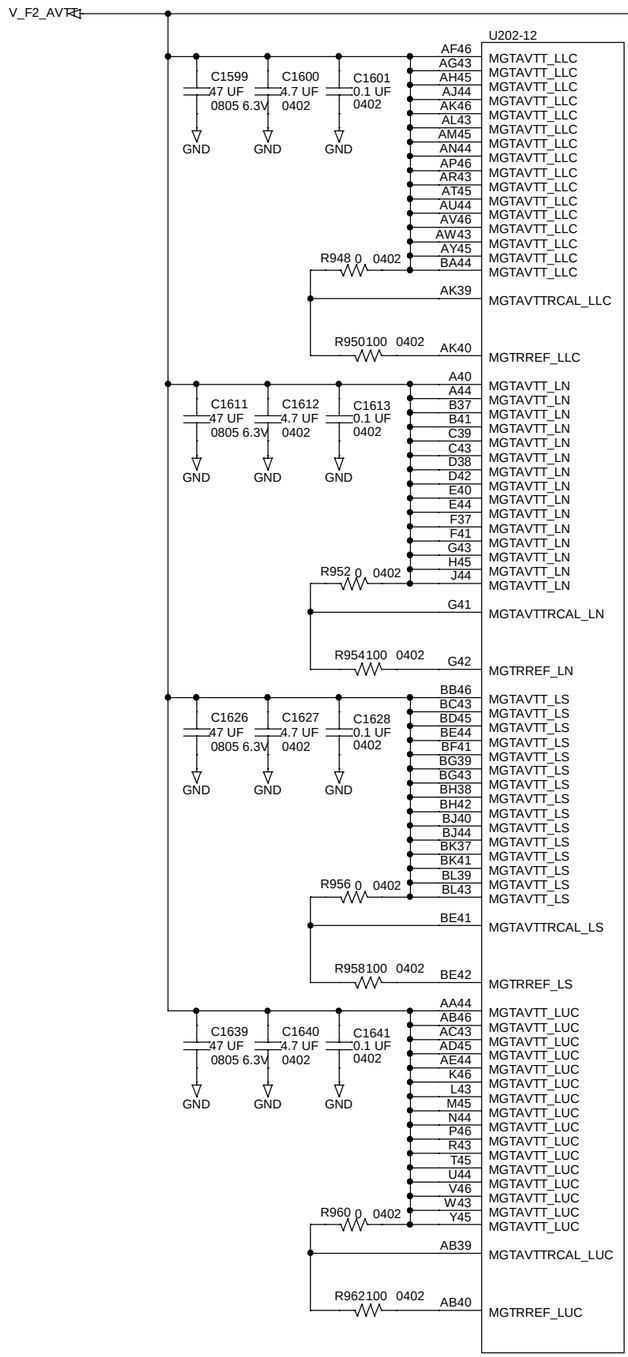
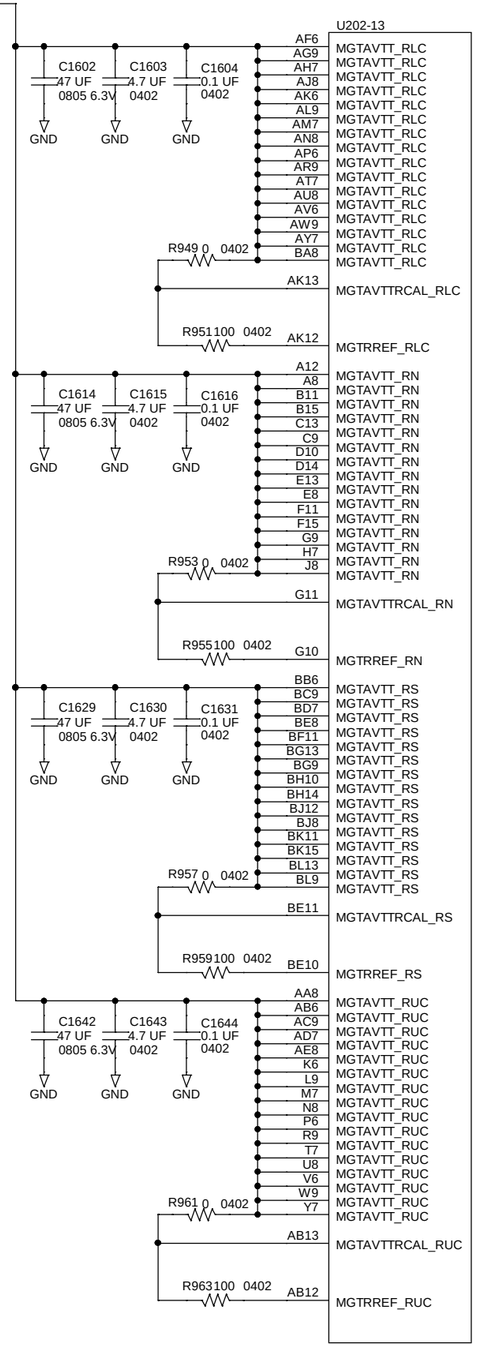
6.03: FPGA#2 GTY TRANSCEIVER POWER







REFER TO THE GTY USER GUIDE FOR DETAILS ON TRACE ROUTING FOR THE MGTRREF RESISTOR.

PLACE CAPACITORS AND RESISTORS THAT ARE ON THIS SHEET NEAR THE BGA PINS.

APOLLO CM W/ DUAL A2577, MK1		
Title: 6.03: FPGA#2 GTY TRANSCEIVER POWER		
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6.04: FPGA#2 CONFIGURATION

MUST BE TIED TO "VCCINT" OR "GND". DO NOT CONNECT TO "VCCO_0". CONNECT TO "GND" FOR STANDARD POR DELAY.

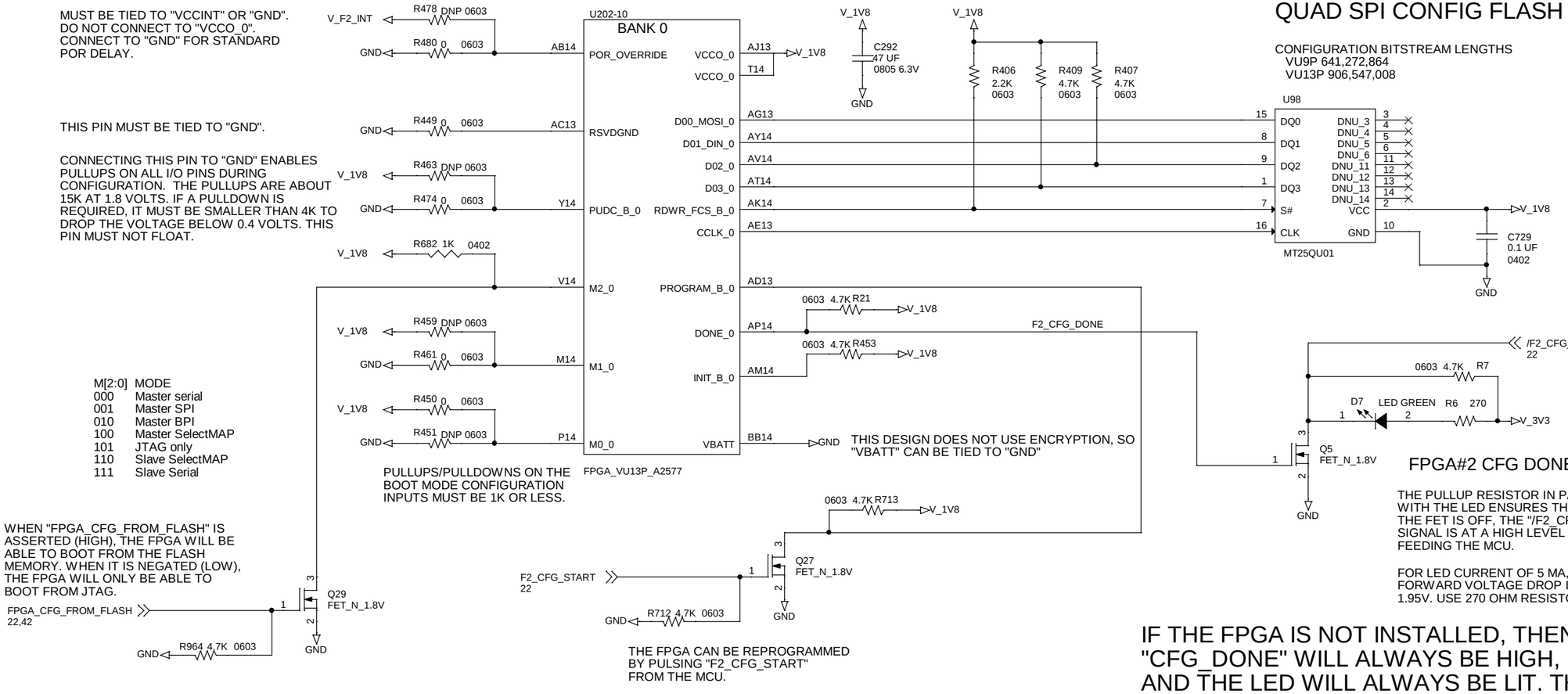
THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

PULLUPS/PULLDOWNS ON THE BOOT MODE CONFIGURATION INPUTS MUST BE 1K OR LESS.

WHEN "FPGA_CFG_FROM_FLASH" IS ASSERTED (HIGH), THE FPGA WILL BE ABLE TO BOOT FROM THE FLASH MEMORY. WHEN IT IS NEGATED (LOW), THE FPGA WILL ONLY BE ABLE TO BOOT FROM JTAG.



QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
VU9P 641,272,864
VU13P 906,547,008

FPGA#2 CFG DONE LED

THE PULLUP RESISTOR IN PARALLEL WITH THE LED ENSURES THAT, WHEN THE FET IS OFF, THE "/F2_CFG_DONE" SIGNAL IS AT A HIGH LEVEL FOR FEEDING THE MCU.

FOR LED CURRENT OF 5 MA, THE FORWARD VOLTAGE DROP IS 1.95V. USE 270 OHM RESISTOR.

IF THE FPGA IS NOT INSTALLED, THEN "CFG_DONE" WILL ALWAYS BE HIGH, AND THE LED WILL ALWAYS BE LIT. THIS IS UNINTENDED AND UNDESIRABLE. CONSIDER ELIMINATING THE FPGA DONE LED,OR ADD A GATE.

APOLLO CM W/ DUAL A2577, MK1		
Title: 6.04: FPGA#2 CONFIGURATION		
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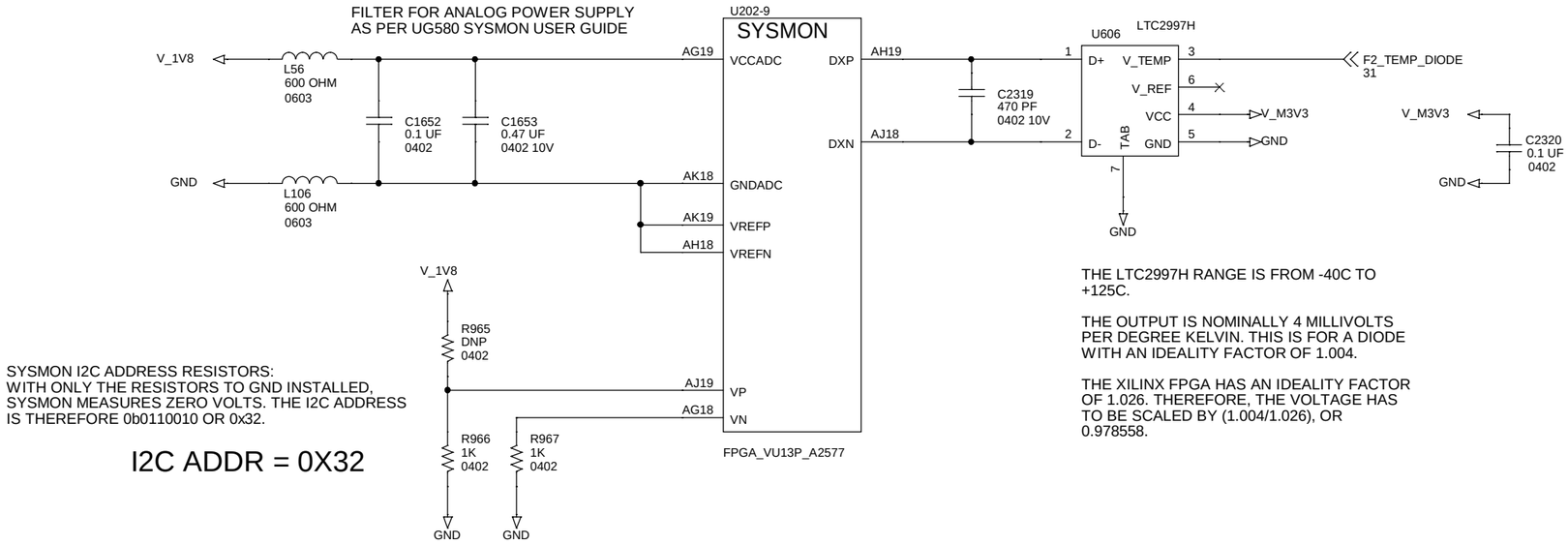
6.05: FPGA#2 SYSTEM MONITOR



APOLLO CM W/ DUAL A2577, MK1		
Title: 6.05: FPGA#2 SYSTEM MONITOR		
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6.06 FPGA#2 I/O SLR0

THESE BANKS ARE NUMBERED THE SAME IN THE VU13P AND VU9P, AND THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#0 FOR THE VU13P AND SLR#0 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
D	61	61
E	62	62
F	63	63

U202-14

BE20 IO_L10N_T1U_N7_QBC_AD4N_61
BE21 IO_L10P_T1U_N6_QBC_AD4P_61
BF22 IO_L11N_T1U_N9_GC_61
BE22 IO_L11P_T1U_N8_GC_61
BE23 IO_L12N_T1U_N11_GC_61
BD23 IO_L12P_T1U_N10_GC_61
BD24 IO_L13N_T2L_N1_GC_QBC_61
BD25 IO_L13P_T2L_N0_GC_QBC_61
BC23 IO_L14N_T2L_N3_GC_61
BC24 IO_L14P_T2L_N2_GC_61
BB25 IO_L15N_T2L_N5_AD11N_61
BB26 IO_L15P_T2L_N4_AD11P_61
BD26 IO_L16N_T2U_N7_QBC_AD3N_61
BC26 IO_L16P_T2U_N6_QBC_AD3P_61
BA24 IO_L17N_T2U_N9_AD10N_61
BA25 IO_L17P_T2U_N8_AD10P_61
BC22 IO_L18N_T2U_N11_AD2N_61
BB22 IO_L18P_T2U_N10_AD2P_61
AW24 IO_L19N_T3L_N1_DBC_AD9N_61
AW25 IO_L19P_T3L_N0_DBC_AD9P_61
BL23 IO_L1N_T0L_N1_DBC_61
BL24 IO_L1P_T0L_N0_DBC_61
AW23 IO_L20N_T3L_N3_AD1N_61
AV24 IO_L20P_T3L_N2_AD1P_61
BA23 IO_L21N_T3L_N5_AD8N_61
AY23 IO_L21P_T3L_N4_AD8P_61
BA27 IO_L22N_T3U_N7_DBC_AD0N_61
AY27 IO_L22P_T3U_N6_DBC_AD0P_61
AY26 IO_L23N_T3U_N9_61
AW26 IO_L23P_T3U_N8_61
AV26 IO_L24N_T3U_N11_61
AV27 IO_L24P_T3U_N10_61
BL22 IO_L2N_T0L_N3_61
BK22 IO_L2P_T0L_N2_61
BJ24 IO_L3N_T0L_N5_AD15N_61
BJ25 IO_L3P_T0L_N4_AD15P_61
BK23 IO_L4N_T0U_N7_DBC_AD7N_61
BJ23 IO_L4P_T0U_N6_DBC_AD7P_61
BL25 IO_L5N_T0U_N9_AD14N_61
BK25 IO_L5P_T0U_N8_AD14P_61
BH23 IO_L6N_T0U_N11_AD6N_61
BH24 IO_L6P_T0U_N10_AD6P_61
BG24 IO_L7N_T1L_N1_QBC_AD13N_61
BG25 IO_L7P_T1L_N0_QBC_AD13P_61
BG22 IO_L8N_T1L_N3_AD5N_61
BF23 IO_L8P_T1L_N2_AD5P_61
BF24 IO_L9N_T1L_N5_AD12N_61
BF25 IO_L9P_T1L_N4_AD12P_61
BH22 IO_T0U_N12_VRP_61
BE25 IO_T1U_N12_61
BB24 IO_T2U_N12_61
AY25 IO_T3U_N12_61

VCCO_61 AW27 AY24 BC25 BD22 BG23 BK24
V_1V8
VREF_61 AV23
R1233 1K 0402
GND

R1236 240 0402
GND

FPGA_VU13P_A2577

THESE SIGNALS MAY BE ASSIGNED TO DIFFERENT PINS OR A DIFFERENT BLOCK DURING LAYOUT TO SIMPLIFY ROUTING. KEEP FPGA CLOCK INPUTS ON "GC" PINS.

nF2_TEST_CONN_0 58
pF2_TEST_CONN_0 58
F2_TEST_CONN_5 58
F2_TEST_CONN_6 58
nF2_TEST_CONN_4 58
pF2_TEST_CONN_4 58
nF2_TEST_CONN_3 58
pF2_TEST_CONN_3 58
nF2_TEST_CONN_2 58
pF2_TEST_CONN_2 58
nF2_TEST_CONN_1 58
pF2_TEST_CONN_1 58

C2491 0.1 UF 0402
ac_nF2_TCDS_RECOV_CLK
R1235 DNP 0603
C2492 0.1 UF 0402
ac_pF2_TCDS_RECOV_CLK
bc_nF2_TCDS_RECOV_CLK
bc_pF2_TCDS_RECOV_CLK

THIS IS THE 40 MHZ RECOVERED TCDS CLOCK.
THE CLOCK FROM FPGA#2 IS NOT USED ANYWHERE, BUT THE PINS ARE RESERVED. THE "DNP" RESISTOR PADS GIVE THE NETS TWO CONNECTIONS.

U202-15

BH27 IO_L10N_T1U_N7_QBC_AD4N_62
BH26 IO_L10P_T1U_N6_QBC_AD4P_62
BF28 IO_L11N_T1U_N9_GC_62
BF27 IO_L11P_T1U_N8_GC_62
BE27 IO_L12N_T1U_N11_GC_62
BE26 IO_L12P_T1U_N10_GC_62
BD29 IO_L13N_T2L_N1_GC_QBC_62
BC28 IO_L13P_T2L_N0_GC_QBC_62
BE28 IO_L14N_T2L_N3_GC_62
BD28 IO_L14P_T2L_N2_GC_62
BE30 IO_L15N_T2L_N5_AD11N_62
BD30 IO_L15P_T2L_N4_AD11P_62
BC27 IO_L16N_T2U_N7_QBC_AD3N_62
BB27 IO_L16P_T2U_N6_QBC_AD3P_62
BC31 IO_L17N_T2U_N9_AD10N_62
BB31 IO_L17P_T2U_N8_AD10P_62
BC29 IO_L18N_T2U_N11_AD2N_62
BB29 IO_L18P_T2U_N10_AD2P_62
BA29 IO_L19N_T3L_N1_DBC_AD9N_62
BA28 IO_L19P_T3L_N0_DBC_AD9P_62
BJ28 IO_L1N_T0L_N1_DBC_62
BH28 IO_L1P_T0L_N0_DBC_62
AY28 IO_L20N_T3L_N3_AD1N_62
AW28 IO_L20P_T3L_N2_AD1P_62
BA30 IO_L21N_T3L_N5_AD8N_62
AY30 IO_L21P_T3L_N4_AD8P_62
AV31 IO_L22N_T3U_N7_DBC_AD0N_62
AU31 IO_L22P_T3U_N6_DBC_AD0P_62
AW29 IO_L23N_T3U_N9_62
AV29 IO_L23P_T3U_N8_62
AY31 IO_L24N_T3U_N11_62
AW31 IO_L24P_T3U_N10_62
BL28 IO_L2N_T0L_N3_62
BL27 IO_L2P_T0L_N2_62
BJ30 IO_L3N_T0L_N5_AD15N_62
BJ29 IO_L3P_T0L_N4_AD15P_62
BK28 IO_L4N_T0U_N7_DBC_AD7N_62
BK27 IO_L4P_T0U_N6_DBC_AD7P_62
BL30 IO_L5N_T0U_N9_AD14N_62
BK30 IO_L5P_T0U_N8_AD14P_62
BK26 IO_L6N_T0U_N11_AD6N_62
BJ26 IO_L6P_T0U_N10_AD6P_62
BG27 IO_L7N_T1L_N1_QBC_AD13N_62
BG26 IO_L7P_T1L_N0_QBC_AD13P_62
BG30 IO_L8N_T1L_N3_AD5N_62
BF29 IO_L8P_T1L_N2_AD5P_62
BH29 IO_L9N_T1L_N5_AD12N_62
BG29 IO_L9P_T1L_N4_AD12P_62
BL29 IO_T0U_N12_VRP_62
BF30 IO_T1U_N12_62
BB30 IO_T2U_N12_62
AW30 IO_T3U_N12_62

VCCO_62 AV30 BA31 BB28 BE29 BF26 BH30 BJ27
V_1V8
VREF_62 AV28
R1232 1K 0402
GND

R1237 240 0402
GND

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U202-16

BC36 IO_L10N_T1U_N7_QBC_AD4N_63
BB36 IO_L10P_T1U_N6_QBC_AD4P_63
BB35 IO_L11N_T1U_N9_GC_63
BA35 IO_L11P_T1U_N8_GC_63
BB34 IO_L12N_T1U_N11_GC_63
BA34 IO_L12P_T1U_N10_GC_63
AW36 IO_L13N_T2L_N1_GC_QBC_63
AW35 IO_L13P_T2L_N0_GC_QBC_63
AY36 IO_L14N_T2L_N3_GC_63
AY35 IO_L14P_T2L_N2_GC_63
AV37 IO_L15N_T2L_N5_AD11N_63
AV36 IO_L15P_T2L_N4_AD11P_63
AV33 IO_L16N_T2U_N7_QBC_AD3N_63
AV32 IO_L16P_T2U_N6_QBC_AD3P_63
AW34 IO_L17N_T2U_N9_AD10N_63
AW33 IO_L17P_T2U_N8_AD10P_63
AV34 IO_L18N_T2U_N11_AD2N_63
AU34 IO_L18P_T2U_N10_AD2P_63
AU37 IO_L19N_T3L_N1_DBC_AD9N_63
AU36 IO_L19P_T3L_N0_DBC_AD9P_63
BE32 IO_L1N_T0L_N1_DBC_63
BE31 IO_L1P_T0L_N0_DBC_63
AU32 IO_L20N_T3L_N3_AD1N_63
AT32 IO_L20P_T3L_N2_AD1P_63
AR37 IO_L21N_T3L_N5_AD8N_63
AR36 IO_L21P_T3L_N4_AD8P_63
AT34 IO_L22N_T3U_N7_DBC_AD0N_63
AT33 IO_L22P_T3U_N6_DBC_AD0P_63
AT35 IO_L23N_T3U_N9_63
AR35 IO_L23P_T3U_N8_63
AR34 IO_L24N_T3U_N11_63
AR33 IO_L24P_T3U_N10_63
BC32 IO_L2N_T0L_N3_63
BB32 IO_L2P_T0L_N2_63
BA32 IO_L3N_T0L_N5_AD15N_63
AY32 IO_L3P_T0L_N4_AD15P_63
BA33 IO_L4N_T0U_N7_DBC_AD7N_63
AY33 IO_L4P_T0U_N6_DBC_AD7P_63
BD33 IO_L5N_T0U_N9_AD14N_63
BC33 IO_L5P_T0U_N8_AD14P_63
BD34 IO_L6N_T0U_N11_AD6N_63
BC34 IO_L6P_T0U_N10_AD6P_63
BD36 IO_L7N_T1L_N1_QBC_AD13N_63
BD35 IO_L7P_T1L_N0_QBC_AD13P_63
BD37 IO_L8N_T1L_N3_AD5N_63
BC37 IO_L8P_T1L_N2_AD5P_63
BB37 IO_L9N_T1L_N5_AD12N_63
BA37 IO_L9P_T1L_N4_AD12P_63
BD31 IO_T0U_N12_VRP_63
AY37 IO_T1U_N12_63
AU35 IO_T2U_N12_63
AT37 IO_T3U_N12_63

VCCO_63 AT36 AU33 AW37 AY34 BC35 BD32
V_1V8
VREF_63 AR32
R1234 1K 0402
GND

R1238 240 0402
GND

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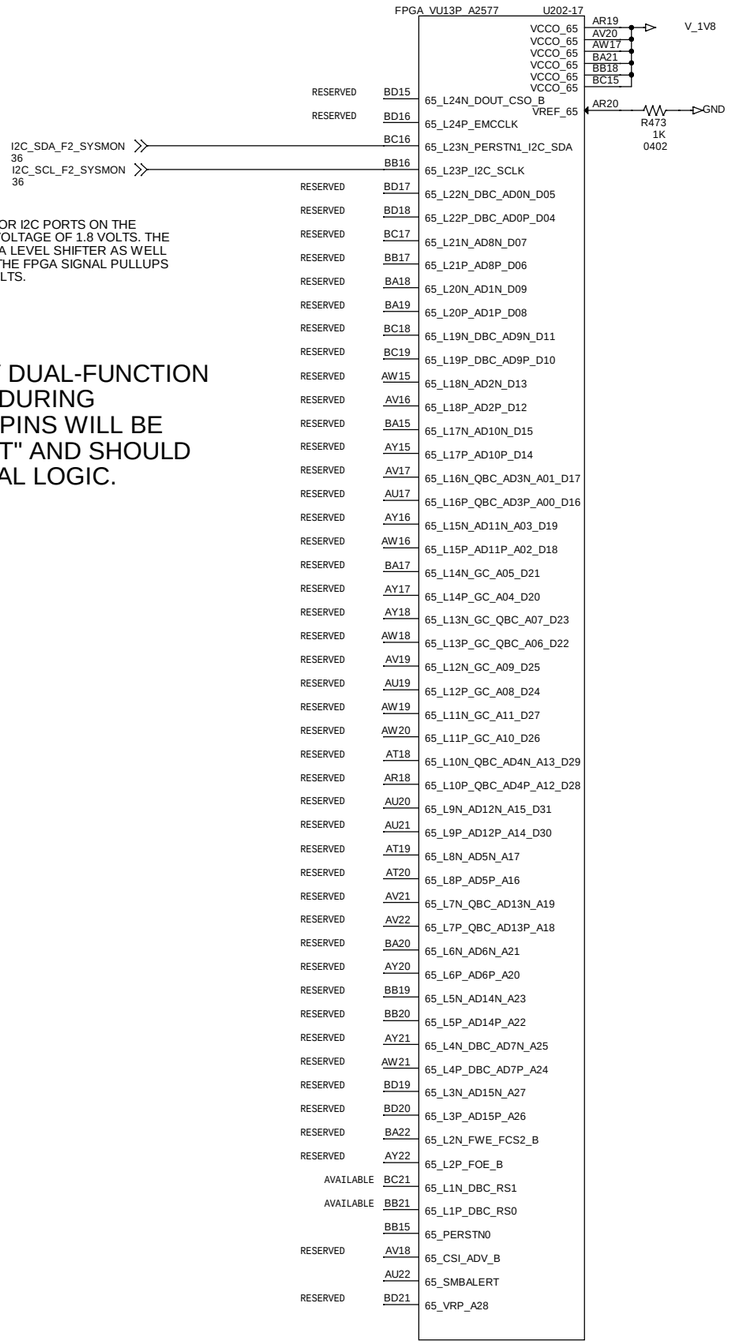
6.07 FPGA#2 I/O SLR1

THESE BANKS ARE NUMBERED THE SAME IN THE VU13P AND VU9P, AND THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#1 FOR THE VU13P AND SLR#1 FOR THE VU9P.

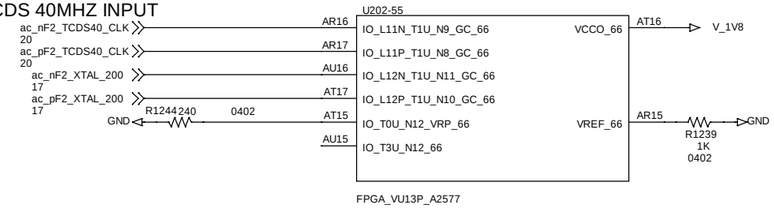
SITE	VU13P BANK	VU9P BANK
C	65	65
B	66	66



THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

F2 LOGIC
TCDS 40MHZ INPUT



APOLLO CM W/ DUAL A2577, MK1				
Title: 6.07 FPGA#2 I/O SLR1				
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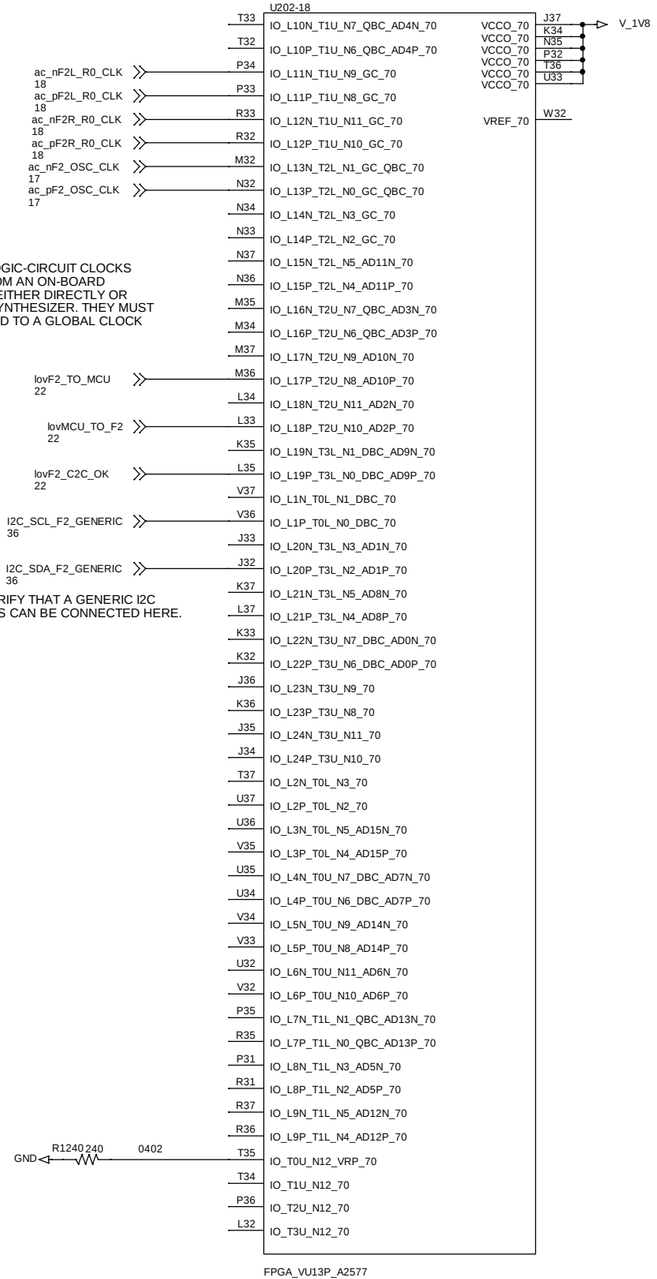
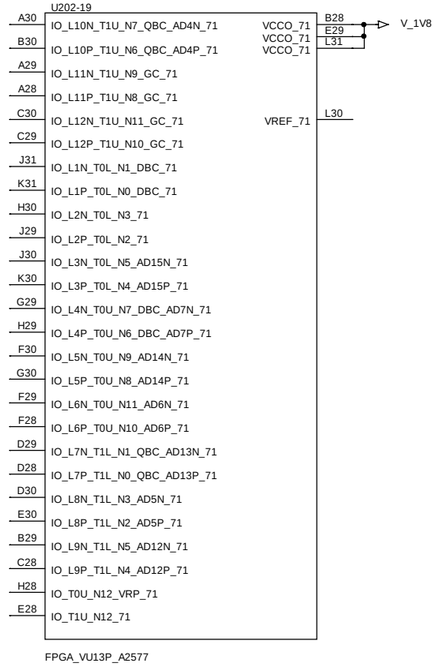
THESE BANKS ARE NUMBERED DIFFERENTLY IN THE VU13P AND VU9P, BUT THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#2 FOR THE VU13P AND SLR#1 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
G	70	67
H	71	68





APOLLO CM W/ DUAL A2577, MK1			
Title: 6.08: FPGA#2 I/O SLR2			
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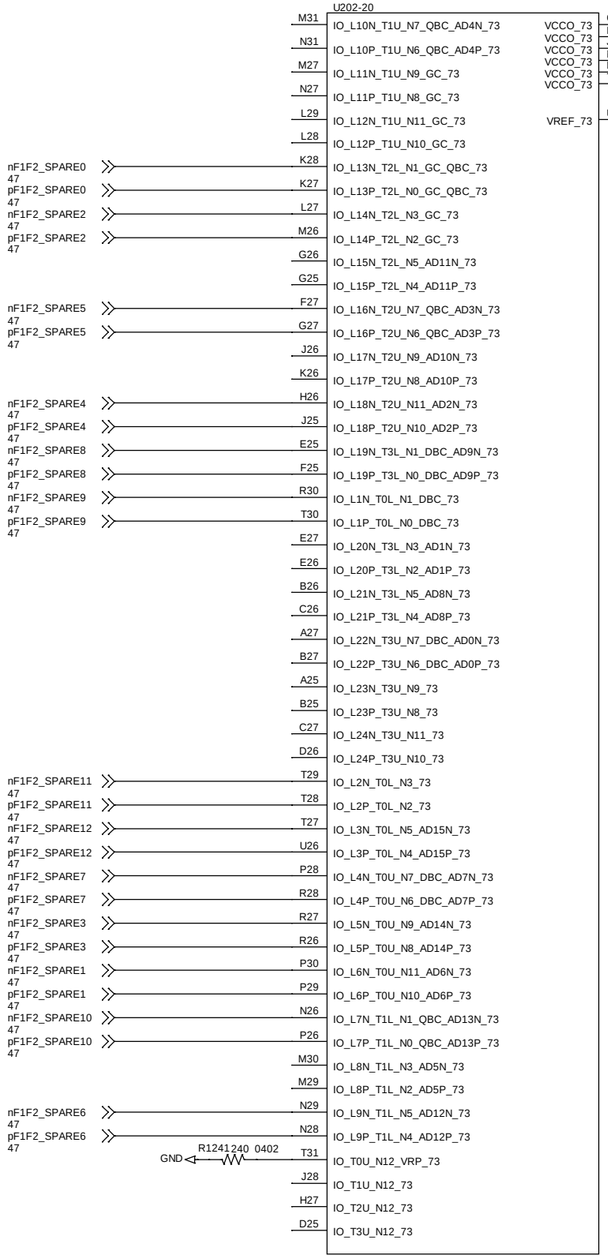
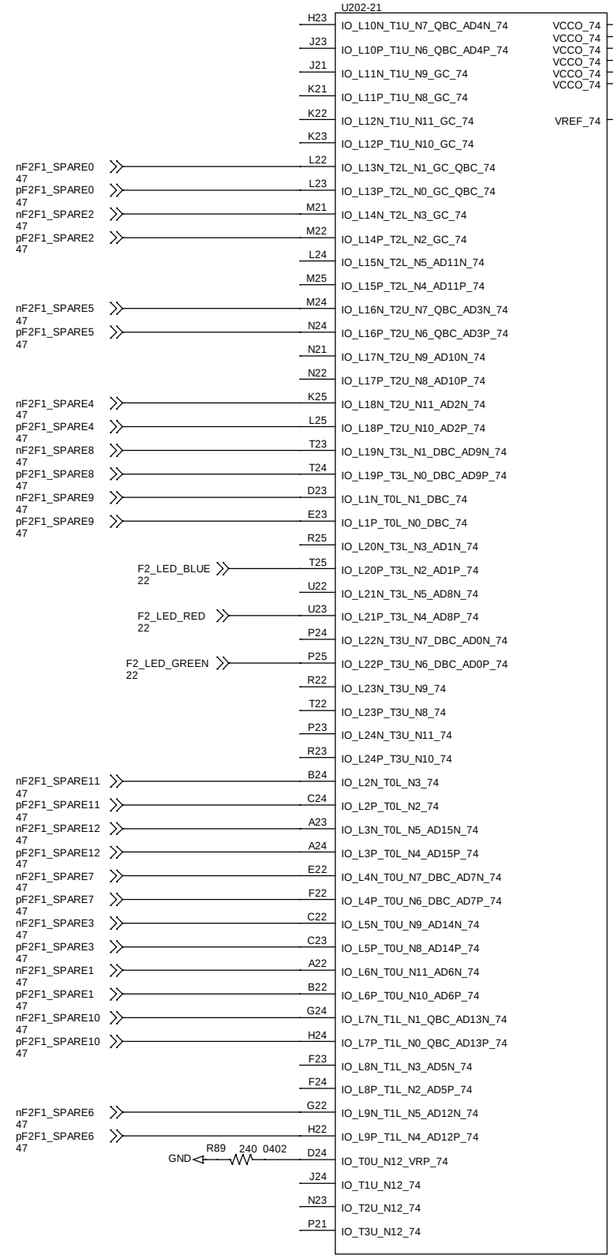
6.09: FPGA#2 I/O SLR3

THESE BANKS ARE NUMBERED DIFFERENTLY IN THE VU13P AND VU9P, BUT THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#3 FOR THE VU13P AND SLR#2 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
I	73	70
J	74	71
K	75	72





THE "F2F1_SPARE" SIGNALS ARE OUTPUTS FROM F2 AND INPUTS TO F1.
THE "F1F2_SPARE" SIGNALS ARE OUTPUTS FROM F1 AND INPUTS TO F2.
THEY ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "_SPARE0" AND "_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE FPGA

APOLLO CM W/ DUAL A2577, MK1		
Title: 6.09: FPGA#2 I/O SLR3		
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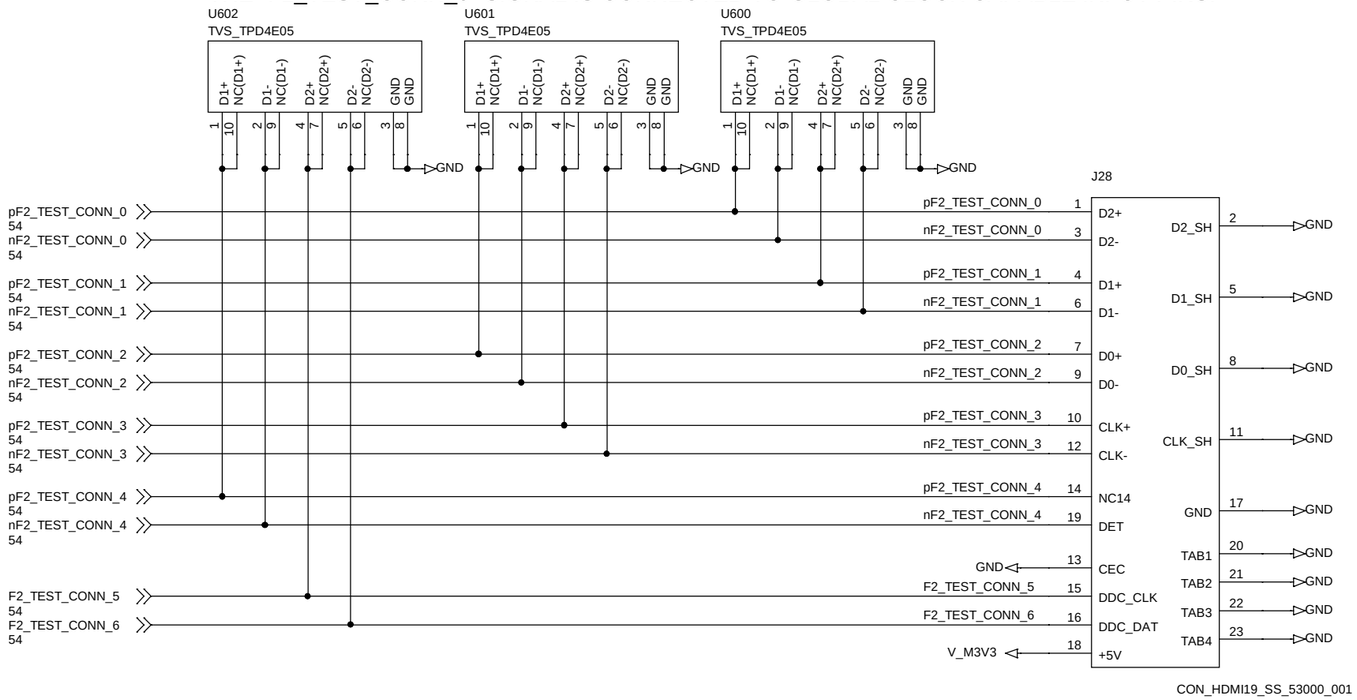
6.10 FPGA#2 TEST CONNECTOR

THIS CONNECTOR IS LOCATED ON THE FRONT PANEL. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

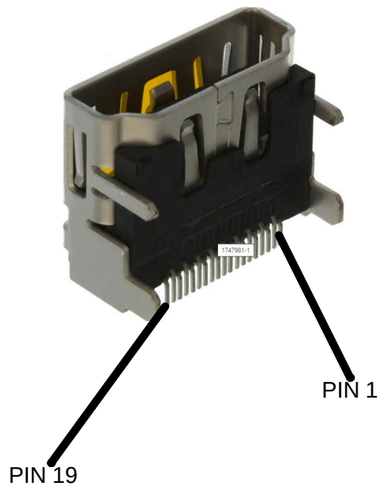
THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

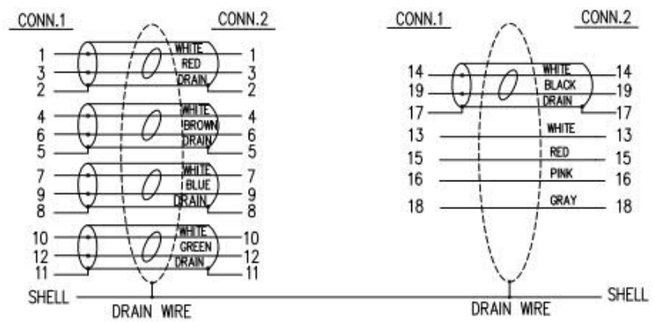
THE "F2_TEST_CONN_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.



CON_HDMI19_SS_53000_001

PIN ASSIGNMENT





APOLLO CM W/ DUAL A2577, MK1		
Title: 6.10 FPGA#2 TEST CONNECTOR		
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7.01: FPGA#1 SM C2C ON QUAD L

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

APOLLO CM W/ DUAL A2577, MK1

Title: 7.01: FPGA#1 SM C2C ON QUAD L

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7.02: FPGA#1 FF#1 X12 ON QUADS AC AD AE

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_AD 18
ac_nF1L_R0_AD 18
ac_pF1L_R1_AD 20
ac_nF1L_R1_AD 20

V_M3V3
R968 3.3K 0603
R969 3.3K 0603
R970 2.2K 0603
R971 2.2K 0603

U551-1 FIREFLY_XMIT_X12
FIREFLY XMIT X12

/F1_FF_RESET 37,60,61,62,63,64,65,66
I2C_SDA_F1_FF1_XMIT 37
I2C_SCL_F1_FF1_XMIT 37
/F1_FF1_XMIT_INT 37
/F1_FF1_XMIT_PRESENT 37
V_3V3
V_F1_FF1_XMIT 30

/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.8/3.3V (>=25G 3.8V <=16G 3.3V), RSVD, GND, G1, G2

C2086 +22 UF 0603 6.3V
C2087 0.1 UF 0402
C2088 +22 UF 0603 6.3V
C2089 0.1 UF 0402
L103 1.0 UH 0806
C2090 +22 UF 0603 6.3V
C2091 0.1 UF 0402
C2092 +22 UF 0603 6.3V
C2093 0.1 UF 0402
L107 1.0 UH 0806

<Implementation>

U551-2 FIREFLY_XMIT_X12
FIREFLY XMIT X12

GND_B19/A19, GND_A19/B17, GND_B16/A16, GND_A16/A17, GND_B13/A13, GND_A13/A14, GND_B10/A10, GND_A10/A11, GND_B7/A7, GND_A7/B5, GND_B4/A4, GND_A4/B2, GND_B1/A1

0P/0N pF1_FF1_XMIT0 / nF1_FF1_XMIT0
1P/1N pF1_FF1_XMIT1 / nF1_FF1_XMIT1
2P/2N pF1_FF1_XMIT2 / nF1_FF1_XMIT2
3P/3N pF1_FF1_XMIT3 / nF1_FF1_XMIT3
4P/4N pF1_FF1_XMIT4 / nF1_FF1_XMIT4
5P/5N pF1_FF1_XMIT5 / nF1_FF1_XMIT5
6P/6N pF1_FF1_XMIT6 / nF1_FF1_XMIT6
7P/7N pF1_FF1_XMIT7 / nF1_FF1_XMIT7
8P/8N pF1_FF1_XMIT8 / nF1_FF1_XMIT8
9P/9N pF1_FF1_XMIT9 / nF1_FF1_XMIT9
10P/10N pF1_FF1_XMIT10 / nF1_FF1_XMIT10
11P/11N pF1_FF1_XMIT11 / nF1_FF1_XMIT11

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U201-24 AC GTY QUAD 121

MGTREFCLK0P_121 / MGTREFCLK0N_121 (BB40 / BB39)
MGTREFCLK1P_121 / MGTREFCLK1N_121 (BA42 / BA41)

pF1_FF1_RECV11 BK34 / nF1_FF1_RECV11 BK35 — MGTYRXP0_121 / MGTYRXN0_121
pF1_FF1_XMIT11 BL37 / nF1_FF1_XMIT11 BL38 — MGTYTXP0_121 / MGTYTXN0_121
pF1_FF1_RECV10 BL32 / nF1_FF1_RECV10 BL33 — MGTYRXP1_121 / MGTYRXN1_121
pF1_FF1_XMIT10 BK39 / nF1_FF1_XMIT10 BK40 — MGTYTXP1_121 / MGTYTXN1_121
pF1_FF1_RECV9 BL46 / nF1_FF1_RECV9 BL47 — MGTYRXP2_121 / MGTYRXN2_121
pF1_FF1_XMIT9 BL41 / nF1_FF1_XMIT9 BL42 — MGTYTXP2_121 / MGTYTXN2_121
pF1_FF1_RECV8 BJ46 / nF1_FF1_RECV8 BJ47 — MGTYRXP3_121 / MGTYRXN3_121
pF1_FF1_XMIT8 BK43 / nF1_FF1_XMIT8 BK44 — MGTYTXP3_121 / MGTYTXN3_121

FPGA_VU13P_A2577

U201-25 AD GTY QUAD 122

MGTREFCLK0P_122 / MGTREFCLK0N_122 (AY40 / AY39)
MGTREFCLK1P_122 / MGTREFCLK1N_122 (AW42 / AW41)

pF1_FF1_RECV7 BH48 / nF1_FF1_RECV7 BH49 — MGTYRXP0_122 / MGTYRXN0_122
pF1_FF1_XMIT7 BG41 / nF1_FF1_XMIT7 BG42 — MGTYTXP0_122 / MGTYTXN0_122
pF1_FF1_RECV6 BG50 / nF1_FF1_RECV6 BG51 — MGTYRXP1_122 / MGTYRXN1_122
pF1_FF1_XMIT6 BJ41 / nF1_FF1_XMIT6 BJ42 — MGTYTXP1_122 / MGTYTXN1_122
pF1_FF1_RECV5 BG46 / nF1_FF1_RECV5 BG47 — MGTYRXP2_122 / MGTYRXN2_122
pF1_FF1_XMIT5 BH43 / nF1_FF1_XMIT5 BH44 — MGTYTXP2_122 / MGTYTXN2_122
pF1_FF1_RECV4 BF48 / nF1_FF1_RECV4 BF49 — MGTYRXP3_122 / MGTYRXN3_122
pF1_FF1_XMIT4 BF43 / nF1_FF1_XMIT4 BF44 — MGTYTXP3_122 / MGTYTXN3_122

FPGA_VU13P_A2577

V_M3V3
R972 3.3K 0603
R973 3.3K 0603
R974 2.2K 0603
R975 2.2K 0603

U559-1 FIREFLY_RECV_X12
FIREFLY RECV X12

/F1_FF_RESET 37,60,61,62,63,64,65,66
I2C_SDA_F1_FF1_RECV 37
I2C_SCL_F1_FF1_RECV 37
/F1_FF1_RECV_INT 37
/F1_FF1_RECV_PRESENT 37
V_3V3

/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.3V, RSVD, GND, G1, G2

C2096 +22 UF 0603 6.3V
C2097 0.1 UF 0402
C2094 +22 UF 0603 6.3V
C2095 0.1 UF 0402
L108 1.0 UH 0806
C2098 +22 UF 0603 6.3V
C2099 0.1 UF 0402
L109 1.0 UH 0806

<Implementation>

U559-2 FIREFLY_RECV_X12
FIREFLY RECV X12

GND_B19/A19, GND_A19/A17, GND_B16/A16, GND_A16/B17, GND_B13/A13, GND_A13/A11, GND_B10/A10, GND_A10/B11, GND_B7/A7, GND_A7/A5, GND_B4/A4, GND_A4/A2, GND_B1/A1

0P/0N pF1_FF1_RECV0 / nF1_FF1_RECV0
1P/1N pF1_FF1_RECV1 / nF1_FF1_RECV1
2P/2N pF1_FF1_RECV2 / nF1_FF1_RECV2
3P/3N pF1_FF1_RECV3 / nF1_FF1_RECV3
4P/4N pF1_FF1_RECV4 / nF1_FF1_RECV4
5P/5N pF1_FF1_RECV5 / nF1_FF1_RECV5
6P/6N pF1_FF1_RECV6 / nF1_FF1_RECV6
7P/7N pF1_FF1_RECV7 / nF1_FF1_RECV7
8P/8N pF1_FF1_RECV8 / nF1_FF1_RECV8
9P/9N pF1_FF1_RECV9 / nF1_FF1_RECV9
10P/10N pF1_FF1_RECV10 / nF1_FF1_RECV10
11P/11N pF1_FF1_RECV11 / nF1_FF1_RECV11

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

U201-26 AE GTY QUAD 123

MGTREFCLK0P_123 / MGTREFCLK0N_123 (AV40 / AV39)
MGTREFCLK1P_123 / MGTREFCLK1N_123 (AU42 / AU41)

pF1_FF1_RECV3 BE50 / nF1_FF1_RECV3 BE51 — MGTYRXP0_123 / MGTYRXN0_123
pF1_FF1_XMIT3 BE45 / nF1_FF1_XMIT3 BE46 — MGTYTXP0_123 / MGTYTXN0_123
pF1_FF1_RECV2 BD48 / nF1_FF1_RECV2 BD49 — MGTYRXP1_123 / MGTYRXN1_123
pF1_FF1_XMIT2 BD43 / nF1_FF1_XMIT2 BD44 — MGTYTXP1_123 / MGTYTXN1_123
pF1_FF1_RECV1 BC50 / nF1_FF1_RECV1 BC51 — MGTYRXP2_123 / MGTYRXN2_123
pF1_FF1_XMIT1 BC45 / nF1_FF1_XMIT1 BC46 — MGTYTXP2_123 / MGTYTXN2_123
pF1_FF1_RECV0 BB48 / nF1_FF1_RECV0 BB49 — MGTYRXP3_123 / MGTYRXN3_123
pF1_FF1_XMIT0 BB43 / nF1_FF1_XMIT0 BB44 — MGTYTXP3_123 / MGTYTXN3_123

FPGA_VU13P_A2577

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

APOLLO CM W/ DUAL A2577, MK1

Title: 7.02: FPGA#1 FF#1 X12 ON QUADS AC AD AE

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7.03: FPGA#1 FF#2 X12 ON QUADS Q R S

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_R 18
ac_nF1L_R0_R 18
ac_pF1L_R1_R 20
ac_nF1L_R1_R 20

V_M3V3 — R976 3.3K 0603 — R977 3.3K 0603 — R978 2.2K 0603 — R979 2.2K 0603

U552-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

/F1_FF_RESET 37,60,61,62,63,64,65,66
I2C_SDA_F1_FF2_XMIT 37
I2C_SCL_F1_FF2_XMIT 37
/F1_FF2_XMIT_INT 37
/F1_FF2_XMIT_PRESENT 37

6 /RESET — G1 G2 — GND
7 SDA
8 SCL
GND — 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V

V_3V3 — C2346 22 UF 0603 6.3V — C2347 0.1 UF 0402 — L110 1.0 UH 0806 — C2348 22 UF 0603 6.3V — C2349 0.1 UF 0402

V_F1_FF2_XMIT 30 — C2350 22 UF 0603 6.3V — C2351 0.1 UF 0402 — L111 1.0 UH 0806 — C2352 22 UF 0603 6.3V — C2353 0.1 UF 0402

10 3.8/3.3V (>=25G 3.8V, <=16G 3.3V)
9 RSVD
GND — 2 GND

<Implementation>

U552-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

B19 A19	GND_B19 GND_A19	0P 0N	B18 pF1_FF2_XMIT0 / B17 nF1_FF2_XMIT0
		1P 1N	A18 pF1_FF2_XMIT1 / A17 nF1_FF2_XMIT1
B16 A16	GND_B16 GND_A16	2P 2N	B15 pF1_FF2_XMIT2 / B14 nF1_FF2_XMIT2
		3P 3N	A15 pF1_FF2_XMIT3 / A14 nF1_FF2_XMIT3
B13 A13	GND_B13 GND_A13	4P 4N	B12 pF1_FF2_XMIT4 / B11 nF1_FF2_XMIT4
		5P 5N	A12 pF1_FF2_XMIT5 / A11 nF1_FF2_XMIT5
B10 A10	GND_B10 GND_A10	6P 6N	B9 pF1_FF2_XMIT6 / B8 nF1_FF2_XMIT6
		7P 7N	A9 pF1_FF2_XMIT7 / A8 nF1_FF2_XMIT7
B7 A7	GND_B7 GND_A7	8P 8N	B6 pF1_FF2_XMIT8 / B5 nF1_FF2_XMIT8
		9P 9N	A6 pF1_FF2_XMIT9 / A5 nF1_FF2_XMIT9
B4 A4	GND_B4 GND_A4	10P 10N	B3 pF1_FF2_XMIT10 / B2 nF1_FF2_XMIT10
		11P 11N	A3 pF1_FF2_XMIT11 / A2 nF1_FF2_XMIT11
B1 A1	GND_B1 GND_A1		

GND — GND — GND — GND — GND — GND — GND

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U201-28 Q — GTY QUAD 125

	AP39 / AP40	MGTREFCLK0P_125 / MGTREFCLK0N_125
	AN41 / AN42	MGTREFCLK1P_125 / MGTREFCLK1N_125
pF1_FF2_RECV11 / nF1_FF2_RECV11	AU50 / AU51	MGTYRXP0_125 / MGTYRXN0_125
pF1_FF2_XMIT11 / nF1_FF2_XMIT11	AU45 / AU46	MGTYTXP0_125 / MGTYTXN0_125
pF1_FF2_RECV10 / nF1_FF2_RECV10	AT48 / AT49	MGTYRXP1_125 / MGTYRXN1_125
pF1_FF2_XMIT10 / nF1_FF2_XMIT10	AT43 / AT44	MGTYTXP1_125 / MGTYTXN1_125
pF1_FF2_RECV9 / nF1_FF2_RECV9	AR50 / AR51	MGTYRXP2_125 / MGTYRXN2_125
pF1_FF2_XMIT9 / nF1_FF2_XMIT9	AR45 / AR46	MGTYTXP2_125 / MGTYTXN2_125
pF1_FF2_RECV8 / nF1_FF2_RECV8	AP48 / AP49	MGTYRXP3_125 / MGTYRXN3_125
pF1_FF2_XMIT8 / nF1_FF2_XMIT8	AP43 / AP44	MGTYTXP3_125 / MGTYTXN3_125

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U201-29 R — GTY QUAD 126

	AM39 / AM40	MGTREFCLK0P_126 / MGTREFCLK0N_126
	AL41 / AL42	MGTREFCLK1P_126 / MGTREFCLK1N_126
pF1_FF2_RECV7 / nF1_FF2_RECV7	AN50 / AN51	MGTYRXP0_126 / MGTYRXN0_126
pF1_FF2_XMIT7 / nF1_FF2_XMIT7	AN45 / AN46	MGTYTXP0_126 / MGTYTXN0_126
pF1_FF2_RECV6 / nF1_FF2_RECV6	AM48 / AM49	MGTYRXP1_126 / MGTYRXN1_126
pF1_FF2_XMIT6 / nF1_FF2_XMIT6	AM43 / AM44	MGTYTXP1_126 / MGTYTXN1_126
pF1_FF2_RECV5 / nF1_FF2_RECV5	AL50 / AL51	MGTYRXP2_126 / MGTYRXN2_126
pF1_FF2_XMIT5 / nF1_FF2_XMIT5	AL45 / AL46	MGTYTXP2_126 / MGTYTXN2_126
pF1_FF2_RECV4 / nF1_FF2_RECV4	AK48 / AK49	MGTYRXP3_126 / MGTYRXN3_126
pF1_FF2_XMIT4 / nF1_FF2_XMIT4	AK43 / AK44	MGTYTXP3_126 / MGTYTXN3_126

FPGA_VU13P_A2577

V_M3V3 — R980 3.3K 0603 — R981 3.3K 0603 — R982 2.2K 0603 — R983 2.2K 0603

U560-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

/F1_FF_RESET 37,60,61,62,63,64,65,66
I2C_SDA_F1_FF2_RECV 37
I2C_SCL_F1_FF2_RECV 37
/F1_FF2_RECV_INT 37
/F1_FF2_RECV_PRESENT 37

6 /RESET — G1 G2 — GND
7 SDA
8 SCL
GND — 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V

V_3V3 — C2356 22 UF 0603 6.3V — C2357 0.1 UF 0402 — L112 1.0 UH 0806 — C2354 22 UF 0603 6.3V — C2355 0.1 UF 0402

L113 1.0 UH 0806 — C2358 22 UF 0603 6.3V — C2359 0.1 UF 0402

10 3.3V
9 RSVD
GND — 2 GND

<Implementation>

U560-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

B19 A19	GND_B19 GND_A19	0P 0N	A18 pF1_FF2_RECV0 / A17 nF1_FF2_RECV0
		1P 1N	B18 pF1_FF2_RECV1 / B17 nF1_FF2_RECV1
B16 A16	GND_B16 GND_A16	2P 2N	A15 pF1_FF2_RECV2 / A14 nF1_FF2_RECV2
		3P 3N	B15 pF1_FF2_RECV3 / B14 nF1_FF2_RECV3
B13 A13	GND_B13 GND_A13	4P 4N	A12 pF1_FF2_RECV4 / A11 nF1_FF2_RECV4
		5P 5N	B12 pF1_FF2_RECV5 / B11 nF1_FF2_RECV5
B10 A10	GND_B10 GND_A10	6P 6N	A9 pF1_FF2_RECV6 / A8 nF1_FF2_RECV6
		7P 7N	B9 pF1_FF2_RECV7 / B8 nF1_FF2_RECV7
B7 A7	GND_B7 GND_A7	8P 8N	A6 pF1_FF2_RECV8 / A5 nF1_FF2_RECV8
		9P 9N	B6 pF1_FF2_RECV9 / B5 nF1_FF2_RECV9
B4 A4	GND_B4 GND_A4	10P 10N	A3 pF1_FF2_RECV10 / A2 nF1_FF2_RECV10
		11P 11N	B3 pF1_FF2_RECV11 / B2 nF1_FF2_RECV11
B1 A1	GND_B1 GND_A1		

GND — GND — GND — GND — GND — GND — GND

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U201-30 S — GTY QUAD 127

	AJ41 / AJ42	MGTREFCLK0P_127 / MGTREFCLK0N_127
	AG41 / AG42	MGTREFCLK1P_127 / MGTREFCLK1N_127
pF1_FF2_RECV3 / nF1_FF2_RECV3	AJ50 / AJ51	MGTYRXP0_127 / MGTYRXN0_127
pF1_FF2_XMIT3 / nF1_FF2_XMIT3	AJ45 / AJ46	MGTYTXP0_127 / MGTYTXN0_127
pF1_FF2_RECV2 / nF1_FF2_RECV2	AH48 / AH49	MGTYRXP1_127 / MGTYRXN1_127
pF1_FF2_XMIT2 / nF1_FF2_XMIT2	AH43 / AH44	MGTYTXP1_127 / MGTYTXN1_127
pF1_FF2_RECV1 / nF1_FF2_RECV1	AG50 / AG51	MGTYRXP2_127 / MGTYRXN2_127
pF1_FF2_XMIT1 / nF1_FF2_XMIT1	AG45 / AG46	MGTYTXP2_127 / MGTYTXN2_127
pF1_FF2_RECV0 / nF1_FF2_RECV0	AF48 / AF49	MGTYRXP3_127 / MGTYRXN3_127
pF1_FF2_XMIT0 / nF1_FF2_XMIT0	AF43 / AF44	MGTYTXP3_127 / MGTYTXN3_127

FPGA_VU13P_A2577

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1	
Title	7.03: FPGA#1 FF#2 X12 ON QUADS Q R S
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7.04: FPGA#1 FF#3 X12 ON QUADS X Y Z

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_Y 18
ac_nF1L_R0_Y 18
ac_pF1L_R1_Y 20
ac_nF1L_R1_Y 20

V_M3V3
R984 3.3K 0603
R985 3.3K 0603
R986 2.2K 0603
R987 2.2K 0603

U553-1 FIREFLY_XMIT_X12
FIREFLY XMIT X12

/F1_FF_RESET 37,60,61,62,63,64,65,66
I2C_SDA_F1_FF3_XMIT 37
I2C_SCL_F1_FF3_XMIT 37
/F1_FF3_XMIT_INT 37
/F1_FF3_XMIT_PRESENT 37
V_3V3
V_F1_FF3_XMIT 30

/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.8/3.3V (>=25G 3.8V <=16G 3.3V), RSVD, GND
G1, G2

C2360 22 UF 0603 6.3V
C2361 0.1 UF 0402
C2362 22 UF 0603 6.3V
C2363 0.1 UF 0402
C2364 0.1 UF 0402
C2365 22 UF 0603 6.3V
C2366 0.1 UF 0402
C2367 22 UF 0603 6.3V
L114 1.0 UH 0806
L115 1.0 UH 0806

<Implementation>

U553-2 FIREFLY_XMIT_X12
FIREFLY XMIT X12

GND_B19/A19, GND_B16/A16, GND_B13/A13, GND_B10/A10, GND_B7/A7, GND_B4/A4, GND_B1/A1

0P/0N pF1_FF3_XMIT0
1P/1N pF1_FF3_XMIT1
2P/2N pF1_FF3_XMIT2
3P/3N pF1_FF3_XMIT3
4P/4N pF1_FF3_XMIT4
5P/5N pF1_FF3_XMIT5
6P/6N pF1_FF3_XMIT6
7P/7N pF1_FF3_XMIT7
8P/8N pF1_FF3_XMIT8
9P/9N pF1_FF3_XMIT9
10P/10N pF1_FF3_XMIT10
11P/11N pF1_FF3_XMIT11

GND_A107, GND_A108, GND_A109, GND_A110, GND_A111, GND_A112

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U201-35 GTY QUAD 132

MGTREFCLK0P_132 R41
MGTREFCLK0N_132 R42
MGTREFCLK1P_132 P39
MGTREFCLK1N_132 P40

pF1_FF3_RECV11 J50 / nF1_FF3_RECV11 J51 — MGTYRXP0_132 / MGTYRXN0_132
pF1_FF3_XMIT11 J45 / nF1_FF3_XMIT11 J46 — MGTYTXP0_132 / MGTYTXN0_132
pF1_FF3_RECV10 H48 / nF1_FF3_RECV10 H49 — MGTYRXP1_132 / MGTYRXN1_132
pF1_FF3_XMIT10 H43 / nF1_FF3_XMIT10 H44 — MGTYTXP1_132 / MGTYTXN1_132
pF1_FF3_RECV9 G50 / nF1_FF3_RECV9 G51 — MGTYRXP2_132 / MGTYRXN2_132
pF1_FF3_XMIT9 G45 / nF1_FF3_XMIT9 G46 — MGTYTXP2_132 / MGTYTXN2_132
pF1_FF3_RECV8 F48 / nF1_FF3_RECV8 F49 — MGTYRXP3_132 / MGTYRXN3_132
pF1_FF3_XMIT8 F43 / nF1_FF3_XMIT8 F44 — MGTYTXP3_132 / MGTYTXN3_132

FPGA_VU13P_A2577

U201-36 GTY QUAD 133

MGTREFCLK0P_133 N41
MGTREFCLK0N_133 N42
MGTREFCLK1P_133 M39
MGTREFCLK1N_133 M40

pF1_FF3_RECV7 E50 / nF1_FF3_RECV7 E51 — MGTYRXP0_133 / MGTYRXN0_133
pF1_FF3_XMIT7 D43 / nF1_FF3_XMIT7 D44 — MGTYTXP0_133 / MGTYTXN0_133
pF1_FF3_RECV6 D48 / nF1_FF3_RECV6 D49 — MGTYRXP1_133 / MGTYRXN1_133
pF1_FF3_XMIT6 B43 / nF1_FF3_XMIT6 B44 — MGTYTXP1_133 / MGTYTXN1_133
pF1_FF3_RECV5 E46 / nF1_FF3_RECV5 E47 — MGTYRXP2_133 / MGTYRXN2_133
pF1_FF3_XMIT5 C41 / nF1_FF3_XMIT5 C42 — MGTYTXP2_133 / MGTYTXN2_133
pF1_FF3_RECV4 C46 / nF1_FF3_RECV4 C47 — MGTYRXP3_133 / MGTYRXN3_133
pF1_FF3_XMIT4 E41 / nF1_FF3_XMIT4 E42 — MGTYTXP3_133 / MGTYTXN3_133

FPGA_VU13P_A2577

U201-37 GTY QUAD 134

MGTREFCLK0P_134 L41
MGTREFCLK0N_134 L42
MGTREFCLK1P_134 K39
MGTREFCLK1N_134 K40

pF1_FF3_RECV3 A46 / nF1_FF3_RECV3 A47 — MGTYRXP0_134 / MGTYRXN0_134
pF1_FF3_XMIT3 A41 / nF1_FF3_XMIT3 A42 — MGTYTXP0_134 / MGTYTXN0_134
pF1_FF3_RECV2 A32 / nF1_FF3_RECV2 A33 — MGTYRXP1_134 / MGTYRXN1_134
pF1_FF3_XMIT2 B39 / nF1_FF3_XMIT2 B40 — MGTYTXP1_134 / MGTYTXN1_134
pF1_FF3_RECV1 B34 / nF1_FF3_RECV1 B35 — MGTYRXP2_134 / MGTYRXN2_134
pF1_FF3_XMIT1 A37 / nF1_FF3_XMIT1 A38 — MGTYTXP2_134 / MGTYTXN2_134
pF1_FF3_RECV0 C32 / nF1_FF3_RECV0 C33 — MGTYRXP3_134 / MGTYRXN3_134
pF1_FF3_XMIT0 C37 / nF1_FF3_XMIT0 C38 — MGTYTXP3_134 / MGTYTXN3_134

FPGA_VU13P_A2577

V_M3V3
R988 3.3K 0603
R989 3.3K 0603
R990 2.2K 0603
R991 2.2K 0603

U561-1 FIREFLY_RECV_X12
FIREFLY RECV X12

/F1_FF_RESET 37,60,61,62,63,64,65,66
I2C_SDA_F1_FF3_RECV 37
I2C_SCL_F1_FF3_RECV 37
/F1_FF3_RECV_INT 37
/F1_FF3_RECV_PRESENT 37
V_3V3

/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.3V, RSVD, GND
G1, G2

C2368 22 UF 0603 6.3V
C2369 0.1 UF 0402
C2370 22 UF 0603 6.3V
C2371 0.1 UF 0402
C2372 22 UF 0603 6.3V
C2373 0.1 UF 0402
L116 1.0 UH 0806
L117 1.0 UH 0806

<Implementation>

U561-2 FIREFLY_RECV_X12
FIREFLY RECV X12

GND_B19/A19, GND_B16/A16, GND_B13/A13, GND_B10/A10, GND_B7/A7, GND_B4/A4, GND_B1/A1

0P/0N pF1_FF3_RECV0
1P/1N pF1_FF3_RECV1
2P/2N pF1_FF3_RECV2
3P/3N pF1_FF3_RECV3
4P/4N pF1_FF3_RECV4
5P/5N pF1_FF3_RECV5
6P/6N pF1_FF3_RECV6
7P/7N pF1_FF3_RECV7
8P/8N pF1_FF3_RECV8
9P/9N pF1_FF3_RECV9
10P/10N pF1_FF3_RECV10
11P/11N pF1_FF3_RECV11

GND_A113, GND_A114, GND_A115, GND_A116, GND_A117, GND_A118

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1

Title: 7.04: FPGA#1 FF#3 X12 ON QUADS X Y Z

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7.05: FPGA#1 FF#4 X4 ON QUAD AF

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_AF 18
ac_nF1L_R0_AF 18
ac_pF1L_R1_AF 19
ac_nF1L_R1_AF 19

U201-27
AF GTY QUAD 124

	AT39	
	AT40	MGTREFCLK0P_124 MGTREFCLK0N_124
	AR41	
	AR42	MGTREFCLK1P_124 MGTREFCLK1N_124
pF1_FF4_RECV0	BA50	MGTYRXP0_124
nF1_FF4_RECV0	BA51	MGTYRXN0_124
pF1_FF4_XMIT0	BA45	MGTYTXP0_124
nF1_FF4_XMIT0	BA46	MGTYTXN0_124
pF1_FF4_RECV1	AY48	MGTYRXP1_124
nF1_FF4_RECV1	AY49	MGTYRXN1_124
pF1_FF4_XMIT1	AY43	MGTYTXP1_124
nF1_FF4_XMIT1	AY44	MGTYTXN1_124
pF1_FF4_RECV2	AW50	MGTYRXP2_124
nF1_FF4_RECV2	AW51	MGTYRXN2_124
pF1_FF4_XMIT2	AW45	MGTYTXP2_124
nF1_FF4_XMIT2	AW46	MGTYTXN2_124
pF1_FF4_RECV3	AV48	MGTYRXP3_124
nF1_FF4_RECV3	AV49	MGTYRXN3_124
pF1_FF4_XMIT3	AV43	MGTYTXP3_124
nF1_FF4_XMIT3	AV44	MGTYTXN3_124

FPGA_VU13P_A2577

V_M3V3
R992 3.3K 0603
R993 3.3K 0603
R994 2.2K 0603
R995 2.2K 0603

U501-1
FIREFLY_XCVR_X4
FIREFLY XCVR X4

/F1_FF_RESET 37,60,61,62,64,65,66	6	/RESET	G1 G2 GND
I2C_SDA_F1_FF4_XCVR 37	7	SDA	
I2C_SCL_F1_FF4_XCVR 37	8	SCL	
GND	4	/SELECT	
/F1_FF4_XCVR_INT 37	5	/INT	
/F1_FF4_XCVR_PRESENT 37	3	/PRESENT	
V_3V3	1	3.3V	
	10	3.3V	
V_1V8	9	1.8V	
GND	2	GND	

V_3V3: C2374 22 UF 0603 6.3V; C1715 0.1 UF 0402; L118 1.0 UH 0806; C2375 22 UF 0603 6.3V; C1717 0.1 UF 0402; L119 1.0 UH 0806; C2376 22 UF 0603 6.3V; C1719 0.1 UF 0402
V_1V8: C2377 22 UF 0603 6.3V; C1721 0.1 UF 0402; L120 1.0 UH 0806; C2378 22 UF 0603 6.3V; C1723 0.1 UF 0402

U501-2
FIREFLY_XCVR_X4
FIREFLY XCVR X4

B19 A19	GND_B19 GND_A19	RX1P RX1N	B17 B18 pF1_FF4_RECV0 nF1_FF4_RECV0
B16 A16	GND_B16 GND_A16	RX2P RX2N	A17 A18 pF1_FF4_RECV1 nF1_FF4_RECV1
B13 A13	GND_B13 GND_A13	RX3P RX3N	B14 B15 pF1_FF4_RECV2 nF1_FF4_RECV2
B7 A7	GND_B7 GND_A7	RX4P RX4N	A14 A15 pF1_FF4_RECV3 nF1_FF4_RECV3
B4 A4	GND_B4 GND_A4	TX4P TX4N	B6 B5 pF1_FF4_XMIT3 nF1_FF4_XMIT3
B1 A1	GND_B1 GND_A1	TX3P TX3N	A6 A5 pF1_FF4_XMIT2 nF1_FF4_XMIT2
GND		TX2P TX2N	B3 B2 pF1_FF4_XMIT1 nF1_FF4_XMIT1
		TX1P TX1N	A3 A2 pF1_FF4_XMIT0 nF1_FF4_XMIT0

GND: J119 1G1 2G1 A119; J122 1G1 2G1 A122; J120 1G1 2G1 A120; J121 1G1 2G1 A121

R996 49p9 0402	B12	RESVD_B12	
R997 49p9 0402	B11	RESVD_B11	
R998 49p9 0402	B10	RESVD_B10	
R999 49p9 0402	B9	RESVD_B9	
R1000 49p9 0402	B8	RESVD_B8	
R1001 49p9 0402	A12	RESVD_A12	
R1002 49p9 0402	A11	RESVD_A11	
R1003 49p9 0402	A10	RESVD_A10	
R1004 49p9 0402	A9	RESVD_A9	
R1005 49p9 0402	A8	RESVD_A8	

GND

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1

Title: 7.05: FPGA#1 FF#4 X4 ON QUAD AF

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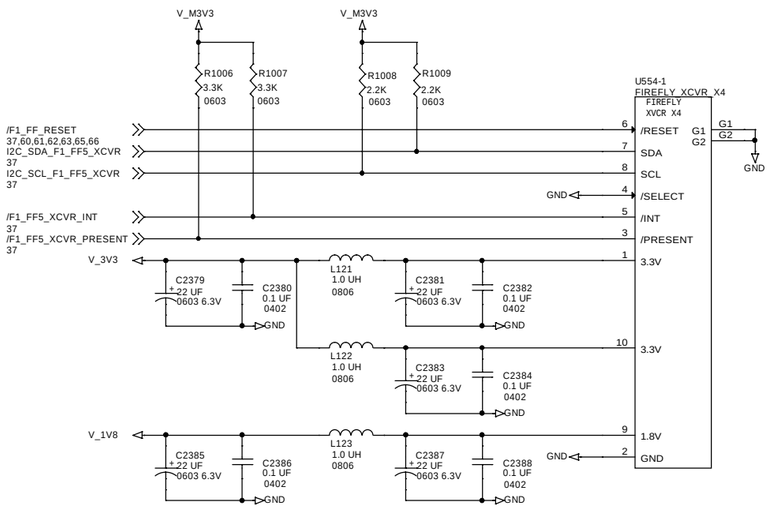
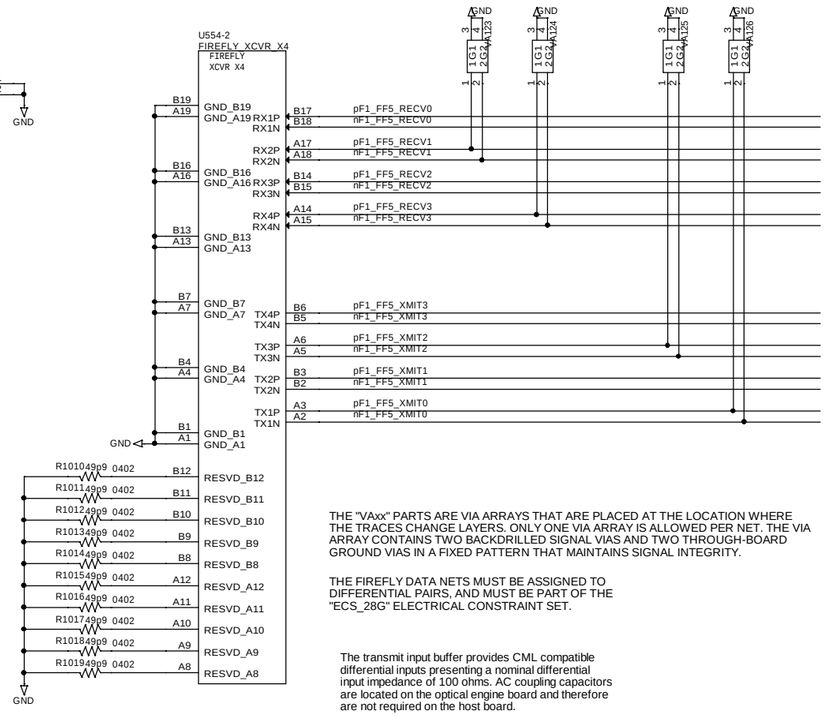
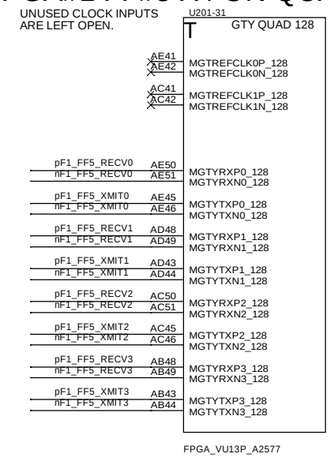
7.06: FPGA#1 FF#5 X4 ON QUAD T







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1		
Title: 7.06: FPGA#1 FF#5 X4 ON QUAD T		
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7.07: FPGA#1 FF#6 X4 ON QUAD U

ac_pF1L_R0_U 18
ac_nF1L_R0_U 18
ac_pF1L_R1_U 19
ac_nF1L_R1_U 19

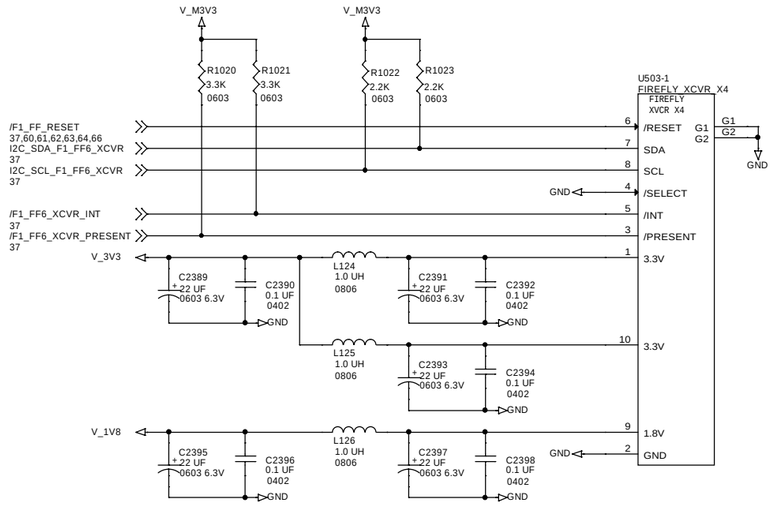
F1 QUAD U (T,U,V)

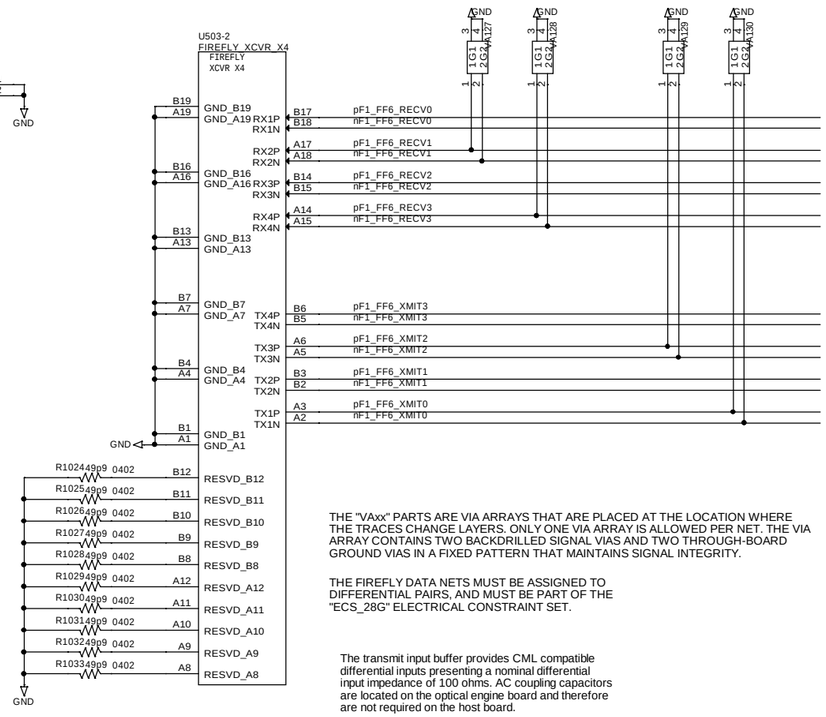
UNUSED CLOCK INPUTS ARE LEFT OPEN.

U201-32
U
GTY QUAD 129

	AA41	
	AA42	MGTREFCLK0P_129
		MGTREFCLK0N_129
	Y39	
	Y40	MGTREFCLK1P_129
		MGTREFCLK1N_129
pF1_FF6_RECV0	AA50	MGTYRXP0_129
nF1_FF6_RECV0	AA51	MGTYRXN0_129
pF1_FF6_XMIT0	AA45	MGTYTXP0_129
nF1_FF6_XMIT0	AA46	MGTYTXN0_129
pF1_FF6_RECV1	Y48	MGTYRXP1_129
nF1_FF6_RECV1	Y49	MGTYRXN1_129
pF1_FF6_XMIT1	Y43	MGTYTXP1_129
nF1_FF6_XMIT1	Y44	MGTYTXN1_129
pF1_FF6_RECV2	W50	MGTYRXP2_129
nF1_FF6_RECV2	W51	MGTYRXN2_129
pF1_FF6_XMIT2	W45	MGTYTXP2_129
nF1_FF6_XMIT2	W46	MGTYTXN2_129
pF1_FF6_RECV3	V48	MGTYRXP3_129
nF1_FF6_RECV3	V49	MGTYRXN3_129
pF1_FF6_XMIT3	V43	MGTYTXP3_129
nF1_FF6_XMIT3	V44	MGTYTXN3_129

FPGA_VU13P_A2577





ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1	
Title: 7.07: FPGA#1 FF#6 X4 ON QUAD U	
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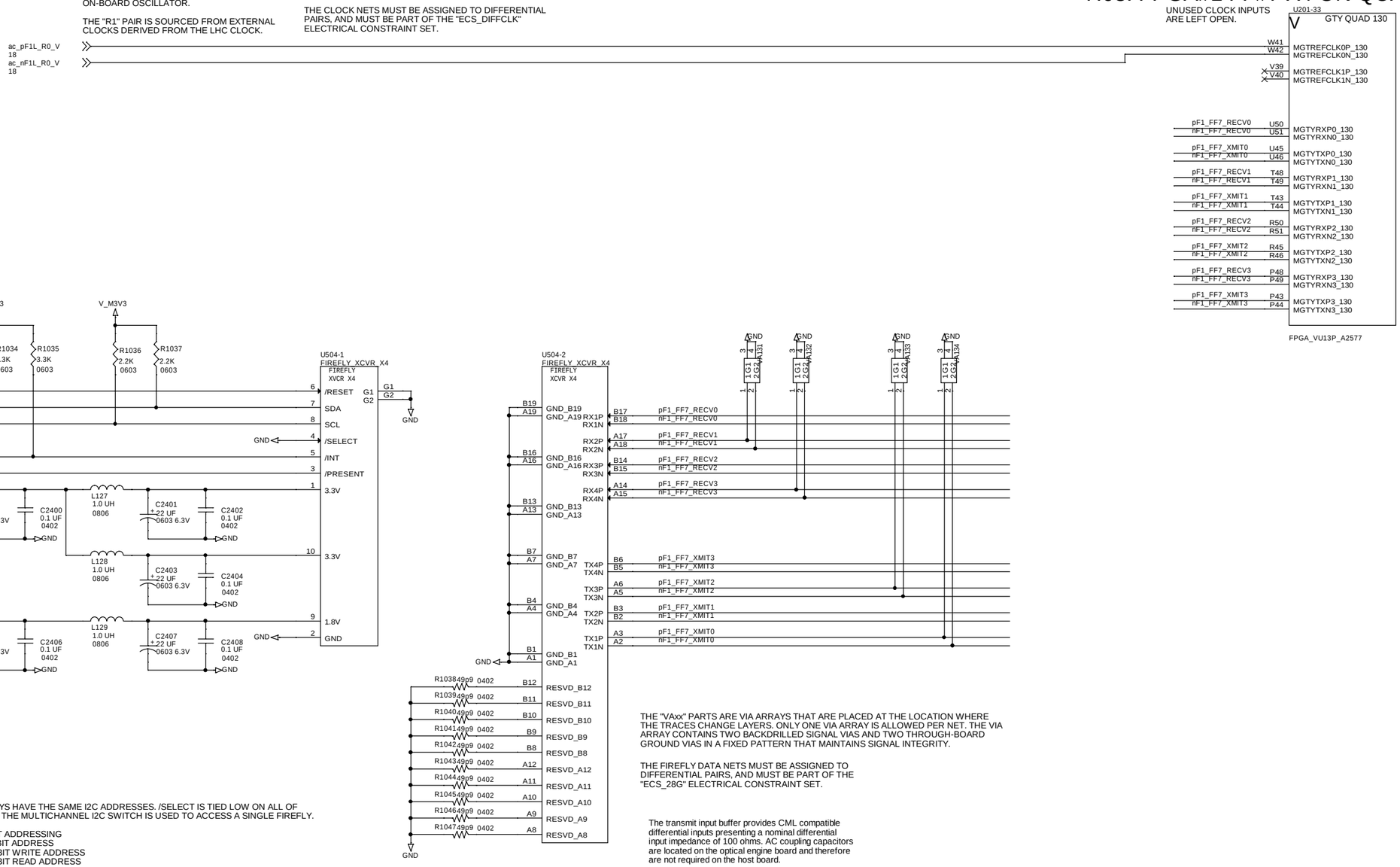
7.08: FPGA#1 FF#7 X4 ON QUAD V

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1

Title: 7.08: FPGA#1 FF#7 X4 ON QUAD V

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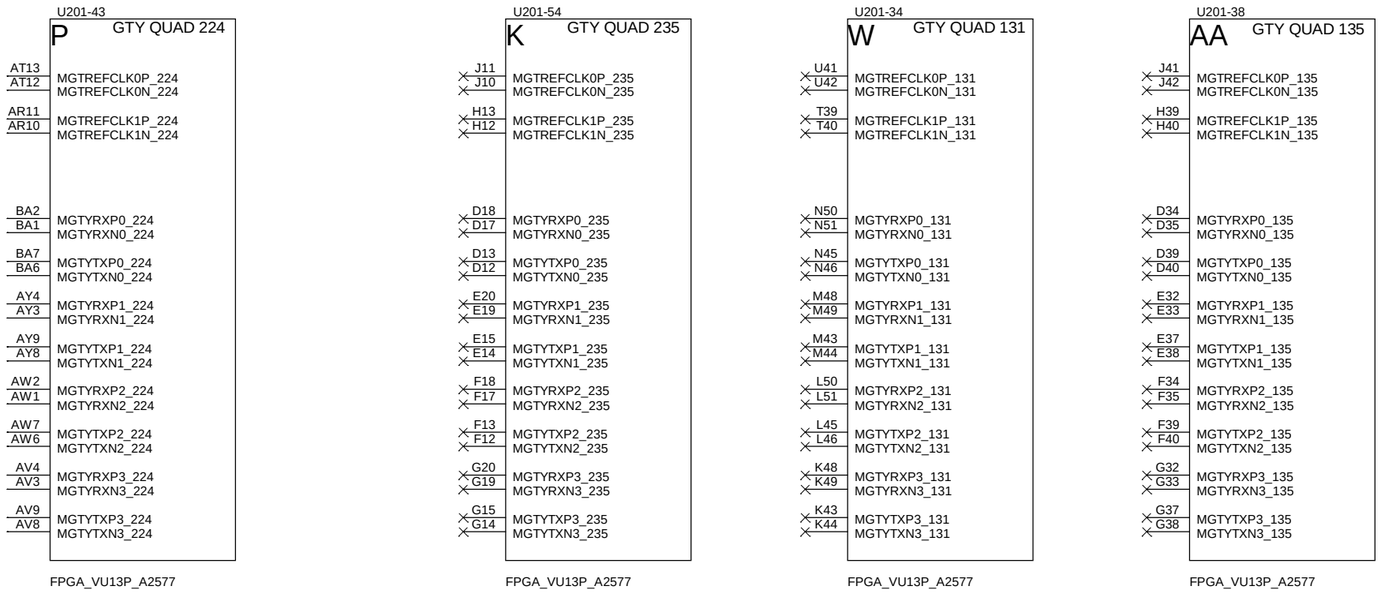
7.09: FPGA#1 UNUSED QUADS K, P, W, AA



APOLLO CM W/ DUAL A2577, MK1		
Title: 7.09: FPGA#1 UNUSED QUADS K, P, W, AA		
Size	Document Number: 6089-119	Rev: A
Date: Thursday, March 18, 2021	Sheet 67 of 82	

8.01: FPGA#2 SM C2C ON QUAD L

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

APOLLO CM W/ DUAL A2577, MK1		
Title: 8.01: FPGA#2 SM C2C ON QUAD L		
Size	Document Number: 6089-119	Rev: A
Date: Thursday, March 18, 2021	Sheet 68 of 82	

8.02: FPGA#2 FF#1 X12 ON QUADS AC AD AE

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF2L_R0_AD 18
ac_nF2L_R0_AD 18
ac_pF2L_R1_AD 20
ac_nF2L_R1_AD 20

V_M3V3

R1048 3.3K 0603
R1049 3.3K 0603
R1050 2.2K 0603
R1051 2.2K 0603

U555-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

/F2_FF_RESET 38,69,70,71,72,73,74,75
I2C_SDA_F2_FF1_XMIT 38
I2C_SCL_F2_FF1_XMIT 38
/F2_FF1_XMIT_INT 38
/F2_FF1_XMIT_PRESENT 38

6 /RESET G1 G2 → GND
7 SDA
8 SCL
GND → 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.8/3.3V >=25G 3.8V <=16G 3.3V
9 RSVD
GND → 2 GND

V_3V3

C2409 +22 UF 0603 6.3V
C2410 0.1 UF 0402
L130 1.0 UH 0806
C2411 +22 UF 0603 6.3V
C2412 0.1 UF 0402

V_F2_FF1_XMIT 30

C2413 +22 UF 0603 6.3V
C2414 0.1 UF 0402
L131 1.0 UH 0806
C2415 +22 UF 0603 6.3V
C2416 0.1 UF 0402

<Implementation>

U555-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

B19 A19	GND_B19 GND_A19	0P 0N	B18 A17	pF2_FF1_XMIT0 nF2_FF1_XMIT0
		1P 1N	A18 A17	pF2_FF1_XMIT1 nF2_FF1_XMIT1
B16 A16	GND_B16 GND_A16	2P 2N	B15 B14	pF2_FF1_XMIT2 nF2_FF1_XMIT2
		3P 3N	A15 A14	pF2_FF1_XMIT3 nF2_FF1_XMIT3
B13 A13	GND_B13 GND_A13	4P 4N	B12 B11	pF2_FF1_XMIT4 nF2_FF1_XMIT4
		5P 5N	A12 A11	pF2_FF1_XMIT5 nF2_FF1_XMIT5
B10 A10	GND_B10 GND_A10	6P 6N	B9 B8	pF2_FF1_XMIT6 nF2_FF1_XMIT6
		7P 7N	A9 A8	pF2_FF1_XMIT7 nF2_FF1_XMIT7
B7 A7	GND_B7 GND_A7	8P 8N	B6 B5	pF2_FF1_XMIT8 nF2_FF1_XMIT8
		9P 9N	A6 A5	pF2_FF1_XMIT9 nF2_FF1_XMIT9
B4 A4	GND_B4 GND_A4	10P 10N	B3 B2	pF2_FF1_XMIT10 nF2_FF1_XMIT10
		11P 11N	A3 A2	pF2_FF1_XMIT11 nF2_FF1_XMIT11
B1 A1	GND_B1 GND_A1			

GND → A135 A136 A137 A138 A139 A140

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U202-24 AC GTY QUAD 121

BB39 BB40		MGTREFCLK0P_121 MGTREFCLK0N_121
BA41 BA42		MGTREFCLK1P_121 MGTREFCLK1N_121
pF2_FF1_RECV11 nF2_FF1_RECV11	BK34 BK35	MGTYRXP0_121 MGTYRXN0_121
pF2_FF1_XMIT11 nF2_FF1_XMIT11	BL37 BL38	MGTYTXP0_121 MGTYTXN0_121
pF2_FF1_RECV10 nF2_FF1_RECV10	BL32 BL33	MGTYRXP1_121 MGTYRXN1_121
pF2_FF1_XMIT10 nF2_FF1_XMIT10	BK39 BK40	MGTYTXP1_121 MGTYTXN1_121
pF2_FF1_RECV9 nF2_FF1_RECV9	BL46 BL47	MGTYRXP2_121 MGTYRXN2_121
pF2_FF1_XMIT9 nF2_FF1_XMIT9	BL41 BL42	MGTYTXP2_121 MGTYTXN2_121
pF2_FF1_RECV8 nF2_FF1_RECV8	BJ46 BJ47	MGTYRXP3_121 MGTYRXN3_121
pF2_FF1_XMIT8 nF2_FF1_XMIT8	BK43 BK44	MGTYTXP3_121 MGTYTXN3_121

FPGA_VU13P_A2577

U202-25 AD GTY QUAD 122

AY39 AY40		MGTREFCLK0P_122 MGTREFCLK0N_122
AW41 AW42		MGTREFCLK1P_122 MGTREFCLK1N_122
pF2_FF1_RECV7 nF2_FF1_RECV7	BH48 BH49	MGTYRXP0_122 MGTYRXN0_122
pF2_FF1_XMIT7 nF2_FF1_XMIT7	BG41 BG42	MGTYTXP0_122 MGTYTXN0_122
pF2_FF1_RECV6 nF2_FF1_RECV6	BG50 BG51	MGTYRXP1_122 MGTYRXN1_122
pF2_FF1_XMIT6 nF2_FF1_XMIT6	BJ41 BJ42	MGTYTXP1_122 MGTYTXN1_122
pF2_FF1_RECV5 nF2_FF1_RECV5	BG46 BG47	MGTYRXP2_122 MGTYRXN2_122
pF2_FF1_XMIT5 nF2_FF1_XMIT5	BH43 BH44	MGTYTXP2_122 MGTYTXN2_122
pF2_FF1_RECV4 nF2_FF1_RECV4	BF48 BF49	MGTYRXP3_122 MGTYRXN3_122
pF2_FF1_XMIT4 nF2_FF1_XMIT4	BF43 BF44	MGTYTXP3_122 MGTYTXN3_122

FPGA_VU13P_A2577

V_M3V3

R1052 3.3K 0603
R1053 3.3K 0603
R1054 2.2K 0603
R1055 2.2K 0603

U562-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

/F2_FF_RESET 38,69,70,71,72,73,74,75
I2C_SDA_F2_FF1_RECV 38
I2C_SCL_F2_FF1_RECV 38
/F2_FF1_RECV_INT 38
/F2_FF1_RECV_PRESENT 38

6 /RESET G1 G2 → GND
7 SDA
8 SCL
GND → 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.3V
9 RSVD
GND → 2 GND

V_3V3

C2417 +22 UF 0603 6.3V
C2418 0.1 UF 0402
L132 1.0 UH 0806
C2419 +22 UF 0603 6.3V
C2420 0.1 UF 0402

L133 1.0 UH 0806
C2421 +22 UF 0603 6.3V
C2422 0.1 UF 0402

<Implementation>

U562-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17	pF2_FF1_RECV0 nF2_FF1_RECV0
		1P 1N	B18 B17	pF2_FF1_RECV1 nF2_FF1_RECV1
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14	pF2_FF1_RECV2 nF2_FF1_RECV2
		3P 3N	B15 B14	pF2_FF1_RECV3 nF2_FF1_RECV3
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11	pF2_FF1_RECV4 nF2_FF1_RECV4
		5P 5N	B12 B11	pF2_FF1_RECV5 nF2_FF1_RECV5
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8	pF2_FF1_RECV6 nF2_FF1_RECV6
		7P 7N	B9 B8	pF2_FF1_RECV7 nF2_FF1_RECV7
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5	pF2_FF1_RECV8 nF2_FF1_RECV8
		9P 9N	B6 B5	pF2_FF1_RECV9 nF2_FF1_RECV9
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2	pF2_FF1_RECV10 nF2_FF1_RECV10
		11P 11N	B3 B2	pF2_FF1_RECV11 nF2_FF1_RECV11
B1 A1	GND_B1 GND_A1			

GND → A141 A142 A143 A144 A145 A146

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U202-26 AE GTY QUAD 123

AV39 AV40		MGTREFCLK0P_123 MGTREFCLK0N_123
AU41 AU42		MGTREFCLK1P_123 MGTREFCLK1N_123
pF2_FF1_RECV3 nF2_FF1_RECV3	BE50 BE51	MGTYRXP0_123 MGTYRXN0_123
pF2_FF1_XMIT3 nF2_FF1_XMIT3	BE45 BE46	MGTYTXP0_123 MGTYTXN0_123
pF2_FF1_RECV2 nF2_FF1_RECV2	BD48 BD49	MGTYRXP1_123 MGTYRXN1_123
pF2_FF1_XMIT2 nF2_FF1_XMIT2	BD43 BD44	MGTYTXP1_123 MGTYTXN1_123
pF2_FF1_RECV1 nF2_FF1_RECV1	BC50 BC51	MGTYRXP2_123 MGTYRXN2_123
pF2_FF1_XMIT1 nF2_FF1_XMIT1	BC45 BC46	MGTYTXP2_123 MGTYTXN2_123
pF2_FF1_RECV0 nF2_FF1_RECV0	BB48 BB49	MGTYRXP3_123 MGTYRXN3_123
pF2_FF1_XMIT0 nF2_FF1_XMIT0	BB43 BB44	MGTYTXP3_123 MGTYTXN3_123

FPGA_VU13P_A2577

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1

Title: 8.02: FPGA#2 FF#1 X12 ON QUADS AC AD AE

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Date: Thursday, March 25, 2021 | Sheet 69 of 82

8.03: FPGA#2 FF#2 X12 ON QUADS Q R S

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF2L_R0_R 18
ac_nF2L_R0_R 18
ac_pF2L_R1_R 20
ac_nF2L_R1_R 20

V_M3V3
R268 3.3K 0603
R267 3.3K 0603
R265 2.2K 0603
R266 2.2K 0603

U106-1 FIREFLY_XMIT_X12 FIREFLY XMIT X12

/F2_FF_RESET 38,69,70,71,72,73,74,75
I2C_SDA_F2_FF2_XMIT 38
I2C_SCL_F2_FF2_XMIT 38
/F2_FF2_XMIT_INT 38
/F2_FF2_XMIT_PRESENT 38

6 /RESET G1 G2
7 SDA
8 SCL
4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.8/3.3V >=25G 3.8V <=16G 3.3V
9 RSVD
2 GND

V_3V3
C2423 +-22 UF 0603 6.3V
C2424 0.1 UF 0402
L134 1.0 UH 0806
C2425 +-22 UF 0603 6.3V
C2426 0.1 UF 0402

V_F2_FF2_XMIT 30
C2427 +-22 UF 0603 6.3V
C2429 0.1 UF 0402
L135 1.0 UH 0806
C2430 +-22 UF 0603 6.3V
C2428 0.1 UF 0402

<Implementation>

U106-2 FIREFLY_XMIT_X12 FIREFLY XMIT X12

B19 A19	GND_B19 GND_A19	0P 0N	B18 B17	pF2_FF2_XMIT0 nF2_FF2_XMIT0
			A18 A17	pF2_FF2_XMIT1 nF2_FF2_XMIT1
		1P 1N		
B16 A16	GND_B16 GND_A16	2P 2N	B15 B14	pF2_FF2_XMIT2 nF2_FF2_XMIT2
			A15 A14	pF2_FF2_XMIT3 nF2_FF2_XMIT3
		3P 3N		
B13 A13	GND_B13 GND_A13	4P 4N	B12 B11	pF2_FF2_XMIT4 nF2_FF2_XMIT4
			A12 A11	pF2_FF2_XMIT5 nF2_FF2_XMIT5
		5P 5N		
B10 A10	GND_B10 GND_A10	6P 6N	B9 B8	pF2_FF2_XMIT6 nF2_FF2_XMIT6
			A9 A8	pF2_FF2_XMIT7 nF2_FF2_XMIT7
		7P 7N		
B7 A7	GND_B7 GND_A7	8P 8N	B6 B5	pF2_FF2_XMIT8 nF2_FF2_XMIT8
			A6 A5	pF2_FF2_XMIT9 nF2_FF2_XMIT9
		9P 9N		
B4 A4	GND_B4 GND_A4	10P 10N	B3 B2	pF2_FF2_XMIT10 nF2_FF2_XMIT10
			A3 A2	pF2_FF2_XMIT11 nF2_FF2_XMIT11
		11P 11N		
B1 A1	GND_B1 GND_A1			

GND
GND_A77 GND_A78 GND_A79 GND_A80 GND_A81 GND_A82

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U202-28 Q GTY QUAD 125

	AP39 AP40	MGTREFCLK0P_125 MGTREFCLK0N_125
	AN41 AN42	MGTREFCLK1P_125 MGTREFCLK1N_125
pF2_FF2_RECV11 nF2_FF2_RECV11	AU50 AU51	MGTYRXP0_125 MGTYRXN0_125
pF2_FF2_XMIT11 nF2_FF2_XMIT11	AU45 AU46	MGTYTXP0_125 MGTYTXN0_125
pF2_FF2_RECV10 nF2_FF2_RECV10	AT48 AT49	MGTYRXP1_125 MGTYRXN1_125
pF2_FF2_XMIT10 nF2_FF2_XMIT10	AT43 AT44	MGTYTXP1_125 MGTYTXN1_125
pF2_FF2_RECV9 nF2_FF2_RECV9	AR50 AR51	MGTYRXP2_125 MGTYRXN2_125
pF2_FF2_XMIT9 nF2_FF2_XMIT9	AR45 AR46	MGTYTXP2_125 MGTYTXN2_125
pF2_FF2_RECV8 nF2_FF2_RECV8	AP48 AP49	MGTYRXP3_125 MGTYRXN3_125
pF2_FF2_XMIT8 nF2_FF2_XMIT8	AP43 AP44	MGTYTXP3_125 MGTYTXN3_125

FPGA_VU13P_A2577

U202-29 R GTY QUAD 126

	AM39 AM40	MGTREFCLK0P_126 MGTREFCLK0N_126
	AL41 AL42	MGTREFCLK1P_126 MGTREFCLK1N_126
pF2_FF2_RECV7 nF2_FF2_RECV7	AN50 AN51	MGTYRXP0_126 MGTYRXN0_126
pF2_FF2_XMIT7 nF2_FF2_XMIT7	AN45 AN46	MGTYTXP0_126 MGTYTXN0_126
pF2_FF2_RECV6 nF2_FF2_RECV6	AM48 AM49	MGTYRXP1_126 MGTYRXN1_126
pF2_FF2_XMIT6 nF2_FF2_XMIT6	AM43 AM44	MGTYTXP1_126 MGTYTXN1_126
pF2_FF2_RECV5 nF2_FF2_RECV5	AL50 AL51	MGTYRXP2_126 MGTYRXN2_126
pF2_FF2_XMIT5 nF2_FF2_XMIT5	AL45 AL46	MGTYTXP2_126 MGTYTXN2_126
pF2_FF2_RECV4 nF2_FF2_RECV4	AK48 AK49	MGTYRXP3_126 MGTYRXN3_126
pF2_FF2_XMIT4 nF2_FF2_XMIT4	AK43 AK44	MGTYTXP3_126 MGTYTXN3_126

FPGA_VU13P_A2577

U202-30 S GTY QUAD 127

	AJ41 AJ42	MGTREFCLK0P_127 MGTREFCLK0N_127
	AG41 AG42	MGTREFCLK1P_127 MGTREFCLK1N_127
pF2_FF2_RECV3 nF2_FF2_RECV3	AJ50 AJ51	MGTYRXP0_127 MGTYRXN0_127
pF2_FF2_XMIT3 nF2_FF2_XMIT3	AJ45 AJ46	MGTYTXP0_127 MGTYTXN0_127
pF2_FF2_RECV2 nF2_FF2_RECV2	AH48 AH49	MGTYRXP1_127 MGTYRXN1_127
pF2_FF2_XMIT2 nF2_FF2_XMIT2	AH43 AH44	MGTYTXP1_127 MGTYTXN1_127
pF2_FF2_RECV1 nF2_FF2_RECV1	AG50 AG51	MGTYRXP2_127 MGTYRXN2_127
pF2_FF2_XMIT1 nF2_FF2_XMIT1	AG45 AG46	MGTYTXP2_127 MGTYTXN2_127
pF2_FF2_RECV0 nF2_FF2_RECV0	AF48 AF49	MGTYRXP3_127 MGTYRXN3_127
pF2_FF2_XMIT0 nF2_FF2_XMIT0	AF43 AF44	MGTYTXP3_127 MGTYTXN3_127

FPGA_VU13P_A2577

V_M3V3
R272 3.3K 0603
R271 3.3K 0603
R269 2.2K 0603
R270 2.2K 0603

U107-1 FIREFLY_RECV_X12 FIREFLY RECV X12

/F2_FF_RESET 38,69,70,71,72,73,74,75
I2C_SDA_F2_FF2_RECV 38
I2C_SCL_F2_FF2_RECV 38
/F2_FF2_RECV_INT 38
/F2_FF2_RECV_PRESENT 38

6 /RESET G1 G2
7 SDA
8 SCL
4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.3V
9 RSVD
2 GND

V_3V3
C2431 +-22 UF 0603 6.3V
C2432 0.1 UF 0402
L136 1.0 UH 0806
C2433 +-22 UF 0603 6.3V
C2434 0.1 UF 0402

L137 1.0 UH 0806
C2435 +-22 UF 0603 6.3V
C2436 0.1 UF 0402

<Implementation>

U107-2 FIREFLY_RECV_X12 FIREFLY RECV X12

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17	pF2_FF2_RECV0 nF2_FF2_RECV0
			B18 B17	pF2_FF2_RECV1 nF2_FF2_RECV1
		1P 1N		
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14	pF2_FF2_RECV2 nF2_FF2_RECV2
			B15 B14	pF2_FF2_RECV3 nF2_FF2_RECV3
		3P 3N		
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11	pF2_FF2_RECV4 nF2_FF2_RECV4
			B12 B11	pF2_FF2_RECV5 nF2_FF2_RECV5
		5P 5N		
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8	pF2_FF2_RECV6 nF2_FF2_RECV6
			B9 B8	pF2_FF2_RECV7 nF2_FF2_RECV7
		7P 7N		
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5	pF2_FF2_RECV8 nF2_FF2_RECV8
			B6 B5	pF2_FF2_RECV9 nF2_FF2_RECV9
		9P 9N		
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2	pF2_FF2_RECV10 nF2_FF2_RECV10
			B3 B2	pF2_FF2_RECV11 nF2_FF2_RECV11
		11P 11N		
B1 A1	GND_B1 GND_A1			

GND
GND_A147 GND_A148 GND_A149 GND_A150 GND_A151 GND_A152

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1			
Title: 8.03: FPGA#2 FF#2 X12 ON QUADS Q R S			
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8.04: FPGA#2 FF#3 X12 ON QUADS X Y Z

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF2L_R0_Y 18
ac_nF2L_R0_Y 18
ac_pF2L_R1_Y 20
ac_nF2L_R1_Y 20

V_M3V3
R260 3.3K 0603
R259 3.3K 0603
R257 2.2K 0603
R258 2.2K 0603

/F2_FF_RESET 38,69,70,71,72,73,74,75
I2C_SDA_F2_FF3_XMIT 38
I2C_SCL_F2_FF3_XMIT 38
/F2_FF3_XMIT_INT 38
/F2_FF3_XMIT_PRESENT 38
V_3V3
V_F2_FF3_XMIT 30

C2437 22 UF 0603 6.3V
C2438 0.1 UF 0402
C2439 22 UF 0603 6.3V
C2440 0.1 UF 0402
L138 1.0 UH 0806
C2441 22 UF 0603 6.3V
C2442 0.1 UF 0402
C2443 22 UF 0603 6.3V
C2444 0.1 UF 0402
L139 1.0 UH 0806

U104-1 FIREFLY_XMIT_X12 FIREFLY XMIT X12
6 /RESET G1 G2
7 SDA
8 SCL
GND 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.8/3.3V >=25G 3.8V <=16G 3.3V
9 RSVD
GND 2 GND
<Implementation>

U104-2 FIREFLY_XMIT_X12 FIREFLY XMIT X12

B19 A19	GND_B19 GND_A19	0P 0N	B18 B17	pF2_FF3_XMIT0 nF2_FF3_XMIT0
		1P 1N	A18 A17	pF2_FF3_XMIT1 nF2_FF3_XMIT1
B16 A16	GND_B16 GND_A16	2P 2N	B15 B14	pF2_FF3_XMIT2 nF2_FF3_XMIT2
		3P 3N	A15 A14	pF2_FF3_XMIT3 nF2_FF3_XMIT3
B13 A13	GND_B13 GND_A13	4P 4N	B12 B11	pF2_FF3_XMIT4 nF2_FF3_XMIT4
		5P 5N	A12 A11	pF2_FF3_XMIT5 nF2_FF3_XMIT5
B10 A10	GND_B10 GND_A10	6P 6N	B9 B8	pF2_FF3_XMIT6 nF2_FF3_XMIT6
		7P 7N	A9 A8	pF2_FF3_XMIT7 nF2_FF3_XMIT7
B7 A7	GND_B7 GND_A7	8P 8N	B6 B5	pF2_FF3_XMIT8 nF2_FF3_XMIT8
		9P 9N	A6 A5	pF2_FF3_XMIT9 nF2_FF3_XMIT9
B4 A4	GND_B4 GND_A4	10P 10N	B3 B2	pF2_FF3_XMIT10 nF2_FF3_XMIT10
		11P 11N	A3 A2	pF2_FF3_XMIT11 nF2_FF3_XMIT11
B1 A1	GND_B1 GND_A1			

GND 3 1 G1 2 G2 A154 / A155 / A156 / A157 / A158

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U202-35 X GTY QUAD 132

R41 R42		MGTREFCLK0P_132 MGTREFCLK0N_132
P39 P40		MGTREFCLK1P_132 MGTREFCLK1N_132
pF2_FF3_RECV11 nF2_FF3_RECV11	J50 J51	MGTYRXP0_132 MGTYRXN0_132
pF2_FF3_XMIT11 nF2_FF3_XMIT11	J45 J46	MGTYTXP0_132 MGTYTXN0_132
pF2_FF3_RECV10 nF2_FF3_RECV10	H48 H49	MGTYRXP1_132 MGTYRXN1_132
pF2_FF3_XMIT10 nF2_FF3_XMIT10	H43 H44	MGTYTXP1_132 MGTYTXN1_132
pF2_FF3_RECV9 nF2_FF3_RECV9	G50 G51	MGTYRXP2_132 MGTYRXN2_132
pF2_FF3_XMIT9 nF2_FF3_XMIT9	G45 G46	MGTYTXP2_132 MGTYTXN2_132
pF2_FF3_RECV8 nF2_FF3_RECV8	F48 F49	MGTYRXP3_132 MGTYRXN3_132
pF2_FF3_XMIT8 nF2_FF3_XMIT8	F43 F44	MGTYTXP3_132 MGTYTXN3_132

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U202-36 Y GTY QUAD 133

N41 N42		MGTREFCLK0P_133 MGTREFCLK0N_133
M39 M40		MGTREFCLK1P_133 MGTREFCLK1N_133
pF2_FF3_RECV7 nF2_FF3_RECV7	E50 E51	MGTYRXP0_133 MGTYRXN0_133
pF2_FF3_XMIT7 nF2_FF3_XMIT7	D43 D44	MGTYTXP0_133 MGTYTXN0_133
pF2_FF3_RECV6 nF2_FF3_RECV6	D48 D49	MGTYRXP1_133 MGTYRXN1_133
pF2_FF3_XMIT6 nF2_FF3_XMIT6	B43 B44	MGTYTXP1_133 MGTYTXN1_133
pF2_FF3_RECV5 nF2_FF3_RECV5	E46 E47	MGTYRXP2_133 MGTYRXN2_133
pF2_FF3_XMIT5 nF2_FF3_XMIT5	C41 C42	MGTYTXP2_133 MGTYTXN2_133
pF2_FF3_RECV4 nF2_FF3_RECV4	C46 C47	MGTYRXP3_133 MGTYRXN3_133
pF2_FF3_XMIT4 nF2_FF3_XMIT4	E41 E42	MGTYTXP3_133 MGTYTXN3_133

FPGA_VU13P_A2577

V_M3V3
R264 3.3K 0603
R263 3.3K 0603
R261 2.2K 0603
R262 2.2K 0603

/F2_FF_RESET 38,69,70,71,72,73,74,75
I2C_SDA_F2_FF3_RECV 38
I2C_SCL_F2_FF3_RECV 38
/F2_FF3_RECV_INT 38
/F2_FF3_RECV_PRESENT 38
V_3V3

C2445 22 UF 0603 6.3V
C2446 0.1 UF 0402
C2447 22 UF 0603 6.3V
C2448 0.1 UF 0402
L140 1.0 UH 0806
C2449 22 UF 0603 6.3V
C2450 0.1 UF 0402
L141 1.0 UH 0806

U105-1 FIREFLY_RECV_X12 FIREFLY RECV X12
6 /RESET G1 G2
7 SDA
8 SCL
GND 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.3V
9 RSVD
GND 2 GND
<Implementation>

U105-2 FIREFLY_RECV_X12 FIREFLY RECV X12

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17	pF2_FF3_RECV0 nF2_FF3_RECV0
		1P 1N	B18 B17	pF2_FF3_RECV1 nF2_FF3_RECV1
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14	pF2_FF3_RECV2 nF2_FF3_RECV2
		3P 3N	B15 B14	pF2_FF3_RECV3 nF2_FF3_RECV3
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11	pF2_FF3_RECV4 nF2_FF3_RECV4
		5P 5N	B12 B11	pF2_FF3_RECV5 nF2_FF3_RECV5
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8	pF2_FF3_RECV6 nF2_FF3_RECV6
		7P 7N	B9 B8	pF2_FF3_RECV7 nF2_FF3_RECV7
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5	pF2_FF3_RECV8 nF2_FF3_RECV8
		9P 9N	B6 B5	pF2_FF3_RECV9 nF2_FF3_RECV9
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2	pF2_FF3_RECV10 nF2_FF3_RECV10
		11P 11N	B3 B2	pF2_FF3_RECV11 nF2_FF3_RECV11
B1 A1	GND_B1 GND_A1			

GND 3 1 G1 2 G2 A159 / A160 / A161 / A162 / A163 / A164

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U202-37 Z GTY QUAD 134

L41 L42		MGTREFCLK0P_134 MGTREFCLK0N_134
K39 K40		MGTREFCLK1P_134 MGTREFCLK1N_134
pF2_FF3_RECV3 nF2_FF3_RECV3	A46 A47	MGTYRXP0_134 MGTYRXN0_134
pF2_FF3_XMIT3 nF2_FF3_XMIT3	A41 A42	MGTYTXP0_134 MGTYTXN0_134
pF2_FF3_RECV2 nF2_FF3_RECV2	A32 A33	MGTYRXP1_134 MGTYRXN1_134
pF2_FF3_XMIT2 nF2_FF3_XMIT2	B39 B40	MGTYTXP1_134 MGTYTXN1_134
pF2_FF3_RECV1 nF2_FF3_RECV1	B34 B35	MGTYRXP2_134 MGTYRXN2_134
pF2_FF3_XMIT1 nF2_FF3_XMIT1	A37 A38	MGTYTXP2_134 MGTYTXN2_134
pF2_FF3_RECV0 nF2_FF3_RECV0	C32 C33	MGTYRXP3_134 MGTYRXN3_134
pF2_FF3_XMIT0 nF2_FF3_XMIT0	C37 C38	MGTYTXP3_134 MGTYTXN3_134

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ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1		
Title: 8.04: FPGA#2 FF#3 X12 ON QUADS X Y Z		
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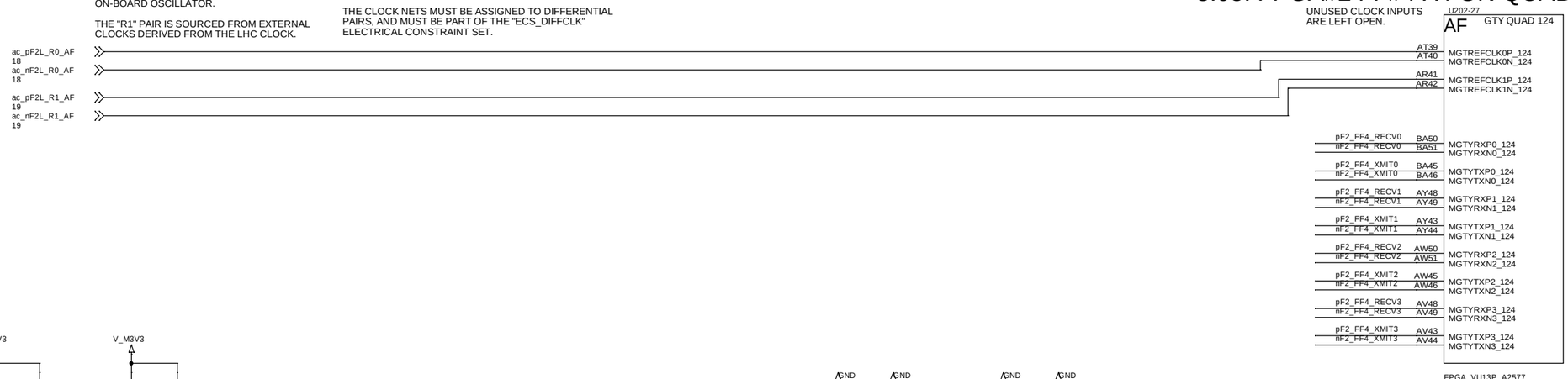
8.05: FPGA#2 FF#4 X4 ON QUAD AF

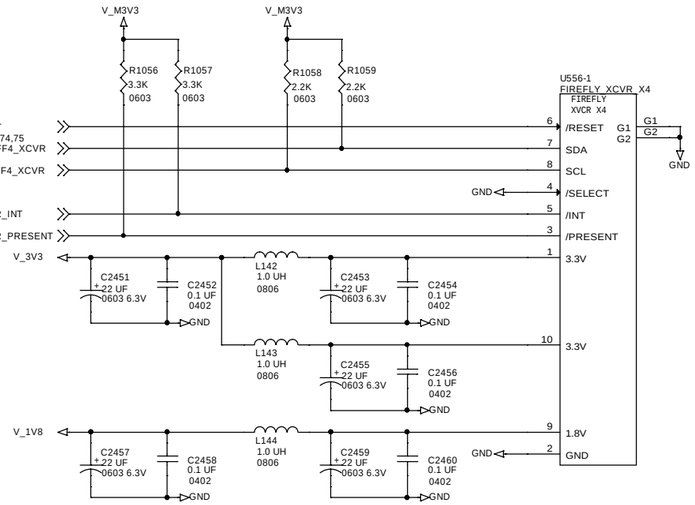
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

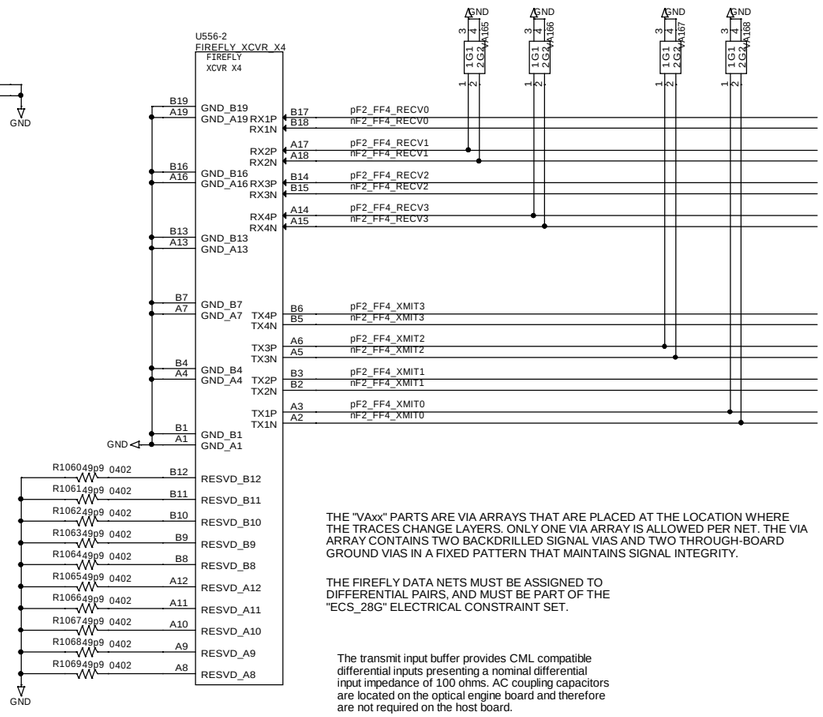
THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.







THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1		
Title: 8.05: FPGA#2 FF#4 X4 ON QUAD AF		
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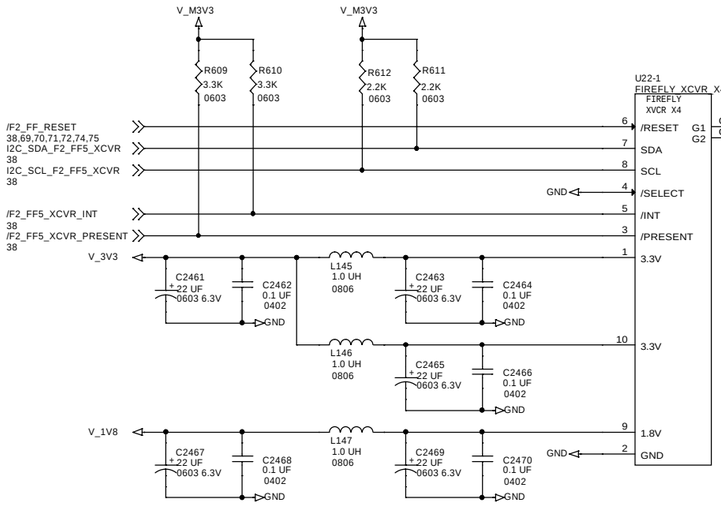
8.06: FPGA#2 FF#5 X4 ON QUAD T

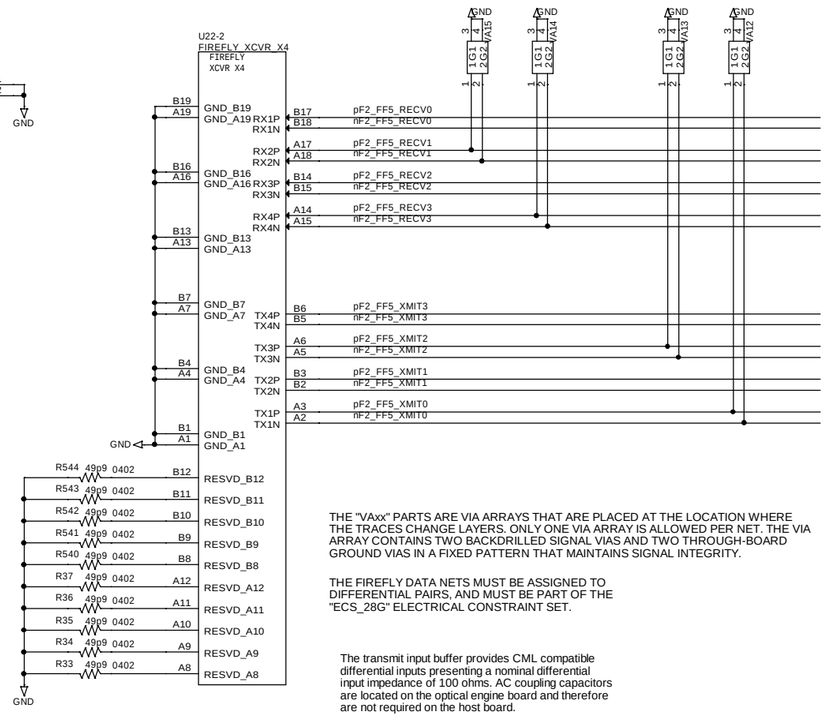
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

U202-31
GTY QUAD 128

	AE41	
	AE42	MGTREFCLK0P_128
		MGTREFCLK0N_128
	AC41	
	AC42	MGTREFCLK1P_128
		MGTREFCLK1N_128
pF2_FF5_RECV0	AE50	MGTYRXP0_128
nF2_FF5_RECV0	AE51	MGTYRXN0_128
pF2_FF5_XMIT0	AE45	MGTYTXP0_128
nF2_FF5_XMIT0	AE46	MGTYTXN0_128
pF2_FF5_RECV1	AD48	MGTYRXP1_128
nF2_FF5_RECV1	AD49	MGTYRXN1_128
pF2_FF5_XMIT1	AD43	MGTYTXP1_128
nF2_FF5_XMIT1	AD44	MGTYTXN1_128
pF2_FF5_RECV2	AC50	MGTYRXP2_128
nF2_FF5_RECV2	AC51	MGTYRXN2_128
pF2_FF5_XMIT2	AC45	MGTYTXP2_128
nF2_FF5_XMIT2	AC46	MGTYTXN2_128
pF2_FF5_RECV3	AB48	MGTYRXP3_128
nF2_FF5_RECV3	AB49	MGTYRXN3_128
pF2_FF5_XMIT3	AB43	MGTYTXP3_128
nF2_FF5_XMIT3	AB44	MGTYTXN3_128

FPGA_VU13P_A2577





ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1		
Title: 8.06: FPGA#2 FF#5 X4 ON QUAD T		
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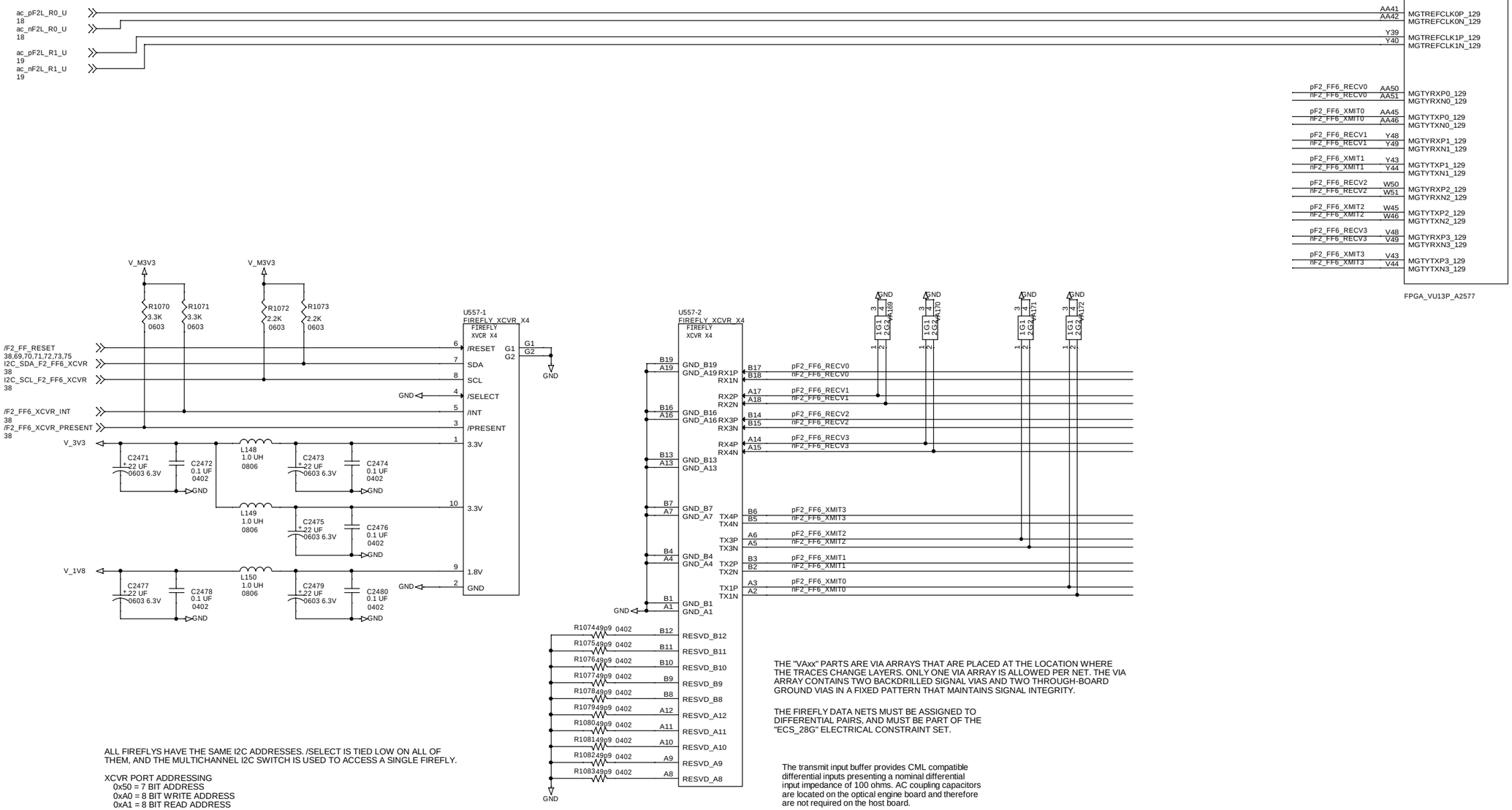
8.07: FPGA#2 FF#6 X4 ON QUAD U

UNUSED CLOCK INPUTS
ARE LEFT OPEN.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1		
Title: 8.07: FPGA#2 FF#6 X4 ON QUAD U		
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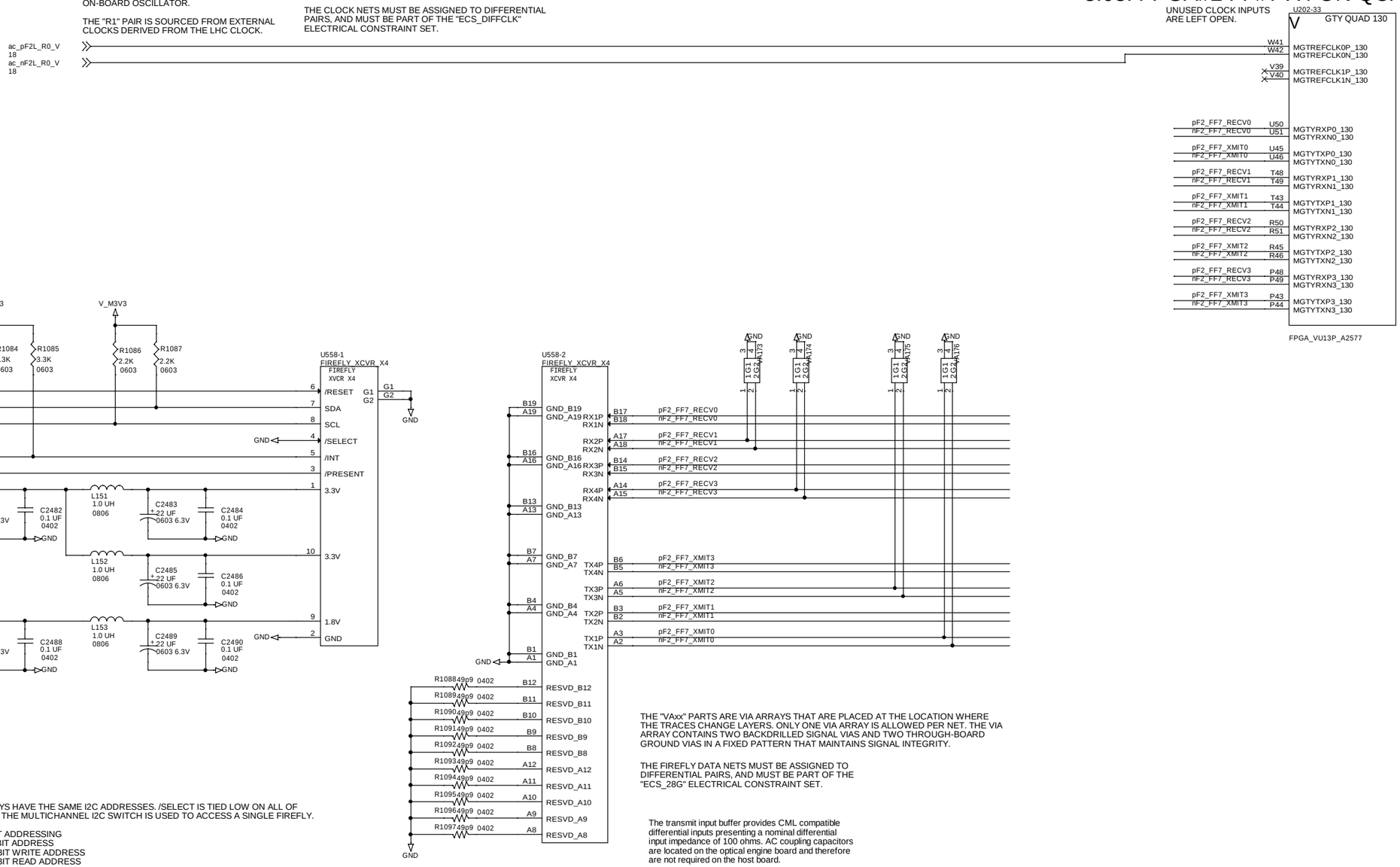
8.08: FPGA#2 FF#7 X4 ON QUAD V

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1

Title: 8.08: FPGA#2 FF#7 X4 ON QUAD V

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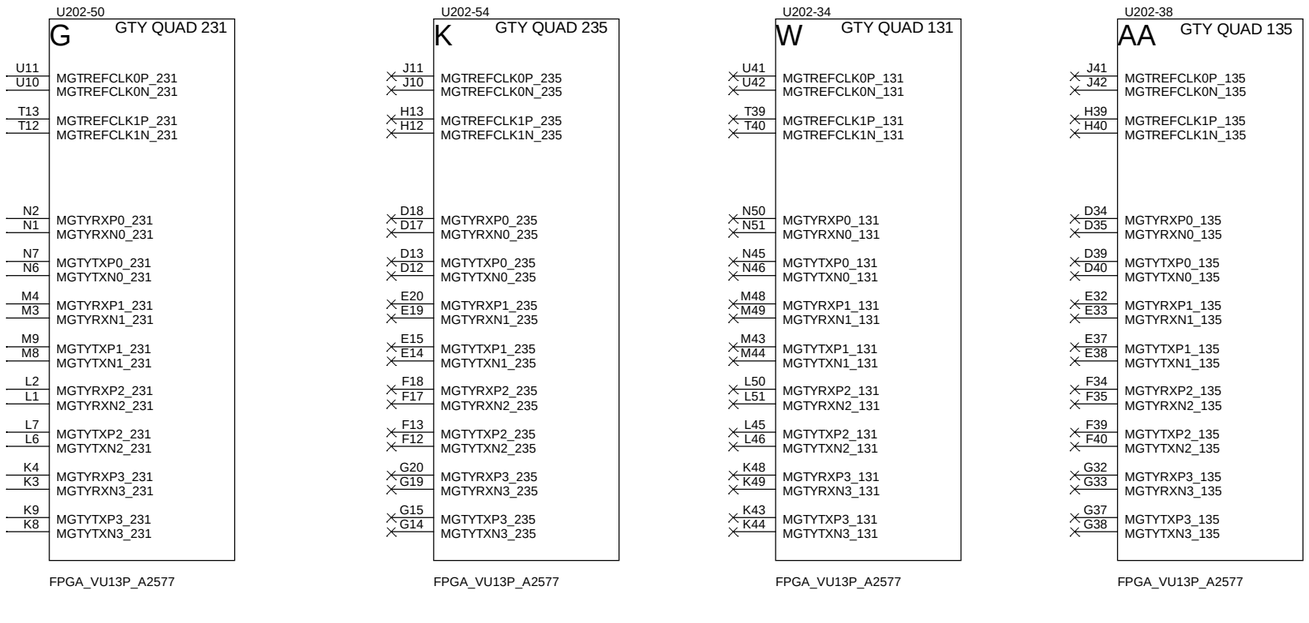
8.09: FPGA#2 UNUSED QUADS G, K, W, AA



APOLLO CM W/ DUAL A2577, MK1		
Title: 8.09: FPGA#2 UNUSED QUADS G, K, W, AA		
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9.01: F1 QUADS M, N, O TO F2 QUADS J, I, H

FPGA#1

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

FPGA#2

U201-40
GTY QUAD 221 M

MGTREFCLK0P_221	BB13	
MGTREFCLK0N_221	BB12	
MGTREFCLK1P_221	BA11	
MGTREFCLK1N_221	BA10	
MGTYRXP0_221	BK18	pF1_M_RECV0
MGTYRXN0_221	BK17	nF1_M_RECV0
MGTYTXP0_221	BL15	pF1_M_XMIT0
MGTYTXN0_221	BL14	nF1_M_XMIT0
MGTYRXP1_221	BL20	pF1_M_RECV1
MGTYRXN1_221	BL19	nF1_M_RECV1
MGTYTXP1_221	BK13	pF1_M_XMIT1
MGTYTXN1_221	BK12	nF1_M_XMIT1
MGTYRXP2_221	BL6	pF1_M_RECV2
MGTYRXN2_221	BL5	nF1_M_RECV2
MGTYTXP2_221	BL11	pF1_M_XMIT2
MGTYTXN2_221	BL10	nF1_M_XMIT2
MGTYRXP3_221	BJ6	pF1_M_RECV3
MGTYRXN3_221	BJ5	nF1_M_RECV3
MGTYTXP3_221	BK9	pF1_M_XMIT3
MGTYTXN3_221	BK8	nF1_M_XMIT3

FPGA_VU13P_A2577

U201-41
GTY QUAD 222 N

MGTREFCLK0P_222	AY13	ac_pF1R_R0_N 18
MGTREFCLK0N_222	AY12	ac_nF1R_R0_N 18
MGTREFCLK1P_222	AW11	ac_pF1R_R1_N 21
MGTREFCLK1N_222	AW10	ac_nF1R_R1_N 21
MGTYRXP0_222	BH4	pF1_N_RECV0
MGTYRXN0_222	BH3	nF1_N_RECV0
MGTYTXP0_222	BG11	pF1_N_XMIT0
MGTYTXN0_222	BG10	nF1_N_XMIT0
MGTYRXP1_222	BG2	pF1_N_RECV1
MGTYRXN1_222	BG1	nF1_N_RECV1
MGTYTXP1_222	BJ11	pF1_N_XMIT1
MGTYTXN1_222	BJ10	nF1_N_XMIT1
MGTYRXP2_222	BG6	pF1_N_RECV2
MGTYRXN2_222	BG5	nF1_N_RECV2
MGTYTXP2_222	BH9	pF1_N_XMIT2
MGTYTXN2_222	BH8	nF1_N_XMIT2
MGTYRXP3_222	BF4	pF1_N_RECV3
MGTYRXN3_222	BF3	nF1_N_RECV3
MGTYTXP3_222	BF9	pF1_N_XMIT3
MGTYTXN3_222	BF8	nF1_N_XMIT3

FPGA_VU13P_A2577

U201-42
GTY QUAD 223 O

MGTREFCLK0P_223	AV13	
MGTREFCLK0N_223	AV12	
MGTREFCLK1P_223	AU11	
MGTREFCLK1N_223	AU10	
MGTYRXP0_223	BE2	pF1_O_RECV0
MGTYRXN0_223	BE1	nF1_O_RECV0
MGTYTXP0_223	BE7	pF1_O_XMIT0
MGTYTXN0_223	BE6	nF1_O_XMIT0
MGTYRXP1_223	BD4	pF1_O_RECV1
MGTYRXN1_223	BD3	nF1_O_RECV1
MGTYTXP1_223	BD9	pF1_O_XMIT1
MGTYTXN1_223	BD8	nF1_O_XMIT1
MGTYRXP2_223	BC2	pF1_O_RECV2
MGTYRXN2_223	BC1	nF1_O_RECV2
MGTYTXP2_223	BC7	pF1_O_XMIT2
MGTYTXN2_223	BC6	nF1_O_XMIT2
MGTYRXP3_223	BB4	pF1_O_RECV3
MGTYRXN3_223	BB3	nF1_O_RECV3
MGTYTXP3_223	BB9	pF1_O_XMIT3
MGTYTXN3_223	BB8	nF1_O_XMIT3

FPGA_VU13P_A2577

pF1_M_RECV0	C1804 0.1 UF 0402	pF2_J_XMIT0	nF2_J_XMIT0
pF1_M_RECV1	C1805 0.1 UF 0402	pF2_J_XMIT1	nF2_J_XMIT1
pF1_M_RECV2	C1807 0.1 UF 0402	pF2_J_XMIT2	nF2_J_XMIT2
pF1_M_RECV3	C1809 0.1 UF 0402	pF2_J_XMIT3	nF2_J_XMIT3
	C1811 0.1 UF 0402		
	C1813 0.1 UF 0402		
	C1815 0.1 UF 0402		
	C1817 0.1 UF 0402		

pF1_M_XMIT0	0402 0.1 UF C1806	pF2_J_RECV0	nF2_J_RECV0
pF1_M_XMIT1	0402 0.1 UF C1808	pF2_J_RECV1	nF2_J_RECV1
pF1_M_XMIT2	0402 0.1 UF C1810	pF2_J_RECV2	nF2_J_RECV2
pF1_M_XMIT3	0402 0.1 UF C1812	pF2_J_RECV3	nF2_J_RECV3
	0402 0.1 UF C1814		
	0402 0.1 UF C1816		
	0402 0.1 UF C1818		
	0402 0.1 UF C1819		

U202-53
GTY QUAD 234 J

L11	MGTREFCLK0P_234	
L10	MGTREFCLK0N_234	
K13	MGTREFCLK1P_234	
K12	MGTREFCLK1N_234	
A6	MGTYRXP0_234	pF2_J_RECV0
A5	MGTYRXN0_234	nF2_J_RECV0
A11	MGTYTXP0_234	pF2_J_XMIT0
A10	MGTYTXN0_234	nF2_J_XMIT0
A20	MGTYRXP1_234	pF2_J_RECV1
A19	MGTYRXN1_234	nF2_J_RECV1
B13	MGTYTXP1_234	pF2_J_XMIT1
B12	MGTYTXN1_234	nF2_J_XMIT1
B18	MGTYRXP2_234	pF2_J_RECV2
B17	MGTYRXN2_234	nF2_J_RECV2
A15	MGTYTXP2_234	pF2_J_XMIT2
A14	MGTYTXN2_234	nF2_J_XMIT2
C20	MGTYRXP3_234	pF2_J_RECV3
C19	MGTYRXN3_234	nF2_J_RECV3
C15	MGTYTXP3_234	pF2_J_XMIT3
C14	MGTYTXN3_234	nF2_J_XMIT3

FPGA_VU13P_A2577

U202-52
GTY QUAD 233 I

ac_pF2R_R0_I 18	MGTREFCLK0P_233	N11
ac_nF2R_R0_I 18	MGTREFCLK0N_233	N10
ac_pF2R_R1_I 21	MGTREFCLK1P_233	M13
ac_nF2R_R1_I 21	MGTREFCLK1N_233	M12
MGTYRXP0_233	E2	pF2_I_RECV0
MGTYRXN0_233	E1	nF2_I_RECV0
MGTYTXP0_233	D9	pF2_I_XMIT0
MGTYTXN0_233	D8	nF2_I_XMIT0
MGTYRXP1_233	D4	pF2_I_RECV1
MGTYRXN1_233	D3	nF2_I_RECV1
MGTYTXP1_233	B9	pF2_I_XMIT1
MGTYTXN1_233	B8	nF2_I_XMIT1
MGTYRXP2_233	E6	pF2_I_RECV2
MGTYRXN2_233	E5	nF2_I_RECV2
MGTYTXP2_233	C11	pF2_I_XMIT2
MGTYTXN2_233	C10	nF2_I_XMIT2
MGTYRXP3_233	C6	pF2_I_RECV3
MGTYRXN3_233	C5	nF2_I_RECV3
MGTYTXP3_233	E11	pF2_I_XMIT3
MGTYTXN3_233	E10	nF2_I_XMIT3

FPGA_VU13P_A2577

pF1_N_RECV0	C1820 0.1 UF 0402	pF2_I_XMIT0	nF2_I_XMIT0
pF1_N_RECV1	C1821 0.1 UF 0402	pF2_I_XMIT1	nF2_I_XMIT1
pF1_N_RECV2	C1823 0.1 UF 0402	pF2_I_XMIT2	nF2_I_XMIT2
pF1_N_RECV3	C1825 0.1 UF 0402	pF2_I_XMIT3	nF2_I_XMIT3
	C1827 0.1 UF 0402		
	C1829 0.1 UF 0402		
	C1831 0.1 UF 0402		
	C1833 0.1 UF 0402		

pF1_N_XMIT0	0402 0.1 UF C1822	pF2_I_RECV0	nF2_I_RECV0
pF1_N_XMIT1	0402 0.1 UF C1824	pF2_I_RECV1	nF2_I_RECV1
pF1_N_XMIT2	0402 0.1 UF C1826	pF2_I_RECV2	nF2_I_RECV2
pF1_N_XMIT3	0402 0.1 UF C1828	pF2_I_RECV3	nF2_I_RECV3
	0402 0.1 UF C1830		
	0402 0.1 UF C1832		
	0402 0.1 UF C1834		
	0402 0.1 UF C1835		

pF1_O_RECV0	C1836 0.1 UF 0402	pF2_H_XMIT0	nF2_H_XMIT0
pF1_O_RECV1	C1837 0.1 UF 0402	pF2_H_XMIT1	nF2_H_XMIT1
pF1_O_RECV2	C1839 0.1 UF 0402	pF2_H_XMIT2	nF2_H_XMIT2
pF1_O_RECV3	C1841 0.1 UF 0402	pF2_H_XMIT3	nF2_H_XMIT3
	C1843 0.1 UF 0402		
	C1845 0.1 UF 0402		
	C1847 0.1 UF 0402		
	C1849 0.1 UF 0402		

pF1_O_XMIT0	0402 0.1 UF C1838	pF2_H_RECV0	nF2_H_RECV0
pF1_O_XMIT1	0402 0.1 UF C1840	pF2_H_RECV1	nF2_H_RECV1
pF1_O_XMIT2	0402 0.1 UF C1842	pF2_H_RECV2	nF2_H_RECV2
pF1_O_XMIT3	0402 0.1 UF C1844	pF2_H_RECV3	nF2_H_RECV3
	0402 0.1 UF C1846		
	0402 0.1 UF C1848		
	0402 0.1 UF C1850		
	0402 0.1 UF C1851		

U202-51
GTY QUAD 232 H

R11	MGTREFCLK0P_232	
R10	MGTREFCLK0N_232	
P13	MGTREFCLK1P_232	
P12	MGTREFCLK1N_232	
J2	MGTYRXP0_232	pF2_H_RECV0
J1	MGTYRXN0_232	nF2_H_RECV0
J7	MGTYTXP0_232	pF2_H_XMIT0
J6	MGTYTXN0_232	nF2_H_XMIT0
H4	MGTYRXP1_232	pF2_H_RECV1
H3	MGTYRXN1_232	nF2_H_RECV1
H9	MGTYTXP1_232	pF2_H_XMIT1
H8	MGTYTXN1_232	nF2_H_XMIT1
G2	MGTYRXP2_232	pF2_H_RECV2
G1	MGTYRXN2_232	nF2_H_RECV2
G7	MGTYTXP2_232	pF2_H_XMIT2
G6	MGTYTXN2_232	nF2_H_XMIT2
F4	MGTYRXP3_232	pF2_H_RECV3
F3	MGTYRXN3_232	nF2_H_RECV3
F9	MGTYTXP3_232	pF2_H_XMIT3
F8	MGTYTXN3_232	nF2_H_XMIT3

FPGA_VU13P_A2577

APOLLO CM W/ DUAL A2577, MK1

Title: 9.01: F1 QUADS M, N, O TO F2 QUADS J, I, H

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9.02: F1 QUADS A, B, C TO F2 QUADS F, E, D

FPGA#1

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

FPGA#2

U201-44 — GTY QUAD 225 A

MGTREFCLK0P_225	AP13		
MGTREFCLK0N_225	AP12		
MGTREFCLK1P_225	AN11		
MGTREFCLK1N_225	AN10		
MGTYRXP0_225	AU2	pF1_A_RECV0	nF1_A_RECV0
MGTYRXN0_225	AU1		
MGTYTXP0_225	AU7	pF1_A_XMIT0	nF1_A_XMIT0
MGTYTXN0_225	AU6		
MGTYRXP1_225	AT4	pF1_A_RECV1	nF1_A_RECV1
MGTYRXN1_225	AT3		
MGTYTXP1_225	AT9	pF1_A_XMIT1	nF1_A_XMIT1
MGTYTXN1_225	AT8		
MGTYRXP2_225	AR2	pF1_A_RECV2	nF1_A_RECV2
MGTYRXN2_225	AR1		
MGTYTXP2_225	AR7	pF1_A_XMIT2	nF1_A_XMIT2
MGTYTXN2_225	AR6		
MGTYRXP3_225	AP4	pF1_A_RECV3	nF1_A_RECV3
MGTYRXN3_225	AP3		
MGTYTXP3_225	AP9	pF1_A_XMIT3	nF1_A_XMIT3
MGTYTXN3_225	AP8		

FPGA_VU13P_A2577

U202-49 — GTY QUAD 230 F

ac_pF2R_R0_F 18	W11		
ac_nF2R_R0_F 18	W10		
MGTREFCLK0P_230	V13		
MGTREFCLK0N_230	V12		
MGTYRXP0_230	U2	pF2_F_RECV0	nF2_F_RECV0
MGTYRXN0_230	U1		
MGTYTXP0_230	U7	pF2_F_XMIT0	nF2_F_XMIT0
MGTYTXN0_230	U6		
MGTYRXP1_230	T4	pF2_F_RECV1	nF2_F_RECV1
MGTYRXN1_230	T3		
MGTYTXP1_230	T9	pF2_F_XMIT1	nF2_F_XMIT1
MGTYTXN1_230	T8		
MGTYRXP2_230	R2	pF2_F_RECV2	nF2_F_RECV2
MGTYRXN2_230	R1		
MGTYTXP2_230	R7	pF2_F_XMIT2	nF2_F_XMIT2
MGTYTXN2_230	R6		
MGTYRXP3_230	P4	pF2_F_RECV3	nF2_F_RECV3
MGTYRXN3_230	P3		
MGTYTXP3_230	P9	pF2_F_XMIT3	nF2_F_XMIT3
MGTYTXN3_230	P8		

FPGA_VU13P_A2577

U201-45 — GTY QUAD 226 B

ac_pF1R_R0_B 18			
ac_nF1R_R0_B 18			
MGTREFCLK0P_226	AM13		
MGTREFCLK0N_226	AM12		
ac_pF1R_R1_B 21			
ac_nF1R_R1_B 21			
MGTREFCLK1P_226	AL11		
MGTREFCLK1N_226	AL10		
MGTYRXP0_226	AN2	pF1_B_RECV0	nF1_B_RECV0
MGTYRXN0_226	AN1		
MGTYTXP0_226	AN7	pF1_B_XMIT0	nF1_B_XMIT0
MGTYTXN0_226	AN6		
MGTYRXP1_226	AM4	pF1_B_RECV1	nF1_B_RECV1
MGTYRXN1_226	AM3		
MGTYTXP1_226	AM9	pF1_B_XMIT1	nF1_B_XMIT1
MGTYTXN1_226	AM8		
MGTYRXP2_226	AL2	pF1_B_RECV2	nF1_B_RECV2
MGTYRXN2_226	AL1		
MGTYTXP2_226	AL7	pF1_B_XMIT2	nF1_B_XMIT2
MGTYTXN2_226	AL6		
MGTYRXP3_226	AK4	pF1_B_RECV3	nF1_B_RECV3
MGTYRXN3_226	AK3		
MGTYTXP3_226	AK9	pF1_B_XMIT3	nF1_B_XMIT3
MGTYTXN3_226	AK8		

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U202-48 — GTY QUAD 229 E

ac_pF2R_R0_E 18			
ac_nF2R_R0_E 18	AA11		
MGTREFCLK0P_229	AA10		
MGTREFCLK0N_229			
ac_pF2R_R1_E 21	Y13		
ac_nF2R_R1_E 21	Y12		
MGTREFCLK1P_229			
MGTREFCLK1N_229			
MGTYRXP0_229	AA2	pF2_E_RECV0	nF2_E_RECV0
MGTYRXN0_229	AA1		
MGTYTXP0_229	AA7	pF2_E_XMIT0	nF2_E_XMIT0
MGTYTXN0_229	AA6		
MGTYRXP1_229	Y4	pF2_E_RECV1	nF2_E_RECV1
MGTYRXN1_229	Y3		
MGTYTXP1_229	Y9	pF2_E_XMIT1	nF2_E_XMIT1
MGTYTXN1_229	Y8		
MGTYRXP2_229	W2	pF2_E_RECV2	nF2_E_RECV2
MGTYRXN2_229	W1		
MGTYTXP2_229	W7	pF2_E_XMIT2	nF2_E_XMIT2
MGTYTXN2_229	W6		
MGTYRXP3_229	V4	pF2_E_RECV3	nF2_E_RECV3
MGTYRXN3_229	V3		
MGTYTXP3_229	V9	pF2_E_XMIT3	nF2_E_XMIT3
MGTYTXN3_229	V8		

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U201-46 — GTY QUAD 227 C

MGTREFCLK0P_227	AJ11		
MGTREFCLK0N_227	AJ10		
MGTREFCLK1P_227	AG11		
MGTREFCLK1N_227	AG10		
MGTYRXP0_227	AJ2	pF1_C_RECV0	nF1_C_RECV0
MGTYRXN0_227	AJ1		
MGTYTXP0_227	AJ7	pF1_C_XMIT0	nF1_C_XMIT0
MGTYTXN0_227	AJ6		
MGTYRXP1_227	AH4	pF1_C_RECV1	nF1_C_RECV1
MGTYRXN1_227	AH3		
MGTYTXP1_227	AH9	pF1_C_XMIT1	nF1_C_XMIT1
MGTYTXN1_227	AH8		
MGTYRXP2_227	AG2	pF1_C_RECV2	nF1_C_RECV2
MGTYRXN2_227	AG1		
MGTYTXP2_227	AG7	pF1_C_XMIT2	nF1_C_XMIT2
MGTYTXN2_227	AG6		
MGTYRXP3_227	AF4	pF1_C_RECV3	nF1_C_RECV3
MGTYRXN3_227	AF3		
MGTYTXP3_227	AF9	pF1_C_XMIT3	nF1_C_XMIT3
MGTYTXN3_227	AF8		

FPGA_VU13P_A2577

U202-47 — GTY QUAD 228 D

MGTREFCLK0P_228	AE11		
MGTREFCLK0N_228	AE10		
MGTREFCLK1P_228	AC11		
MGTREFCLK1N_228	AC10		
MGTYRXP0_228	AE2	pF2_D_RECV0	nF2_D_RECV0
MGTYRXN0_228	AE1		
MGTYTXP0_228	AE7	pF2_D_XMIT0	nF2_D_XMIT0
MGTYTXN0_228	AE6		
MGTYRXP1_228	AD4	pF2_D_RECV1	nF2_D_RECV1
MGTYRXN1_228	AD3		
MGTYTXP1_228	AD9	pF2_D_XMIT1	nF2_D_XMIT1
MGTYTXN1_228	AD8		
MGTYRXP2_228	AC2	pF2_D_RECV2	nF2_D_RECV2
MGTYRXN2_228	AC1		
MGTYTXP2_228	AC7	pF2_D_XMIT2	nF2_D_XMIT2
MGTYTXN2_228	AC6		
MGTYRXP3_228	AB4	pF2_D_RECV3	nF2_D_RECV3
MGTYRXN3_228	AB3		
MGTYTXP3_228	AB9	pF2_D_XMIT3	nF2_D_XMIT3
MGTYTXN3_228	AB8		

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AC Coupling Capacitors

pF1_A_RECV0	nF1_A_RECV0	C1852 0.1 UF 0402	pF2_F_XMIT0 nF2_F_XMIT0
pF1_A_RECV1	nF1_A_RECV1	C1853 0.1 UF 0402	pF2_F_XMIT1 nF2_F_XMIT1
pF1_A_RECV2	nF1_A_RECV2	C1855 0.1 UF 0402	pF2_F_XMIT2 nF2_F_XMIT2
pF1_A_RECV3	nF1_A_RECV3	C1857 0.1 UF 0402	pF2_F_XMIT3 nF2_F_XMIT3
		C1859 0.1 UF 0402	
		C1861 0.1 UF 0402	
		C1863 0.1 UF 0402	
		C1865 0.1 UF 0402	

pF1_A_XMIT0	nF1_A_XMIT0	0402 0.1 UF C1854	pF2_F_RECV0 nF2_F_RECV0
		0402 0.1 UF C1856	
pF1_A_XMIT1	nF1_A_XMIT1	0402 0.1 UF C1858	pF2_F_RECV1 nF2_F_RECV1
		0402 0.1 UF C1860	
pF1_A_XMIT2	nF1_A_XMIT2	0402 0.1 UF C1862	pF2_F_RECV2 nF2_F_RECV2
		0402 0.1 UF C1864	
pF1_A_XMIT3	nF1_A_XMIT3	0402 0.1 UF C1866	pF2_F_RECV3 nF2_F_RECV3
		0402 0.1 UF C1867	

pF1_B_RECV0	nF1_B_RECV0	C1868 0.1 UF 0402	pF2_E_XMIT0 nF2_E_XMIT0
pF1_B_RECV1	nF1_B_RECV1	C1869 0.1 UF 0402	pF2_E_XMIT1 nF2_E_XMIT1
pF1_B_RECV2	nF1_B_RECV2	C1871 0.1 UF 0402	pF2_E_XMIT2 nF2_E_XMIT2
pF1_B_RECV3	nF1_B_RECV3	C1873 0.1 UF 0402	pF2_E_XMIT3 nF2_E_XMIT3
		C1875 0.1 UF 0402	
		C1877 0.1 UF 0402	
		C1879 0.1 UF 0402	
		C1881 0.1 UF 0402	

pF1_B_XMIT0	nF1_B_XMIT0	0402 0.1 UF C1870	pF2_E_RECV0 nF2_E_RECV0
		0402 0.1 UF C1872	
pF1_B_XMIT1	nF1_B_XMIT1	0402 0.1 UF C1874	pF2_E_RECV1 nF2_E_RECV1
		0402 0.1 UF C1876	
pF1_B_XMIT2	nF1_B_XMIT2	0402 0.1 UF C1878	pF2_E_RECV2 nF2_E_RECV2
		0402 0.1 UF C1880	
pF1_B_XMIT3	nF1_B_XMIT3	0402 0.1 UF C1882	pF2_E_RECV3 nF2_E_RECV3
		0402 0.1 UF C1883	

pF1_C_RECV0	nF1_C_RECV0	C1884 0.1 UF 0402	pF2_D_XMIT0 nF2_D_XMIT0
pF1_C_RECV1	nF1_C_RECV1	C1885 0.1 UF 0402	pF2_D_XMIT1 nF2_D_XMIT1
pF1_C_RECV2	nF1_C_RECV2	C1887 0.1 UF 0402	pF2_D_XMIT2 nF2_D_XMIT2
pF1_C_RECV3	nF1_C_RECV3	C1889 0.1 UF 0402	pF2_D_XMIT3 nF2_D_XMIT3
		C1891 0.1 UF 0402	
		C1893 0.1 UF 0402	
		C1895 0.1 UF 0402	
		C1897 0.1 UF 0402	

pF1_C_XMIT0	nF1_C_XMIT0	0402 0.1 UF C1886	pF2_D_RECV0 nF2_D_RECV0
		0402 0.1 UF C1888	
pF1_C_XMIT1	nF1_C_XMIT1	0402 0.1 UF C1890	pF2_D_RECV1 nF2_D_RECV1
		0402 0.1 UF C1892	
pF1_C_XMIT2	nF1_C_XMIT2	0402 0.1 UF C1894	pF2_D_RECV2 nF2_D_RECV2
		0402 0.1 UF C1896	
pF1_C_XMIT3	nF1_C_XMIT3	0402 0.1 UF C1898	pF2_D_RECV3 nF2_D_RECV3
		0402 0.1 UF C1899	

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Title: 9.02: F1 QUADS A, B, C TO F2 QUADS F, E, D

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9.03: F1 QUADS H, I, J TO F2 QUADS O, N, M

FPGA#1

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

FPGA#2

U201-51
GTY QUAD 232 H

MGTREFCLK0P_232	R11	
MGTREFCLK0N_232	R10	
MGTREFCLK1P_232	P13	
MGTREFCLK1N_232	P12	
MGTYRXP0_232	J2	pF1_H_RECV0
MGTYRXN0_232	J1	nF1_H_RECV0
MGTYTXP0_232	J7	pF1_H_XMIT0
MGTYTXN0_232	J6	nF1_H_XMIT0
MGTYRXP1_232	H4	pF1_H_RECV1
MGTYRXN1_232	H3	nF1_H_RECV1
MGTYTXP1_232	H9	pF1_H_XMIT1
MGTYTXN1_232	H8	nF1_H_XMIT1
MGTYRXP2_232	G2	pF1_H_RECV2
MGTYRXN2_232	G1	nF1_H_RECV2
MGTYTXP2_232	G7	pF1_H_XMIT2
MGTYTXN2_232	G6	nF1_H_XMIT2
MGTYRXP3_232	F4	pF1_H_RECV3
MGTYRXN3_232	F3	nF1_H_RECV3
MGTYTXP3_232	F9	pF1_H_XMIT3
MGTYTXN3_232	F8	nF1_H_XMIT3

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U201-52
GTY QUAD 233 I

MGTREFCLK0P_233	N11	ac_pF1R_R0_I 18
MGTREFCLK0N_233	N10	ac_nF1R_R0_I 18
MGTREFCLK1P_233	M13	ac_pF1R_R1_I 21
MGTREFCLK1N_233	M12	ac_nF1R_R1_I 21
MGTYRXP0_233	E2	pF1_I_RECV0
MGTYRXN0_233	E1	nF1_I_RECV0
MGTYTXP0_233	D9	pF1_I_XMIT0
MGTYTXN0_233	D8	nF1_I_XMIT0
MGTYRXP1_233	D4	pF1_I_RECV1
MGTYRXN1_233	D3	nF1_I_RECV1
MGTYTXP1_233	B9	pF1_I_XMIT1
MGTYTXN1_233	B8	nF1_I_XMIT1
MGTYRXP2_233	E6	pF1_I_RECV2
MGTYRXN2_233	E5	nF1_I_RECV2
MGTYTXP2_233	C11	pF1_I_XMIT2
MGTYTXN2_233	C10	nF1_I_XMIT2
MGTYRXP3_233	C6	pF1_I_RECV3
MGTYRXN3_233	C5	nF1_I_RECV3
MGTYTXP3_233	E11	pF1_I_XMIT3
MGTYTXN3_233	E10	nF1_I_XMIT3

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U201-53
GTY QUAD 234 J

MGTREFCLK0P_234	L11	
MGTREFCLK0N_234	L10	
MGTREFCLK1P_234	K13	
MGTREFCLK1N_234	K12	
MGTYRXP0_234	A6	pF1_J_RECV0
MGTYRXN0_234	A5	nF1_J_RECV0
MGTYTXP0_234	A11	pF1_J_XMIT0
MGTYTXN0_234	A10	nF1_J_XMIT0
MGTYRXP1_234	A20	pF1_J_RECV1
MGTYRXN1_234	A19	nF1_J_RECV1
MGTYTXP1_234	B13	pF1_J_XMIT1
MGTYTXN1_234	B12	nF1_J_XMIT1
MGTYRXP2_234	B18	pF1_J_RECV2
MGTYRXN2_234	B17	nF1_J_RECV2
MGTYTXP2_234	A15	pF1_J_XMIT2
MGTYTXN2_234	A14	nF1_J_XMIT2
MGTYRXP3_234	C20	pF1_J_RECV3
MGTYRXN3_234	C19	nF1_J_RECV3
MGTYTXP3_234	C15	pF1_J_XMIT3
MGTYTXN3_234	C14	nF1_J_XMIT3

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pF1_H_RECV0	C1900 0.1 UF 0402	pF2_O_XMIT0	nF2_O_XMIT0
nF1_H_RECV0	C1901 0.1 UF 0402		
pF1_H_RECV1	C1903 0.1 UF 0402	pF2_O_XMIT1	nF2_O_XMIT1
nF1_H_RECV1	C1905 0.1 UF 0402		
pF1_H_RECV2	C1907 0.1 UF 0402	pF2_O_XMIT2	nF2_O_XMIT2
nF1_H_RECV2	C1909 0.1 UF 0402		
pF1_H_RECV3	C1911 0.1 UF 0402	pF2_O_XMIT3	nF2_O_XMIT3
nF1_H_RECV3	C1913 0.1 UF 0402		
pF1_I_RECV0	C1916 0.1 UF 0402	pF2_N_XMIT0	nF2_N_XMIT0
nF1_I_RECV0	C1917 0.1 UF 0402		
pF1_I_RECV1	C1919 0.1 UF 0402	pF2_N_XMIT1	nF2_N_XMIT1
nF1_I_RECV1	C1921 0.1 UF 0402		
pF1_I_RECV2	C1923 0.1 UF 0402	pF2_N_XMIT2	nF2_N_XMIT2
nF1_I_RECV2	C1925 0.1 UF 0402		
pF1_I_RECV3	C1927 0.1 UF 0402	pF2_N_XMIT3	nF2_N_XMIT3
nF1_I_RECV3	C1929 0.1 UF 0402		
pF1_J_RECV0	C1932 0.1 UF 0402	pF2_M_XMIT0	nF2_M_XMIT0
nF1_J_RECV0	C1933 0.1 UF 0402		
pF1_J_RECV1	C1935 0.1 UF 0402	pF2_M_XMIT1	nF2_M_XMIT1
nF1_J_RECV1	C1937 0.1 UF 0402		
pF1_J_RECV2	C1939 0.1 UF 0402	pF2_M_XMIT2	nF2_M_XMIT2
nF1_J_RECV2	C1941 0.1 UF 0402		
pF1_J_RECV3	C1943 0.1 UF 0402	pF2_M_XMIT3	nF2_M_XMIT3
nF1_J_RECV3	C1945 0.1 UF 0402		

pF1_H_XMIT0	0402 0.1 UF C1902	pF2_O_RECV0	nF2_O_RECV0
nF1_H_XMIT0	0402 0.1 UF C1904		
pF1_H_XMIT1	0402 0.1 UF C1906	pF2_O_RECV1	nF2_O_RECV1
nF1_H_XMIT1	0402 0.1 UF C1908		
pF1_H_XMIT2	0402 0.1 UF C1910	pF2_O_RECV2	nF2_O_RECV2
nF1_H_XMIT2	0402 0.1 UF C1912		
pF1_H_XMIT3	0402 0.1 UF C1914	pF2_O_RECV3	nF2_O_RECV3
nF1_H_XMIT3	0402 0.1 UF C1915		
pF1_I_XMIT0	0402 0.1 UF C1918	pF2_N_RECV0	nF2_N_RECV0
nF1_I_XMIT0	0402 0.1 UF C1920		
pF1_I_XMIT1	0402 0.1 UF C1922	pF2_N_RECV1	nF2_N_RECV1
nF1_I_XMIT1	0402 0.1 UF C1924		
pF1_I_XMIT2	0402 0.1 UF C1926	pF2_N_RECV2	nF2_N_RECV2
nF1_I_XMIT2	0402 0.1 UF C1928		
pF1_I_XMIT3	0402 0.1 UF C1930	pF2_N_RECV3	nF2_N_RECV3
nF1_I_XMIT3	0402 0.1 UF C1931		
pF1_J_XMIT0	0402 0.1 UF C1934	pF2_M_RECV0	nF2_M_RECV0
nF1_J_XMIT0	0402 0.1 UF C1936		
pF1_J_XMIT1	0402 0.1 UF C1938	pF2_M_RECV1	nF2_M_RECV1
nF1_J_XMIT1	0402 0.1 UF C1940		
pF1_J_XMIT2	0402 0.1 UF C1942	pF2_M_RECV2	nF2_M_RECV2
nF1_J_XMIT2	0402 0.1 UF C1944		
pF1_J_XMIT3	0402 0.1 UF C1946	pF2_M_RECV3	nF2_M_RECV3
nF1_J_XMIT3	0402 0.1 UF C1947		

U202-42
GTY QUAD 223 O

AV13	MGTREFCLK0P_223	
AV12	MGTREFCLK0N_223	
AU11	MGTREFCLK1P_223	
AU10	MGTREFCLK1N_223	
pF2_O_RECV0	BE2	MGTYRXP0_223
nF2_O_RECV0	BE1	MGTYRXN0_223
pF2_O_XMIT0	BE7	MGTYTXP0_223
nF2_O_XMIT0	BE6	MGTYTXN0_223
pF2_O_RECV1	BD4	MGTYRXP1_223
nF2_O_RECV1	BD3	MGTYRXN1_223
pF2_O_XMIT1	BD9	MGTYTXP1_223
nF2_O_XMIT1	BD8	MGTYTXN1_223
pF2_O_RECV2	BC2	MGTYRXP2_223
nF2_O_RECV2	BC1	MGTYRXN2_223
pF2_O_XMIT2	BC7	MGTYTXP2_223
nF2_O_XMIT2	BC6	MGTYTXN2_223
pF2_O_RECV3	BB4	MGTYRXP3_223
nF2_O_RECV3	BB3	MGTYRXN3_223
pF2_O_XMIT3	BB9	MGTYTXP3_223
nF2_O_XMIT3	BB8	MGTYTXN3_223

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U202-41
GTY QUAD 222 N

ac_pF2R_R0_N 18		
ac_nF2R_R0_N 18	AY13	MGTREFCLK0P_222
	AY12	MGTREFCLK0N_222
ac_pF2R_R1_N 21	AW11	MGTREFCLK1P_222
ac_nF2R_R1_N 21	AW10	MGTREFCLK1N_222
pF2_N_RECV0	BH4	MGTYRXP0_222
nF2_N_RECV0	BH3	MGTYRXN0_222
pF2_N_XMIT0	BG11	MGTYTXP0_222
nF2_N_XMIT0	BG10	MGTYTXN0_222
pF2_N_RECV1	BG2	MGTYRXP1_222
nF2_N_RECV1	BG1	MGTYRXN1_222
pF2_N_XMIT1	BJ11	MGTYTXP1_222
nF2_N_XMIT1	BJ10	MGTYTXN1_222
pF2_N_RECV2	BG6	MGTYRXP2_222
nF2_N_RECV2	BG5	MGTYRXN2_222
pF2_N_XMIT2	BH9	MGTYTXP2_222
nF2_N_XMIT2	BH8	MGTYTXN2_222
pF2_N_RECV3	BF4	MGTYRXP3_222
nF2_N_RECV3	BF3	MGTYRXN3_222
pF2_N_XMIT3	BF9	MGTYTXP3_222
nF2_N_XMIT3	BF8	MGTYTXN3_222

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U202-40
GTY QUAD 221 M

BB13	MGTREFCLK0P_221	
BB12	MGTREFCLK0N_221	
BA11	MGTREFCLK1P_221	
BA10	MGTREFCLK1N_221	
pF2_M_RECV0	BK18	MGTYRXP0_221
nF2_M_RECV0	BK17	MGTYRXN0_221
pF2_M_XMIT0	BL15	MGTYTXP0_221
nF2_M_XMIT0	BL14	MGTYTXN0_221
pF2_M_RECV1	BL20	MGTYRXP1_221
nF2_M_RECV1	BL19	MGTYRXN1_221
pF2_M_XMIT1	BK13	MGTYTXP1_221
nF2_M_XMIT1	BK12	MGTYTXN1_221
pF2_M_RECV2	BL6	MGTYRXP2_221
nF2_M_RECV2	BL5	MGTYRXN2_221
pF2_M_XMIT2	BL11	MGTYTXP2_221
nF2_M_XMIT2	BL10	MGTYTXN2_221
pF2_M_RECV3	BJ6	MGTYRXP3_221
nF2_M_RECV3	BJ5	MGTYRXN3_221
pF2_M_XMIT3	BK9	MGTYTXP3_221
nF2_M_XMIT3	BK8	MGTYTXN3_221

FPGA_VU13P_A2577

APOLLO CM W/ DUAL A2577, MK1

Title: 9.03: F1 QUADS H, I, J TO F2 QUADS O, N, M

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9.04: F1 QUADS D, E, F TO F2 QUADS C, B, A

FPGA#1

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

FPGA#2

U201-47 — GTY QUAD 228 D

MGTREFCLK0P_228	AE11	
MGTREFCLK0N_228	AE10	
MGTREFCLK1P_228	AC11	
MGTREFCLK1N_228	AC10	
MGTYRXP0_228	AE2	pF1_D_RECV0
MGTYRXN0_228	AE1	nF1_D_RECV0
MGTYTXP0_228	AE7	pF1_D_XMIT0
MGTYTXN0_228	AE6	nF1_D_XMIT0
MGTYRXP1_228	AD4	pF1_D_RECV1
MGTYRXN1_228	AD3	nF1_D_RECV1
MGTYTXP1_228	AD9	pF1_D_XMIT1
MGTYTXN1_228	AD8	nF1_D_XMIT1
MGTYRXP2_228	AC2	pF1_D_RECV2
MGTYRXN2_228	AC1	nF1_D_RECV2
MGTYTXP2_228	AC7	pF1_D_XMIT2
MGTYTXN2_228	AC6	nF1_D_XMIT2
MGTYRXP3_228	AB4	pF1_D_RECV3
MGTYRXN3_228	AB3	nF1_D_RECV3
MGTYTXP3_228	AB9	pF1_D_XMIT3
MGTYTXN3_228	AB8	nF1_D_XMIT3

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U201-48 — GTY QUAD 229 E

MGTREFCLK0P_229	AA11	ac_pF1R_R0_E 18
MGTREFCLK0N_229	AA10	ac_nF1R_R0_E 18
MGTREFCLK1P_229	Y13	ac_pF1R_R1_E 21
MGTREFCLK1N_229	Y12	ac_nF1R_R1_E 21
MGTYRXP0_229	AA2	pF1_E_RECV0
MGTYRXN0_229	AA1	nF1_E_RECV0
MGTYTXP0_229	AA7	pF1_E_XMIT0
MGTYTXN0_229	AA6	nF1_E_XMIT0
MGTYRXP1_229	Y4	pF1_E_RECV1
MGTYRXN1_229	Y3	nF1_E_RECV1
MGTYTXP1_229	Y9	pF1_E_XMIT1
MGTYTXN1_229	Y8	nF1_E_XMIT1
MGTYRXP2_229	W2	pF1_E_RECV2
MGTYRXN2_229	W1	nF1_E_RECV2
MGTYTXP2_229	W7	pF1_E_XMIT2
MGTYTXN2_229	W6	nF1_E_XMIT2
MGTYRXP3_229	V4	pF1_E_RECV3
MGTYRXN3_229	V3	nF1_E_RECV3
MGTYTXP3_229	V9	pF1_E_XMIT3
MGTYTXN3_229	V8	nF1_E_XMIT3

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U201-49 — GTY QUAD 230 F

MGTREFCLK0P_230	W11	ac_pF1R_R0_F 18
MGTREFCLK0N_230	W10	ac_nF1R_R0_F 18
MGTREFCLK1P_230	V13	
MGTREFCLK1N_230	V12	
MGTYRXP0_230	U2	pF1_F_RECV0
MGTYRXN0_230	U1	nF1_F_RECV0
MGTYTXP0_230	U7	pF1_F_XMIT0
MGTYTXN0_230	U6	nF1_F_XMIT0
MGTYRXP1_230	T4	pF1_F_RECV1
MGTYRXN1_230	T3	nF1_F_RECV1
MGTYTXP1_230	T9	pF1_F_XMIT1
MGTYTXN1_230	T8	nF1_F_XMIT1
MGTYRXP2_230	R2	pF1_F_RECV2
MGTYRXN2_230	R1	nF1_F_RECV2
MGTYTXP2_230	R7	pF1_F_XMIT2
MGTYTXN2_230	R6	nF1_F_XMIT2
MGTYRXP3_230	P4	pF1_F_RECV3
MGTYRXN3_230	P3	nF1_F_RECV3
MGTYTXP3_230	P9	pF1_F_XMIT3
MGTYTXN3_230	P8	nF1_F_XMIT3

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pF1_D_RECV0	C1948 0.1 UF 0402	pF2_C_XMIT0
nF1_D_RECV0	C1949 0.1 UF 0402	nF2_C_XMIT0
pF1_D_RECV1	C1951 0.1 UF 0402	pF2_C_XMIT1
nF1_D_RECV1	C1953 0.1 UF 0402	nF2_C_XMIT1
pF1_D_RECV2	C1955 0.1 UF 0402	pF2_C_XMIT2
nF1_D_RECV2	C1957 0.1 UF 0402	nF2_C_XMIT2
pF1_D_RECV3	C1959 0.1 UF 0402	pF2_C_XMIT3
nF1_D_RECV3	C1961 0.1 UF 0402	nF2_C_XMIT3

pF1_D_XMIT0	0402 0.1 UF C1950	pF2_C_RECV0
nF1_D_XMIT0	0402 0.1 UF C1952	nF2_C_RECV0
pF1_D_XMIT1	0402 0.1 UF C1954	pF2_C_RECV1
nF1_D_XMIT1	0402 0.1 UF C1956	nF2_C_RECV1
pF1_D_XMIT2	0402 0.1 UF C1958	pF2_C_RECV2
nF1_D_XMIT2	0402 0.1 UF C1960	nF2_C_RECV2
pF1_D_XMIT3	0402 0.1 UF C1962	pF2_C_RECV3
nF1_D_XMIT3	0402 0.1 UF C1963	nF2_C_RECV3

U202-46 — GTY QUAD 227 C

AJ11	MGTREFCLK0P_227	
AJ10	MGTREFCLK0N_227	
AG11	MGTREFCLK1P_227	
AG10	MGTREFCLK1N_227	
pF2_C_RECV0	AJ2	MGTYRXP0_227
nF2_C_RECV0	AJ1	MGTYRXN0_227
pF2_C_XMIT0	AJ7	MGTYTXP0_227
nF2_C_XMIT0	AJ6	MGTYTXN0_227
pF2_C_RECV1	AH4	MGTYRXP1_227
nF2_C_RECV1	AH3	MGTYRXN1_227
pF2_C_XMIT1	AH9	MGTYTXP1_227
nF2_C_XMIT1	AH8	MGTYTXN1_227
pF2_C_RECV2	AG2	MGTYRXP2_227
nF2_C_RECV2	AG1	MGTYRXN2_227
pF2_C_XMIT2	AG7	MGTYTXP2_227
nF2_C_XMIT2	AG6	MGTYTXN2_227
pF2_C_RECV3	AF4	MGTYRXP3_227
nF2_C_RECV3	AF3	MGTYRXN3_227
pF2_C_XMIT3	AF9	MGTYTXP3_227
nF2_C_XMIT3	AF8	MGTYTXN3_227

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U202-45 — GTY QUAD 226 B

ac_pF2R_R0_B 18	AM13	MGTREFCLK0P_226
ac_nF2R_R0_B 18	AM12	MGTREFCLK0N_226
ac_pF2R_R1_B 21	AL11	MGTREFCLK1P_226
ac_nF2R_R1_B 21	AL10	MGTREFCLK1N_226
pF2_B_RECV0	AN2	MGTYRXP0_226
nF2_B_RECV0	AN1	MGTYRXN0_226
pF2_B_XMIT0	AN7	MGTYTXP0_226
nF2_B_XMIT0	AN6	MGTYTXN0_226
pF2_B_RECV1	AM4	MGTYRXP1_226
nF2_B_RECV1	AM3	MGTYRXN1_226
pF2_B_XMIT1	AM9	MGTYTXP1_226
nF2_B_XMIT1	AM8	MGTYTXN1_226
pF2_B_RECV2	AL2	MGTYRXP2_226
nF2_B_RECV2	AL1	MGTYRXN2_226
pF2_B_XMIT2	AL7	MGTYTXP2_226
nF2_B_XMIT2	AL6	MGTYTXN2_226
pF2_B_RECV3	AK4	MGTYRXP3_226
nF2_B_RECV3	AK3	MGTYRXN3_226
pF2_B_XMIT3	AK9	MGTYTXP3_226
nF2_B_XMIT3	AK8	MGTYTXN3_226

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pF1_E_RECV0	C1964 0.1 UF 0402	pF2_B_XMIT0
nF1_E_RECV0	C1965 0.1 UF 0402	nF2_B_XMIT0
pF1_E_RECV1	C1967 0.1 UF 0402	pF2_B_XMIT1
nF1_E_RECV1	C1969 0.1 UF 0402	nF2_B_XMIT1
pF1_E_RECV2	C1971 0.1 UF 0402	pF2_B_XMIT2
nF1_E_RECV2	C1973 0.1 UF 0402	nF2_B_XMIT2
pF1_E_RECV3	C1975 0.1 UF 0402	pF2_B_XMIT3
nF1_E_RECV3	C1977 0.1 UF 0402	nF2_B_XMIT3

pF1_E_XMIT0	0402 0.1 UF C1966	pF2_B_RECV0
nF1_E_XMIT0	0402 0.1 UF C1968	nF2_B_RECV0
pF1_E_XMIT1	0402 0.1 UF C1970	pF2_B_RECV1
nF1_E_XMIT1	0402 0.1 UF C1972	nF2_B_RECV1
pF1_E_XMIT2	0402 0.1 UF C1974	pF2_B_RECV2
nF1_E_XMIT2	0402 0.1 UF C1976	nF2_B_RECV2
pF1_E_XMIT3	0402 0.1 UF C1978	pF2_B_RECV3
nF1_E_XMIT3	0402 0.1 UF C1979	nF2_B_RECV3

U202-44 — GTY QUAD 225 A

AP13	MGTREFCLK0P_225	
AP12	MGTREFCLK0N_225	
AN11	MGTREFCLK1P_225	
AN10	MGTREFCLK1N_225	
pF2_A_RECV0	AU2	MGTYRXP0_225
nF2_A_RECV0	AU1	MGTYRXN0_225
pF2_A_XMIT0	AU7	MGTYTXP0_225
nF2_A_XMIT0	AU6	MGTYTXN0_225
pF2_A_RECV1	AT4	MGTYRXP1_225
nF2_A_RECV1	AT3	MGTYRXN1_225
pF2_A_XMIT1	AT9	MGTYTXP1_225
nF2_A_XMIT1	AT8	MGTYTXN1_225
pF2_A_RECV2	AR2	MGTYRXP2_225
nF2_A_RECV2	AR1	MGTYRXN2_225
pF2_A_XMIT2	AR7	MGTYTXP2_225
nF2_A_XMIT2	AR6	MGTYTXN2_225
pF2_A_RECV3	AP4	MGTYRXP3_225
nF2_A_RECV3	AP3	MGTYRXN3_225
pF2_A_XMIT3	AP9	MGTYTXP3_225
nF2_A_XMIT3	AP8	MGTYTXN3_225

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pF1_F_RECV0	C1980 0.1 UF 0402	pF2_A_XMIT0
nF1_F_RECV0	C1981 0.1 UF 0402	nF2_A_XMIT0
pF1_F_RECV1	C1983 0.1 UF 0402	pF2_A_XMIT1
nF1_F_RECV1	C1985 0.1 UF 0402	nF2_A_XMIT1
pF1_F_RECV2	C1987 0.1 UF 0402	pF2_A_XMIT2
nF1_F_RECV2	C1989 0.1 UF 0402	nF2_A_XMIT2
pF1_F_RECV3	C1991 0.1 UF 0402	pF2_A_XMIT3
nF1_F_RECV3	C1993 0.1 UF 0402	nF2_A_XMIT3

pF1_F_XMIT0	0402 0.1 UF C1982	pF2_A_RECV0
nF1_F_XMIT0	0402 0.1 UF C1984	nF2_A_RECV0
pF1_F_XMIT1	0402 0.1 UF C1986	pF2_A_RECV1
nF1_F_XMIT1	0402 0.1 UF C1988	nF2_A_RECV1
pF1_F_XMIT2	0402 0.1 UF C1990	pF2_A_RECV2
nF1_F_XMIT2	0402 0.1 UF C1992	nF2_A_RECV2
pF1_F_XMIT3	0402 0.1 UF C1994	pF2_A_RECV3
nF1_F_XMIT3	0402 0.1 UF C1995	nF2_A_RECV3

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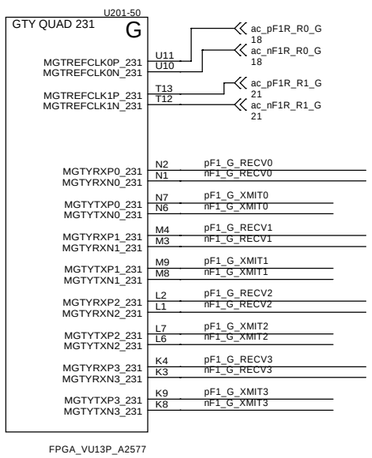
9.05: F1 QUAD G TO F2 QUAD P

FPGA#1



UNUSED CLOCK INPUTS ARE LEFT OPEN.

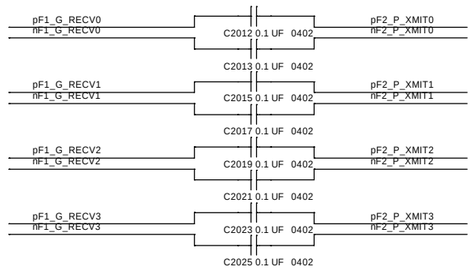
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

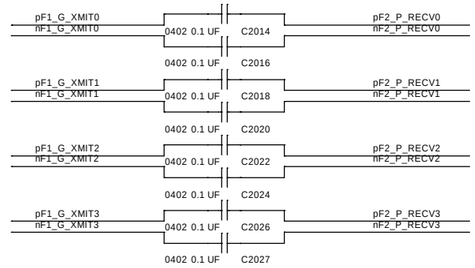
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

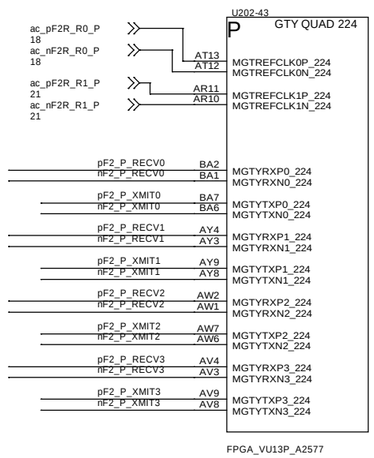
THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.





FPGA#2



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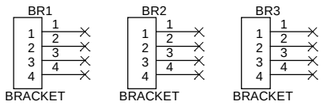
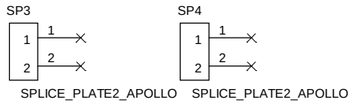
THESE SHAPES DEFINE MECHANICAL OBJECTS
THAT SHOULD BE IN THE BILL OF MATERIALS.

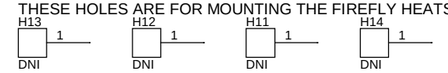


BRACKETS FOR SUPPORTING
A SUB-FRONT PANEL

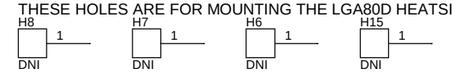
THESE SHAPES DEFINE HOLES AND KEEPOUT
AREAS FOR THE SPLICE PLATES.



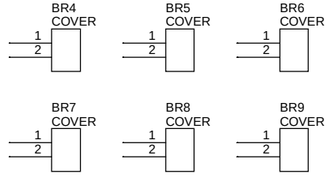
THESE HOLES ARE FOR MOUNTING THE FIREFLY HEATSINK



THESE HOLES ARE FOR MOUNTING THE LGA80D HEATSINK



THESE BRACKETS ARE FOR MOUNTING THE COVERS.
THE BRACKETS ATTACH ON THE BOTTOM SIDE OF
THE BOARD.



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