THIS IS A FLAT SCHEMATIC, NOT A HIERARCHICAL ONE. NETS USE "OFFPAGE CONNECTOR" SYMBOLS TO GO FROM PAGE TO PAGE. ON ANY PAGE, THE NUMBER OF THE CONNECTING PAGE(S) IS SHOWN IN A SMALL NUMBER BELOW THE SIGNAL NAME.

THE SCHEMATIC IS DIVIDED INTO SECTIONS OF RELATED FUNCTIONALITY. THE SECTIONS ARE:
1: NOTES AND BLOCK DIAGRAMS
2: OFF-BOARD SIGNALS (SM AND FRONT PANEL), GLOBAL CLOCKING
3: POWER SOURCES AND CONTROLS
4: I2C CONTROLS
5: FPGA#1 POWER AND SIGNAL (NON-MGT)
6: FPGA#2 POWER AND SIGNAL (NON-MGT)
7: FPGA#1 GTY TRANSCEIVERS (MOSTLY FIREFLY)
8: FPGA#2 GTY TRANSCEIVERS (MOSTLY FIREFLY)
9: BETWEEN-FPGA GTY TRANSCEIVERS

These are some general signal naming conventions:

1) Signals connected to the FPGAs contain either "F1" or "F2".

2) Signals connected to the Service Module contain "SM".

3) Signals connected to the Front Panel contain "FP".

4) Signal names starting with “PG” are “Power Good” signals from power modules.

5) Signal names starting with “EN” are “Enable” signals to turn on power modules.

6) GTY reference clock names indicate FPGA followed by side (F1L, F1R, F2L, F2R), then the reference clock (R0 or R1), finishing with the sequence order (1 thru 7).

7) Power source names start with "V_", then the voltage with the letter "V" as a decimal point. (V_3V3 is a 3.3 volt source)

8) The MCU I/Os are 3.3 volt and the FPGA I/Os are 1.8 volt. Level shifters are used for the conversion. Signal names on the FPGA side are prefaced with "lov" (low voltage) and signals on the MCU side are prefaced with "hiv" (high voltage).

TO DO:

THIS DESIGN INCLUDES FPGA CONFIGURATION MEMORIES. WE SHOULD STILL VERIFY THAT PROGRAMMING AND BOOTING WORK ON CMv1.

VERIFY PROPER RESISTOR VALUES FOR ALL LGA80D CONFIGURATIONS.

APOLLO CM W/ DUAL A2577, MK1

Title: 1.01: NOTES

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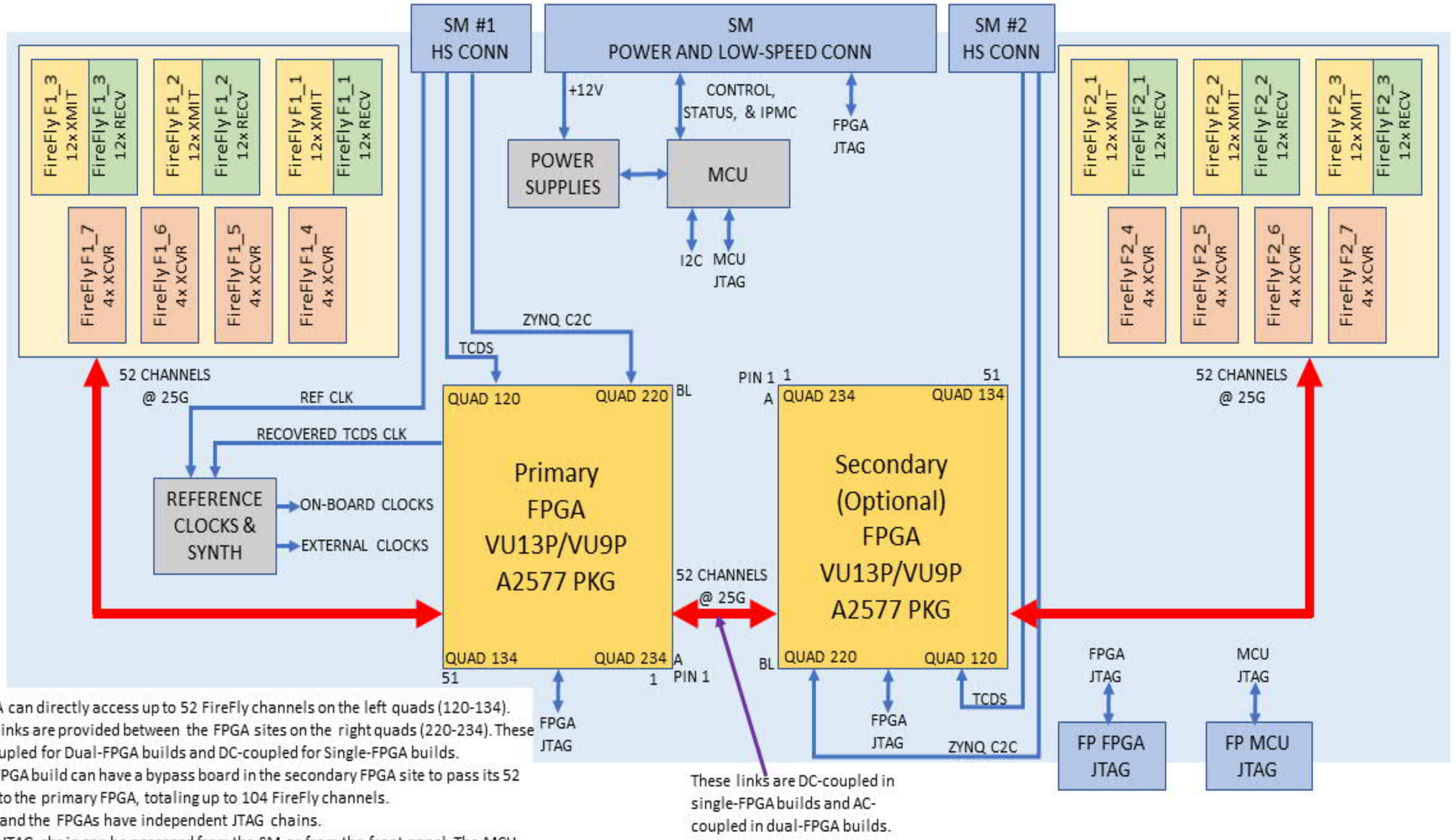
Date: Tuesday, June 15, 2021 | Sheet 1 of 84

Apollo CM Dual A2577: Block Diagram



Notes:

- Each FPGA can directly access up to 52 FireFly channels on the left quads (120-134).
- Up to 52 links are provided between the FPGA sites on the right quads (220-234). These are AC-coupled for Dual-FPGA builds and DC-coupled for Single-FPGA builds.
- A single-FPGA build can have a bypass board in the secondary FPGA site to pass its 52 channels to the primary FPGA, totaling up to 104 FireFly channels.
- The MCU and the FPGAs have independent JTAG chains.
- The FPGA JTAG chain can be accessed from the SM or from the front panel. The MCU JTAG only has front panel access. The MCU code can be changed from an SM serial port.
- The recovered TCDS clock is only available from the primary FPGA.

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.02: BLOCK DIAGRAM		
Size	Document Number: 6089-119	Rev: A
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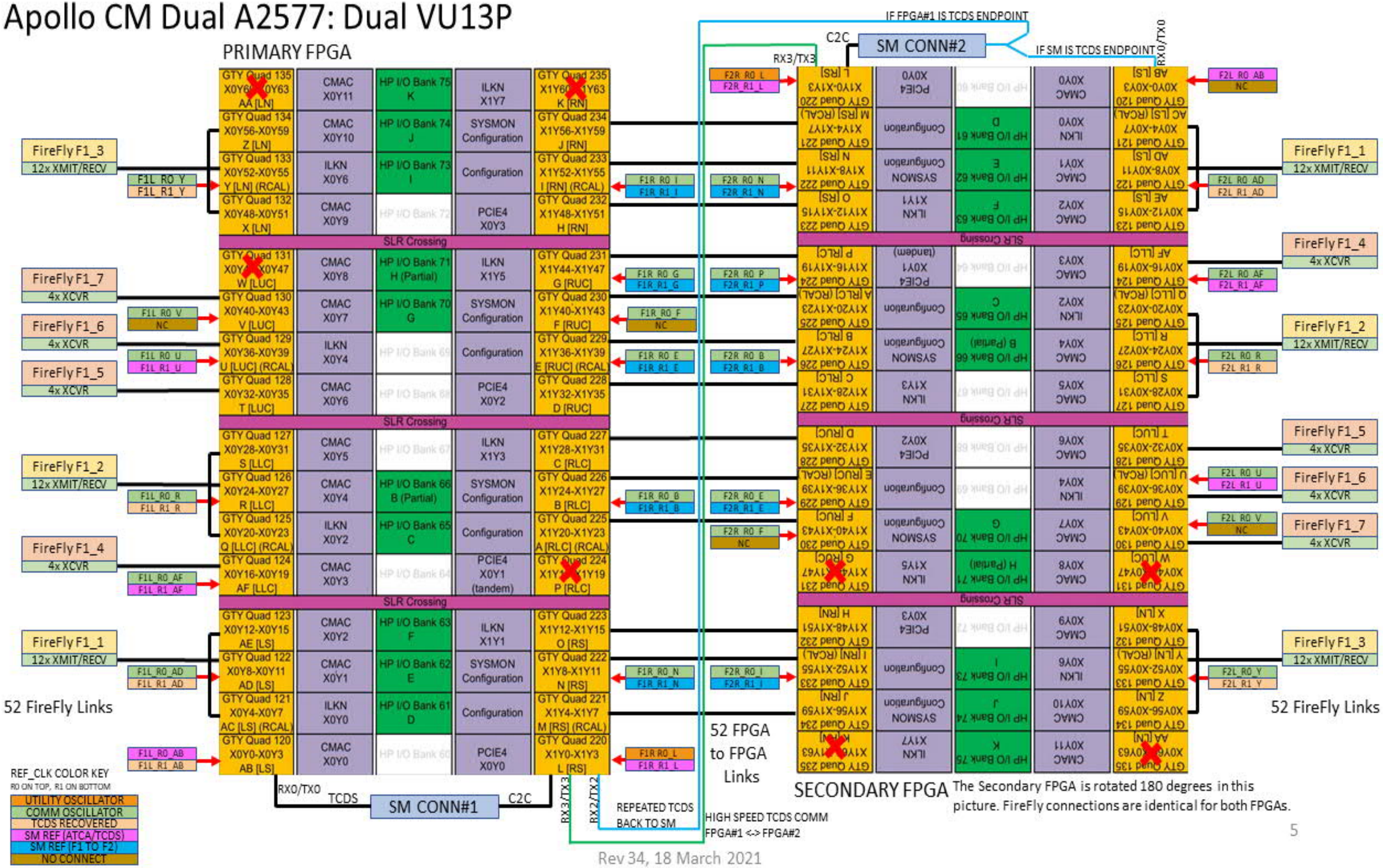
Apollo CM Dual A2577: Dual VU13P



Rev 34, 18 March 2021

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.03: DUAL VU13P		
Size	Document Number: 6089-119	Rev: A
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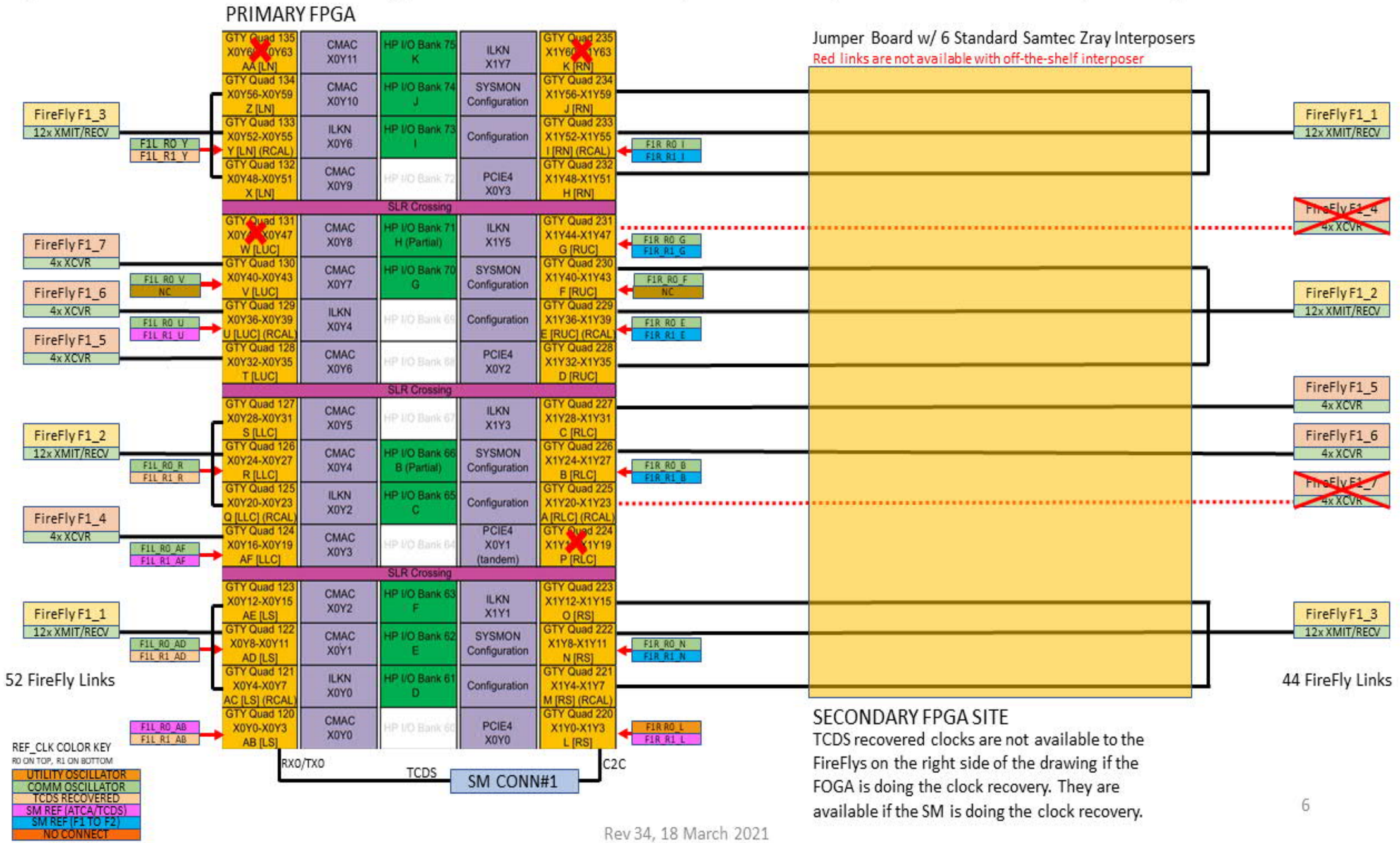
Apollo CM Dual A2577: Single VU13P with Jumper Board (off-the-self Interposers)



SECONDARY FPGA SITE

TCDS recovered clocks are not available to the FireFlys on the right side of the drawing if the FOGA is doing the clock recovery. They are available if the SM is doing the clock recovery.

Rev 34, 18 March 2021

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.04: SINGLE VU13P AND JUMPER		
Size	Document Number: 6089-119	Rev: A
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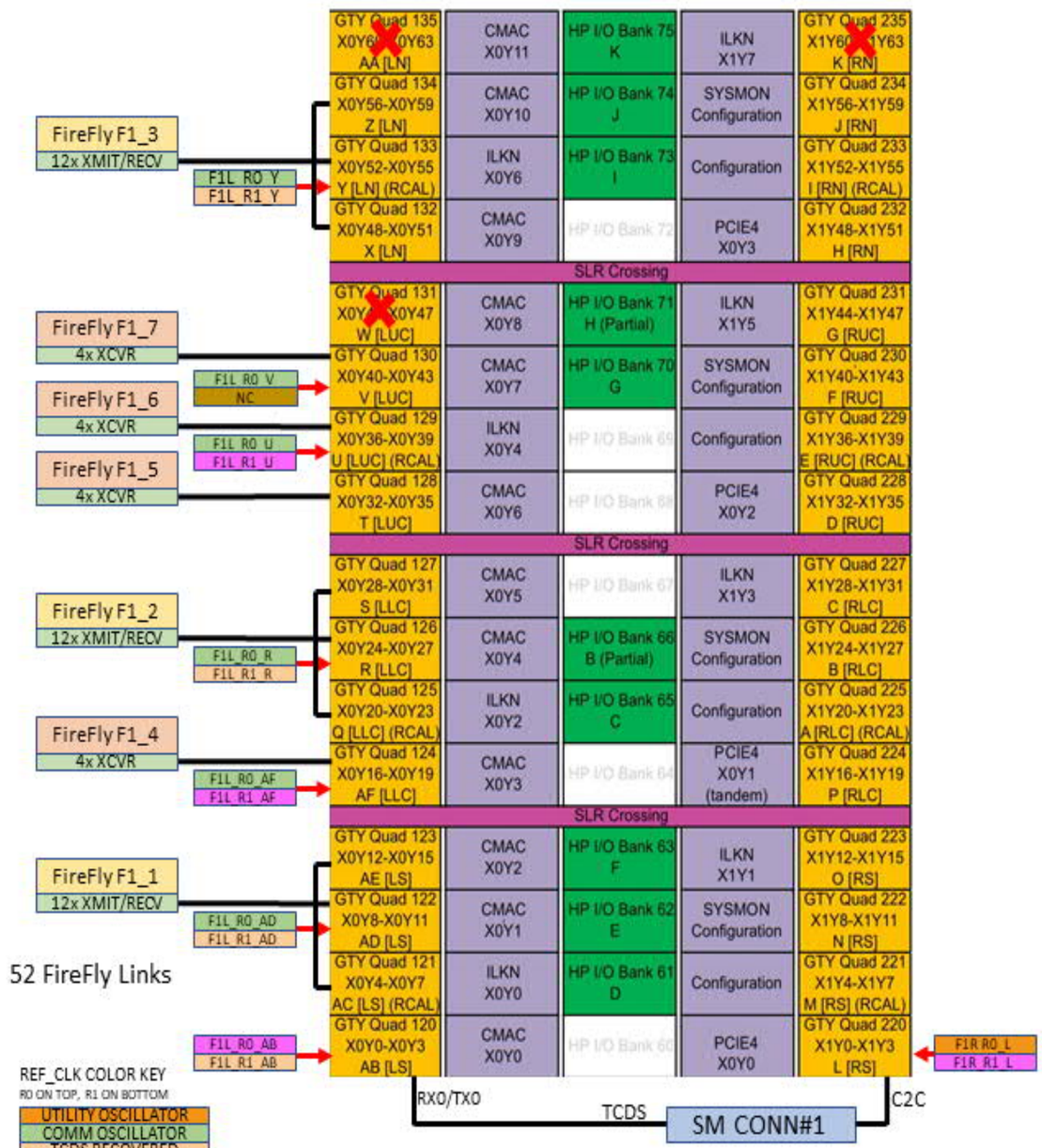
Apollo CM Dual A2577: Single VU13P

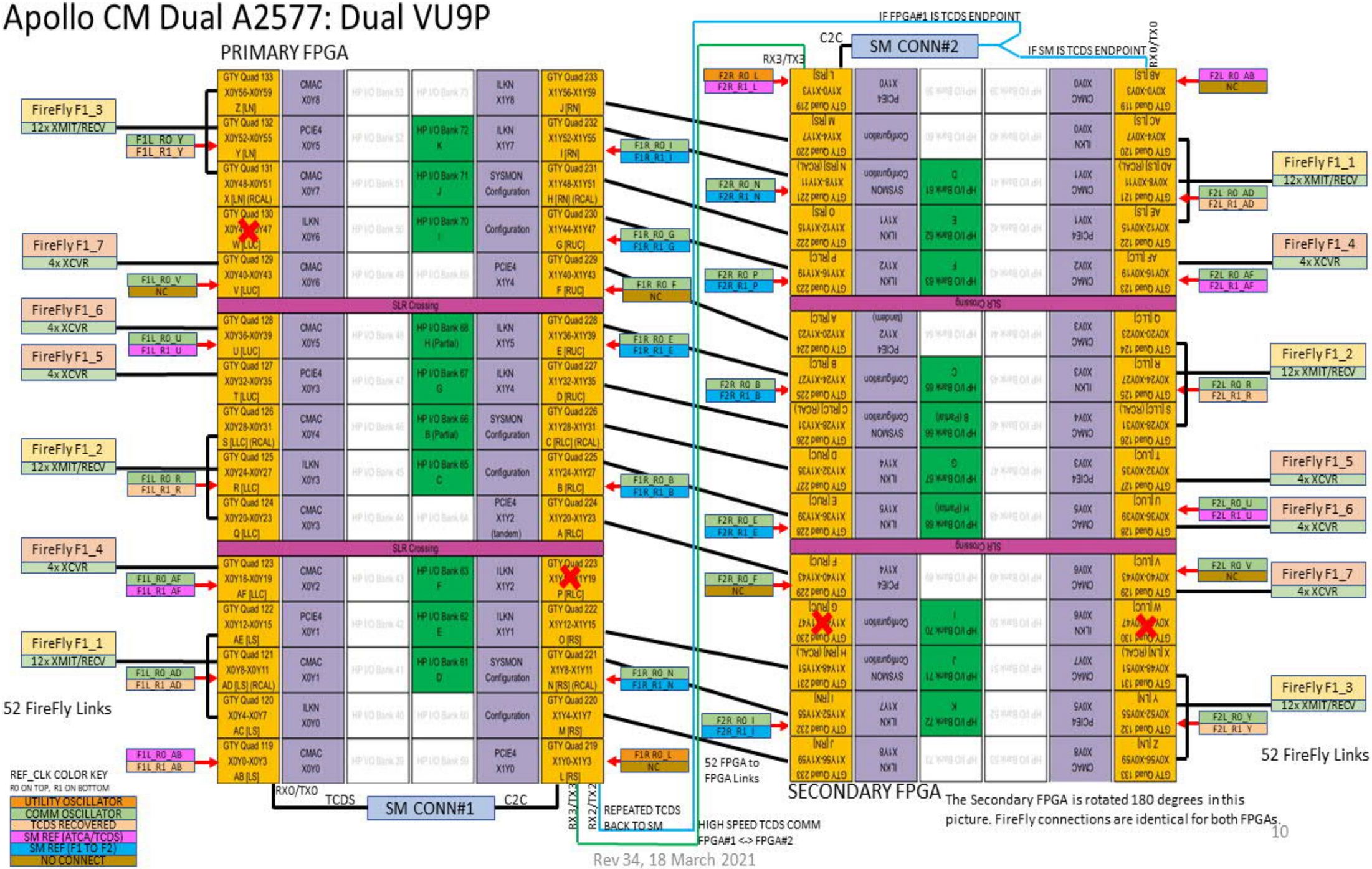


7

Rev 34, 18 March 2021

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.05: SINGLE VU13P		
Size	Document Number: 6089-119	Rev: A
Date: Tuesday, June 15, 2021	Sheet 5 of 84	

Apollo CM Dual A2577: Dual VU9P



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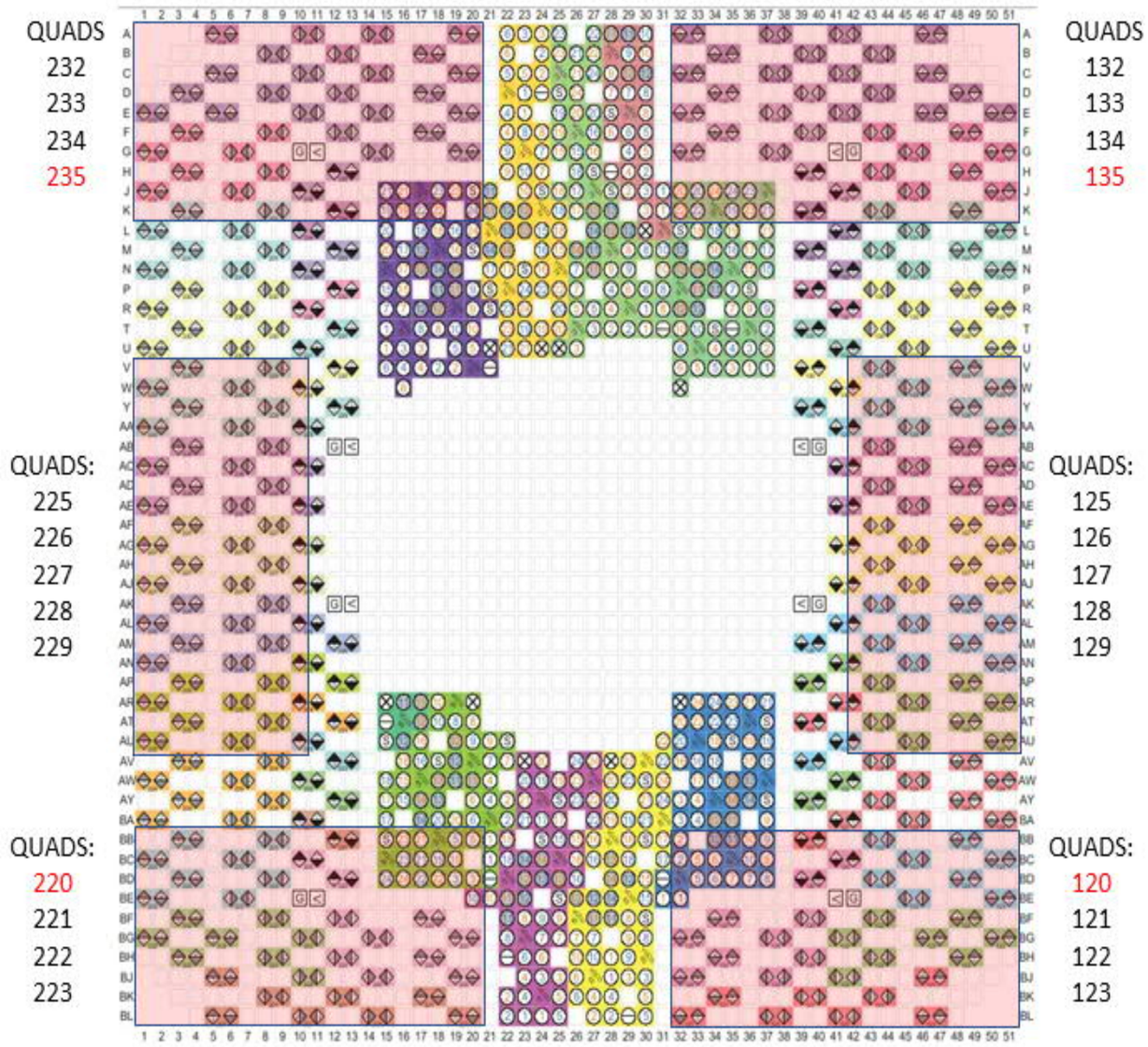
Rev 34, 18 March 2021

APOLLO CM W/ DUAL A2577, MK1			
Title: 1.06: DUAL VU9P			
Size	Document Number: 6089-119		Rev: A
Date: Tuesday, June 15, 2021	Sheet 6 of 84		

Apollo CM Dual A2577: 6 Interposer proof of principle

Diagram shows interposer location and available quads when 6 10x20 interposers are used to connect the jumper board.

Only quads numbered in black will be routed on the initial version. Quads numbered in red, while accessible to the interposers, will not be routed on the jumper board.



APOLLO CM W/ DUAL A2577, MK1		
Title: 1.07: SIX 10X20 INTERPOSERS		
Size	Document Number: 6089-119	Rev: A
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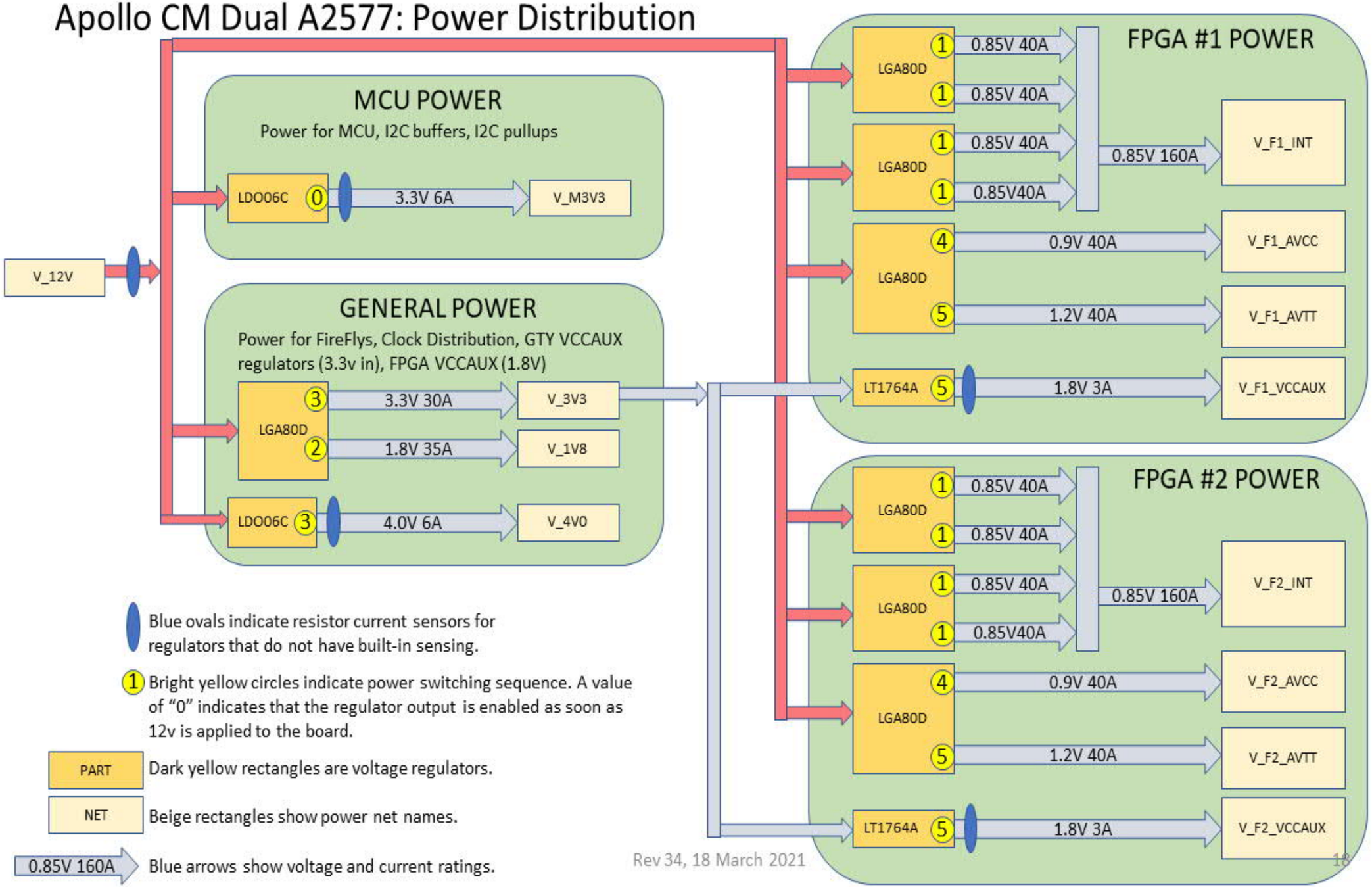
Apollo CM Dual A2577: Power Distribution



Blue ovals indicate resistor current sensors for regulators that do not have built-in sensing.

(1) Bright yellow circles indicate power switching sequence. A value of "0" indicates that the regulator output is enabled as soon as 12v is applied to the board.

PART — Dark yellow rectangles are voltage regulators.

NET — Beige rectangles show power net names.

0.85V 160A — Blue arrows show voltage and current ratings.

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APOLLO CM W/ DUAL A2577, MK1		
Title: 1.08: POWER		
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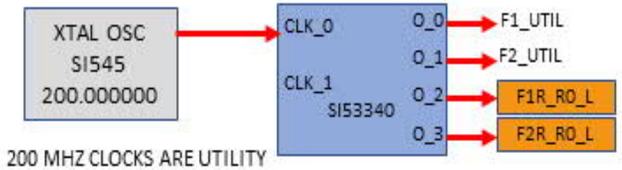
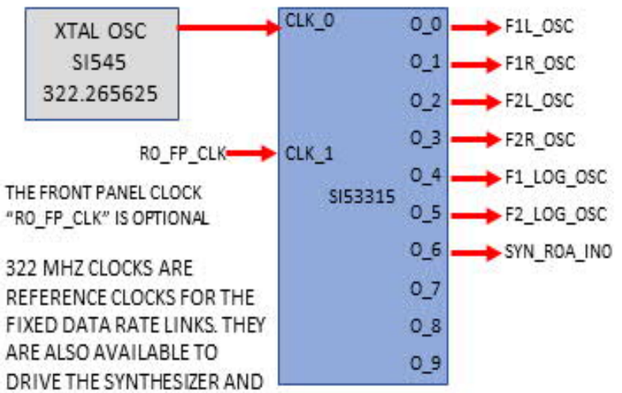
Apollo CM Dual A2577: On-Board Clock Sources

Oscillator Clocks / Reference Clock 0 (R0) Distribution

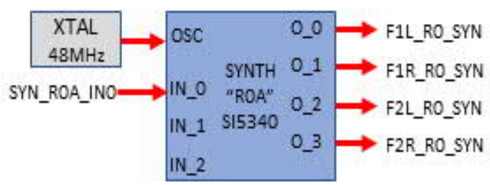


200 MHZ CLOCKS ARE UTILITY CLOCKS FOR THE FPGA LOGIC AND REFERENCE CLOCKS FOR THE SM C2C LINKS

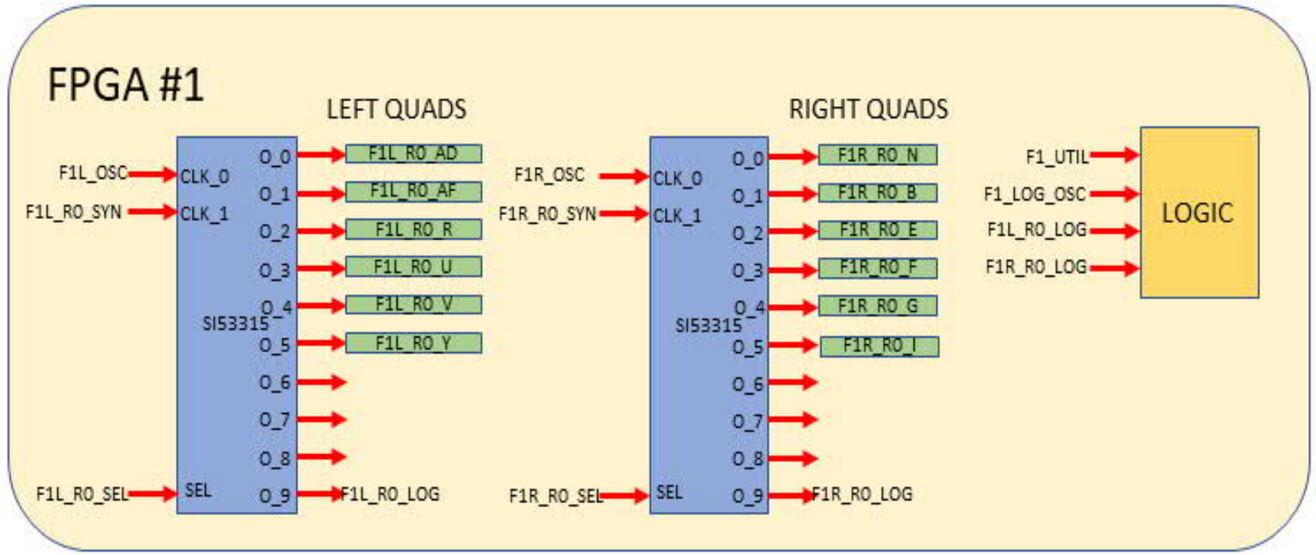


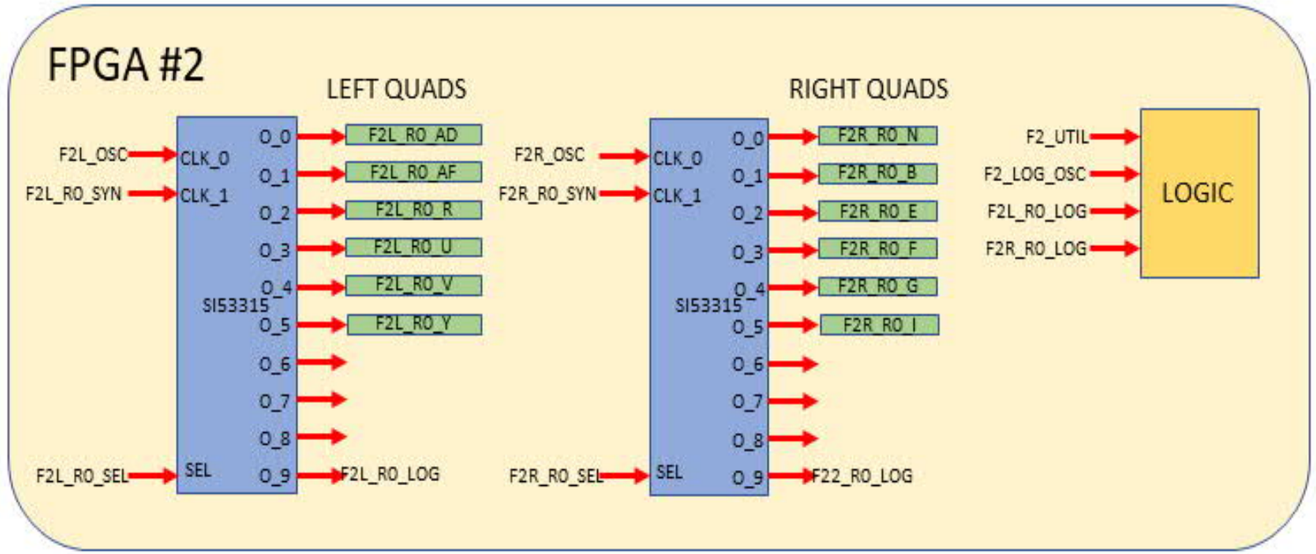
THE FRONT PANEL CLOCK "R0_FP_CLK" IS OPTIONAL

322 MHZ CLOCKS ARE REFERENCE CLOCKS FOR THE FIXED DATA RATE LINKS. THEY ARE ALSO AVAILABLE TO DRIVE THE SYNTHESIZER AND THE FPGA LOGIC.



THE REFERENCE CLOCK 0 SYNTHESIZER CAN BE DRIVEN BY A LOCAL OSCILLATOR OR THE FIXED DATA RATE OSCILLATOR (AND FRONT PANEL INPUT) FANOUT.





APOLLO CM W/ DUAL A2577, MK1		
Title: 1.09: ON-BOARD OSCILLATOR CLOCKS		
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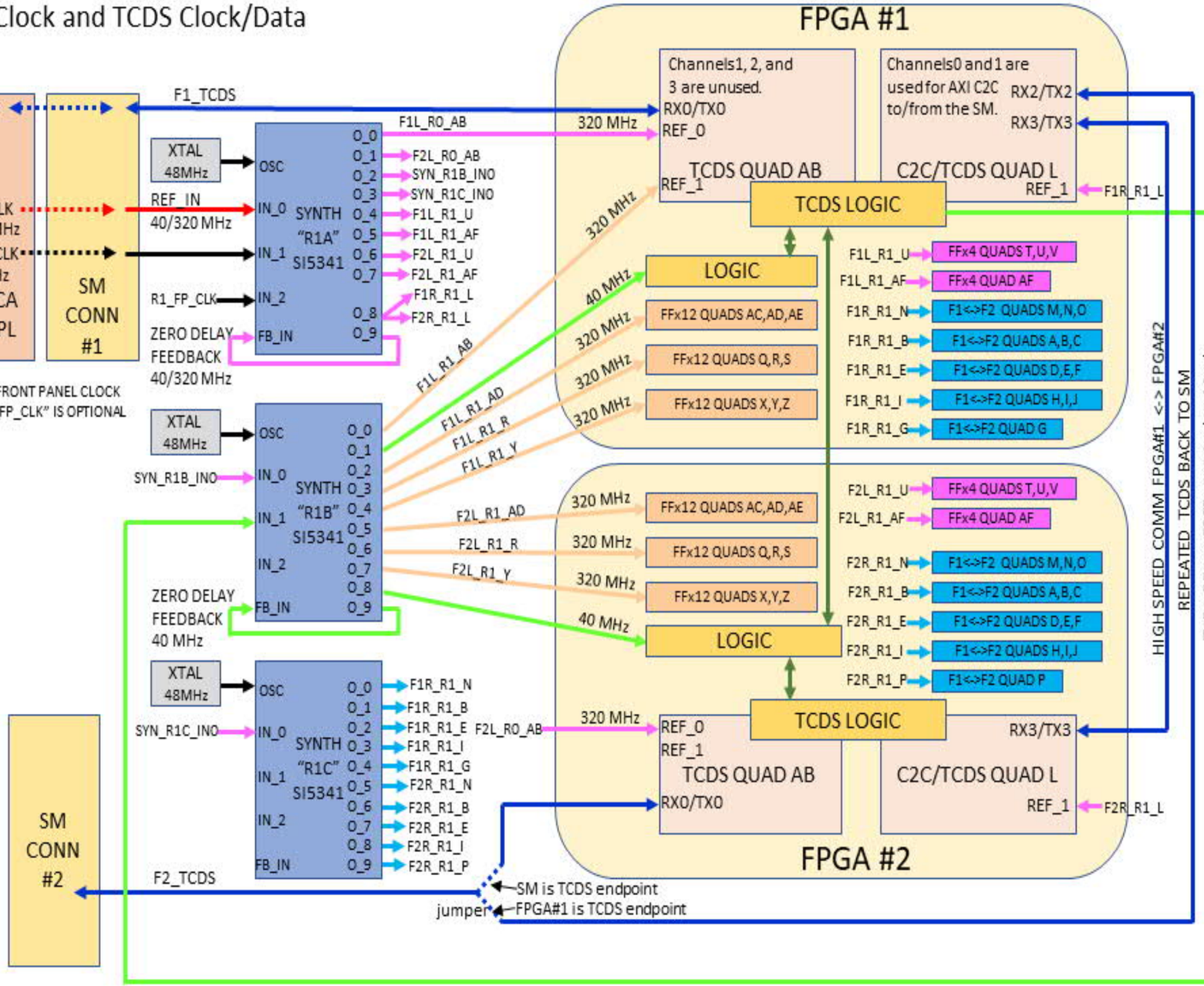
Apollo CM Dual A2577: External Clock Sources

ATCA Clock and TCDS Clock/Data



GBIT CLOCK/DATA COMBINED

LHC REFERENCE CLOCK

If the SM is not the TCDS endpoint, then this is a 320 MHz clock passed directly from the ATCA backplane. If the SM is the TCDS endpoint, then this is the 40 MHz clock recovered from the backplane TCDS signal. In either case, the frequency of this clock changes when the LHC is ramping.

320 MHz REF CLOCK

If the top synthesizer is using the clock on "IN_0", then these 320 MHz clocks all have zero phase offset relative to the incoming LHC REFERENCE CLOCK signal.

40 MHz TCDS RECOVERED CLOCK

This clock is recovered from the incoming TCDS signal. The TCDS LOGIC synchronizes this clock to the bunch crossing. It also adjusts the phase to compensate for distribution delay changes. It will always maintain a fixed phase relative to the bunch crossing. The frequency also varies during filling. This clock is made available to the logic in the FPGAs for synchronizing operations.

320 MHz TCDS RECOVERED CLOCK

These clocks drive the detector-facing FireFly devices, as well as the quad that sends the outgoing TCDS signal back to the SM. They track the TCDS RECOVERED CLOCK.

FPGA TO FPGA R1 CLOCK

These clocks drive the R1 reference for the FPGA quads that connect to the other FPGA. The frequency follows the 320 MHz REF CLOCK.

TTC/TTS DATA/CONTROL

These signals contain clocks/data/control extracted from the incoming TCDS signal (TTC) or destined for the outgoing TCDS signal (TTS). They are used within each FPGA, and can also pass from one FPGA to the other.

OTHER CLOCKS

These include the 40 MHz LHC clock and the outputs of various crystal oscillators. These can be used for testing or for adding flexibility to the synthesizer outputs.

GTY QUADS

FFx12 QUADS	12-lane FireFlys. For the IT-DTC, these will be detector facing.
FFx4 QUADS	4-lane FireFlys.
F1<->F2 QUADS	Connections between the two FPGAs. These will be FireFly links in the case of a single FPGA with jumpers at the secondary FPGA site.
TCDS QUAD	Dedicated for TCDS function.

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APOLLO CM W/ DUAL A2577, MK1		
Title: 1.10: EXTERNAL CLOCKS		
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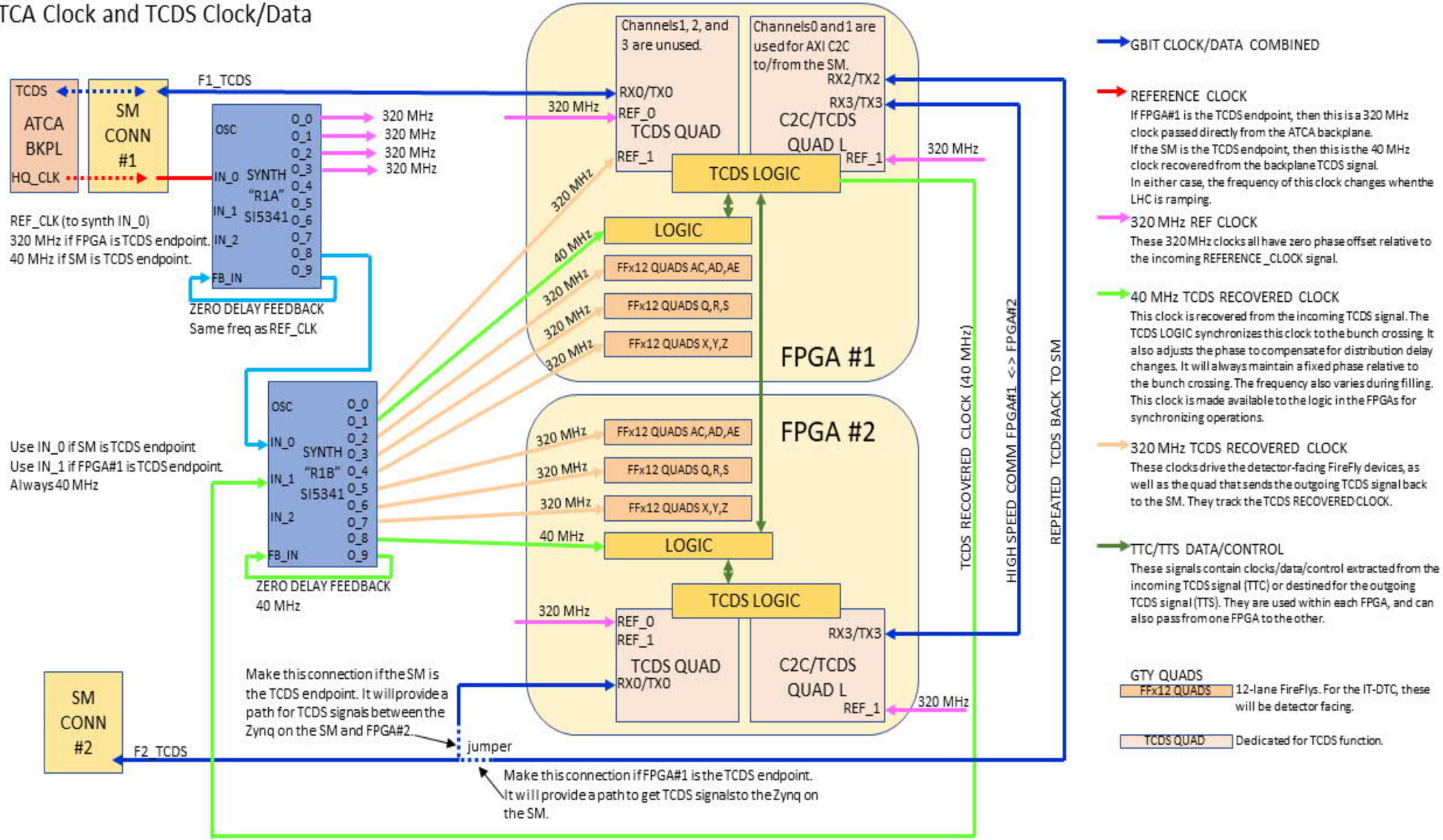
Apollo CM Dual A2577: TCDS Simplified

ATCA Clock and TCDS Clock/Data



GBIT CLOCK/DATA COMBINED

REFERENCE CLOCK
If FPGA#1 is the TCDS endpoint, then this is a 320 MHz clock passed directly from the ATCA backplane.
If the SM is the TCDS endpoint, then this is the 40 MHz clock recovered from the backplane TCDS signal.
In either case, the frequency of this clock changes when the LHC is ramping.

320 MHz REF CLOCK
These 320 MHz clocks all have zero phase offset relative to the incoming REFERENCE_CLOCK signal.

40 MHz TCDS RECOVERED CLOCK
This clock is recovered from the incoming TCDS signal. The TCDS LOGIC synchronizes this clock to the bunch crossing. It also adjusts the phase to compensate for distribution delay changes. It will always maintain a fixed phase relative to the bunch crossing. The frequency also varies during filling. This clock is made available to the logic in the FPGAs for synchronizing operations.

320 MHz TCDS RECOVERED CLOCK
These clocks drive the detector-facing FireFly devices, as well as the quad that sends the outgoing TCDS signal back to the SM. They track the TCDS RECOVERED CLOCK.

TTC/TTS DATA/CONTROL
These signals contain clocks/data/control extracted from the incoming TCDS signal (TTC) or destined for the outgoing TCDS signal (TTS). They are used within each FPGA, and can also pass from one FPGA to the other.

GTY QUADS

FFx12 QUADS	12-lane FireFlys. For the IT-DTC, these will be detector facing.
TCDS QUAD	Dedicated for TCDS function.

Rev 34, 18 March 2021

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.11: TCDS SIMPLIFIED		
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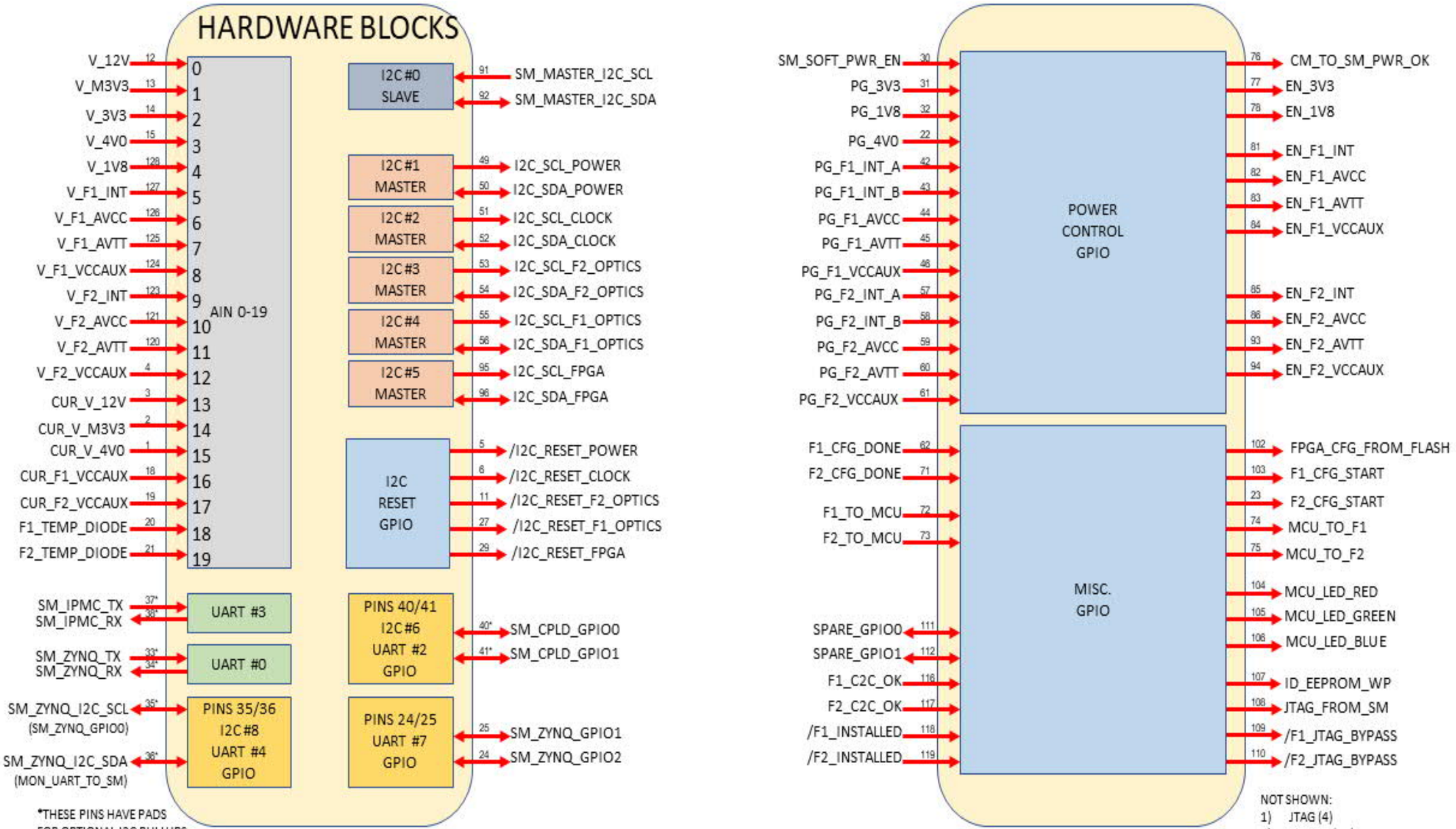
Apollo CM Dual A2577: MCU Connections and Internal Resources

1) Connect a non-SYSMON FPGA I2C block for user use
2) Consider a single I2C for optics



Rev 34, 18 March 2021

APOLLO CM W/ DUAL A2577, MK1		
Title: 1.12: MCU I/O AND INTERNALS		
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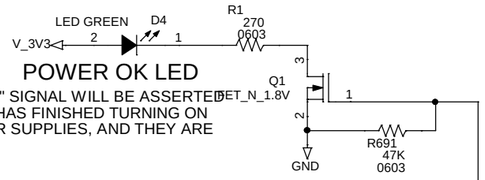
2.01: SM POWER AND CONTROL CONNECTOR

POWER OK LED

THE "POWER_OK" SIGNAL WILL BE ASSERTED WHEN THE MCU HAS FINISHED TURNING ON ALL FPGA POWER SUPPLIES, AND THEY ARE ALL GOOD.



I2C0 IS A SLAVE INTERFACE. IT IS CONNECTED TO THE IPMC ON THE SM.

I2C8 CAN BE A MASTER OR A SLAVE. IT IS USED TO GET MONITORING DATA INTO THE ZYNQ. ON CMv1, THIS IS THE UART#4 PATH. IT IS CONNECTED TO THE ZYNQ ON THE SM.

I2C6 IS AVAILABLE FOR FUTURE USE. IT IS CONNECTED TO THE CPLD ON THE SM. PULLUPS ARE NOT INSTALLED.

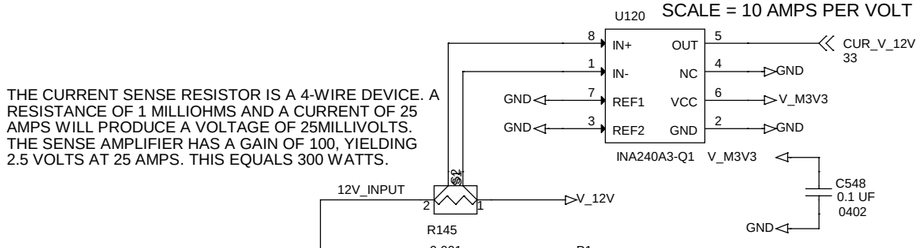
THE I2C7 PINS ARE INITIALLY USED FOR UART#3 CONNECTIONS TO THE IPMC ON THE SM. PULLUPS ARE NOT INSTALLED.

THE I2C9 PINS ARE INITIALLY USED FOR UART#0 CONNECTIONS TO THE ZYNQ ON THE SM.THIS PROVIDES A BOOTLOADER FUNCTION FOR THE MCU. PULLUPS ARE NOT INSTALLED.

IF THE SERVICE BLADE HAS I2C PULLUP RESISTORS, THEN THESE RESISTORS SHOULD BE A LARGE VALUE, JUST SUFFICIENT TO HOLD THE CONTROLLER INPUTS HIGH. IF THE SERVICE BLADE DOES NOT HAVE I2C PULLUP RESISTORS, THEN THESE NEED TO BE AN APPROPRIATE VALUE FOR I2C OPERATION.

V_12V
R = 0.001 OHM
GAIN = 100 V/V
SCALE = 10 AMPS PER VOLT

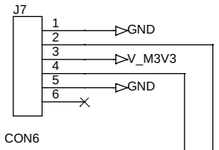
THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 1 MILLIOHMS AND A CURRENT OF 25 AMPS WILL PRODUCE A VOLTAGE OF 25MILLIVOLTS. THE SENSE AMPLIFIER HAS A GAIN OF 100, YIELDING 2.5 VOLTS AT 25 AMPS. THIS EQUALS 300 WATTS.



THIS CONNECTOR IS FOR A STANDALONE USB-TO-UART CABLE. SEE DIGIKEY 768-1015 (FTDI TTL-232R-3V3). THE FACTORY CONNECTOR NEEDS TO BE REPLACED WITH A 6-PIN 2MM PLUG.

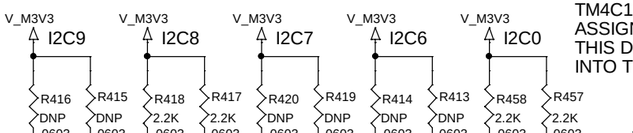
THIS SHOULD ONLY BE USED WHEN THE CM IS NOT MATED TO AN SM.

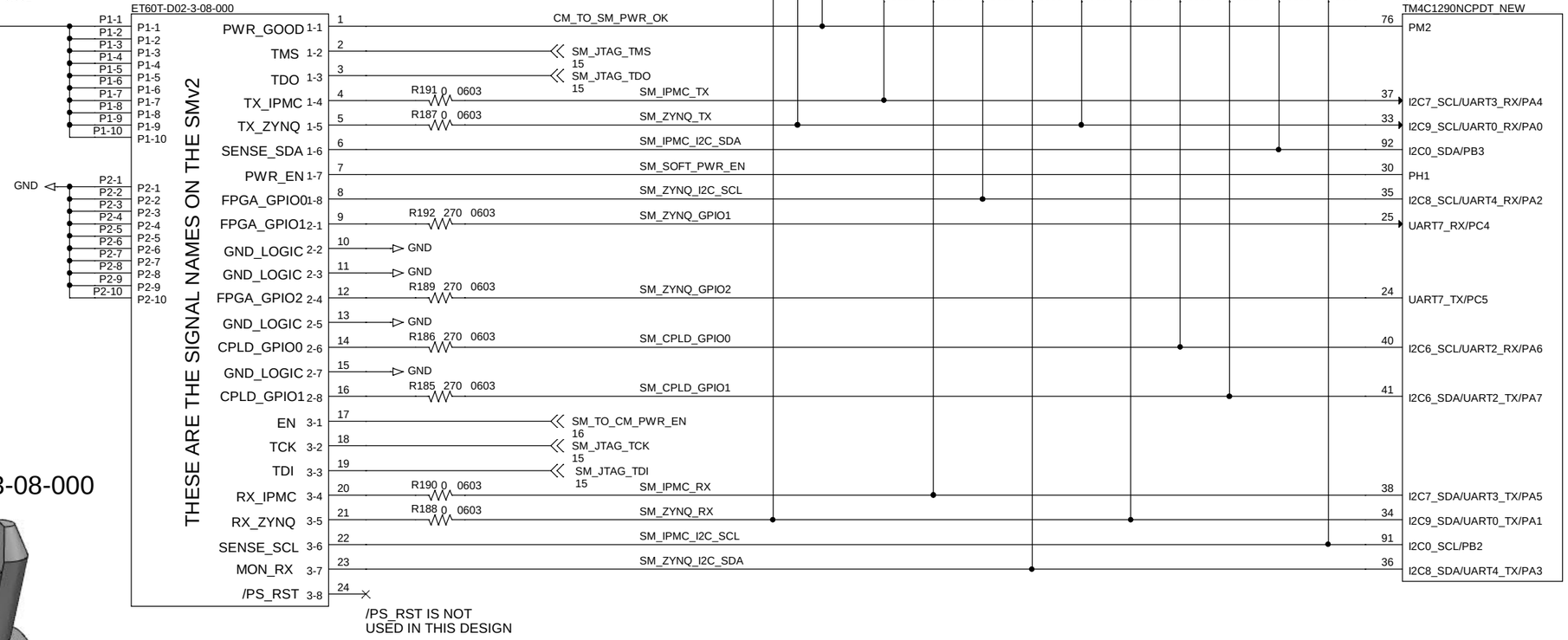
MCU UART



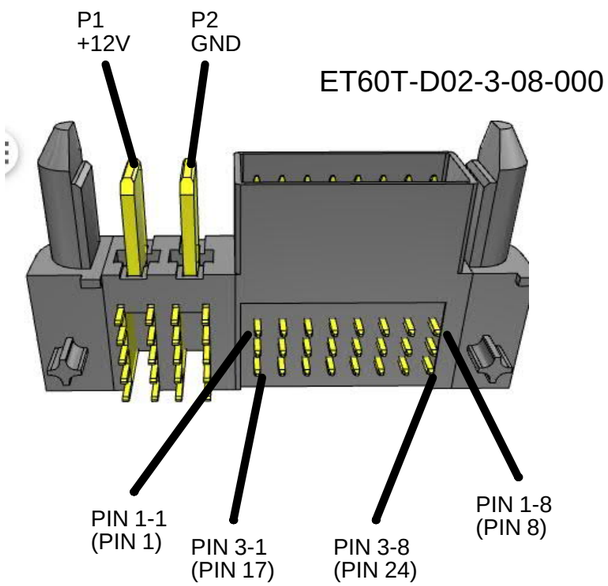
TM4C SLAVE I2C ADDR = 0X40

TM4C1290 I2C ADDRESS:
ASSIGN A SLAVE ADDRESS TO THIS DEVICE BY WRITING A VALUE INTO THE "I2CSOAR" REGISTER.





/PS_RST IS NOT USED IN THIS DESIGN



ZERO-OHM RESISTORS ON PIN 4 AND PIN 20 ARE PLACED ADJACENT TO EACH OTHER. IF "TX" AND "RX" NEED TO BE SWAPPED, REMOVE AND ROTATE THE JUMPERS BY 90 DEGREES.

THE SAME IS TRUE FOR THE RESISTORS ON PIN 5 AND PIN 21.

IN ROW 2, PINS 1, 4, 6, AND 8 ARE "GND" ON SMv1. A CMv2 BOARD MUST BE ABLE TO TOLERATE A HARD GND CONNECTION ON THESE PINS IN CASE IT IS CONNECTED TO AN SMv1.

IF THE MCU IS DRIVING AN OUTPUT HIGH, AND THE SIGNAL IS SHORTED TO GND, A 270 OHM RESISTOR WILL LIMIT THE CURRENT TO 12 MA. THE RESISTOR POWER WILL BE 0.04 WATTS.

APOLLO CM W/ DUAL A2577, MK1

Title: 2.01: SM POWER AND CONTROL CONNECTOR

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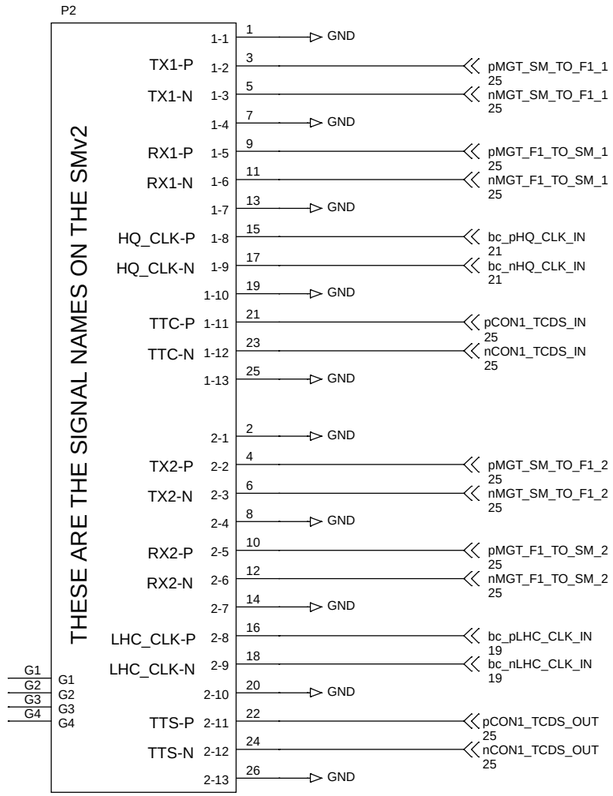
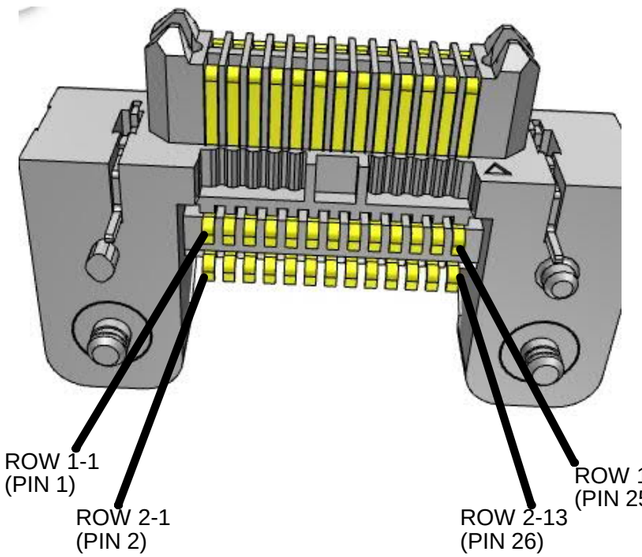
2.02: SM HIGH SPEED CONNECTORS

THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. AC COUPLING CAPACITORS ARE ASSUMED TO BE ON THE SM.

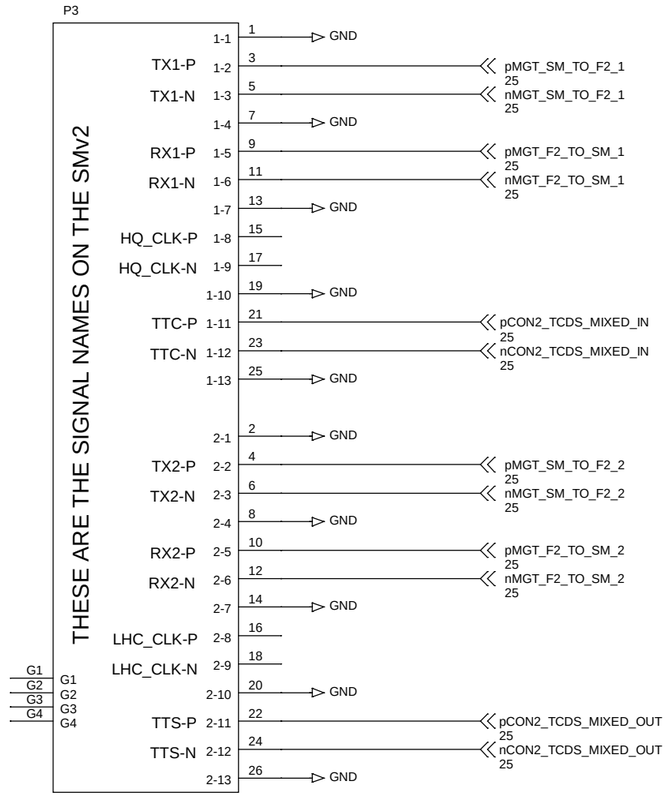
FPGA#1 AND BACKPLANE CLOCK SIGNALS





ERM8-013-01-L-D-RA-DS

FPGA#2 SIGNALS



THE TCDS SIGNALS ON HIGH SPEED CONNECTOR #2 ARE LABELED "MIXED" BECAUSE THEY CAN EITHER BE REGULAR TCDS SIGNALS WHEN THE SM IS THE TCDS ENDPOINT, OR THEY CAN BE REPEATED TCDS SIGNALS WHEN FPGA#1 IS THE TCDS ENDPOINT.

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.02: SM HIGH SPEED CONNECTORS		
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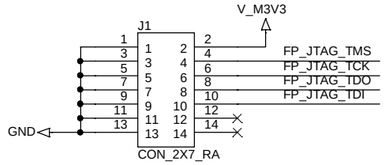
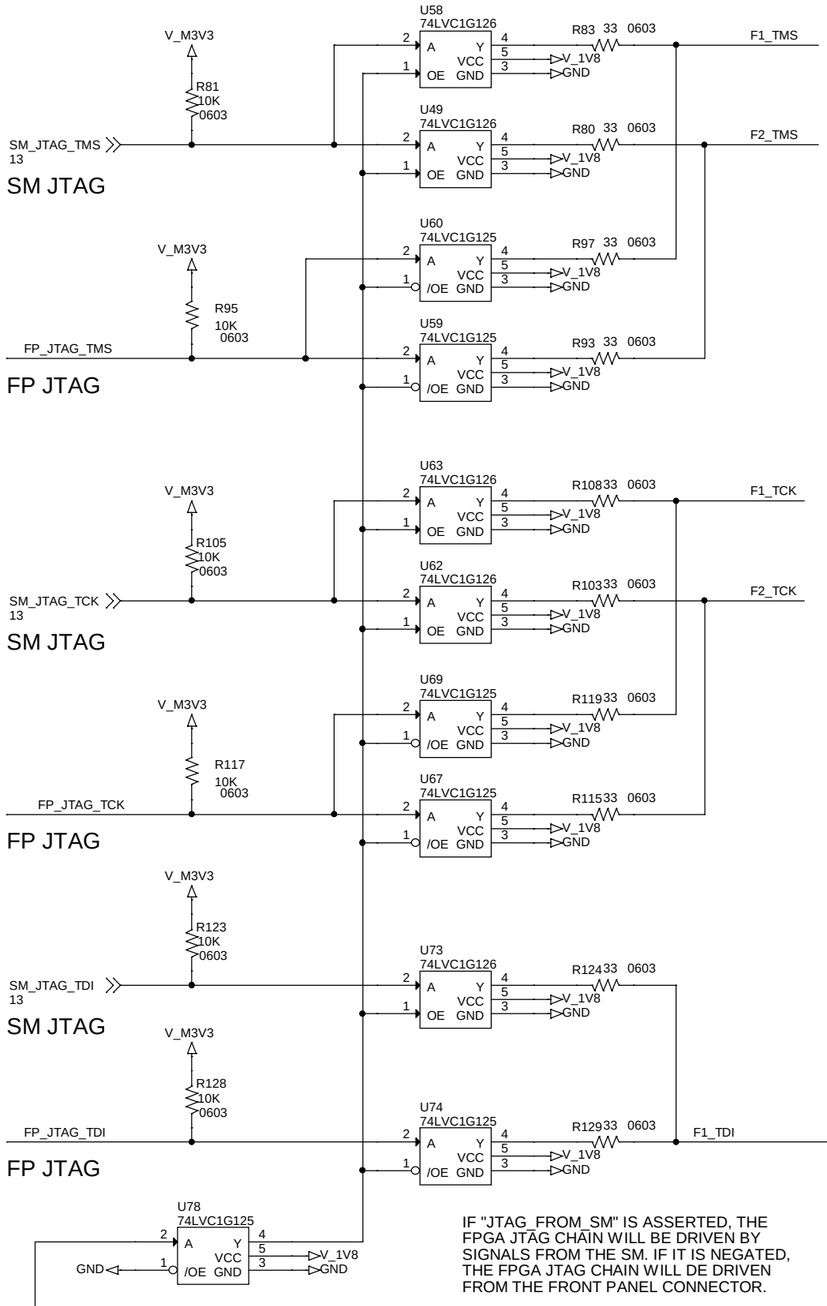
2.03: MCU AND FPGA JTAG

THE FPGA JTAG REFERENCE IS 3.3 VOLTS.

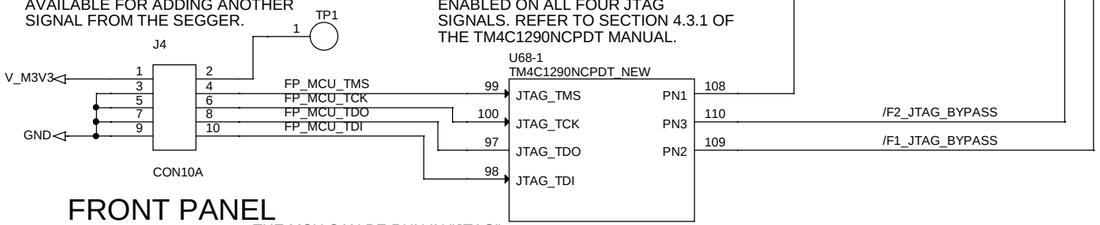


FRONT PANEL
FPGA JTAG



THE TEST POINT ON PIN 2 IS AVAILABLE FOR ADDING ANOTHER SIGNAL FROM THE SEGGER.

THE MCU HAS INTERNAL PULLUPS ENABLED ON ALL FOUR JTAG SIGNALS. REFER TO SECTION 4.3.1 OF THE TM4C1290NCPDT MANUAL.

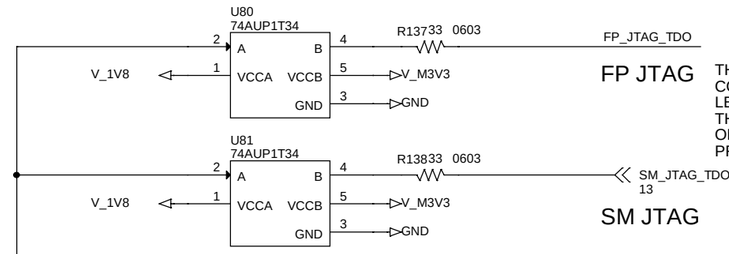


THE MCU CONNECTOR ON THE FRONT PANEL IS A 10-PIN 50-MIL PITCH CONNECTOR. A SEGGER MODEL 8.06.28 "50-MIL 10-PIN PATCH ADAPTER" IS USED AT THE PROGRAMMER.

THE MCU JTAG REFERENCE IS 3.3 VOLTS.

FRONT PANEL
MCU JTAG

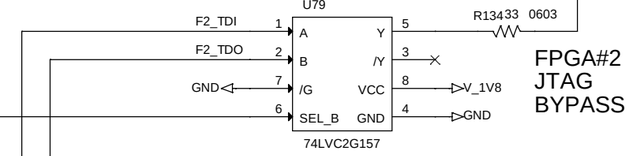
THE MCU CAN BE RUN IN "JTAG" MODE OR "ARM SWD" MODE.



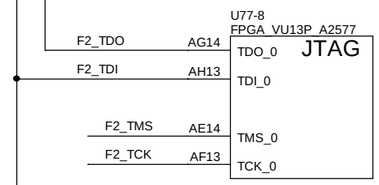
FP JTAG

SM JTAG

THESE VOLTAGE TRANSLATORS CONVERT THE 1.8 VOLT LOGIC LEVEL FROM THE LAST FPGA TO THE 3.3 VOLT LOGIC LEVEL USED ON THE SM OR THE EXTERNAL PROGRAMMER.

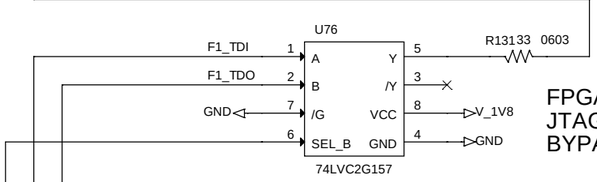


FPGA#2
JTAG
BYPASS

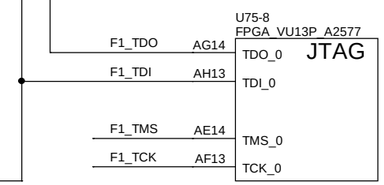


FPGA#2

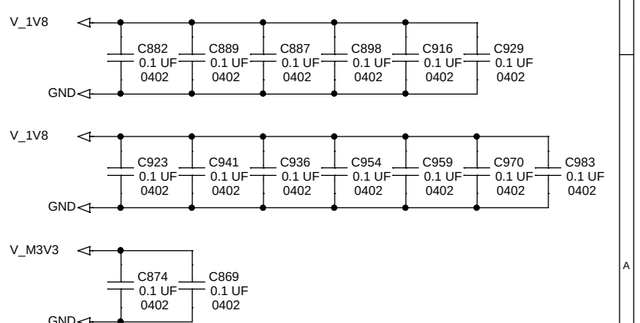
F2_TDI



FPGA#1
JTAG
BYPASS



FPGA#1



APOLLO CM W/ DUAL A2577, MK1		
Title: 2.03: MCU AND FPGA JTAG		
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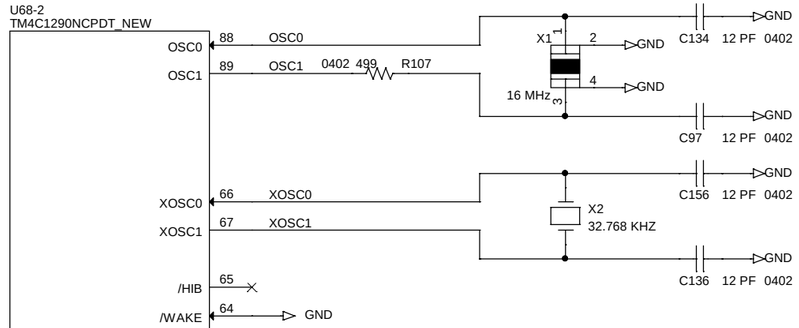
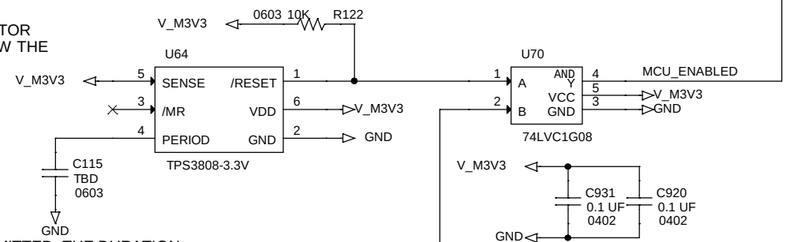
2.04: MCU I/O AND POWER



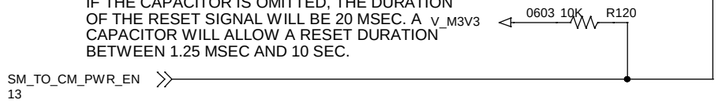
AS PER TABLE 25.7 OF THE TM4C1290 MANUAL, THE UNUSED "/WAKE" PIN GET TIED TO GND AND "/HIB" IS NC.

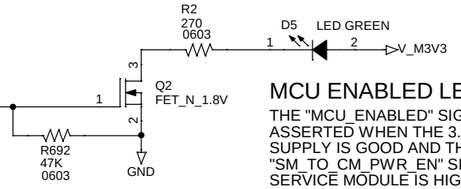
THE ACTIVE-LO "/RESET" INPUT WILL BE ASSERTED WHEN EITHER OF THE FOLLOWING ARE TRUE:
1) POWER HAS JUST BEEN APPLIED
2) THE SERVICE MODULE IS ATTACHED AND IS HOLDING "SM_TO_CM_PWR_EN" LO.

IF THE SERVICE MODULE IS NOT ATTACHED, THE PULLUP RESISTOR ON"SM_TO_CM_PWR_EN" WILL ASSERT THAT SIGNAL AND ALLOW THE BOARD TO POWER UP.



IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

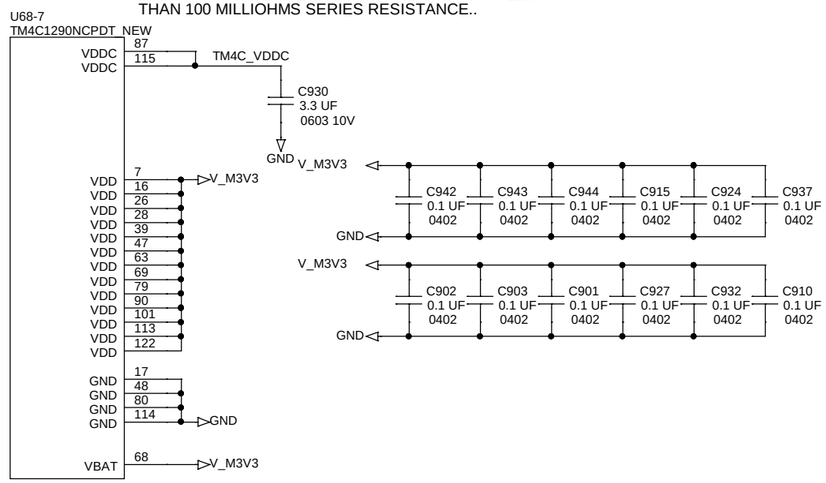




MCU ENABLED LED

THE "MCU_ENABLED" SIGNAL WILL BE ASSERTED WHEN THE 3.3V MANAGEMENT SUPPLY IS GOOD AND THE "SM_TO_CM_PWR_EN" SIGNAL FROM THE SERVICE MODULE IS HIGH.

AS PER TABLE 26.15 OF THE TM4C1290 MANUAL, THE "VDDC" PINS GET TIED TOGETHER AND CONNECTED TO A CAPACITOR BETWEEN 2.5 UF AND 4 UF WITH LESS THAN 100 MILLIOHMS SERIES RESISTANCE..



AS PER TABLE 25.7 OF THE TM4C1290 MANUAL, THE UNUSED "VBAT" PIN GET TIED TO VDD.

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.04: MCU I/O AND POWER		
Size	Document Number: 6089-119	Rev: A
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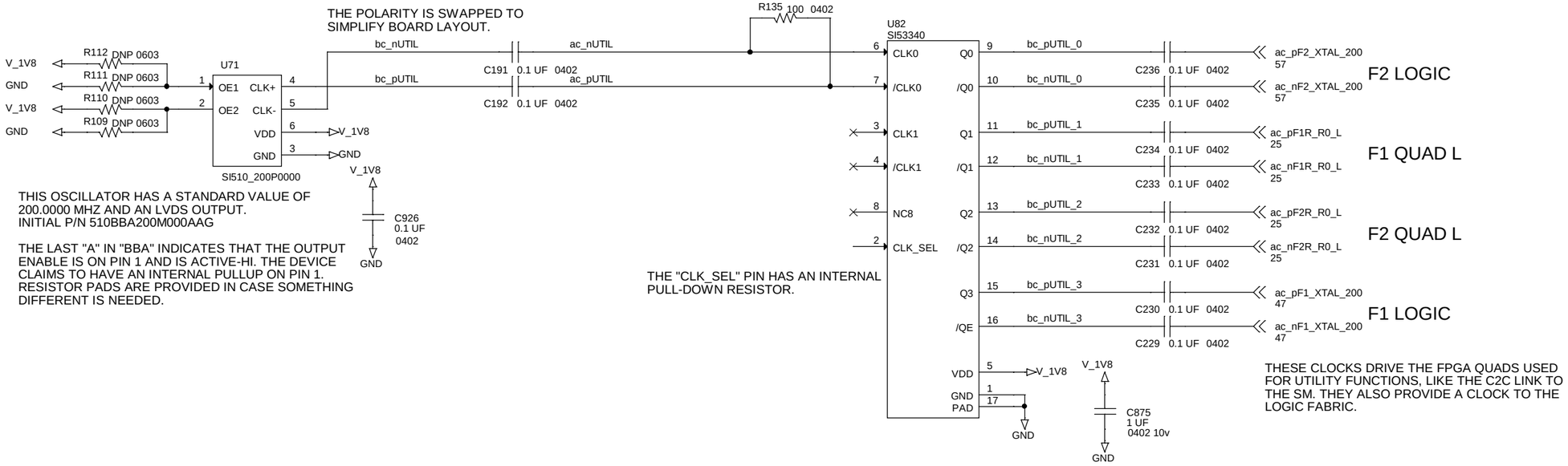
2.05: UTILITY CLOCK



APOLLO CM W/ DUAL A2577, MK1		
Title: 2.05: UTILITY CLOCK		
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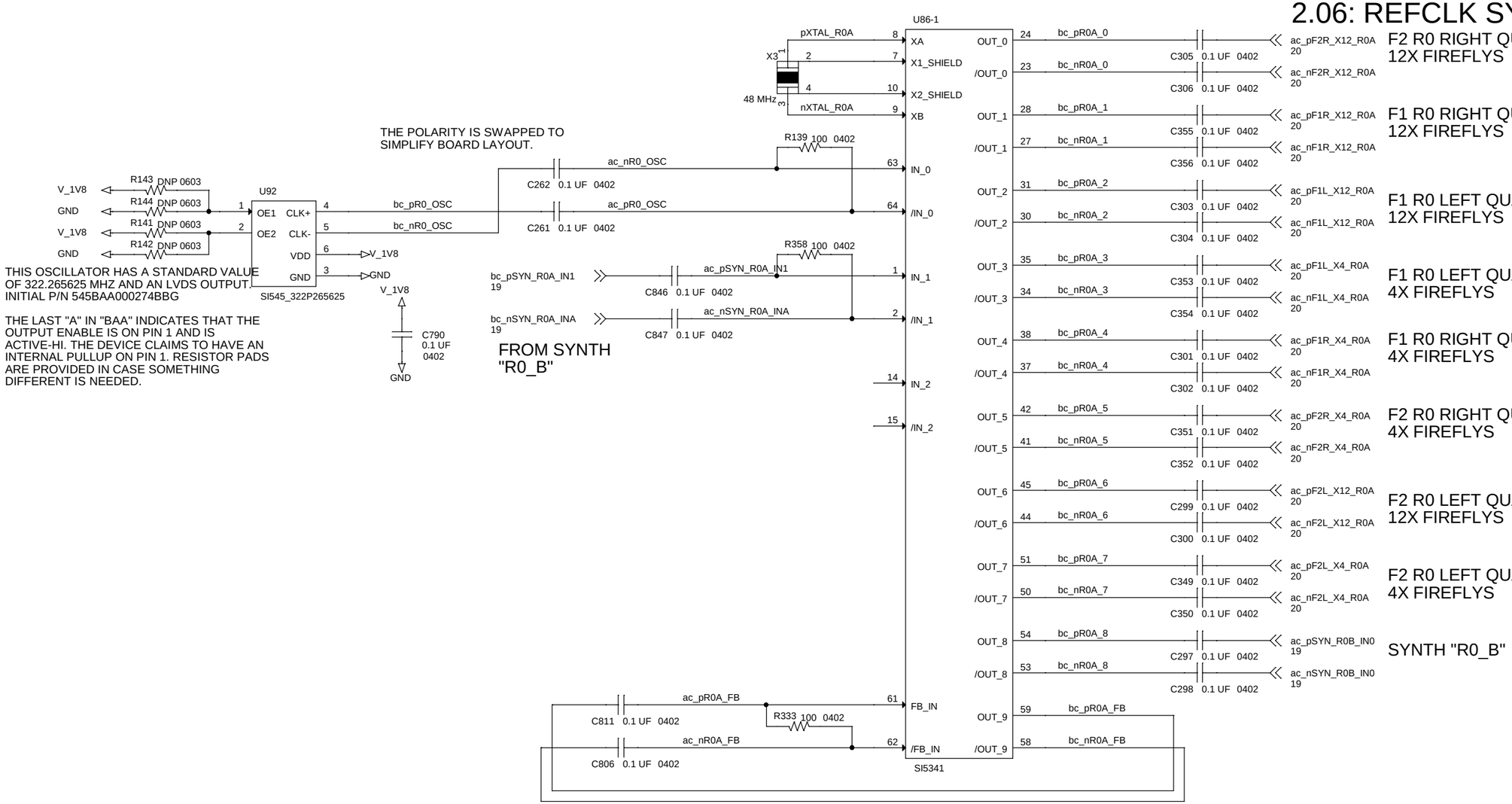
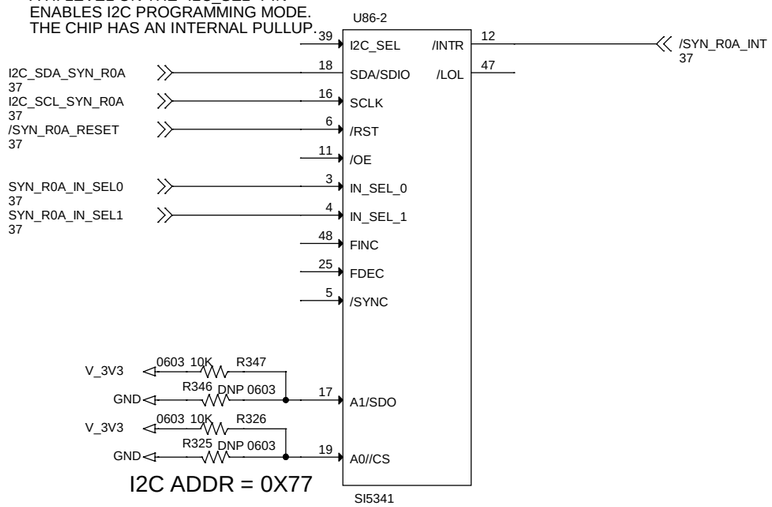
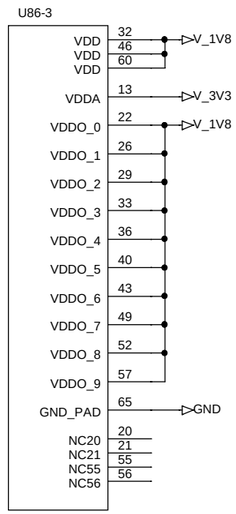
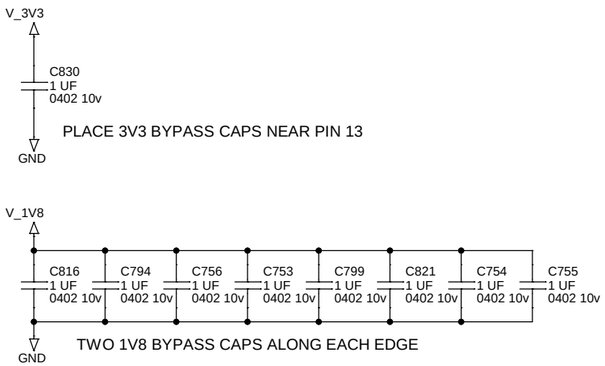
2.06: REFCLK SYNTHESIZER R0A









APOLLO CM W/ DUAL A2577, MK1		
Title: 2.06: REFCLK SYNTHESIZER R0A		
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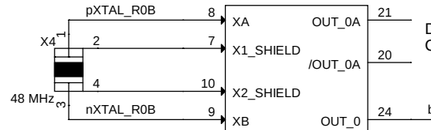
2.07: REFCLK SYNTHESIZER R0B

THE REFERENCE CLOCK 0 SYNTHESIZER “B” CAN BE DRIVEN BY A LOCAL CRYSTAL, THE OUTPUT OF SYNTHESIZER “A”, THE 40 MHZ LHC CLOCK FROM THE BACKPLANE, OR THE OPTIONAL FRONT PANEL CONNECTOR. THE LHC CLOCK WOULD BE USED FOR SYSTEM-WIDE SYNCHRONOUS COMMUNICATION.



DO NOT USE PINS 20,21 TO MAINTAIN COMPATIBILITY WITH THE SI5341.

FROM SYNTH "R0_A"

ac_pSYN_R0B_IN0 18 — R354 100 0402 — 63 IN_0

ac_nSYN_R0B_IN0 18 — 64 /IN_0

LHC_CLK
ALWAYS 40 MHZ

bc_pLHC_CLK_IN 14 — C848 0.1 UF 0402 — ac_pLHC_CLK_IN — R355 100 0402 — 1 IN_1

bc_nLHC_CLK_IN 14 — C849 0.1 UF 0402 — ac_nLHC_CLK_IN — 2 /IN_1

J2
CON5

GND	9	TAB9 GND	5	GND
	8	TAB8 NC4	4	
	7	TAB7 D+	3	bc_pR0_FP_CLK
	6	TAB6 D-	2	bc_nR0_FP_CLK
		VBUS	1	

bc_pR0_FP_CLK — C850 0.1 UF 0402 — ac_pR0_FP_CLK — R356 100 0402 — 14 IN_2

bc_nR0_FP_CLK — C851 0.1 UF 0402 — ac_nR0_FP_CLK — 15 /IN_2

OPTIONAL FRONT PANEL CONNECTOR FOR AN LVDS EXTERNAL CLOCK.

THE CONNECTOR IS A "USB 2.0 MINI-B" STYLE. SEE SHEET 2.07 FOR A PICTURE.

OUT_0	24	bc_pR0B_1 — C313 0.1 UF 0402 — ac_pF2R_X4_R0B 20	F2 R0 RIGHT QUADS 4X FIREFLYS
/OUT_0	23	bc_nR0B_1 — C314 0.1 UF 0402 — ac_nF2R_X4_R0B 20	
OUT_1	28	bc_pR0B_2 — C363 0.1 UF 0402 — ac_pF2R_X12_R0B 20	F2 R0 RIGHT QUADS 12X FIREFLYS
/OUT_1	27	bc_nR0B_2 — C364 0.1 UF 0402 — ac_nF2R_X12_R0B 20	
OUT_2	31	bc_pR0B_3 — C311 0.1 UF 0402 — ac_pF1R_X4_R0B 20	F1 R0 RIGHT QUADS 4X FIREFLYS
/OUT_2	30	bc_nR0B_3 — C312 0.1 UF 0402 — ac_nF1R_X4_R0B 20	
OUT_3	35	bc_pR0B_4 — C361 0.1 UF 0402 — ac_pF1R_X12_R0B 20	F1 R0 RIGHT QUADS 12X FIREFLYS
/OUT_3	34	bc_nR0B_4 — C362 0.1 UF 0402 — ac_nF1R_X12_R0B 20	
OUT_4	38	bc_pR0B_5 — C309 0.1 UF 0402 — ac_pF1L_X4_R0B 20	F1 R0 LEFT QUADS 4X FIREFLYS
/OUT_4	37	bc_nR0B_5 — C310 0.1 UF 0402 — ac_nF1L_X4_R0B 20	
OUT_5	42	bc_pR0B_6 — C359 0.1 UF 0402 — ac_pF1L_X12_R0B 20	F1 R0 LEFT QUADS 12X FIREFLYS
/OUT_5	41	bc_nR0B_6 — C360 0.1 UF 0402 — ac_nF1L_X12_R0B 20	
OUT_6	45	bc_pR0B_7 — C307 0.1 UF 0402 — ac_pF2L_X12_R0B 20	F2 R0 LEFT QUADS 12X FIREFLYS
/OUT_6	44	bc_nR0B_7 — C308 0.1 UF 0402 — ac_nF2L_X12_R0B 20	
OUT_7	51	bc_pR0B_8 — C357 0.1 UF 0402 — ac_pF2L_X4_R0B 20	F2 R0 LEFT QUADS 4X FIREFLYS
/OUT_7	50	bc_nR0B_8 — C358 0.1 UF 0402 — ac_nF2L_X4_R0B 20	
OUT_8	54	bc_pSYN_R0A_IN1 18	TO SYNTH "R0_A"
/OUT_8	53	bc_nSYN_R0A_INA 18	
OUT_9	56	DO NOT USE PINS 55,56 TO MAINTAIN COMPATIBILITY WITH THE SI5341.	
/OUT_9	55		

ac_pR0B_FB — C812 0.1 UF 0402 — R334 100 0402 — 61 FB_IN — OUT_9A 59 bc_pR0B_FB

ac_nR0B_FB — C807 0.1 UF 0402 — 62 /FB_IN — /OUT_9A 58 bc_nR0B_FB

SI5395

U87-3

VDD	32	V_1V8
VDD	46	
VDD	60	
VDDA	13	V_3V3
VDDO_0	22	V_1V8
VDDO_1	26	
VDDO_2	29	
VDDO_3	33	
VDDO_4	36	
VDDO_5	40	
VDDO_6	43	
VDDO_7	49	
VDDO_8	52	
VDDO_9	57	
GND_PAD	65	GND

SI5395

V_1V8: C817 1 UF 0402 10v, C795 1 UF 0402 10v, C757 1 UF 0402 10v, C758 1 UF 0402 10v, C800 1 UF 0402 10v, C822 1 UF 0402 10v, C760 1 UF 0402 10v, C759 1 UF 0402 10v — GND

V_3V3: C831 1 UF 0402 10v — GND

A HI LEVEL ON THE "I2C_SEL" PIN ENABLES I2C PROGRAMMING MODE. THE CHIP HAS AN INTERNAL PULLUP.

A LOW LEVEL ON THE "/OE" PIN WILL ENABLE THE OUTPUTS. THE CHIP HAS AN INTERNAL PULLDOWN.

THE "FINC" AND "FDEC" PINS HAVE INTERNAL PULLDOWNS AND CAN BE LEFT UNCONNECTED.

U87-2

	39	I2C_SEL	/INTR	12 — /SYN_R0B_INT 37
I2C_SDA_SYN_R0B 37	18	SDA/SDIO	/LOL	47
I2C_SCL_SYN_R0B 37	16	SCLK		
/SYN_R0B_RESET 37	6	/RST		
	11	/OE		
SYN_R0B_IN_SEL0 37	3	IN_SEL_0		
SYN_R0B_IN_SEL1 37	4	IN_SEL_1		
	48	FINC		
	25	FDEC		
	5	RSVD		
V_3V3 — 0603 10K R349; GND — R348 DNP 0603	17	A1/SDO		
V_3V3 — 0603 10K R328; GND — R327 DNP 0603	19	A0//CS		

I2C ADDR = 0X77 SI5395

REFCLK R0B SYNTHESIZER

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.07: REFCLK SYNTHESIZER R0B		
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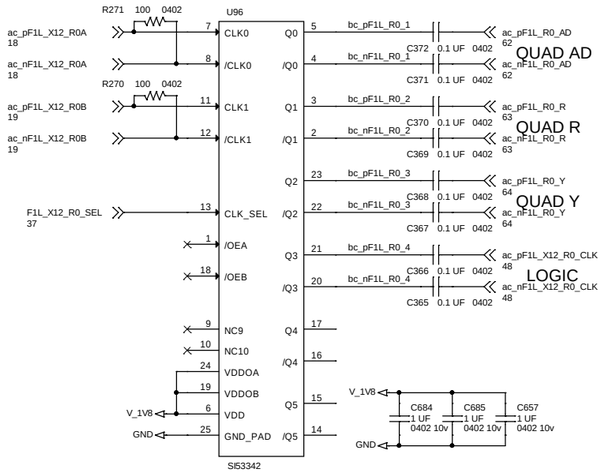
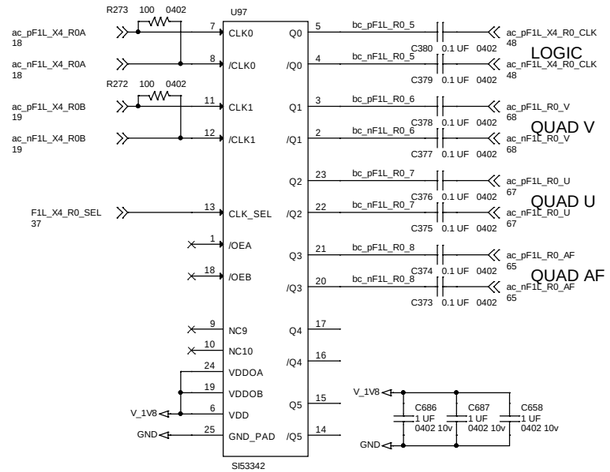
2.08: REFCK_R0_FANOUT

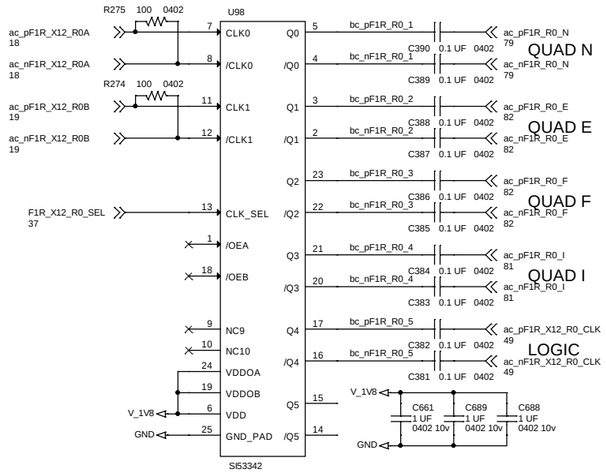
FPGA#1 LEFT



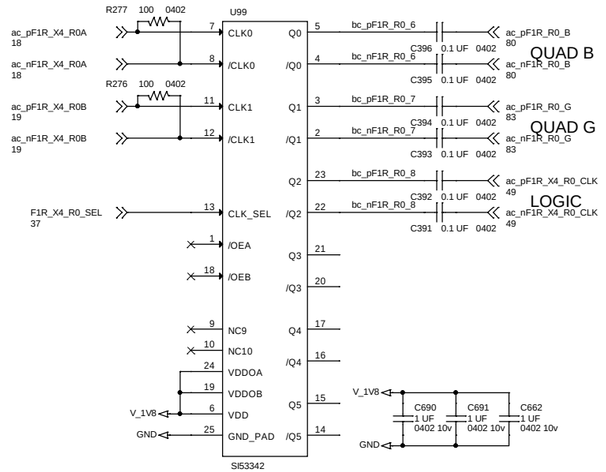
FPGA#1 LEFT



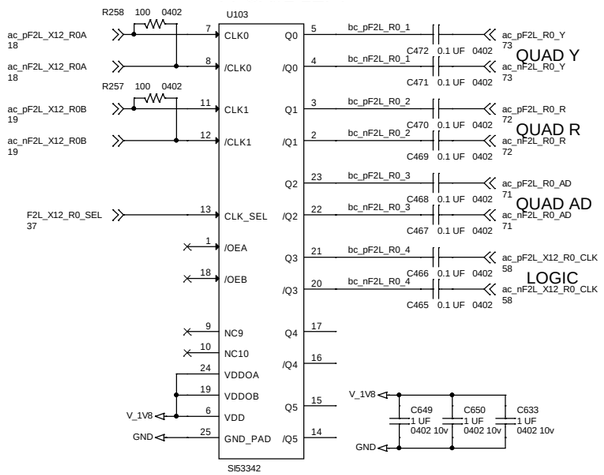
FPGA#1 RIGHT



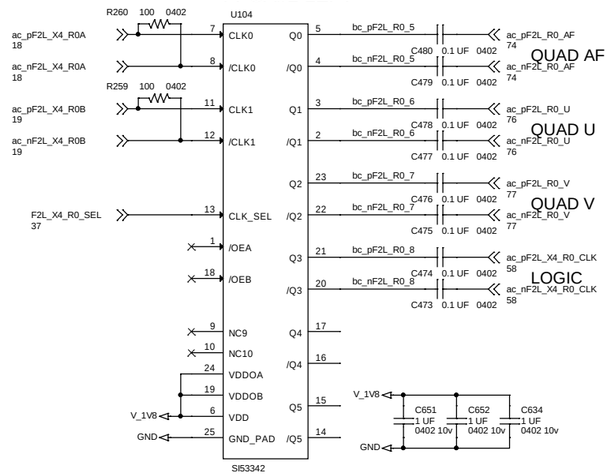
FPGA#1 RIGHT



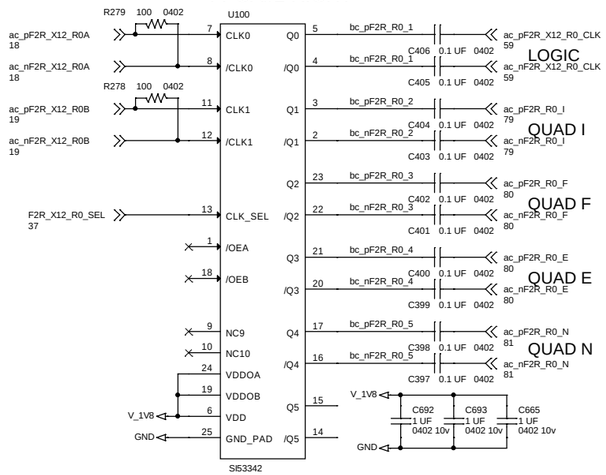
FPGA#2 LEFT



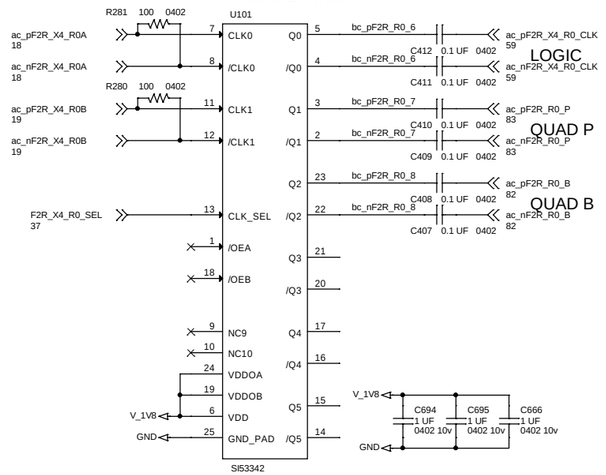
FPGA#2 LEFT



FPGA#2 RIGHT



FPGA#2 RIGHT



ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.08: REFCK_R0_FANOUT		
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2.09: REFCLK SYNTHESIZER R1A

U91-1

pXTAL_R1A → 8 XA
X7 (48 MHz): 2 → 7 X1_SHIELD; 4 → 10 X2_SHIELD
nXTAL_R1A → 9 XB

IF THE HQ_CLK OR LHC_CLK IS AC-COUPLED ON THE SM, USE ZERO-OHM RESISTORS ON THESE CAPACITOR PADS.

HQ_CLK

320 MHZ IF FPGA#1 IS TCDS ENDPOINT.
40 MHZ IF SM IS TCDS ENDPOINT

bc_pHQ_CLK_IN (14) — C837 0.1 UF 0402 — ac_pHQ_CLK_IN — R338 100 0402 → 63 IN_0
bc_nHQ_CLK_IN (14) — C838 0.1 UF 0402 — ac_nHQ_CLK_IN → 64 /IN_0

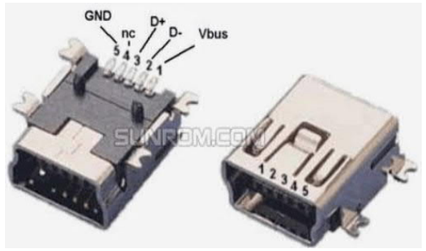
1 IN_1
2 /IN_1

J3
CON5

GND ← 9 TAB9 GND 5 → GND
8 TAB8 NC4 4 ×
7 TAB7 D+ 3 — bc_pR1_FP_CLK — C843 0.1 UF 0402 — ac_pR1_FP_CLK — R353 100 0402 → 14 IN_2
6 TAB6 D- 2 — bc_nR1_FP_CLK — C844 0.1 UF 0402 — ac_nR1_FP_CLK → 15 /IN_2
VBUS 1 ×

OPTIONAL FRONT PANEL CONNECTOR FOR AN LVDS EXTERNAL CLOCK.

THE CONNECTOR IS A "USB 2.0 MINI-B" STYLE.



A HI LEVEL ON THE "I2C_SEL" PIN ENABLES I2C PROGRAMMING MODE. THE CHIP HAS AN INTERNAL PULLUP.

U91-2

39 I2C_SEL — /INTR 12 → /SYN_R1A_INT (37)
I2C_SDA_SYN_R1A (37) ↔ 18 SDA/SDIO — /LOL 47
I2C_SCL_SYN_R1A (37) → 16 SCLK
/SYN_R1A_RESET (37) → 6 /RST
11 /OE
SYN_R1A_IN_SEL0 (37) → 3 IN_SEL_0
SYN_R1A_IN_SEL1 (37) → 4 IN_SEL_1
48 FINC
25 FDEC
5 RSVD

V_3V3 — 0603 10K R344 — R343 DNP 0603 — GND → 17 A1/SDO
V_3V3 — 0603 10K R324 — R323 DNP 0603 — GND → 19 A0//CS

I2C ADDR = 0X77

SI5395

ZERO-DELAY FEEDBACK
320 MHZ IF FPGA#1 IS TCDS ENDPOINT.
40 MHZ IF SM IS TCDS ENDPOINT

ac_pR1A_FB — C810 0.1 UF 0402 — R331 100 0402 → 61 FB_IN
ac_nR1A_FB — C803 0.1 UF 0402 → 62 /FB_IN

SI5395

DO NOT USE PINS 20,21 TO MAINTAIN COMPATIBILITY WITH THE SI5341.

OUT_0A	21	bc_pR1A_10	C347 0.1 UF 0402	
/OUT_0A	20	bc_nR1A_10	C348 0.1 UF 0402	
OUT_0	24	bc_pR1A_0	C439 0.1 UF 0402 — ac_pF1L_R0_AB 25	F1 QUAD AB (TCDS QUAD)
/OUT_0	23	bc_nR1A_0	C440 0.1 UF 0402 — ac_nF1L_R0_AB 25	
OUT_1	28	bc_pR1A_1	C345 0.1 UF 0402 — ac_pF2L_R0_AB 25	F2 QUAD AB (TCDS QUAD)
/OUT_1	27	bc_nR1A_1	C346 0.1 UF 0402 — ac_nF2L_R0_AB 25	
OUT_2	31	bc_pR1A_2	C437 0.1 UF 0402 — ac_pSYN_R1B_IN0 22	SYN R1B IN0
/OUT_2	30	bc_nR1A_2	C438 0.1 UF 0402 — ac_nSYN_R1B_IN0 22	
OUT_3	35	bc_pR1A_3	C343 0.1 UF 0402 — ac_pSYN_R1C_IN0 23	SYN R1C IN0
/OUT_3	34	bc_nR1A_3	C344 0.1 UF 0402 — ac_nSYN_R1C_IN0 23	
OUT_4	38	bc_pR1A_4	C435 0.1 UF 0402 — ac_pF1L_R1_AF 65	F1 QUAD AF
/OUT_4	37	bc_nR1A_4	C436 0.1 UF 0402 — ac_nF1L_R1_AF 65	
OUT_5	42	bc_pR1A_5	C341 0.1 UF 0402 — ac_pF1L_R1_U 67	F1 QUAD U (T,U,V)
/OUT_5	41	bc_nR1A_5	C342 0.1 UF 0402 — ac_nF1L_R1_U 67	
OUT_6	45	bc_pR1A_6	C433 0.1 UF 0402 — ac_pF2L_R1_AF 74	F2 QUAD AF
/OUT_6	44	bc_nR1A_6	C434 0.1 UF 0402 — ac_nF2L_R1_AF 74	
OUT_7	51	bc_pR1A_7	C339 0.1 UF 0402 — ac_pF2L_R1_U 76	F2 QUAD U (T,U,V)
/OUT_7	50	bc_nR1A_7	C340 0.1 UF 0402 — ac_nF2L_R1_U 76	
OUT_8	54	bc_pR1A_8	C431 0.1 UF 0402 — ac_pF1R_R1_L 25	F1 QUAD L (C2C/TCDS QUAD)
/OUT_8	53	bc_nR1A_8	C432 0.1 UF 0402 — ac_nF1R_R1_L 25	
OUT_9	56	bc_pR1A_9	C337 0.1 UF 0402 — ac_pF2R_R1_L 25	F2 QUAD L (C2C/TCDS QUAD)
/OUT_9	55	bc_nR1A_9	C338 0.1 UF 0402 — ac_nF2R_R1_L 25	
OUT_9A	59	bc_pR1A_FB		
/OUT_9A	58	bc_nR1A_FB		

DO NOT USE PINS 55,56 TO MAINTAIN COMPATIBILITY WITH THE SI5341.

U91-3

VDD 32, 46, 60 → V_1V8
VDDA 13 → V_3V3
VDDO_0 22 → V_1V8
VDDO_1 26
VDDO_2 29
VDDO_3 33
VDDO_4 36
VDDO_5 40
VDDO_6 43
VDDO_7 49
VDDO_8 52
VDDO_9 57
GND_PAD 65 → GND

SI5395

V_3V3 — C829 1 UF 0402 10v — GND

V_1V8 — C751 1 UF 0402 10v — C815 1 UF 0402 10v — C793 1 UF 0402 10v — C750 1 UF 0402 10v — C749 1 UF 0402 10v — C820 1 UF 0402 10v — C798 1 UF 0402 10v — C748 1 UF 0402 10v — GND

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1

Title: 2.09: REFCLK SYNTHESIZER R1A

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2.10: REFCLK SYNTHESIZER R1B

U90-1

pXTAL_R1B → 8 XA
X6 (48 MHz) 1 / 2 / 4 / 3
nXTAL_R1B → 9 XB
7 X1_SHIELD
10 X2_SHIELD

DO NOT USE PINS 20,21 TO MAINTAIN COMPATIBILITY WITH THE SI5341.

SYN R1B IN0

ac_pSYN_R1B_IN0 (21) → R351 100 0402 → 63 IN_0
ac_nSYN_R1B_IN0 (21) → 64 /IN_0

TCDS RECOVERED CLOCK
ALWAYS 40 MHZ

bc_pF1_TCDS_RECOV_CLK (46) → C841 0.1 UF 0402 → ac_pF1_TCDS_RECOV_CLK → R352 100 0402 → 1 IN_1
bc_nF1_TCDS_RECOV_CLK (46) → C842 0.1 UF 0402 → ac_nF1_TCDS_RECOV_CLK → 2 /IN_1

14 IN_2
15 /IN_2

OUT_0	24	bc_pR1B_0	C335 0.1 UF 0402	ac_pF1L_R1_AB 25	F1 QUAD AB (TCDS QUAD)
/OUT_0	23	bc_nR1B_0	C336 0.1 UF 0402	ac_nF1L_R1_AB 25	
OUT_1	28	bc_pR1B_1	C429 0.1 UF 0402	ac_pF1_TCDS40_CLK 47	F1 LOGIC TCDS 40MHZ INPUT
/OUT_1	27	bc_nR1B_1	C430 0.1 UF 0402	ac_nF1_TCDS40_CLK 47	
OUT_2	31	bc_pR1B_2	C333 0.1 UF 0402	ac_pF1L_R1_AD 62	F1 QUAD AD (AC,AD,AE)
/OUT_2	30	bc_nR1B_2	C334 0.1 UF 0402	ac_nF1L_R1_AD 62	
OUT_3	35	bc_pR1B_3	C427 0.1 UF 0402	ac_pF1L_R1_R 63	F1 QUAD R (Q,R,S)
/OUT_3	34	bc_nR1B_3	C428 0.1 UF 0402	ac_nF1L_R1_R 63	
OUT_4	38	bc_pR1B_4	C331 0.1 UF 0402	ac_pF1L_R1_Y 64	F1 QUAD Y (X,Y,Z)
/OUT_4	37	bc_nR1B_4	C332 0.1 UF 0402	ac_nF1L_R1_Y 64	
OUT_5	42	bc_pR1B_5	C425 0.1 UF 0402	ac_pNO_F2_TCDS40_CLK 23	NO F2 TCDS 40MHZ SYNTH R1C
			C329 0.1 UF 0402	ac_pF2_TCDS40_CLK 57	F2 LOGIC TCDS 40MHZ INPUT
/OUT_5	41	bc_nR1B_5	C330 0.1 UF 0402	ac_nF2_TCDS40_CLK 57	
			C426 0.1 UF 0402	ac_nNO_F2_TCDS40_CLK 23	NO F2 TCDS 40MHZ SYNTH R1C
OUT_6	45	bc_pR1B_6	C423 0.1 UF 0402	ac_pF2L_R1_AD 71	F2 QUAD AD (AC,AD,AE)
/OUT_6	44	bc_nR1B_6	C424 0.1 UF 0402	ac_nF2L_R1_AD 71	
OUT_7	51	bc_pR1B_7	C327 0.1 UF 0402	ac_pF2L_R1_R 72	F2 QUAD R (Q,R,S)
/OUT_7	50	bc_nR1B_7	C328 0.1 UF 0402	ac_nF2L_R1_R 72	
OUT_8	54	bc_pR1B_8	C421 0.1 UF 0402	ac_pF2L_R1_Y 73	F2 QUAD Y (X,Y,Z)
/OUT_8	53	bc_nR1B_8	C422 0.1 UF 0402	ac_nF2L_R1_Y 73	

IF F2 IS NOT INSTALLED, OMIT THE CAPACITORS THAT COUPLE THIS 40 MHZ CLOCK TO F2 AND INSTALL THE CAPACITORS THAT COUPLE THE CLOCK TO SYNTH R1C. THIS WILL PROVIDE A TCDS-RECOVERED REFERENCE CLOCK SIGNAL TO THE GTY QUADS ON THE RIGHT SIDE OF F1.

OUT_9 56
/OUT_9 55

DO NOT USE PINS 55,56 TO MAINTAIN COMPATIBILITY WITH THE SI5341.

ZERO-DELAY FEEDBACK
320 MHZ IF FPGA#1 IS TCDS ENDPOINT.
40 MHZ IF SM IS TCDS ENDPOINT

ac_pR1b_FB → C809 0.1 UF 0402 → R330 100 0402 → 61 FB_IN
ac_nR1b_FB → C802 0.1 UF 0402 → 62 /FB_IN
OUT_9A 59 bc_pR1b_FB
/OUT_9A 58 bc_nR1b_FB
SI5395

A HI LEVEL ON THE "I2C_SEL" PIN ENABLES I2C PROGRAMMING MODE. THE CHIP HAS AN INTERNAL PULLUP.

U90-2

39	I2C_SEL	/INTR	12 → /SYN_R1B_INT 37
18	SDA/SDIO	/LOL	47
16	SCLK		
6	/RST		
11	/OE		
3	IN_SEL_0		
4	IN_SEL_1		
48	FINC		
25	FDEC		
5	RSVD		
17	A1/SDO		
19	A0//CS		

I2C_SDA_SYN_R1B 37
I2C_SCL_SYN_R1B 37
/SYN_R1B_RESET 37
SYN_R1B_IN_SEL0 37
SYN_R1B_IN_SEL1 37

V_3V3 → 0603 10K R342 → GND (R341 DNP 0603)
V_3V3 → 0603 10K R322 → GND (R321 DNP 0603)

I2C ADDR = 0X77

SI5395

V_3V3 → C828 1 UF 0402 10v → GND

U90-3

VDD	32	V_1V8
VDD	46	
VDD	60	
VDDA	13	V_3V3
VDDO_0	22	V_1V8
VDDO_1	26	
VDDO_2	29	
VDDO_3	33	
VDDO_4	36	
VDDO_5	40	
VDDO_6	43	
VDDO_7	49	
VDDO_8	52	
VDDO_9	57	
GND_PAD	65	GND

SI5395

V_1V8 → C797 1 UF 0402 10v, C744 1 UF 0402 10v, C745 1 UF 0402 10v, C746 1 UF 0402 10v, C747 1 UF 0402 10v, C819 1 UF 0402 10v, C792 1 UF 0402 10v, C814 1 UF 0402 10v → GND

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1

Title: 2.10: REFCLK SYNTHESIZER R1B

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2.11: REFCLK SYNTHESIZER R1C

U89-1

pXTAL_R1C → XA (8)
X5 (1, 2, 4, 3) 48 MHz
nXTAL_R1C → XB (9)
X1_SHIELD (7)
X2_SHIELD (10)
OUT_0A (21)
/OUT_0A (20)

DO NOT USE PINS 20,21 TO MAINTAIN COMPATIBILITY WITH THE SI5341.

SYN R1C IN0

ac_pSYN_R1C_IN0 21 → R337 100 0402 → IN_0 (63)
ac_nSYN_R1C_IN0 21 → /IN_0 (64)

NO F2
TCDS 40MHZ SYNTH R1C

ac_pNO_F2_TCDS40_CLK 22 → R350 100 0402 → IN_1 (1)
ac_nNO_F2_TCDS40_CLK 22 → /IN_1 (2)

IF F2 IS NOT INSTALLED, THIS WILL PROVIDE A TCDS-RECOVERED REFERENCE CLOCK SIGNAL TO THE GTY QUADS ON THE RIGHT SIDE OF F1. IF F2 IS INSTALLED, THERE WILL NOT BE ANY SIGNAL ON THIS INPUT.

IN_2 (14)
/IN_2 (15)

OUT_0 (24)	bc_pR1C_0	C325 0.1 UF 0402	ac_pF1R_R1_N 79	F1 QUAD N (M,N,O)
/OUT_0 (23)	bc_nR1C_0	C326 0.1 UF 0402	ac_nF1R_R1_N 79	
OUT_1 (28)	bc_pR1C_1	C419 0.1 UF 0402	ac_pF2R_R1_I 79	F2 QUAD I (H,I,J)
/OUT_1 (27)	bc_nR1C_1	C420 0.1 UF 0402	ac_nF2R_R1_I 79	
OUT_2 (31)	bc_pR1C_2	C323 0.1 UF 0402	ac_pF2R_R1_E 80	F2 QUAD E (D,E,F)
/OUT_2 (30)	bc_nR1C_2	C324 0.1 UF 0402	ac_nF2R_R1_E 80	
OUT_3 (35)	bc_pR1C_3	C417 0.1 UF 0402	ac_pF2R_R1_B 82	F2 QUAD B (A,B,C)
/OUT_3 (34)	bc_nR1C_3	C418 0.1 UF 0402	ac_nF2R_R1_B 82	
OUT_4 (38)	bc_pR1C_4	C321 0.1 UF 0402	ac_pF2R_R1_P 83	F2 QUAD P
/OUT_4 (37)	bc_nR1C_4	C322 0.1 UF 0402	ac_nF2R_R1_P 83	
OUT_5 (42)	bc_pR1C_5	C415 0.1 UF 0402	ac_pF2R_R1_N 81	F2 QUAD N (M,N,O)
/OUT_5 (41)	bc_nR1C_5	C416 0.1 UF 0402	ac_nF2R_R1_N 81	
OUT_6 (45)	bc_pR1C_6	C319 0.1 UF 0402	ac_pF1R_R1_B 80	F1 QUAD B (A,B,C)
/OUT_6 (44)	bc_nR1C_6	C320 0.1 UF 0402	ac_nF1R_R1_B 80	
OUT_7 (51)	bc_pR1C_7	C317 0.1 UF 0402	ac_pF1R_R1_E 82	F1 QUAD E (D,E,F)
/OUT_7 (50)	bc_nR1C_7	C318 0.1 UF 0402	ac_nF1R_R1_E 82	
OUT_8 (54)	bc_pR1C_8	C413 0.1 UF 0402	ac_pF1R_R1_G 83	F1 QUAD G
/OUT_8 (53)	bc_nR1C_8	C414 0.1 UF 0402	ac_nF1R_R1_G 83	

OUT_9 (56)
/OUT_9 (55)

DO NOT USE PINS 55,56 TO MAINTAIN COMPATIBILITY WITH THE SI5341.

OUT_9A (59)	bc_pR1C_9	C315 0.1 UF 0402	ac_pF1R_R1_I 81	F1 QUAD I (H,I,J)
/OUT_9A (58)	bc_nR1C_9	C316 0.1 UF 0402	ac_nF1R_R1_I 81	

FB_IN (61)
/FB_IN (62)

SI5395

A HI LEVEL ON THE "I2C_SEL" PIN ENABLES I2C PROGRAMMING MODE. THE CHIP HAS AN INTERNAL PULLUP.

U89-2

I2C_SEL (39)		/INTR (12)	→ /SYN_R1C_INT 37
I2C_SDA_SYN_R1C 37	SDA/SDIO (18)	/LOL (47)	
I2C_SCL_SYN_R1C 37	SCLK (16)		
/SYN_R1C_RESET 37	/RST (6)		
	/OE (11)		
SYN_R1C_IN_SEL0 37	IN_SEL_0 (3)		
SYN_R1C_IN_SEL1 37	IN_SEL_1 (4)		
	FINC (48)		
	FDEC (25)		
	RSVD (5)		

V_3V3 → 0603 10K R340 → A1/SDO (17)
GND → R339 DNP 0603 → A1/SDO (17)
V_3V3 → 0603 10K R320 → A0//CS (19)
GND → R319 DNP 0603 → A0//CS (19)

I2C ADDR = 0X77

SI5395

V_3V3 → C827 1 UF 0402 10v → GND

U89-3

VDD (32)	V_1V8
VDD (46)	
VDD (60)	
VDDA (13)	V_3V3
VDDO_0 (22)	V_1V8
VDDO_1 (26)	
VDDO_2 (29)	
VDDO_3 (33)	
VDDO_4 (36)	
VDDO_5 (40)	
VDDO_6 (43)	
VDDO_7 (49)	
VDDO_8 (52)	
VDDO_9 (57)	
GND_PAD (65)	GND

SI5395

V_1V8 → C813 1 UF 0402 10v, C791 1 UF 0402 10v, C743 1 UF 0402 10v, C742 1 UF 0402 10v, C740 1 UF 0402 10v, C741 1 UF 0402 10v, C818 1 UF 0402 10v, C796 1 UF 0402 10v → GND

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM W/ DUAL A2577, MK1		
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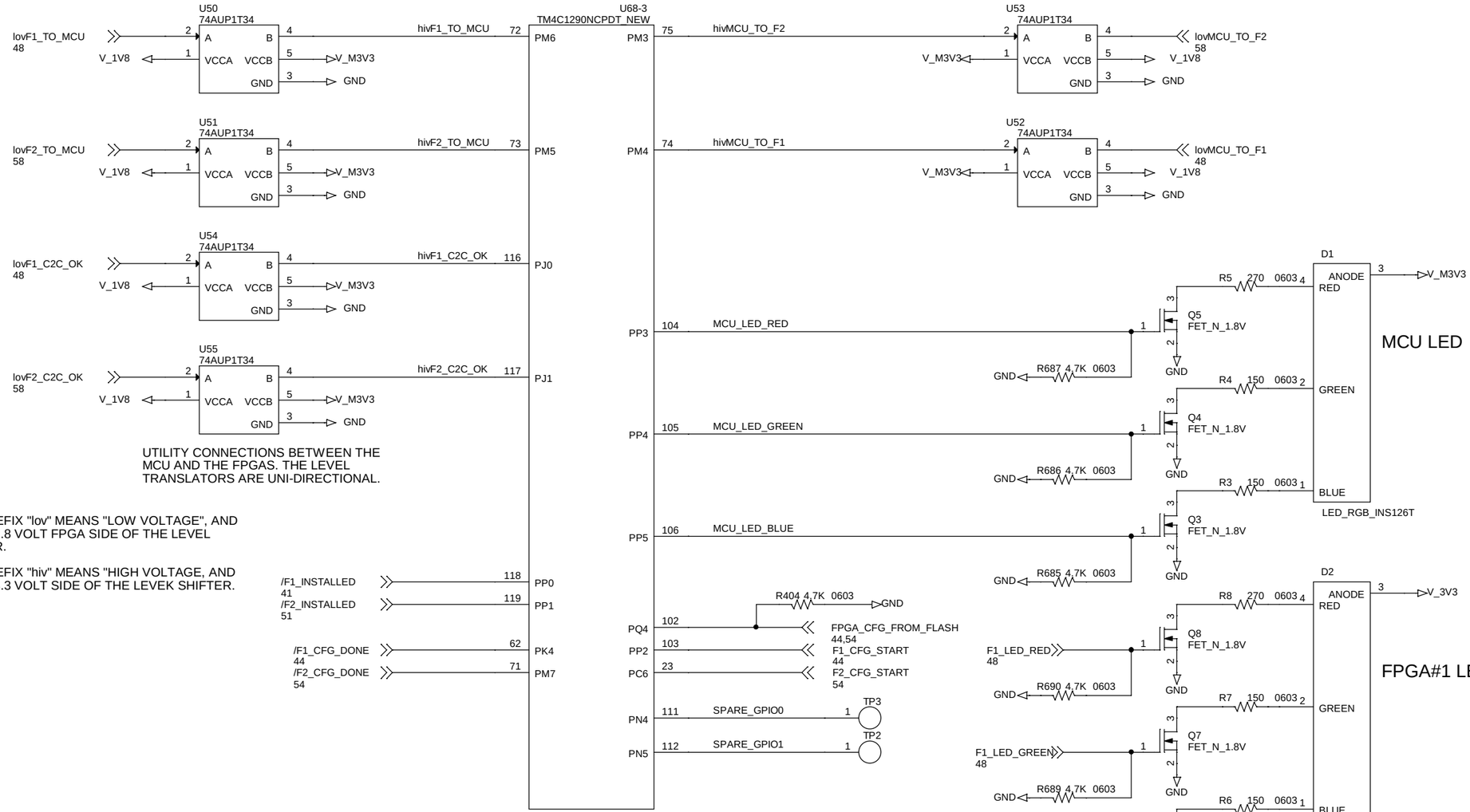
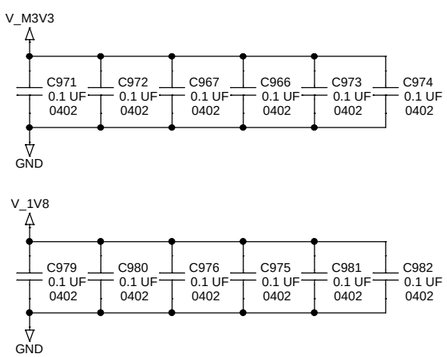
2.12: LEDS AND LEVEL SHIFTERS



UTILITY CONNECTIONS BETWEEN THE MCU AND THE FPGAS. THE LEVEL TRANSLATORS ARE UNI-DIRECTIONAL.

THE PREFIX "lov" MEANS "LOW VOLTAGE", AND IS THE 1.8 VOLT FPGA SIDE OF THE LEVEL SHIFTER.

THE PREFIX "hiv" MEANS "HIGH VOLTAGE, AND IS THE 3.3 VOLT SIDE OF THE LEVEK SHIFTER.



APOLLO CM W/ DUAL A2577, MK1		
Title: 2.12: LEDS AND LEVEL SHIFTERS		
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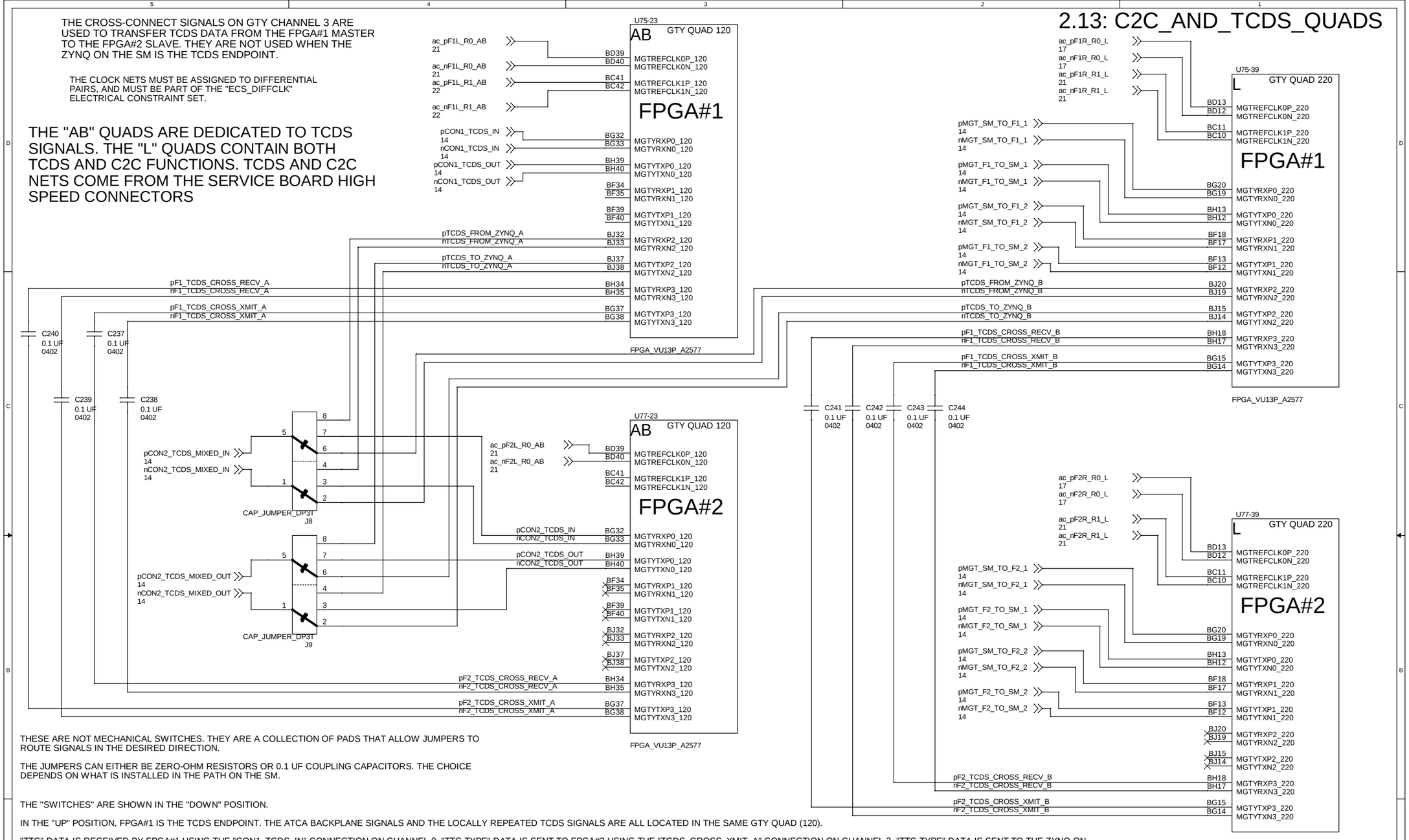
2.13: C2C_AND_TCDS_QUADS

THE CROSS-CONNECT SIGNALS ON GTY CHANNEL 3 ARE USED TO TRANSFER TCDS DATA FROM THE FPGA#1 MASTER TO THE FPGA#2 SLAVE. THEY ARE NOT USED WHEN THE ZYNQ ON THE SM IS THE TCDS ENDPOINT.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "AB" QUADS ARE DEDICATED TO TCDS SIGNALS. THE "L" QUADS CONTAIN BOTH TCDS AND C2C FUNCTIONS. TCDS AND C2C NETS COME FROM THE SERVICE BOARD HIGH SPEED CONNECTORS



THESE ARE NOT MECHANICAL SWITCHES. THEY ARE A COLLECTION OF PADS THAT ALLOW JUMPERS TO ROUTE SIGNALS IN THE DESIRED DIRECTION.

THE JUMPERS CAN EITHER BE ZERO-OHM RESISTORS OR 0.1 UF COUPLING CAPACITORS. THE CHOICE DEPENDS ON WHAT IS INSTALLED IN THE PATH ON THE SM.

THE "SWITCHES" ARE SHOWN IN THE "DOWN" POSITION.

IN THE "UP" POSITION, FPGA#1 IS THE TCDS ENDPOINT. THE ATCA BACKPLANE SIGNALS AND THE LOCALLY REPEATED TCDS SIGNALS ARE ALL LOCATED IN THE SAME GTY QUAD (120).

"TTC" DATA IS RECEIVED BY FPGA#1 USING THE "CON1_TCDS_IN" CONNECTION ON CHANNEL 0. "TTC-TYPE" DATA IS SENT TO FPGA#2 USING THE "TCDS_CROSS_XMIT_A" CONNECTION ON CHANNEL 3. "TTC-TYPE" DATA IS SENT TO THE ZYNQ ON THE SM USING THE "TCDS_TO_ZYNQ_A" CONNECTION ON CHANNEL 2.

"TTS-TYPE" RESPONSE DATA FROM FPGA#2 IS RECEIVED ON THE "TCDS_CROSS_RECV_A" CONNECTION ON CHANNEL 3. "TTS-TYPE" RESPONSE DATA FROM THE SM COMES IN ON THE "TCDS_FROM_ZYNQ_A" CONNECTION ON CHANNEL 2. FPGA#1 MERGES THE "TTS" RESPONSE DATA FROM THE SM AND FPGA#2, AND SENDS IT TO THE ATCA BACKPLANE USING THE "CON1_TCDS_OUT" CONNECTION ON CHANNEL 0.

==========

IN THE "MIDDLE" POSITION, THE SM IS THE TCDS ENDPOINT. EACH FPGA HAS ITS OWN CONNECTION TO THE SM. NO CROSS CONNECTIONS BETWEEN THE TWO FPGAS ARE USED.

"TTC-TYPE" DATA IS RECEIVED BY FPGA#1 USING THE "CON1_TCDS_IN" CONNECTION ON CHANNEL 0.
"TTC-TYPE" DATA IS RECEIVED BY FPGA#2 USING THE "CON2_TCDS_MIXED_IN / CON2_TCDS_IN" CONNECTION ON CHANNEL 0.

"TTS-TYPE" RESPONSE DATA FROM FPGA#1 IS SENT TO THE SM USING THE "CON1_TCDS_OUT" CONNECTION ON CHANNEL 0. "TTS-TYPE" RESPONSE DATA FROM FPGA#2 IS SENT TO THE SM USING THE "CON2_TCDS_OUT / CONN2_TCDS_MIXED_OUT" CONNECTION ON CHANNEL 0. THE SM MERGES THE "TTS" RESPONSE DATA FROM THE TWO FPGAS.

==========

IN THE "DOWN" POSITION, FPGA#1 IS THE TCDS ENDPOINT. THE ATCA BACKPLANE SIGNALS ARE CONNECTED TO GTY QUAD 120. RELAYING THE "TTC-TYPE" DATA TO FPGA#2 AND THE SM IS DONE IN A DIFFERENT GTY QUAD, QUAD 220. THE "TTS-TYPE" RESPONSE DATA FROM FPGA#2 AND THE SM IS RECEIVED IN QUAD 220. IT IS COMBINED WITH "TTS-TYPE" DATA FROM FPGA#1 AND SENT TO THE ATCA BACKPLANE FROM QUAD 120.

"TTC" DATA IS RECEIVED BY FPGA#1 USING THE "CON1_TCDS_IN" CONNECTION ON CHANNEL 0.
"TTC-TYPE" DATA IS SENT TO FPGA#2 USING THE "TCDS_CROSS_XMIT_B" CONNECTION ON CHANNEL 3 OF QUAD 220.
"TTC-TYPE" DATA IS SENT TO THE ZYNQ ON THE SM USING THE "TCDS_TO_ZYNQ_B" CONNECTION ON CHANNEL 2 OF QUAD 220.

"TTS-TYPE" RESPONSE DATA FROM FPGA#2 IS RECEIVED ON THE "TCDS_CROSS_RECV_B" CONNECTION ON CHANNEL 3 OF QUAD 220. "TTS-TYPE" RESPONSE DATA FROM THE SM COMES IN ON THE "TCDS_FROM_ZYNQ_B" CONNECTION ON CHANNEL 2 OF QUAD 220. FPGA#1 MERGES THE "TTS" RESPONSE DATA FROM THE SM AND FPGA#2, AND SENDS IT TO THE ATCA BACKPLANE USING THE "CON1_TCDS_OUT" CONNECTION ON CHANNEL 0 OF QUAD 120.

APOLLO CM W/ DUAL A2577, MK1		
Title: 2.13: C2C_AND_TCDS_QUADS		
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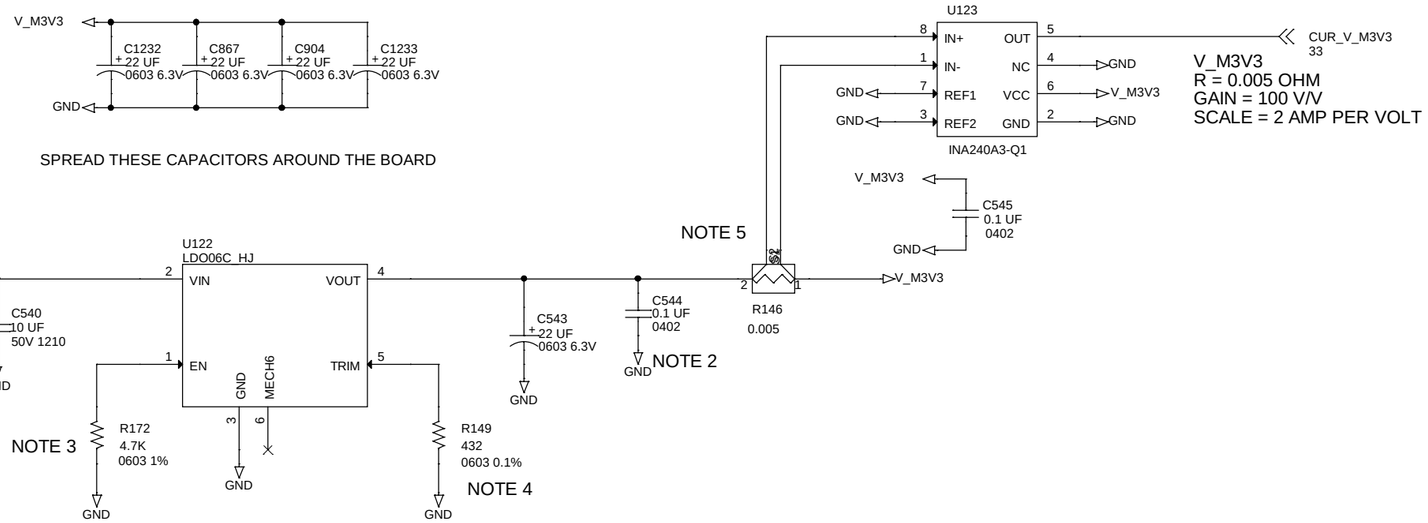
3.01: POWER MANAGEMENT M3V3



GENERAL NOTES:

V_M3V3 IS THE "MANAGEMENT" POWER. IT PROVIDES POWER TO THE POWER SEQUENCING CIRCUIT. IT IS ALWAYS ON WHEN +12V IS SUPPLIED TO THE BOARD.

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

NOTES:

NOTE 1 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL INPUT CAPACITORS.

NOTE 2 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL OUTPUT CAPACITORS.

NOTE 3 UNDERVOLTAGE LOCKOUT RESISTOR
R = 14.81 * (6.81 / ((6.81*Ven) - 18.16))
A 4.7K RESISTOR GIVES 5.8 VOLTS MINIMUM TURNON VOLTAGE

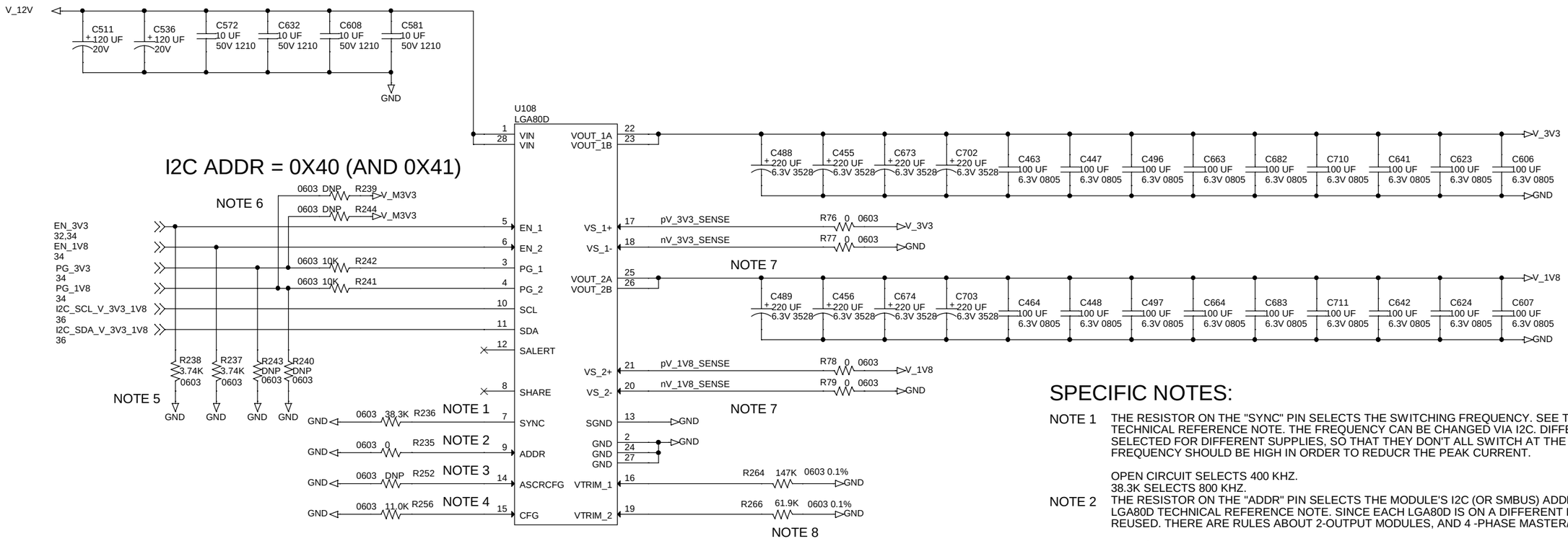
NOTE 4 OUTPUT SETPOINT RESISTOR
R = 1.182 / (VOUT - 0.591)
FOR 3.3 VOLTS, R = 436 OHMS (IF R=432 THEN V=3.327)

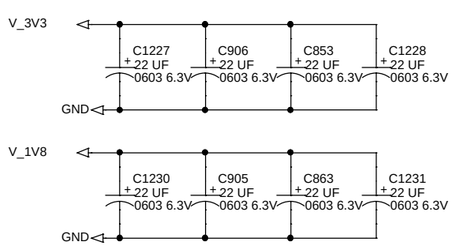
NOTE 5 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 5 MILLIOHMS AND A CURRENT OF 5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LDO06C REGULATOR IS RATED FOR 6 AMPS. IF MORE THAN 5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 5 MILLIOHMS.

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.01: POWER MANAGEMENT M3V3		
Size	Document Number: 6089-119	Rev: A
Date: Tuesday, June 15, 2021	Sheet 26 of 84	

3.02: POWER GLOBAL 3.3V AND 1.8V





NOTE 9

SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME. FOR 3.3V, THE FREQUENCY SHOULD BE HIGH IN ORDER TO REDUCR THE PEAK CURRENT.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=11K SELECTS 2-OUTPUT @ 35A(avg)/45A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 147K FOR 3.3V
RSET = 61.9K FOR 1.8V

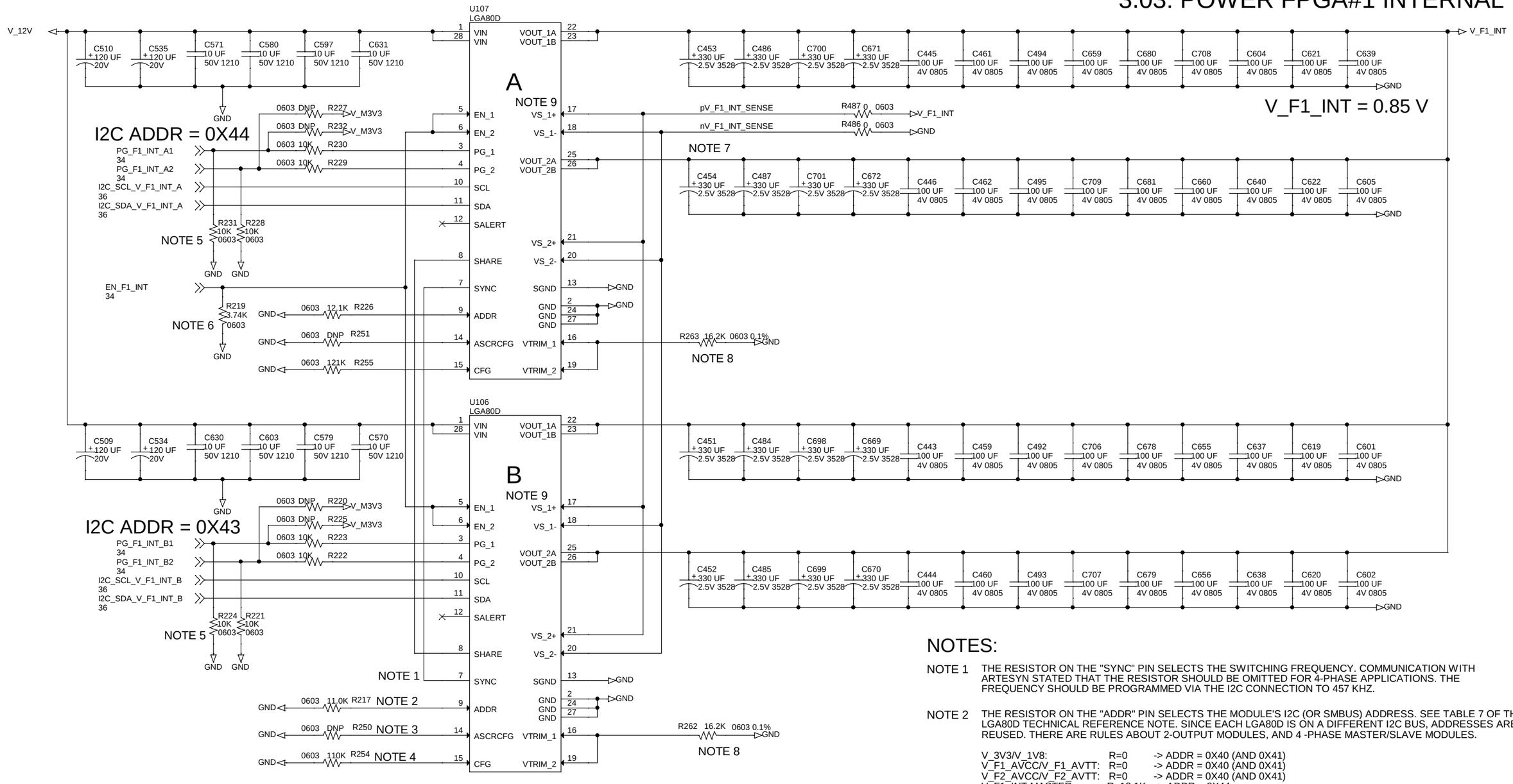
NOTE 9 SPREAD THESE CAPACITORS AROUND THE BOARD

GENERAL NOTES:

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.02: POWER GLOBAL 3.3V AND 1.8V		
Size	Document Number: 6089-119	Rev: A
Date: Tuesday, June 15, 2021	Sheet 27 of 84	

3.03: POWER FPGA#1 INTERNAL



NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. COMMUNICATION WITH ARTESYN STATED THAT THE RESISTOR SHOULD BE OMITTED FOR 4-PHASE APPLICATIONS. THE FREQUENCY SHOULD BE PROGRAMMED VIA THE I2C CONNECTION TO 457 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 10K.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 110K ON THE MASTER AND 121K ON THE SLAVE FOR 4-PHASE @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

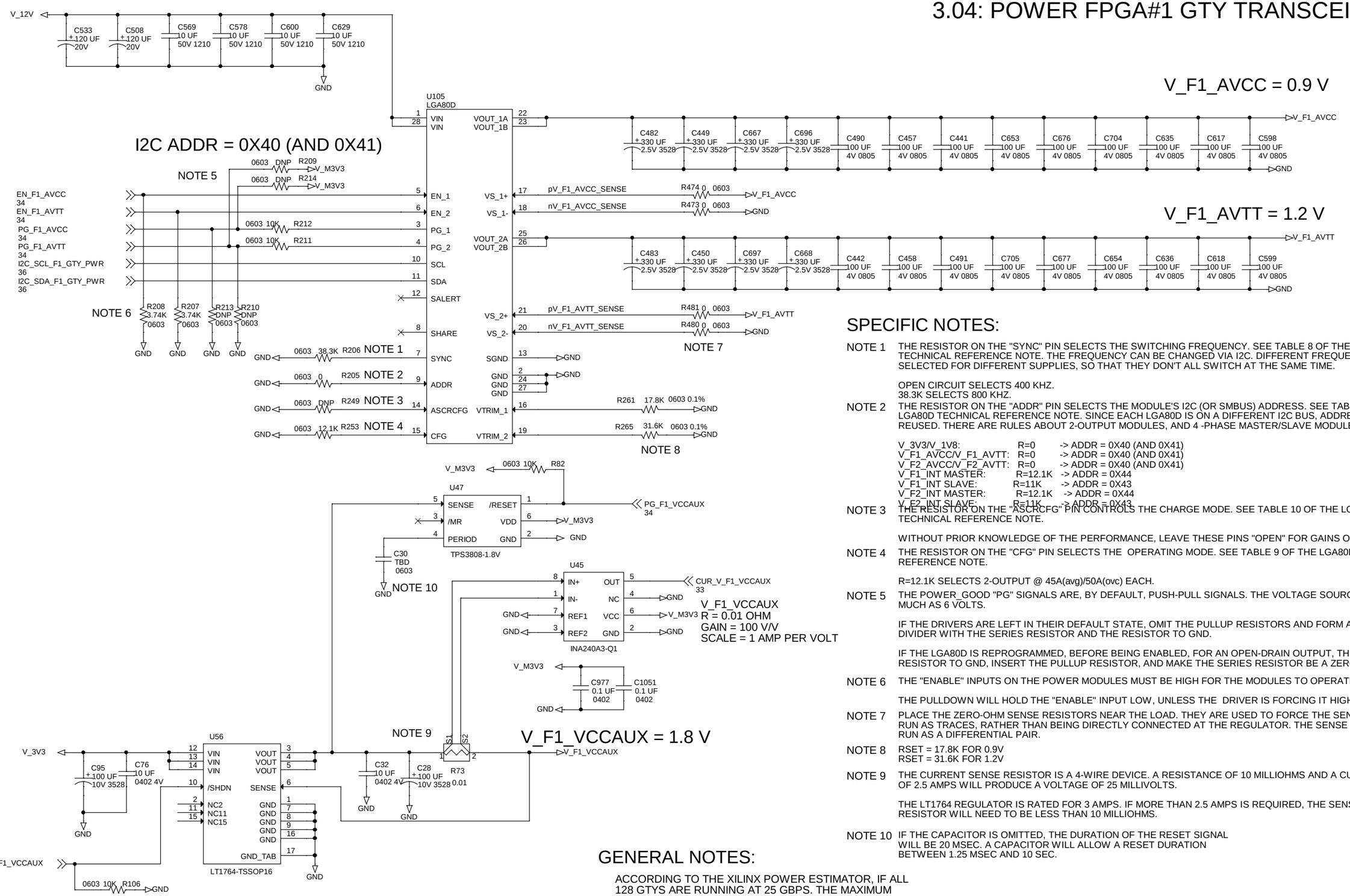
NOTE 8 RSET = 16.2K FOR 0.85V

NOTE 9 THE MASTER IS LABELED "A".
THE SLAVE IS LABELED "B".

NOTE 10 PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.03: POWER FPGA#1 INTERNAL		
Size	Document Number: 6089-119	Rev: A
Date: Thursday, June 24, 2021	Sheet 28 of 84	

3.04: POWER FPGA#1 GTY TRANSCEIVER



SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=12.1K SELECTS 2-OUTPUT @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 17.8K FOR 0.9V
RSET = 31.6K FOR 1.2V

NOTE 9 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 10 MILLIOHMS AND A CURRENT OF 2.5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LT1764 REGULATOR IS RATED FOR 3 AMPS. IF MORE THAN 2.5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 10 MILLIOHMS.

NOTE 10 IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

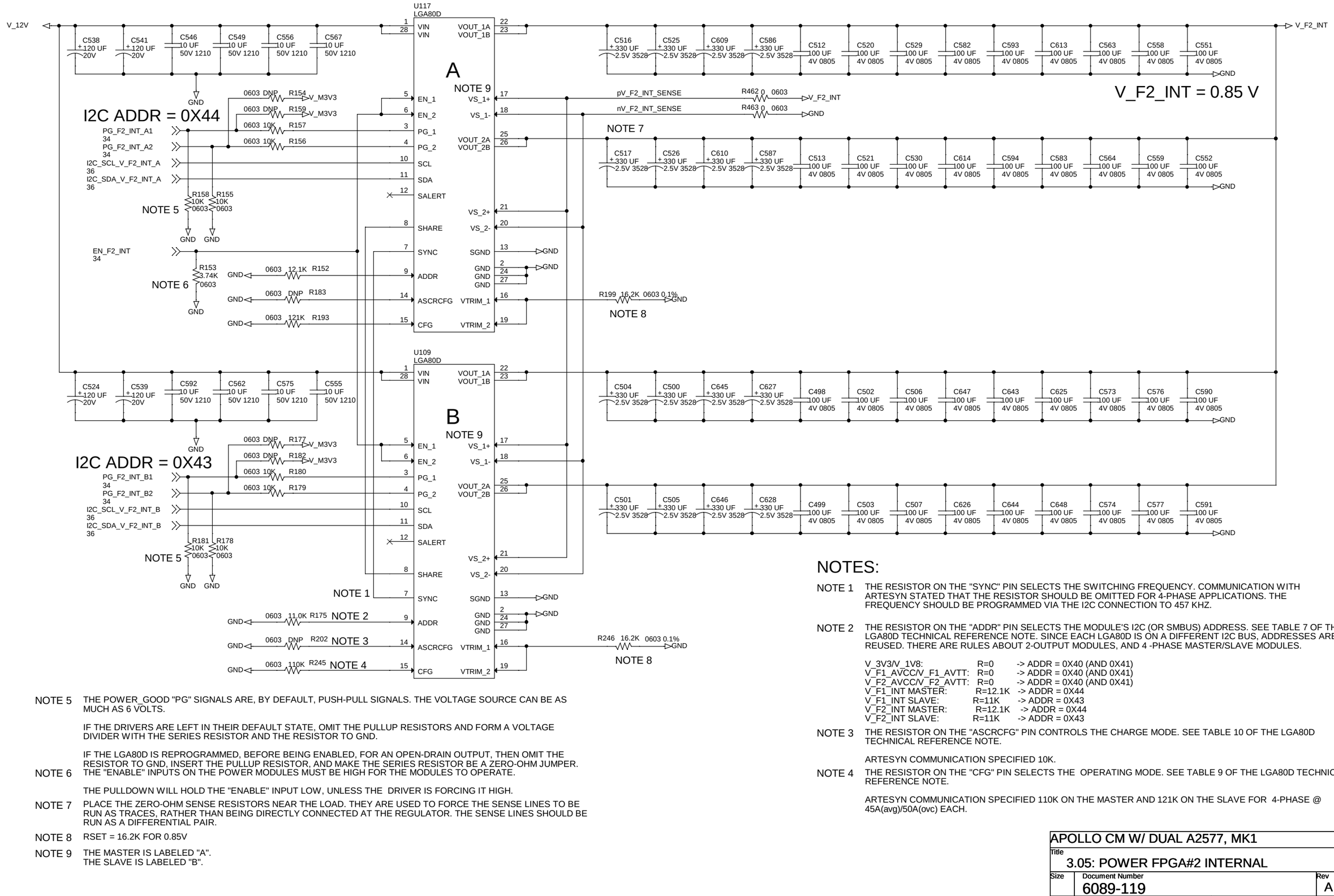
GENERAL NOTES:

ACCORDING TO THE XILINX POWER ESTIMATOR, IF ALL 128 GTYS ARE RUNNING AT 25 GBPS. THE MAXIMUM CURRENT DRAWS WILL BE:
GTY_AVCC = 11.5 AMPS
GTY_AVTT = 30 AMPS
GTY_VCCAUX = 2.5 AMPS

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.04: POWER FPGA#1 GTY TRANSCEIVER		
Size	Document Number: 6089-119	Rev: A
Date: Tuesday, June 15, 2021	Sheet 29 of 84	

3.05: POWER FPGA#2 INTERNAL



NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

NOTE 6 IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER. THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 16.2K FOR 0.85V

NOTE 9 THE MASTER IS LABELED "A".
THE SLAVE IS LABELED "B".

NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. COMMUNICATION WITH ARTESYN STATED THAT THE RESISTOR SHOULD BE OMITTED FOR 4-PHASE APPLICATIONS. THE FREQUENCY SHOULD BE PROGRAMMED VIA THE I2C CONNECTION TO 457 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

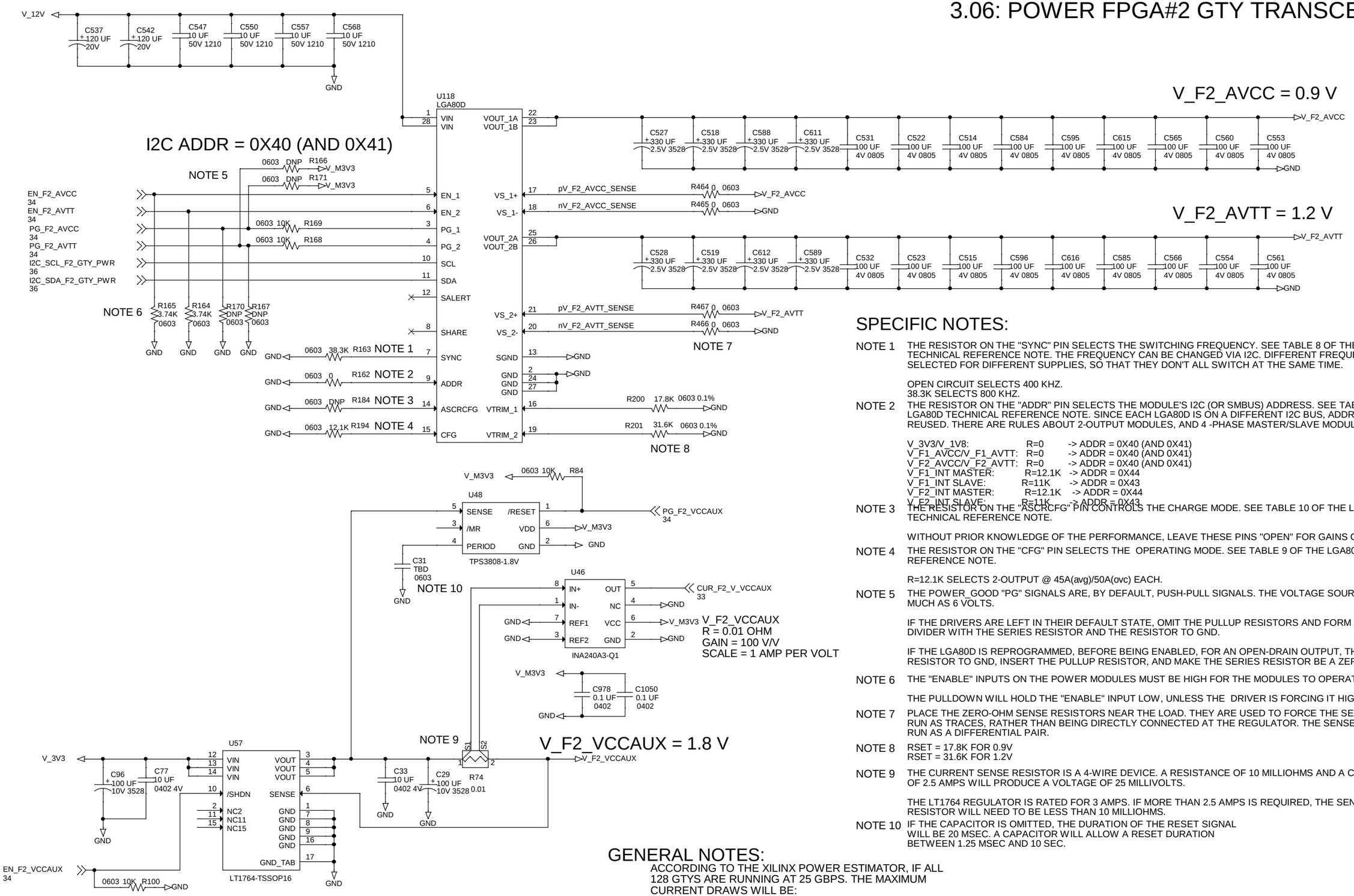
ARTESYN COMMUNICATION SPECIFIED 10K.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 110K ON THE MASTER AND 121K ON THE SLAVE FOR 4-PHASE @ 45A(avg)/50A(ovc) EACH.

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.05: POWER FPGA#2 INTERNAL		
Size	Document Number: 6089-119	Rev: A
Date: Thursday, June 24, 2021	Sheet 30 of 84	

3.06: POWER FPGA#2 GTY TRANSCEIVER



SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=12.1K SELECTS 2-OUTPUT @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 17.8K FOR 0.9V
RSET = 31.6K FOR 1.2V

NOTE 9 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 10 MILLIOHMS AND A CURRENT OF 2.5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LT1764 REGULATOR IS RATED FOR 3 AMPS. IF MORE THAN 2.5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 10 MILLIOHMS.

NOTE 10 IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

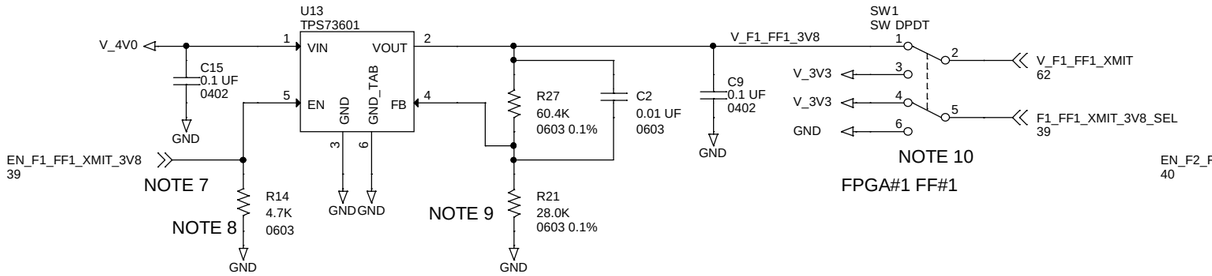
GENERAL NOTES:

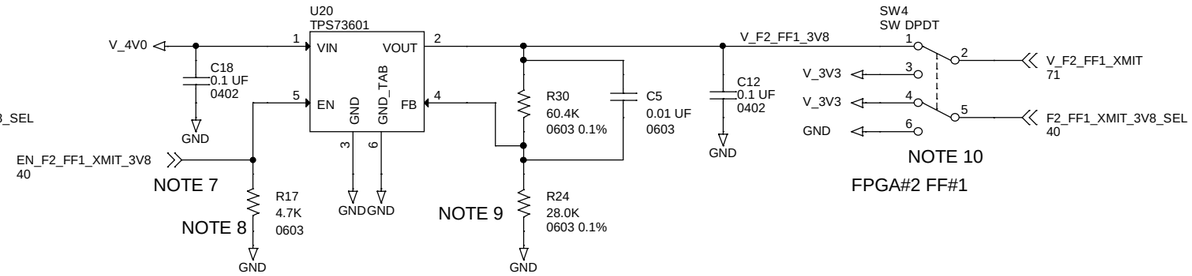
ACCORDING TO THE XILINX POWER ESTIMATOR, IF ALL 128 GTYS ARE RUNNING AT 25 GBPS. THE MAXIMUM CURRENT DRAWS WILL BE:
GTY_AVCC = 11.5 AMPS
GTY_AVTT = 30 AMPS
GTY_VCCAUX = 2.5 AMPS

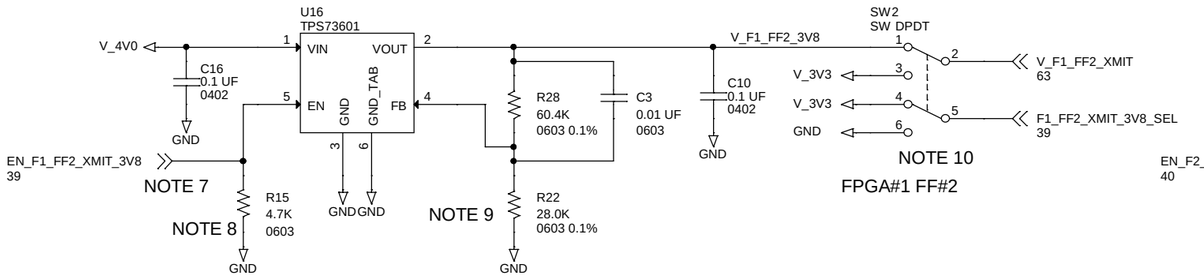
PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

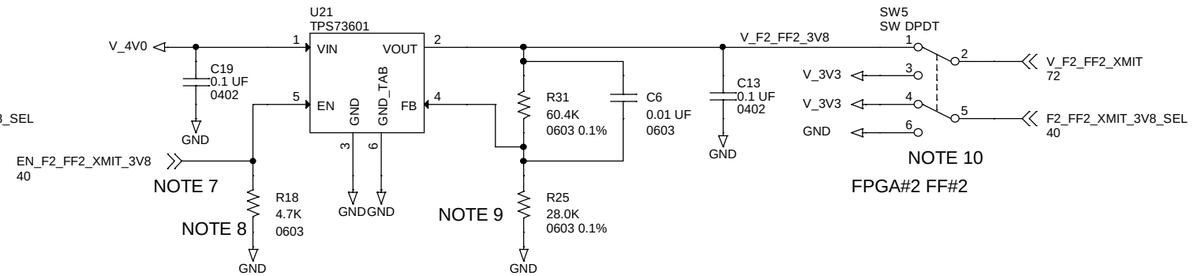
APOLLO CM W/ DUAL A2577, MK1		
Title: 3.06: POWER FPGA#2 GTY TRANSCEIVER		
Size	Document Number: 6089-119	Rev: A
Date: Tuesday, June 15, 2021	Sheet 31 of 84	

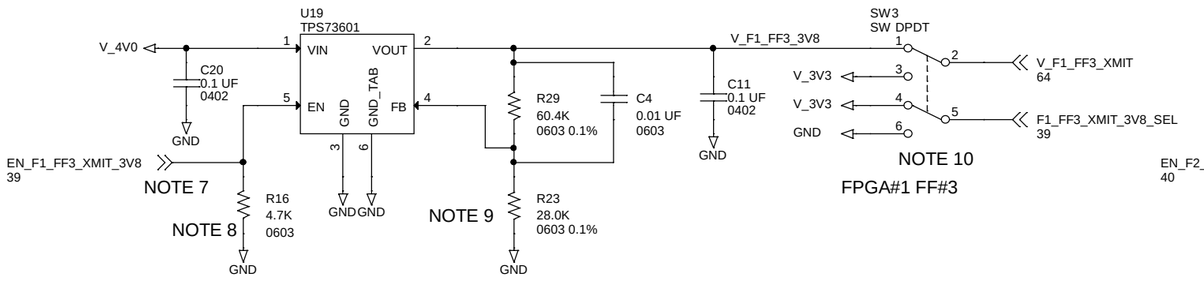
3.07: POWER FOR FF X12 XMIT

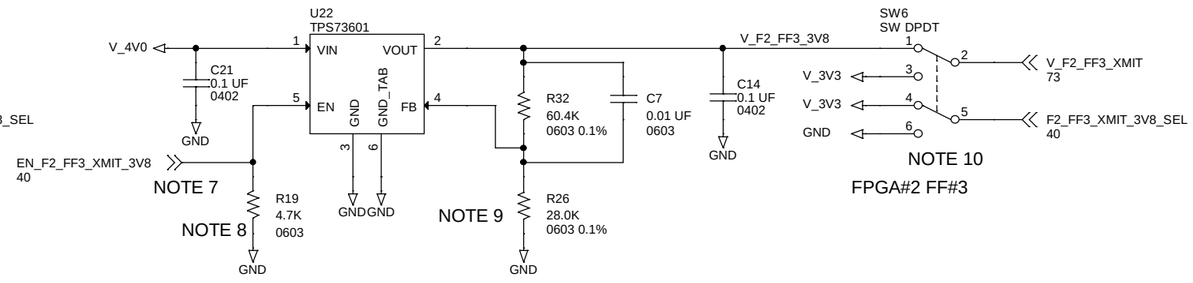




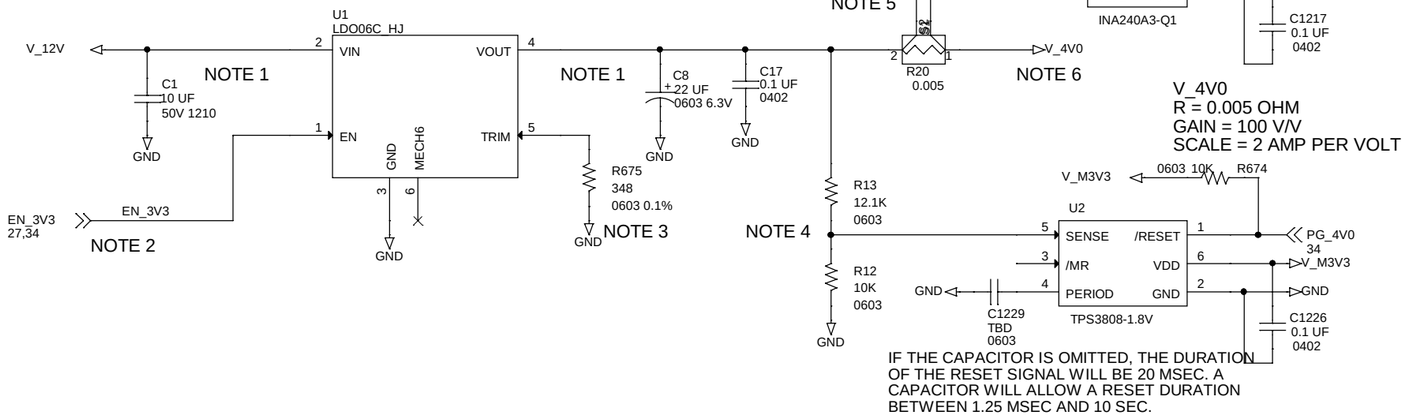








V_4V0 IS USED TO SUPPLY THE 3.8 VOLT REGULATORS FOR THE 12-LANE FIREFLY TRANSMITTERS.



NOTE 1 THE LDO06C DOES NOT REQUIRE ANY EXTERNAL INPUT OR OUTPUT CAPACITORS.

NOTE 2 THE LDO06C IS ENABLED AT THE SAME TIME AS THE BOARD-WIDE 3.3V SUPPLY.

NOTE 3 LDO06C OUTPUT SETPOINT RESISTOR
R = 1.182 / (VOUT - 0.591)
FOR 4.0 VOLTS, R=347 OHMS

NOTE 4 THE MONITORING CHIP EXPECTS 1.8 VOLTS AT THE INPUT, SO THE 4.0 VOLTS IS DIVIDED.

NOTE 5 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 5 MILLIOHMS AND A CURRENT OF 5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LDO06C REGULATOR IS RATED FOR 6 AMPS. IF MORE THAN 5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 5 MILLIOHMS.

NOTE 6 V_4V0 IS ONLY CONNECTED ONTHIS PAGE, EXCEPT FOR MEASURING BY THE MCU ADC.

NOTE 7 THE TPS73601 REGULATOR SHOULD NOT BE ENABLED UNTIL THE FIREFLY TRANSMITTER TYPE HAS BEEN DETERMINED AND THE VOLTAGE SWITCH IS FOUND TO BE IN THE CORRECT POSITION.

NOTE 8 PULLDOWNS ARE NEEDED ON THE CONTROL INPUTS, SINCE THE I2C DRIVER DEVICES NEED TO BE CONFIGURED AS OUTPUTS BEFORE THEY CAN CONTOL THE LOGIC LEVEL. THE I2C DRIVERS HAVE A BUILT-IN 100K PULLUP.

NOTE 9 THE TPS73601 OUTPUT VOLTAGE IS CALCULATED BY:
VOUT = 1.204 * ((Rtop+Rbot)/Rbot)
IF Rtop = 60.4k AND Rbot=28K, THEN VOUT = 3.8 V

NOTE 10 THE SWITCH IS SHOWN IN THE POSITION TO PROVIDE 3.8 VOLTS TO THE FIREFLY TRANSMITTER. THE "*_3V8_SEL" SIGNAL WILL BE HIGH.

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.07: POWER FOR FF X12 XMIT		
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3.08: VOLT, CUR, TEMP MEASURE

TEST POINTS TO
MEASURE VOLTAGES

THE 12 VOLT SUPPLY
LEVEL IS DIVIDED BY 6

THE M3.3 VOLT SUPPLY
LEVEL IS DIVIDED BY 2

THE 3.3 VOLT SUPPLY
LEVEL IS DIVIDED BY 2

THE 4.0 VOLT SUPPLY
LEVEL IS DIVIDED BY 2

U68-5
TM4C1290NCPDT_NEW

VREFA+ 9
VDDA 8 → V_M3V3
GNDA 10 → GND

THE VALUE OF "MCU_VREFA" SETS THE VOLTAGE THAT WILL CORRESPOND TO THE ADC FULL SCALE VALUE OF 4095. THE MINIMUM VOLTAGE IS 2.4 VOLTS.

THIS DESIGN USES 2.5 VOLTS FOR FULL SCALE.

U65
LT1790-2.5V

V_M3V3 → C928 0.1 UF 0402 → GND
4 VIN
6 VOUT → MCU_VREFA
5 NC5
3 NC3
GND 2 → GND
GND 1 → GND
C117 1 UF 0402 10v → GND
C116 0.1 UF 0402 → GND

V_12V	PM5	R98 249 0805	R99 249 0805	R118 100 0402	C135 0.1 UF 0805 FILM
			R447 100 0402 → GND		
V_M3V3	PM6	R443 100 0402		R121 100 0402	C137 0.1 UF 0805 FILM
			R444 100 0402 → GND		
V_3V3	PM7	R439 100 0402		R125 100 0402	C154 0.1 UF 0805 FILM
			R440 100 0402 → GND		
V_4V0	PM2	R435 100 0402		R127 100 0402	C155 0.1 UF 0805 FILM
			R436 100 0402 → GND		
V_1V8	PM8			R92 100 0402	C41 0.1 UF 0805 FILM
V_F1_INT	PM18			R91 100 0402	C40 0.1 UF 0805 FILM
V_F1_AVCC	PM22			R90 100 0402	C39 0.1 UF 0805 FILM
V_F1_AVTT	PM23			R89 100 0402	C38 0.1 UF 0805 FILM
V_F1_VCCAUX	PM10			R88 100 0402	C37 0.1 UF 0805 FILM
V_F2_INT	PM17			R87 100 0402	C36 0.1 UF 0805 FILM
V_F2_AVCC	PM19			R86 100 0402	C35 0.1 UF 0805 FILM
V_F2_AVTT	PM20			R85 100 0402	C34 0.1 UF 0805 FILM
V_F2_VCCAUX	PM11			R104 100 0402	C98 0.1 UF 0805 FILM
CUR_V_12V 13	PM25			R102 100 0402	C94 0.1 UF 0805 FILM
CUR_V_M3V3 26	PM26			R96 100 0402	C75 0.1 UF 0805 FILM
CUR_V_4V0 32	PM4			R94 100 0402	C74 0.1 UF 0805 FILM
CUR_V_F1_VCCAUX 29	PM13			R130 100 0402	C173 0.1 UF 0805 FILM
CUR_F2_V_VCCAUX 31	PM12			R132 100 0402	C174 0.1 UF 0805 FILM
F1_TEMP_DIODE 45	PM14			R133 100 0402	C193 0.1 UF 0805 FILM
F2_TEMP_DIODE 55	PM15			R136 100 0402	C194 0.1 UF 0805 FILM

12	AIN_0	
13	AIN_1	
14	AIN_2	
15	AIN_3	
128	AIN_4	
127	AIN_5	
126	AIN_6	
125	AIN_7	
124	AIN_8	
123	AIN_9	
121	AIN_10	
120	AIN_11	
4	AIN_12	
3	AIN_13	
2	AIN_14	
1	AIN_15	
18	AIN_16	
19	AIN_17	
20	AIN_18	
21	AIN_19	

PM9 1 → GND
PM1 1 → GND
PM21 1 → GND
PM3 1 → GND
PM24 1 → GND
PM16 1 → GND

THE ANTI-ALIASING CUTOFF FREQUENCY IS 15.9 KHZ

A 16 MHZ ADC CLOCK PROVIDES A SAMPLING RATE OF 1 MEGA-SAMPLES PER SECOND. IF ALL 20 ADC CHANNELS ARE USED, THE SAMPLE RATE PER CHANNEL IS 50 KILO-SAMPLES PER SECOND, AND THE NYQUIST FREQUENCY IS 25 KHZ.

THE MAXIMUM SOURCE IMPEDANCE FEEDING THE ADC INPUTS IS 500 OHMS.

APOLLO CM W/ DUAL A2577, MK1

Title: 3.08: VOLT, CUR, TEMP MEASURE

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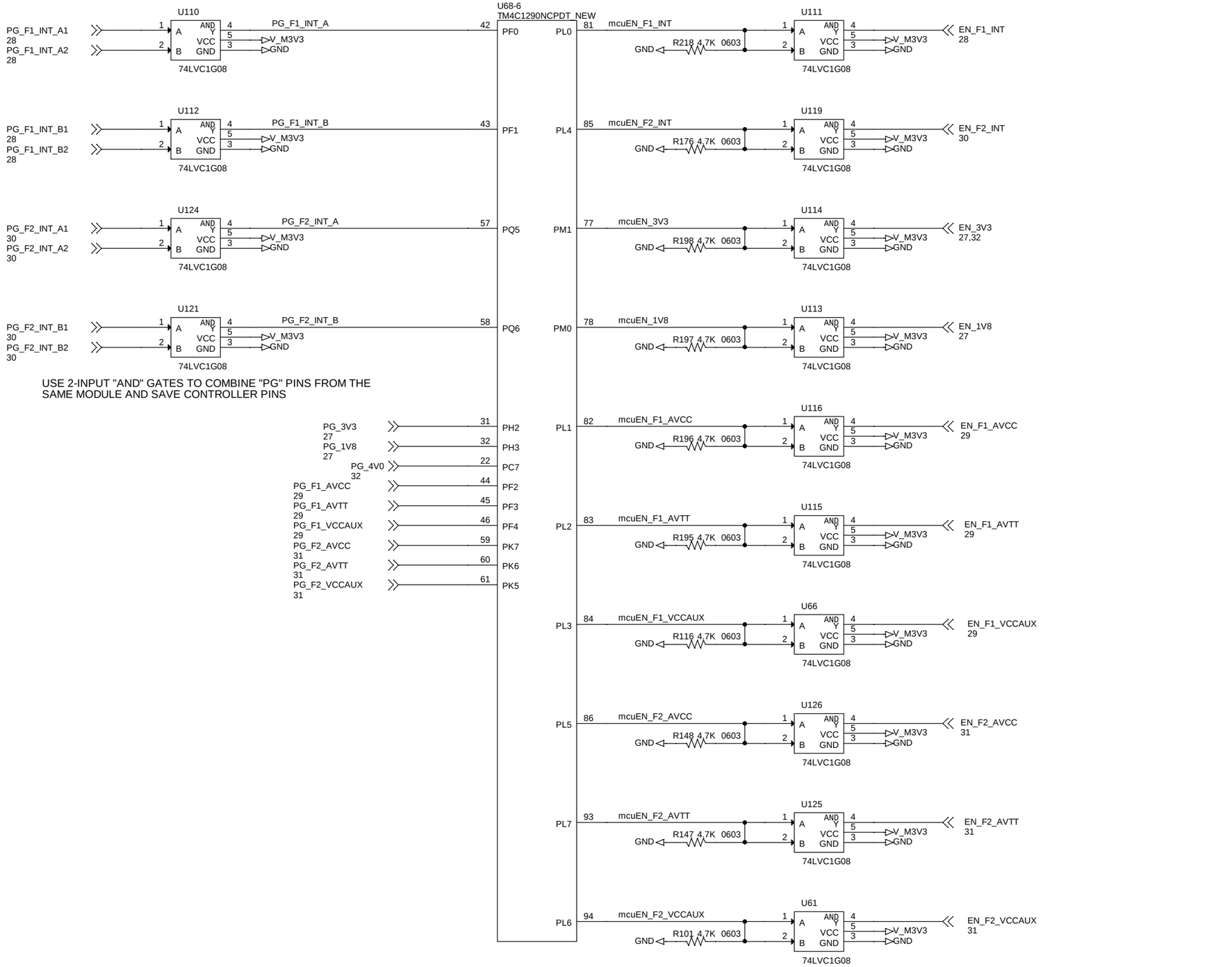
3.09: POWER CONTROL



THE ACTIVE-HI "ENABLE" SIGNALS WILL ONLY BE ASSERTED WHEN V_M3V3 IS PRESENT AND THE CONTROLLER OUTPUT IS HIGH. OTHERWISE, PULLDOWN RESISTORS ON THE GATE INPUT AND THE POWER MODULE INPUT WILL KEEP THE ENABLE SIGNALS LOW.

APOLLO CM W/ DUAL A2577, MK1		
Title: 3.09: POWER CONTROL		
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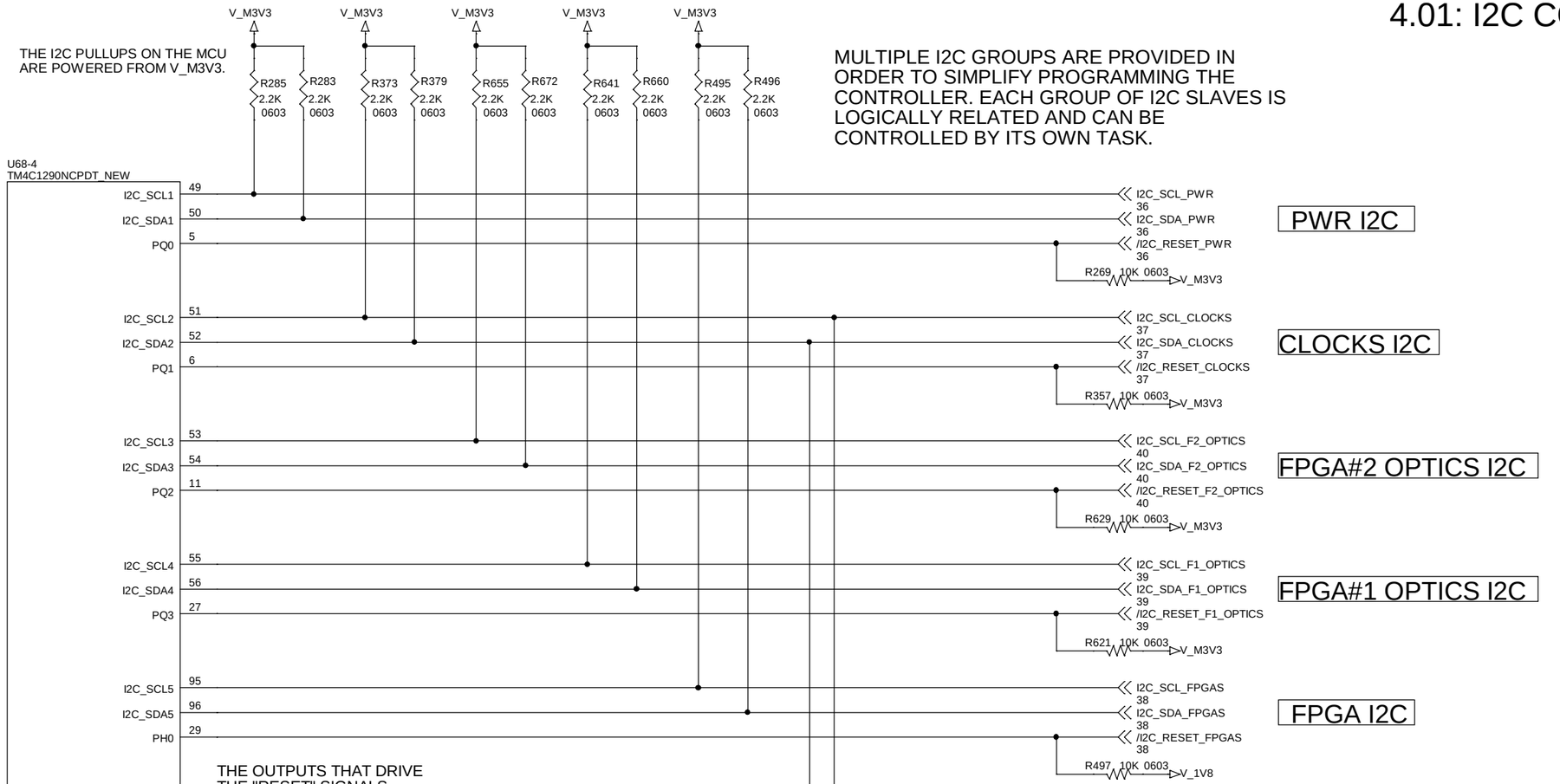
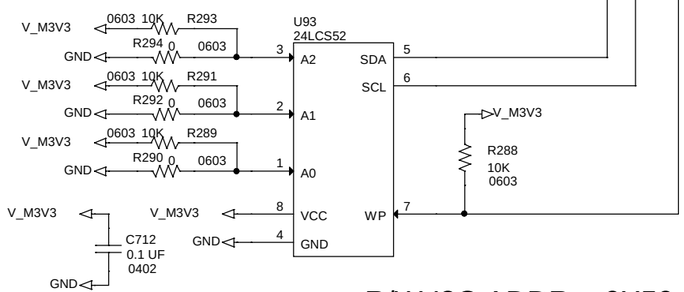
4.01: I2C CONTROLLER

THE I2C PULLUPS ON THE MCU ARE POWERED FROM V_M3V3.

MULTIPLE I2C GROUPS ARE PROVIDED IN ORDER TO SIMPLIFY PROGRAMMING THE CONTROLLER. EACH GROUP OF I2C SLAVES IS LOGICALLY RELATED AND CAN BE CONTROLLED BY ITS OWN TASK.



THE OUTPUTS THAT DRIVE THE "RESET" SIGNALS NEED TO BE OPEN-DRAIN.



THIS EEPROM IS FOR STORING UNCHANGING INFORMATION, LIKE SERIAL NUMBERS OR OTHER BOARD IDENTIFIERS.

THE EEPROM IS CONNECTED TO THE I2C BUS THAT RUNS THE CLOCKING CHIPS.

R/W I2C ADDR = 0X50

WP I2C ADDR = 0X30

24LCS52 I2C ADDRESS:
READ OR WRITE
1 0 1 0 A2 A1 A0
RANGE: 0X50 TO 0X57
WRITE-PROTECT REGISTER
0 1 1 0 A2 A1 A0

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

APOLLO CM W/ DUAL A2577, MK1		
Title: 4.01: I2C CONTROLLER		
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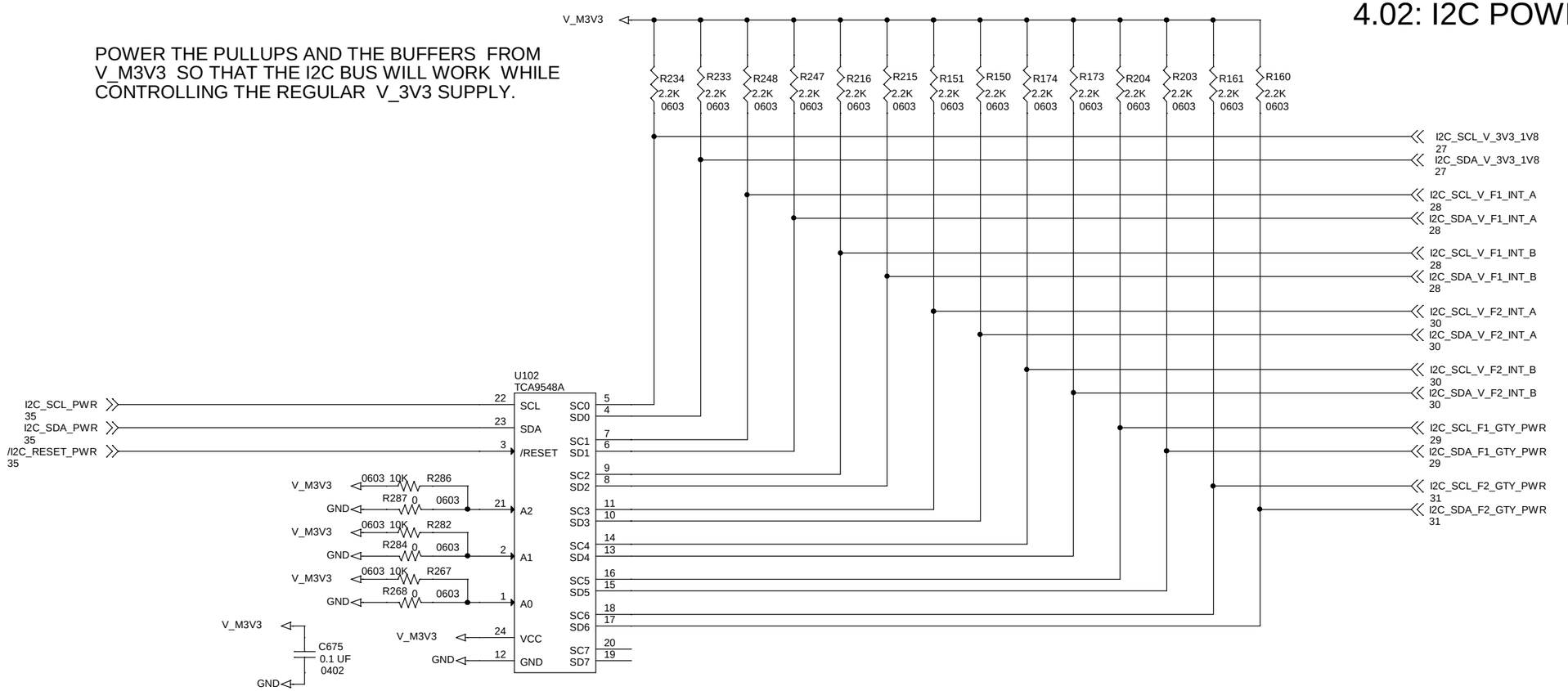
4.02: I2C POWER CONTROL

POWER THE PULLUPS AND THE BUFFERS FROM V_M3V3 SO THAT THE I2C BUS WILL WORK WHILE CONTROLLING THE REGULAR V_3V3 SUPPLY.



I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

APOLLO CM W/ DUAL A2577, MK1		
Title: 4.02: I2C POWER CONTROL		
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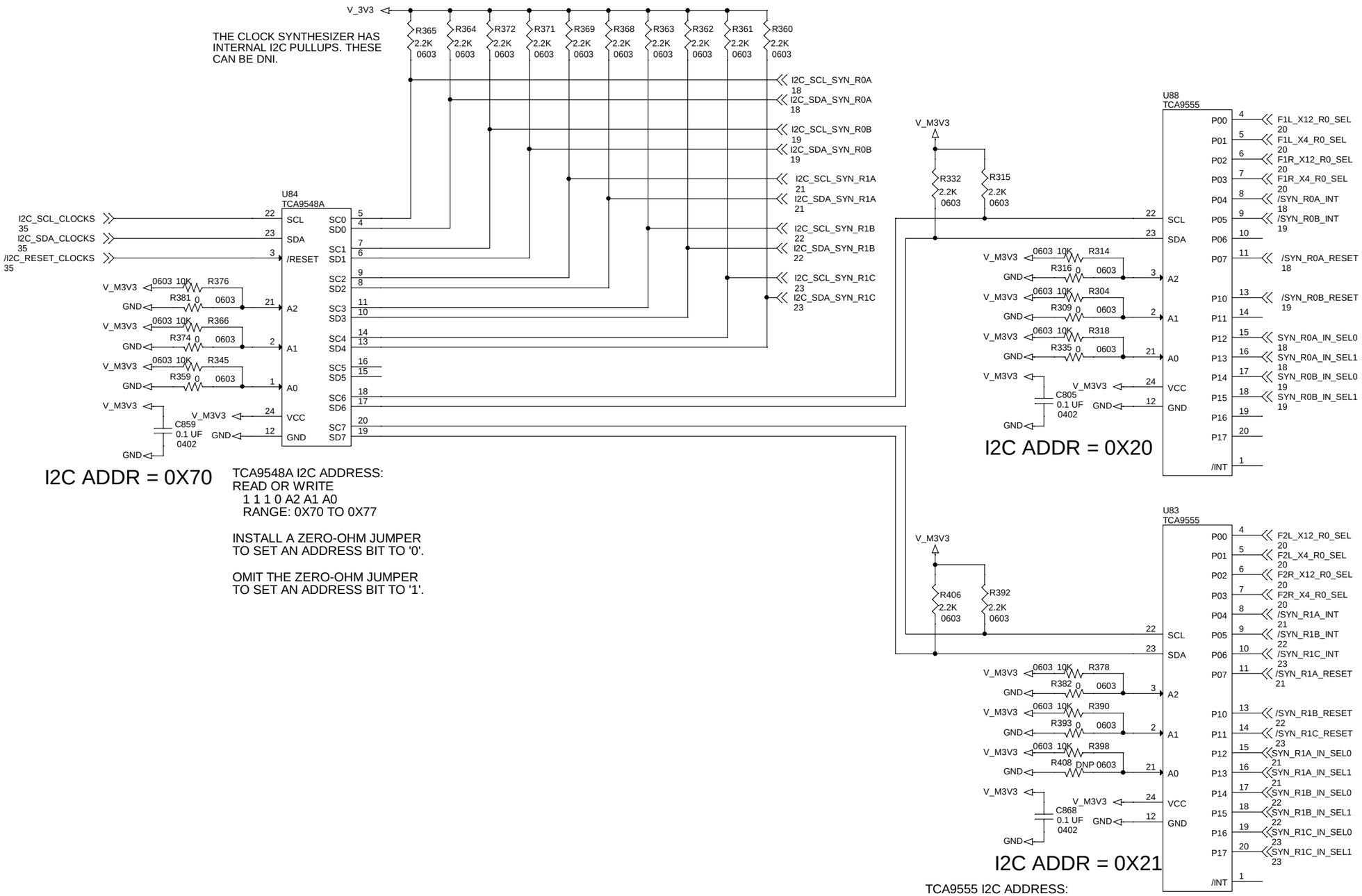
4.03: I2C CLOCK CONTROL



APOLLO CM W/ DUAL A2577, MK1		
Title: 4.03: I2C CLOCK CONTROL		
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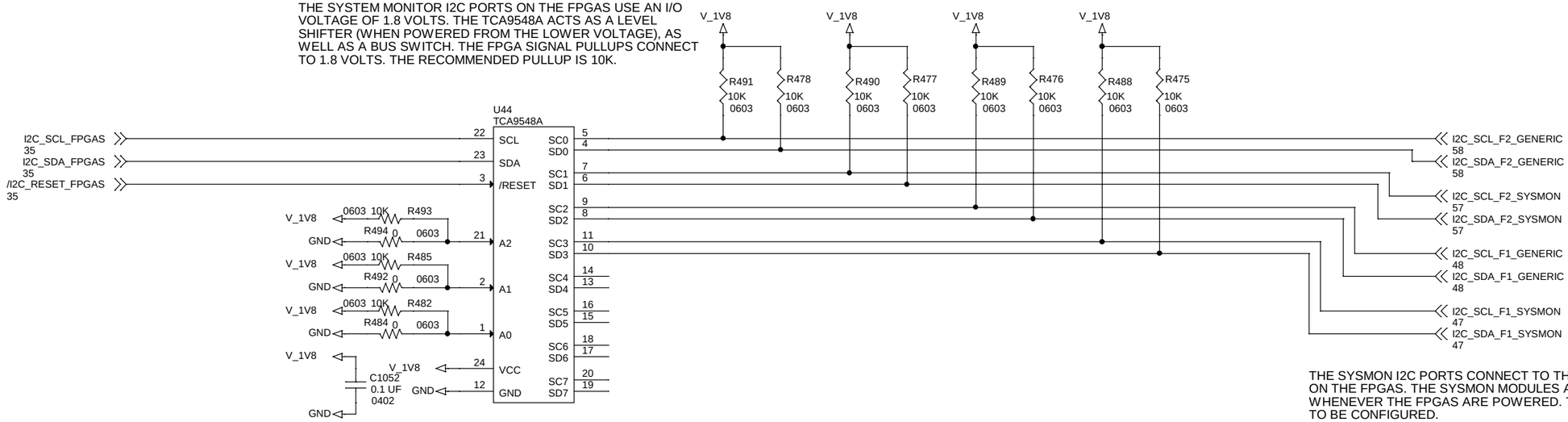
4.04: I2C FPGA INTERNALS

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER (WHEN POWERED FROM THE LOWER VOLTAGE), AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS. THE RECOMMENDED PULLUP IS 10K.



I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

THE SYSMON I2C PORTS CONNECT TO THE SYSMON MODULE PINS ON THE FPGAS. THE SYSMON MODULES ARE AVAILABLE WHENEVER THE FPGAS ARE POWERED. THE FPGAS DO NOT HAVE TO BE CONFIGURED.

THE GENERIC I2C PORTS CONNECT TO I2C MODULES THAT ARE LOADED AS PART OF THE CONFIGURATION PROCESS. THEY ARE NOT AVAILABLE BEFORE THE FPGA HAS BEEN CONFIGURED.

THE GENERIC MODULES HAVE MORE CAPABILITY THAN THE SYSMON MODULES.

A2	A1	A0	I2C BUS SLAVE ADDRESS
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

APOLLO CM W/ DUAL A2577, MK1

Title: 4.04: I2C FPGA INTERNALS

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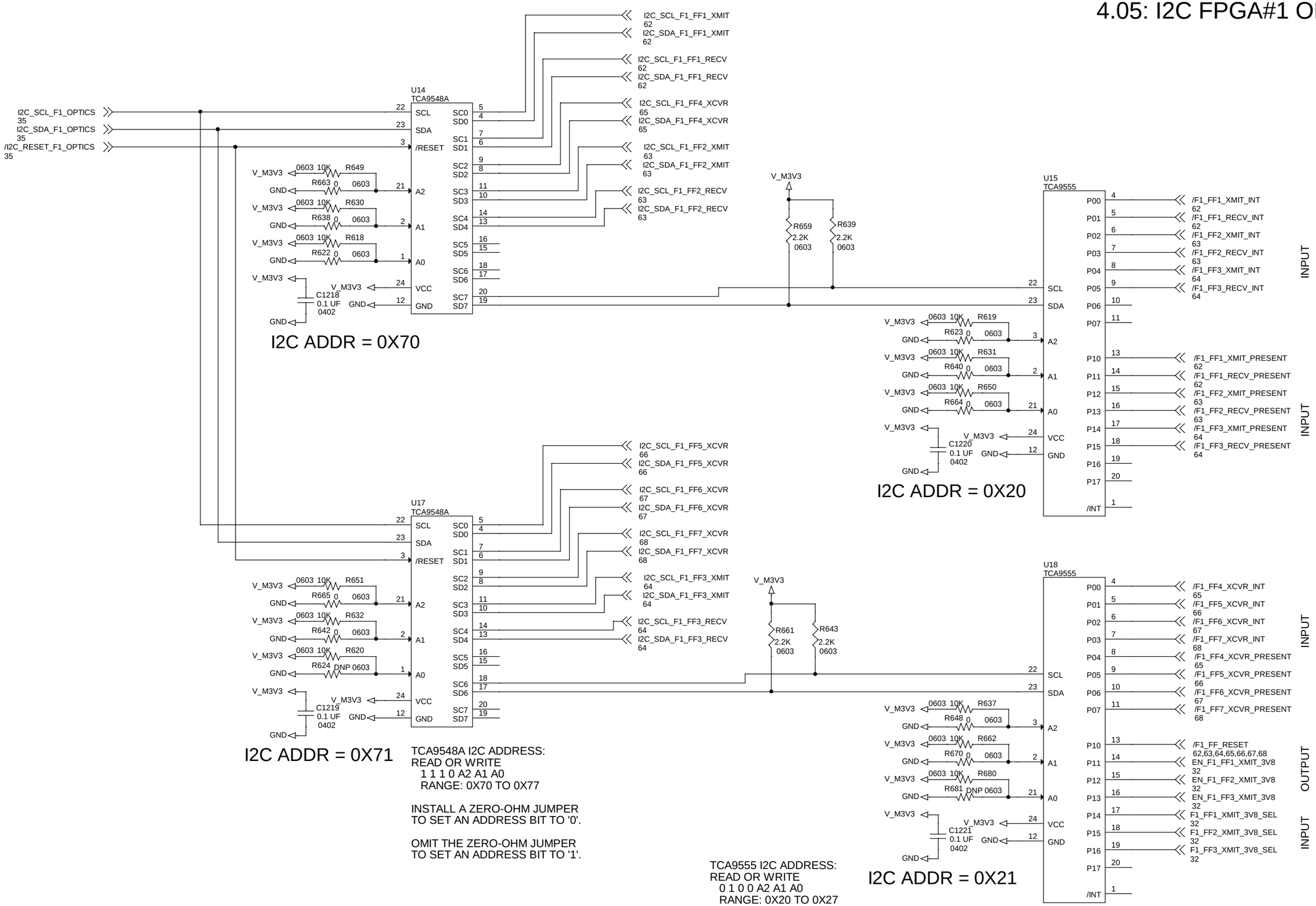
4.05: I2C FPGA#1 OPTICS



APOLLO CM W/ DUAL A2577, MK1		
Title: 4.05: I2C FPGA#1 OPTICS		
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4.06: I2C FPGA#2 OPTICS

I2C_SCL_F2_OPTICS 35
I2C_SDA_F2_OPTICS 35
/I2C_RESET_F2_OPTICS 35

U9 TCA9548A

SCL, SDA, /RESET, A2, A1, A0, VCC, GND

SC0/SD0 → I2C_SCL_F2_FF1_XMIT 71 / I2C_SDA_F2_FF1_XMIT 71
SC1/SD1 → I2C_SCL_F2_FF1_RECV 71 / I2C_SDA_F2_FF1_RECV 71
SC2/SD2 → I2C_SCL_F2_FF4_XCVR 74 / I2C_SDA_F2_FF4_XCVR 74
SC3/SD3 → I2C_SCL_F2_FF2_XMIT 72 / I2C_SDA_F2_FF2_XMIT 72
SC4/SD4 → I2C_SCL_F2_FF2_RECV 72 / I2C_SDA_F2_FF2_RECV 72
SC5/SD5 → (DNP)
SC6/SD6 → (DNP)
SC7/SD7 → I2C_SCL_F2_FF5_XCVR 75 / I2C_SDA_F2_FF5_XCVR 75

V_M3V3 — 0603 10K R666 — R676 0 0603 — GND → A2
V_M3V3 — 0603 10K R644 — R652 0 0603 — GND → A1
V_M3V3 — 0603 10K R625 — R633 0 0603 — GND → A0
V_M3V3 → VCC
C1222 0.1 UF 0402 (V_M3V3 / GND)

I2C ADDR = 0X70

U10 TCA9555

V_M3V3 → R671 2.2K 0603 / R653 2.2K 0603

SCL, SDA

V_M3V3 — 0603 10K R626 — R634 0 0603 — GND → A2
V_M3V3 — 0603 10K R645 — R654 0 0603 — GND → A1
V_M3V3 — 0603 10K R667 — R677 0 0603 — GND → A0
V_M3V3 → VCC
C1223 0.1 UF 0402 (V_M3V3 / GND)

I2C ADDR = 0X20

INPUT
P00 → /F2_FF1_XMIT_INT 71
P01 → /F2_FF1_RECV_INT 71
P02 → /F2_FF2_XMIT_INT 72
P03 → /F2_FF2_RECV_INT 72
P04 → /F2_FF3_XMIT_INT 73
P05 → /F2_FF3_RECV_INT 73

INPUT
P10 → /F2_FF1_XMIT_PRESENT 71
P11 → /F2_FF1_RECV_PRESENT 71
P12 → /F2_FF2_XMIT_PRESENT 72
P13 → /F2_FF2_RECV_PRESENT 72
P14 → /F2_FF3_XMIT_PRESENT 73
P15 → /F2_FF3_RECV_PRESENT 73
P16
P17
/INT

U11 TCA9548A

SCL, SDA, /RESET, A2, A1, A0, VCC, GND

SC0/SD0 → I2C_SCL_F2_FF6_XCVR 76 / I2C_SDA_F2_FF6_XCVR 76
SC1/SD1 → I2C_SCL_F2_FF7_XCVR 77 / I2C_SDA_F2_FF7_XCVR 77
SC2/SD2 → I2C_SCL_F2_FF3_XMIT 73 / I2C_SDA_F2_FF3_XMIT 73
SC3/SD3 → I2C_SCL_F2_FF3_RECV 73 / I2C_SDA_F2_FF3_RECV 73
SC4/SD4 → (DNP)
SC5/SD5 → (DNP)
SC6/SD6 → (DNP)
SC7/SD7 → (DNP)

V_M3V3 — 0603 10K R668 — R678 0 0603 — GND → A2
V_M3V3 — 0603 10K R646 — R656 0 0603 — GND → A1
V_M3V3 — 0603 10K R627 — R635 DNP 0603 — GND → A0
V_M3V3 → VCC
C1224 0.1 UF 0402 (V_M3V3 / GND)

I2C ADDR = 0X71

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

V_M3V3 → R673 2.2K 0603 / R657 2.2K 0603

U12 TCA9555

SCL, SDA

V_M3V3 — 0603 10K R628 — R636 0 0603 — GND → A2
V_M3V3 — 0603 10K R647 — R658 0 0603 — GND → A1
V_M3V3 — 0603 10K R669 — R679 DNP 0603 — GND → A0
V_M3V3 → VCC
C1225 0.1 UF 0402 (V_M3V3 / GND)

I2C ADDR = 0X21

INPUT
P00 → /F2_FF4_XCVR_INT 74
P01 → /F2_FF5_XCVR_INT 75
P02 → /F2_FF6_XCVR_INT 76
P03 → /F2_FF7_XCVR_INT 77
P04 → /F2_FF4_XCVR_PRESENT 74
P05 → /F2_FF5_XCVR_PRESENT 75
P06 → /F2_FF6_XCVR_PRESENT 76
P07 → /F2_FF7_XCVR_PRESENT 77

OUTPUT
P10 → /F2_FF_RESET 71,72,73,74,75,76,77
P11 → EN_F2_FF1_XMIT_3V8 32
P12 → EN_F2_FF2_XMIT_3V8 32
P13 → EN_F2_FF3_XMIT_3V8 32

INPUT
P14 → F2_FF1_XMIT_3V8_SEL 32
P15 → F2_FF2_XMIT_3V8_SEL 32
P16 → F2_FF3_XMIT_3V8_SEL 32
P17
/INT

TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

APOLLO CM W/ DUAL A2577, MK1		
Title: 4.06: I2C FPGA#2 OPTICS		
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5.01: FPGA#1 GND

U75-1 FPGA_VU13P_A2577

A13	GND	GND	AE12
A16	GND	GND	AE16
A17	GND	GND	AE18
A18	GND	GND	AE20
A21	GND	GND	AE22
A26	GND	GND	AE24
A31	GND	GND	AE26
A34	GND	GND	AE28
A35	GND	GND	AE3
A36	GND	GND	AE30
A39	GND	GND	AE32
A4	GND	GND	AE34
A43	GND	GND	AE36
A45	GND	GND	AE38
A48	GND	GND	AE4
A7	GND	GND	AE40
A9	GND	GND	AE43
AA12	GND	GND	AE47
AA14	GND	GND	AE48
AA16	GND	GND	AE49
AA18	GND	GND	AE5
AA20	GND	GND	AE9
AA22	GND	GND	AF1
AA24	GND	GND	AF10
AA26	GND	GND	AF12
AA28	GND	GND	AF15
AA3	GND	GND	AF17
AA30	GND	GND	AF19
AA32	GND	GND	AF2
AA34	GND	GND	AF21
AA36	GND	GND	AF23
AA38	GND	GND	AF25
AA4	GND	GND	AF27
AA40	GND	GND	AF29
AA43	GND	GND	AF31
AA47	GND	GND	AF33
AA48	GND	GND	AF35
AA49	GND	GND	AF37
AA5	GND	GND	AF39
AA9	GND	GND	AF40
AB1	GND	GND	AF42
AB10	GND	GND	AF45
AB15	GND	GND	AF47
AB17	GND	GND	AF5
AB19	GND	GND	AF50
AB2	GND	GND	AF51
AB21	GND	GND	AF7
AB23	GND	GND	AG12
AB25	GND	GND	AG16
AB27	GND	GND	AG20
AB29	GND	GND	AG22
AB31	GND	GND	AG24
AB33	GND	GND	AG26
AB35	GND	GND	AG28
AB37	GND	GND	AG3
AB38	GND	GND	AG30
AB42	GND	GND	AG32
AB45	GND	GND	AG34
AB47	GND	GND	AG36
AB5	GND	GND	AG38
AB50	GND	GND	AG4
AB51	GND	GND	AG40
AB7	GND	GND	AG44
AC14	GND	GND	AG47
AC16	GND	GND	AG48
AC18	GND	GND	AG49
AC20	GND	GND	AG5
AC22	GND	GND	AG8
AC24	GND	GND	AH1
AC26	GND	GND	AH11
AC28	GND	GND	AH12
AC3	GND	GND	AH15
AC30	GND	GND	AH17
AC32	GND	GND	AH2
AC34	GND	GND	AH21
AC36	GND	GND	AH23
AC38	GND	GND	AH25
AC39	GND	GND	AH27
AC4	GND	GND	AH29
AC44	GND	GND	AH31
AC47	GND	GND	AH33
AC48	GND	GND	AH35
AC49	GND	GND	AH37
AC5	GND	GND	AH39
AC8	GND	GND	AH40
AD1	GND	GND	AH41
AD11	GND	GND	AH46
AD12	GND	GND	AH47
AD15	GND	GND	AH5
AD17	GND	GND	AH50
AD19	GND	GND	AH51
AD2	GND	GND	AH6
AD21	GND	GND	AJ14
AD23	GND	GND	AJ16
AD25	GND	GND	AJ20
AD27	GND	GND	AJ22
AD29	GND	GND	AJ24
AD31	GND	GND	AJ26
AD33	GND	GND	AJ28
AD35	GND	GND	AJ3
AD37	GND	GND	AJ30
AD39	GND	GND	AJ32
AD40	GND	GND	AJ34
AD41	GND	GND	AJ36
AD46	GND	GND	AJ38
AD47	GND	GND	AJ39
AD5	GND	GND	AJ47
AD50	GND	GND	AJ43
AD51	GND	GND	AJ48
AD6	GND	GND	AJ4

GND GND

U75-2 FPGA_VU13P_A2577

AJ49	GND	GND	AP42
AJ5	GND	GND	AP45
AJ9	GND	GND	AP47
AK1	GND	GND	AP5
AK10	GND	GND	AP50
AK15	GND	GND	AP51
AK17	GND	GND	AP7
AK2	GND	GND	AR12
AK21	GND	GND	AR14
AK23	GND	GND	AR22
AK25	GND	GND	AR24
AK27	GND	GND	AR26
AK29	GND	GND	AR28
AK31	GND	GND	AR3
AK33	GND	GND	AR30
AK35	GND	GND	AR38
AK37	GND	GND	AR4
AK38	GND	GND	AR40
AK42	GND	GND	AR44
AK45	GND	GND	AR47
AK47	GND	GND	AR48
AK5	GND	GND	AR49
AK50	GND	GND	AR5
AK51	GND	GND	AR8
AK7	GND	GND	AT1
AL12	GND	GND	AT11
AL14	GND	GND	AT2
AL16	GND	GND	AT21
AL18	GND	GND	AT23
AL20	GND	GND	AT25
AL22	GND	GND	AT27
AL24	GND	GND	AT29
AL26	GND	GND	AT31
AL28	GND	GND	AT38
AL3	GND	GND	AT41
AL30	GND	GND	AT46
AL32	GND	GND	AT47
AL34	GND	GND	AT5
AL36	GND	GND	AT50
AL38	GND	GND	AT51
AL4	GND	GND	AT6
AL40	GND	GND	AU13
AL44	GND	GND	AU14
AL47	GND	GND	AU18
AL48	GND	GND	AU24
AL49	GND	GND	AU26
AL5	GND	GND	AU28
AL8	GND	GND	AU3
AM1	GND	GND	AU30
AM11	GND	GND	AU38
AM15	GND	GND	AU39
AM17	GND	GND	AU4
AM19	GND	GND	AU43
AM2	GND	GND	AU47
AM21	GND	GND	AU48
AM23	GND	GND	AU49
AM25	GND	GND	AU5
AM27	GND	GND	AU9
AM29	GND	GND	AV1
AM31	GND	GND	AV10
AM33	GND	GND	AV15
AM35	GND	GND	AV2
AM37	GND	GND	AV25
AM38	GND	GND	AV35
AM41	GND	GND	AV38
AM46	GND	GND	AV42
AM47	GND	GND	AV45
AM5	GND	GND	AV47
AM50	GND	GND	AV5
AM51	GND	GND	AV50
AM6	GND	GND	AV51
AN12	GND	GND	AV7
AN14	GND	GND	AW12
AN16	GND	GND	AW14
AN18	GND	GND	AW22
AN20	GND	GND	AW3
AN22	GND	GND	AW32
AN24	GND	GND	AW38
AN26	GND	GND	AW4
AN28	GND	GND	AW40
AN3	GND	GND	AW44
AN30	GND	GND	AW47
AN32	GND	GND	AW48
AN34	GND	GND	AW49
AN36	GND	GND	AW5
AN38	GND	GND	AW8
AN4	GND	GND	AY1
AN40	GND	GND	AY11
AN43	GND	GND	AY19
AN47	GND	GND	AY2
AN48	GND	GND	AY29
AN49	GND	GND	AY38
AN5	GND	GND	AY41
AN9	GND	GND	AY46
AP1	GND	GND	AY47
AP10	GND	GND	AY5
AP15	GND	GND	AY50
AP17	GND	GND	AY51
AP19	GND	GND	AY6
AP2	GND	GND	B10
AP21	GND	GND	B14
AP23	GND	GND	B16
AP25	GND	GND	B19
AP27	GND	GND	B20
AP29	GND	GND	B21
AP31	GND	GND	B23
AP33	GND	GND	B3
AP35	GND	GND	B31
AP37	GND	GND	B32
AP38	GND	GND	B33

GND GND

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B36	GND	GND	BG12
B38	GND	GND	BG16
B4	GND	GND	BG17
B42	GND	GND	BG18
B45	GND	GND	BG21
B46	GND	GND	BG28
B47	GND	GND	BG3
B48	GND	GND	BG31
B49	GND	GND	BG34
B5	GND	GND	BG35
B6	GND	GND	BG36
B7	GND	GND	BG4
BA12	GND	GND	BG40
BA14	GND	GND	BG44
BA16	GND	GND	BG45
BA26	GND	GND	BG48
BA3	GND	GND	BG49
BA36	GND	GND	BG7
BA38	GND	GND	BG8
BA4	GND	GND	BH1
BA40	GND	GND	BH11
BA43	GND	GND	BH15
BA47	GND	GND	BH16
BA48	GND	GND	BH19
BA49	GND	GND	BH2
BA5	GND	GND	BH20
BA9	GND	GND	BH21
BB1	GND	GND	BH25
BB10	GND	GND	BH31
BB2	GND	GND	BH32
BB23	GND	GND	BH33
BB33	GND	GND	BH36
BB38	GND	GND	BH37
BB42	GND	GND	BH41
BB45	GND	GND	BH45
BB47	GND	GND	BH46
BB5	GND	GND	BH47
BB50	GND	GND	BH5
BB51	GND	GND	BH50
BB7	GND	GND	BH51
BC12	GND	GND	BH6
BC14	GND	GND	BH7
BC20	GND	GND	BJ13
BC3	GND	GND	BJ16
BC30	GND	GND	BJ17
BC38	GND	GND	BJ18
BC4	GND	GND	BJ2
BC40	GND	GND	BJ21
BC44	GND	GND	BJ22
BC47	GND	GND	BJ3
BC48	GND	GND	BJ31
BC49	GND	GND	BJ34
BC5	GND	GND	BJ35
BC8	GND	GND	BJ36
BD1	GND	GND	BJ39
BD11	GND	GND	BJ4
BD14	GND	GND	BJ43
BD2	GND	GND	BJ45
BD27	GND	GND	BJ48
BD38	GND	GND	BJ49
BD41	GND	GND	BJ50
BD46	GND	GND	BJ7
BD47	GND	GND	BJ9
BD5	GND	GND	BK10
BD50	GND	GND	BK14
BD51	GND	GND	BK16
BD6	GND	GND	BK19
BE12	GND	GND	BK20
BE14	GND	GND	BK21
BE15	GND	GND	BK29
BE16	GND	GND	BK3
BE17	GND	GND	BK31
BE18	GND	GND	BK32
BE19	GND	GND	BK33
BE24	GND	GND	BK36
BE3	GND	GND	BK38
BE33	GND	GND	BK4
BE34	GND	GND	BK42
BE35	GND	GND	BK45
BE36	GND	GND	BK46
BE37	GND	GND	BK47
BE38	GND	GND	BK48
BE4	GND	GND	BK49
BE40	GND	GND	BK5
BE43	GND	GND	BK6
BE47	GND	GND	BK7
BE48	GND	GND	BL12
BE49	GND	GND	BL16
BE5	GND	GND	BL17
BE9	GND	GND	BL18
BF1	GND	GND	BL21
BF10	GND	GND	BL26
BF16	GND	GND	BL31
BF19	GND	GND	BL34
BF2	GND	GND	BL35
BF20	GND	GND	BL36
BF21	GND	GND	BL4
BF31	GND	GND	BL40
BF32	GND	GND	BL44
BF33	GND	GND	BL45
BF36	GND	GND	BL48
BF42	GND	GND	BL7
BF45	GND	GND	BL8
BF46	GND	GND	C12
BF47	GND	GND	C16
BF5	GND	GND	C17
BF50	GND	GND	C18
BF51	GND	GND	C2
BF6	GND	GND	C21
BF7	GND	GND	C3

GND GND

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C31	GND	GND	H35
C34	GND	GND	H36
C35	GND	GND	H37
C36	GND	GND	H38
C4	GND	GND	H41
C40	GND	GND	H46
C44	GND	GND	H47
C45	GND	GND	H5
C48	GND	GND	H50
C49	GND	GND	H51
C50	GND	GND	H6
C7	GND	GND	J12
C8	GND	GND	J14
D1	GND	GND	J22
D11	GND	GND	J3
D15	GND	GND	J38
D16	GND	GND	J4
D19	GND	GND	J40
D2	GND	GND	J43
D20	GND	GND	J47
D21	GND	GND	J48
D27	GND	GND	J49
D31	GND	GND	J5
D32	GND	GND	J9
D33	GND	GND	K1
D36	GND	GND	K10
D37	GND	GND	K14
D41	GND	GND	K19
D45	GND	GND	K2
D46	GND	GND	K29
D47	GND	GND	K38
D5	GND	GND	K42
D50	GND	GND	K45
D51	GND	GND	K47
D6	GND	GND	K5
D7	GND	GND	K50
E12	GND	GND	K51
E16	GND	GND	K7
E17	GND	GND	L12
E18	GND	GND	L14
E21	GND	GND	L16
E24	GND	GND	L26
E3	GND	GND	L3
E31	GND	GND	L36
E34	GND	GND	L38
E35	GND	GND	L4
E36	GND	GND	L40
E39	GND	GND	L44
E4	GND	GND	L47
E43	GND	GND	L48
E45	GND	GND	L49
E48	GND	GND	L5
E49	GND	GND	L8
E7	GND	GND	M1
E9	GND	GND	M11
F1	GND	GND	M2
F10	GND	GND	M23
F14	GND	GND	M33
F16	GND	GND	M38
F19	GND	GND	M41
F2	GND	GND	M46
F20	GND	GND	M47
F21	GND	GND	M5
F31	GND	GND	M50
F32	GND	GND	M51
F33	GND	GND	M6
F36	GND	GND	N13
F38	GND	GND	N14
F42	GND	GND	N20
F45	GND	GND	N3
F46	GND	GND	N30
F47	GND	GND	N38
F5	GND	GND	N39
F50	GND	GND	N4
F51	GND	GND	N43
F6	GND	GND	N47
F7	GND	GND	N48
G12	GND	GND	N49
G16	GND	GND	N5
G18	GND	GND	N9
G21	GND	GND	P1
G28	GND	GND	P10
G3	GND	GND	P17
G31	GND	GND	P2
G34	GND	GND	P27
G36	GND	GND	P37
G4	GND	GND	P38
G40	GND	GND	P42
G44	GND	GND	P45
G47	GND	GND	P47
G48	GND	GND	P5
G49	GND	GND	P50
G5	GND	GND	P51
G8	GND	GND	P7
H1	GND	GND	R12
H11	GND	GND	R14
H14	GND	GND	R24
H15	GND	GND	R3
H16	GND	GND	R34
H17	GND	GND	R38
H18	GND	GND	R4
H19	GND	GND	R40
H2	GND	GND	R44
H20	GND	GND	R47
H21	GND	GND	R48
H25	GND	GND	R49
H31	GND	GND	R5
H32	GND	GND	R8
H33	GND	GND	T1
H34	GND	GND	T11

GND GND

U75-5 FPGA_VU13P_A2577

T2	GND
T21	GND
T38	GND
T41	GND
T46	GND
T47	GND
T5	GND
T50	GND
T51	GND
T6	GND
U13	GND
U14	GND
U18	GND
U28	GND
U3	GND
U30	GND
U38	GND
U39	GND
U4	GND
U43	GND
U47	GND
U48	GND
U49	GND
U5	GND
U9	GND
V1	GND
V10	GND
V2	GND
V23	GND
V25	GND
V27	GND
V29	GND
V31	GND
V38	GND
V42	GND
V45	GND
V47	GND
V5	GND
V50	GND
V51	GND
V7	GND
W12	GND
W14	GND
W18	GND
W20	GND
W22	GND
W24	GND
W26	GND
W28	GND
W3	GND
W30	GND
W34	GND
W36	GND
W38	GND
W4	GND
W40	GND
W44	GND
W47	GND
W48	GND
W49	GND
W5	GND
W8	GND
Y1	GND
Y11	GND
Y15	GND
Y17	GND
Y19	GND
Y2	GND
Y21	GND
Y23	GND
Y25	GND
Y27	GND
Y29	GND
Y31	GND
Y33	GND
Y35	GND
Y37	GND
Y38	GND
Y41	GND
Y46	GND
Y47	GND
Y5	GND
Y50	GND
Y51	GND

GND

R454 10K 0603

V_M3V3

Y6

GND

/F1_INSTALLED
24

IF THE FPGA IS INSTALLED, THEN THE ACTIVE-LO "/F1_INSTALLED" SIGNAL WILL BE PULLED TO GND. IF THE FPGA IS NOT INSTALLED, THE SIGNAL WILL BE HI.

ANY FPGA GND PIN CAN BE USED.

APOLLO CM W/ DUAL A2577, MK1

Title: 5.01: FPGA#1 GND

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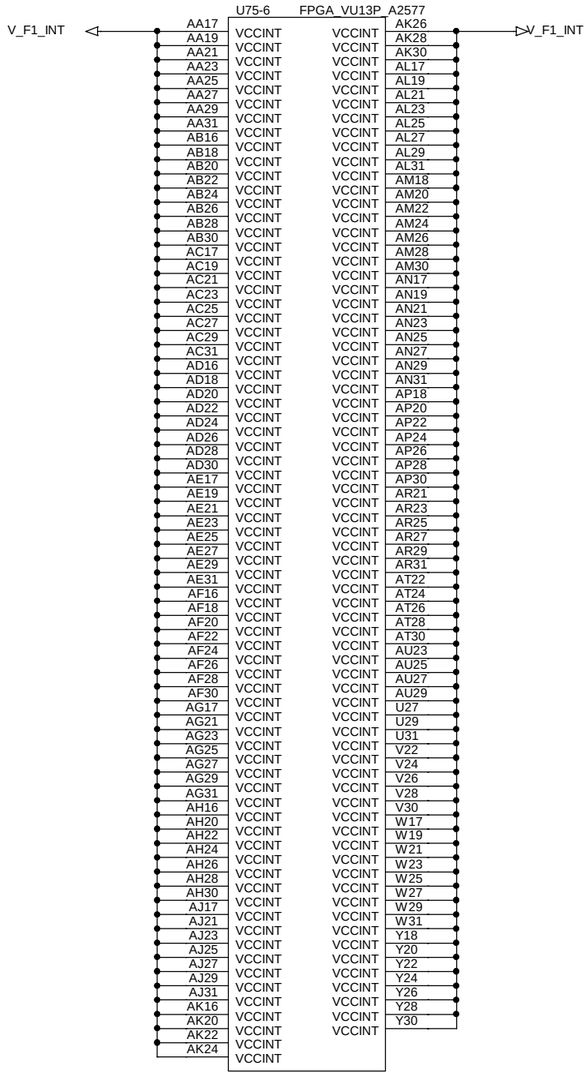
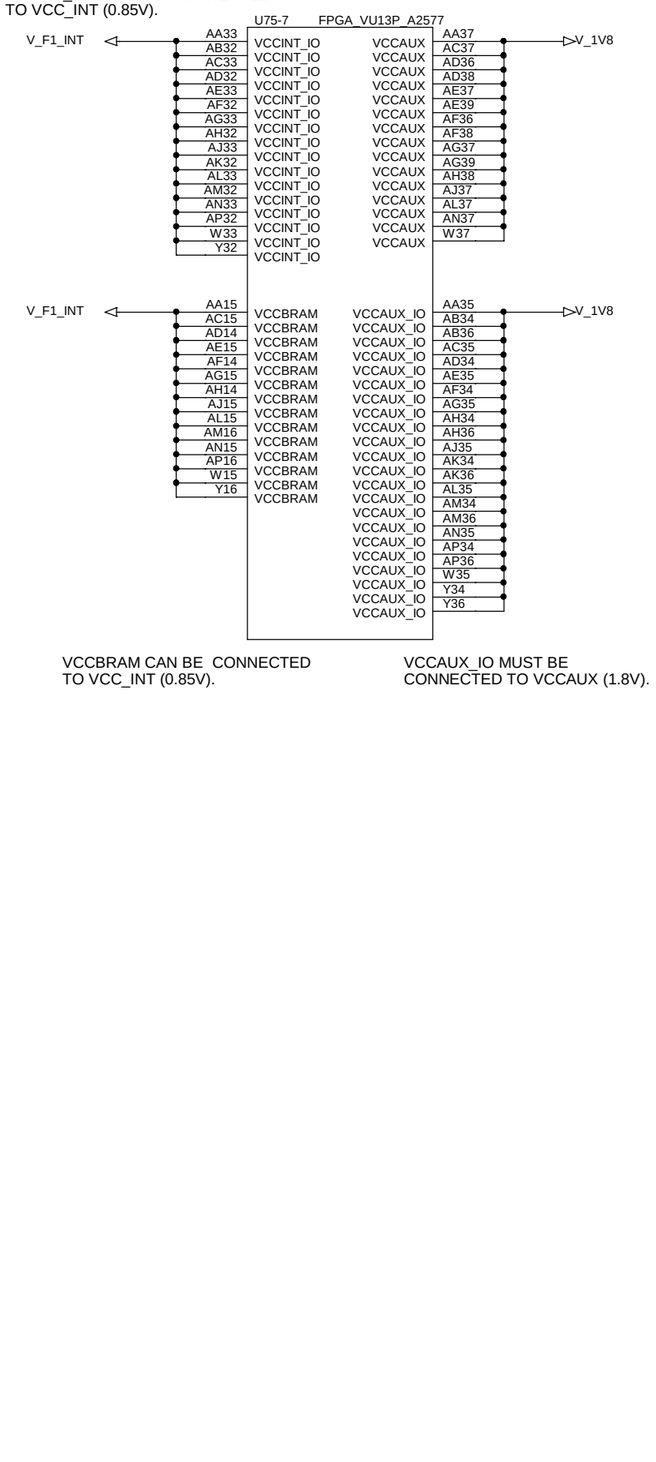
5.02: FPGA#1 POWER INTERNAL

VCCINT MUST BE 0.85V.

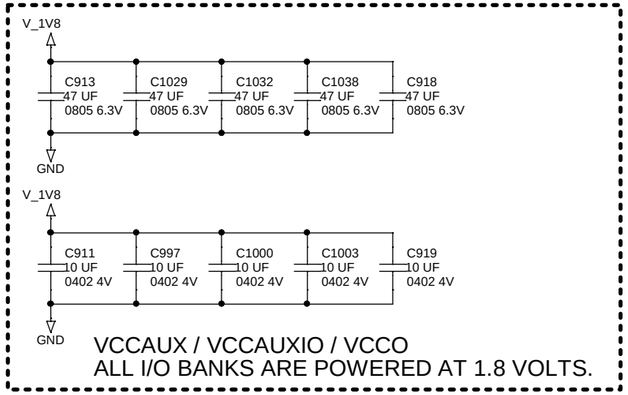


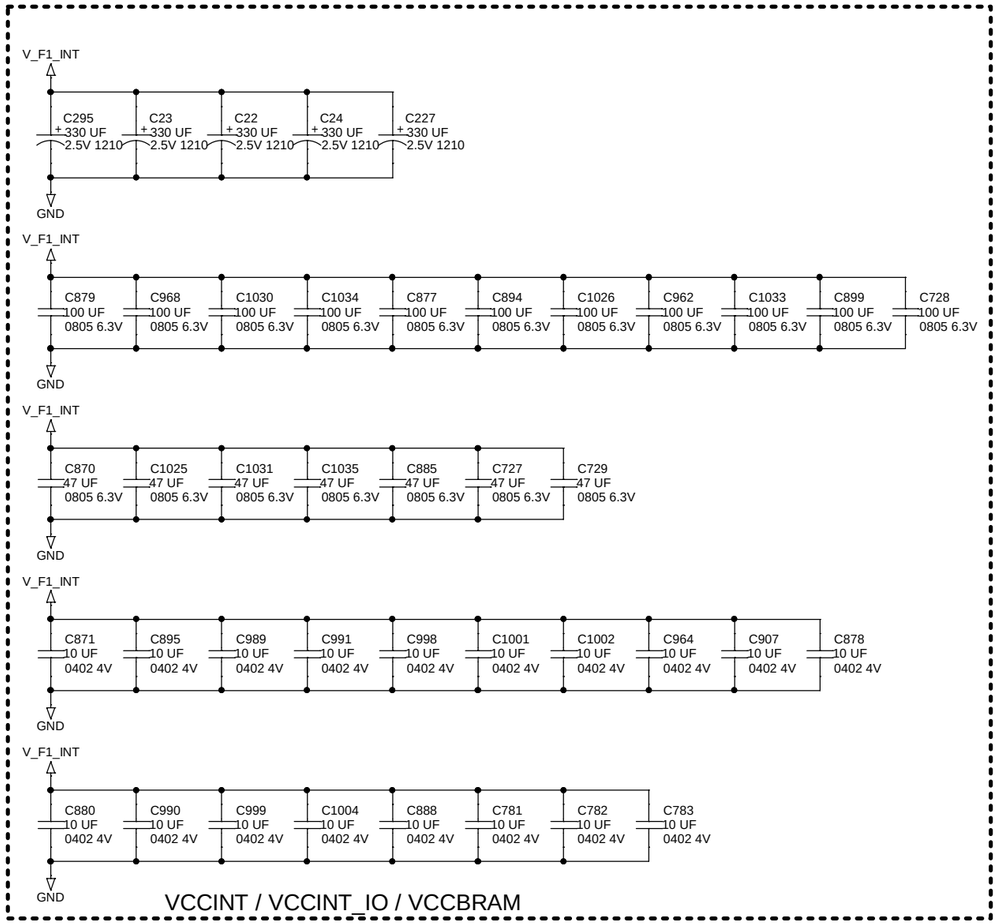
VCCINT_IO MUST BE CONNECTED TO VCC_INT (0.85V).



VCCBRAM CAN BE CONNECTED TO VCC_INT (0.85V).

VCCAUX_IO MUST BE CONNECTED TO VCCAUX (1.8V).





BYPASS CAPACITOR VALUES AND QUANTITIES FROM "UG583 UltraScale Architecture PCB Design"

APOLLO CM W/ DUAL A2577, MK1		
Title: 5.02: FPGA#1 POWER INTERNAL		
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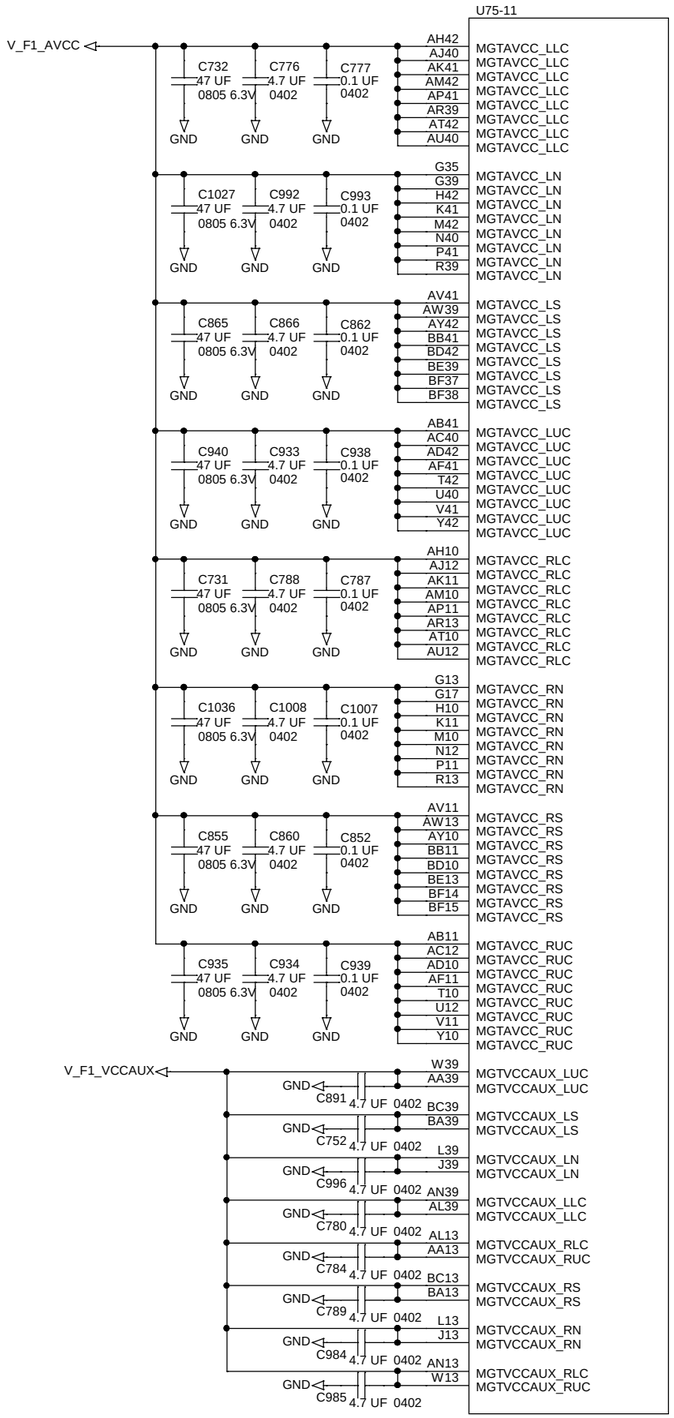
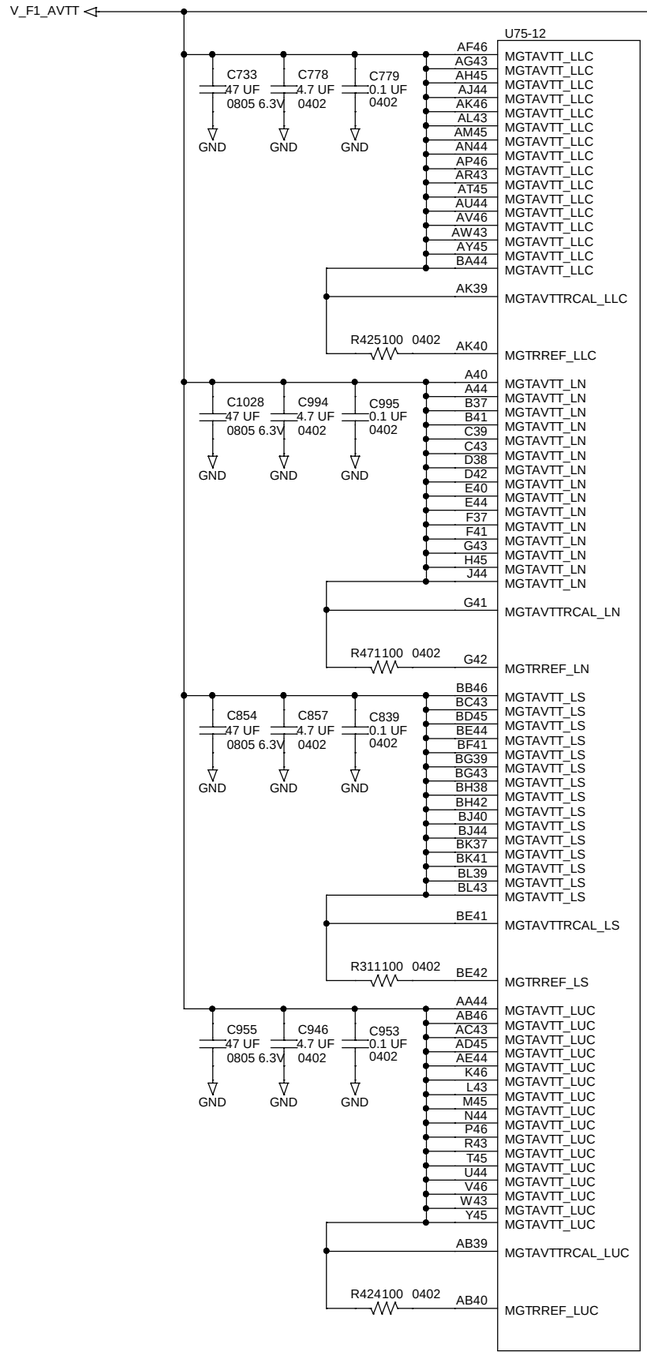
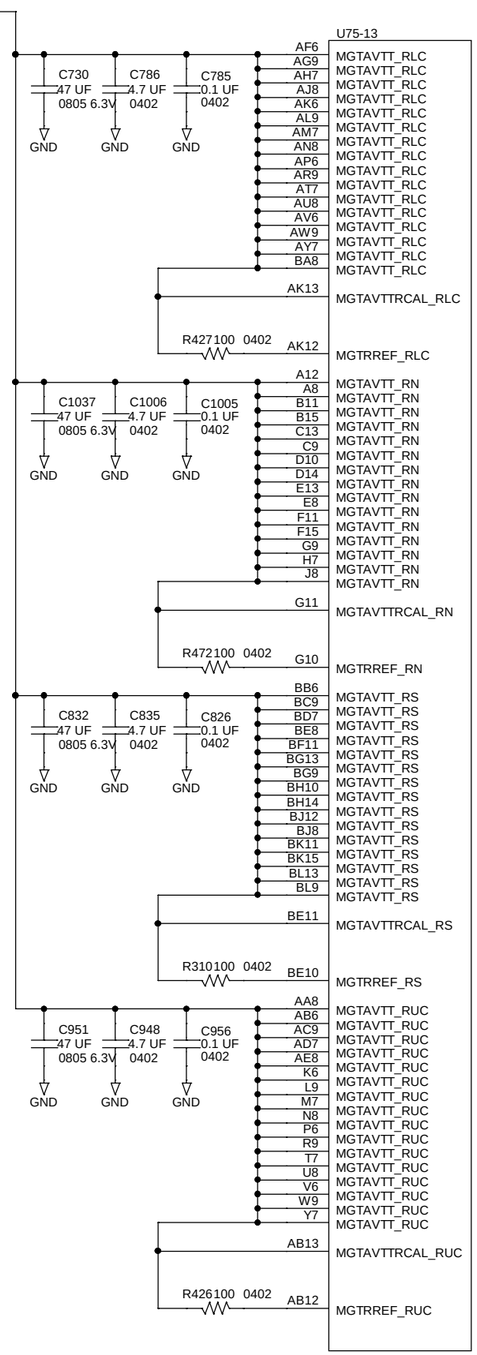
5.03: FPGA#1 GTY TRANSCEIVER POWER







REFER TO THE GTY USER GUIDE FOR DETAILS ON TRACE ROUTING FOR THE MGTRREF RESISTOR.

PLACE CAPACITORS AND RESISTORS THAT ARE ON THIS SHEET NEAR THE BGA PINS.

APOLLO CM W/ DUAL A2577, MK1		
Title: 5.03: FPGA#1 GTY TRANSCEIVER POWER		
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5.04: FPGA#1 CONFIGURATION

QUAD SPI CONFIG FLASH

MUST BE TIED TO "VCCINT" OR "GND". DO NOT CONNECT TO "VCCO_0". CONNECT TO "GND" FOR STANDARD POR DELAY.

THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

PULLUPS/PULLDOWNS ON THE BOOT MODE CONFIGURATION INPUTS MUST BE 1K OR LESS.

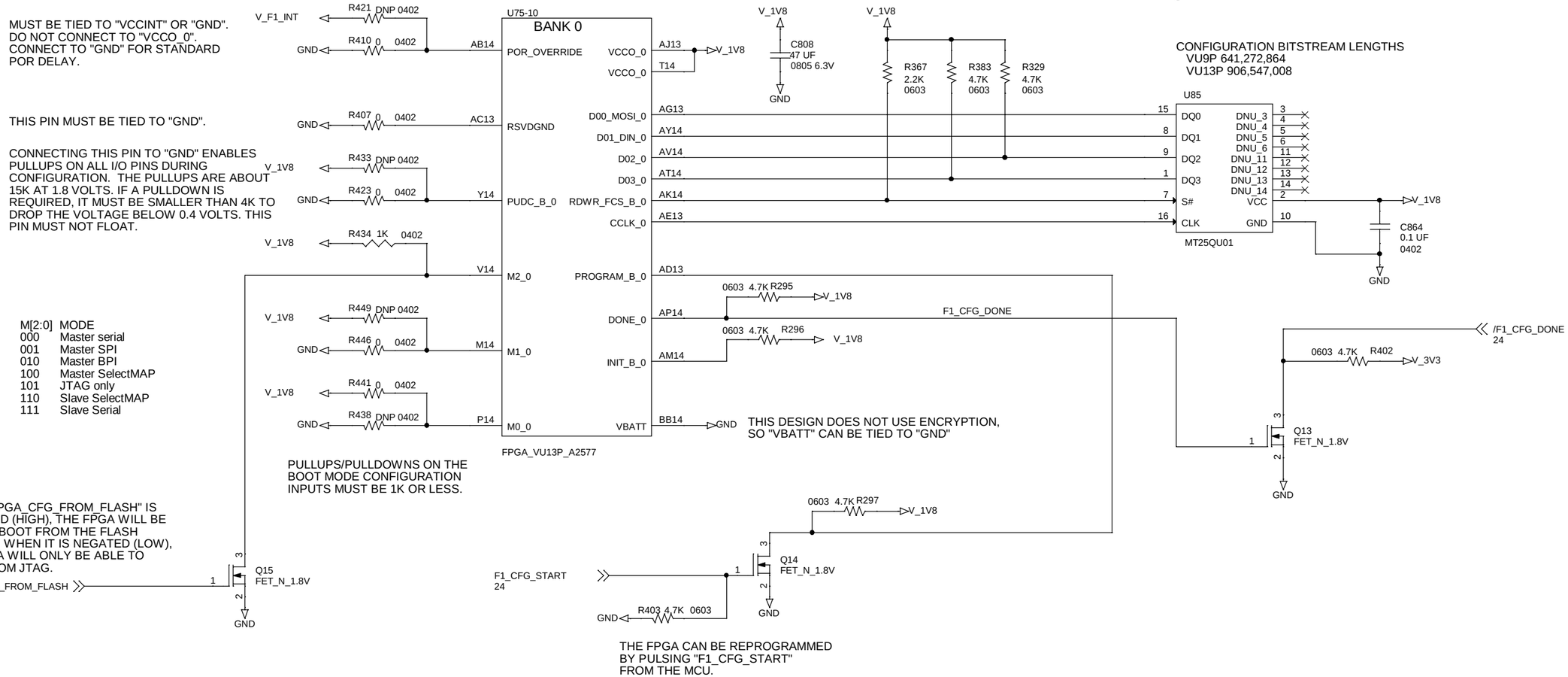
WHEN "FPGA_CFG_FROM_FLASH" IS ASSERTED (HIGH), THE FPGA WILL BE ABLE TO BOOT FROM THE FLASH MEMORY. WHEN IT IS NEGATED (LOW), THE FPGA WILL ONLY BE ABLE TO BOOT FROM JTAG.

FPGA_CFG_FROM_FLASH 24,54

THE FPGA CAN BE REPROGRAMMED BY PULSING "F1_CFG_START" FROM THE MCU.

THIS DESIGN DOES NOT USE ENCRYPTION, SO "VBATT" CAN BE TIED TO "GND"

CONFIGURATION BITSTREAM LENGTHS
VU9P 641,272,864
VU13P 906,547,008



APOLLO CM W/ DUAL A2577, MK1			
Title: 5.04: FPGA#1 CONFIGURATION			
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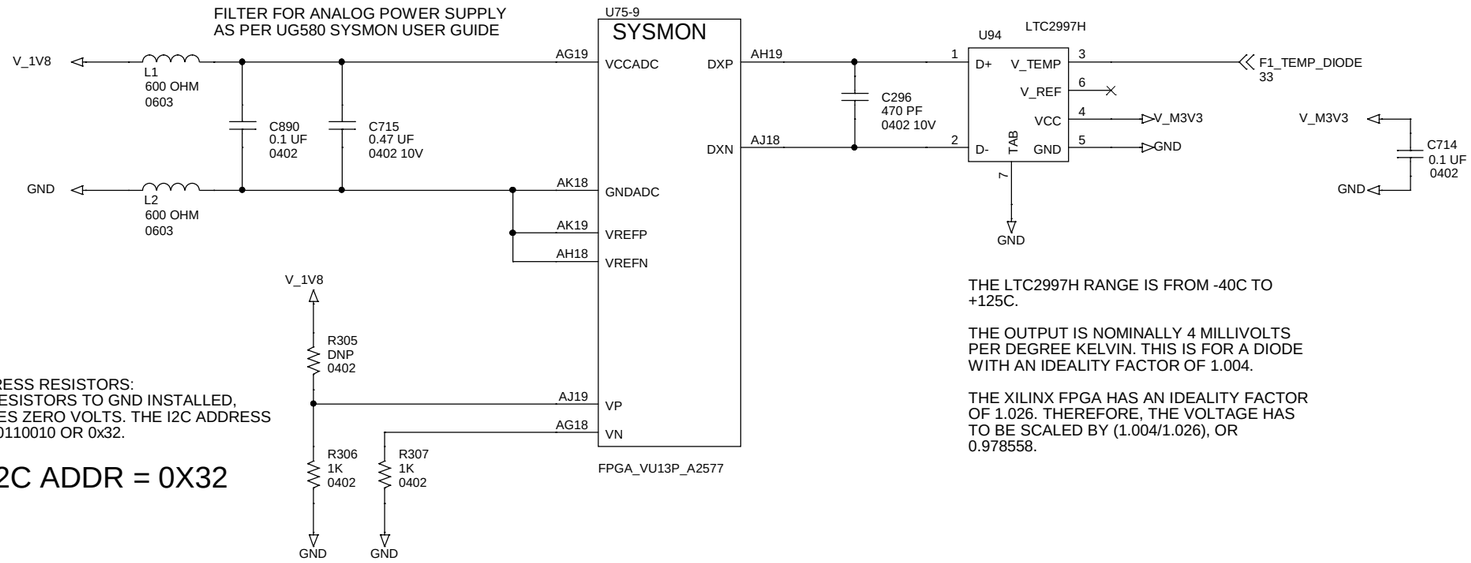
5.05: FPGA#1 SYSTEM MONITOR

FOR THE VU9P, THE MASTER SLR INDEX IS SLR1, AND THE SLAVE SLR INDEX ARE SLR0 AND SLR2.

FOR THE VU13P, THE MASTER SLR INDEX IS SLR1, AND THE SLAVE SLR INDEX ARE SLR0, SLR2, AND SLR3.

ONLY THE MASTER SLR IS ACCESSABLE FROM THE I2C CONNECTIONS.



SYSMON I2C ADDRESS RESISTORS:
WITH ONLY THE RESISTORS TO GND INSTALLED, SYSMON MEASURES ZERO VOLTS. THE I2C ADDRESS IS THEREFORE 0b0110010 OR 0x32.

I2C ADDR = 0X32

THE LTC2997H RANGE IS FROM -40C TO +125C.

THE OUTPUT IS NOMINALLY 4 MILLIVOLTS PER DEGREE KELVIN. THIS IS FOR A DIODE WITH AN IDEALITY FACTOR OF 1.004.

THE XILINX FPGA HAS AN IDEALITY FACTOR OF 1.026. THEREFORE, THE VOLTAGE HAS TO BE SCALED BY (1.004/1.026), OR 0.978558.

APOLLO CM W/ DUAL A2577, MK1		
Title: 5.05: FPGA#1 SYSTEM MONITOR		
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5.06 FPGA#1 I/O SLR0

THESE BANKS ARE NUMBERED THE SAME IN THE VU13P AND VU9P, AND THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#0 FOR THE VU13P AND SLR#0 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
D	61	61
E	62	62
F	63	63

U75-14

BE20	IO_L10N_T1U_N7_QBC_AD4N_61	VCCO_61	AW27	V_1V8
BE21	IO_L10P_T1U_N6_QBC_AD4P_61	VCCO_61	AY24	
BF22	IO_L11N_T1U_N9_GC_61	VCCO_61	BC25	
BE22	IO_L11P_T1U_N8_GC_61	VCCO_61	BD22	
BE23	IO_L12N_T1U_N11_GC_61	VCCO_61	BG23	
BD23	IO_L12P_T1U_N10_GC_61	VCCO_61	BK24	
BD24	IO_L13N_T2L_N1_GC_QBC_61	VREF_61	AV23	OMIT "VREF" AND "VRP" RESISTORS ON UNUSED I/O BANKS.
BD25	IO_L13P_T2L_N0_GC_QBC_61			
BC23	IO_L14N_T2L_N3_GC_61			
BC24	IO_L14P_T2L_N2_GC_61			
BB25	IO_L15N_T2L_N5_AD11N_61			
BB26	IO_L15P_T2L_N4_AD11P_61			
BD26	IO_L16N_T2U_N7_QBC_AD3N_61			
BC26	IO_L16P_T2U_N6_QBC_AD3P_61			
BA24	IO_L17N_T2U_N9_AD10N_61			
BA25	IO_L17P_T2U_N8_AD10P_61			
BC22	IO_L18N_T2U_N11_AD2N_61			
BB22	IO_L18P_T2U_N10_AD2P_61			
AW24	IO_L19N_T3L_N1_DBC_AD9N_61			
AW25	IO_L19P_T3L_N0_DBC_AD9P_61			
BL23	IO_L1N_T0L_N1_DBC_61			
BL24	IO_L1P_T0L_N0_DBC_61			
AW23	IO_L20N_T3L_N3_AD1N_61			
AV24	IO_L20P_T3L_N2_AD1P_61			
BA23	IO_L21N_T3L_N5_AD8N_61			
AY23	IO_L21P_T3L_N4_AD8P_61			
BA27	IO_L22N_T3U_N7_DBC_AD0N_61			
AY27	IO_L22P_T3U_N6_DBC_AD0P_61			
AY26	IO_L23N_T3U_N9_61			
AW26	IO_L23P_T3U_N8_61			
AV26	IO_L24N_T3U_N11_61			
AV27	IO_L24P_T3U_N10_61			
BL22	IO_L2N_T0L_N3_61			
BK22	IO_L2P_T0L_N2_61			
BJ24	IO_L3N_T0L_N5_AD15N_61			
BJ25	IO_L3P_T0L_N4_AD15P_61			
BK23	IO_L4N_T0U_N7_DBC_AD7N_61			
BJ23	IO_L4P_T0U_N6_DBC_AD7P_61			
BL25	IO_L5N_T0U_N9_AD14N_61			
BK25	IO_L5P_T0U_N8_AD14P_61			
BH23	IO_L6N_T0U_N11_AD6N_61			
BH24	IO_L6P_T0U_N10_AD6P_61			
BG24	IO_L7N_T1L_N1_QBC_AD13N_61			
BG25	IO_L7P_T1L_N0_QBC_AD13P_61			
BG22	IO_L8N_T1L_N3_AD5N_61			
BF23	IO_L8P_T1L_N2_AD5P_61			
BF24	IO_L9N_T1L_N5_AD12N_61			
BF25	IO_L9P_T1L_N4_AD12P_61			
BH22	IO_T0U_N12_VRP_61			
BE25	IO_T1U_N12_61			
BB24	IO_T2U_N12_61			
AY25	IO_T3U_N12_61			

OMIT "VREF" AND "VRP" RESISTORS ON UNUSED I/O BANKS.

FPGA_VU13P_A2577

nF1_TEST_CONN_0 50
pF1_TEST_CONN_0 50
pF1_TEST_CONN_5 50
nF1_TEST_CONN_6 50
nF1_TEST_CONN_4 50
pF1_TEST_CONN_4 50
nF1_TEST_CONN_3 50
pF1_TEST_CONN_3 50
nF1_TEST_CONN_2 50
pF1_TEST_CONN_2 50
nF1_TEST_CONN_1 50
pF1_TEST_CONN_1 50

THIS IS THE 40 MHZ RECOVERED TCDS CLOCK. USING BANK 62 KEEPS THIS INTHE SAME SLR AS THE TCDS LOGIC.

bc_nF1_TCDS_RECOV_CLK 22
bc_pF1_TCDS_RECOV_CLK 22
nF2F1_SPARE2 58
pF2F1_SPARE2 58
nF2F1_SPARE1 58
pF2F1_SPARE1 58
nF2F1_SPARE0 58
pF2F1_SPARE0 58

GND — R317 240 0402

U75-15

BH27	IO_L10N_T1U_N7_QBC_AD4N_62	VCCO_62	AV30	V_1V8
BH26	IO_L10P_T1U_N6_QBC_AD4P_62	VCCO_62	BA31	
BF28	IO_L11N_T1U_N9_GC_62	VCCO_62	BB28	
BF27	IO_L11P_T1U_N8_GC_62	VCCO_62	BE29	
BE27	IO_L12N_T1U_N11_GC_62	VCCO_62	BF26	
BE26	IO_L12P_T1U_N10_GC_62	VCCO_62	BH30	
BD29	IO_L13N_T2L_N1_GC_QBC_62	VCCO_62	BJ27	
BC28	IO_L13P_T2L_N0_GC_QBC_62	VREF_62	AV28	R377 1K 0402 GND
BE28	IO_L14N_T2L_N3_GC_62			
BD28	IO_L14P_T2L_N2_GC_62			
BE30	IO_L15N_T2L_N5_AD11N_62			
BD30	IO_L15P_T2L_N4_AD11P_62			
BC27	IO_L16N_T2U_N7_QBC_AD3N_62			
BB27	IO_L16P_T2U_N6_QBC_AD3P_62			
BC31	IO_L17N_T2U_N9_AD10N_62			
BB31	IO_L17P_T2U_N8_AD10P_62			
BC29	IO_L18N_T2U_N11_AD2N_62			
BB29	IO_L18P_T2U_N10_AD2P_62			
BA29	IO_L19N_T3L_N1_DBC_AD9N_62			
BA28	IO_L19P_T3L_N0_DBC_AD9P_62			
BJ28	IO_L1N_T0L_N1_DBC_62			
BH28	IO_L1P_T0L_N0_DBC_62			
AY28	IO_L20N_T3L_N3_AD1N_62			
AW28	IO_L20P_T3L_N2_AD1P_62			
BA30	IO_L21N_T3L_N5_AD8N_62			
AY30	IO_L21P_T3L_N4_AD8P_62			
AV31	IO_L22N_T3U_N7_DBC_AD0N_62			
AU31	IO_L22P_T3U_N6_DBC_AD0P_62			
AW29	IO_L23N_T3U_N9_62			
AV29	IO_L23P_T3U_N8_62			
AY31	IO_L24N_T3U_N11_62			
AW31	IO_L24P_T3U_N10_62			
BL28	IO_L2N_T0L_N3_62			
BL27	IO_L2P_T0L_N2_62			
BJ30	IO_L3N_T0L_N5_AD15N_62			
BJ29	IO_L3P_T0L_N4_AD15P_62			
BK28	IO_L4N_T0U_N7_DBC_AD7N_62			
BK27	IO_L4P_T0U_N6_DBC_AD7P_62			
BL30	IO_L5N_T0U_N9_AD14N_62			
BK30	IO_L5P_T0U_N8_AD14P_62			
BK26	IO_L6N_T0U_N11_AD6N_62			
BJ26	IO_L6P_T0U_N10_AD6P_62			
BG27	IO_L7N_T1L_N1_QBC_AD13N_62			
BG26	IO_L7P_T1L_N0_QBC_AD13P_62			
BG30	IO_L8N_T1L_N3_AD5N_62			
BF29	IO_L8P_T1L_N2_AD5P_62			
BH29	IO_L9N_T1L_N5_AD12N_62			
BG29	IO_L9P_T1L_N4_AD12P_62			
BL29	IO_T0U_N12_VRP_62			
BF30	IO_T1U_N12_62			
BB30	IO_T2U_N12_62			
AW30	IO_T3U_N12_62			

FPGA_VU13P_A2577

U75-16

BC36	IO_L10N_T1U_N7_QBC_AD4N_63	VCCO_63	AT36	V_1V8
BB36	IO_L10P_T1U_N6_QBC_AD4P_63	VCCO_63	AU33	
BB35	IO_L11N_T1U_N9_GC_63	VCCO_63	AW37	
BA35	IO_L11P_T1U_N8_GC_63	VCCO_63	AY34	
BB34	IO_L12N_T1U_N11_GC_63	VCCO_63	BC35	
BA34	IO_L12P_T1U_N10_GC_63	VCCO_63	BD32	
AW36	IO_L13N_T2L_N1_GC_QBC_63	VREF_63	AR32	OMIT "VREF" AND "VRP" RESISTORS ON UNUSED I/O BANKS.
AW35	IO_L13P_T2L_N0_GC_QBC_63			
AY36	IO_L14N_T2L_N3_GC_63			
AY35	IO_L14P_T2L_N2_GC_63			
AV37	IO_L15N_T2L_N5_AD11N_63			
AV36	IO_L15P_T2L_N4_AD11P_63			
AV33	IO_L16N_T2U_N7_QBC_AD3N_63			
AV32	IO_L16P_T2U_N6_QBC_AD3P_63			
AW34	IO_L17N_T2U_N9_AD10N_63			
AW33	IO_L17P_T2U_N8_AD10P_63			
AV34	IO_L18N_T2U_N11_AD2N_63			
AU34	IO_L18P_T2U_N10_AD2P_63			
AU37	IO_L19N_T3L_N1_DBC_AD9N_63			
AU36	IO_L19P_T3L_N0_DBC_AD9P_63			
BE32	IO_L1N_T0L_N1_DBC_63			
BE31	IO_L1P_T0L_N0_DBC_63			
AU32	IO_L20N_T3L_N3_AD1N_63			
AT32	IO_L20P_T3L_N2_AD1P_63			
AR37	IO_L21N_T3L_N5_AD8N_63			
AR36	IO_L21P_T3L_N4_AD8P_63			
AT34	IO_L22N_T3U_N7_DBC_AD0N_63			
AT33	IO_L22P_T3U_N6_DBC_AD0P_63			
AT35	IO_L23N_T3U_N9_63			
AR35	IO_L23P_T3U_N8_63			
AR34	IO_L24N_T3U_N11_63			
AR33	IO_L24P_T3U_N10_63			
BC32	IO_L2N_T0L_N3_63			
BB32	IO_L2P_T0L_N2_63			
BA32	IO_L3N_T0L_N5_AD15N_63			
AY32	IO_L3P_T0L_N4_AD15P_63			
BA33	IO_L4N_T0U_N7_DBC_AD7N_63			
AY33	IO_L4P_T0U_N6_DBC_AD7P_63			
BD33	IO_L5N_T0U_N9_AD14N_63			
BC33	IO_L5P_T0U_N8_AD14P_63			
BD34	IO_L6N_T0U_N11_AD6N_63			
BC34	IO_L6P_T0U_N10_AD6P_63			
BD36	IO_L7N_T1L_N1_QBC_AD13N_63			
BD35	IO_L7P_T1L_N0_QBC_AD13P_63			
BD37	IO_L8N_T1L_N3_AD5N_63			
BC37	IO_L8P_T1L_N2_AD5P_63			
BB37	IO_L9N_T1L_N5_AD12N_63			
BA37	IO_L9P_T1L_N4_AD12P_63			
BD31	IO_T0U_N12_VRP_63			
AY37	IO_T1U_N12_63			
AU35	IO_T2U_N12_63			
AT37	IO_T3U_N12_63			

OMIT "VREF" AND "VRP" RESISTORS ON UNUSED I/O BANKS.

FPGA_VU13P_A2577

APOLLO CM W/ DUAL A2577, MK1			
Title: 5.06 FPGA#1 I/O SLR0			
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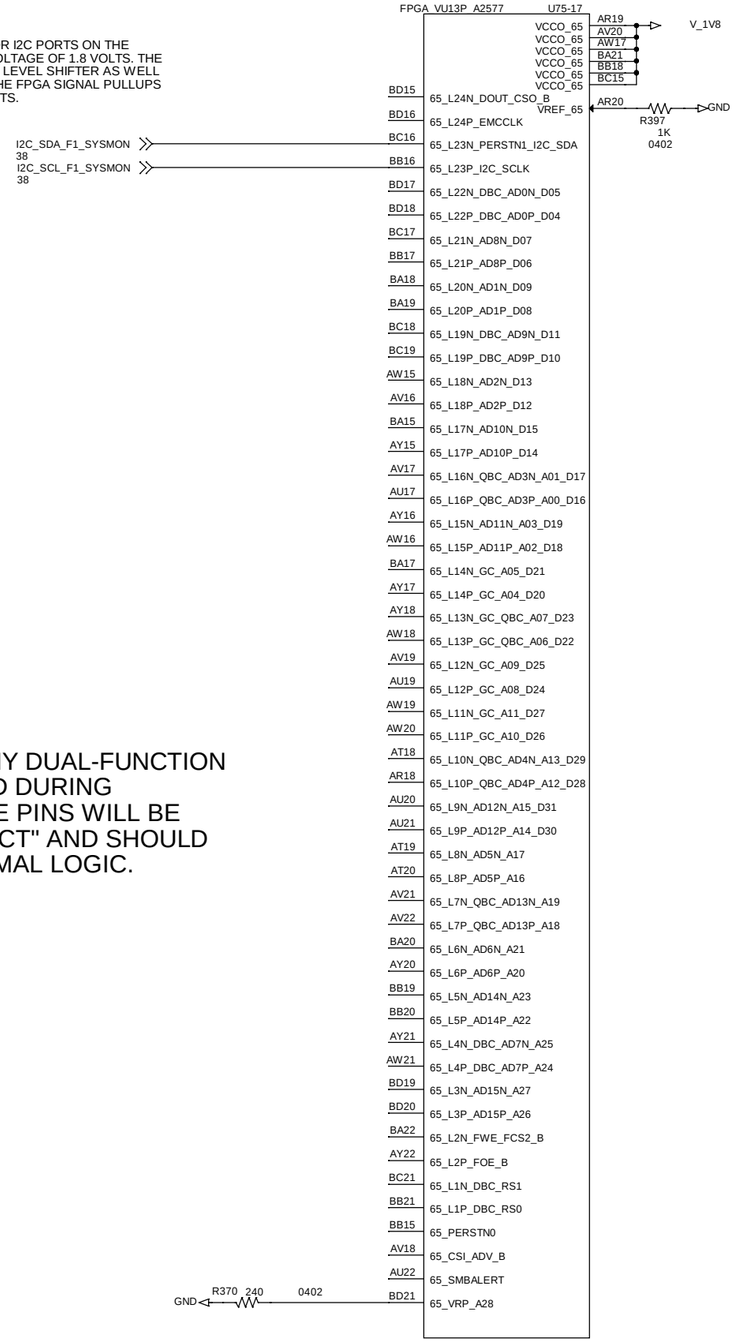
5.07 FPGA#1 I/O SLR1

THESE BANKS ARE NUMBERED THE SAME IN THE VU13P AND VU9P, AND THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#1 FOR THE VU13P AND SLR#1 FOR THE VU9P.

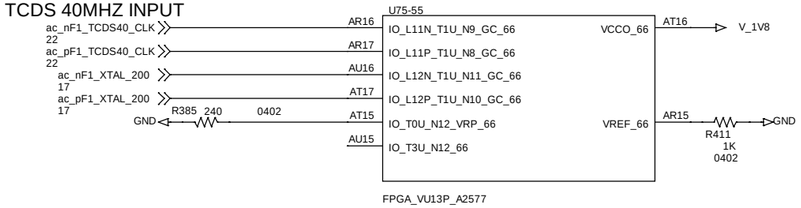
SITE	VU13P BANK	VU9P BANK
C	65	65
B	66	66

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.



F1 LOGIC
TCDS 40MHZ INPUT



APOLLO CM W/ DUAL A2577, MK1		
Title: 5.07 FPGA#1 I/O SLR1		
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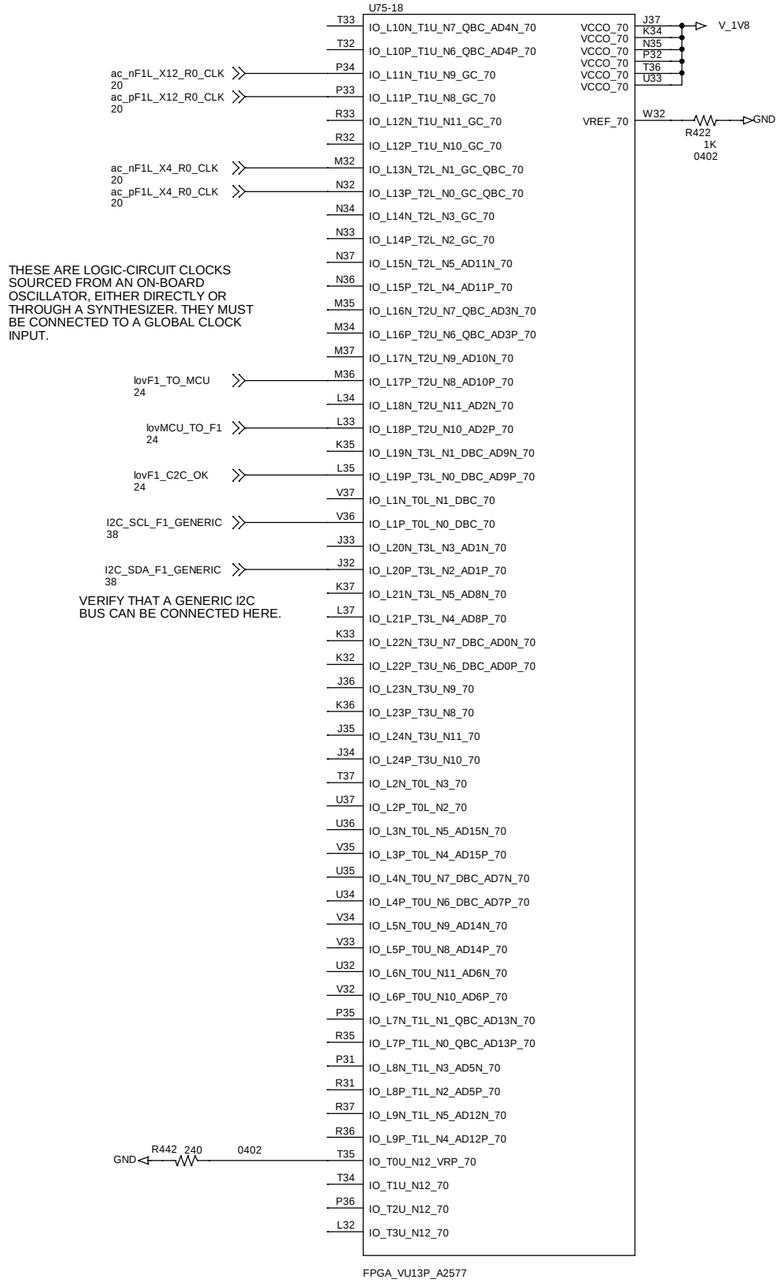
5.08: FPGA#1 I/O SLR2

THESE BANKS ARE NUMBERED DIFFERENTLY IN THE VU13P AND VU9P, BUT THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#2 FOR THE VU13P AND SLR#1 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
G	70	67
H	71	68



THESE ARE LOGIC-CIRCUIT CLOCKS SOURCED FROM AN ON-BOARD OSCILLATOR, EITHER DIRECTLY OR THROUGH A SYNTHESIZER. THEY MUST BE CONNECTED TO A GLOBAL CLOCK INPUT.

VERIFY THAT A GENERIC I2C BUS CAN BE CONNECTED HERE.

THE TRI-COLOR LED IS CONNECTED TO DIFFERENT PINS ON EACH FPGA, IN ORDER TO SIMPLIFY LAYOUT.

PIN B29 IS PULLED HIGH ON FPGA#1 AND IS TIED TO GND ON FPGA#2. IT ALLOWS THE FIRMWARE TO KNOW WHICH FPGA IT IS RUNNING IN.

THE "F2F1_SPARE" SIGNALS ARE OUTPUTS FROM F2 AND INPUTS TO F1.
THE "F1F2_SPARE" SIGNALS ARE OUTPUTS FROM F1 AND INPUTS TO F2.
THEY ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE FPGA

APOLLO CM W/ DUAL A2577, MK1		
Title: 5.08: FPGA#1 I/O SLR2		
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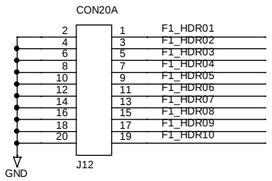
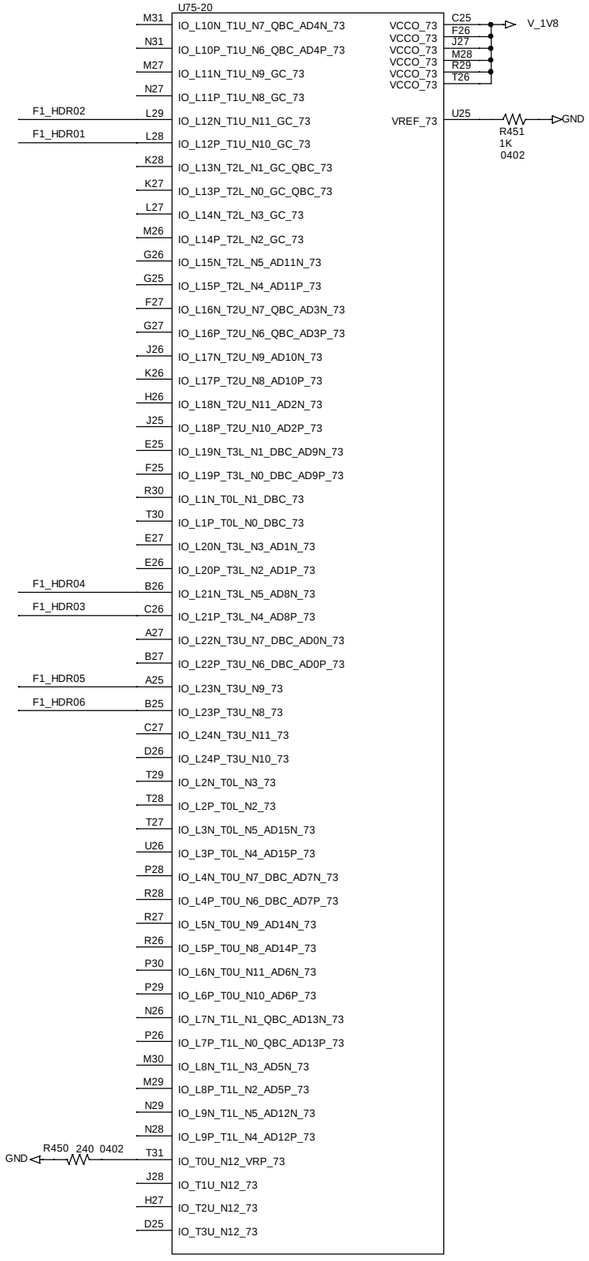
5.09: FPGA#1 I/O SLR3

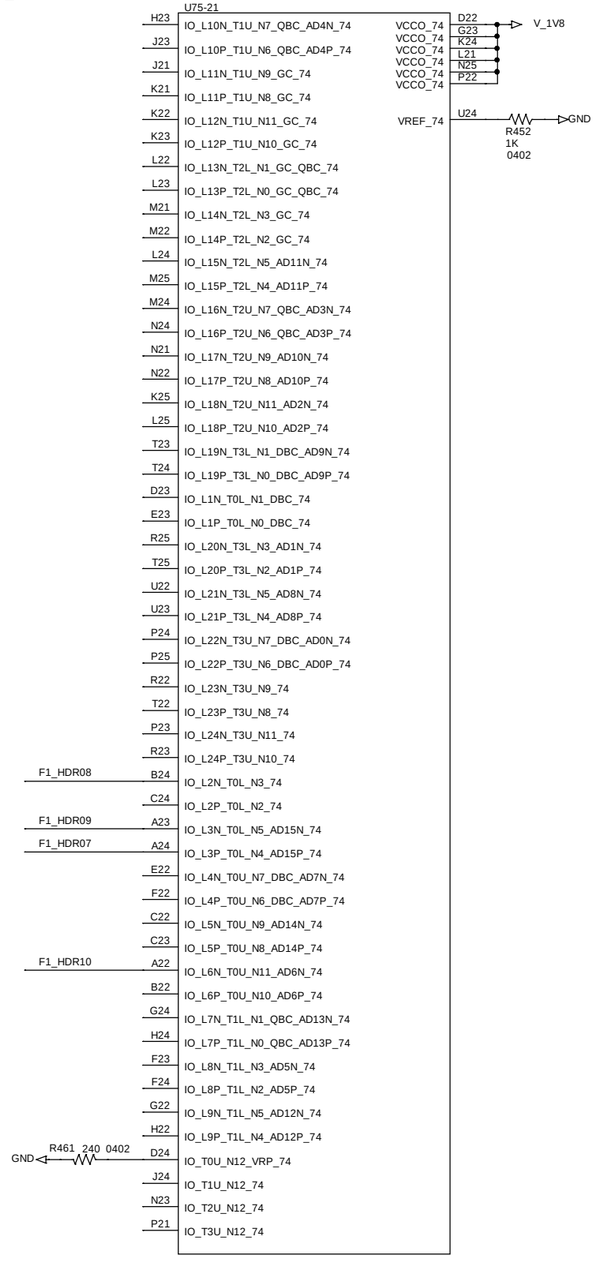


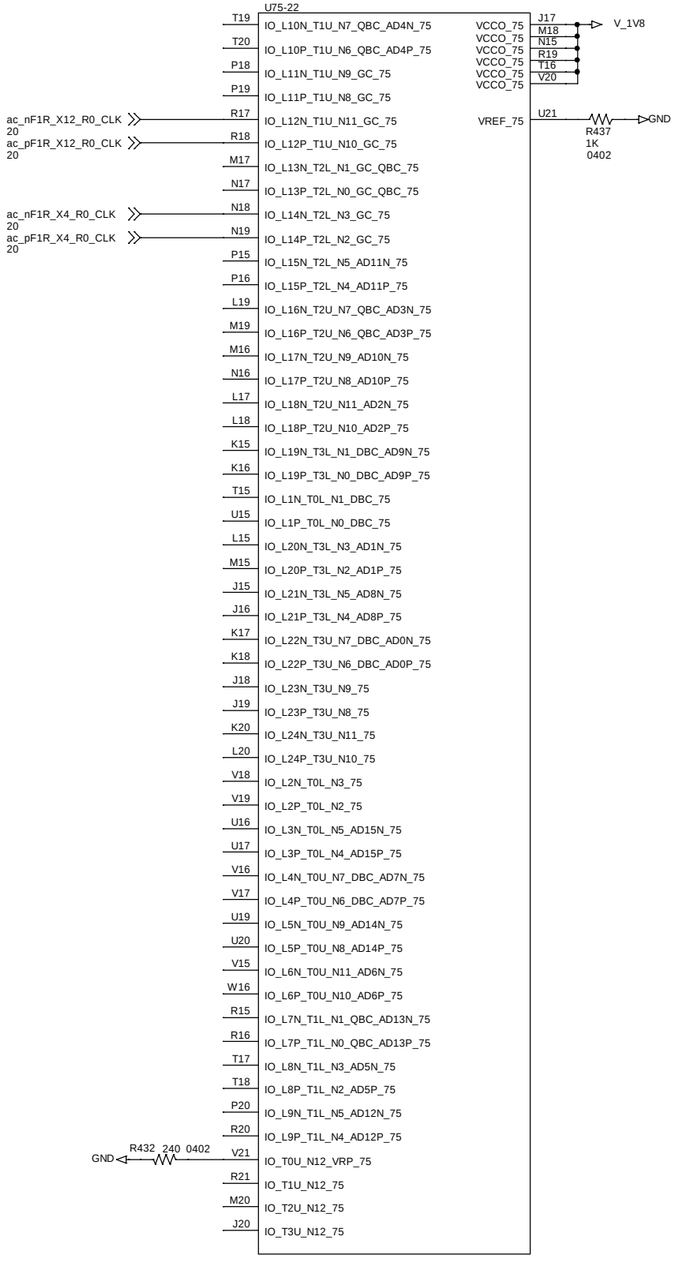
THE "F1_HDRnn" SIGNALS ARE CONNECTED FROM THE FPGA TO PADS ON THE BOTTOM SIDE OF THE BOARD. A 20-PIN HEADER CAN BE ATTACHED. THESE SIGNALS ARE FOR DEBUGGING, OR FUTURE USE. HDR01 AND HDR02 ARE CONNECTED TO CLOCK-CAPABLE INPUTS.

THESE BANKS ARE NUMBERED DIFFERENTLY IN THE VU13P AND VU9P, BUT THE PIN NUMBERS ARE THE SAME. THEY ARE IN SLR#3 FOR THE VU13P AND SLR#2 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
I	73	70
J	74	71
K	75	72







Title	APOLLO CM W/ DUAL A2577, MK1		
	5.09: FPGA#1 I/O SLR3		
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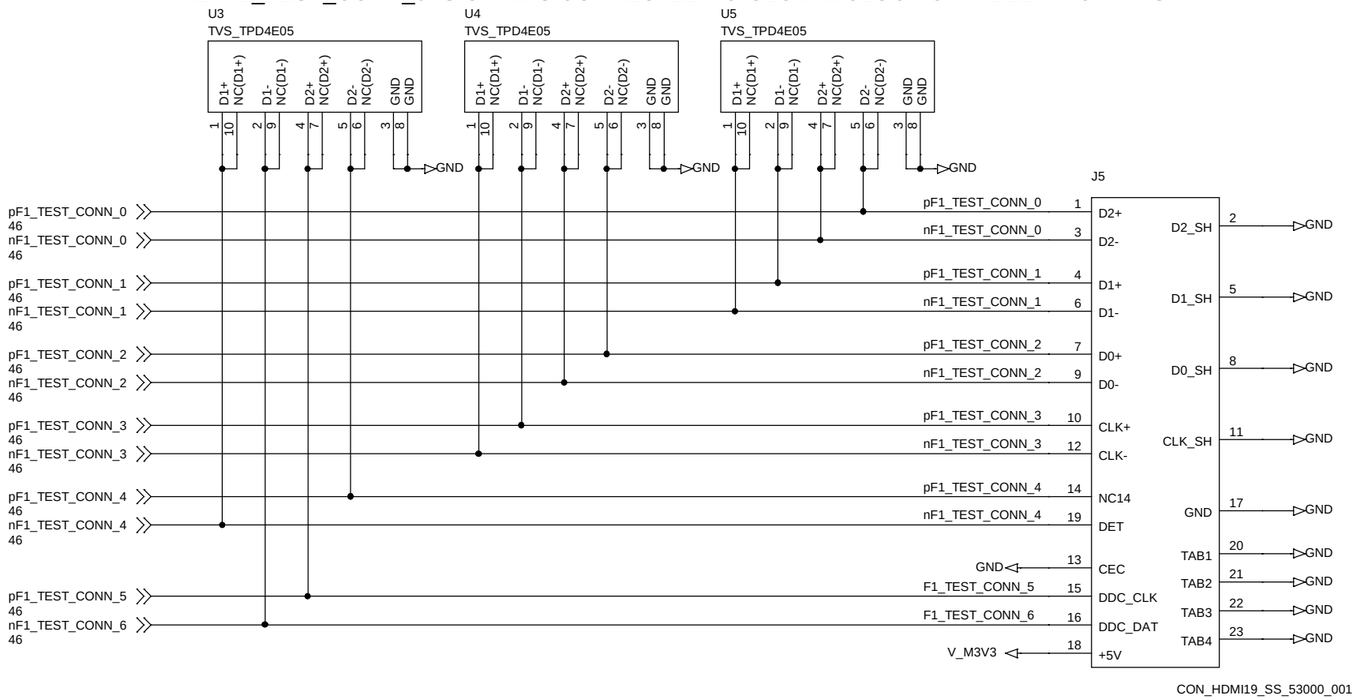
5.10: FPGA#1 TEST CONNECTOR

THIS CONNECTOR IS LOCATED ON THE FRONT PANEL. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

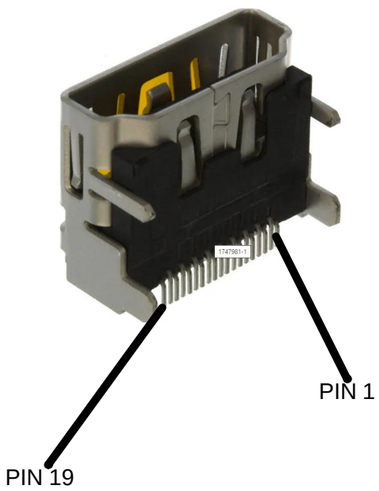
THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

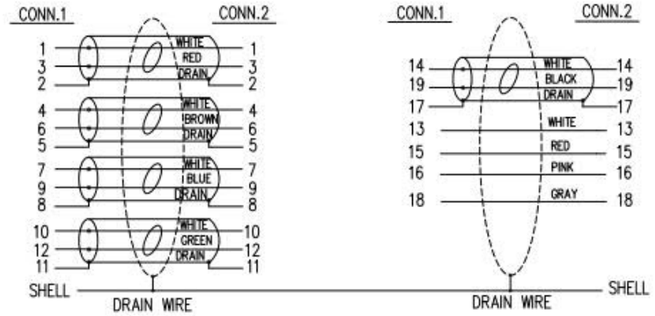
THE "F1_TEST_CONN_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.



CON_HDMI19_SS_53000_001

PIN ASSIGNMENT





APOLLO CM W/ DUAL A2577, MK1		
Title: 5.10: FPGA#1 TEST CONNECTOR		
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6.01: FPGA#2 GND

U77-1 FPGA_VU13P_A2577

A13	GND	GND	AE12
A16	GND	GND	AE16
A17	GND	GND	AE18
A18	GND	GND	AE20
A21	GND	GND	AE22
A26	GND	GND	AE24
A31	GND	GND	AE26
A34	GND	GND	AE28
A35	GND	GND	AE3
A36	GND	GND	AE30
A39	GND	GND	AE32
A4	GND	GND	AE34
A43	GND	GND	AE36
A45	GND	GND	AE38
A48	GND	GND	AE4
A7	GND	GND	AE40
A9	GND	GND	AE43
AA12	GND	GND	AE47
AA14	GND	GND	AE48
AA16	GND	GND	AE49
AA18	GND	GND	AE5
AA20	GND	GND	AE9
AA22	GND	GND	AF1
AA24	GND	GND	AF10
AA26	GND	GND	AF12
AA28	GND	GND	AF15
AA3	GND	GND	AF17
AA30	GND	GND	AF19
AA32	GND	GND	AF2
AA34	GND	GND	AF21
AA36	GND	GND	AF23
AA38	GND	GND	AF25
AA4	GND	GND	AF27
AA40	GND	GND	AF29
AA43	GND	GND	AF31
AA47	GND	GND	AF33
AA48	GND	GND	AF35
AA49	GND	GND	AF37
AA5	GND	GND	AF39
AA9	GND	GND	AF40
AB1	GND	GND	AF42
AB10	GND	GND	AF45
AB15	GND	GND	AF47
AB17	GND	GND	AF5
AB19	GND	GND	AF50
AB2	GND	GND	AF51
AB21	GND	GND	AF7
AB23	GND	GND	AG12
AB25	GND	GND	AG16
AB27	GND	GND	AG20
AB29	GND	GND	AG22
AB31	GND	GND	AG24
AB33	GND	GND	AG26
AB35	GND	GND	AG28
AB37	GND	GND	AG3
AB38	GND	GND	AG30
AB42	GND	GND	AG32
AB45	GND	GND	AG34
AB47	GND	GND	AG36
AB5	GND	GND	AG38
AB50	GND	GND	AG4
AB51	GND	GND	AG40
AB7	GND	GND	AG44
AC14	GND	GND	AG47
AC16	GND	GND	AG48
AC18	GND	GND	AG49
AC20	GND	GND	AG5
AC22	GND	GND	AG8
AC24	GND	GND	AH1
AC26	GND	GND	AH11
AC28	GND	GND	AH12
AC3	GND	GND	AH15
AC30	GND	GND	AH17
AC32	GND	GND	AH2
AC34	GND	GND	AH21
AC36	GND	GND	AH23
AC38	GND	GND	AH25
AC39	GND	GND	AH27
AC4	GND	GND	AH29
AC44	GND	GND	AH31
AC47	GND	GND	AH33
AC48	GND	GND	AH35
AC49	GND	GND	AH37
AC5	GND	GND	AH39
AC8	GND	GND	AH40
AD1	GND	GND	AH41
AD11	GND	GND	AH46
AD12	GND	GND	AH47
AD15	GND	GND	AH5
AD17	GND	GND	AH50
AD19	GND	GND	AH51
AD2	GND	GND	AH6
AD21	GND	GND	AJ14
AD23	GND	GND	AJ16
AD25	GND	GND	AJ20
AD27	GND	GND	AJ22
AD29	GND	GND	AJ24
AD31	GND	GND	AJ26
AD33	GND	GND	AJ28
AD35	GND	GND	AJ3
AD37	GND	GND	AJ30
AD39	GND	GND	AJ32
AD40	GND	GND	AJ34
AD41	GND	GND	AJ36
AD46	GND	GND	AJ38
AD47	GND	GND	AJ39
AD5	GND	GND	AJ47
AD50	GND	GND	AJ43
AD51	GND	GND	AJ48
AD6	GND	GND	AJ4

GND GND

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AJ49	GND	GND	AP42
AJ5	GND	GND	AP45
AJ9	GND	GND	AP47
AK1	GND	GND	AP5
AK10	GND	GND	AP50
AK15	GND	GND	AP51
AK17	GND	GND	AP7
AK2	GND	GND	AR12
AK21	GND	GND	AR14
AK23	GND	GND	AR22
AK25	GND	GND	AR24
AK27	GND	GND	AR26
AK29	GND	GND	AR28
AK31	GND	GND	AR3
AK33	GND	GND	AR30
AK35	GND	GND	AR38
AK37	GND	GND	AR4
AK38	GND	GND	AR40
AK42	GND	GND	AR44
AK45	GND	GND	AR47
AK47	GND	GND	AR48
AK5	GND	GND	AR49
AK50	GND	GND	AR5
AK51	GND	GND	AR8
AK7	GND	GND	AT1
AL12	GND	GND	AT11
AL14	GND	GND	AT2
AL16	GND	GND	AT21
AL18	GND	GND	AT23
AL20	GND	GND	AT25
AL22	GND	GND	AT27
AL24	GND	GND	AT29
AL26	GND	GND	AT31
AL28	GND	GND	AT38
AL3	GND	GND	AT41
AL30	GND	GND	AT46
AL32	GND	GND	AT47
AL34	GND	GND	AT5
AL36	GND	GND	AT50
AL38	GND	GND	AT51
AL4	GND	GND	AT6
AL40	GND	GND	AU13
AL44	GND	GND	AU14
AL47	GND	GND	AU18
AL48	GND	GND	AU24
AL49	GND	GND	AU26
AL5	GND	GND	AU28
AL8	GND	GND	AU3
AM1	GND	GND	AU30
AM11	GND	GND	AU38
AM15	GND	GND	AU39
AM17	GND	GND	AU4
AM19	GND	GND	AU43
AM2	GND	GND	AU47
AM21	GND	GND	AU48
AM23	GND	GND	AU49
AM25	GND	GND	AU5
AM27	GND	GND	AU9
AM29	GND	GND	AV1
AM31	GND	GND	AV10
AM33	GND	GND	AV15
AM35	GND	GND	AV2
AM37	GND	GND	AV25
AM38	GND	GND	AV35
AM41	GND	GND	AV38
AM46	GND	GND	AV42
AM47	GND	GND	AV45
AM5	GND	GND	AV47
AM50	GND	GND	AV5
AM51	GND	GND	AV50
AM6	GND	GND	AV51
AN12	GND	GND	AV7
AN14	GND	GND	AW12
AN16	GND	GND	AW14
AN18	GND	GND	AW22
AN20	GND	GND	AW3
AN22	GND	GND	AW32
AN24	GND	GND	AW38
AN26	GND	GND	AW4
AN28	GND	GND	AW40
AN3	GND	GND	AW44
AN30	GND	GND	AW47
AN32	GND	GND	AW48
AN34	GND	GND	AW49
AN36	GND	GND	AW5
AN38	GND	GND	AW8
AN4	GND	GND	AY1
AN40	GND	GND	AY11
AN43	GND	GND	AY19
AN47	GND	GND	AY2
AN48	GND	GND	AY29
AN49	GND	GND	AY38
AN5	GND	GND	AY41
AN9	GND	GND	AY46
AP1	GND	GND	AY47
AP10	GND	GND	AY5
AP15	GND	GND	AY50
AP17	GND	GND	AY51
AP19	GND	GND	AY6
AP2	GND	GND	B10
AP21	GND	GND	B14
AP23	GND	GND	B16
AP25	GND	GND	B19
AP27	GND	GND	B20
AP29	GND	GND	B21
AP31	GND	GND	B23
AP33	GND	GND	B3
AP35	GND	GND	B31
AP37	GND	GND	B32
AP38	GND	GND	B33

GND GND

U77-3 FPGA_VU13P_A2577

B36	GND	GND	BG12
B38	GND	GND	BG16
B4	GND	GND	BG17
B42	GND	GND	BG18
B45	GND	GND	BG21
B46	GND	GND	BG28
B47	GND	GND	BG3
B48	GND	GND	BG31
B49	GND	GND	BG34
B5	GND	GND	BG35
B6	GND	GND	BG36
B7	GND	GND	BG4
BA12	GND	GND	BG40
BA14	GND	GND	BG44
BA16	GND	GND	BG45
BA26	GND	GND	BG48
BA3	GND	GND	BG49
BA36	GND	GND	BG7
BA38	GND	GND	BG8
BA4	GND	GND	BH1
BA40	GND	GND	BH11
BA43	GND	GND	BH15
BA47	GND	GND	BH16
BA48	GND	GND	BH19
BA49	GND	GND	BH2
BA5	GND	GND	BH20
BA9	GND	GND	BH21
BB1	GND	GND	BH25
BB10	GND	GND	BH31
BB2	GND	GND	BH32
BB23	GND	GND	BH33
BB33	GND	GND	BH36
BB38	GND	GND	BH37
BB42	GND	GND	BH41
BB45	GND	GND	BH45
BB47	GND	GND	BH46
BB5	GND	GND	BH47
BB50	GND	GND	BH5
BB51	GND	GND	BH50
BB7	GND	GND	BH51
BC12	GND	GND	BH6
BC14	GND	GND	BH7
BC20	GND	GND	BJ13
BC3	GND	GND	BJ16
BC30	GND	GND	BJ17
BC38	GND	GND	BJ18
BC4	GND	GND	BJ2
BC40	GND	GND	BJ21
BC44	GND	GND	BJ22
BC47	GND	GND	BJ3
BC48	GND	GND	BJ31
BC49	GND	GND	BJ34
BC5	GND	GND	BJ35
BC8	GND	GND	BJ36
BD1	GND	GND	BJ39
BD11	GND	GND	BJ4
BD14	GND	GND	BJ43
BD2	GND	GND	BJ45
BD27	GND	GND	BJ48
BD38	GND	GND	BJ49
BD41	GND	GND	BJ50
BD46	GND	GND	BJ7
BD47	GND	GND	BJ9
BD5	GND	GND	BK10
BD50	GND	GND	BK14
BD51	GND	GND	BK16
BD6	GND	GND	BK19
BE12	GND	GND	BK20
BE14	GND	GND	BK21
BE15	GND	GND	BK29
BE16	GND	GND	BK3
BE17	GND	GND	BK31
BE18	GND	GND	BK32
BE19	GND	GND	BK33
BE24	GND	GND	BK36
BE3	GND	GND	BK38
BE33	GND	GND	BK4
BE34	GND	GND	BK42
BE35	GND	GND	BK45
BE36	GND	GND	BK46
BE37	GND	GND	BK47
BE38	GND	GND	BK48
BE4	GND	GND	BK49
BE40	GND	GND	BK5
BE43	GND	GND	BK6
BE47	GND	GND	BK7
BE48	GND	GND	BL12
BE49	GND	GND	BL16
BE5	GND	GND	BL17
BE9	GND	GND	BL18
BF1	GND	GND	BL21
BF10	GND	GND	BL26
BF16	GND	GND	BL31
BF19	GND	GND	BL34
BF2	GND	GND	BL35
BF20	GND	GND	BL36
BF21	GND	GND	BL4
BF31	GND	GND	BL40
BF32	GND	GND	BL44
BF33	GND	GND	BL45
BF36	GND	GND	BL48
BF42	GND	GND	BL7
BF45	GND	GND	BL8
BF46	GND	GND	C12
BF47	GND	GND	C16
BF5	GND	GND	C17
BF50	GND	GND	C18
BF51	GND	GND	C2
BF6	GND	GND	C21
BF7	GND	GND	C3

GND GND

U77-4 FPGA_VU13P_A2577

C31	GND	GND	H35
C34	GND	GND	H36
C35	GND	GND	H37
C36	GND	GND	H38
C4	GND	GND	H41
C40	GND	GND	H46
C44	GND	GND	H47
C45	GND	GND	H5
C48	GND	GND	H50
C49	GND	GND	H51
C50	GND	GND	H6
C7	GND	GND	J12
C8	GND	GND	J14
D1	GND	GND	J22
D11	GND	GND	J3
D15	GND	GND	J38
D16	GND	GND	J4
D19	GND	GND	J40
D2	GND	GND	J43
D20	GND	GND	J47
D21	GND	GND	J48
D27	GND	GND	J49
D31	GND	GND	J5
D32	GND	GND	J9
D33	GND	GND	K1
D36	GND	GND	K10
D37	GND	GND	K14
D41	GND	GND	K19
D45	GND	GND	K2
D46	GND	GND	K29
D47	GND	GND	K38
D5	GND	GND	K42
D50	GND	GND	K45
D51	GND	GND	K47
D6	GND	GND	K5
D7	GND	GND	K50
E12	GND	GND	K51
E16	GND	GND	K7
E17	GND	GND	L12
E18	GND	GND	L14
E21	GND	GND	L16
E24	GND	GND	L26
E3	GND	GND	L3
E31	GND	GND	L36
E34	GND	GND	L38
E35	GND	GND	L4
E36	GND	GND	L40
E39	GND	GND	L44
E4	GND	GND	L47
E43	GND	GND	L48
E45	GND	GND	L49
E48	GND	GND	L5
E49	GND	GND	L8
E7	GND	GND	M1
E9	GND	GND	M11
F1	GND	GND	M2
F10	GND	GND	M23
F14	GND	GND	M33
F16	GND	GND	M38
F19	GND	GND	M41
F2	GND	GND	M46
F20	GND	GND	M47
F21	GND	GND	M5
F31	GND	GND	M50
F32	GND	GND	M51
F33	GND	GND	M6
F36	GND	GND	N13
F38	GND	GND	N14
F42	GND	GND	N20
F45	GND	GND	N3
F46	GND	GND	N30
F47	GND	GND	N38
F5	GND	GND	N39
F50	GND	GND	N4
F51	GND	GND	N43
F6	GND	GND	N47
F7	GND	GND	N48
G12	GND	GND	N49
G16	GND	GND	N5
G18	GND	GND	N9
G21	GND	GND	P1
G28	GND	GND	P10
G3	GND	GND	P17
G31	GND	GND	P2
G34	GND	GND	P27
G36	GND	GND	P37
G4	GND	GND	P38
G40	GND	GND	P42
G44	GND	GND	P45
G47	GND	GND	P47
G48	GND	GND	P5
G49	GND	GND	P50
G5	GND	GND	P51
G8	GND	GND	P7
H1	GND	GND	R12
H11	GND	GND	R14
H14	GND	GND	R24
H15	GND	GND	R3
H16	GND	GND	R34
H17	GND	GND	R38
H18	GND	GND	R4
H19	GND	GND	R40
H2	GND	GND	R44
H20	GND	GND	R47
H21	GND	GND	R48
H25	GND	GND	R49
H31	GND	GND	R5
H32	GND	GND	R8
H33	GND	GND	T1
H34	GND	GND	T11

GND GND

U77-5 FPGA_VU13P_A2577

T2	GND
T21	GND
T38	GND
T41	GND
T46	GND
T47	GND
T5	GND
T50	GND
T51	GND
T6	GND
U13	GND
U14	GND
U18	GND
U28	GND
U3	GND
U30	GND
U38	GND
U39	GND
U4	GND
U43	GND
U47	GND
U48	GND
U49	GND
U5	GND
U9	GND
V1	GND
V10	GND
V2	GND
V23	GND
V25	GND
V27	GND
V29	GND
V31	GND
V38	GND
V42	GND
V45	GND
V47	GND
V5	GND
V50	GND
V51	GND
V7	GND
W12	GND
W14	GND
W18	GND
W20	GND
W22	GND
W24	GND
W26	GND
W28	GND
W3	GND
W30	GND
W34	GND
W36	GND
W38	GND
W4	GND
W40	GND
W44	GND
W47	GND
W48	GND
W49	GND
W5	GND
W8	GND
Y1	GND
Y11	GND
Y15	GND
Y17	GND
Y19	GND
Y2	GND
Y21	GND
Y23	GND
Y25	GND
Y27	GND
Y29	GND
Y31	GND
Y33	GND
Y35	GND
Y37	GND
Y38	GND
Y41	GND
Y46	GND
Y47	GND
Y5	GND
Y50	GND
Y51	GND

GND

R455 10K 0603

V_M3V3

GND Y6 /F2_INSTALLED 24

IF THE FPGA IS INSTALLED, THEN THE ACTIVE-LO "/F2_INSTALLED" SIGNAL WILL BE PULLED TO GND. IF THE FPGA IS NOT INSTALLED, THE SIGNAL WILL BE HI.

ANY FPGA GND PIN CAN BE USED.

APOLLO CM W/ DUAL A2577, MK1

Title: 6.01: FPGA#2 GND

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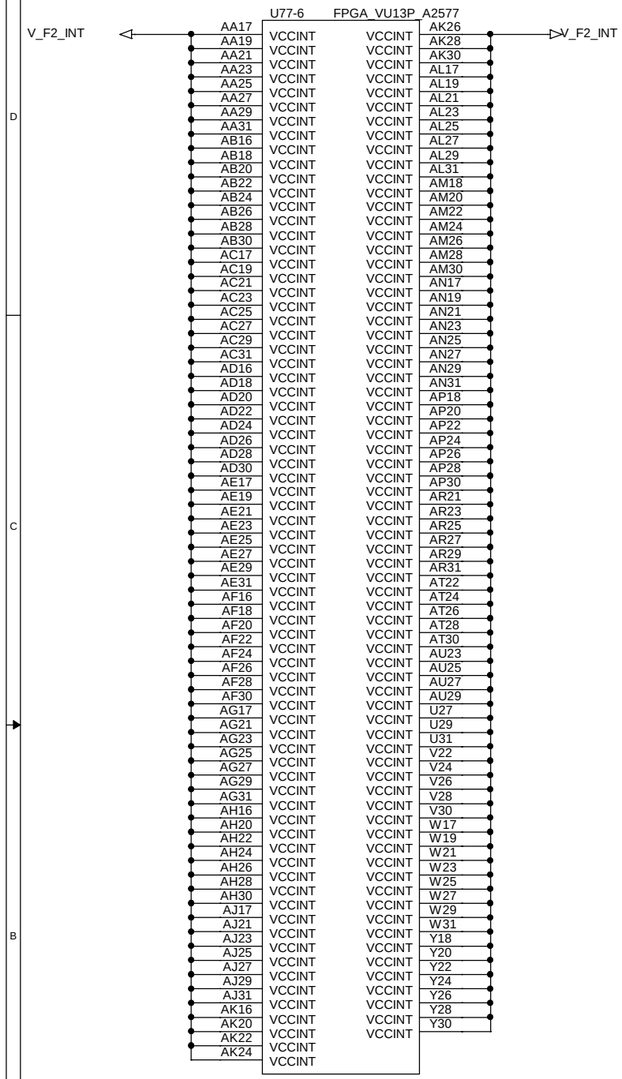
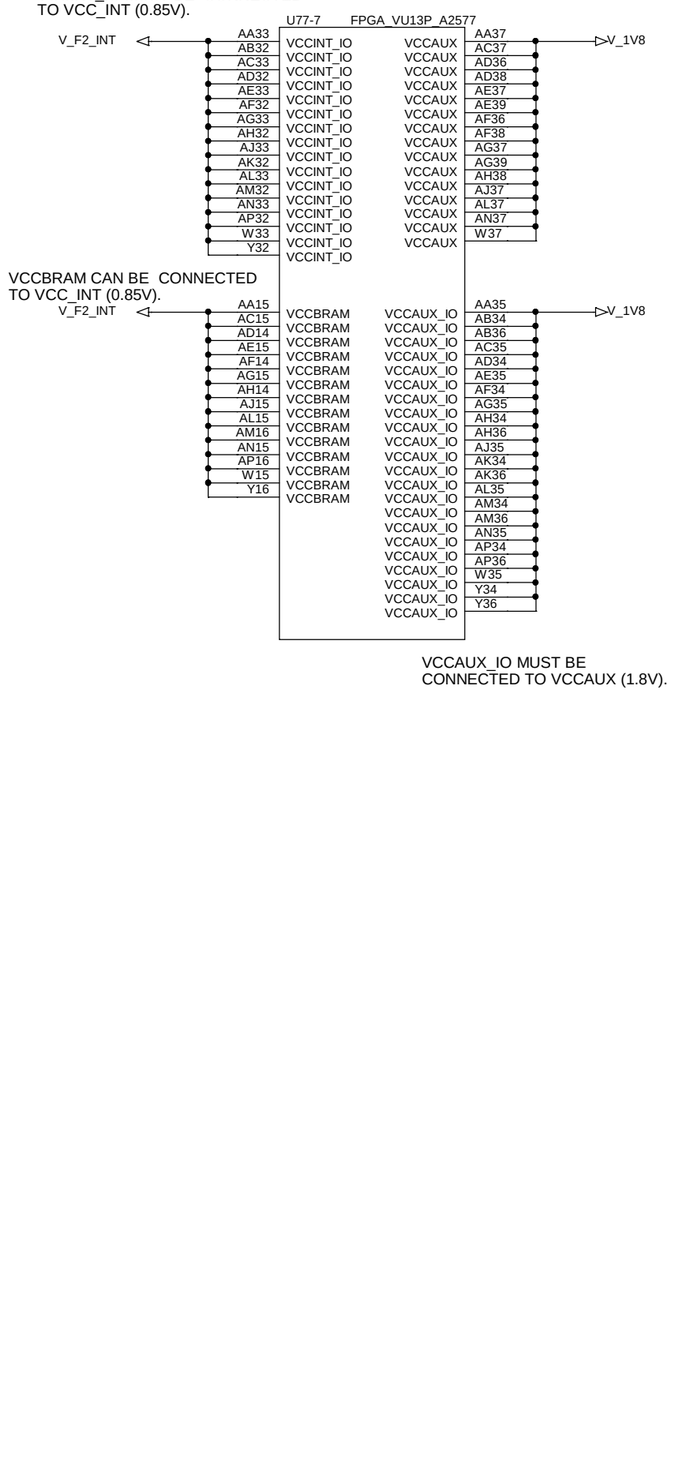
6.02: FPGA#2 POWER INTERNAL

VCCINT MUST BE 0.85V.

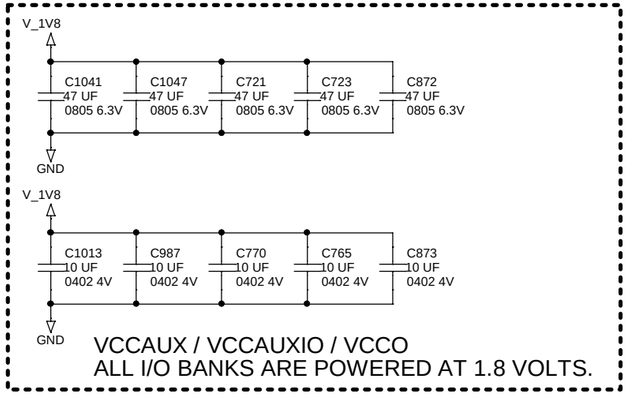


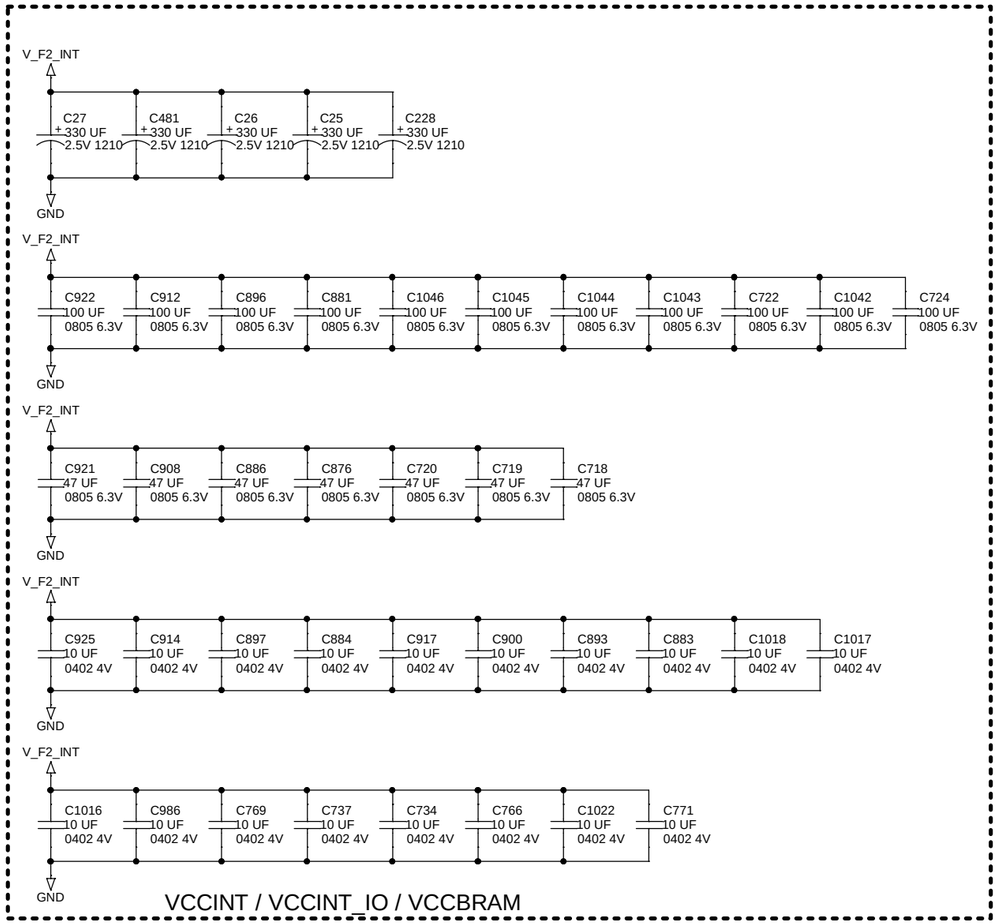
VCCINT_IO MUST BE CONNECTED TO VCC_INT (0.85V).

VCCBRAM CAN BE CONNECTED TO VCC_INT (0.85V).



VCCAUX_IO MUST BE CONNECTED TO VCCAUX (1.8V).





BYPASS CAPACITOR VALUES AND QUANTITIES FROM
"UG583 UltraScale Architecture PCB Design"

APOLLO CM W/ DUAL A2577, MK1		
Title: 6.02: FPGA#2 POWER INTERNAL		
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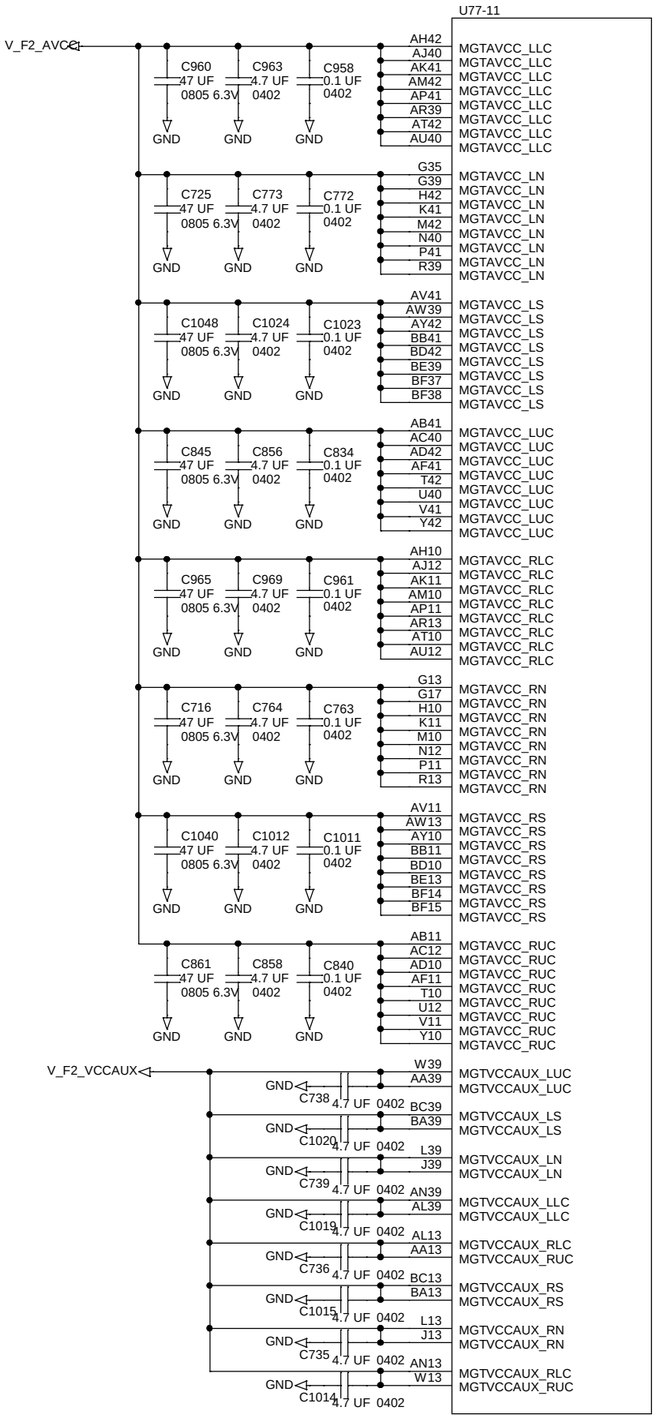
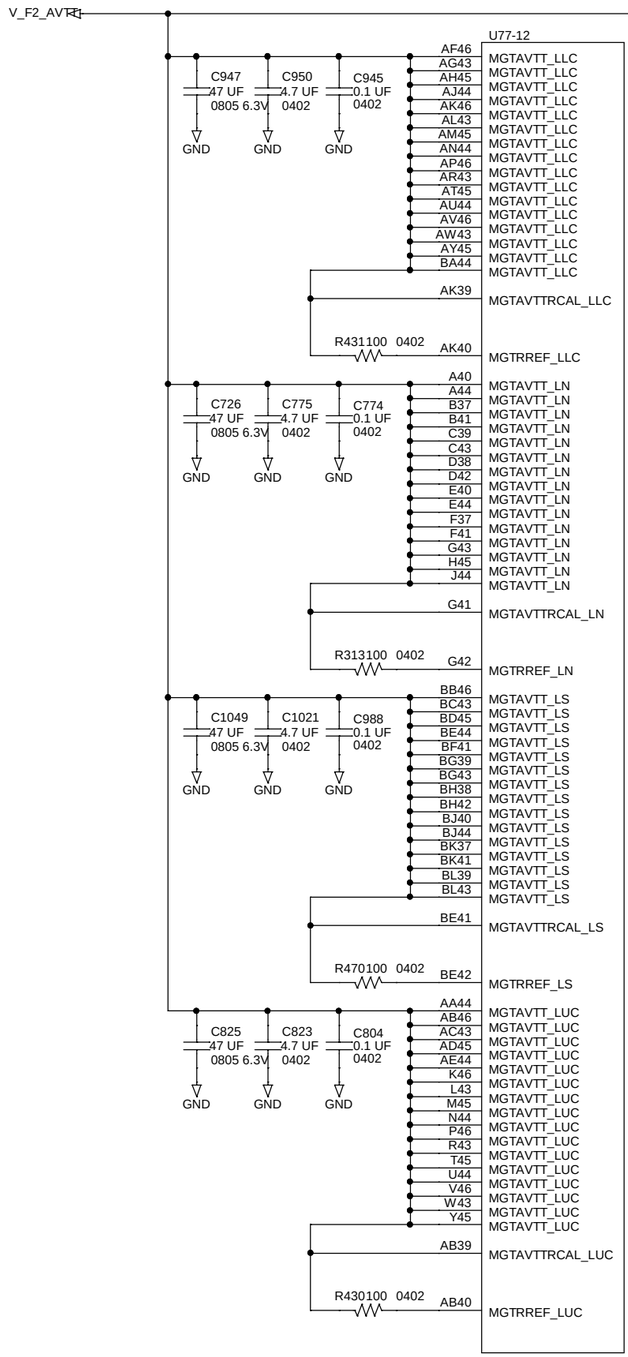
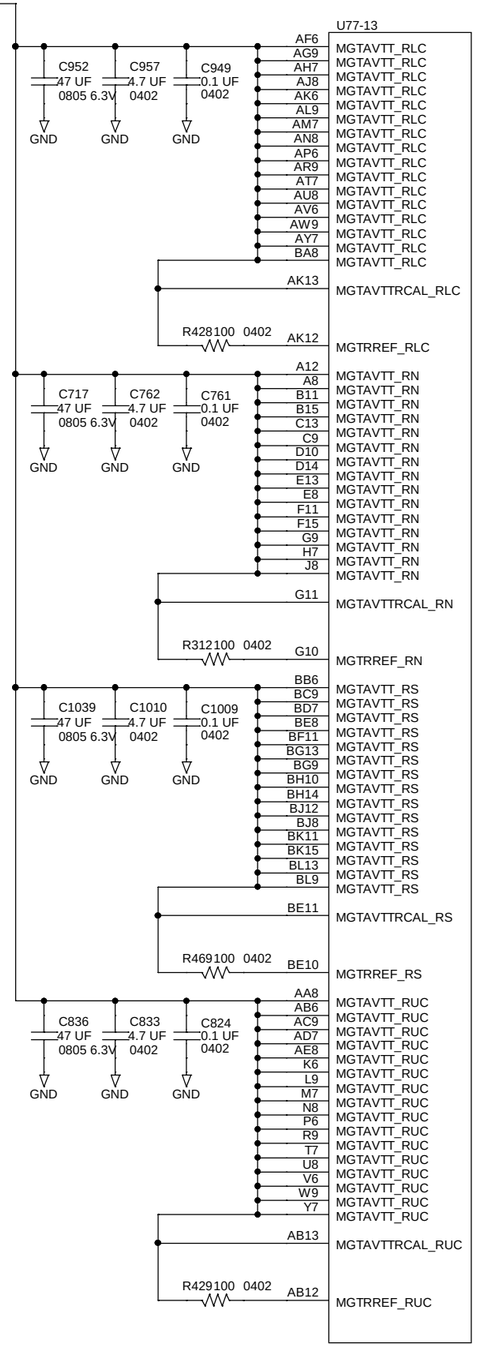
6.03: FPGA#2 GTY TRANSCEIVER POWER







REFER TO THE GTY USER GUIDE FOR DETAILS ON TRACE ROUTING FOR THE MGTRREF RESISTOR.

PLACE CAPACITORS AND RESISTORS THAT ARE ON THIS SHEET NEAR THE BGA PINS.

APOLLO CM W/ DUAL A2577, MK1		
Title: 6.03: FPGA#2 GTY TRANSCEIVER POWER		
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6.04: FPGA#2 CONFIGURATION

MUST BE TIED TO "VCCINT" OR "GND". DO NOT CONNECT TO "VCCO_0". CONNECT TO "GND" FOR STANDARD POR DELAY.

THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

PULLUPS/PULLDOWNS ON THE BOOT MODE CONFIGURATION INPUTS MUST BE 1K OR LESS.

WHEN "FPGA_CFG_FROM_FLASH" IS ASSERTED (HIGH), THE FPGA WILL BE ABLE TO BOOT FROM THE FLASH MEMORY. WHEN IT IS NEGATED (LOW), THE FPGA WILL ONLY BE ABLE TO BOOT FROM JTAG.

FPGA_CFG_FROM_FLASH 24,44

THIS DESIGN DOES NOT USE ENCRYPTION, SO "VBATT" CAN BE TIED TO "GND"

THE FPGA CAN BE REPROGRAMMED BY PULSING "F2_CFG_START" FROM THE MCU.

QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
VU9P 641,272,864
VU13P 906,547,008

MT25QU01

FPGA_VU13P_A2577

Title	APOLLO CM W/ DUAL A2577, MK1
	6.04: FPGA#2 CONFIGURATION
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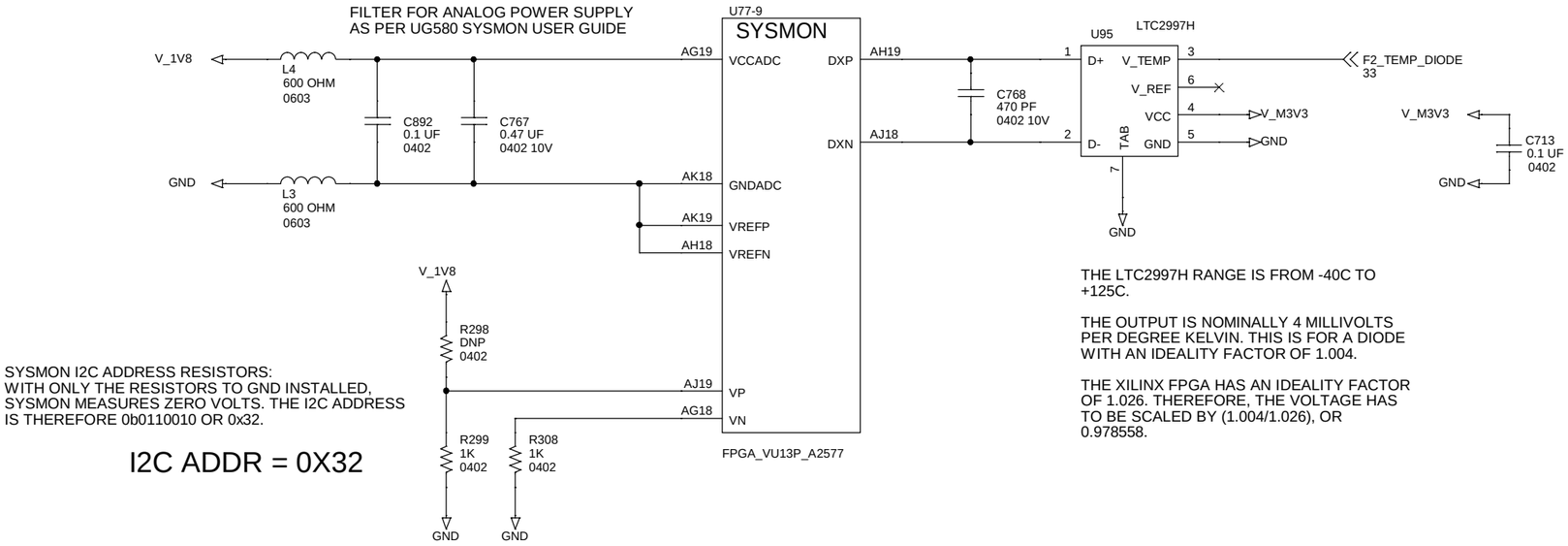
6.05: FPGA#2 SYSMON



APOLLO CM W/ DUAL A2577, MK1		
Title: 6.05: FPGA#2 SYSTEM MONITOR		
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6.06 FPGA#2 I/O SLR0

THESE BANKS ARE NUMBERED THE SAME IN THE VU13P AND VU9P, AND THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#0 FOR THE VU13P AND SLR#0 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
D	61	61
E	62	62
F	63	63

U77-14

BE20	IO_L10N_T1U_N7_QBC_AD4N_61	VCCO_61	AW27
BE21	IO_L10P_T1U_N6_QBC_AD4P_61	VCCO_61	AY24
BF22	IO_L11N_T1U_N9_GC_61	VCCO_61	BC25
BE22	IO_L11P_T1U_N8_GC_61	VCCO_61	BD22
BE23	IO_L12N_T1U_N11_GC_61	VCCO_61	BG23
BD23	IO_L12P_T1U_N10_GC_61	VCCO_61	BK24
BD24	IO_L13N_T2L_N1_GC_QBC_61		
BD25	IO_L13P_T2L_N0_GC_QBC_61	VREF_61	AV23
BC23	IO_L14N_T2L_N3_GC_61		
BC24	IO_L14P_T2L_N2_GC_61		
BB25	IO_L15N_T2L_N5_AD11N_61		
BB26	IO_L15P_T2L_N4_AD11P_61		
BD26	IO_L16N_T2U_N7_QBC_AD3N_61		
BC26	IO_L16P_T2U_N6_QBC_AD3P_61		
BA24	IO_L17N_T2U_N9_AD10N_61		
BA25	IO_L17P_T2U_N8_AD10P_61		
BC22	IO_L18N_T2U_N11_AD2N_61		
BB22	IO_L18P_T2U_N10_AD2P_61		
AW24	IO_L19N_T3L_N1_DBC_AD9N_61		
AW25	IO_L19P_T3L_N0_DBC_AD9P_61		
BL23	IO_L1N_T0L_N1_DBC_61		
BL24	IO_L1P_T0L_N0_DBC_61		
AW23	IO_L20N_T3L_N3_AD1N_61		
AV24	IO_L20P_T3L_N2_AD1P_61		
BA23	IO_L21N_T3L_N5_AD8N_61		
AY23	IO_L21P_T3L_N4_AD8P_61		
BA27	IO_L22N_T3U_N7_DBC_AD0N_61		
AY27	IO_L22P_T3U_N6_DBC_AD0P_61		
AY26	IO_L23N_T3U_N9_61		
AW26	IO_L23P_T3U_N8_61		
AV26	IO_L24N_T3U_N11_61		
AV27	IO_L24P_T3U_N10_61		
BL22	IO_L2N_T0L_N3_61		
BK22	IO_L2P_T0L_N2_61		
BJ24	IO_L3N_T0L_N5_AD15N_61		
BJ25	IO_L3P_T0L_N4_AD15P_61		
BK23	IO_L4N_T0U_N7_DBC_AD7N_61		
BJ23	IO_L4P_T0U_N6_DBC_AD7P_61		
BL25	IO_L5N_T0U_N9_AD14N_61		
BK25	IO_L5P_T0U_N8_AD14P_61		
BH23	IO_L6N_T0U_N11_AD6N_61		
BH24	IO_L6P_T0U_N10_AD6P_61		
BG24	IO_L7N_T1L_N1_QBC_AD13N_61		
BG25	IO_L7P_T1L_N0_QBC_AD13P_61		
BG22	IO_L8N_T1L_N3_AD5N_61		
BF23	IO_L8P_T1L_N2_AD5P_61		
BF24	IO_L9N_T1L_N5_AD12N_61		
BF25	IO_L9P_T1L_N4_AD12P_61		
BH22	IO_T0U_N12_VRP_61		
BE25	IO_T1U_N12_61		
BB24	IO_T2U_N12_61		
AY25	IO_T3U_N12_61		

V_1V8

OMIT "VREF" AND "VRP" RESISTORS ON UNUSED I/O BANKS.

OMIT "VREF" AND "VRP" RESISTORS ON UNUSED I/O BANKS.

FPGA_VU13P_A2577

U77-15

BH27	IO_L10N_T1U_N7_QBC_AD4N_62	VCCO_62	AV30
BH26	IO_L10P_T1U_N6_QBC_AD4P_62	VCCO_62	BA31
BF28	IO_L11N_T1U_N9_GC_62	VCCO_62	BB28
BF27	IO_L11P_T1U_N8_GC_62	VCCO_62	BE29
BE27	IO_L12N_T1U_N11_GC_62	VCCO_62	BF26
BE26	IO_L12P_T1U_N10_GC_62	VCCO_62	BH30
BD29	IO_L13N_T2L_N1_GC_QBC_62	VCCO_62	BJ27
BC28	IO_L13P_T2L_N0_GC_QBC_62		
BE28	IO_L14N_T2L_N3_GC_62	VREF_62	AV28
BD28	IO_L14P_T2L_N2_GC_62		
BE30	IO_L15N_T2L_N5_AD11N_62		
BD30	IO_L15P_T2L_N4_AD11P_62		
BC27	IO_L16N_T2U_N7_QBC_AD3N_62		
BB27	IO_L16P_T2U_N6_QBC_AD3P_62		
BC31	IO_L17N_T2U_N9_AD10N_62		
BB31	IO_L17P_T2U_N8_AD10P_62		
BC29	IO_L18N_T2U_N11_AD2N_62		
BB29	IO_L18P_T2U_N10_AD2P_62		
BA29	IO_L19N_T3L_N1_DBC_AD9N_62		
BA28	IO_L19P_T3L_N0_DBC_AD9P_62		
BJ28	IO_L1N_T0L_N1_DBC_62		
BH28	IO_L1P_T0L_N0_DBC_62		
AY28	IO_L20N_T3L_N3_AD1N_62		
AW28	IO_L20P_T3L_N2_AD1P_62		
BA30	IO_L21N_T3L_N5_AD8N_62		
AY30	IO_L21P_T3L_N4_AD8P_62		
AV31	IO_L22N_T3U_N7_DBC_AD0N_62		
AU31	IO_L22P_T3U_N6_DBC_AD0P_62		
AW29	IO_L23N_T3U_N9_62		
AV29	IO_L23P_T3U_N8_62		
AY31	IO_L24N_T3U_N11_62		
AW31	IO_L24P_T3U_N10_62		
BL28	IO_L2N_T0L_N3_62		
BL27	IO_L2P_T0L_N2_62		
BJ30	IO_L3N_T0L_N5_AD15N_62		
BJ29	IO_L3P_T0L_N4_AD15P_62		
BK28	IO_L4N_T0U_N7_DBC_AD7N_62		
BK27	IO_L4P_T0U_N6_DBC_AD7P_62		
BL30	IO_L5N_T0U_N9_AD14N_62		
BK30	IO_L5P_T0U_N8_AD14P_62		
BK26	IO_L6N_T0U_N11_AD6N_62		
BJ26	IO_L6P_T0U_N10_AD6P_62		
BG27	IO_L7N_T1L_N1_QBC_AD13N_62		
BG26	IO_L7P_T1L_N0_QBC_AD13P_62		
BG30	IO_L8N_T1L_N3_AD5N_62		
BF29	IO_L8P_T1L_N2_AD5P_62		
BH29	IO_L9N_T1L_N5_AD12N_62		
BG29	IO_L9P_T1L_N4_AD12P_62		
BL29	IO_T0U_N12_VRP_62		
BF30	IO_T1U_N12_62		
BB30	IO_T2U_N12_62		
AW30	IO_T3U_N12_62		

V_1V8

R456 1K 0402 GND

nF2_TEST_CONN_0 60
pF2_TEST_CONN_0 60
F2_TEST_CONN_5 60
F2_TEST_CONN_6 60
nF2_TEST_CONN_4 60
pF2_TEST_CONN_4 60
nF2_TEST_CONN_3 60
pF2_TEST_CONN_3 60
nF2_TEST_CONN_2 60
pF2_TEST_CONN_2 60
nF2_TEST_CONN_1 60
pF2_TEST_CONN_1 60

THE TRI-COLOR LED IS CONNECTED TO DIFFERENT PINS ON EACH FPGA, IN ORDER TO SIMPLIFY LAYOUT.

F2_LED_GREEN 24
F2_LED_BLUE 24
F2_LED_RED 24

TH40 MHZ RECOVERED TCDS CLOCK USES PINS BK26 AND BJ26 ON FPGA#1. THE CLOCK FROM FPGA#2 IS NOT USED ANYWHERE, BUT THE PINS ARE RESERVED.

nF1F2_SPARE2 48
pF1F2_SPARE2 48
nF1F2_SPARE1 48
pF1F2_SPARE1 48
nF1F2_SPARE0 48
pF1F2_SPARE0 48

R468 240 0402 GND

FPGA_VU13P_A2577

U77-16

BC36	IO_L10N_T1U_N7_QBC_AD4N_63	VCCO_63	AT36
BB36	IO_L10P_T1U_N6_QBC_AD4P_63	VCCO_63	AU33
BB35	IO_L11N_T1U_N9_GC_63	VCCO_63	AW37
BA35	IO_L11P_T1U_N8_GC_63	VCCO_63	AY34
BB34	IO_L12N_T1U_N11_GC_63	VCCO_63	BC35
BA34	IO_L12P_T1U_N10_GC_63	VCCO_63	BD32
AW36	IO_L13N_T2L_N1_GC_QBC_63		
AW35	IO_L13P_T2L_N0_GC_QBC_63	VREF_63	AR32
AY36	IO_L14N_T2L_N3_GC_63		
AY35	IO_L14P_T2L_N2_GC_63		
AV37	IO_L15N_T2L_N5_AD11N_63		
AV36	IO_L15P_T2L_N4_AD11P_63		
AV33	IO_L16N_T2U_N7_QBC_AD3N_63		
AV32	IO_L16P_T2U_N6_QBC_AD3P_63		
AW34	IO_L17N_T2U_N9_AD10N_63		
AW33	IO_L17P_T2U_N8_AD10P_63		
AV34	IO_L18N_T2U_N11_AD2N_63		
AU34	IO_L18P_T2U_N10_AD2P_63		
AU37	IO_L19N_T3L_N1_DBC_AD9N_63		
AU36	IO_L19P_T3L_N0_DBC_AD9P_63		
BE32	IO_L1N_T0L_N1_DBC_63		
BE31	IO_L1P_T0L_N0_DBC_63		
AU32	IO_L20N_T3L_N3_AD1N_63		
AT32	IO_L20P_T3L_N2_AD1P_63		
AR37	IO_L21N_T3L_N5_AD8N_63		
AR36	IO_L21P_T3L_N4_AD8P_63		
AT34	IO_L22N_T3U_N7_DBC_AD0N_63		
AT33	IO_L22P_T3U_N6_DBC_AD0P_63		
AT35	IO_L23N_T3U_N9_63		
AR35	IO_L23P_T3U_N8_63		
AR34	IO_L24N_T3U_N11_63		
AR33	IO_L24P_T3U_N10_63		
BC32	IO_L2N_T0L_N3_63		
BB32	IO_L2P_T0L_N2_63		
BA32	IO_L3N_T0L_N5_AD15N_63		
AY32	IO_L3P_T0L_N4_AD15P_63		
BA33	IO_L4N_T0U_N7_DBC_AD7N_63		
AY33	IO_L4P_T0U_N6_DBC_AD7P_63		
BD33	IO_L5N_T0U_N9_AD14N_63		
BC33	IO_L5P_T0U_N8_AD14P_63		
BD34	IO_L6N_T0U_N11_AD6N_63		
BC34	IO_L6P_T0U_N10_AD6P_63		
BD36	IO_L7N_T1L_N1_QBC_AD13N_63		
BD35	IO_L7P_T1L_N0_QBC_AD13P_63		
BD37	IO_L8N_T1L_N3_AD5N_63		
BC37	IO_L8P_T1L_N2_AD5P_63		
BB37	IO_L9N_T1L_N5_AD12N_63		
BA37	IO_L9P_T1L_N4_AD12P_63		
BD31	IO_T0U_N12_VRP_63		
AY37	IO_T1U_N12_63		
AU35	IO_T2U_N12_63		
AT37	IO_T3U_N12_63		

V_1V8

OMIT "VREF" AND "VRP" RESISTORS ON UNUSED I/O BANKS.

FPGA_VU13P_A2577

APOLLO CM W/ DUAL A2577, MK1			
Title: 6.06 FPGA#2 I/O SLR0			
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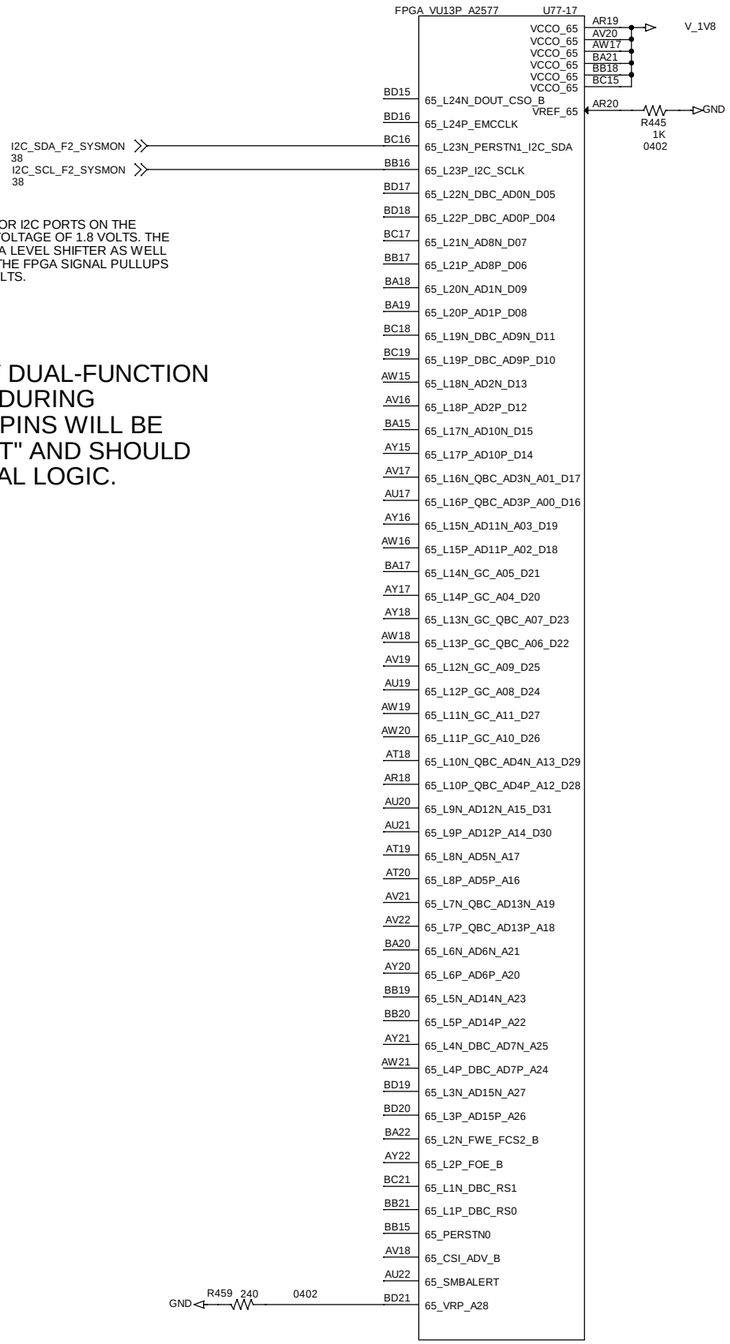
Date: Tuesday, June 15, 2021		Sheet 56 of 84	

THESE BANKS ARE NUMBERED THE SAME IN THE VU13P AND VU9P, AND THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#1 FOR THE VU13P AND SLR#1 FOR THE VU9P.

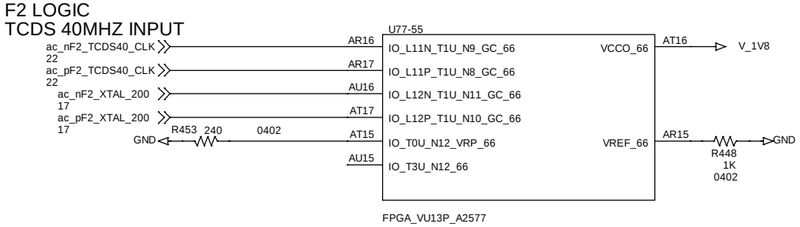
SITE	VU13P BANK	VU9P BANK
C	65	65
B	66	66



THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

F2 LOGIC
TCDS 40MHZ INPUT



APOLLO CM W/ DUAL A2577, MK1			
Title: 6.07 FPGA#2 I/O SLR1			
Size	Document Number: 6089-119		Rev: A
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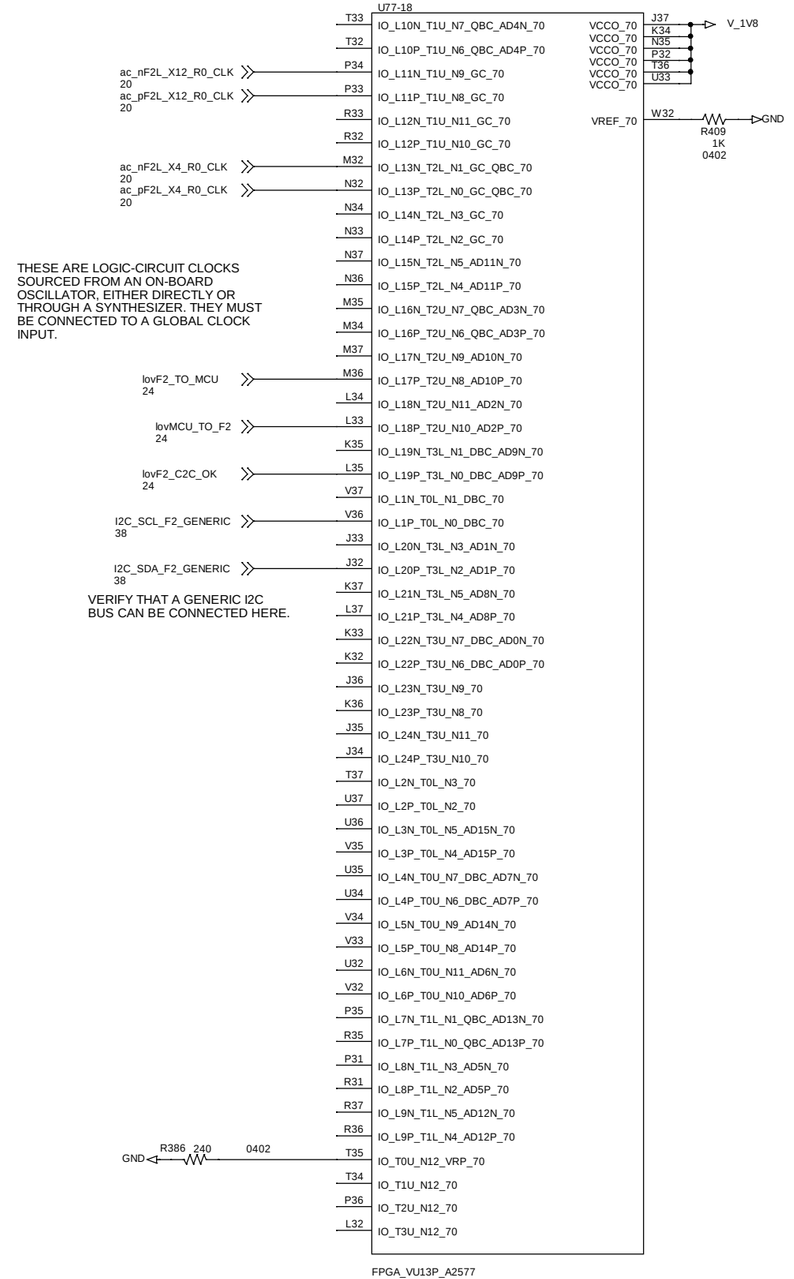
6.08: FPGA#2 I/O SLR2

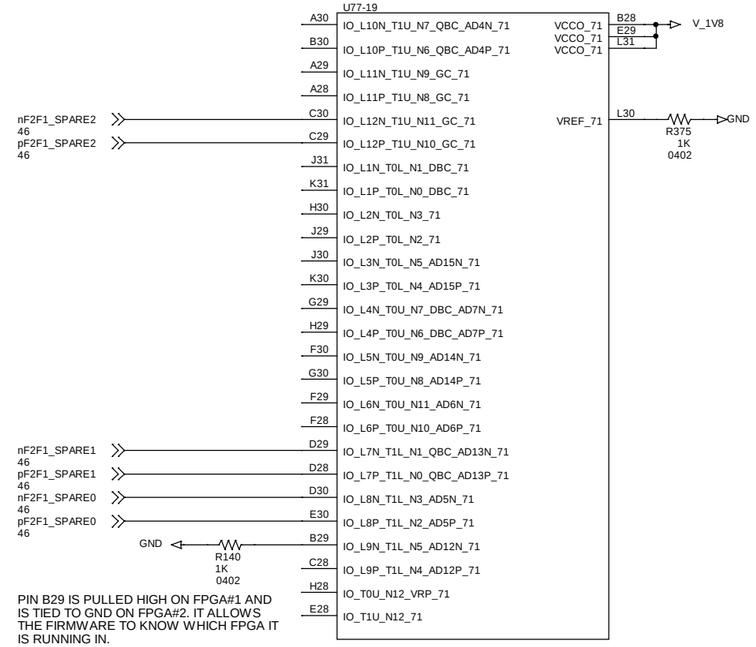
THESE BANKS ARE NUMBERED DIFFERENTLY IN THE VU13P AND VU9P, BUT THE PIN NUMBERS ARE THE SAME.
THEY ARE IN SLR#2 FOR THE VU13P AND SLR#1 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
G	70	67
H	71	68



THESE ARE LOGIC-CIRCUIT CLOCKS SOURCED FROM AN ON-BOARD OSCILLATOR, EITHER DIRECTLY OR THROUGH A SYNTHESIZER. THEY MUST BE CONNECTED TO A GLOBAL CLOCK INPUT.

VERIFY THAT A GENERIC I2C BUS CAN BE CONNECTED HERE.



PIN B29 IS PULLED HIGH ON FPGA#1 AND IS TIED TO GND ON FPGA#2. IT ALLOWS THE FIRMWARE TO KNOW WHICH FPGA IT IS RUNNING IN.

THE "F2F1_SPARE" SIGNALS ARE OUTPUTS FROM F2 AND INPUTS TO F1.
THE "F1F2_SPARE" SIGNALS ARE OUTPUTS FROM F1 AND INPUTS TO F2.
THEY ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE FPGA

APOLLO CM W/ DUAL A2577, MK1

Title: 6.08: FPGA#2 I/O SLR2

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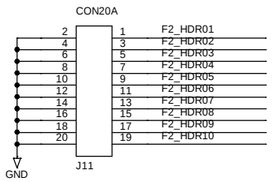
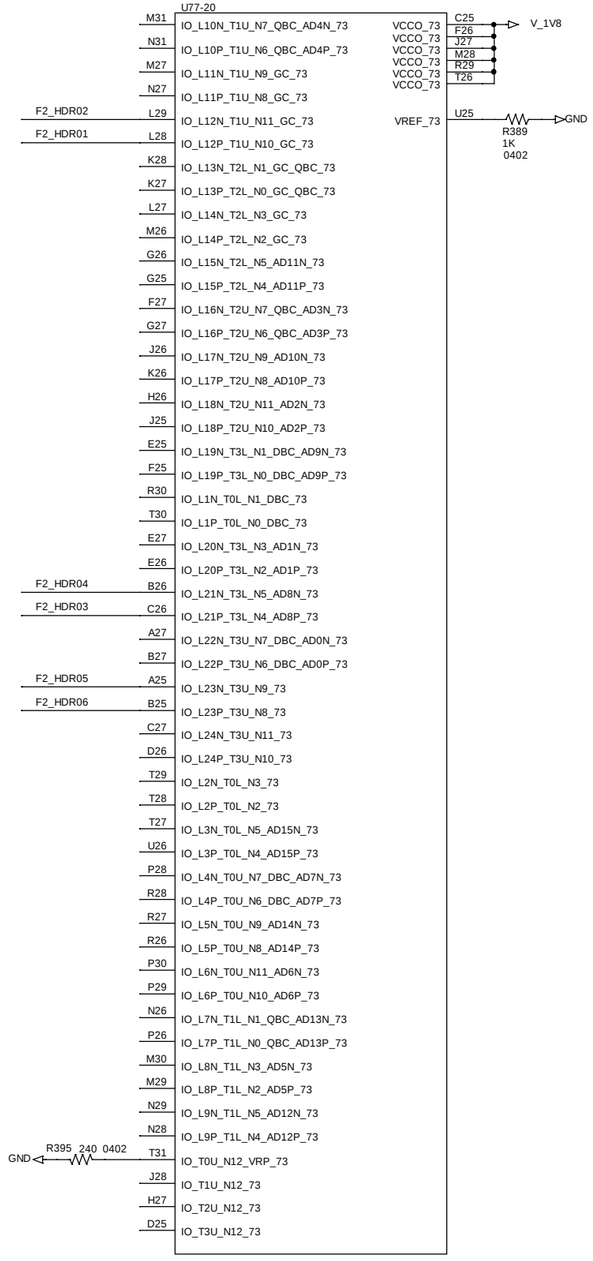
6.09: FPGA#2 I/O SLR3

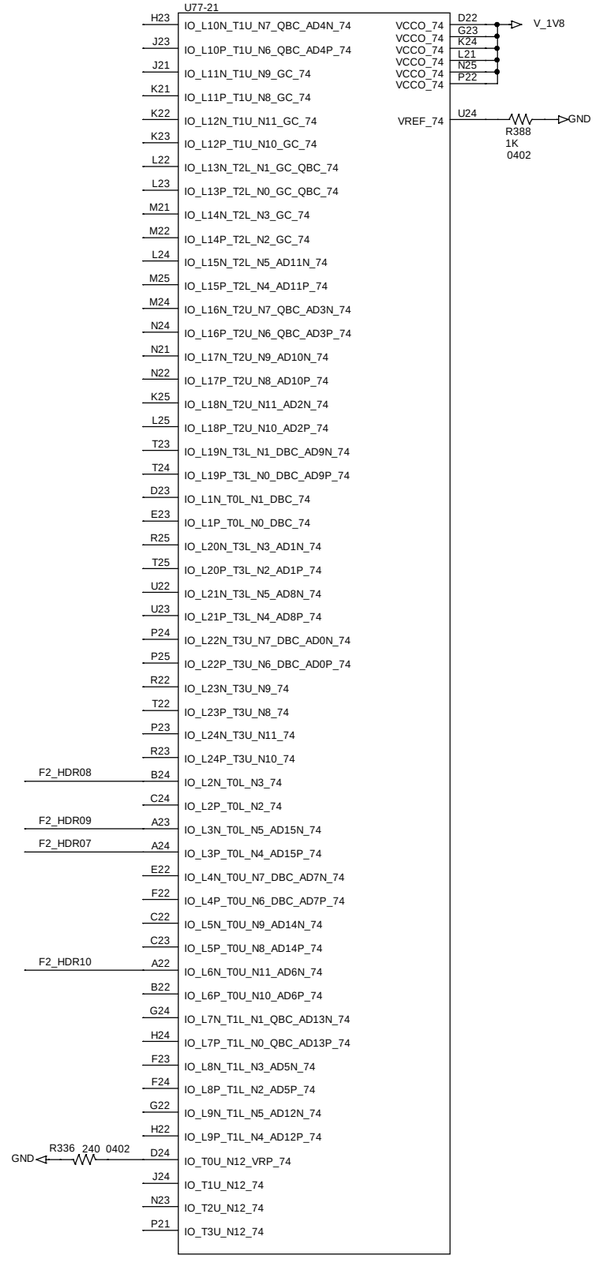


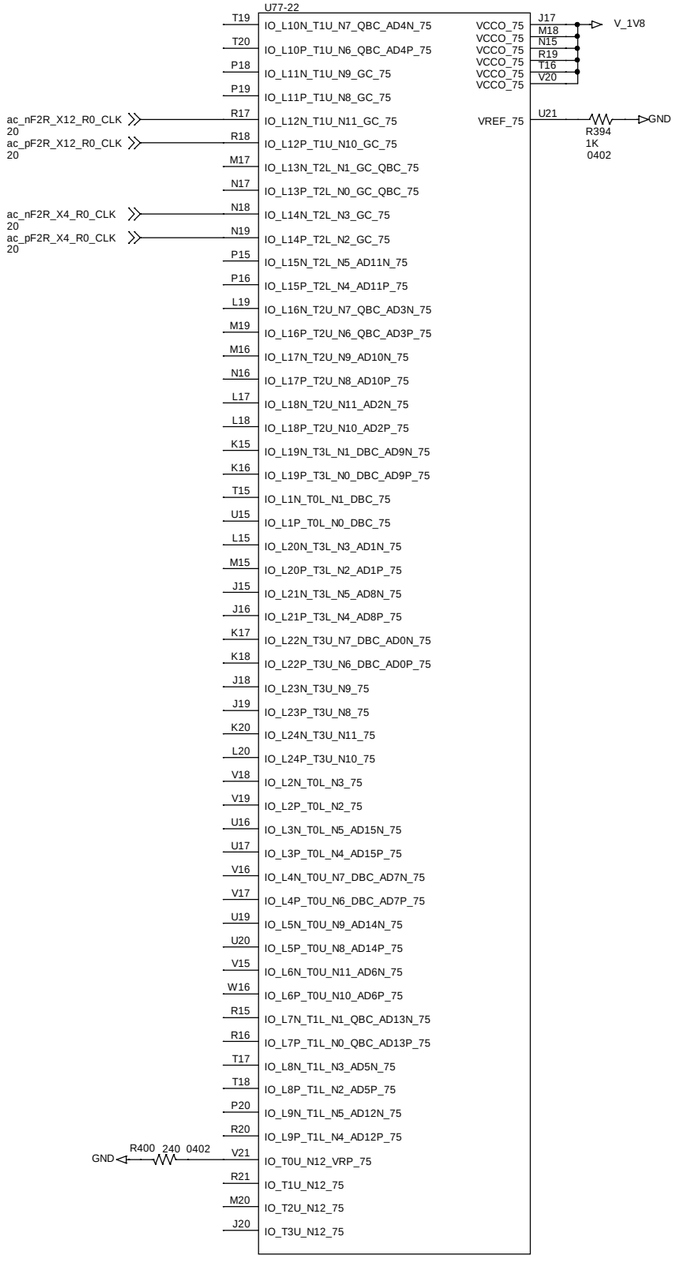
THE "F2_HDRnn" SIGNALS ARE CONNECTED FROM THE FPGA TO PADS ON THE BOTTOM SIDE OF THE BOARD. A 20-PIN HEADER CAN BE ATTACHED. THESE SIGNALS ARE FOR DEBUGGING, OR FUTURE USE. HDR01 AND HDR02 ARE CONNECTED TO CLOCK-CAPABLE INPUTS.

THESE BANKS ARE NUMBERED DIFFERENTLY IN THE VU13P AND VU9P, BUT THE PIN NUMBERS ARE THE SAME. THEY ARE IN SLR#3 FOR THE VU13P AND SLR#2 FOR THE VU9P.

SITE	VU13P BANK	VU9P BANK
I	73	70
J	74	71
K	75	72







APOLLO CM W/ DUAL A2577, MK1			
Title: 6.09: FPGA#2 I/O SLR3			
Size	Document Number: 6089-119		Rev: A
Date: Thursday, June 24, 2021	Sheet 59 of 84		

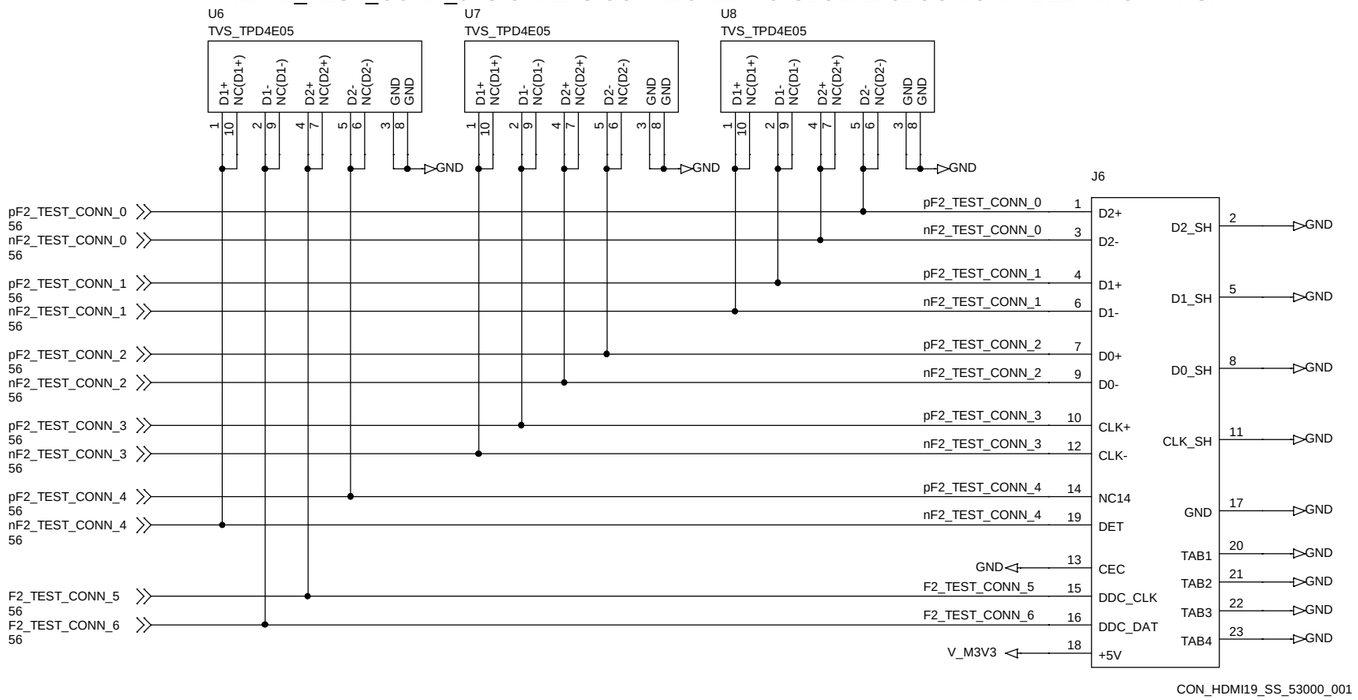
6.10 FPGA#2 TEST CONNECTOR

THIS CONNECTOR IS LOCATED ON THE FRONT PANEL. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

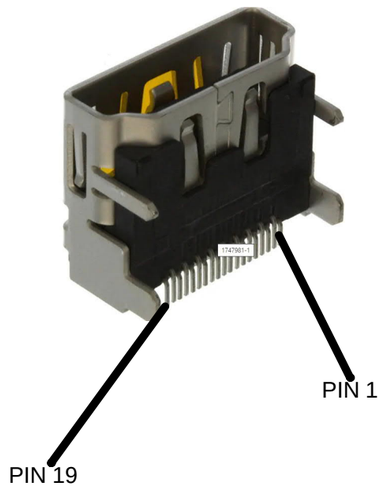
TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

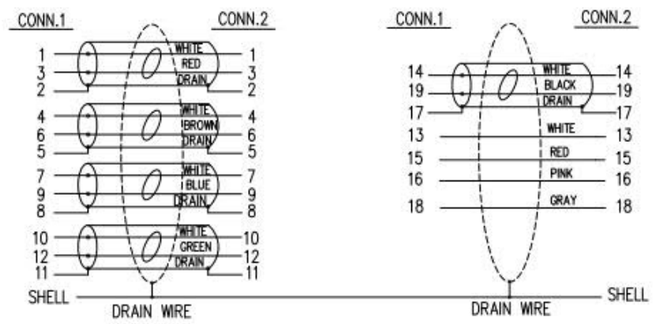
THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "F2_TEST_CONN_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.



PIN ASSIGNMENT





APOLLO CM W/ DUAL A2577, MK1		
Title: 6.10 FPGA#2 TEST CONNECTOR		
Size	Document Number: 6089-119	Rev: A
Date: Tuesday, June 15, 2021	Sheet 60 of 84	

7.01: FPGA#1 SM C2C ON QUAD L

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

APOLLO CM W/ DUAL A2577, MK1		
Title: 7.01: FPGA#1 SM C2C ON QUAD L		
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7.02: FPGA#1 FF#1 X12 ON QUADS AC AD AE

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_AD 20
ac_nF1L_R0_AD 20
ac_pF1L_R1_AD 22
ac_nF1L_R1_AD 22

V_M3V3
R538 3.3K 0603
R539 3.3K 0603
R541 2.2K 0603
R540 2.2K 0603

U24-1 FIREFLY_XMIT_X12 FIREFLY XMIT X12

/F1_FF_RESET 39,62,63,64,65,66,67,68
I2C_SDA_F1_FF1_XMIT 39
I2C_SCL_F1_FF1_XMIT 39
/F1_FF1_XMIT_INT 39
/F1_FF1_XMIT_PRESENT 39
V_3V3
V_F1_FF1_XMIT 32

/RESET G1 G2
SDA
SCL
/SELECT
/INT
/PRESENT
3.3V
3.8/3.3V >=25G 3.8V <=16G 3.3V
RSVD
GND

C1053 +-22 UF 0603 6.3V
C1087 0.1 UF 0402
L5 1.0 UH 0806
C1121 +-22 UF 0603 6.3V
C1169 0.1 UF 0402
C1054 +-22 UF 0603 6.3V
C1088 0.1 UF 0402
L6 1.0 UH 0806
C1122 +-22 UF 0603 6.3V
C1170 0.1 UF 0402

<Implementation>

U24-2 FIREFLY_XMIT_X12 FIREFLY XMIT X12

B19 A19	GND_B19 GND_A19	0P 0N	B18 B17	pF1_FF1_XMIT0 nF1_FF1_XMIT0
		1P 1N	A18 A17	pF1_FF1_XMIT1 nF1_FF1_XMIT1
B16 A16	GND_B16 GND_A16	2P 2N	B15 B14	pF1_FF1_XMIT2 nF1_FF1_XMIT2
		3P 3N	A15 A14	pF1_FF1_XMIT3 nF1_FF1_XMIT3
B13 A13	GND_B13 GND_A13	4P 4N	B12 B11	pF1_FF1_XMIT4 nF1_FF1_XMIT4
		5P 5N	A12 A11	pF1_FF1_XMIT5 nF1_FF1_XMIT5
B10 A10	GND_B10 GND_A10	6P 6N	B9 B8	pF1_FF1_XMIT6 nF1_FF1_XMIT6
		7P 7N	A9 A8	pF1_FF1_XMIT7 nF1_FF1_XMIT7
B7 A7	GND_B7 GND_A7	8P 8N	B6 B5	pF1_FF1_XMIT8 nF1_FF1_XMIT8
		9P 9N	A6 A5	pF1_FF1_XMIT9 nF1_FF1_XMIT9
B4 A4	GND_B4 GND_A4	10P 10N	B3 B2	pF1_FF1_XMIT10 nF1_FF1_XMIT10
B1 A1	GND_B1 GND_A1	11P 11N	A3 A2	pF1_FF1_XMIT11 nF1_FF1_XMIT11

GND 3 1 G1 2 G2 VA6 … VA1

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U75-24 AC GTY QUAD 121

	BB39 BB40	MGTREFCLK0P_121 MGTREFCLK0N_121
	BA41 BA42	MGTREFCLK1P_121 MGTREFCLK1N_121
pF1_FF1_RECV11 nF1_FF1_RECV11	BK34 BK35	MGTYRXP0_121 MGTYRXN0_121
pF1_FF1_XMIT11 nF1_FF1_XMIT11	BL37 BL38	MGTYTXP0_121 MGTYTXN0_121
pF1_FF1_RECV10 nF1_FF1_RECV10	BL32 BL33	MGTYRXP1_121 MGTYRXN1_121
pF1_FF1_XMIT10 nF1_FF1_XMIT10	BK39 BK40	MGTYTXP1_121 MGTYTXN1_121
pF1_FF1_RECV9 nF1_FF1_RECV9	BL46 BL47	MGTYRXP2_121 MGTYRXN2_121
pF1_FF1_XMIT9 nF1_FF1_XMIT9	BL41 BL42	MGTYTXP2_121 MGTYTXN2_121
pF1_FF1_RECV8 nF1_FF1_RECV8	BJ46 BJ47	MGTYRXP3_121 MGTYRXN3_121
pF1_FF1_XMIT8 nF1_FF1_XMIT8	BK43 BK44	MGTYTXP3_121 MGTYTXN3_121

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U75-25 AD GTY QUAD 122

	AY39 AY40	MGTREFCLK0P_122 MGTREFCLK0N_122
	AW41 AW42	MGTREFCLK1P_122 MGTREFCLK1N_122
pF1_FF1_RECV7 nF1_FF1_RECV7	BH48 BH49	MGTYRXP0_122 MGTYRXN0_122
pF1_FF1_XMIT7 nF1_FF1_XMIT7	BG41 BG42	MGTYTXP0_122 MGTYTXN0_122
pF1_FF1_RECV6 nF1_FF1_RECV6	BG50 BG51	MGTYRXP1_122 MGTYRXN1_122
pF1_FF1_XMIT6 nF1_FF1_XMIT6	BJ41 BJ42	MGTYTXP1_122 MGTYTXN1_122
pF1_FF1_RECV5 nF1_FF1_RECV5	BG46 BG47	MGTYRXP2_122 MGTYRXN2_122
pF1_FF1_XMIT5 nF1_FF1_XMIT5	BH43 BH44	MGTYTXP2_122 MGTYTXN2_122
pF1_FF1_RECV4 nF1_FF1_RECV4	BF48 BF49	MGTYRXP3_122 MGTYRXN3_122
pF1_FF1_XMIT4 nF1_FF1_XMIT4	BF43 BF44	MGTYTXP3_122 MGTYTXN3_122

FPGA_VU13P_A2577

V_M3V3
R542 3.3K 0603
R543 3.3K 0603
R545 2.2K 0603
R544 2.2K 0603

U25-1 FIREFLY_RECV_X12 FIREFLY RECV X12

/F1_FF_RESET 39,62,63,64,65,66,67,68
I2C_SDA_F1_FF1_RECV 39
I2C_SCL_F1_FF1_RECV 39
/F1_FF1_RECV_INT 39
/F1_FF1_RECV_PRESENT 39
V_3V3

/RESET G1 G2
SDA
SCL
/SELECT
/INT
/PRESENT
3.3V
3.3V
RSVD
GND

C1073 +-22 UF 0603 6.3V
C1089 0.1 UF 0402
L7 1.0 UH 0806
C1123 +-22 UF 0603 6.3V
C1171 0.1 UF 0402
L8 1.0 UH 0806
C1124 +-22 UF 0603 6.3V
C1172 0.1 UF 0402

<Implementation>

U25-2 FIREFLY_RECV_X12 FIREFLY RECV X12

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17	pF1_FF1_RECV0 nF1_FF1_RECV0
		1P 1N	B18 B17	pF1_FF1_RECV1 nF1_FF1_RECV1
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14	pF1_FF1_RECV2 nF1_FF1_RECV2
		3P 3N	B15 B14	pF1_FF1_RECV3 nF1_FF1_RECV3
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11	pF1_FF1_RECV4 nF1_FF1_RECV4
		5P 5N	B12 B11	pF1_FF1_RECV5 nF1_FF1_RECV5
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8	pF1_FF1_RECV6 nF1_FF1_RECV6
		7P 7N	B9 B8	pF1_FF1_RECV7 nF1_FF1_RECV7
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5	pF1_FF1_RECV8 nF1_FF1_RECV8
		9P 9N	B6 B5	pF1_FF1_RECV9 nF1_FF1_RECV9
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2	pF1_FF1_RECV10 nF1_FF1_RECV10
B1 A1	GND_B1 GND_A1	11P 11N	B3 B2	pF1_FF1_RECV11 nF1_FF1_RECV11

GND 3 1 G1 2 G2 VA12 … VA7

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

U75-26 AE GTY QUAD 123

	AV39 AV40	MGTREFCLK0P_123 MGTREFCLK0N_123
	AU41 AU42	MGTREFCLK1P_123 MGTREFCLK1N_123
pF1_FF1_RECV3 nF1_FF1_RECV3	BE50 BE51	MGTYRXP0_123 MGTYRXN0_123
pF1_FF1_XMIT3 nF1_FF1_XMIT3	BE45 BE46	MGTYTXP0_123 MGTYTXN0_123
pF1_FF1_RECV2 nF1_FF1_RECV2	BD48 BD49	MGTYRXP1_123 MGTYRXN1_123
pF1_FF1_XMIT2 nF1_FF1_XMIT2	BD43 BD44	MGTYTXP1_123 MGTYTXN1_123
pF1_FF1_RECV1 nF1_FF1_RECV1	BC50 BC51	MGTYRXP2_123 MGTYRXN2_123
pF1_FF1_XMIT1 nF1_FF1_XMIT1	BC45 BC46	MGTYTXP2_123 MGTYTXN2_123
pF1_FF1_RECV0 nF1_FF1_RECV0	BB48 BB49	MGTYRXP3_123 MGTYRXN3_123
pF1_FF1_XMIT0 nF1_FF1_XMIT0	BB43 BB44	MGTYTXP3_123 MGTYTXN3_123

FPGA_VU13P_A2577

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1

Title: 7.02: FPGA#1 FF#1 X12 ON QUADS AC AD AE

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7.03: FPGA#1 FF#2 X12 ON QUADS Q R S

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_R 20
ac_nF1L_R0_R 20
ac_pF1L_R1_R 22
ac_nF1L_R1_R 22

V_M3V3 — R550 3.3K 0603 — R551 3.3K 0603 — R553 2.2K 0603 — R552 2.2K 0603

/F1_FF_RESET 39,62,63,64,65,66,67,68
I2C_SDA_F1_FF2_XMIT 39
I2C_SCL_F1_FF2_XMIT 39
/F1_FF2_XMIT_INT 39
/F1_FF2_XMIT_PRESENT 39

V_3V3 — C1056 22 UF 0603 6.3V — C1092 0.1 UF 0402 — L12 1.0 UH 0806 — C1128 22 UF 0603 6.3V — C1176 0.1 UF 0402

V_F1_FF2_XMIT 32 — C1057 22 UF 0603 6.3V — C1093 0.1 UF 0402 — L13 1.0 UH 0806 — C1129 22 UF 0603 6.3V — C1177 0.1 UF 0402

U27-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

6	/RESET	G1 G2
7	SDA	
8	SCL	
4	/SELECT	GND
5	/INT	
3	/PRESENT	
1	3.3V	
10	3.8/3.3V >=25G 3.8V <=16G 3.3V	
9	RSVD	
2	GND	GND

<Implementation>

U27-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

B19 A19	GND_B19 GND_A19	0P 0N	B18 B17 — pF1_FF2_XMIT0 / nF1_FF2_XMIT0
		1P 1N	A18 A17 — pF1_FF2_XMIT1 / nF1_FF2_XMIT1
B16 A16	GND_B16 GND_A16	2P 2N	B15 B14 — pF1_FF2_XMIT2 / nF1_FF2_XMIT2
		3P 3N	A15 A14 — pF1_FF2_XMIT3 / nF1_FF2_XMIT3
B13 A13	GND_B13 GND_A13	4P 4N	B12 B11 — pF1_FF2_XMIT4 / nF1_FF2_XMIT4
		5P 5N	A12 A11 — pF1_FF2_XMIT5 / nF1_FF2_XMIT5
B10 A10	GND_B10 GND_A10	6P 6N	B9 B8 — pF1_FF2_XMIT6 / nF1_FF2_XMIT6
		7P 7N	A9 A8 — pF1_FF2_XMIT7 / nF1_FF2_XMIT7
B7 A7	GND_B7 GND_A7	8P 8N	B6 B5 — pF1_FF2_XMIT8 / nF1_FF2_XMIT8
		9P 9N	A6 A5 — pF1_FF2_XMIT9 / nF1_FF2_XMIT9
B4 A4	GND_B4 GND_A4	10P 10N	B3 B2 — pF1_FF2_XMIT10 / nF1_FF2_XMIT10
		11P 11N	A3 A2 — pF1_FF2_XMIT11 / nF1_FF2_XMIT11
B1 A1	GND_B1 GND_A1		

GND — 1 G1 2 G2 — A22 A21 A20 A19 A18 A17

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U75-28 Q — GTY QUAD 125

AP39 AP40	MGTREFCLK0P_125 MGTREFCLK0N_125
AN41 AN42	MGTREFCLK1P_125 MGTREFCLK1N_125
pF1_FF2_RECV11 AU50 / nF1_FF2_RECV11 AU51	MGTYRXP0_125 MGTYRXN0_125
pF1_FF2_XMIT11 AU45 / nF1_FF2_XMIT11 AU46	MGTYTXP0_125 MGTYTXN0_125
pF1_FF2_RECV10 AT48 / nF1_FF2_RECV10 AT49	MGTYRXP1_125 MGTYRXN1_125
pF1_FF2_XMIT10 AT43 / nF1_FF2_XMIT10 AT44	MGTYTXP1_125 MGTYTXN1_125
pF1_FF2_RECV9 AR50 / nF1_FF2_RECV9 AR51	MGTYRXP2_125 MGTYRXN2_125
pF1_FF2_XMIT9 AR45 / nF1_FF2_XMIT9 AR46	MGTYTXP2_125 MGTYTXN2_125
pF1_FF2_RECV8 AP48 / nF1_FF2_RECV8 AP49	MGTYRXP3_125 MGTYRXN3_125
pF1_FF2_XMIT8 AP43 / nF1_FF2_XMIT8 AP44	MGTYTXP3_125 MGTYTXN3_125

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U75-29 R — GTY QUAD 126

AM39 AM40	MGTREFCLK0P_126 MGTREFCLK0N_126
AL41 AL42	MGTREFCLK1P_126 MGTREFCLK1N_126
pF1_FF2_RECV7 AN50 / nF1_FF2_RECV7 AN51	MGTYRXP0_126 MGTYRXN0_126
pF1_FF2_XMIT7 AN45 / nF1_FF2_XMIT7 AN46	MGTYTXP0_126 MGTYTXN0_126
pF1_FF2_RECV6 AM48 / nF1_FF2_RECV6 AM49	MGTYRXP1_126 MGTYRXN1_126
pF1_FF2_XMIT6 AM43 / nF1_FF2_XMIT6 AM44	MGTYTXP1_126 MGTYTXN1_126
pF1_FF2_RECV5 AL50 / nF1_FF2_RECV5 AL51	MGTYRXP2_126 MGTYRXN2_126
pF1_FF2_XMIT5 AL45 / nF1_FF2_XMIT5 AL46	MGTYTXP2_126 MGTYTXN2_126
pF1_FF2_RECV4 AK48 / nF1_FF2_RECV4 AK49	MGTYRXP3_126 MGTYRXN3_126
pF1_FF2_XMIT4 AK43 / nF1_FF2_XMIT4 AK44	MGTYTXP3_126 MGTYTXN3_126

FPGA_VU13P_A2577

V_M3V3 — R554 3.3K 0603 — R555 3.3K 0603 — R557 2.2K 0603 — R556 2.2K 0603

/F1_FF_RESET 39,62,63,64,65,66,67,68
I2C_SDA_F1_FF2_RECV 39
I2C_SCL_F1_FF2_RECV 39
/F1_FF2_RECV_INT 39
/F1_FF2_RECV_PRESENT 39

V_3V3 — C1075 22 UF 0603 6.3V — C1094 0.1 UF 0402 — L14 1.0 UH 0806 — C1130 22 UF 0603 6.3V — C1178 0.1 UF 0402

L15 1.0 UH 0806 — C1131 22 UF 0603 6.3V — C1179 0.1 UF 0402

U28-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

6	/RESET	G1 G2
7	SDA	
8	SCL	
4	/SELECT	GND
5	/INT	
3	/PRESENT	
1	3.3V	
10	3.3V	
9	RSVD	
2	GND	GND

<Implementation>

U28-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17 — pF1_FF2_RECV0 / nF1_FF2_RECV0
		1P 1N	B18 B17 — pF1_FF2_RECV1 / nF1_FF2_RECV1
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14 — pF1_FF2_RECV2 / nF1_FF2_RECV2
		3P 3N	B15 B14 — pF1_FF2_RECV3 / nF1_FF2_RECV3
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11 — pF1_FF2_RECV4 / nF1_FF2_RECV4
		5P 5N	B12 B11 — pF1_FF2_RECV5 / nF1_FF2_RECV5
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8 — pF1_FF2_RECV6 / nF1_FF2_RECV6
		7P 7N	B9 B8 — pF1_FF2_RECV7 / nF1_FF2_RECV7
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5 — pF1_FF2_RECV8 / nF1_FF2_RECV8
		9P 9N	B6 B5 — pF1_FF2_RECV9 / nF1_FF2_RECV9
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2 — pF1_FF2_RECV10 / nF1_FF2_RECV10
		11P 11N	B3 B2 — pF1_FF2_RECV11 / nF1_FF2_RECV11
B1 A1	GND_B1 GND_A1		

GND — 1 G1 2 G2 — A25 A27 A26 A25 A24 A23

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U75-30 S — GTY QUAD 127

AJ41 AJ42	MGTREFCLK0P_127 MGTREFCLK0N_127
AG41 AG42	MGTREFCLK1P_127 MGTREFCLK1N_127
pF1_FF2_RECV3 AJ50 / nF1_FF2_RECV3 AJ51	MGTYRXP0_127 MGTYRXN0_127
pF1_FF2_XMIT3 AJ45 / nF1_FF2_XMIT3 AJ46	MGTYTXP0_127 MGTYTXN0_127
pF1_FF2_RECV2 AH48 / nF1_FF2_RECV2 AH49	MGTYRXP1_127 MGTYRXN1_127
pF1_FF2_XMIT2 AH43 / nF1_FF2_XMIT2 AH44	MGTYTXP1_127 MGTYTXN1_127
pF1_FF2_RECV1 AG50 / nF1_FF2_RECV1 AG51	MGTYRXP2_127 MGTYRXN2_127
pF1_FF2_XMIT1 AG45 / nF1_FF2_XMIT1 AG46	MGTYTXP2_127 MGTYTXN2_127
pF1_FF2_RECV0 AF48 / nF1_FF2_RECV0 AF49	MGTYRXP3_127 MGTYRXN3_127
pF1_FF2_XMIT0 AF43 / nF1_FF2_XMIT0 AF44	MGTYTXP3_127 MGTYTXN3_127

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ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1		
Title: 7.03: FPGA#1 FF#2 X12 ON QUADS Q R S		
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7.04: FPGA#1 FF#3 X12 ON QUADS X Y Z

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_Y 20
ac_nF1L_R0_Y 20
ac_pF1L_R1_Y 22
ac_nF1L_R1_Y 22

V_M3V3
R570 3.3K 0603
R571 3.3K 0603
R573 2.2K 0603
R572 2.2K 0603

U32-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

/F1_FF_RESET 39,62,63,64,65,66,67,68
I2C_SDA_F1_FF3_XMIT 39
I2C_SCL_F1_FF3_XMIT 39
/F1_FF3_XMIT_INT 39
/F1_FF3_XMIT_PRESENT 39

6 /RESET G1 G2
7 SDA
8 SCL
4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.8/3.3V >=25G 3.8V <=16G 3.3V
9 RSVD
2 GND

V_3V3
C1061 22 UF 0603 6.3V
C1101 0.1 UF 0402
L25 1.0 UH 0806
C1141 22 UF 0603 6.3V
C1189 0.1 UF 0402

V_F1_FF3_XMIT 32
C1062 22 UF 0603 6.3V
C1102 0.1 UF 0402
L26 1.0 UH 0806
C1142 22 UF 0603 6.3V
C1190 0.1 UF 0402

<Implementation>

U32-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

B19 A19	GND_B19 GND_A19	0P 0N	B18 B17	pF1_FF3_XMIT0 nF1_FF3_XMIT0
		1P 1N	A18 A17	pF1_FF3_XMIT1 nF1_FF3_XMIT1
B16 A16	GND_B16 GND_A16	2P 2N	B15 B14	pF1_FF3_XMIT2 nF1_FF3_XMIT2
		3P 3N	A15 A14	pF1_FF3_XMIT3 nF1_FF3_XMIT3
B13 A13	GND_B13 GND_A13	4P 4N	B12 B11	pF1_FF3_XMIT4 nF1_FF3_XMIT4
		5P 5N	A12 A11	pF1_FF3_XMIT5 nF1_FF3_XMIT5
B10 A10	GND_B10 GND_A10	6P 6N	B9 B8	pF1_FF3_XMIT6 nF1_FF3_XMIT6
		7P 7N	A9 A8	pF1_FF3_XMIT7 nF1_FF3_XMIT7
B7 A7	GND_B7 GND_A7	8P 8N	B6 B5	pF1_FF3_XMIT8 nF1_FF3_XMIT8
		9P 9N	A6 A5	pF1_FF3_XMIT9 nF1_FF3_XMIT9
B4 A4	GND_B4 GND_A4	10P 10N	B3 B2	pF1_FF3_XMIT10 nF1_FF3_XMIT10
		11P 11N	A3 A2	pF1_FF3_XMIT11 nF1_FF3_XMIT11
B1 A1	GND_B1 GND_A1			

GND: 1 G1 2 G2 /A45, /A46, /A44, /A43, /A42, /A41

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U75-35 X GTY QUAD 132

R41 R42		MGTREFCLK0P_132 MGTREFCLK0N_132
P39 P40		MGTREFCLK1P_132 MGTREFCLK1N_132
pF1_FF3_RECV11 nF1_FF3_RECV11	J50 J51	MGTYRXP0_132 MGTYRXN0_132
pF1_FF3_XMIT11 nF1_FF3_XMIT11	J45 J46	MGTYTXP0_132 MGTYTXN0_132
pF1_FF3_RECV10 nF1_FF3_RECV10	H48 H49	MGTYRXP1_132 MGTYRXN1_132
pF1_FF3_XMIT10 nF1_FF3_XMIT10	H43 H44	MGTYTXP1_132 MGTYTXN1_132
pF1_FF3_RECV9 nF1_FF3_RECV9	G50 G51	MGTYRXP2_132 MGTYRXN2_132
pF1_FF3_XMIT9 nF1_FF3_XMIT9	G45 G46	MGTYTXP2_132 MGTYTXN2_132
pF1_FF3_RECV8 nF1_FF3_RECV8	F48 F49	MGTYRXP3_132 MGTYRXN3_132
pF1_FF3_XMIT8 nF1_FF3_XMIT8	F43 F44	MGTYTXP3_132 MGTYTXN3_132

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U75-36 Y GTY QUAD 133

N41 N42		MGTREFCLK0P_133 MGTREFCLK0N_133
M39 M40		MGTREFCLK1P_133 MGTREFCLK1N_133
pF1_FF3_RECV7 nF1_FF3_RECV7	E50 E51	MGTYRXP0_133 MGTYRXN0_133
pF1_FF3_XMIT7 nF1_FF3_XMIT7	D43 D44	MGTYTXP0_133 MGTYTXN0_133
pF1_FF3_RECV6 nF1_FF3_RECV6	D48 D49	MGTYRXP1_133 MGTYRXN1_133
pF1_FF3_XMIT6 nF1_FF3_XMIT6	B43 B44	MGTYTXP1_133 MGTYTXN1_133
pF1_FF3_RECV5 nF1_FF3_RECV5	E46 E47	MGTYRXP2_133 MGTYRXN2_133
pF1_FF3_XMIT5 nF1_FF3_XMIT5	C41 C42	MGTYTXP2_133 MGTYTXN2_133
pF1_FF3_RECV4 nF1_FF3_RECV4	C46 C47	MGTYRXP3_133 MGTYRXN3_133
pF1_FF3_XMIT4 nF1_FF3_XMIT4	E41 E42	MGTYTXP3_133 MGTYTXN3_133

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V_M3V3
R574 3.3K 0603
R575 3.3K 0603
R577 2.2K 0603
R576 2.2K 0603

U33-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

/F1_FF_RESET 39,62,63,64,65,66,67,68
I2C_SDA_F1_FF3_RECV 39
I2C_SCL_F1_FF3_RECV 39
/F1_FF3_RECV_INT 39
/F1_FF3_RECV_PRESENT 39

6 /RESET G1 G2
7 SDA
8 SCL
4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.3V
9 RSVD
2 GND

V_3V3
C1079 22 UF 0603 6.3V
C1103 0.1 UF 0402
L27 1.0 UH 0806
C1143 22 UF 0603 6.3V
C1191 0.1 UF 0402

L28 1.0 UH 0806
C1144 22 UF 0603 6.3V
C1192 0.1 UF 0402

<Implementation>

U33-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17	pF1_FF3_RECV0 nF1_FF3_RECV0
		1P 1N	B18 B17	pF1_FF3_RECV1 nF1_FF3_RECV1
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14	pF1_FF3_RECV2 nF1_FF3_RECV2
		3P 3N	B15 B14	pF1_FF3_RECV3 nF1_FF3_RECV3
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11	pF1_FF3_RECV4 nF1_FF3_RECV4
		5P 5N	B12 B11	pF1_FF3_RECV5 nF1_FF3_RECV5
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8	pF1_FF3_RECV6 nF1_FF3_RECV6
		7P 7N	B9 B8	pF1_FF3_RECV7 nF1_FF3_RECV7
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5	pF1_FF3_RECV8 nF1_FF3_RECV8
		9P 9N	B6 B5	pF1_FF3_RECV9 nF1_FF3_RECV9
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2	pF1_FF3_RECV10 nF1_FF3_RECV10
		11P 11N	B3 B2	pF1_FF3_RECV11 nF1_FF3_RECV11
B1 A1	GND_B1 GND_A1			

GND: 1 G1 2 G2 /A52, /A51, /A50, /A49, /A48, /A47

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U75-37 Z GTY QUAD 134

L41 L42		MGTREFCLK0P_134 MGTREFCLK0N_134
K39 K40		MGTREFCLK1P_134 MGTREFCLK1N_134
pF1_FF3_RECV3 nF1_FF3_RECV3	A46 A47	MGTYRXP0_134 MGTYRXN0_134
pF1_FF3_XMIT3 nF1_FF3_XMIT3	A41 A42	MGTYTXP0_134 MGTYTXN0_134
pF1_FF3_RECV2 nF1_FF3_RECV2	A32 A33	MGTYRXP1_134 MGTYRXN1_134
pF1_FF3_XMIT2 nF1_FF3_XMIT2	B39 B40	MGTYTXP1_134 MGTYTXN1_134
pF1_FF3_RECV1 nF1_FF3_RECV1	B34 B35	MGTYRXP2_134 MGTYRXN2_134
pF1_FF3_XMIT1 nF1_FF3_XMIT1	A37 A38	MGTYTXP2_134 MGTYTXN2_134
pF1_FF3_RECV0 nF1_FF3_RECV0	C32 C33	MGTYRXP3_134 MGTYRXN3_134
pF1_FF3_XMIT0 nF1_FF3_XMIT0	C37 C38	MGTYTXP3_134 MGTYTXN3_134

FPGA_VU13P_A2577

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1

Title: 7.04: FPGA#1 FF#3 X12 ON QUADS X Y Z

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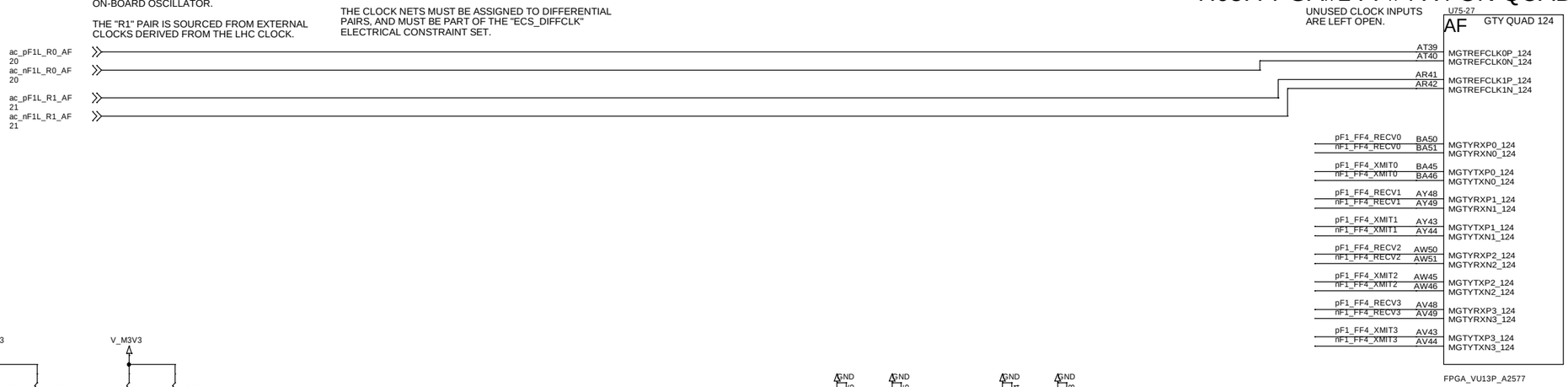
7.05: FPGA#1 FF#4 X4 ON QUAD AF

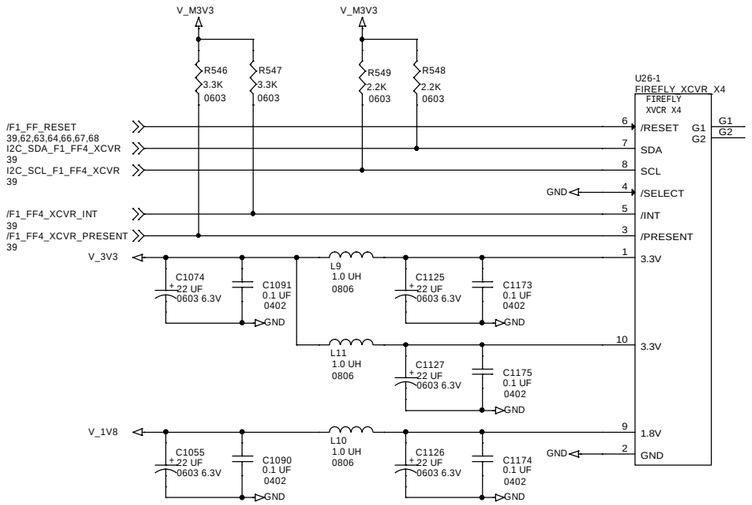
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

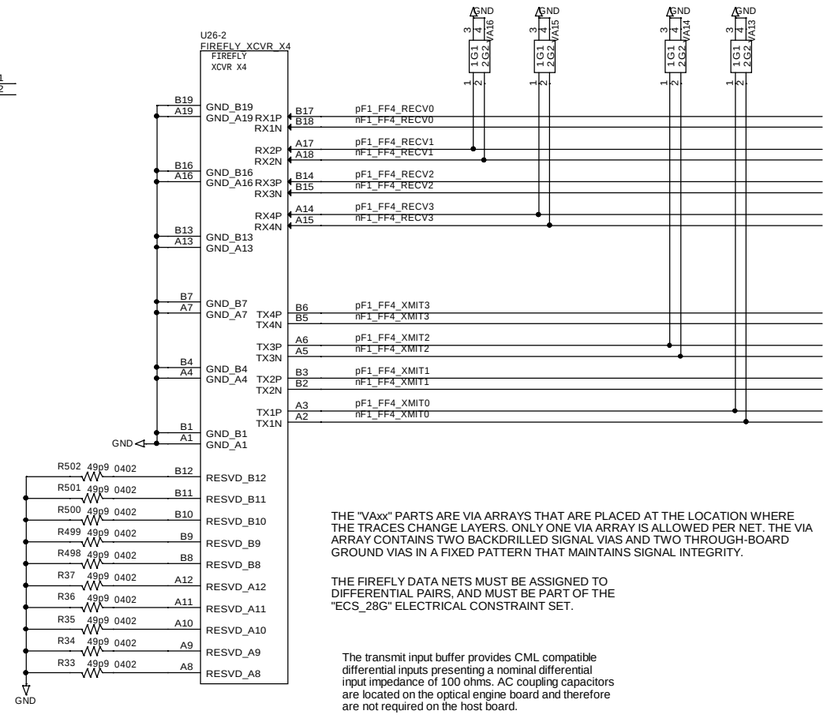
THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.







THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1

Title: 7.05: FPGA#1 FF#4 X4 ON QUAD AF

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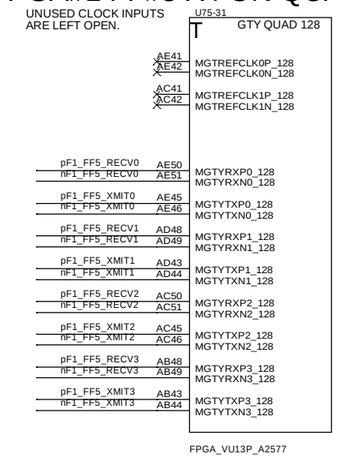
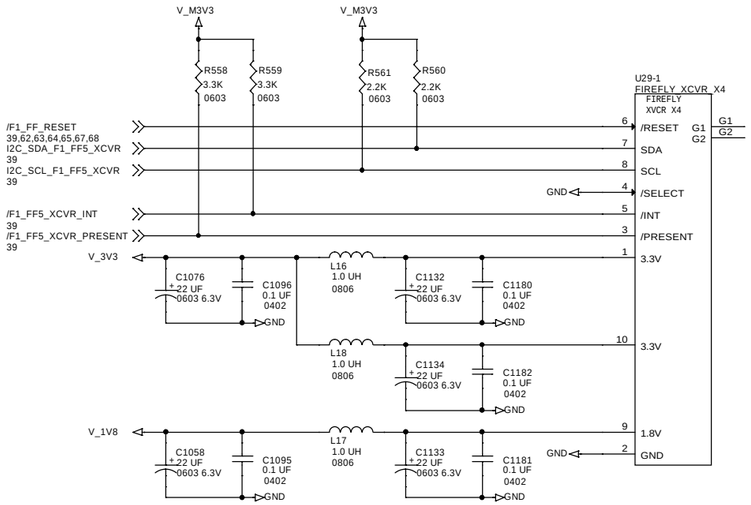
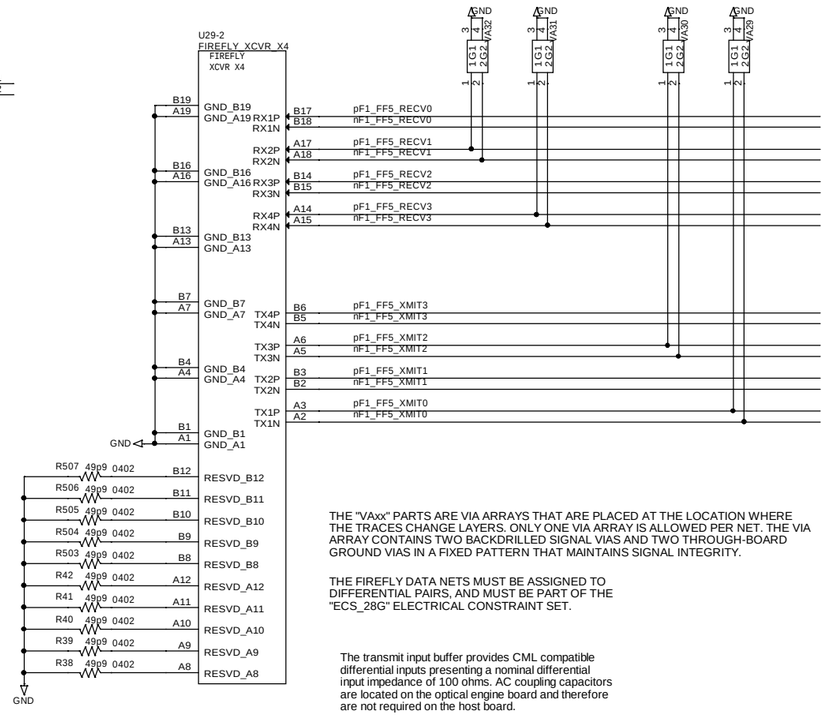
7.06: FPGA#1 FF#5 X4 ON QUAD T

UNUSED CLOCK INPUTS
ARE LEFT OPEN.



FPGA_VU13P_A2577





THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1			
Title: 7.06: FPGA#1 FF#5 X4 ON QUAD T			
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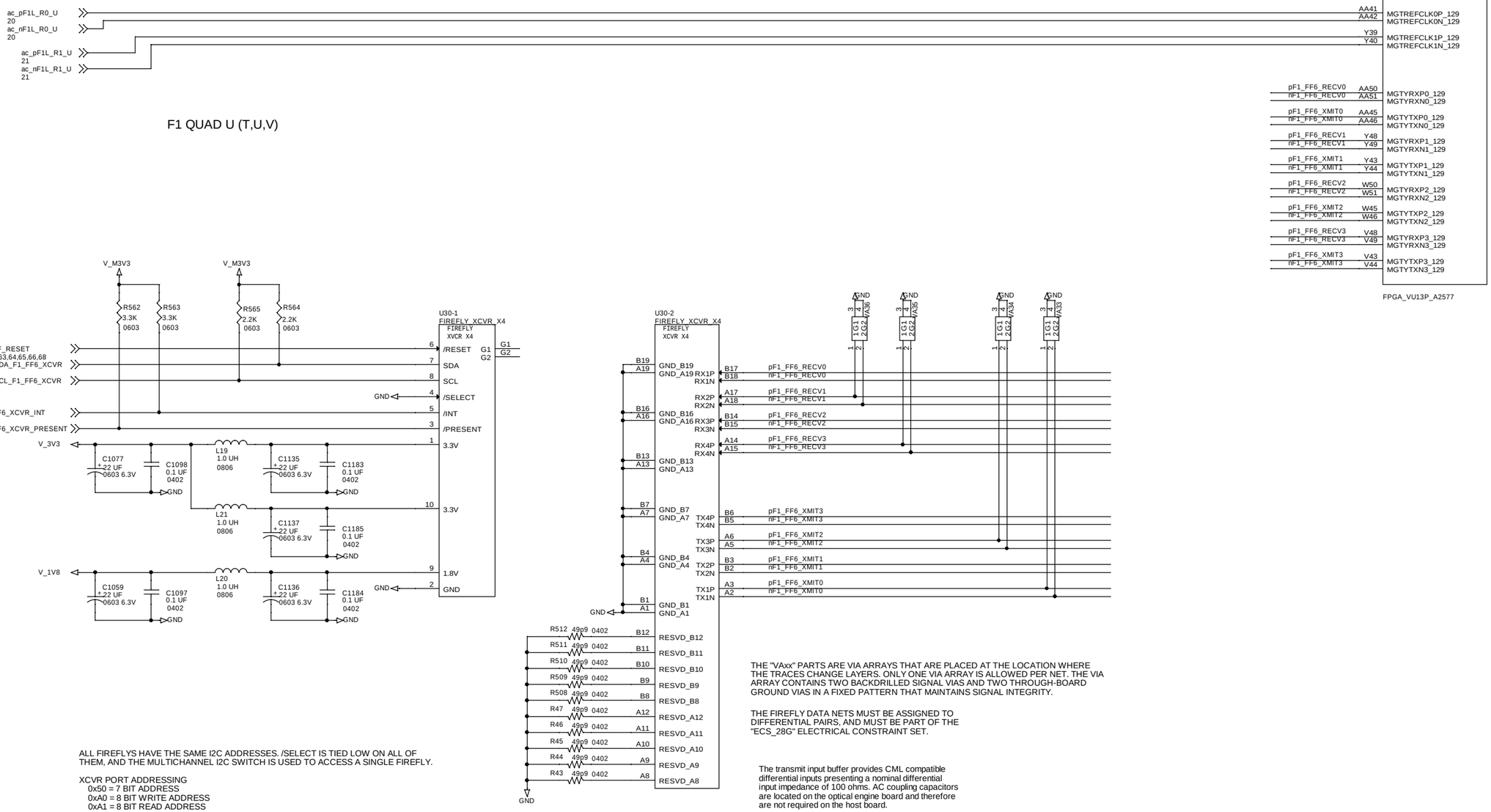
7.07: FPGA#1 FF#6 X4 ON QUAD U

F1 QUAD U (T,U,V)



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1		
Title: 7.07: FPGA#1 FF#6 X4 ON QUAD U		
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7.08: FPGA#1 FF#7 X4 ON QUAD V

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

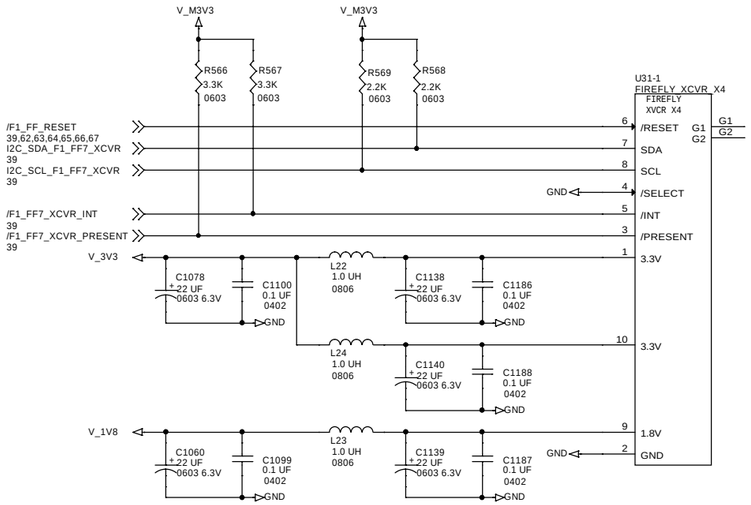
ac_pF1L_R0_V 20
ac_nF1L_R0_V 20

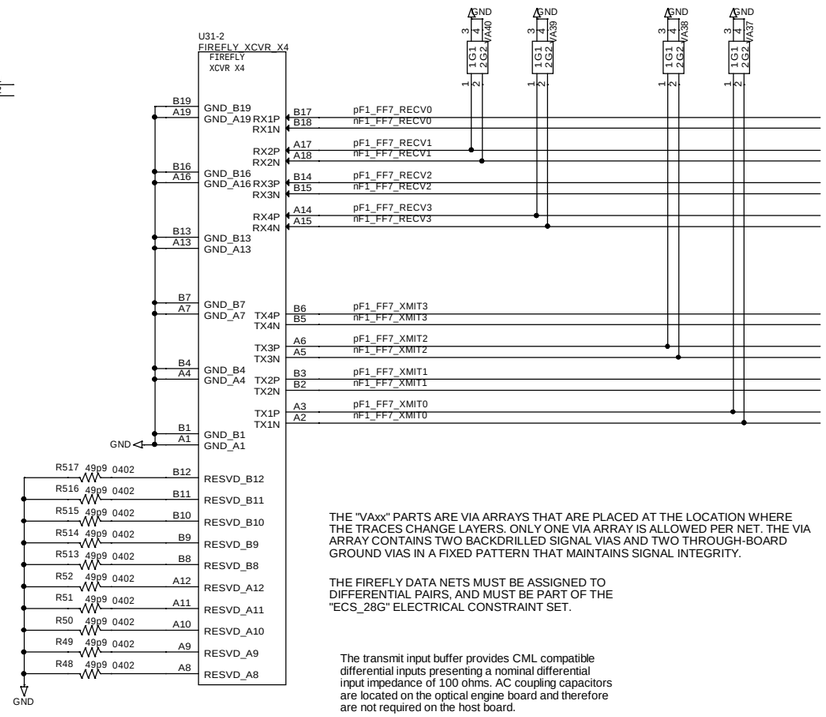
U75-33 V — GTY QUAD 130

W41 MGTREFCLK0P_130
W42 MGTREFCLK0N_130
V39 MGTREFCLK1P_130
V40 MGTREFCLK1N_130

pF1_FF7_RECV0	U50	MGTYRXP0_130
nF1_FF7_RECV0	U51	MGTYRXN0_130
pF1_FF7_XMIT0	U45	MGTYTXP0_130
nF1_FF7_XMIT0	U46	MGTYTXN0_130
pF1_FF7_RECV1	T48	MGTYRXP1_130
nF1_FF7_RECV1	T49	MGTYRXN1_130
pF1_FF7_XMIT1	T43	MGTYTXP1_130
nF1_FF7_XMIT1	T44	MGTYTXN1_130
pF1_FF7_RECV2	R50	MGTYRXP2_130
nF1_FF7_RECV2	R51	MGTYRXN2_130
pF1_FF7_XMIT2	R45	MGTYTXP2_130
nF1_FF7_XMIT2	R46	MGTYTXN2_130
pF1_FF7_RECV3	P48	MGTYRXP3_130
nF1_FF7_RECV3	P49	MGTYRXN3_130
pF1_FF7_XMIT3	P43	MGTYTXP3_130
nF1_FF7_XMIT3	P44	MGTYTXN3_130

FPGA_VU13P_A2577





ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

APOLLO CM W/ DUAL A2577, MK1			
Title: 7.08: FPGA#1 FF#7 X4 ON QUAD V			
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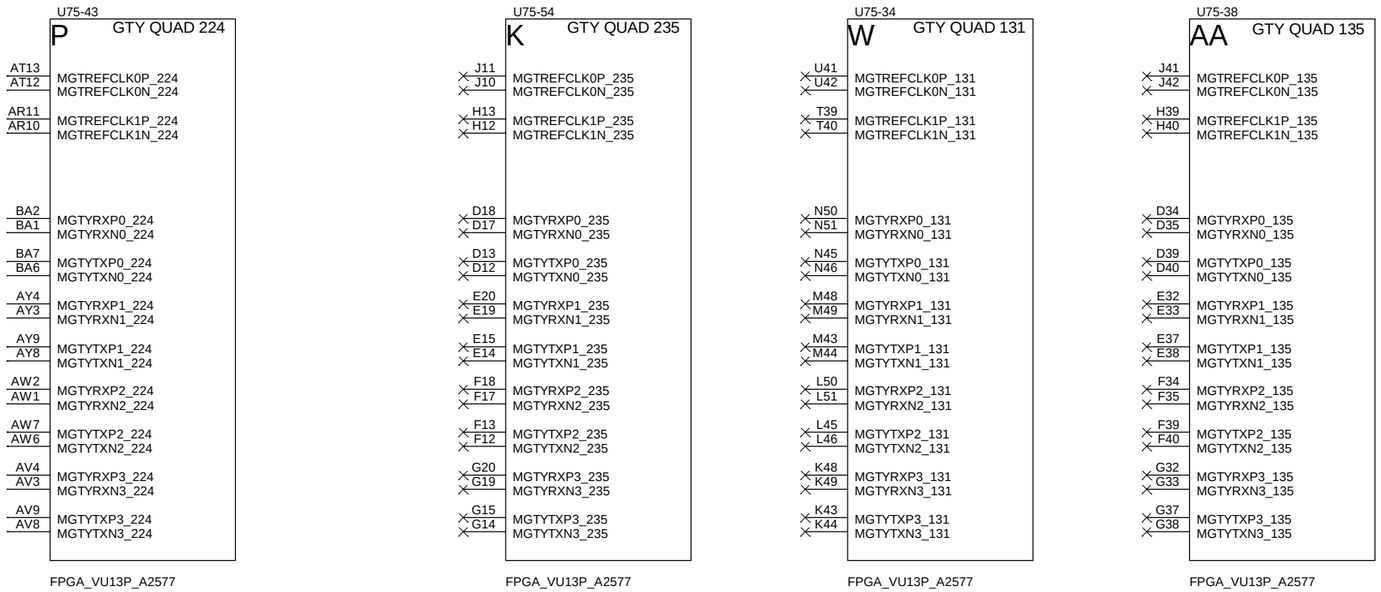
7.09: FPGA#1 UNUSED QUADS K, P, W, AA



APOLLO CM W/ DUAL A2577, MK1		
Title: 7.09: FPGA#1 UNUSED QUADS K, P, W, AA		
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8.01: FPGA#2 SM C2C ON QUAD L

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

APOLLO CM W/ DUAL A2577, MK1		
Title: 8.01: FPGA#2 SM C2C ON QUAD L		
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8.02: FPGA#2 FF#1 X12 ON QUADS AC AD AE

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF2L_R0_AD 20
ac_nF2L_R0_AD 20
ac_pF2L_R1_AD 22
ac_nF2L_R1_AD 22

V_M3V3
R578 3.3K 0603
R579 3.3K 0603
R581 2.2K 0603
R580 2.2K 0603

U34-1 FIREFLY_XMIT_X12 — FIREFLY XMIT X12

/F2_FF_RESET 40,71,72,73,74,75,76,77
I2C_SDA_F2_FF1_XMIT 40
I2C_SCL_F2_FF1_XMIT 40
/F2_FF1_XMIT_INT 40
/F2_FF1_XMIT_PRESENT 40
V_3V3

C1063 22 UF 0603 6.3V
C1104 0.1 UF 0402
L29 1.0 UH 0806
C1145 22 UF 0603 6.3V
C1193 0.1 UF 0402

V_F2_FF1_XMIT 32
C1064 22 UF 0603 6.3V
C1105 0.1 UF 0402
L30 1.0 UH 0806
C1146 22 UF 0603 6.3V
C1194 0.1 UF 0402

/RESET G1 G2
SDA
SCL
/SELECT
/INT
/PRESENT
3.3V
3.8/3.3V >=25G 3.8V <=16G 3.3V
RSVD
GND
<Implementation>

U34-2 FIREFLY_XMIT_X12 — FIREFLY XMIT X12

B19 A19	GND_B19 GND_A19	0P 0N	B18 A17	pF2_FF1_XMIT0 nF2_FF1_XMIT0
		1P 1N	A18 A17	pF2_FF1_XMIT1 nF2_FF1_XMIT1
B16 A16	GND_B16 GND_A16	2P 2N	B15 B14	pF2_FF1_XMIT2 nF2_FF1_XMIT2
		3P 3N	A15 A14	pF2_FF1_XMIT3 nF2_FF1_XMIT3
B13 A13	GND_B13 GND_A13	4P 4N	B12 B11	pF2_FF1_XMIT4 nF2_FF1_XMIT4
		5P 5N	A12 A11	pF2_FF1_XMIT5 nF2_FF1_XMIT5
B10 A10	GND_B10 GND_A10	6P 6N	B9 B8	pF2_FF1_XMIT6 nF2_FF1_XMIT6
		7P 7N	A9 A8	pF2_FF1_XMIT7 nF2_FF1_XMIT7
B7 A7	GND_B7 GND_A7	8P 8N	B6 B5	pF2_FF1_XMIT8 nF2_FF1_XMIT8
		9P 9N	A6 A5	pF2_FF1_XMIT9 nF2_FF1_XMIT9
B4 A4	GND_B4 GND_A4	10P 10N	B3 B2	pF2_FF1_XMIT10 nF2_FF1_XMIT10
		11P 11N	A3 A2	pF2_FF1_XMIT11 nF2_FF1_XMIT11
B1 A1	GND_B1 GND_A1			

GND — 3 4 1 G1 2 G2 VIA57 / VIA56 / VIA55 / VIA54

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U77-24 AC — GTY QUAD 121

	BB39 BB40	MGTREFCLK0P_121 MGTREFCLK0N_121
	BA41 BA42	MGTREFCLK1P_121 MGTREFCLK1N_121
pF2_FF1_RECV11 nF2_FF1_RECV11	BK34 BK35	MGTYRXP0_121 MGTYRXN0_121
pF2_FF1_XMIT11 nF2_FF1_XMIT11	BL37 BL38	MGTYTXP0_121 MGTYTXN0_121
pF2_FF1_RECV10 nF2_FF1_RECV10	BL32 BL33	MGTYRXP1_121 MGTYRXN1_121
pF2_FF1_XMIT10 nF2_FF1_XMIT10	BK39 BK40	MGTYTXP1_121 MGTYTXN1_121
pF2_FF1_RECV9 nF2_FF1_RECV9	BL46 BL47	MGTYRXP2_121 MGTYRXN2_121
pF2_FF1_XMIT9 nF2_FF1_XMIT9	BL41 BL42	MGTYTXP2_121 MGTYTXN2_121
pF2_FF1_RECV8 nF2_FF1_RECV8	BJ46 BJ47	MGTYRXP3_121 MGTYRXN3_121
pF2_FF1_XMIT8 nF2_FF1_XMIT8	BK43 BK44	MGTYTXP3_121 MGTYTXN3_121

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U77-25 AD — GTY QUAD 122

	AY39 AY40	MGTREFCLK0P_122 MGTREFCLK0N_122
	AW41 AW42	MGTREFCLK1P_122 MGTREFCLK1N_122
pF2_FF1_RECV7 nF2_FF1_RECV7	BH48 BH49	MGTYRXP0_122 MGTYRXN0_122
pF2_FF1_XMIT7 nF2_FF1_XMIT7	BG41 BG42	MGTYTXP0_122 MGTYTXN0_122
pF2_FF1_RECV6 nF2_FF1_RECV6	BG50 BG51	MGTYRXP1_122 MGTYRXN1_122
pF2_FF1_XMIT6 nF2_FF1_XMIT6	BJ41 BJ42	MGTYTXP1_122 MGTYTXN1_122
pF2_FF1_RECV5 nF2_FF1_RECV5	BG46 BG47	MGTYRXP2_122 MGTYRXN2_122
pF2_FF1_XMIT5 nF2_FF1_XMIT5	BH43 BH44	MGTYTXP2_122 MGTYTXN2_122
pF2_FF1_RECV4 nF2_FF1_RECV4	BF48 BF49	MGTYRXP3_122 MGTYRXN3_122
pF2_FF1_XMIT4 nF2_FF1_XMIT4	BF43 BF44	MGTYTXP3_122 MGTYTXN3_122

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V_M3V3
R582 3.3K 0603
R583 3.3K 0603
R585 2.2K 0603
R584 2.2K 0603

U35-1 FIREFLY_RECV_X12 — FIREFLY RECV X12

/F2_FF_RESET 40,71,72,73,74,75,76,77
I2C_SDA_F2_FF1_RECV 40
I2C_SCL_F2_FF1_RECV 40
/F2_FF1_RECV_INT 40
/F2_FF1_RECV_PRESENT 40
V_3V3

C1080 22 UF 0603 6.3V
C1106 0.1 UF 0402
L31 1.0 UH 0806
C1147 22 UF 0603 6.3V
C1195 0.1 UF 0402

L32 1.0 UH 0806
C1148 22 UF 0603 6.3V
C1196 0.1 UF 0402

/RESET G1 G2
SDA
SCL
/SELECT
/INT
/PRESENT
3.3V
3.3V
RSVD
GND
<Implementation>

U35-2 FIREFLY_RECV_X12 — FIREFLY RECV X12

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17	pF2_FF1_RECV0 nF2_FF1_RECV0
		1P 1N	B18 B17	pF2_FF1_RECV1 nF2_FF1_RECV1
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14	pF2_FF1_RECV2 nF2_FF1_RECV2
		3P 3N	B15 B14	pF2_FF1_RECV3 nF2_FF1_RECV3
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11	pF2_FF1_RECV4 nF2_FF1_RECV4
		5P 5N	B12 B11	pF2_FF1_RECV5 nF2_FF1_RECV5
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8	pF2_FF1_RECV6 nF2_FF1_RECV6
		7P 7N	B9 B8	pF2_FF1_RECV7 nF2_FF1_RECV7
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5	pF2_FF1_RECV8 nF2_FF1_RECV8
		9P 9N	B6 B5	pF2_FF1_RECV9 nF2_FF1_RECV9
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2	pF2_FF1_RECV10 nF2_FF1_RECV10
		11P 11N	B3 B2	pF2_FF1_RECV11 nF2_FF1_RECV11
B1 A1	GND_B1 GND_A1			

GND — 3 4 1 G1 2 G2 VIA63 / VIA62 / VIA61 / VIA60 / VIA59

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U77-26 AE — GTY QUAD 123

	AV39 AV40	MGTREFCLK0P_123 MGTREFCLK0N_123
	AU41 AU42	MGTREFCLK1P_123 MGTREFCLK1N_123
pF2_FF1_RECV3 nF2_FF1_RECV3	BE50 BE51	MGTYRXP0_123 MGTYRXN0_123
pF2_FF1_XMIT3 nF2_FF1_XMIT3	BE45 BE46	MGTYTXP0_123 MGTYTXN0_123
pF2_FF1_RECV2 nF2_FF1_RECV2	BD48 BD49	MGTYRXP1_123 MGTYRXN1_123
pF2_FF1_XMIT2 nF2_FF1_XMIT2	BD43 BD44	MGTYTXP1_123 MGTYTXN1_123
pF2_FF1_RECV1 nF2_FF1_RECV1	BC50 BC51	MGTYRXP2_123 MGTYRXN2_123
pF2_FF1_XMIT1 nF2_FF1_XMIT1	BC45 BC46	MGTYTXP2_123 MGTYTXN2_123
pF2_FF1_RECV0 nF2_FF1_RECV0	BB48 BB49	MGTYRXP3_123 MGTYRXN3_123
pF2_FF1_XMIT0 nF2_FF1_XMIT0	BB43 BB44	MGTYTXP3_123 MGTYTXN3_123

FPGA_VU13P_A2577

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1

Title: 8.02: FPGA#2 FF#1 X12 ON QUADS AC AD AE

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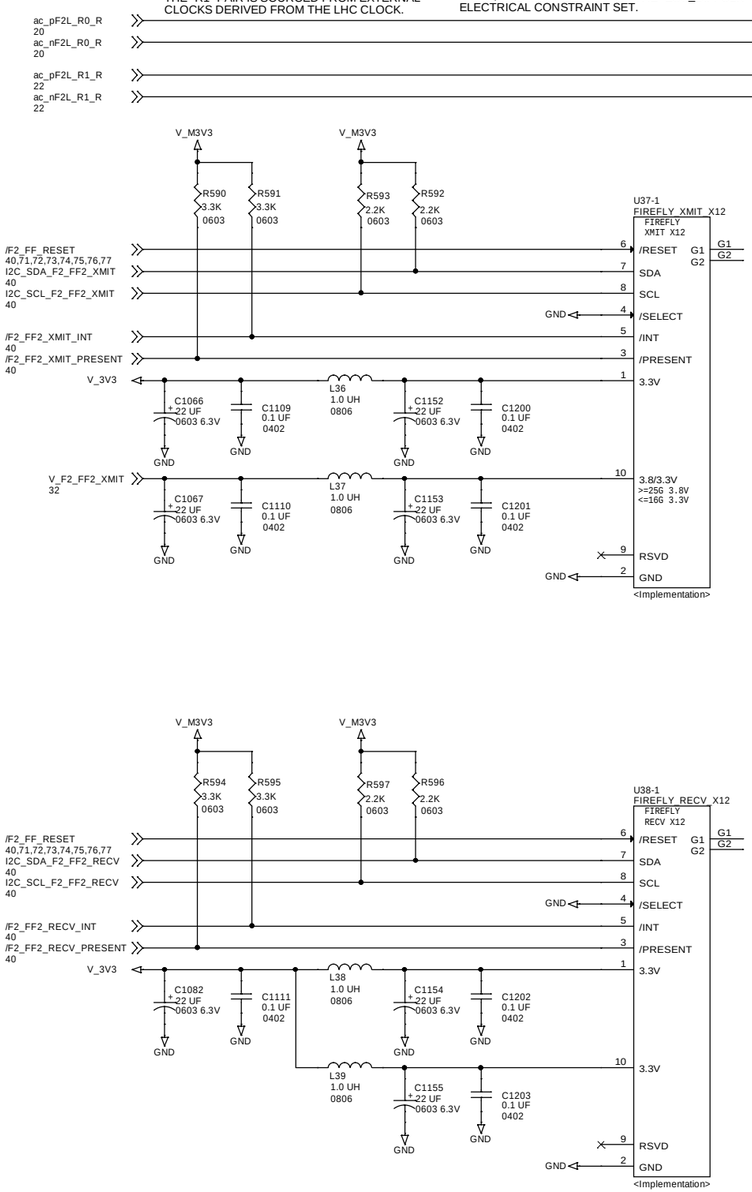
8.03: FPGA#2 FF#2 X12 ON QUADS Q R S

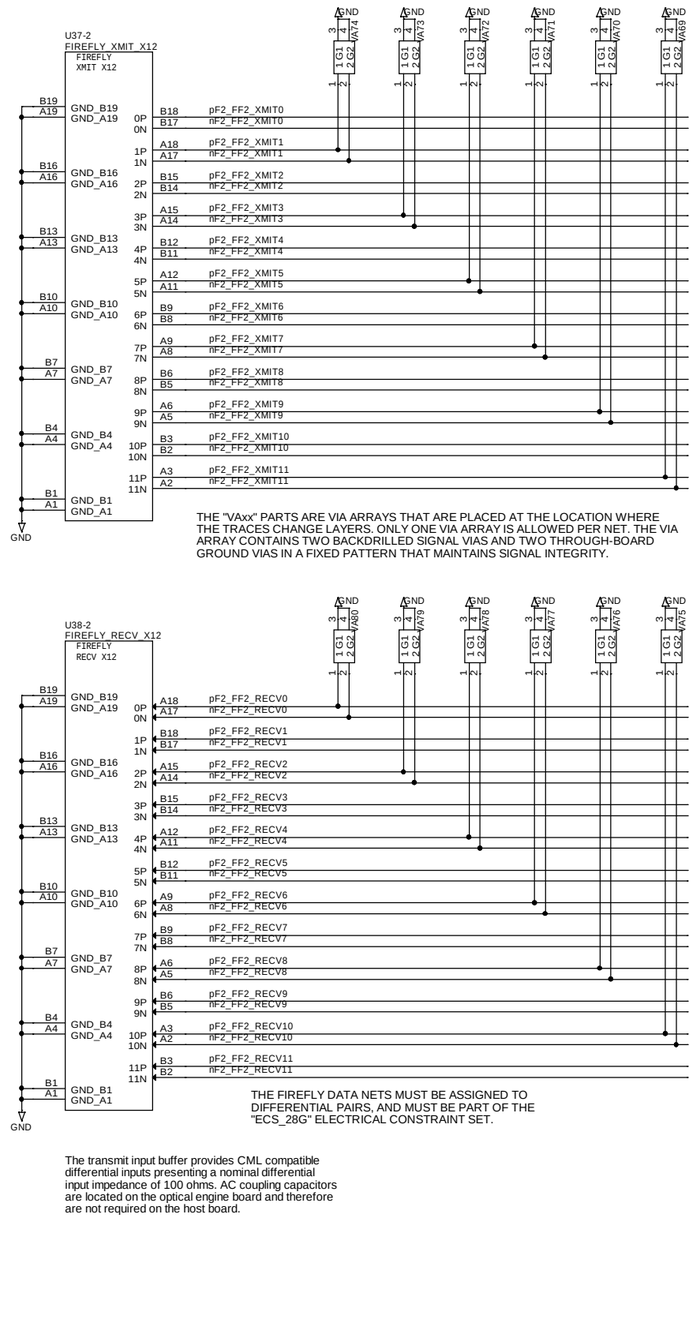
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

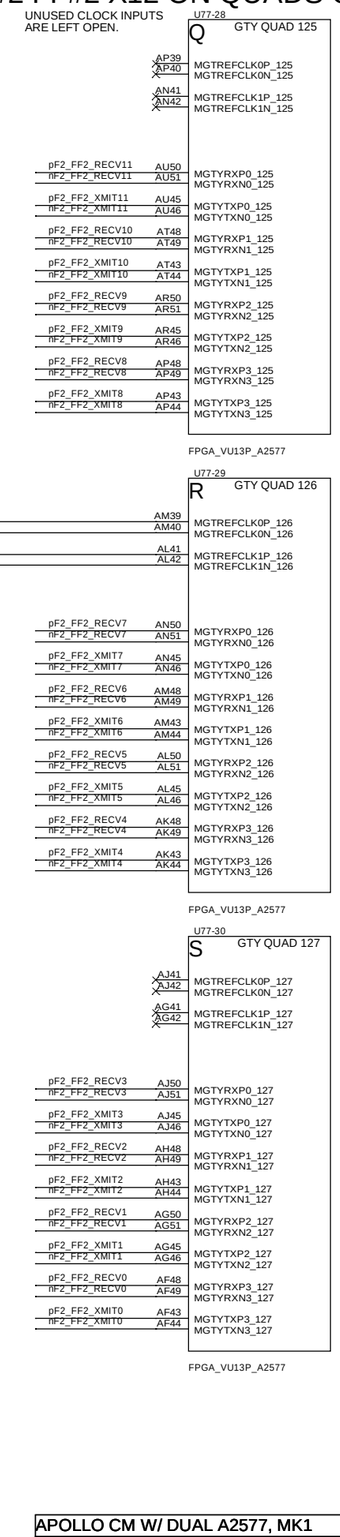
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.





THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.



THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1			
Title: 8.03: FPGA#2 FF#2 X12 ON QUADS Q R S			
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8.04: FPGA#2 FF#3 X12 ON QUADS X Y Z

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF2L_R0_Y 20
ac_nF2L_R0_Y 20
ac_pF2L_R1_Y 22
ac_nF2L_R1_Y 22

V_M3V3
R610 3.3K 0603
R611 3.3K 0603
R613 2.2K 0603
R612 2.2K 0603

U42-1 FIREFLY_XMIT_X12 FIREFLY XMIT X12

/F2_FF_RESET 40,71,72,73,74,75,76,77
I2C_SDA_F2_FF3_XMIT 40
I2C_SCL_F2_FF3_XMIT 40
/F2_FF3_XMIT_INT 40
/F2_FF3_XMIT_PRESENT 40

6 /RESET G1 G2
7 SDA
8 SCL
GND 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.8/3.3V >=25G 3.8V <=16G 3.3V
9 RSVD
GND 2 GND
<Implementation>

V_3V3
C1071 22 UF 0603 6.3V
C1118 0.1 UF 0402
L49 1.0 UH 0806
C1165 22 UF 0603 6.3V
C1213 0.1 UF 0402

V_F2_FF3_XMIT 32
C1072 22 UF 0603 6.3V
C1119 0.1 UF 0402
L50 1.0 UH 0806
C1166 22 UF 0603 6.3V
C1214 0.1 UF 0402

U42-2 FIREFLY_XMIT_X12 FIREFLY XMIT X12

B19 A19	GND_B19 GND_A19	0P 0N	B18 B17 — pF2_FF3_XMIT0 nF2_FF3_XMIT0
		1P 1N	A18 A17 — pF2_FF3_XMIT1 nF2_FF3_XMIT1
B16 A16	GND_B16 GND_A16	2P 2N	B15 B14 — pF2_FF3_XMIT2 nF2_FF3_XMIT2
		3P 3N	A15 A14 — pF2_FF3_XMIT3 nF2_FF3_XMIT3
B13 A13	GND_B13 GND_A13	4P 4N	B12 B11 — pF2_FF3_XMIT4 nF2_FF3_XMIT4
		5P 5N	A12 A11 — pF2_FF3_XMIT5 nF2_FF3_XMIT5
B10 A10	GND_B10 GND_A10	6P 6N	B9 B8 — pF2_FF3_XMIT6 nF2_FF3_XMIT6
		7P 7N	A9 A8 — pF2_FF3_XMIT7 nF2_FF3_XMIT7
B7 A7	GND_B7 GND_A7	8P 8N	B6 B5 — pF2_FF3_XMIT8 nF2_FF3_XMIT8
		9P 9N	A6 A5 — pF2_FF3_XMIT9 nF2_FF3_XMIT9
B4 A4	GND_B4 GND_A4	10P 10N	B3 B2 — pF2_FF3_XMIT10 nF2_FF3_XMIT10
		11P 11N	A3 A2 — pF2_FF3_XMIT11 nF2_FF3_XMIT11
B1 A1	GND_B1 GND_A1		

GND 1 G1 2 G2 A94 A97 A96 A95 A94 A93

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U77-35 X GTY QUAD 132

R41 R42		MGTREFCLK0P_132 MGTREFCLK0N_132
P39 P40		MGTREFCLK1P_132 MGTREFCLK1N_132
pF2_FF3_RECV11 nF2_FF3_RECV11	J50 J51	MGTYRXP0_132 MGTYRXN0_132
pF2_FF3_XMIT11 nF2_FF3_XMIT11	J45 J46	MGTYTXP0_132 MGTYTXN0_132
pF2_FF3_RECV10 nF2_FF3_RECV10	H48 H49	MGTYRXP1_132 MGTYRXN1_132
pF2_FF3_XMIT10 nF2_FF3_XMIT10	H43 H44	MGTYTXP1_132 MGTYTXN1_132
pF2_FF3_RECV9 nF2_FF3_RECV9	G50 G51	MGTYRXP2_132 MGTYRXN2_132
pF2_FF3_XMIT9 nF2_FF3_XMIT9	G45 G46	MGTYTXP2_132 MGTYTXN2_132
pF2_FF3_RECV8 nF2_FF3_RECV8	F48 F49	MGTYRXP3_132 MGTYRXN3_132
pF2_FF3_XMIT8 nF2_FF3_XMIT8	F43 F44	MGTYTXP3_132 MGTYTXN3_132

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U77-36 Y GTY QUAD 133

N41 N42		MGTREFCLK0P_133 MGTREFCLK0N_133
M39 M40		MGTREFCLK1P_133 MGTREFCLK1N_133
pF2_FF3_RECV7 nF2_FF3_RECV7	E50 E51	MGTYRXP0_133 MGTYRXN0_133
pF2_FF3_XMIT7 nF2_FF3_XMIT7	D43 D44	MGTYTXP0_133 MGTYTXN0_133
pF2_FF3_RECV6 nF2_FF3_RECV6	D48 D49	MGTYRXP1_133 MGTYRXN1_133
pF2_FF3_XMIT6 nF2_FF3_XMIT6	B43 B44	MGTYTXP1_133 MGTYTXN1_133
pF2_FF3_RECV5 nF2_FF3_RECV5	E46 E47	MGTYRXP2_133 MGTYRXN2_133
pF2_FF3_XMIT5 nF2_FF3_XMIT5	C41 C42	MGTYTXP2_133 MGTYTXN2_133
pF2_FF3_RECV4 nF2_FF3_RECV4	C46 C47	MGTYRXP3_133 MGTYRXN3_133
pF2_FF3_XMIT4 nF2_FF3_XMIT4	E41 E42	MGTYTXP3_133 MGTYTXN3_133

FPGA_VU13P_A2577

V_M3V3
R614 3.3K 0603
R615 3.3K 0603
R617 2.2K 0603
R616 2.2K 0603

U43-1 FIREFLY_RECV_X12 FIREFLY RECV X12

/F2_FF_RESET 40,71,72,73,74,75,76,77
I2C_SDA_F2_FF3_RECV 40
I2C_SCL_F2_FF3_RECV 40
/F2_FF3_RECV_INT 40
/F2_FF3_RECV_PRESENT 40

6 /RESET G1 G2
7 SDA
8 SCL
GND 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.3V
9 RSVD
GND 2 GND
<Implementation>

V_3V3
C1086 22 UF 0603 6.3V
C1120 0.1 UF 0402
L51 1.0 UH 0806
C1167 22 UF 0603 6.3V
C1215 0.1 UF 0402

L52 1.0 UH 0806
C1168 22 UF 0603 6.3V
C1216 0.1 UF 0402

U43-2 FIREFLY_RECV_X12 FIREFLY RECV X12

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17 — pF2_FF3_RECV0 nF2_FF3_RECV0
		1P 1N	B18 B17 — pF2_FF3_RECV1 nF2_FF3_RECV1
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14 — pF2_FF3_RECV2 nF2_FF3_RECV2
		3P 3N	B15 B14 — pF2_FF3_RECV3 nF2_FF3_RECV3
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11 — pF2_FF3_RECV4 nF2_FF3_RECV4
		5P 5N	B12 B11 — pF2_FF3_RECV5 nF2_FF3_RECV5
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8 — pF2_FF3_RECV6 nF2_FF3_RECV6
		7P 7N	B9 B8 — pF2_FF3_RECV7 nF2_FF3_RECV7
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5 — pF2_FF3_RECV8 nF2_FF3_RECV8
		9P 9N	B6 B5 — pF2_FF3_RECV9 nF2_FF3_RECV9
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2 — pF2_FF3_RECV10 nF2_FF3_RECV10
		11P 11N	B3 B2 — pF2_FF3_RECV11 nF2_FF3_RECV11
B1 A1	GND_B1 GND_A1		

GND 1 G1 2 G2 A104 A103 A102 A101 A100 A99

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U77-37 Z GTY QUAD 134

L41 L42		MGTREFCLK0P_134 MGTREFCLK0N_134
K39 K40		MGTREFCLK1P_134 MGTREFCLK1N_134
pF2_FF3_RECV3 nF2_FF3_RECV3	A46 A47	MGTYRXP0_134 MGTYRXN0_134
pF2_FF3_XMIT3 nF2_FF3_XMIT3	A41 A42	MGTYTXP0_134 MGTYTXN0_134
pF2_FF3_RECV2 nF2_FF3_RECV2	A32 A33	MGTYRXP1_134 MGTYRXN1_134
pF2_FF3_XMIT2 nF2_FF3_XMIT2	B39 B40	MGTYTXP1_134 MGTYTXN1_134
pF2_FF3_RECV1 nF2_FF3_RECV1	B34 B35	MGTYRXP2_134 MGTYRXN2_134
pF2_FF3_XMIT1 nF2_FF3_XMIT1	A37 A38	MGTYTXP2_134 MGTYTXN2_134
pF2_FF3_RECV0 nF2_FF3_RECV0	C32 C33	MGTYRXP3_134 MGTYRXN3_134
pF2_FF3_XMIT0 nF2_FF3_XMIT0	C37 C38	MGTYTXP3_134 MGTYTXN3_134

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ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM W/ DUAL A2577, MK1

Title: 8.04: FPGA#2 FF#3 X12 ON QUADS X Y Z

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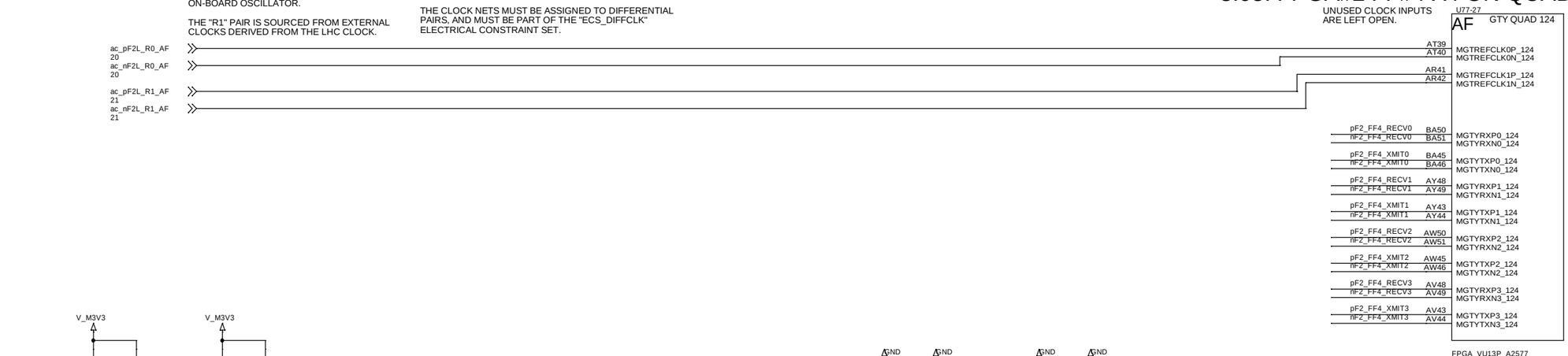
8.05: FPGA#2 FF#4 X4 ON QUAD AF

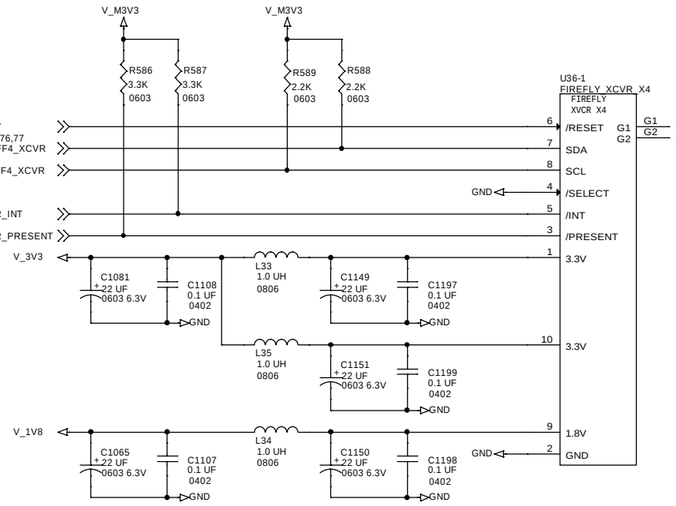
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

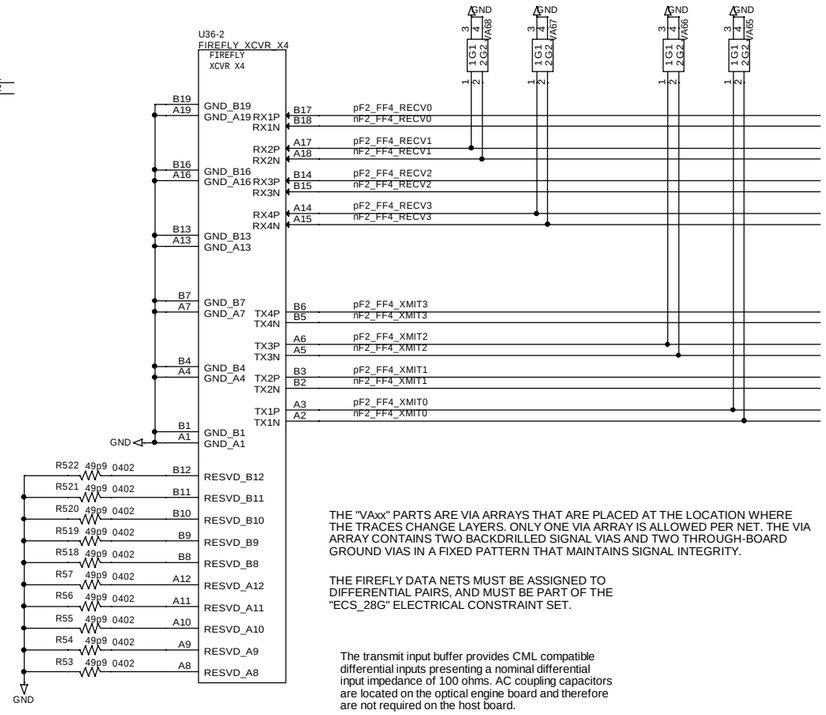
THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.







THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1

Title: 8.05: FPGA#2 FF#4 X4 ON QUAD AF

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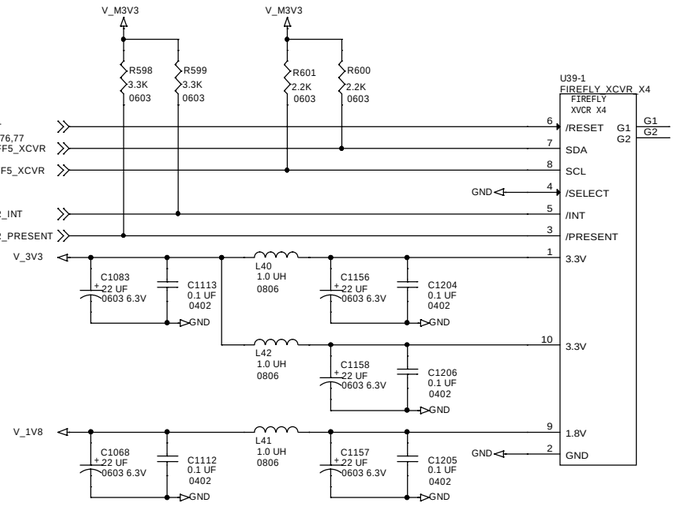
8.06: FPGA#2 FF#5 X4 ON QUAD T

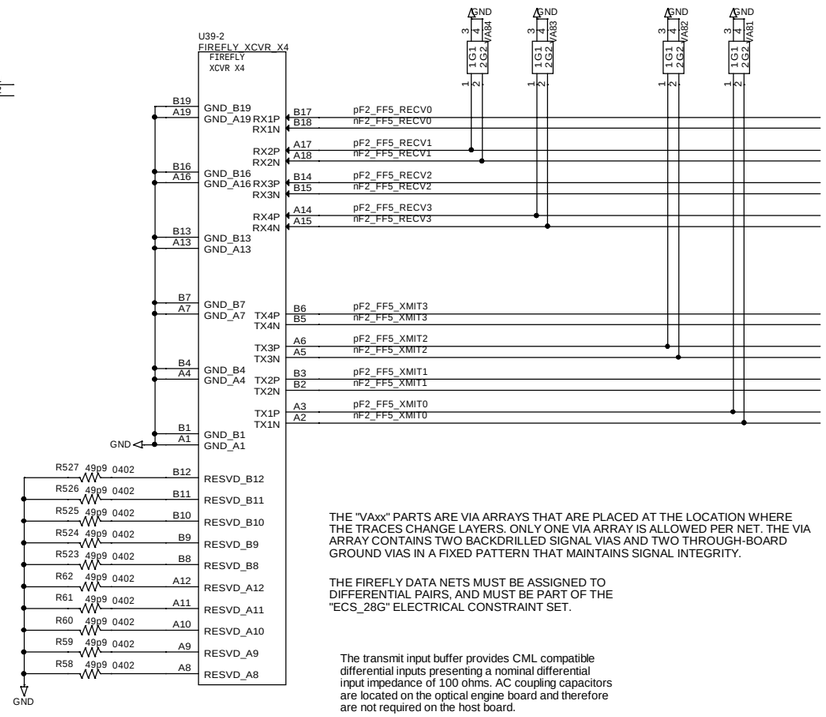
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

U77-31
GTY QUAD 128

	AE41	
	AE42	MGTREFCLK0P_128
		MGTREFCLK0N_128
	AC41	
	AC42	MGTREFCLK1P_128
		MGTREFCLK1N_128
pF2_FF5_RECV0	AE50	MGTYRXP0_128
nF2_FF5_RECV0	AE51	MGTYRXN0_128
pF2_FF5_XMIT0	AE45	MGTYTXP0_128
nF2_FF5_XMIT0	AE46	MGTYTXN0_128
pF2_FF5_RECV1	AD48	MGTYRXP1_128
nF2_FF5_RECV1	AD49	MGTYRXN1_128
pF2_FF5_XMIT1	AD43	MGTYTXP1_128
nF2_FF5_XMIT1	AD44	MGTYTXN1_128
pF2_FF5_RECV2	AC50	MGTYRXP2_128
nF2_FF5_RECV2	AC51	MGTYRXN2_128
pF2_FF5_XMIT2	AC45	MGTYTXP2_128
nF2_FF5_XMIT2	AC46	MGTYTXN2_128
pF2_FF5_RECV3	AB48	MGTYRXP3_128
nF2_FF5_RECV3	AB49	MGTYRXN3_128
pF2_FF5_XMIT3	AB43	MGTYTXP3_128
nF2_FF5_XMIT3	AB44	MGTYTXN3_128

FPGA_VU13P_A2577





ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1

Title: 8.06: FPGA#2 FF#5 X4 ON QUAD T

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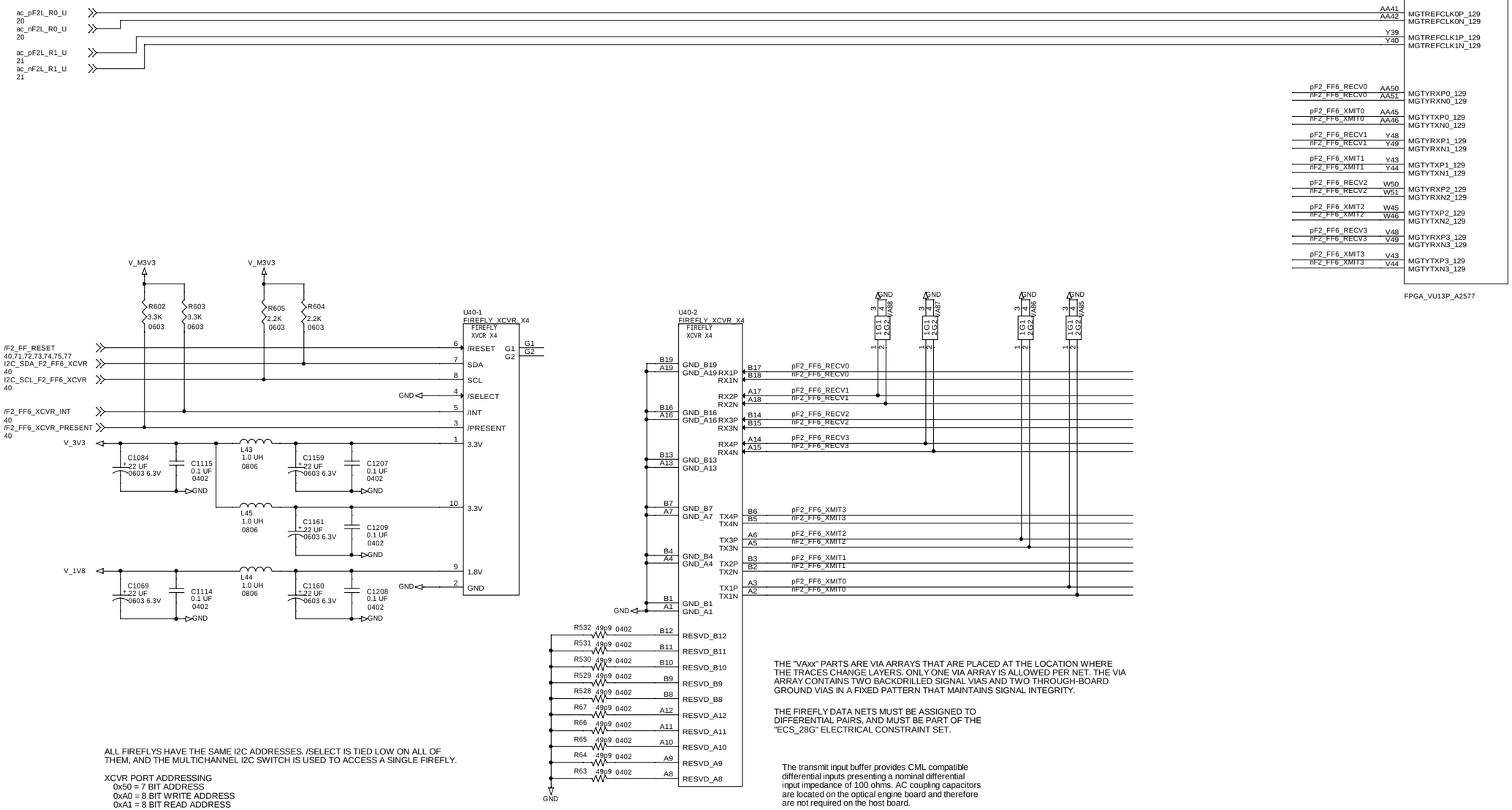
8.07: FPGA#2 FF#6 X4 ON QUAD U

UNUSED CLOCK INPUTS
ARE LEFT OPEN.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1		
Title: 8.07: FPGA#2 FF#6 X4 ON QUAD U		
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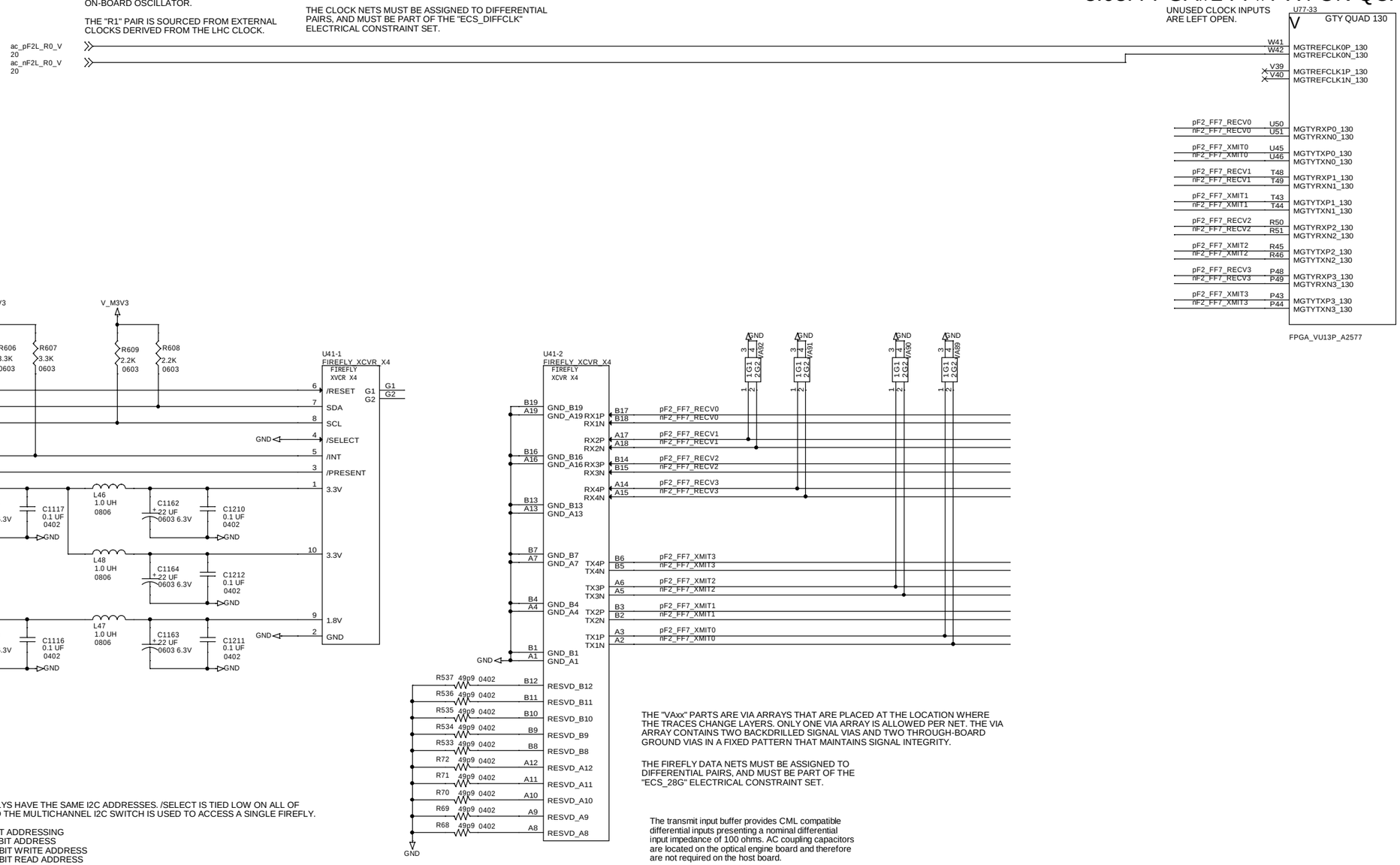
8.08: FPGA#2 FF#7 X4 ON QUAD V

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM W/ DUAL A2577, MK1		
Title: 8.08: FPGA#2 FF#7 X4 ON QUAD V		
Size	Document Number: 6089-119	Rev: A
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8.09: FPGA#2 UNUSED QUADS G, K, W, AA

U77-50

G GTY QUAD 231

U11	MGTREFCLK0P_231
U10	MGTREFCLK0N_231
T13	MGTREFCLK1P_231
T12	MGTREFCLK1N_231
N2	MGTYRXP0_231
N1	MGTYRXN0_231
N7	MGTYTXP0_231
N6	MGTYTXN0_231
M4	MGTYRXP1_231
M3	MGTYRXN1_231
M9	MGTYTXP1_231
M8	MGTYTXN1_231
L2	MGTYRXP2_231
L1	MGTYRXN2_231
L7	MGTYTXP2_231
L6	MGTYTXN2_231
K4	MGTYRXP3_231
K3	MGTYRXN3_231
K9	MGTYTXP3_231
K8	MGTYTXN3_231

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U77-54

K GTY QUAD 235

J11	MGTREFCLK0P_235
J10	MGTREFCLK0N_235
H13	MGTREFCLK1P_235
H12	MGTREFCLK1N_235
D18	MGTYRXP0_235
D17	MGTYRXN0_235
D13	MGTYTXP0_235
D12	MGTYTXN0_235
E20	MGTYRXP1_235
E19	MGTYRXN1_235
E15	MGTYTXP1_235
E14	MGTYTXN1_235
F18	MGTYRXP2_235
F17	MGTYRXN2_235
F13	MGTYTXP2_235
F12	MGTYTXN2_235
G20	MGTYRXP3_235
G19	MGTYRXN3_235
G15	MGTYTXP3_235
G14	MGTYTXN3_235

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U77-34

W GTY QUAD 131

U41	MGTREFCLK0P_131
U42	MGTREFCLK0N_131
T39	MGTREFCLK1P_131
T40	MGTREFCLK1N_131
N50	MGTYRXP0_131
N51	MGTYRXN0_131
N45	MGTYTXP0_131
N46	MGTYTXN0_131
M48	MGTYRXP1_131
M49	MGTYRXN1_131
M43	MGTYTXP1_131
M44	MGTYTXN1_131
L50	MGTYRXP2_131
L51	MGTYRXN2_131
L45	MGTYTXP2_131
L46	MGTYTXN2_131
K48	MGTYRXP3_131
K49	MGTYRXN3_131
K43	MGTYTXP3_131
K44	MGTYTXN3_131

FPGA_VU13P_A2577

U77-38

AA GTY QUAD 135

J41	MGTREFCLK0P_135
J42	MGTREFCLK0N_135
H39	MGTREFCLK1P_135
H40	MGTREFCLK1N_135
D34	MGTYRXP0_135
D35	MGTYRXN0_135
D39	MGTYTXP0_135
D40	MGTYTXN0_135
E32	MGTYRXP1_135
E33	MGTYRXN1_135
E37	MGTYTXP1_135
E38	MGTYTXN1_135
F34	MGTYRXP2_135
F35	MGTYRXN2_135
F39	MGTYTXP2_135
F40	MGTYTXN2_135
G32	MGTYRXP3_135
G33	MGTYRXN3_135
G37	MGTYTXP3_135
G38	MGTYTXN3_135

FPGA_VU13P_A2577

APOLLO CM W/ DUAL A2577, MK1

Title: 8.09: FPGA#2 UNUSED QUADS G, K, W, AA

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9.01: F1 QUADS M, N, O TO F2 QUADS J, I, H

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

FPGA#1

U75-40
GTY QUAD 221 M

MGTREFCLK0P_221	BB13	
MGTREFCLK0N_221	BB12	
MGTREFCLK1P_221	BA11	
MGTREFCLK1N_221	BA10	
MGTYRXP0_221	BK18	pF1_M_RECV0
MGTYRXN0_221	BK17	nF1_M_RECV0
MGTYTXP0_221	BL15	pF1_M_XMIT0
MGTYTXN0_221	BL14	nF1_M_XMIT0
MGTYRXP1_221	BL20	pF1_M_RECV1
MGTYRXN1_221	BL19	nF1_M_RECV1
MGTYTXP1_221	BK13	pF1_M_XMIT1
MGTYTXN1_221	BK12	nF1_M_XMIT1
MGTYRXP2_221	BL6	pF1_M_RECV2
MGTYRXN2_221	BL5	nF1_M_RECV2
MGTYTXP2_221	BL11	pF1_M_XMIT2
MGTYTXN2_221	BL10	nF1_M_XMIT2
MGTYRXP3_221	BJ6	pF1_M_RECV3
MGTYRXN3_221	BJ5	nF1_M_RECV3
MGTYTXP3_221	BK9	pF1_M_XMIT3
MGTYTXN3_221	BK8	nF1_M_XMIT3

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pF1_M_RECV0	C284 0.1 UF 0402	pF2_J_XMIT0
nF1_M_RECV0		nF2_J_XMIT0
	C283 0.1 UF 0402	
pF1_M_RECV1	C286 0.1 UF 0402	pF2_J_XMIT1
nF1_M_RECV1		nF2_J_XMIT1
	C285 0.1 UF 0402	
pF1_M_RECV2	C282 0.1 UF 0402	pF2_J_XMIT2
nF1_M_RECV2		nF2_J_XMIT2
	C281 0.1 UF 0402	
pF1_M_RECV3	C280 0.1 UF 0402	pF2_J_XMIT3
nF1_M_RECV3		nF2_J_XMIT3
	C279 0.1 UF 0402	

pF1_M_XMIT0	0402 0.1 UF C294	pF2_J_RECV0
nF1_M_XMIT0		nF2_J_RECV0
	0402 0.1 UF C293	
pF1_M_XMIT1	0402 0.1 UF C292	pF2_J_RECV1
nF1_M_XMIT1		nF2_J_RECV1
	0402 0.1 UF C291	
pF1_M_XMIT2	0402 0.1 UF C290	pF2_J_RECV2
nF1_M_XMIT2		nF2_J_RECV2
	0402 0.1 UF C289	
pF1_M_XMIT3	0402 0.1 UF C288	pF2_J_RECV3
nF1_M_XMIT3		nF2_J_RECV3
	0402 0.1 UF C287	

FPGA#2

U77-53
GTY QUAD 234 J

L11		MGTREFCLK0P_234
L10		MGTREFCLK0N_234
K13		MGTREFCLK1P_234
K12		MGTREFCLK1N_234
pF2_J_RECV3	A6	MGTYRXP0_234
nF2_J_RECV3	A5	MGTYRXN0_234
pF2_J_XMIT3	A11	MGTYTXP0_234
nF2_J_XMIT3	A10	MGTYTXN0_234
pF2_J_RECV2	A20	MGTYRXP1_234
nF2_J_RECV2	A19	MGTYRXN1_234
pF2_J_XMIT2	B13	MGTYTXP1_234
nF2_J_XMIT2	B12	MGTYTXN1_234
pF2_J_RECV1	B18	MGTYRXP2_234
nF2_J_RECV1	B17	MGTYRXN2_234
pF2_J_XMIT1	A15	MGTYTXP2_234
nF2_J_XMIT1	A14	MGTYTXN2_234
pF2_J_RECV0	C20	MGTYRXP3_234
nF2_J_RECV0	C19	MGTYRXN3_234
pF2_J_XMIT0	C15	MGTYTXP3_234
nF2_J_XMIT0	C14	MGTYTXN3_234

FPGA_VU13P_A2577

U75-41
GTY QUAD 222 N

		ac_pF1R_R0_N 20
		ac_nF1R_R0_N 20
		ac_pF1R_R1_N 23
		ac_nF1R_R1_N 23
MGTREFCLK0P_222	AY13	
MGTREFCLK0N_222	AY12	
MGTREFCLK1P_222	AW11	
MGTREFCLK1N_222	AW10	
MGTYRXP0_222	BH4	pF1_N_RECV0
MGTYRXN0_222	BH3	nF1_N_RECV0
MGTYTXP0_222	BG11	pF1_N_XMIT0
MGTYTXN0_222	BG10	nF1_N_XMIT0
MGTYRXP1_222	BG2	pF1_N_RECV1
MGTYRXN1_222	BG1	nF1_N_RECV1
MGTYTXP1_222	BJ11	pF1_N_XMIT1
MGTYTXN1_222	BJ10	nF1_N_XMIT1
MGTYRXP2_222	BG6	pF1_N_RECV2
MGTYRXN2_222	BG5	nF1_N_RECV2
MGTYTXP2_222	BH9	pF1_N_XMIT2
MGTYTXN2_222	BH8	nF1_N_XMIT2
MGTYRXP3_222	BF4	pF1_N_RECV3
MGTYRXN3_222	BF3	nF1_N_RECV3
MGTYTXP3_222	BF9	pF1_N_XMIT3
MGTYTXN3_222	BF8	nF1_N_XMIT3

FPGA_VU13P_A2577

pF1_N_RECV0	C270 0.1 UF 0402	pF2_I_XMIT0
nF1_N_RECV0		nF2_I_XMIT0
	C269 0.1 UF 0402	
pF1_N_RECV1	C266 0.1 UF 0402	pF2_I_XMIT1
nF1_N_RECV1		nF2_I_XMIT1
	C265 0.1 UF 0402	
pF1_N_RECV2	C268 0.1 UF 0402	pF2_I_XMIT2
nF1_N_RECV2		nF2_I_XMIT2
	C267 0.1 UF 0402	
pF1_N_RECV3	C264 0.1 UF 0402	pF2_I_XMIT3
nF1_N_RECV3		nF2_I_XMIT3
	C263 0.1 UF 0402	

pF1_N_XMIT0	0402 0.1 UF C274	pF2_I_RECV0
nF1_N_XMIT0		nF2_I_RECV0
	0402 0.1 UF C273	
pF1_N_XMIT1	0402 0.1 UF C278	pF2_I_RECV1
nF1_N_XMIT1		nF2_I_RECV1
	0402 0.1 UF C277	
pF1_N_XMIT2	0402 0.1 UF C276	pF2_I_RECV2
nF1_N_XMIT2		nF2_I_RECV2
	0402 0.1 UF C275	
pF1_N_XMIT3	0402 0.1 UF C272	pF2_I_RECV3
nF1_N_XMIT3		nF2_I_RECV3
	0402 0.1 UF C271	

U77-52
GTY QUAD 233 I

ac_pF2R_R0_I 20		
ac_nF2R_R0_I 20		
ac_pF2R_R1_I 23		
ac_nF2R_R1_I 23		
	N11	MGTREFCLK0P_233
	N10	MGTREFCLK0N_233
	M13	MGTREFCLK1P_233
	M12	MGTREFCLK1N_233
pF2_I_RECV3	E2	MGTYRXP0_233
nF2_I_RECV3	E1	MGTYRXN0_233
pF2_I_XMIT3	D9	MGTYTXP0_233
nF2_I_XMIT3	D8	MGTYTXN0_233
pF2_I_RECV2	D4	MGTYRXP1_233
nF2_I_RECV2	D3	MGTYRXN1_233
pF2_I_XMIT2	B9	MGTYTXP1_233
nF2_I_XMIT2	B8	MGTYTXN1_233
pF2_I_RECV1	E6	MGTYRXP2_233
nF2_I_RECV1	E5	MGTYRXN2_233
pF2_I_XMIT1	C11	MGTYTXP2_233
nF2_I_XMIT1	C10	MGTYTXN2_233
pF2_I_RECV0	C6	MGTYRXP3_233
nF2_I_RECV0	C5	MGTYRXN3_233
pF2_I_XMIT0	E11	MGTYTXP3_233
nF2_I_XMIT0	E10	MGTYTXN3_233

FPGA_VU13P_A2577

U75-42
GTY QUAD 223 O

MGTREFCLK0P_223	AV13	
MGTREFCLK0N_223	AV12	
MGTREFCLK1P_223	AU11	
MGTREFCLK1N_223	AU10	
MGTYRXP0_223	BE2	pF1_O_RECV0
MGTYRXN0_223	BE1	nF1_O_RECV0
MGTYTXP0_223	BE7	pF1_O_XMIT0
MGTYTXN0_223	BE6	nF1_O_XMIT0
MGTYRXP1_223	BD4	pF1_O_RECV1
MGTYRXN1_223	BD3	nF1_O_RECV1
MGTYTXP1_223	BD9	pF1_O_XMIT1
MGTYTXN1_223	BD8	nF1_O_XMIT1
MGTYRXP2_223	BC2	pF1_O_RECV2
MGTYRXN2_223	BC1	nF1_O_RECV2
MGTYTXP2_223	BC7	pF1_O_XMIT2
MGTYTXN2_223	BC6	nF1_O_XMIT2
MGTYRXP3_223	BB4	pF1_O_RECV3
MGTYRXN3_223	BB3	nF1_O_RECV3
MGTYTXP3_223	BB9	pF1_O_XMIT3
MGTYTXN3_223	BB8	nF1_O_XMIT3

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pF1_O_RECV0	C252 0.1 UF 0402	pF2_H_XMIT0
nF1_O_RECV0		nF2_H_XMIT0
	C251 0.1 UF 0402	
pF1_O_RECV1	C250 0.1 UF 0402	pF2_H_XMIT1
nF1_O_RECV1		nF2_H_XMIT1
	C249 0.1 UF 0402	
pF1_O_RECV2	C248 0.1 UF 0402	pF2_H_XMIT2
nF1_O_RECV2		nF2_H_XMIT2
	C247 0.1 UF 0402	
pF1_O_RECV3	C246 0.1 UF 0402	pF2_H_XMIT3
nF1_O_RECV3		nF2_H_XMIT3
	C245 0.1 UF 0402	

pF1_O_XMIT0	0402 0.1 UF C260	pF2_H_RECV0
nF1_O_XMIT0		nF2_H_RECV0
	0402 0.1 UF C259	
pF1_O_XMIT1	0402 0.1 UF C258	pF2_H_RECV1
nF1_O_XMIT1		nF2_H_RECV1
	0402 0.1 UF C257	
pF1_O_XMIT2	0402 0.1 UF C256	pF2_H_RECV2
nF1_O_XMIT2		nF2_H_RECV2
	0402 0.1 UF C255	
pF1_O_XMIT3	0402 0.1 UF C254	pF2_H_RECV3
nF1_O_XMIT3		nF2_H_RECV3
	0402 0.1 UF C253	

U77-51
GTY QUAD 232 H

	R11	MGTREFCLK0P_232
	R10	MGTREFCLK0N_232
	P13	MGTREFCLK1P_232
	P12	MGTREFCLK1N_232
pF2_H_RECV3	J2	MGTYRXP0_232
nF2_H_RECV3	J1	MGTYRXN0_232
pF2_H_XMIT3	J7	MGTYTXP0_232
nF2_H_XMIT3	J6	MGTYTXN0_232
pF2_H_RECV2	H4	MGTYRXP1_232
nF2_H_RECV2	H3	MGTYRXN1_232
pF2_H_XMIT2	H9	MGTYTXP1_232
nF2_H_XMIT2	H8	MGTYTXN1_232
pF2_H_RECV1	G2	MGTYRXP2_232
nF2_H_RECV1	G1	MGTYRXN2_232
pF2_H_XMIT1	G7	MGTYTXP2_232
nF2_H_XMIT1	G6	MGTYTXN2_232
pF2_H_RECV0	F4	MGTYRXP3_232
nF2_H_RECV0	F3	MGTYRXN3_232
pF2_H_XMIT0	F9	MGTYTXP3_232
nF2_H_XMIT0	F8	MGTYTXN3_232

FPGA_VU13P_A2577

APOLLO CM W/ DUAL A2577, MK1

Title: 9.01: F1 QUADS M, N, O TO F2 QUADS J, I, H

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	6089-119	A

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9.02: F1 QUADS A, B, C TO F2 QUADS F, E, D

FPGA#1

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

FPGA#2

U75-44
GTY QUAD 225 A

MGTREFCLK0P_225	AP13	
MGTREFCLK0N_225	AP12	
MGTREFCLK1P_225	AN11	
MGTREFCLK1N_225	AN10	
MGTYRXP0_225	AU2	pF1_A_RECV0
MGTYRXN0_225	AU1	nF1_A_RECV0
MGTYTXP0_225	AU7	pF1_A_XMIT0
MGTYTXN0_225	AU6	nF1_A_XMIT0
MGTYRXP1_225	AT4	pF1_A_RECV1
MGTYRXN1_225	AT3	nF1_A_RECV1
MGTYTXP1_225	AT9	pF1_A_XMIT1
MGTYTXN1_225	AT8	nF1_A_XMIT1
MGTYRXP2_225	AR2	pF1_A_RECV2
MGTYRXN2_225	AR1	nF1_A_RECV2
MGTYTXP2_225	AR7	pF1_A_XMIT2
MGTYTXN2_225	AR6	nF1_A_XMIT2
MGTYRXP3_225	AP4	pF1_A_RECV3
MGTYRXN3_225	AP3	nF1_A_RECV3
MGTYTXP3_225	AP9	pF1_A_XMIT3
MGTYTXN3_225	AP8	nF1_A_XMIT3

FPGA_VU13P_A2577

U75-45
GTY QUAD 226 B

MGTREFCLK0P_226	AM13	ac_pF1R_R0_B 20
MGTREFCLK0N_226	AM12	ac_nF1R_R0_B 20
MGTREFCLK1P_226	AL11	ac_pF1R_R1_B 23
MGTREFCLK1N_226	AL10	ac_nF1R_R1_B 23
MGTYRXP0_226	AN2	pF1_B_RECV0
MGTYRXN0_226	AN1	nF1_B_RECV0
MGTYTXP0_226	AN7	pF1_B_XMIT0
MGTYTXN0_226	AN6	nF1_B_XMIT0
MGTYRXP1_226	AM4	pF1_B_RECV1
MGTYRXN1_226	AM3	nF1_B_RECV1
MGTYTXP1_226	AM9	pF1_B_XMIT1
MGTYTXN1_226	AM8	nF1_B_XMIT1
MGTYRXP2_226	AL2	pF1_B_RECV2
MGTYRXN2_226	AL1	nF1_B_RECV2
MGTYTXP2_226	AL7	pF1_B_XMIT2
MGTYTXN2_226	AL6	nF1_B_XMIT2
MGTYRXP3_226	AK4	pF1_B_RECV3
MGTYRXN3_226	AK3	nF1_B_RECV3
MGTYTXP3_226	AK9	pF1_B_XMIT3
MGTYTXN3_226	AK8	nF1_B_XMIT3

FPGA_VU13P_A2577

U75-46
GTY QUAD 227 C

MGTREFCLK0P_227	AJ11	
MGTREFCLK0N_227	AJ10	
MGTREFCLK1P_227	AG11	
MGTREFCLK1N_227	AG10	
MGTYRXP0_227	AJ2	pF1_C_RECV0
MGTYRXN0_227	AJ1	nF1_C_RECV0
MGTYTXP0_227	AJ7	pF1_C_XMIT0
MGTYTXN0_227	AJ6	nF1_C_XMIT0
MGTYRXP1_227	AH4	pF1_C_RECV1
MGTYRXN1_227	AH3	nF1_C_RECV1
MGTYTXP1_227	AH9	pF1_C_XMIT1
MGTYTXN1_227	AH8	nF1_C_XMIT1
MGTYRXP2_227	AG2	pF1_C_RECV2
MGTYRXN2_227	AG1	nF1_C_RECV2
MGTYTXP2_227	AG7	pF1_C_XMIT2
MGTYTXN2_227	AG6	nF1_C_XMIT2
MGTYRXP3_227	AF4	pF1_C_RECV3
MGTYRXN3_227	AF3	nF1_C_RECV3
MGTYTXP3_227	AF9	pF1_C_XMIT3
MGTYTXN3_227	AF8	nF1_C_XMIT3

FPGA_VU13P_A2577

pF1_A_RECV0	C218	0.1 UF	0402	pF2_F_XMIT0
nF1_A_RECV0				nF2_F_XMIT0
pF1_A_RECV1	C216	0.1 UF	0402	pF2_F_XMIT1
nF1_A_RECV1				nF2_F_XMIT1
pF1_A_RECV2	C214	0.1 UF	0402	pF2_F_XMIT2
nF1_A_RECV2				nF2_F_XMIT2
pF1_A_RECV3	C212	0.1 UF	0402	pF2_F_XMIT3
nF1_A_RECV3				nF2_F_XMIT3

C217 0.1 UF 0402
C215 0.1 UF 0402
C213 0.1 UF 0402
C211 0.1 UF 0402

pF1_A_XMIT0	0402	0.1 UF	C226	pF2_F_RECV0
nF1_A_XMIT0				nF2_F_RECV0
pF1_A_XMIT1	0402	0.1 UF	C224	pF2_F_RECV1
nF1_A_XMIT1				nF2_F_RECV1
pF1_A_XMIT2	0402	0.1 UF	C222	pF2_F_RECV2
nF1_A_XMIT2				nF2_F_RECV2
pF1_A_XMIT3	0402	0.1 UF	C220	pF2_F_RECV3
nF1_A_XMIT3				nF2_F_RECV3

0402 0.1 UF C225
0402 0.1 UF C223
0402 0.1 UF C221
0402 0.1 UF C219

U77-49
GTY QUAD 230 F

ac_pF2R_R0_F 20	W11	
ac_nF2R_R0_F 20	W10	
	V13	MGTREFCLK0P_230
	V12	MGTREFCLK0N_230
		MGTREFCLK1P_230
		MGTREFCLK1N_230
pF2_F_RECV3	U2	MGTYRXP0_230
nF2_F_RECV3	U1	MGTYRXN0_230
pF2_F_XMIT3	U7	MGTYTXP0_230
nF2_F_XMIT3	U6	MGTYTXN0_230
pF2_F_RECV2	T4	MGTYRXP1_230
nF2_F_RECV2	T3	MGTYRXN1_230
pF2_F_XMIT2	T9	MGTYTXP1_230
nF2_F_XMIT2	T8	MGTYTXN1_230
pF2_F_RECV1	R2	MGTYRXP2_230
nF2_F_RECV1	R1	MGTYRXN2_230
pF2_F_XMIT1	R7	MGTYTXP2_230
nF2_F_XMIT1	R6	MGTYTXN2_230
pF2_F_RECV0	P4	MGTYRXP3_230
nF2_F_RECV0	P3	MGTYRXN3_230
pF2_F_XMIT0	P9	MGTYTXP3_230
nF2_F_XMIT0	P8	MGTYTXN3_230

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U77-48
GTY QUAD 229 E

ac_pF2R_R0_E 20	AA11	
ac_nF2R_R0_E 20	AA10	
		MGTREFCLK0P_229
		MGTREFCLK0N_229
ac_pF2R_R1_E 23	Y13	
ac_nF2R_R1_E 23	Y12	
		MGTREFCLK1P_229
		MGTREFCLK1N_229
pF2_E_RECV3	AA2	MGTYRXP0_229
nF2_E_RECV3	AA1	MGTYRXN0_229
pF2_E_XMIT3	AA7	MGTYTXP0_229
nF2_E_XMIT3	AA6	MGTYTXN0_229
pF2_E_RECV2	Y4	MGTYRXP1_229
nF2_E_RECV2	Y3	MGTYRXN1_229
pF2_E_XMIT2	Y9	MGTYTXP1_229
nF2_E_XMIT2	Y8	MGTYTXN1_229
pF2_E_RECV1	W2	MGTYRXP2_229
nF2_E_RECV1	W1	MGTYRXN2_229
pF2_E_XMIT1	W7	MGTYTXP2_229
nF2_E_XMIT1	W6	MGTYTXN2_229
pF2_E_RECV0	V4	MGTYRXP3_229
nF2_E_RECV0	V3	MGTYRXN3_229
pF2_E_XMIT0	V9	MGTYTXP3_229
nF2_E_XMIT0	V8	MGTYTXN3_229

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pF1_B_RECV0	C202	0.1 UF	0402	pF2_E_XMIT0
nF1_B_RECV0				nF2_E_XMIT0
pF1_B_RECV1	C200	0.1 UF	0402	pF2_E_XMIT1
nF1_B_RECV1				nF2_E_XMIT1
pF1_B_RECV2	C198	0.1 UF	0402	pF2_E_XMIT2
nF1_B_RECV2				nF2_E_XMIT2
pF1_B_RECV3	C196	0.1 UF	0402	pF2_E_XMIT3
nF1_B_RECV3				nF2_E_XMIT3

C201 0.1 UF 0402
C199 0.1 UF 0402
C197 0.1 UF 0402
C195 0.1 UF 0402

pF1_B_XMIT0	0402	0.1 UF	C210	pF2_E_RECV0
nF1_B_XMIT0				nF2_E_RECV0
pF1_B_XMIT1	0402	0.1 UF	C208	pF2_E_RECV1
nF1_B_XMIT1				nF2_E_RECV1
pF1_B_XMIT2	0402	0.1 UF	C206	pF2_E_RECV2
nF1_B_XMIT2				nF2_E_RECV2
pF1_B_XMIT3	0402	0.1 UF	C204	pF2_E_RECV3
nF1_B_XMIT3				nF2_E_RECV3

0402 0.1 UF C209
0402 0.1 UF C207
0402 0.1 UF C205
0402 0.1 UF C203

U77-47
GTY QUAD 228 D

	AE11	MGTREFCLK0P_228
	AE10	MGTREFCLK0N_228
	AC11	MGTREFCLK1P_228
	AC10	MGTREFCLK1N_228
pF2_D_RECV3	AE2	MGTYRXP0_228
nF2_D_RECV3	AE1	MGTYRXN0_228
pF2_D_XMIT3	AE7	MGTYTXP0_228
nF2_D_XMIT3	AE6	MGTYTXN0_228
pF2_D_RECV2	AD4	MGTYRXP1_228
nF2_D_RECV2	AD3	MGTYRXN1_228
pF2_D_XMIT2	AD9	MGTYTXP1_228
nF2_D_XMIT2	AD8	MGTYTXN1_228
pF2_D_RECV1	AC2	MGTYRXP2_228
nF2_D_RECV1	AC1	MGTYRXN2_228
pF2_D_XMIT1	AC7	MGTYTXP2_228
nF2_D_XMIT1	AC6	MGTYTXN2_228
pF2_D_RECV0	AB4	MGTYRXP3_228
nF2_D_RECV0	AB3	MGTYRXN3_228
pF2_D_XMIT0	AB9	MGTYTXP3_228
nF2_D_XMIT0	AB8	MGTYTXN3_228

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pF1_C_RECV0	C182	0.1 UF	0402	pF2_D_XMIT0
nF1_C_RECV0				nF2_D_XMIT0
pF1_C_RECV1	C180	0.1 UF	0402	pF2_D_XMIT1
nF1_C_RECV1				nF2_D_XMIT1
pF1_C_RECV2	C178	0.1 UF	0402	pF2_D_XMIT2
nF1_C_RECV2				nF2_D_XMIT2
pF1_C_RECV3	C176	0.1 UF	0402	pF2_D_XMIT3
nF1_C_RECV3				nF2_D_XMIT3

C181 0.1 UF 0402
C179 0.1 UF 0402
C177 0.1 UF 0402
C175 0.1 UF 0402

pF1_C_XMIT0	0402	0.1 UF	C190	pF2_D_RECV0
nF1_C_XMIT0				nF2_D_RECV0
pF1_C_XMIT1	0402	0.1 UF	C188	pF2_D_RECV1
nF1_C_XMIT1				nF2_D_RECV1
pF1_C_XMIT2	0402	0.1 UF	C186	pF2_D_RECV2
nF1_C_XMIT2				nF2_D_RECV2
pF1_C_XMIT3	0402	0.1 UF	C184	pF2_D_RECV3
nF1_C_XMIT3				nF2_D_RECV3

0402 0.1 UF C189
0402 0.1 UF C187
0402 0.1 UF C185
0402 0.1 UF C183

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Title: 9.02: F1 QUADS A, B, C TO F2 QUADS F, E, D

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9.03: F1 QUADS H, I, J TO F2 QUADS O, N, M

FPGA#1

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

FPGA#2

U75-51
GTY QUAD 232 H

MGTREFCLK0P_232	R11	
MGTREFCLK0N_232	R10	
MGTREFCLK1P_232	P13	
MGTREFCLK1N_232	P12	
MGTYRXP0_232	J2	pF1_H_RECV0
MGTYRXN0_232	J1	nF1_H_RECV0
MGTYTXP0_232	J7	pF1_H_XMIT0
MGTYTXN0_232	J6	nF1_H_XMIT0
MGTYRXP1_232	H4	pF1_H_RECV1
MGTYRXN1_232	H3	nF1_H_RECV1
MGTYTXP1_232	H9	pF1_H_XMIT1
MGTYTXN1_232	H8	nF1_H_XMIT1
MGTYRXP2_232	G2	pF1_H_RECV2
MGTYRXN2_232	G1	nF1_H_RECV2
MGTYTXP2_232	G7	pF1_H_XMIT2
MGTYTXN2_232	G6	nF1_H_XMIT2
MGTYRXP3_232	F4	pF1_H_RECV3
MGTYRXN3_232	F3	nF1_H_RECV3
MGTYTXP3_232	F9	pF1_H_XMIT3
MGTYTXN3_232	F8	nF1_H_XMIT3

FPGA_VU13P_A2577

U75-52
GTY QUAD 233 I

MGTREFCLK0P_233	N11	ac_pF1R_R0_I 20
MGTREFCLK0N_233	N10	ac_nF1R_R0_I 20
MGTREFCLK1P_233	M13	ac_pF1R_R1_I 23
MGTREFCLK1N_233	M12	ac_nF1R_R1_I 23
MGTYRXP0_233	E2	pF1_I_RECV0
MGTYRXN0_233	E1	nF1_I_RECV0
MGTYTXP0_233	D9	pF1_I_XMIT0
MGTYTXN0_233	D8	nF1_I_XMIT0
MGTYRXP1_233	D4	pF1_I_RECV1
MGTYRXN1_233	D3	nF1_I_RECV1
MGTYTXP1_233	B9	pF1_I_XMIT1
MGTYTXN1_233	B8	nF1_I_XMIT1
MGTYRXP2_233	E6	pF1_I_RECV2
MGTYRXN2_233	E5	nF1_I_RECV2
MGTYTXP2_233	C11	pF1_I_XMIT2
MGTYTXN2_233	C10	nF1_I_XMIT2
MGTYRXP3_233	C6	pF1_I_RECV3
MGTYRXN3_233	C5	nF1_I_RECV3
MGTYTXP3_233	E11	pF1_I_XMIT3
MGTYTXN3_233	E10	nF1_I_XMIT3

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U75-53
GTY QUAD 234 J

MGTREFCLK0P_234	L11	
MGTREFCLK0N_234	L10	
MGTREFCLK1P_234	K13	
MGTREFCLK1N_234	K12	
MGTYRXP0_234	A6	pF1_J_RECV0
MGTYRXN0_234	A5	nF1_J_RECV0
MGTYTXP0_234	A11	pF1_J_XMIT0
MGTYTXN0_234	A10	nF1_J_XMIT0
MGTYRXP1_234	A20	pF1_J_RECV1
MGTYRXN1_234	A19	nF1_J_RECV1
MGTYTXP1_234	B13	pF1_J_XMIT1
MGTYTXN1_234	B12	nF1_J_XMIT1
MGTYRXP2_234	B18	pF1_J_RECV2
MGTYRXN2_234	B17	nF1_J_RECV2
MGTYTXP2_234	A15	pF1_J_XMIT2
MGTYTXN2_234	A14	nF1_J_XMIT2
MGTYRXP3_234	C20	pF1_J_RECV3
MGTYRXN3_234	C19	nF1_J_RECV3
MGTYTXP3_234	C15	pF1_J_XMIT3
MGTYTXN3_234	C14	nF1_J_XMIT3

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pF1_H_RECV0 / nF1_H_RECV0 — C85 0.1 UF 0402 — pF2_O_XMIT0 / nF2_O_XMIT0
pF1_H_RECV1 / nF1_H_RECV1 — C83 0.1 UF 0402 — pF2_O_XMIT1 / nF2_O_XMIT1
pF1_H_RECV2 / nF1_H_RECV2 — C81 0.1 UF 0402 — pF2_O_XMIT2 / nF2_O_XMIT2
pF1_H_RECV3 / nF1_H_RECV3 — C79 0.1 UF 0402 — pF2_O_XMIT3 / nF2_O_XMIT3
C84 0.1 UF 0402
C82 0.1 UF 0402
C80 0.1 UF 0402
C78 0.1 UF 0402

pF1_H_XMIT0 / nF1_H_XMIT0 — 0402 0.1 UF C93 — pF2_O_RECV0 / nF2_O_RECV0
pF1_H_XMIT1 / nF1_H_XMIT1 — 0402 0.1 UF C91 — pF2_O_RECV1 / nF2_O_RECV1
pF1_H_XMIT2 / nF1_H_XMIT2 — 0402 0.1 UF C89 — pF2_O_RECV2 / nF2_O_RECV2
pF1_H_XMIT3 / nF1_H_XMIT3 — 0402 0.1 UF C87 — pF2_O_RECV3 / nF2_O_RECV3
0402 0.1 UF C92
0402 0.1 UF C90
0402 0.1 UF C88
0402 0.1 UF C86

U77-42
GTY QUAD 223 O

MGTREFCLK0P_223	AV13	
MGTREFCLK0N_223	AV12	
MGTREFCLK1P_223	AU11	
MGTREFCLK1N_223	AU10	
MGTYRXP0_223	BE2	pF2_O_RECV3
MGTYRXN0_223	BE1	nF2_O_RECV3
MGTYTXP0_223	BE7	pF2_O_XMIT3
MGTYTXN0_223	BE6	nF2_O_XMIT3
MGTYRXP1_223	BD4	pF2_O_RECV2
MGTYRXN1_223	BD3	nF2_O_RECV2
MGTYTXP1_223	BD9	pF2_O_XMIT2
MGTYTXN1_223	BD8	nF2_O_XMIT2
MGTYRXP2_223	BC2	pF2_O_RECV1
MGTYRXN2_223	BC1	nF2_O_RECV1
MGTYTXP2_223	BC7	pF2_O_XMIT1
MGTYTXN2_223	BC6	nF2_O_XMIT1
MGTYRXP3_223	BB4	pF2_O_RECV0
MGTYRXN3_223	BB3	nF2_O_RECV0
MGTYTXP3_223	BB9	pF2_O_XMIT0
MGTYTXN3_223	BB8	nF2_O_XMIT0

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U77-41
GTY QUAD 222 N

ac_pF2R_R0_N 20		
ac_nF2R_R0_N 20		
ac_pF2R_R1_N 23		
ac_nF2R_R1_N 23		
MGTREFCLK0P_222	AY13	
MGTREFCLK0N_222	AY12	
MGTREFCLK1P_222	AW11	
MGTREFCLK1N_222	AW10	
MGTYRXP0_222	BH4	pF2_N_RECV3
MGTYRXN0_222	BH3	nF2_N_RECV3
MGTYTXP0_222	BG11	pF2_N_XMIT3
MGTYTXN0_222	BG10	nF2_N_XMIT3
MGTYRXP1_222	BG2	pF2_N_RECV2
MGTYRXN1_222	BG1	nF2_N_RECV2
MGTYTXP1_222	BJ11	pF2_N_XMIT2
MGTYTXN1_222	BJ10	nF2_N_XMIT2
MGTYRXP2_222	BG6	pF2_N_RECV1
MGTYRXN2_222	BG5	nF2_N_RECV1
MGTYTXP2_222	BH9	pF2_N_XMIT1
MGTYTXN2_222	BH8	nF2_N_XMIT1
MGTYRXP3_222	BF4	pF2_N_RECV0
MGTYRXN3_222	BF3	nF2_N_RECV0
MGTYTXP3_222	BF9	pF2_N_XMIT0
MGTYTXN3_222	BF8	nF2_N_XMIT0

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pF1_I_RECV0 / nF1_I_RECV0 — C65 0.1 UF 0402 — pF2_N_XMIT0 / nF2_N_XMIT0
pF1_I_RECV1 / nF1_I_RECV1 — C63 0.1 UF 0402 — pF2_N_XMIT1 / nF2_N_XMIT1
pF1_I_RECV2 / nF1_I_RECV2 — C58 0.1 UF 0402 — pF2_N_XMIT2 / nF2_N_XMIT2
pF1_I_RECV3 / nF1_I_RECV3 — C60 0.1 UF 0402 — pF2_N_XMIT3 / nF2_N_XMIT3
C64 0.1 UF 0402
C62 0.1 UF 0402
C59 0.1 UF 0402
C61 0.1 UF 0402

pF1_I_XMIT0 / nF1_I_XMIT0 — 0402 0.1 UF C73 — pF2_N_RECV0 / nF2_N_RECV0
pF1_I_XMIT1 / nF1_I_XMIT1 — 0402 0.1 UF C71 — pF2_N_RECV1 / nF2_N_RECV1
pF1_I_XMIT2 / nF1_I_XMIT2 — 0402 0.1 UF C68 — pF2_N_RECV2 / nF2_N_RECV2
pF1_I_XMIT3 / nF1_I_XMIT3 — 0402 0.1 UF C66 — pF2_N_RECV3 / nF2_N_RECV3
0402 0.1 UF C72
0402 0.1 UF C70
0402 0.1 UF C69
0402 0.1 UF C67

pF1_J_RECV0 / nF1_J_RECV0 — C48 0.1 UF 0402 — pF2_M_XMIT0 / nF2_M_XMIT0
pF1_J_RECV1 / nF1_J_RECV1 — C46 0.1 UF 0402 — pF2_M_XMIT1 / nF2_M_XMIT1
pF1_J_RECV2 / nF1_J_RECV2 — C44 0.1 UF 0402 — pF2_M_XMIT2 / nF2_M_XMIT2
pF1_J_RECV3 / nF1_J_RECV3 — C42 0.1 UF 0402 — pF2_M_XMIT3 / nF2_M_XMIT3
C49 0.1 UF 0402
C47 0.1 UF 0402
C45 0.1 UF 0402
C43 0.1 UF 0402

pF1_J_XMIT0 / nF1_J_XMIT0 — 0402 0.1 UF C56 — pF2_M_RECV0 / nF2_M_RECV0
pF1_J_XMIT1 / nF1_J_XMIT1 — 0402 0.1 UF C54 — pF2_M_RECV1 / nF2_M_RECV1
pF1_J_XMIT2 / nF1_J_XMIT2 — 0402 0.1 UF C50 — pF2_M_RECV2 / nF2_M_RECV2
pF1_J_XMIT3 / nF1_J_XMIT3 — 0402 0.1 UF C52 — pF2_M_RECV3 / nF2_M_RECV3
0402 0.1 UF C57
0402 0.1 UF C55
0402 0.1 UF C51
0402 0.1 UF C53

U77-40
GTY QUAD 221 M

MGTREFCLK0P_221	BB13	
MGTREFCLK0N_221	BB12	
MGTREFCLK1P_221	BA11	
MGTREFCLK1N_221	BA10	
MGTYRXP0_221	BK18	pF2_M_RECV3
MGTYRXN0_221	BK17	nF2_M_RECV3
MGTYTXP0_221	BL15	pF2_M_XMIT3
MGTYTXN0_221	BL14	nF2_M_XMIT3
MGTYRXP1_221	BL20	pF2_M_RECV2
MGTYRXN1_221	BL19	nF2_M_RECV2
MGTYTXP1_221	BK13	pF2_M_XMIT2
MGTYTXN1_221	BK12	nF2_M_XMIT2
MGTYRXP2_221	BL6	pF2_M_RECV1
MGTYRXN2_221	BL5	nF2_M_RECV1
MGTYTXP2_221	BL11	pF2_M_XMIT1
MGTYTXN2_221	BL10	nF2_M_XMIT1
MGTYRXP3_221	BJ6	pF2_M_RECV0
MGTYRXN3_221	BJ5	nF2_M_RECV0
MGTYTXP3_221	BK9	pF2_M_XMIT0
MGTYTXN3_221	BK8	nF2_M_XMIT0

FPGA_VU13P_A2577

APOLLO CM W/ DUAL A2577, MK1

Title: 9.03: F1 QUADS H, I, J TO F2 QUADS O, N, M

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9.04: F1 QUADS D, E, F TO F2 QUADS C, B, A

FPGA#1

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

FPGA#2

U75-47 — GTY QUAD 228 D

MGTREFCLK0P_228	AE11	
MGTREFCLK0N_228	AE10	
MGTREFCLK1P_228	AC11	
MGTREFCLK1N_228	AC10	
MGTYRXP0_228	AE2	pF1_D_RECV0
MGTYRXN0_228	AE1	nF1_D_RECV0
MGTYTXP0_228	AE7	pF1_D_XMIT0
MGTYTXN0_228	AE6	nF1_D_XMIT0
MGTYRXP1_228	AD4	pF1_D_RECV1
MGTYRXN1_228	AD3	nF1_D_RECV1
MGTYTXP1_228	AD9	pF1_D_XMIT1
MGTYTXN1_228	AD8	nF1_D_XMIT1
MGTYRXP2_228	AC2	pF1_D_RECV2
MGTYRXN2_228	AC1	nF1_D_RECV2
MGTYTXP2_228	AC7	pF1_D_XMIT2
MGTYTXN2_228	AC6	nF1_D_XMIT2
MGTYRXP3_228	AB4	pF1_D_RECV3
MGTYRXN3_228	AB3	nF1_D_RECV3
MGTYTXP3_228	AB9	pF1_D_XMIT3
MGTYTXN3_228	AB8	nF1_D_XMIT3

FPGA_VU13P_A2577

U75-48 — GTY QUAD 229 E

MGTREFCLK0P_229	AA11	ac_pF1R_R0_E 20
MGTREFCLK0N_229	AA10	ac_nF1R_R0_E 20
MGTREFCLK1P_229	Y13	ac_pF1R_R1_E 23
MGTREFCLK1N_229	Y12	ac_nF1R_R1_E 23
MGTYRXP0_229	AA2	pF1_E_RECV0
MGTYRXN0_229	AA1	nF1_E_RECV0
MGTYTXP0_229	AA7	pF1_E_XMIT0
MGTYTXN0_229	AA6	nF1_E_XMIT0
MGTYRXP1_229	Y4	pF1_E_RECV1
MGTYRXN1_229	Y3	nF1_E_RECV1
MGTYTXP1_229	Y9	pF1_E_XMIT1
MGTYTXN1_229	Y8	nF1_E_XMIT1
MGTYRXP2_229	W2	pF1_E_RECV2
MGTYRXN2_229	W1	nF1_E_RECV2
MGTYTXP2_229	W7	pF1_E_XMIT2
MGTYTXN2_229	W6	nF1_E_XMIT2
MGTYRXP3_229	V4	pF1_E_RECV3
MGTYRXN3_229	V3	nF1_E_RECV3
MGTYTXP3_229	V9	pF1_E_XMIT3
MGTYTXN3_229	V8	nF1_E_XMIT3

FPGA_VU13P_A2577

U75-49 — GTY QUAD 230 F

MGTREFCLK0P_230	W11	ac_pF1R_R0_F 20
MGTREFCLK0N_230	W10	ac_nF1R_R0_F 20
MGTREFCLK1P_230	V13	
MGTREFCLK1N_230	V12	
MGTYRXP0_230	U2	pF1_F_RECV0
MGTYRXN0_230	U1	nF1_F_RECV0
MGTYTXP0_230	U7	pF1_F_XMIT0
MGTYTXN0_230	U6	nF1_F_XMIT0
MGTYRXP1_230	T4	pF1_F_RECV1
MGTYRXN1_230	T3	nF1_F_RECV1
MGTYTXP1_230	T9	pF1_F_XMIT1
MGTYTXN1_230	T8	nF1_F_XMIT1
MGTYRXP2_230	R2	pF1_F_RECV2
MGTYRXN2_230	R1	nF1_F_RECV2
MGTYTXP2_230	R7	pF1_F_XMIT2
MGTYTXN2_230	R6	nF1_F_XMIT2
MGTYRXP3_230	P4	pF1_F_RECV3
MGTYRXN3_230	P3	nF1_F_RECV3
MGTYTXP3_230	P9	pF1_F_XMIT3
MGTYTXN3_230	P8	nF1_F_XMIT3

FPGA_VU13P_A2577

pF1_D_RECV0	nF1_D_RECV0	C164 0.1 UF 0402	pF2_C_XMIT0 nF2_C_XMIT0
pF1_D_RECV1	nF1_D_RECV1	C162 0.1 UF 0402	pF2_C_XMIT1 nF2_C_XMIT1
pF1_D_RECV2	nF1_D_RECV2	C160 0.1 UF 0402	pF2_C_XMIT2 nF2_C_XMIT2
pF1_D_RECV3	nF1_D_RECV3	C158 0.1 UF 0402	pF2_C_XMIT3 nF2_C_XMIT3
		C163 0.1 UF 0402	
		C161 0.1 UF 0402	
		C159 0.1 UF 0402	
		C157 0.1 UF 0402	

pF1_D_XMIT0	nF1_D_XMIT0	0402 0.1 UF C172	pF2_C_RECV0 nF2_C_RECV0
pF1_D_XMIT1	nF1_D_XMIT1	0402 0.1 UF C170	pF2_C_RECV1 nF2_C_RECV1
pF1_D_XMIT2	nF1_D_XMIT2	0402 0.1 UF C168	pF2_C_RECV2 nF2_C_RECV2
pF1_D_XMIT3	nF1_D_XMIT3	0402 0.1 UF C166	pF2_C_RECV3 nF2_C_RECV3
		0402 0.1 UF C171	
		0402 0.1 UF C169	
		0402 0.1 UF C167	
		0402 0.1 UF C165	

U77-46 — GTY QUAD 227 C

AJ11	MGTREFCLK0P_227	
AJ10	MGTREFCLK0N_227	
AG11	MGTREFCLK1P_227	
AG10	MGTREFCLK1N_227	
pF2_C_RECV3	AJ2	MGTYRXP0_227
nF2_C_RECV3	AJ1	MGTYRXN0_227
pF2_C_XMIT3	AJ7	MGTYTXP0_227
nF2_C_XMIT3	AJ6	MGTYTXN0_227
pF2_C_RECV2	AH4	MGTYRXP1_227
nF2_C_RECV2	AH3	MGTYRXN1_227
pF2_C_XMIT2	AH9	MGTYTXP1_227
nF2_C_XMIT2	AH8	MGTYTXN1_227
pF2_C_RECV1	AG2	MGTYRXP2_227
nF2_C_RECV1	AG1	MGTYRXN2_227
pF2_C_XMIT1	AG7	MGTYTXP2_227
nF2_C_XMIT1	AG6	MGTYTXN2_227
pF2_C_RECV0	AF4	MGTYRXP3_227
nF2_C_RECV0	AF3	MGTYRXN3_227
pF2_C_XMIT0	AF9	MGTYTXP3_227
nF2_C_XMIT0	AF8	MGTYTXN3_227

FPGA_VU13P_A2577

U77-45 — GTY QUAD 226 B

ac_pF2R_R0_B 20	AM13	MGTREFCLK0P_226
ac_nF2R_R0_B 20	AM12	MGTREFCLK0N_226
ac_pF2R_R1_B 23	AL11	MGTREFCLK1P_226
ac_nF2R_R1_B 23	AL10	MGTREFCLK1N_226
pF2_B_RECV3	AN2	MGTYRXP0_226
nF2_B_RECV3	AN1	MGTYRXN0_226
pF2_B_XMIT3	AN7	MGTYTXP0_226
nF2_B_XMIT3	AN6	MGTYTXN0_226
pF2_B_RECV2	AM4	MGTYRXP1_226
nF2_B_RECV2	AM3	MGTYRXN1_226
pF2_B_XMIT2	AM9	MGTYTXP1_226
nF2_B_XMIT2	AM8	MGTYTXN1_226
pF2_B_RECV1	AL2	MGTYRXP2_226
nF2_B_RECV1	AL1	MGTYRXN2_226
pF2_B_XMIT1	AL7	MGTYTXP2_226
nF2_B_XMIT1	AL6	MGTYTXN2_226
pF2_B_RECV0	AK4	MGTYRXP3_226
nF2_B_RECV0	AK3	MGTYRXN3_226
pF2_B_XMIT0	AK9	MGTYTXP3_226
nF2_B_XMIT0	AK8	MGTYTXN3_226

FPGA_VU13P_A2577

pF1_E_RECV0	nF1_E_RECV0	C145 0.1 UF 0402	pF2_B_XMIT0 nF2_B_XMIT0
pF1_E_RECV1	nF1_E_RECV1	C143 0.1 UF 0402	pF2_B_XMIT1 nF2_B_XMIT1
pF1_E_RECV2	nF1_E_RECV2	C141 0.1 UF 0402	pF2_B_XMIT2 nF2_B_XMIT2
pF1_E_RECV3	nF1_E_RECV3	C139 0.1 UF 0402	pF2_B_XMIT3 nF2_B_XMIT3
		C144 0.1 UF 0402	
		C142 0.1 UF 0402	
		C140 0.1 UF 0402	
		C138 0.1 UF 0402	

pF1_E_XMIT0	nF1_E_XMIT0	0402 0.1 UF C153	pF2_B_RECV0 nF2_B_RECV0
pF1_E_XMIT1	nF1_E_XMIT1	0402 0.1 UF C151	pF2_B_RECV1 nF2_B_RECV1
pF1_E_XMIT2	nF1_E_XMIT2	0402 0.1 UF C149	pF2_B_RECV2 nF2_B_RECV2
pF1_E_XMIT3	nF1_E_XMIT3	0402 0.1 UF C147	pF2_B_RECV3 nF2_B_RECV3
		0402 0.1 UF C152	
		0402 0.1 UF C150	
		0402 0.1 UF C148	
		0402 0.1 UF C146	

U77-44 — GTY QUAD 225 A

AP13	MGTREFCLK0P_225	
AP12	MGTREFCLK0N_225	
AN11	MGTREFCLK1P_225	
AN10	MGTREFCLK1N_225	
pF2_A_RECV3	AU2	MGTYRXP0_225
nF2_A_RECV3	AU1	MGTYRXN0_225
pF2_A_XMIT3	AU7	MGTYTXP0_225
nF2_A_XMIT3	AU6	MGTYTXN0_225
pF2_A_RECV2	AT4	MGTYRXP1_225
nF2_A_RECV2	AT3	MGTYRXN1_225
pF2_A_XMIT2	AT9	MGTYTXP1_225
nF2_A_XMIT2	AT8	MGTYTXN1_225
pF2_A_RECV1	AR2	MGTYRXP2_225
nF2_A_RECV1	AR1	MGTYRXN2_225
pF2_A_XMIT1	AR7	MGTYTXP2_225
nF2_A_XMIT1	AR6	MGTYTXN2_225
pF2_A_RECV0	AP4	MGTYRXP3_225
nF2_A_RECV0	AP3	MGTYRXN3_225
pF2_A_XMIT0	AP9	MGTYTXP3_225
nF2_A_XMIT0	AP8	MGTYTXN3_225

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pF1_F_RECV0	nF1_F_RECV0	C125 0.1 UF 0402	pF2_A_XMIT0 nF2_A_XMIT0
pF1_F_RECV1	nF1_F_RECV1	C123 0.1 UF 0402	pF2_A_XMIT1 nF2_A_XMIT1
pF1_F_RECV2	nF1_F_RECV2	C121 0.1 UF 0402	pF2_A_XMIT2 nF2_A_XMIT2
pF1_F_RECV3	nF1_F_RECV3	C119 0.1 UF 0402	pF2_A_XMIT3 nF2_A_XMIT3
		C124 0.1 UF 0402	
		C122 0.1 UF 0402	
		C120 0.1 UF 0402	
		C118 0.1 UF 0402	

pF1_F_XMIT0	nF1_F_XMIT0	0402 0.1 UF C133	pF2_A_RECV0 nF2_A_RECV0
pF1_F_XMIT1	nF1_F_XMIT1	0402 0.1 UF C131	pF2_A_RECV1 nF2_A_RECV1
pF1_F_XMIT2	nF1_F_XMIT2	0402 0.1 UF C129	pF2_A_RECV2 nF2_A_RECV2
pF1_F_XMIT3	nF1_F_XMIT3	0402 0.1 UF C127	pF2_A_RECV3 nF2_A_RECV3
		0402 0.1 UF C132	
		0402 0.1 UF C130	
		0402 0.1 UF C128	
		0402 0.1 UF C126	

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9.05: F1 QUAD G TO F2 QUAD P

FPGA#1

U75-50

GTY QUAD 231 G

MGTREFCLK0P_231	U11	ac_pF1R_R0_G 20
MGTREFCLK0N_231	U10	ac_nF1R_R0_G 20
MGTREFCLK1P_231	T13	ac_pF1R_R1_G 23
MGTREFCLK1N_231	T12	ac_nF1R_R1_G 23
MGTYRXP0_231	N2	pF1_G_RECV0
MGTYRXN0_231	N1	nF1_G_RECV0
MGTYTXP0_231	N7	pF1_G_XMIT0
MGTYTXN0_231	N6	nF1_G_XMIT0
MGTYRXP1_231	M4	pF1_G_RECV1
MGTYRXN1_231	M3	nF1_G_RECV1
MGTYTXP1_231	M9	pF1_G_XMIT1
MGTYTXN1_231	M8	nF1_G_XMIT1
MGTYRXP2_231	L2	pF1_G_RECV2
MGTYRXN2_231	L1	nF1_G_RECV2
MGTYTXP2_231	L7	pF1_G_XMIT2
MGTYTXN2_231	L6	nF1_G_XMIT2
MGTYRXP3_231	K4	pF1_G_RECV3
MGTYRXN3_231	K3	nF1_G_RECV3
MGTYTXP3_231	K9	pF1_G_XMIT3
MGTYTXN3_231	K8	nF1_G_XMIT3

FPGA_VU13P_A2577

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

REPLACE THE COUPLING CAPACITORS WITH ZERO-OHM RESISTORS ON BOARDS WHERE FPGA#2 IS REPLACED BY A JUMPER BOARD.

pF1_G_RECV0	nF1_G_RECV0	C106 0.1 UF 0402	pF2_P_XMIT0 nF2_P_XMIT0
pF1_G_RECV1	nF1_G_RECV1	C104 0.1 UF 0402	pF2_P_XMIT1 nF2_P_XMIT1
pF1_G_RECV2	nF1_G_RECV2	C102 0.1 UF 0402	pF2_P_XMIT2 nF2_P_XMIT2
pF1_G_RECV3	nF1_G_RECV3	C100 0.1 UF 0402	pF2_P_XMIT3 nF2_P_XMIT3
		C105 0.1 UF 0402	
		C103 0.1 UF 0402	
		C101 0.1 UF 0402	
		C99 0.1 UF 0402	

pF1_G_XMIT0	nF1_G_XMIT0	0402 0.1 UF C114	pF2_P_RECV0 nF2_P_RECV0
pF1_G_XMIT1	nF1_G_XMIT1	0402 0.1 UF C112	pF2_P_RECV1 nF2_P_RECV1
pF1_G_XMIT2	nF1_G_XMIT2	0402 0.1 UF C110	pF2_P_RECV2 nF2_P_RECV2
pF1_G_XMIT3	nF1_G_XMIT3	0402 0.1 UF C108	pF2_P_RECV3 nF2_P_RECV3
		0402 0.1 UF C113	
		0402 0.1 UF C111	
		0402 0.1 UF C109	
		0402 0.1 UF C107	

FPGA#2

U77-43

GTY QUAD 224 P

ac_pF2R_R0_P 20	AT13	MGTREFCLK0P_224
ac_nF2R_R0_P 20	AT12	MGTREFCLK0N_224
ac_pF2R_R1_P 23	AR11	MGTREFCLK1P_224
ac_nF2R_R1_P 23	AR10	MGTREFCLK1N_224
pF2_P_RECV3	BA2	MGTYRXP0_224
nF2_P_RECV3	BA1	MGTYRXN0_224
pF2_P_XMIT3	BA7	MGTYTXP0_224
nF2_P_XMIT3	BA6	MGTYTXN0_224
pF2_P_RECV2	AY4	MGTYRXP1_224
nF2_P_RECV2	AY3	MGTYRXN1_224
pF2_P_XMIT2	AY9	MGTYTXP1_224
nF2_P_XMIT2	AY8	MGTYTXN1_224
pF2_P_RECV1	AW2	MGTYRXP2_224
nF2_P_RECV1	AW1	MGTYRXN2_224
pF2_P_XMIT1	AW7	MGTYTXP2_224
nF2_P_XMIT1	AW6	MGTYTXN2_224
pF2_P_RECV0	AV4	MGTYRXP3_224
nF2_P_RECV0	AV3	MGTYRXN3_224
pF2_P_XMIT0	AV9	MGTYTXP3_224
nF2_P_XMIT0	AV8	MGTYTXN3_224

FPGA_VU13P_A2577

APOLLO CM W/ DUAL A2577, MK1

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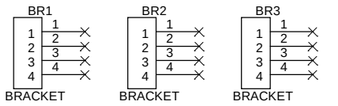
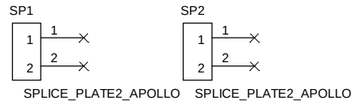
THESE SHAPES DEFINE MECHANICAL OBJECTS
THAT SHOULD BE IN THE BILL OF MATERIALS.

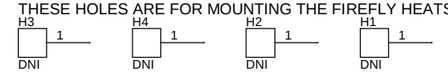


BRACKETS FOR SUPPORTING
A SUB-FRONT PANEL

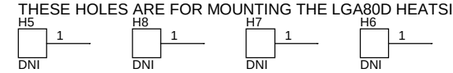
THESE SHAPES DEFINE HOLES AND KEEPOUT
AREAS FOR THE SPLICE PLATES.



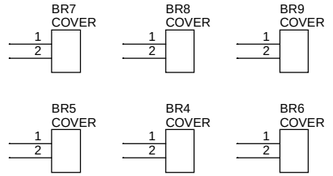
THESE HOLES ARE FOR MOUNTING THE FIREFLY HEATSINK



THESE HOLES ARE FOR MOUNTING THE LGA80D HEATSINK



THESE BRACKETS ARE FOR MOUNTING THE COVERS.
THE BRACKETS ATTACH ON THE BOTTOM SIDE OF
THE BOARD.



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