6089-119 Rev B Checkout

Status

S/N 201 (RevA)
- Installed single VU13P-1
- Modified FPGA site to fix JTAG wiring screwup
- Sent to BU with one 25Gx4 and one 14Gx12 CERN FireFly

S/N 202 (RevA)
- No FPGA
- Used for MCU development in PSB lab
- FireFly??

S/N 203
- Installed dual VU13P-1
- TCDS jumpers “MIDDLE”
- Full FireFly load – 8 25Gx4 and 6 14G x12 CERN
- Mated to SM10 in ATCA shelf

S/N 204
- Installed single VU13P-2
- TCDS jumpers “UP”
- Testing 25Gx12 FireFly
- 2 25Gx4 FireFly with pin-fin heatsinks
- Standalone in PSB lab

Problems

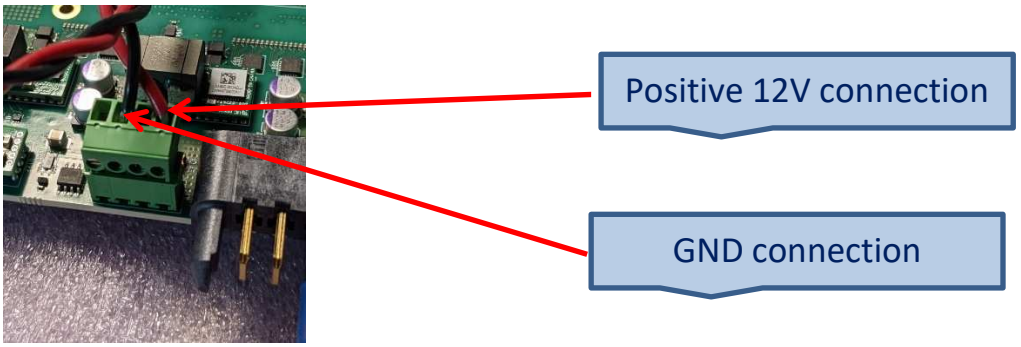
1) The 6-pin surface-mount header for the MCU console serial cable does not have any mechanical attachment points. Any force rips the pads off the board.
    a. Use a connector plugged into the low-speed SM connector to access the serial console.
    b. Instruct MPL to omit this connector on future builds
    c. Design and build a testing board that uses the three SM connectors.

Check polarized capacitors

1) Visually verify the orientation of the 14 120uf capacitors, in round aluminum cans, on the top side of the board. The blue mark indicates the negative terminal. Looking at the board with the P1 connector pointing at you, the 4 pairs of capacitors on the right side of the board should have the blue mark pointing to the left. The 3 pairs of capacitors on the left side of the board should have the blue marks pointing away from each other.
2) Visually verify the orientation of the 28 220uf or 330 uf capacitors on the top side of the board. Four are adjacent to each of the 7 large LGA80D voltage regulators. The gray bars indicate the positive terminal. The bar should be near the "+" symbol on the silkscreen.
3) Visually verify the orientation of the 28 220uf or 330 uf capacitors on the bottom side of the board, opposite the capacitors from step 2 above. The gray bars indicate the positive terminal. The bar should be near the "+" symbol on the silkscreen.
4) Visually verify the value of the 8 220uf capacitors connected to the LGA80D regulator in the middle of the row, U108. Look at 4 on the top side and 4 on the bottom side of the board. Use a microscope to examine them. They should have "227" written on them. These are 220 uf 6.3 volts capacitors. If they have "337" written on them, then they are the wrong value for this location, because they are 330 uf 2.5 volt capacitors and the voltage rating is insufficient.

Connect and Check 12v Input

1) Connect a variable voltage source to J10, the green on-board power connector. Verify that the positive lead is closest to the black P1 connector.

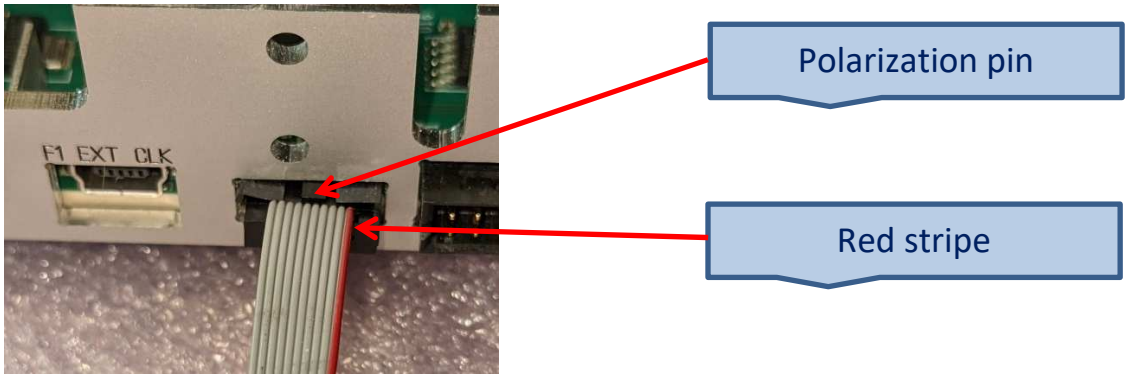


2) Connect a voltmeter to the "12V" and "GND" test points. Connect an ammeter in series with the 12 volt source.
3) Set the power supply to zero volts. Turn it on, then raise the voltage slightly to about 0.5 volts. Verify that the "12V" test point is positive with respect to the "GND" test point.
4) Move the voltmeter to the "M3V3" test point.
5) Gradually increase the voltage to 12 volts. The 3.3 volt level should appear when the input is slightly higher than 6.5 volts. Stop at 12 volts and measure the input current and the "M3V3" voltage. The current should be around 0.4 to 0.5 amps, and the M3V3 voltage should be around 3.3 volts.

Connect Segger MCU JTAG Adapter

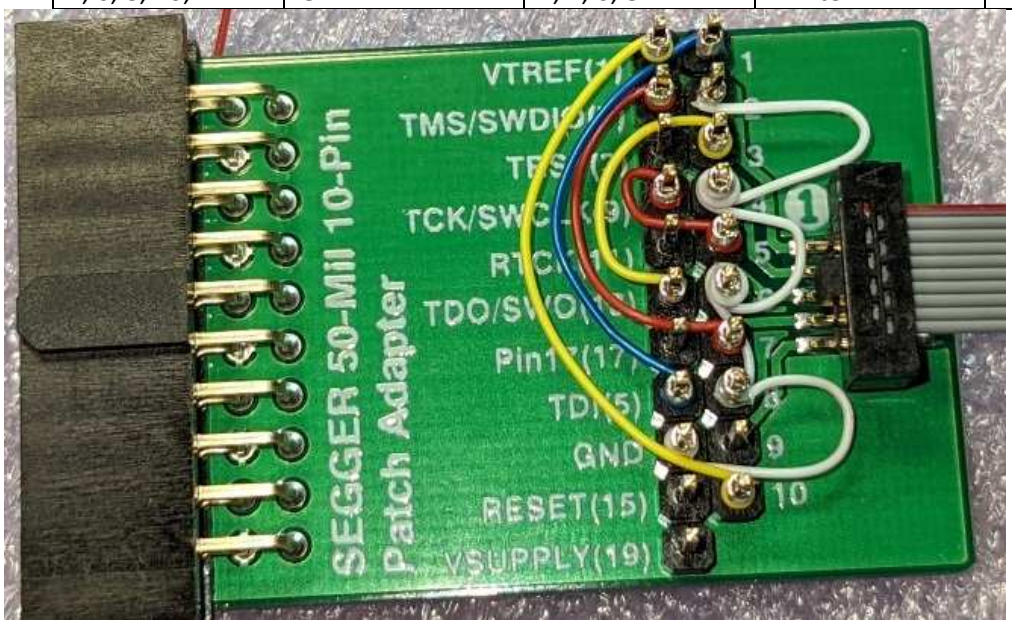
1) Turn off the DC power.

2) Plug the cable for the Segger adapter into the front panel MCU JTAG connector. The polarization pin and the red stripe should be as shown below.



3) Connect the other end of the cable to a Segger adapter that is wired according to the following table and the photo as shown below. The names in the "Segger 20-pin header name" column are printed on the left side of the adapter. The numbers in the "Adapter 10-pin cable number" column are printed on the right side of the adapter.

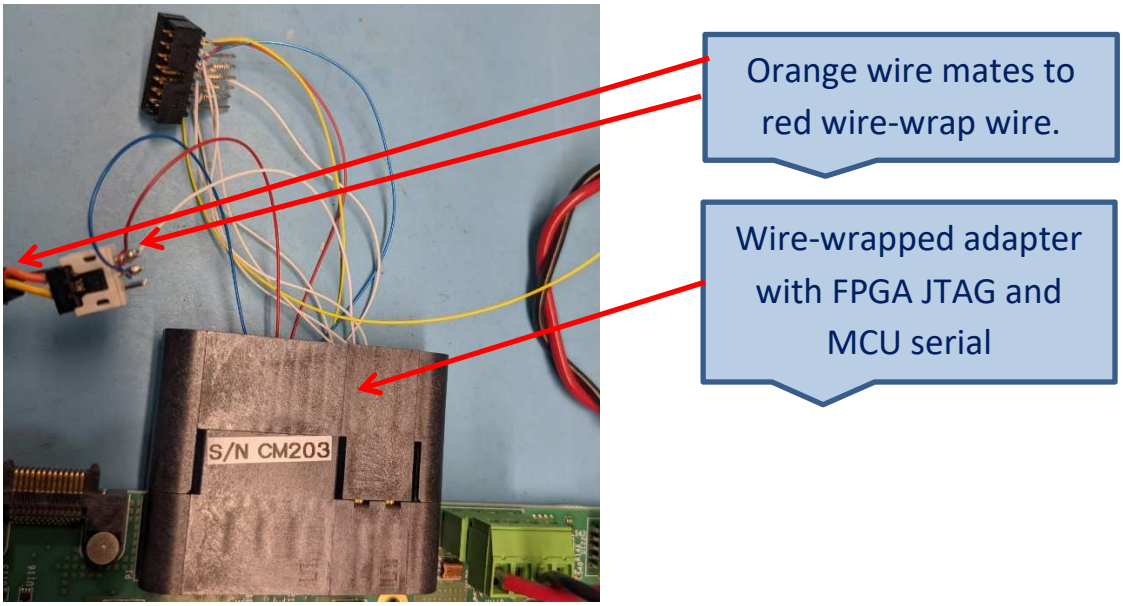
Segger 20-pin header number	Segger 20-pin header name	Adapter 10-pin cable number	Color	
1	VTREF (1)	10	Yellow	
5	TDI (5)	1	Blue	
7	TMS/SWDIO (7)	7	Red	
9	TCK/SWCLK (9)	5	Red	
13	TDO/SWO (13)	3	Yellow	
4, 6, 8, 10, 12	GND	2, 4, 6, 8	White	



Connect MCU Serial Cable

1) The MCU serial cable should only be connected to the low-speed SM connector. Do not use any on-board connectors that may be present. A formal testing board will be designed. Until that is available, just use the wire-wrapped adapter cable. It also provides a JTAG connection to the FPGAs.

2) To use the MCU serial cable, connect it in the orientation shown in the photo below.



Prepare MCU programs

1) Setup the compiler environment on LNX750 with the following commands:

```
cd /home/crs/apollo/mcu
source setup_mcu.sh
```

The file "setup_mcu.sh" contains:

```
export PATH=/home/wittich/Downloads/gcc-arm-none-eabi-9-2019-q4-major/bin:${PATH}
export FREERTOS_ROOT=/home/wittich/src/FreeRTOSv10.2.1/FreeRTOS/Source
```

2) Download the repo that contains both the bootloader and the application:

```
git clone git@github.com:apollo-lhc/cm_mcu.git
```

3) Change to the bootloader project and compile the code with the "REV2=1" flag:

```
cd /home/crs/apollo/mcu/cm_mcu/projects/boot_loader
make -k REV2=1 DEBUG=1
```

4) Change to the application project and compile the code, again with the "REV2=1" flag:

```
cd /home/crs/apollo/mcu/cm_mcu/projects/cm_mcu
make -k REV2=1 DEBUG=1
```

Program the MCU

1) Turn on the 12V DC power.

2) Change to the bootloader project "gcc" directory and download the code to the board:

```
cd /home/crs/apollo/mcu/cm_mcu/projects/boot_loader/gcc
JLinkExe -commandfile /home/wittich/jlinkloadbl.cmd
```

3) Change to the application project "gcc" directory and download the code to the board:

```
cd /home/crs/apollo/mcu/cm_mcu/projects/cm_mcu/gcc
JLinkExe -commandfile /home/wittich/jlinkload.cmd
```

4) After programming, the green MCU_ENABLED and PWR_OK leds should be lit. The current on the 12V input should be around 1.8 to 2.0 amps.

5) Connect a voltmeter to the "12V" testpoint on the board. Adjust the DC power supply until the voltage at the test point is 12.0 volts. Make the voltage and current measurements to fill in the following table:

	S/N 203	S/N 204	
12V test point		12.0 V	
12V on DC power supply		12.19 V	
12V Current (from ammeter)		1.85 A	
I_12v test point		0.184 V	
Calculated 12V current @10 amps per volt		1.84 A	
Voltage @ M3V3		3.32 V	
I_M3V3 test point		0.042 V	
Calculated M3V3 current @ 2 amps per volt		0.084 A	
1V8 test point		1.796 V	
3V3 test point		3.304 V	
4V0 test point		3.979	
test point			
test point			
test point			
test point			
test point			
test point			

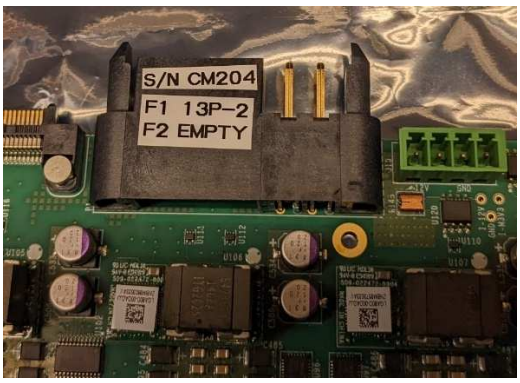
test point			
test point			
test point			
test point			

NOTE: The 12V voltage is divided by 6 before the MCU
NOTE: The M3V3 voltage is divided by 2 before the MCU

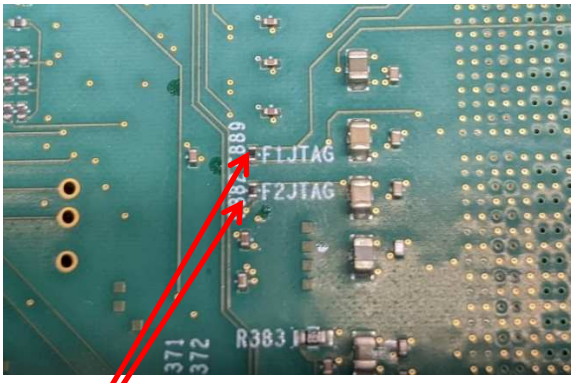
Install FPGAs, Configure JTAG jumpers, and Verify the JTAG chain

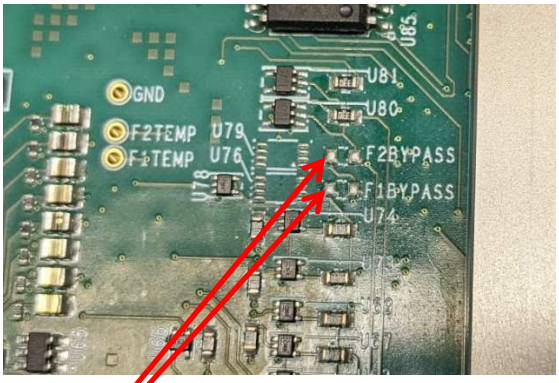
1) At this point, the MCU can be programmed and the power supplies are functioning. Send the board back to the assembler, along with the appropriate FPGAs.

2) The FPGAs do not have a human-readable indication of the speed grade. Add labels indicating the FPGA type and the speed grade that is installed in each site. The FPGA type will either be “9P”, “13P”, or “EMPTY”. The speed grade will either be “-1” or “-2”.



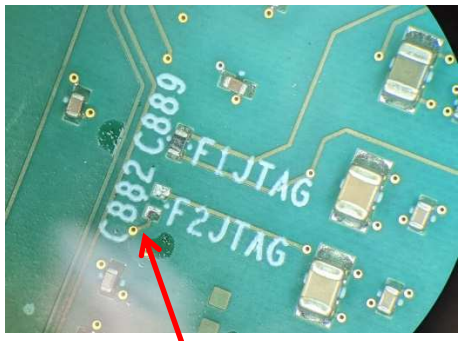
3) The boards were initially assembled with both JTAG “IN CHAIN” jumpers (C889 and C882) installed, and both “BYPASS” jumpers (R131 and R134) omitted. If two FPGAs are installed, nothing more needs to be done. If only FPGA#1 was installed (U75), then the 0402 “IN CHAIN” jumper for FPGA#2 (C882) needs to be removed, and an 0603 “BYPASS” jumper (R134) needs to be installed.

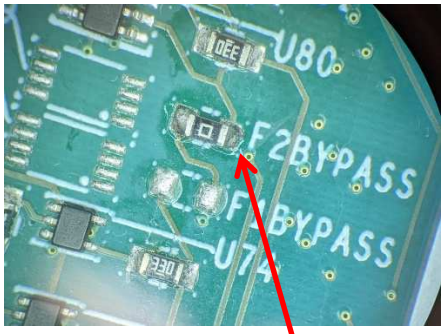




Both “IN_CHAIN” jumpers installed for 2-FPGA board

Both “BYPASS” jumpers omitted for 2-FPGA board





"IN_CHAIN" jumper for FPGA#2 removed for single-FPGA board

"BYPASS" jumper for FPGA#2 installed for single-FPGA board

4) Re-connect the 12V power cable and the MCU serial cable. Connect the Xilinx JTAG programmer to the front panel connector. Turn on the 12V power. On the MCU console, enter the command:

```
jtag_sm off
```

5) Start the Vivado hardware manager and connect to the board. Vivado should detect the number of FPGAs that are connected. Connect to the "SysMon" core and display a dashboard that shows the FPGA's temperature.

Configure TCSD jumpers

The boards are initially assembled with no TCDS jumpers. Four 0402 zero-ohm jumpers need to be added to control the signal flow from/to the second high-speed connector (P3) on the SM. Two are for routing the signal coming from P3 through J8 and two are for routing the signal going back to P3 through J9. The orientation of the jumpers as “UP”, “MIDDLE”, or “DOWN” matches the picture of the jumper blocks on schematic sheet 2.13 “FPGA#1 AND FPGA#2 TCBS QUADS AB”.

FPGA#1 can either be a TCDS-endpoint or a TCDS-slave of the Zynq on the SM.
FPGA#2 can either be a TCDS-slave of FPGA#1 or a TCDS-slave of the Zynq on the SM.
The TCDS functionality can either be implemented in dedicated GTY quads or in a quad that is shared with the C2C links from the SM.

There are enough permutations that confusion is guaranteed. Following are the resultant signal paths of the various jumper settings:

1) NO JUMPERS: TCDS signals on the first high-speed connector (P2) connect to FPGA#1 quad AB (VU13P GTY quad 120) port “zero”. This quad is dedicated to TCDS operations. This connection will always exist.

   The FPGA#2 site will not have any direct TCDS connections to the SM.

   This is the choice for a single-FPGA production board that will use a dedicated quad for TCDS operations. Depending on how the SM is configured, FPGA#1 can be the TCDS endpoint, or it can be a TCDS-slave of the Zynq.

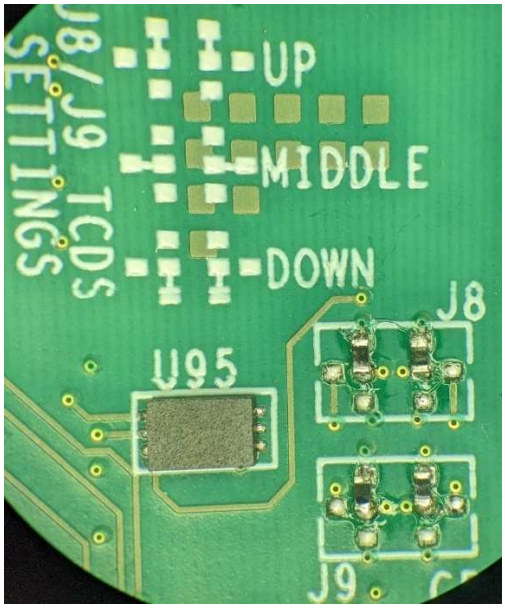
   It also works for the case where FPGA#1 is the TCDS-endpoint and FPGA#2 is a TCDS-slave of FPGA#1. TCDS signals will pass between the two FPGAs using port “three” of quad AB (VU13P GTY quad 120).

2) JUMPERS “UP”: TCDS signals on the second high-speed connector (P3) connect to FPGA#1 quad AB (VU13P quad 120) port “two”. This quad is dedicated to TCDS operations.

   This is identical in every way to the NO JUMPER case except that the connection to the SM is on the second high-speed connector and the connection is made to port “two” of the GTY quad.

   This connection can be useful for comparing the operation and signal quality of a direct connection to the SM vs. one that passes through jumpers and a variety of longer traces.

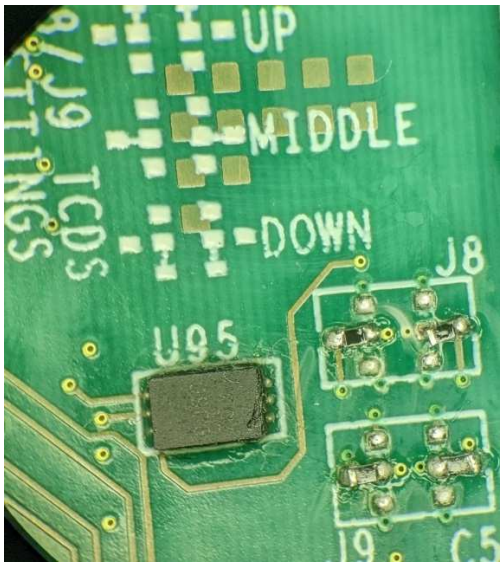
   CM-204 (single VU13P-2) is connected and labeled this way



3) JUMPERS “MIDDLE”: TCDS signals on the second high-speed connector (P3) connect to FPGA#2 quad AB (VU13P quad 120) port “zero”. This quad is dedicated to TCDS operations.

   This is the only configuration that gives FPGA#2 a direct connection to the SM.
   This connection is most appropriate for the case where both FPGAs are TCDS-slaves of the Zynq on the SM. Both FPGAs will be connected identically to their respective high-speed connector. However, it will still support operating FPGA#1 as the TCDS-endpoint and FPGA#2 as a TCDS-slave.

   CM-203 (dual VU13P-1) is connected and labeled this way

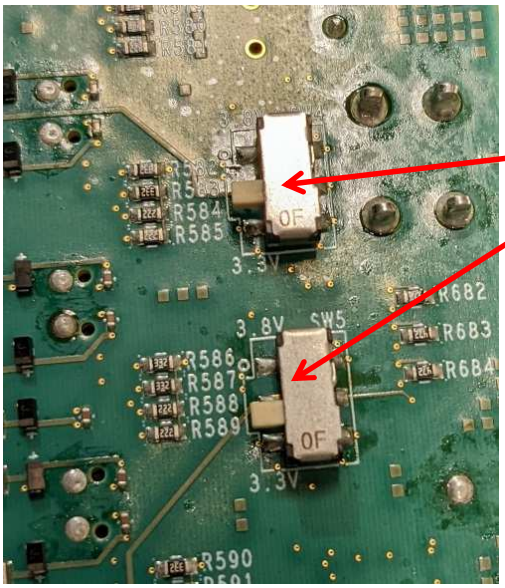


4) JUMPERS “DOWN”: TCDS signals on the second high-speed connector (P3) connect to FPGA#1 quad L (VU13P quad 220) port “two”. This quad is shared with C2C operations.

   This connection is useful for testing TCDS operation in a quad that is also used for something else. There is no connection available between the SM and FPGA#2.

Set FireFly voltage switches

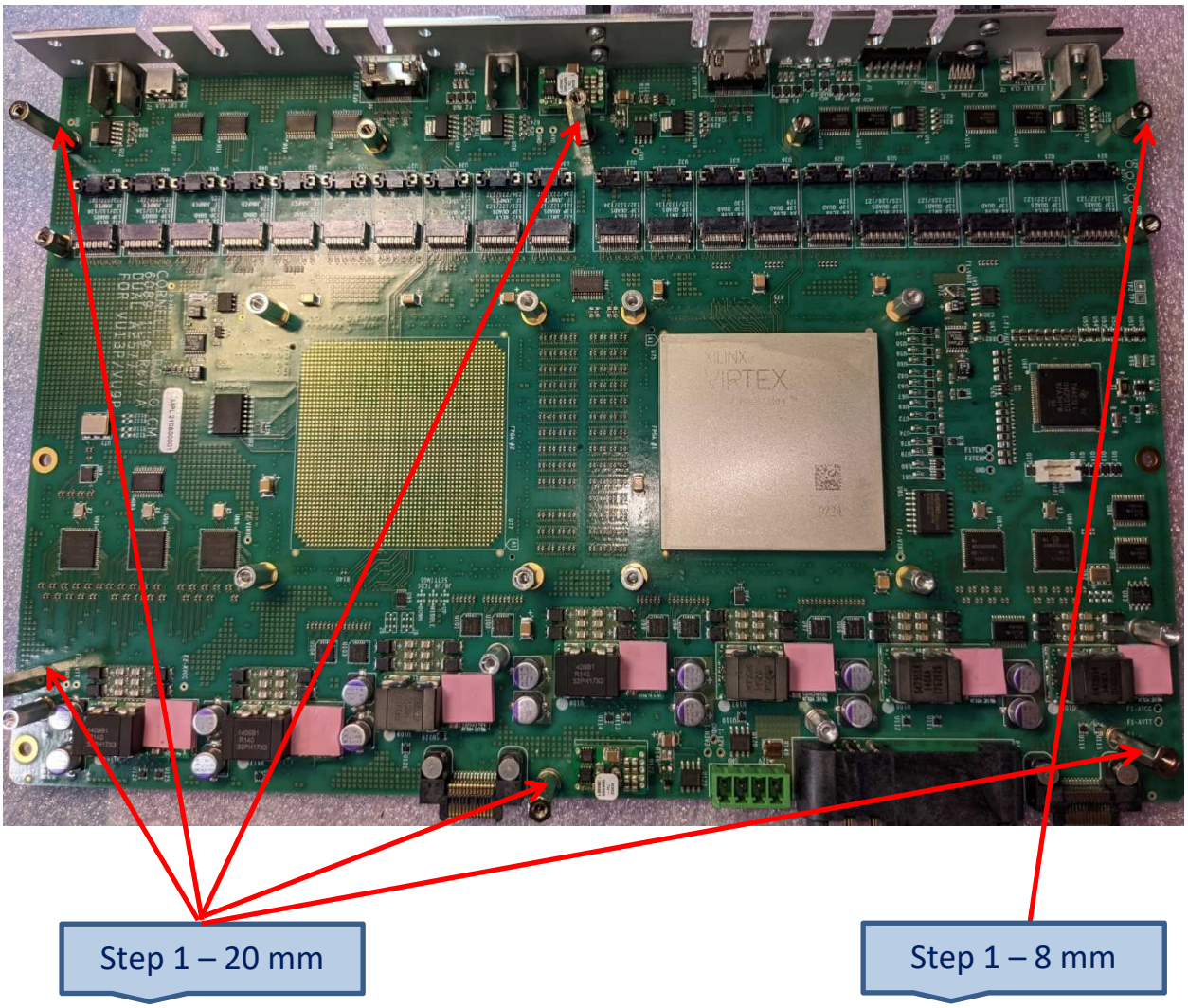
Set all FireFly voltage selection switches to the “3.3V” position. This will help avoid damage to devices that don’t use 3.8 volts on the transmitters.



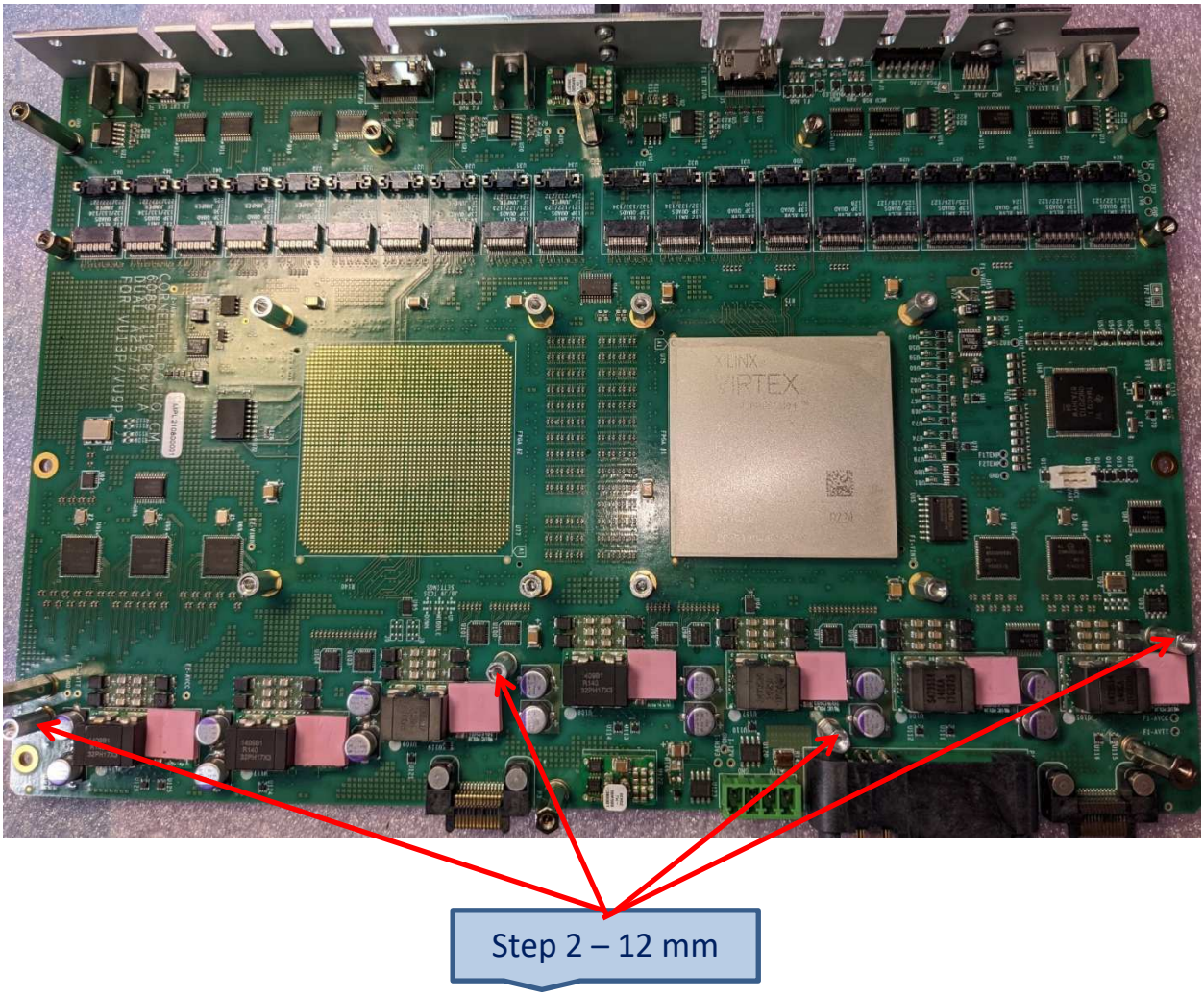
Selector switches in the “3.3V” (OFF) position.
(2 of 6 places shown)

Add standoffs and spacers

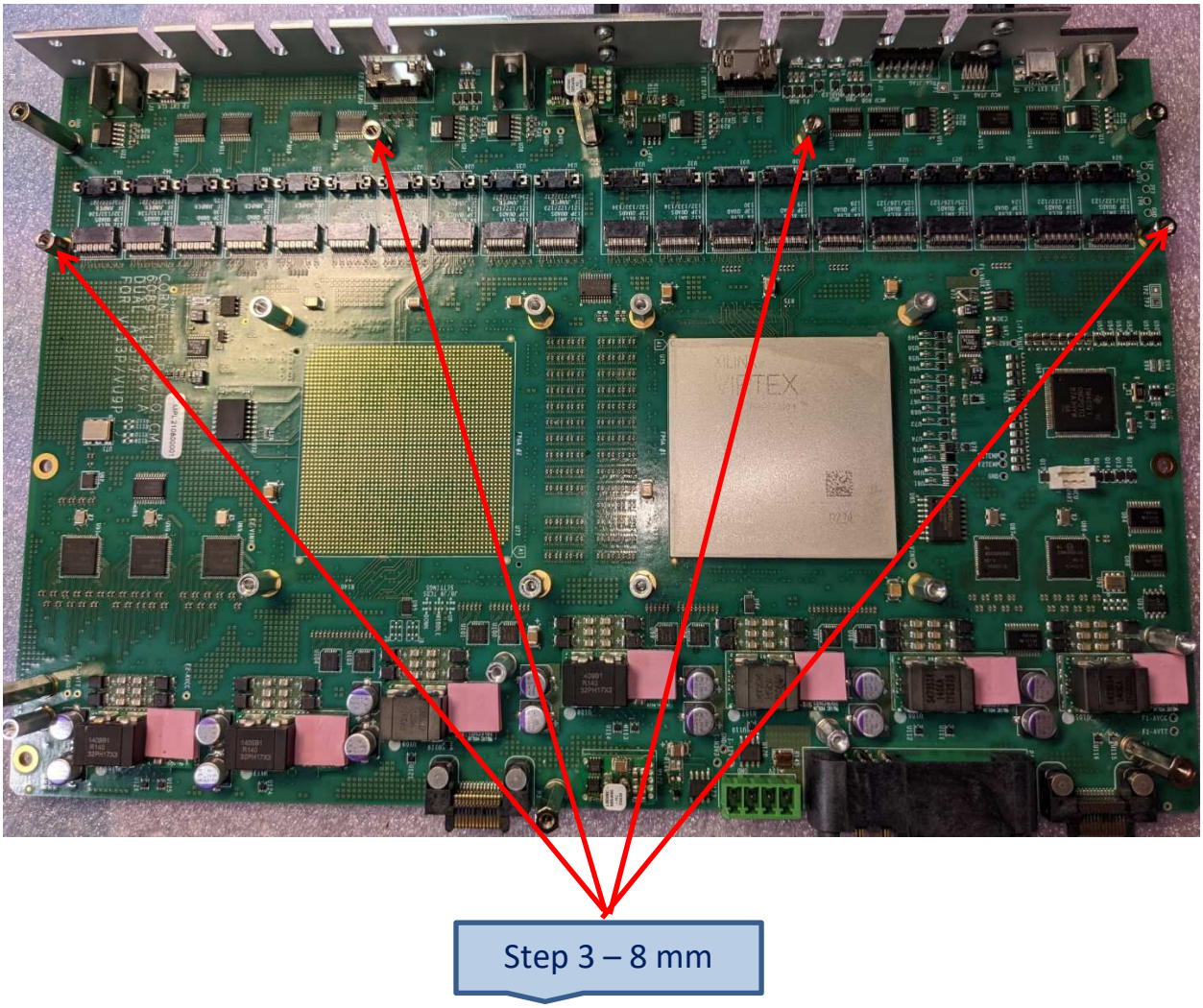
1) Install 6 bottom cover mounting blocks and top cover standoffs
    a. The covers are 1/32" (0.8 mm) thick. The ATCA spec has a maximum cover height of 22.74 mm. Therefore, the top of the mounted standoff must be less than 21.94 mm above the board. Check this measurement after installing the cover standoffs in case the washers are thicker than expected.
    b. From the bottom side of the board, insert an M2.5x8 screw thru a cover block.
    c. From the top side of the board, insert a temporary M2.5 screw through the non-plated hole in the board and into the cover block. This is a temporary screw that will prevent the cover block from rotating while the standoff is tightened.
    d. From the top side of the board, drop two M2.5 flat washers and one M2.5 lock washer on the screw.
    e. Add an M2.5 x 20 mm standoff in 5 of the 6 places. Use an M2.5 x 8 mm standoff as a nut in the corner where the SM's front panel board will be located (near R27). This corner of the cover does not get screwed down due to the front panel board.
    f. Tighten the screw and standoff. Assure that the cover block remains square within the silkscreen outline on the bottom side of the board. Remove the temporary screw.


Step 1 – 20 mm
Step 1 – 8 mm

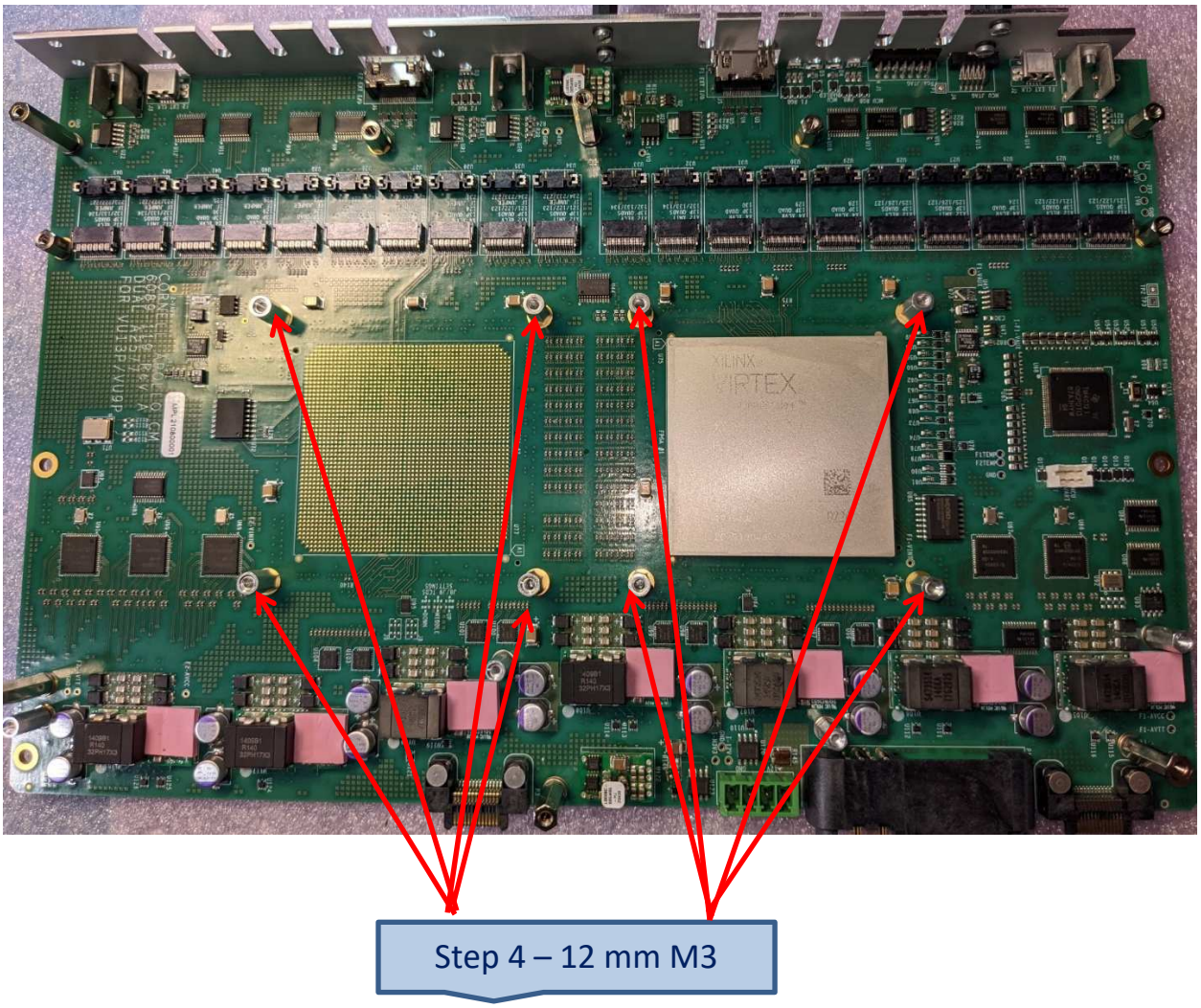
2) Install four standoffs for the LGA80D heatsink
    a. The thermal pad for the LGA80D regulators is Laird Tflex HD300 (DigiKey P/N 926-1594). The uncompressed thickness is 0.07” (1.778 mm).
    b. The mounted height of a 12-mm standoff, a lockwasher, and a flat washer is between 13 mm and 13.1 mm. When a heatsink without any thermal pad is attached, the gap between the heatsink and the inductor is 1.25 mm, and between the heatsink and the chip on the regulator 1.47 mm. The pad is compressed by 30% over the inductor and 17% over the chip.
    c. From the bottom side of the board, insert an M2.5x6 screw into an LGA80D heatsink mounting hole.
    d. From the top side of the board, drop one M2.5 flat washer and one M2.5 lock washer on the screw.
    e. Add an M2.5 x 12 mm standoff.
    f. Tighten the screw and standoff.
    g. If they are in place, remove the white label from each LGA80D.



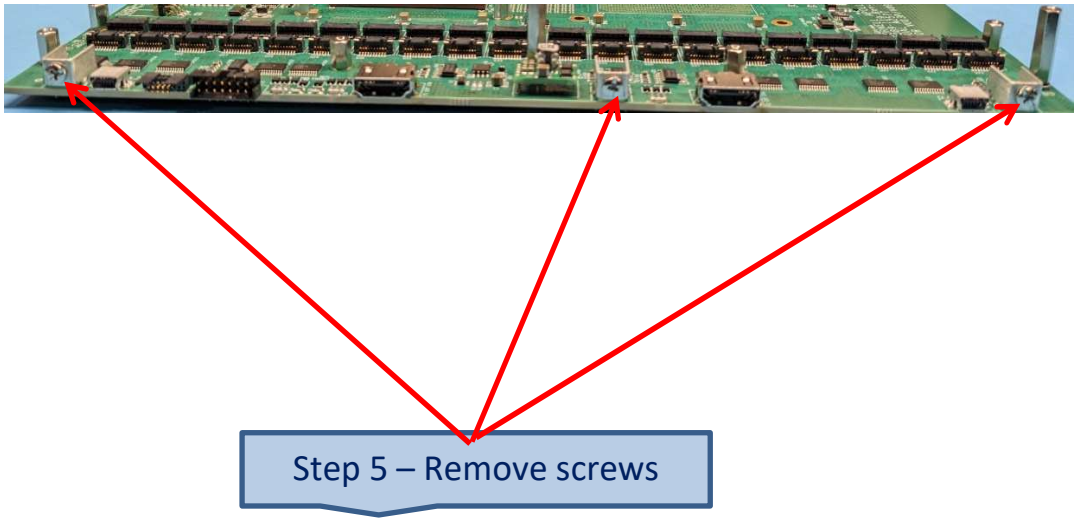
3) Install four standoffs for the FireFly heatsink
    a. From the bottom side of the board, insert an M2.5x6 screw plus an M2.5 lockwasher and an M2.5 flatwasher into a FireFly heatsink mounting hole.
    b. From the top side of the board add an M2.5 x 8 mm standoff.
    c. Tighten the screw and standoff.



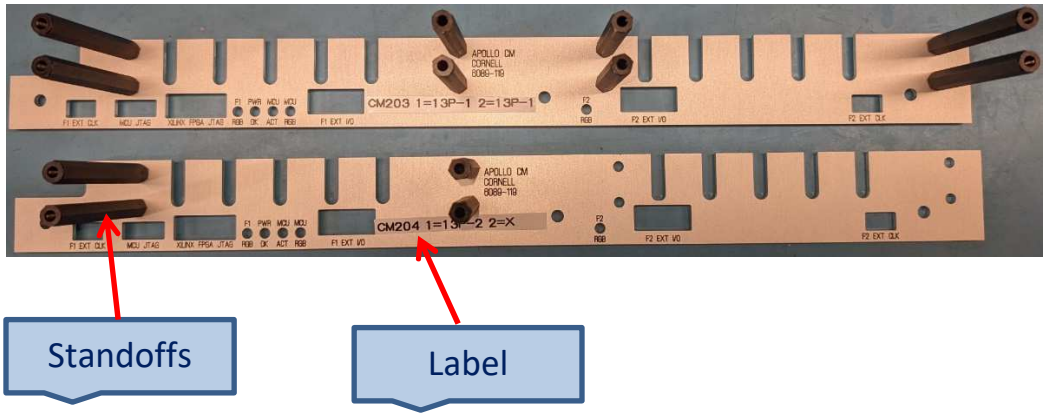
4) For each FPGA site that will need a heatsink, install:
    a. M3x8 screw plus M3 lockwasher from bottom side
    b. M3 standoff, 12 mm long, from top side

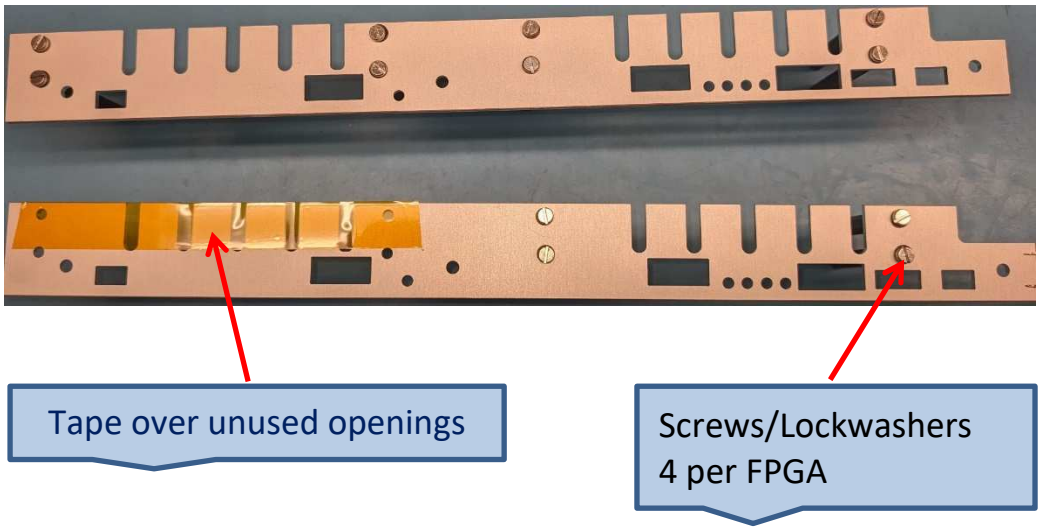


5) Remove and discard the screws from the front panel mounting blocks.

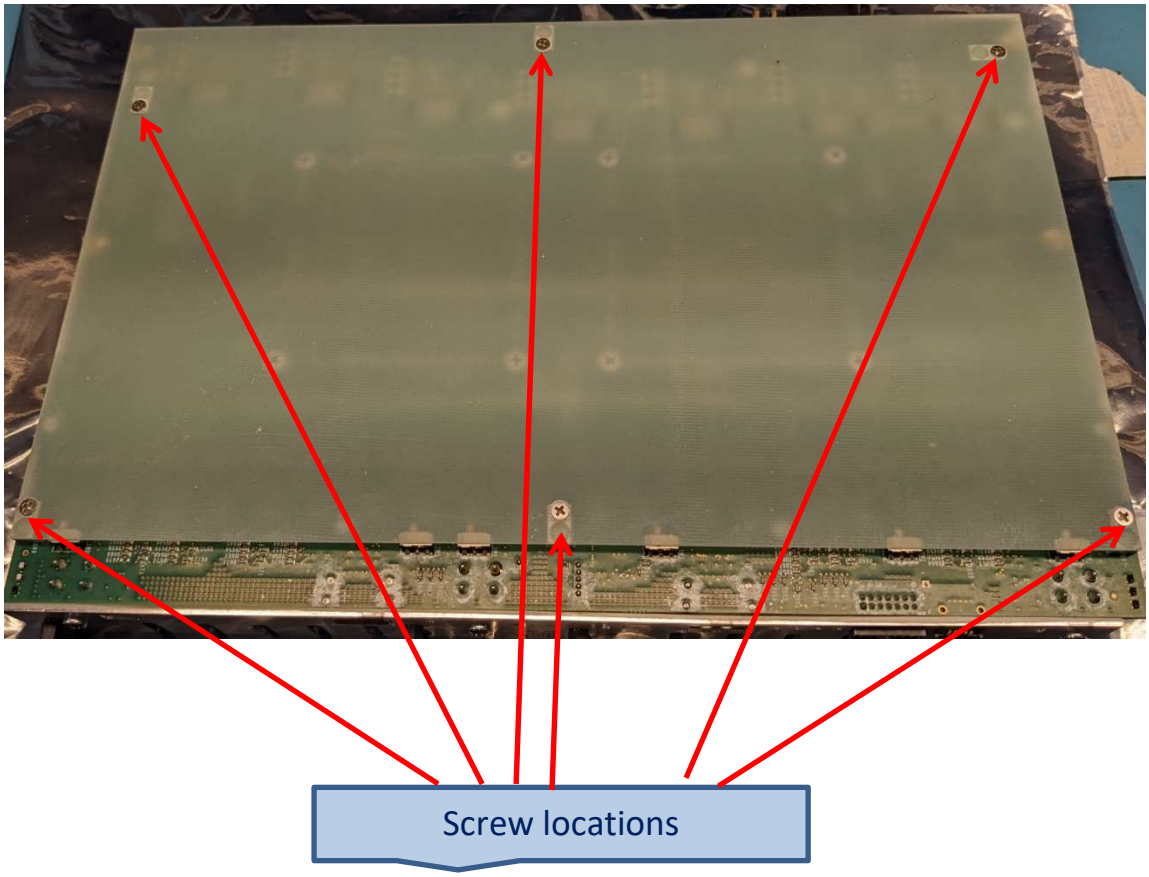


6) Prepare and attach front panel
    a. For each FPGA that is installed, attach four 45 mm standoffs for the fiber optic connectors by inserting M2.5x6 screws plus M2.5 lockwashers from the back side and threading on the spacers from the front side. Tighten so as to not strip the plastic threads.
    b. Print and attach a label that shows the CM serial number plus the type and speed of each FPGA. The format is “CMxxx 1=yyy 2=zzz” where “xxx” is the serial number that matched the one on the board, “yyy” and “zzz” ar the FPGA type and speed identifiers from the set {13P-1, 13P-2, 9P-1, 9P-2, X}. “X” indicates no FPGA.
    c. For boards with only one FPGA, cover the slots where the fibers would pass through with Kapton tape.
    d. Attach the front panel to the board with three M3x6 screws.



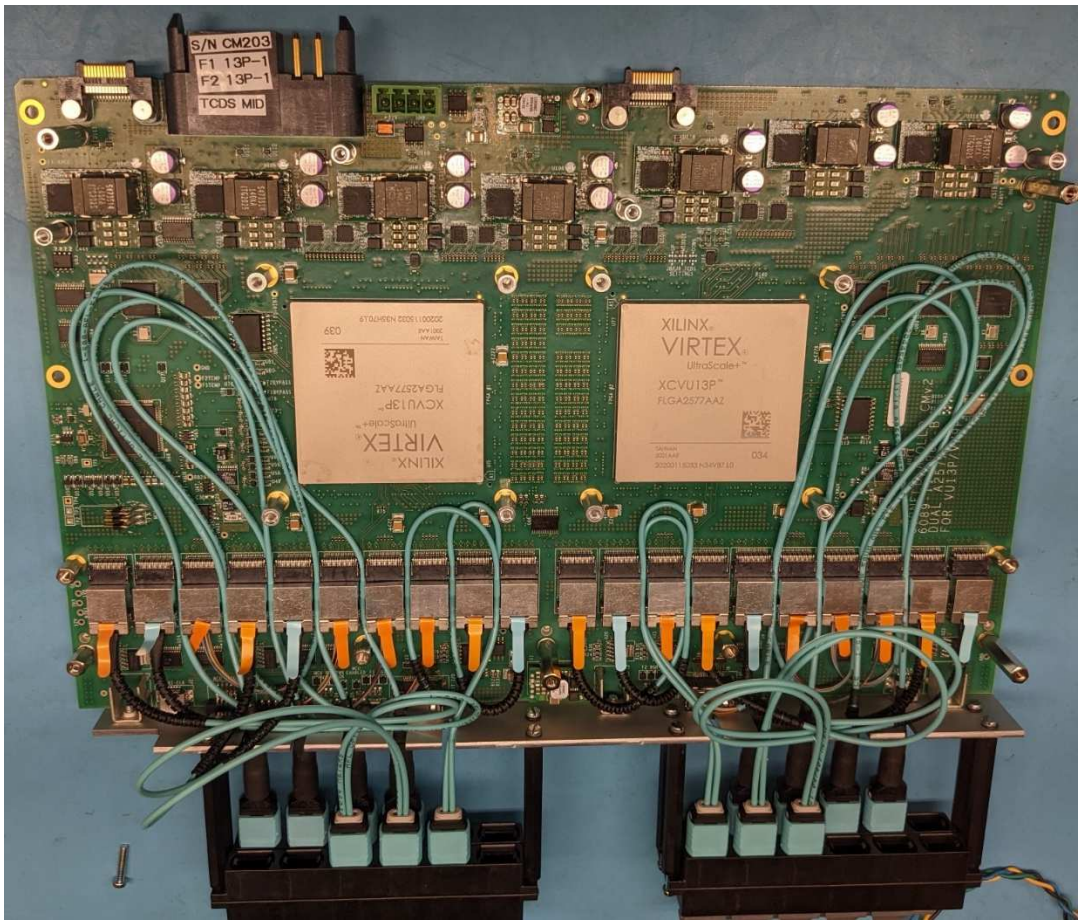


7) Attach a bottom cover with six M2.5x4 flathead screws.

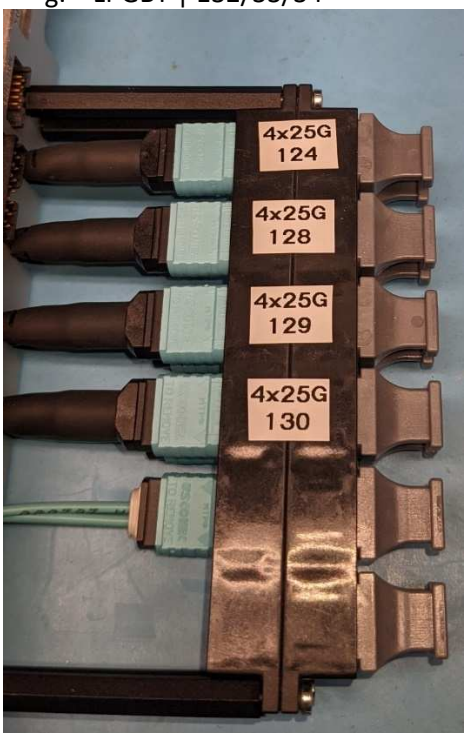


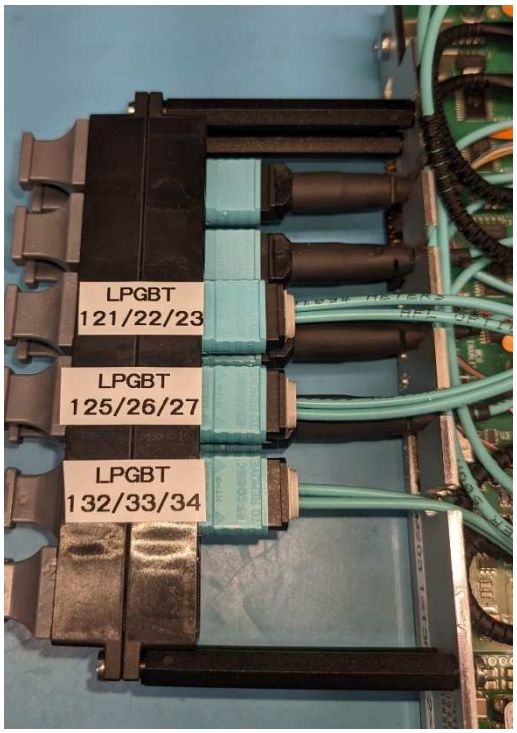
Install FireFly modules

1) Figure out how to label the FireFly modules to show what type they are. The current choices are:
    a. 25Gx4 transceiver in a single package
    b. 14Gx12 transmit/receive pair in two packages
    c. CERN LPGBT x12 transmit/receive pair in two packages
    d. 25Gx12 transmit/receive pair in two packages
2) Plug in all the required FireFly modules. The sites are labeled for the type of module as follows:
    a. X12 XMIT: 12 lane transmitter
    b. X12 RECV: 12 lane receiver
    c. X4 XCVR: 4 lane transmit/receive
3) Check the positions of the 12-lane transmitter voltage select switches on the bottom of the board. All should be set to 3.3V unless any 12 lane transmitter require 3.8 volts instead.
4) Route the blue fiber cables between FireFly modules. The photo below shows typical routing. The fibers must not stick up above the black part of the FireFly socket, even if the socket is empty. Otherwise, the FPGA heatsink will not mount correctly.

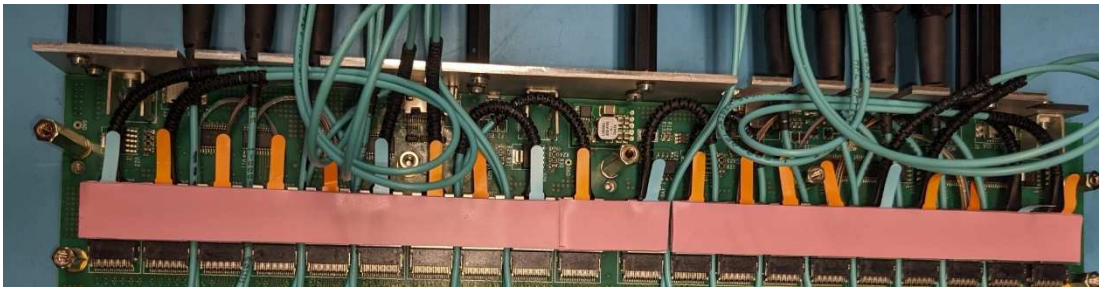


5) Plug the MTP connectors into the front panel junction blocks. Put them is the same order as they are installed on the board.
6) Label the junction blocks with the FireFly type and the quad number for the installed FPGA. For the VU13P the required labels are:
    a. 4x25G | 124
    b. 4x25G | 128
    c. 4x25G | 129
    d. 4x25G | 130
    e. LPGBT| 121/22/23
    f. LPGBT | 125/26/27
    g. LPGBT | 132/33/34

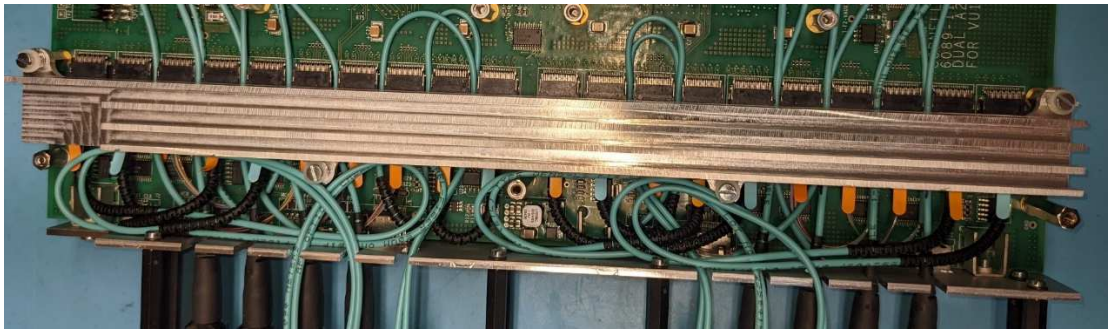


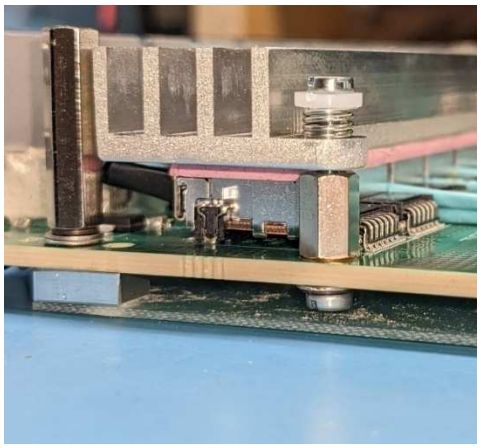


7) Cut ½" wide strips of pink 1.78 mm thick Laird Tflex HD300 (DigiKey P/N 926-1594). Apply them to the top of the FireFlys. Do not allow the foam to project beyond the face of the FireFly modules that is closest to the FPGAs. If it does, it will interfere with the FPGA heatsink. Make joints between FireFly modules, not on top of them.



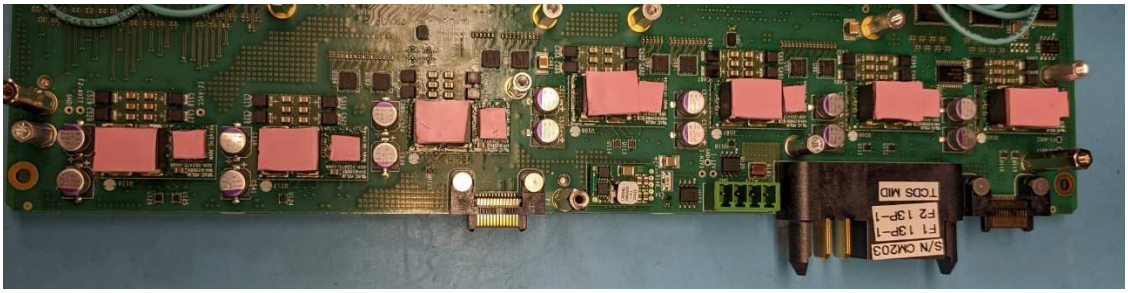
8) Mount the FireFly heatsink using 4 M2.5x12 screws, 4 M2.5 shoulder washers, and 4 S001YJ1D springs. Tighten the screws just until the springs are fully compressed. Dress the cables that fit between the heatsink and the front panel.



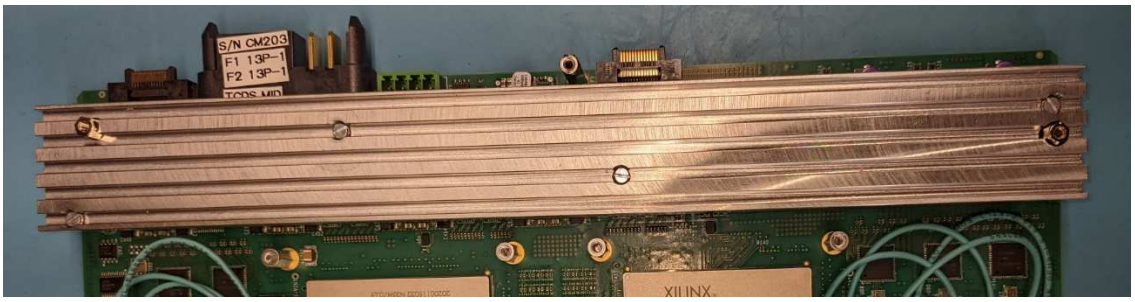


Install LGA80D heatsink

1) Place a 10-mm x 15-mm rectangle of 1.7 mm thick pink heatsink foam on top of the inductors on each LGA80D. Place an 8-mm x 8-mm square of 1.7 mm thick pink heatsink foam on top of the big chip on each LGA80D.



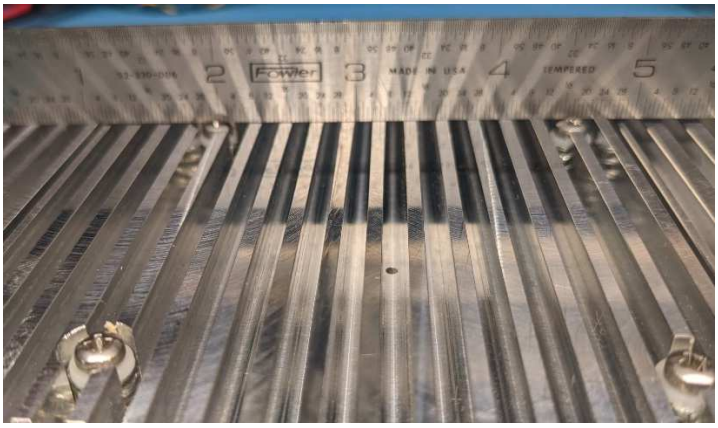
2) Place an LGA80D heatsink over the two tall cover standoffs. Loosely place an M2.5x6 screw plus an M2.5 lockwasher in each of the four mounting holes. Uniformly tighten the four mounting screws.

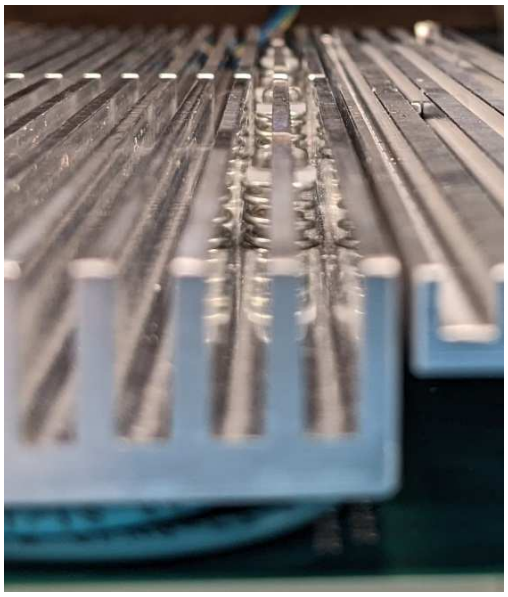


Install FPGA Heatsinks

1) If not already done, enlarge the 4 mounting holes on each FPGA heatsink to ¼ “. This allows the heatsink to move freely without rubbing on the standoffs.
2) Move the fiber optic cables away from any thick parts, and spread out any places where more than 2 fibers are stacked atop each other. Use Kapton tape to hold them in place if needed. Otherwise, the cables may interfere with good thermal contact between the heatsink and the FPGA.
3) Cut a ¼” square of 20 mil thermal foam and place it over the small hole in the center of each heatsink. This will prevent the thermal putty from being squeezed any thinner than 20 mils, and it will prevent thermal putty from coming through the hole.
4) Measure a generous ¼ tsp of thermal putty and place it in the center of the FPGA.

5) Place the heatsink over the standoffs and gently compress it.
6) Place springs over each standoff and insert an M3x12 mm screw and an M3 shoulder washer through the springs and into the standoff. Drive the screws until the top of the head is just below the top of the heatsink, and a straightedge does not catch the screw head. One-by-one, turn each screw 1 turn. After a few turns, the screw should bottom out against the screw holding the standoff to the board. The spring will not be fully compressed. The pressure will cause the thermal putty to gradually be pushed out around the perimeter of the FPGA.





Install splice plates and the top cover

1) Install splice plates at each end of the board using M3x6 screws. The screws should not touch the heatsinks.