

## Using the git repository

Initially, create a local copy of the CMv2 hardware repository with the command:

```
git clone git@github.com:apollo-lhc/Cornell\_CM\_Rev2\_HW
```

If you already have a local repository and you want to get all updates:

```
git pull
```

If you only want the update for a single file:

```
git fetch --all
```

```
git checkout origin/master name_of_file
```

Do your work in the sub-directories of the “ClockBuilderPRO” directory. When you are ready to save stuff in the repository, use:

```
git status
```

If the status shows that you have files that are not part of the repository, and you want them to be:

```
git add name_of_file
```

Update the local repository and push the changes to the repository on github.com:

```
git commit -a -m “description of changes”
```

```
git push origin master
```

## Running the LoadSynth program

Change directory to the “ClockBuilderPRO/programs” directory:

```
cd programs
```

Start the LoadSynth program, specifying which synth to configure and which file to use as the source of the configuration data:

```
python3 LoadSynth.py R0A ../projects/Si5341-RevD-R0Av0001-Registers.h --quiet
```

The synth is one of [ R0A, R0B, R1A, R1B, R1C ]. The case does not matter. One must be specified.

The relative path specification ahead of the configuration data file name is required if the register file is not in the same directory as the program (and it should not be). A configuration file must be specified

## Running the RampSynth program

Change directory to the “ClockBuilderPRO/programs” directory:

```
cd programs
```

Start the RampSynth program, specifying which synth to configure, what type of ramping to do, and which file to use as the source of the configuration data:

```
python3 RampSynth.py R0A up ../projects/Si5341-RevD-R0Av0003-Registers.h --quiet
```

The synth is one of [ R0A, R0B, R1A, R1B, R1C]. The case does not matter.

The type is one of [ UP, DOWN, BOTH, CONT]. The case does not matter. “UP” will ramp by increasing the frequency. “DOWN” will ramp by decreasing the frequency. “BOTH” will first ramp down, then ramp up. It will stop at the original frequency. “CONT” will continuously ramp down, then up, then down... It will go until interrupted, at which time it will leave the synthesizer at whatever the frequency currently is. To get back to a known frequency you need to run “LoadSynth” again.

The relative path specification ahead of the configuration data file name is required if the register file is not in the same directory as the program (and it should not be). The only need for the configuration file is to extract the data needed to calculate the number of steps.

NOTE: Maybe add a command line parameter “steps” to allow the user to specify the number of steps, rather than using the number extracted from the configuration data.

## Instructions for using Clock Builder PRO with the Apollo CMv2

This is initially written for an SI5341. Differences for an SI5395 will be accounted for later.

Step 1 – For the device ID register contents, enter the 8-character string consisting of the synthesizer name [one of R0A, R0B, R1A, R1B, R1C], followed by a lowercase “v”, then a 4 digit revision number [in the example “R0Av0001”]. This string will appear later in file names.

In the design notes block, enter a line like the one shown below. It should contain the schematic drawing number and revision [in the example “6089-119-RevA”] and the schematic sheet number where the associated device can be found [in the example :schematic sheet 2.06”].

Press “Next”

CB New Si5341 Project - ClockBuilder Pro

**ClockBuilder Pro** v4.1 **SKYWORKS**

Step 1 of 10 - Design ID & Notes ▼ Configuring Si5341ABCD Rev D

**Design ID**  
The device has 8 registers, DESIGN\_ID0 through DESIGN\_ID7, that can be used to store a design/configuration/revision identifier.

Design ID:  (optional; max 8 characters)  
The string you enter here is stored as ASCII bytes in registers DESIGN\_ID0 through DESIGN\_ID7.

Padding Mode: ☒ **NULL Padded**  
If you do not enter the full 8 characters, the remaining bytes of DESIGN\_IDx will be padded with 0x00 bytes (aka NULL character).  
☐ **Space Padded**  
If you do not enter the full 8 characters, the remaining bytes of DESIGN\_IDx will be padded with 0x20 bytes (space character).

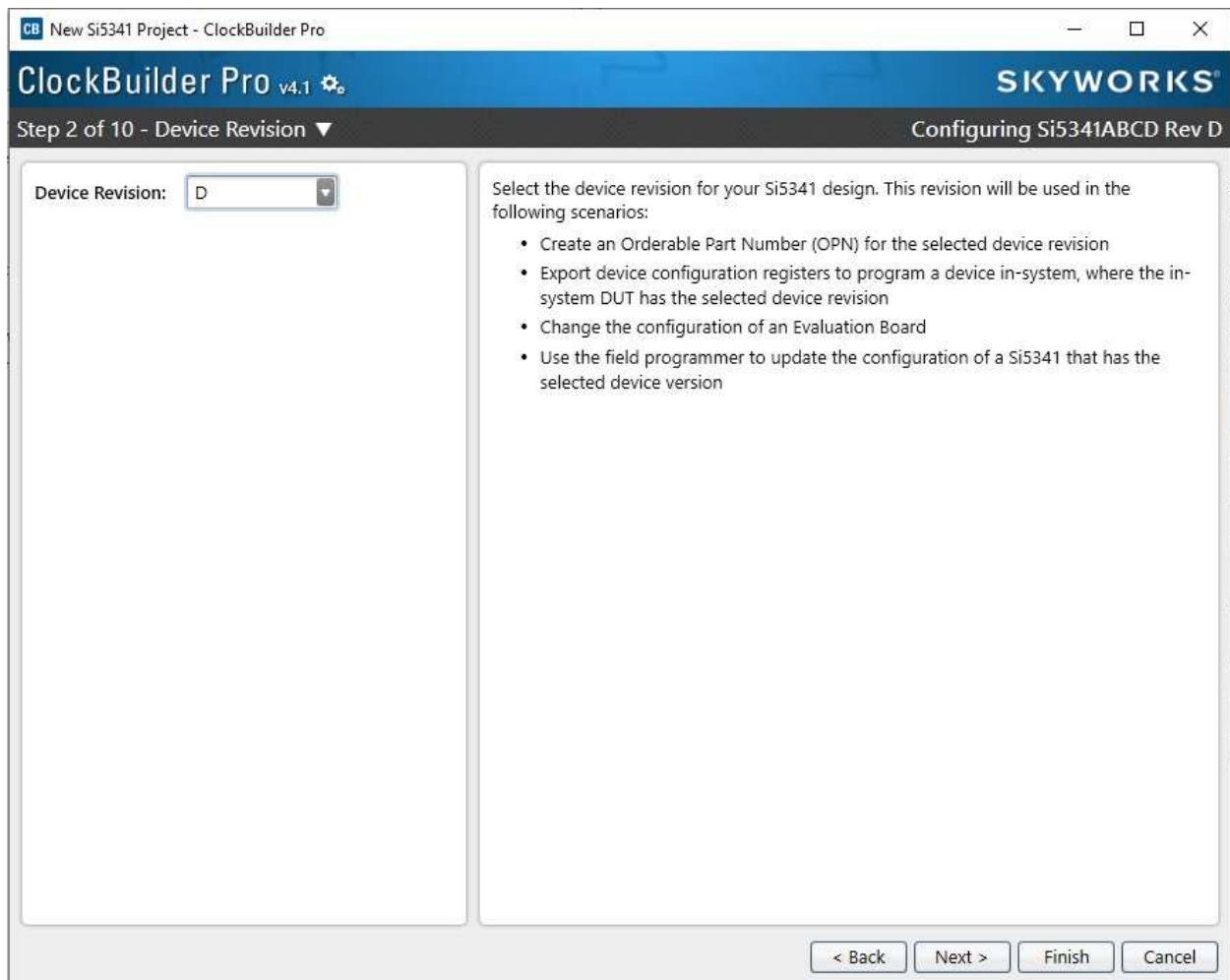
**Design Notes**  
Enter anything you want here. The text is stored in your project file and included in design reports and custom part number datasheet addendums. While the text is word wrapped in reports, you can use newlines to start a new paragraph.

Synthesizer for Apollo CMv2, 6089-119-RevA, schematic sheet 2.06


< Back Next > Finish Cancel

Step 2 – The SI5341 only comes with Device Revision “D”.

Press “Next”.



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Step 2 of 10 - Device Revision ▼

Configuring Si5341ABCD Rev D

Device Revision:

Select the device revision for your Si5341 design. This revision will be used in the following scenarios:

- Create an Orderable Part Number (OPN) for the selected device revision
- Export device configuration registers to program a device in-system, where the in-system DUT has the selected device revision
- Change the configuration of an Evaluation Board
- Use the field programmer to update the configuration of a Si5341 that has the selected device version

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Step 3 – In the “I/O Power Supply” box, select “VDDA (3.3V)”. That is the only selection that needs to be made on this page.

The device will be run in “I2C” mode, not “SPI”. This is selected by having the “I2C\_SEL” pin on the device be not connected. The internal pullup selects I2C.

The base I2C address is 0x77. It is set by configuration resistors on the board. Each of the five synthesizers is on its own single-device I2C bus, so they are all configured for address 0x77. Leave the Base I2C Address setting unchanged [1 1 1 0 1 A1 A0] for a range of 0x74 to 0x77

Press “Next”.

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Step 3 of 10 - Host Interface Configuring Si5341ABCD Rev D

Configuration and operation of the Si5341 is controlled by reading and writing registers using the I2C or SPI interface. The I2C\_SEL pin selects between I2C or SPI operation.

**I<sup>2</sup>C**  
I2C\_SEL pin = High

**SPI 4-Wire**  
I2C\_SEL pin = Low

**SPI 3-Wire**  
I2C\_SEL pin = Low

**I/O Power Supply**

☐ VDD (Core)  
The serial interface pins are always 3.3V tolerant, even when the device's VDD pin is supplied from a 1.8V source. The status outputs will have a VOH of ~ 1.8V. The control inputs are 3.3V tolerant.

☒ **VDDA (3.3V)**  
When the I2C or SPI host is operating at 3.3V and device at VDD=1.8V, this option must be selected. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds. The status outputs will have a VOH of ~ 3.3V and the control inputs expect 3.3V CMOS levels.

**SPI Mode**

☒ **4-Wire**  
4-wire SPI has separate serial data in and data out pins (SDI and SDO) which are unidirectional signals.

☐ 3-Wire  
3-wire SPI has a single serial data SDIO pin which is bidirectional.

**Base I2C Address**  
The upper 5-bits of the I2C address are configurable. The lower 2-bits are controlled using the A0 and A1 pins on the Si5341.

Address:

6	5	4	3	2	1	0
1	1	1	0	1	A1	A0

Address Range: 116d to 119d / 0x74 to 0x77

Host interface registers defined by this page – IO\_VDD\_SEL, SPI\_3WIRE, and I2C\_ADDR – are not written to EVBs. They are included in exports and orderable part number non-volatile memory. See the Family Reference Manual for more information.

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Step 4 – Generally chose one input for a design and leave all other inputs unused, even if there is a signal that is potentially available. Live switching is not usually needed. For instance, all five synthesizers have a 48 MHz crystal connected to the XA/XB pins. The ROA synthesizer also has a 322.265625 oscillator connected to the IN0 pins, and an output from the ROB synthesizer connected to the IN1 pins. This design will just use the 322.265625 MHz oscillator. In the “Mode” column for IN0 select “Enabled” from the popup window. Set the frequency to 322.265625 MHz. Be sure to indicate “MHz” in the value.

Four of the five synthesizers have wiring in place to support “Zero Delay Mode”. If it is available, and the application warrants using it, check the “Enable Zero Delay Mode” box and select the output that is connected for ZDM. ZDM is not available for the crystal input. For synthesizer ROA, it is not necessary when using the oscillator on IN\_0, but may be desirable when using the ROB output on IN\_1.

If you wanted to use the crystal instead, then select “Crystal Mode” for the XA/XB input and disable the other inputs. Disable ZDM as well, otherwise an error will be indicated.

Press “Next”.

**Input Clock Modes and Frequencies**

Input	Mode	Frequency
XA/XB	Unused	N/A
IN0	Enabled	322.265625 MHz
IN1	Unused	N/A
IN2	Unused	N/A

**Zero Delay Mode (ZDM)**

☒ Enable Zero Delay Mode

External Feedback Output: OUT9

**Important Notes About Zero Delay Mode (ZDM):**

- ZDM is optional. It is intended for applications that require a controlled minimum delay between the selected input and outputs.
- For optimal ZDM operation and performance, tie the FB\_IN clock pins to the OUT9 output clock pins.
- Although any one of the output clocks can be fed back to the FB\_IN pins, using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay (typically 100 ps). OUT9 is strongly recommended by Skyworks.

**Block Diagram:**

The diagram illustrates the clock input options and the Zero Delay Mode (ZDM) configuration. It shows the IN\_SEL[1:0] input, the IN0, IN1, and IN2 inputs, and the XA/XB input options. The XA/XB input options include the OSC (Oscillator) and the External Reference Clock Input Mode. The ZDM section shows the FB\_IN input and the P<sub>fb</sub> divider. The output is labeled OUT9.

**Frequency Plan Valid** **Design OK** **Typical Pd 660 mW, Tj 37 °C**

**Navigation:** < Back Next > Finish Cancel

Step 5 – For this design, only one input clock is defined and input clock selection is not used.

If input clock selection is needed, the board is designed to support using the “IN\_SEL[1:0]” pins. These pins are driven from I2C registers that appear on schematic sheet 4.03. These registers will power-up with all zeroes on the outputs, so the power-up selection will be the 48 MHz crystal (even if it not enabled).

The input clock selection can also be done from a register.

Press “Next”.

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Step 5 of 10 - Input Clock Selection ▼ Configuring Si5341ABCD Rev D

Because you have only defined one input clock, input clock selection does not need to be configured.

**Manual Clock Select Mode**

☒ **Register**  
Use the input select register via serial interface to select the input clock.  
Power on Default:

☐ **Pins**  
Use the IN\_SEL[1:0] pins to select the input clock.

Input clock selection can be made manually using the IN\_SEL[1:0] pins or with an input select register using the serial interface. A device register selects input selection as pin selectable or register selectable. When the zero delay mode is enabled, IN3 becomes the feedback input and is not available for selection as a clock input.

Frequency Plan Valid Design OK Typical Pd 660 mW, Tj 37 °C

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Step 6 – Enable the outputs that are both connected and will be used by selecting “Enabled (Powered-up with Output Enabled)” in the “Mode” column.

For boards with only FPGA#1 populated, outputs to FPGA#2 should be left disabled. This will both save power and minimize electrical noise. The 100 ohm terminators are internal to the FPGA and are not present if the FPGA is not installed, so the signal will reflect and ring on the PCB traces.

For boards with only FPGA#1 populated and no jumper board in the FPGA#2 site, outputs to the right side of FPGA#1 should be left disabled. This will save power. [Verify that this is true for TCDS signals.]

Some outputs connect to other synthesizers and will only be used under special circumstances. Leave them disabled until needed. This will save power.

The “Disabled State” for each output can be left at “Stop Low”.

The “Format” for each output should be set to “LVDS 1.8 V”.

Enter the desired frequency for each enabled output. Be sure to indicate “MHz” in the value.

If ZDM is being used, pick the “N0” manual assignment in the “N Divider/DCO/ZDM” column.

Press “Next”.

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Step 6 of 10 - Define Output Clocks Configuring Si5341ABCD Rev D

Output	Mode	Disabled State	Format	Frequency	N Divider / DCO / ZDM
OUT0	Unused	N/A	N/A	N/A	N/A
OUT1	Unused	N/A	N/A	N/A	N/A
OUT2	Enabled	Stop Low	LVDS 1.8 V	322.2656... MHz [ 322 + 17/64 MHz ]	N0... ✓
OUT3	Enabled	Stop Low	LVDS 1.8 V	322.2656... MHz [ 322 + 17/64 MHz ]	N0... ✓
OUT4	Unused	N/A	N/A	N/A	N/A
OUT5	Unused	N/A	N/A	N/A	N/A
OUT6	Unused	N/A	N/A	N/A	N/A
OUT7	Unused	N/A	N/A	N/A	N/A
OUT8	Unused	N/A	N/A	N/A	N/A
OUT9	ZDM	Stop Low	LVDS 1.8 V	ZDM (322.265625 MHz)	N0... ✓

Clock Placement Wizard ... FOTF Supported ...

Frequency Plan Valid Design OK Typical Pd 660 mW, Tj 37 °C

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**Schematic Diagram:** Shows an oscillator (OSC) connected to a DSPLL, which feeds into Dividers & Phase Adjust, and finally to outputs OUT0 through OUT9.



Step 7 – This project does not use “DCO Mode”

Press “Next”.

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Step 7 of 10 - DCO (Digitally Controlled Oscillator) ▼

Configuring Si5341ABCD Rev D

Mode: ☒ Frequency Increment/Decrement via FINC/FDEC Register & Pin Control  
☐ Write to Divider Registers Directly

Nx	DCO Enable	Desired Step Size	Range ?	Initial Step Size	Output	Frequency	Initial Step Size
N0	<input checked="" type="checkbox"/>	1 ppm	± 200 ppm	---	OUT2 OUT3 OUT9	322.2656... MHz 322.2656... MHz 322.2656... MHz	---
N1	<input type="checkbox"/>	1 ppm	± 200 ppm		No Outputs		
N2	<input type="checkbox"/>	1 ppm	± 200 ppm		No Outputs		
N3	<input type="checkbox"/>	1 ppm	± 200 ppm		No Outputs		
N4	<input type="checkbox"/>	1 ppm	± 200 ppm		No Outputs		

DCO Report ...

Overview

DCO mode is designed for small , glitchless frequency changes. A [short introductory video](#) is available. The [Family Reference Manual](#) and [AN959](#) has more detailed technical information.

FINC/FDEC Mode

Output frequencies are adjustable in pre-defined steps defined by frequency step words (FSW). The frequency adjustments are initiated using the frequency increment (FINC) or decrement (FDEC) device registers or pins.

$$F_{out} = \frac{F_{vco} * N_{x\_DEN}}{(N_{x\_NUM} \pm n * N_{x\_FSTEPW}) * R_y}$$

The N\_FSTEP\_MSK register controls whether all or a sub-set of Nx dividers are incremented or decremented. Any DCO enabled Nx divider will be included in FINC/FDEC by CBPro. Your host can change this in-system via I2C/SPI.

Register Direct Write Mode

In this mode, the host directly writes the Nx\_NUM register value to set a new output frequency for all output(s) on an Nx divider.

$$F_{out} = \frac{F_{vco} * N_{x\_DEN}}{N_{x\_NUM} * R_y}$$

The host writes the Nx\_UPDATE register to cause the change to take effect.

Frequency Plan Valid

Design OK

Typical Pd 660 mW, Tj 37 °C

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Finish

Cancel

Step 8 – Unless otherwise known, the frequency planner should be instructed to maximize the number of low jitter outputs.

Press “Next”.

CB New Si5341 Project - ClockBuilder Pro

**ClockBuilder Pro** v4.1 **SKYWORKS**

Step 8 of 10 - Configure Frequency Planner ▼ Configuring Si5341ABCD Rev D

☒ **Maximize the number of low jitter outputs**  
CBPro will select the frequency plan with the most number of outputs on an integer N divider.

☐ **Select one output as lowest jitter**  
CBPro will ensure that the selected output is on an integer N divider. Where possible, other outputs that are even common multiple related will be placed on the same divider, within the bounds of any manual N divider assignment you have configured.

Output:

The ClockBuilder Pro frequency planner tries a variety of possible VCO frequencies and divider values to compute your frequency plan. You can modify the criteria used to select the best frequency plan.

Other factors may still be weighted higher than the options to the left depending on device configuration and revision.

These settings will have no effect when using the CBProFOTF1 Command Line Tool to do Frequency-On-The-Fly (FOTF). The FOTF tool will optimize for lowest jitter across all plans.

Frequency Plan Valid Design OK Typical Pd 660 mW, Tj 37 °C

< Back Next > Finish Cancel

Step 9 – Unless otherwise known, the LOS (Loss Of Signal) values should be left as is.

Press “Next”.

CB

New Si5341 Project - ClockBuilder Pro

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ClockBuilder Pro v4.1 ⚙

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Step 9 of 10 - LOS (Loss of Signal) ▾

Configuring Si5341ABCD Rev D

LOS Detect

Thresholds for assert and de-assert of LOS are specified in number of corresponding clock cycles at the input to the phase detector, which is the input clock divided by it's P divider. This is translated to a time based on the frequency of the corresponding phase detector input clock.

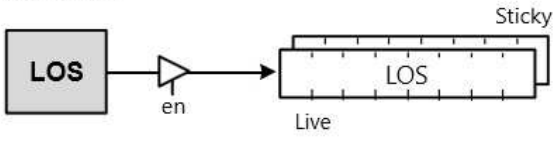
Input Clock	Assert Threshold ?	De-Assert Threshold ?	Validation Time ?
IN0	4,000	4,000	100 ms
IN1	N/A	N/A	N/A
IN2	N/A	N/A	N/A
FB_IN	4,000	4,000	100 ms

XA/XB Threshold and validation times are not configurable for LOS on XA/XB

The loss of signal monitor measures the period of each phase detector input clock cycle to detect phase irregularities or missing clock edges.

Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors.

The LOS status for each of the monitors is accessible by reading a status register.



⌚ Frequency Plan Valid

✓ Design OK

⚙ Typical Pd 660 mW, Tj 37 °C

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Finish

Cancel

Step 10 – The interrupt output pin is connected to an I2C registers that appear on schematic sheet 4.03. It will not actually generate an interrupt. It will be available for polling by the MCU.

Use the default settings unless something different is desired.

Press “Next”.

CB New Si5341 Project - ClockBuilder Pro

**ClockBuilder Pro** v4.1

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Step 10 of 10 - Interrupt Pin ▼

Configuring Si5341ABCD Rev D

**INTR Config - Define What Alert Conditions Should Assert INTR**

LOSREF\_FLG ?

LOSXAXB\_FLG ☒ ?

(IN0) LOS\_FLG[0] ☒ ?

(IN1) LOS\_FLG[1] ☐ ?

(IN2) LOS\_FLG[2] ☐ ?

(FB\_IN) LOS\_FLG[3] ☒ ?

LOL\_FLG ?

SMBUS\_TIMEOUT\_FLG ☒ ?

SYSINCAL\_FLG ?

LOS

INTR

The interrupt pin (INTR) indicates a change in state in a configurable group of status registers. Most status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTR pin is reset by clearing the sticky status registers.

When you check a status condition in the editor, you are indicating that you want that signal to contribute to INTR. Note that there are some conditions that will always contribute to INTR: loss of XA/XB signal and system calibration in progress. Mouse over the ? icons to learn more.

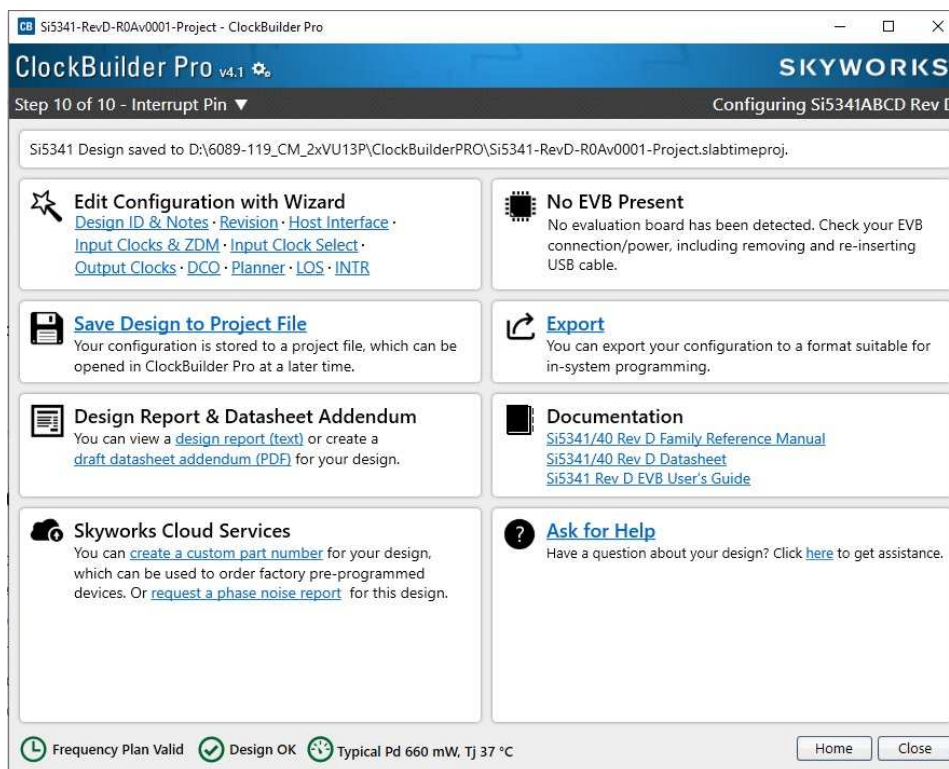
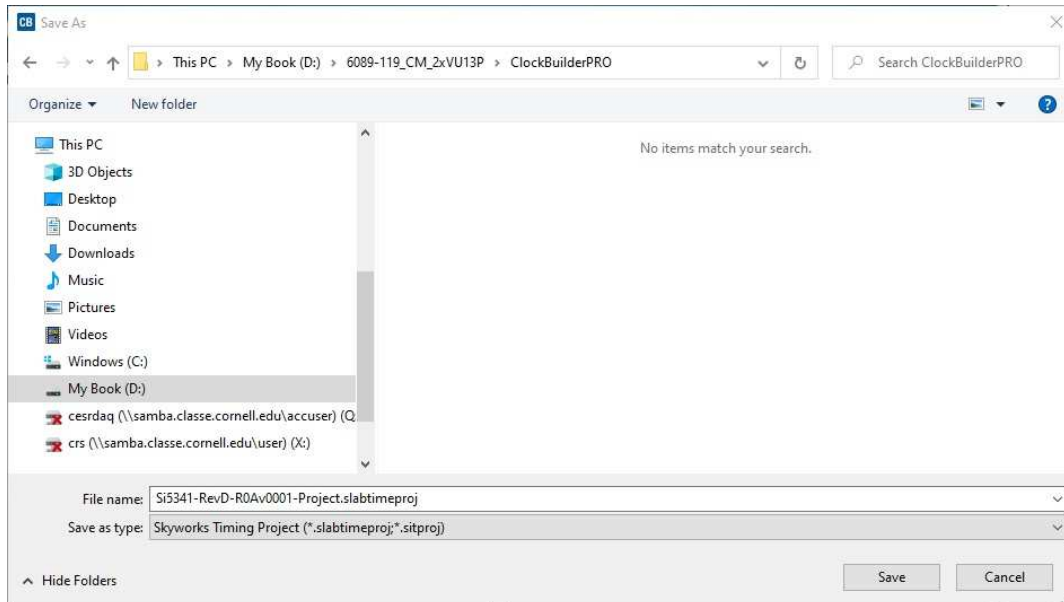
Frequency Plan Valid Design OK Typical Pd 660 mW, Tj 37 °C

< Back Next > Finish Cancel

Step 11 - The design dashboard will appear after step 10.

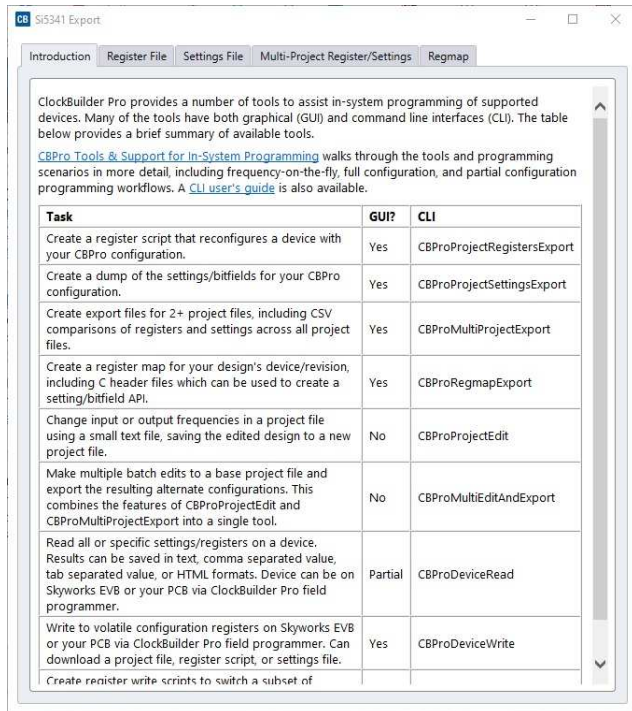
After making any changes, save the design to a project file. The name of the project file should reflect the “Design ID” entered in step 1.

Press “Save”. The design dashboard will reappear with a confirmation message.



Step 12 – Export a configuration file that can be downloaded to the hardware. Select “Export” on the dashboard.

In the popup “export” window, select the “Register File” tab.



Under the register file tab, select “C Code Header File”. Check the box for “Include pre- and post-...”. Press “Save to File”. It will be saved as a “.h” file.

