lpGBT-symmetric Back-end links

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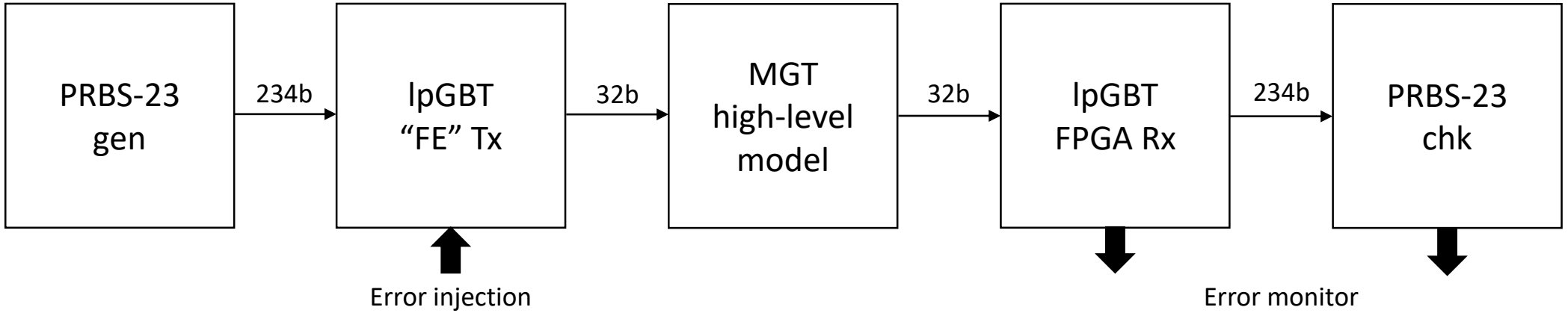
Simulation overview

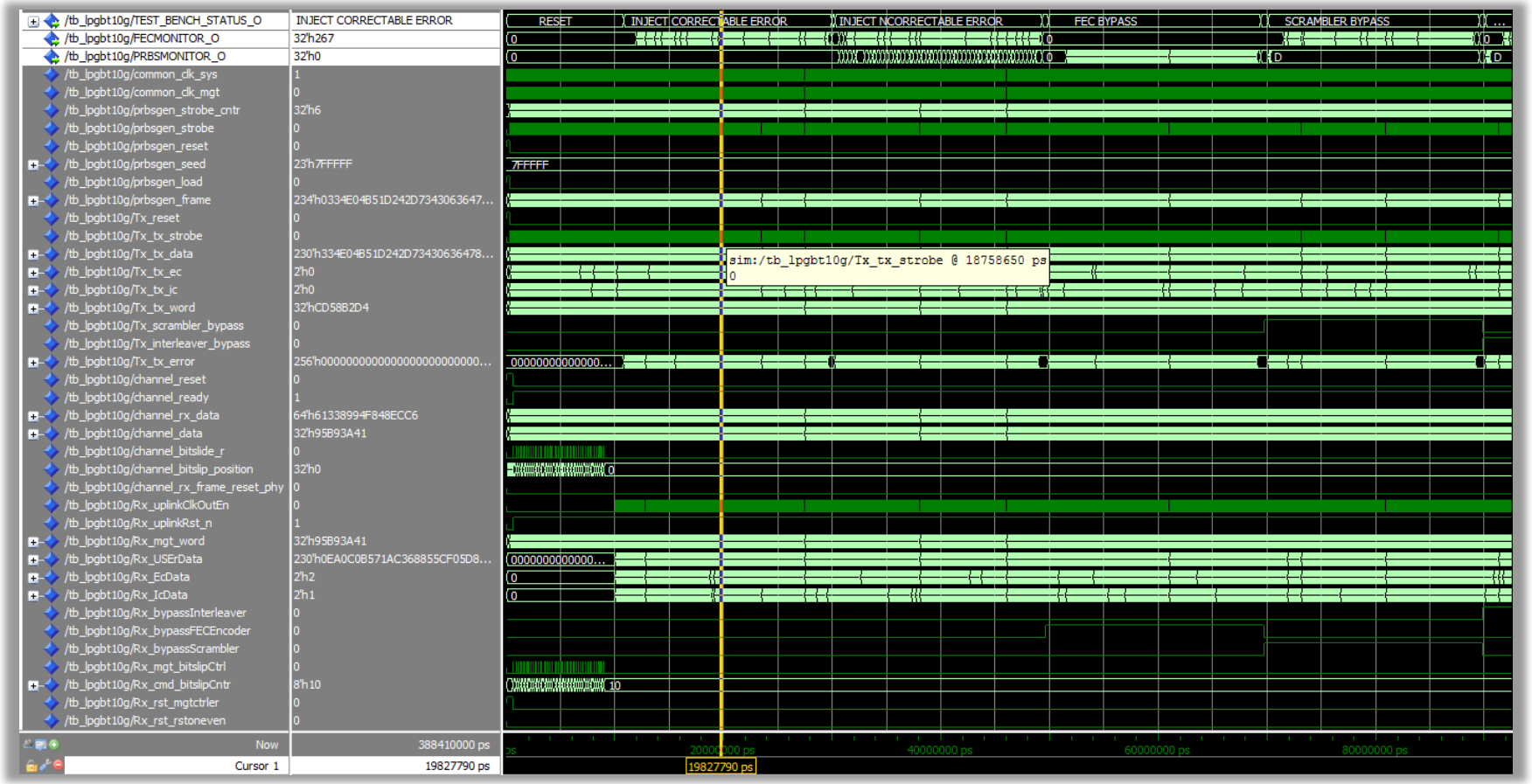
- Block-diagram
  - lpGBT 10.24Gbps / FEC5
  - lpGBT FE Tx: VHDL wrapper of the original Verilog files adapted for FPGA impl.



  - MGT word-size configurable
  - FEC, DATA-RATE configurable
  - A few scenarios were tested:
    - Burst-error of maximum length always correctable (6 consecutive bits)
    - Burst-error of length 7 (sometimes not corrected)
    - Bypass (de)scrambler, (de)interleaver and FEC decoding (while injecting single-bit errors)
    - Do a few resets rx and checked the resetoneven logic could be active

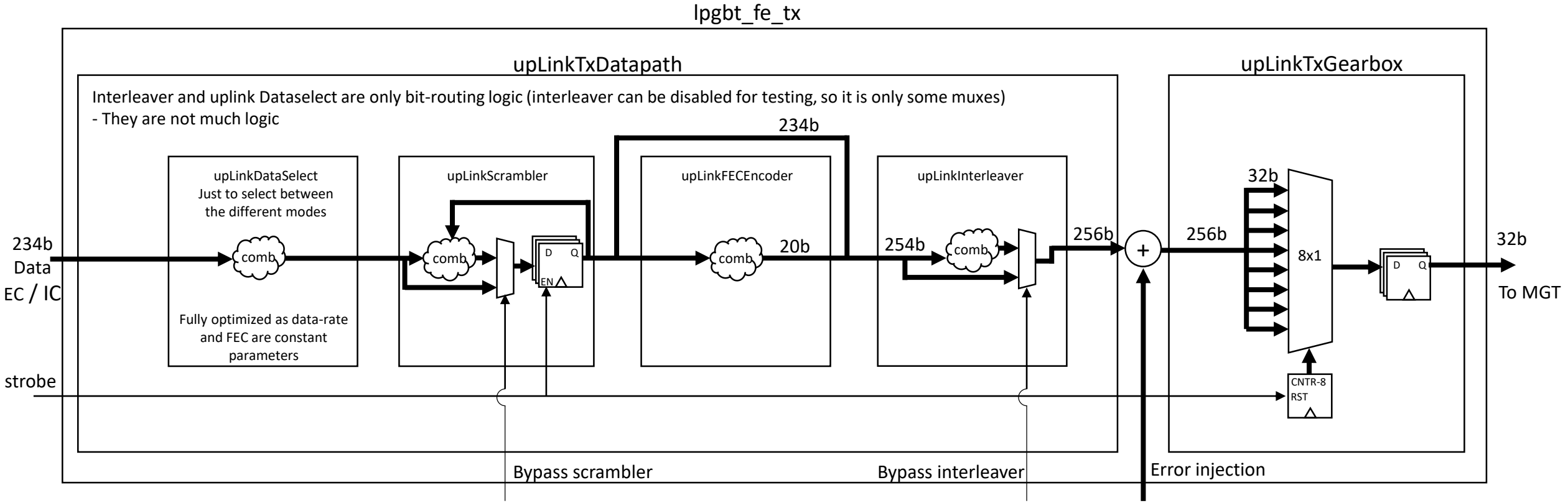
Simulation overview

- Run simulation
  - Open ModelSim (tested on ModelSim SE-64 10.7)
  - Go to folder ./firmware/source/datapath/tb_lpGBT10G)
  - Write: do run_sim_lpgbt_symmetric.do ☺



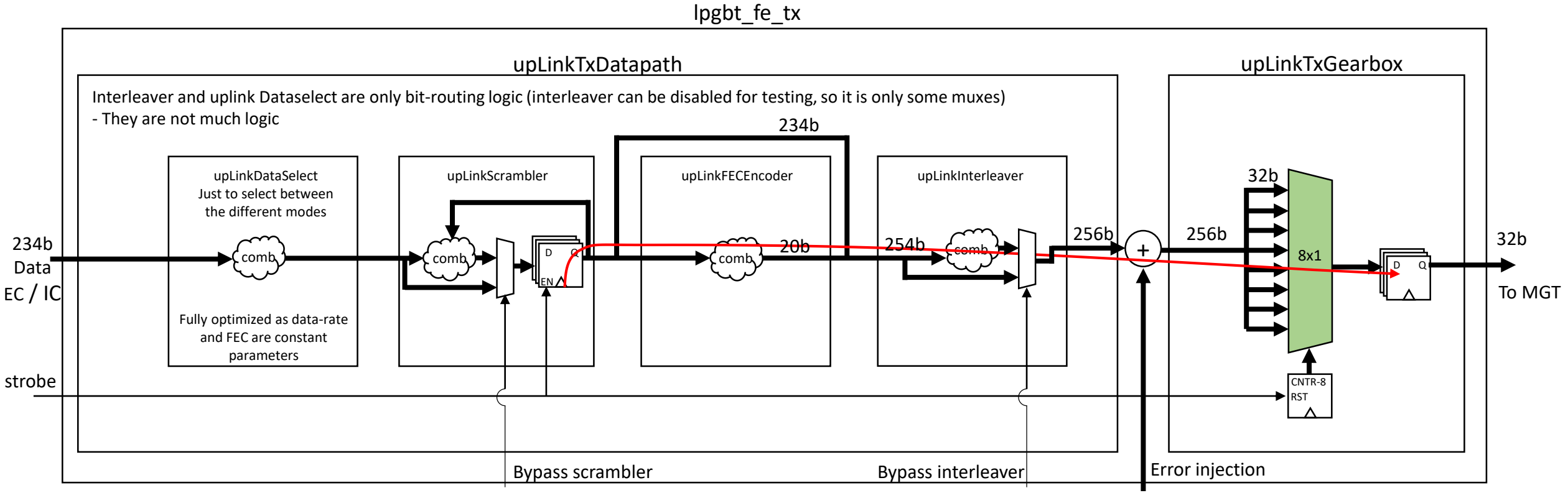
lpGBT FE Tx 10G-FEC5

- lpGBT FE Tx overview
  - upLinkTxDatapath: Verilog codes from ASIC designers with some adaptations for FPGA impl.
  - Fully synchronous to txusrclk from MGT
    - If needed, recommended to do any needed clock-domain-crossing before input



lpGBT FE Tx 10G-FEC5

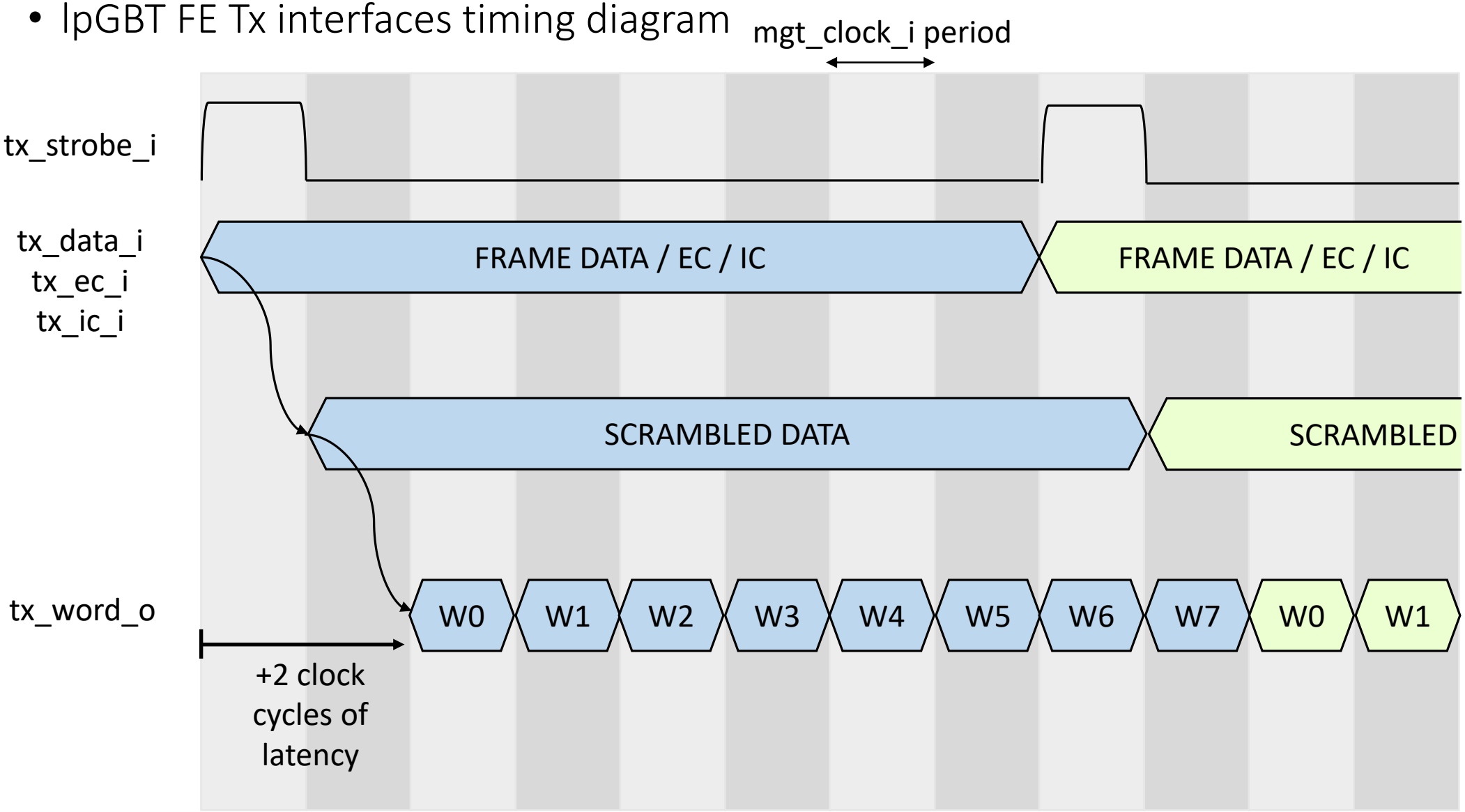
- lpGBT FE Tx timing constraint for STA
  - No special constraints needed (the MGT reference clock has to be constrained of course)
  - Information that data message are sent first than FEC parity bits can relax STA:
    - A multicycle path constraint can be applied to paths going through FEC encoder: shown below



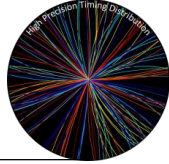
- A multicycle path can be applied to bits passing through the red arrow (i.e. through FECEncoder)
  - Implemented in exdsg. see lpgbt10G_timing.xdc

lpGBT FE Tx 10G-FEC5

- lpGBT FE Tx interfaces timing diagram



lpGBT-FPGA Rx 10G-FEC5



- Official lpGBT-FPGA design (https://gitlab.cern.ch/gbt-fpga/lpgbt-fpga)