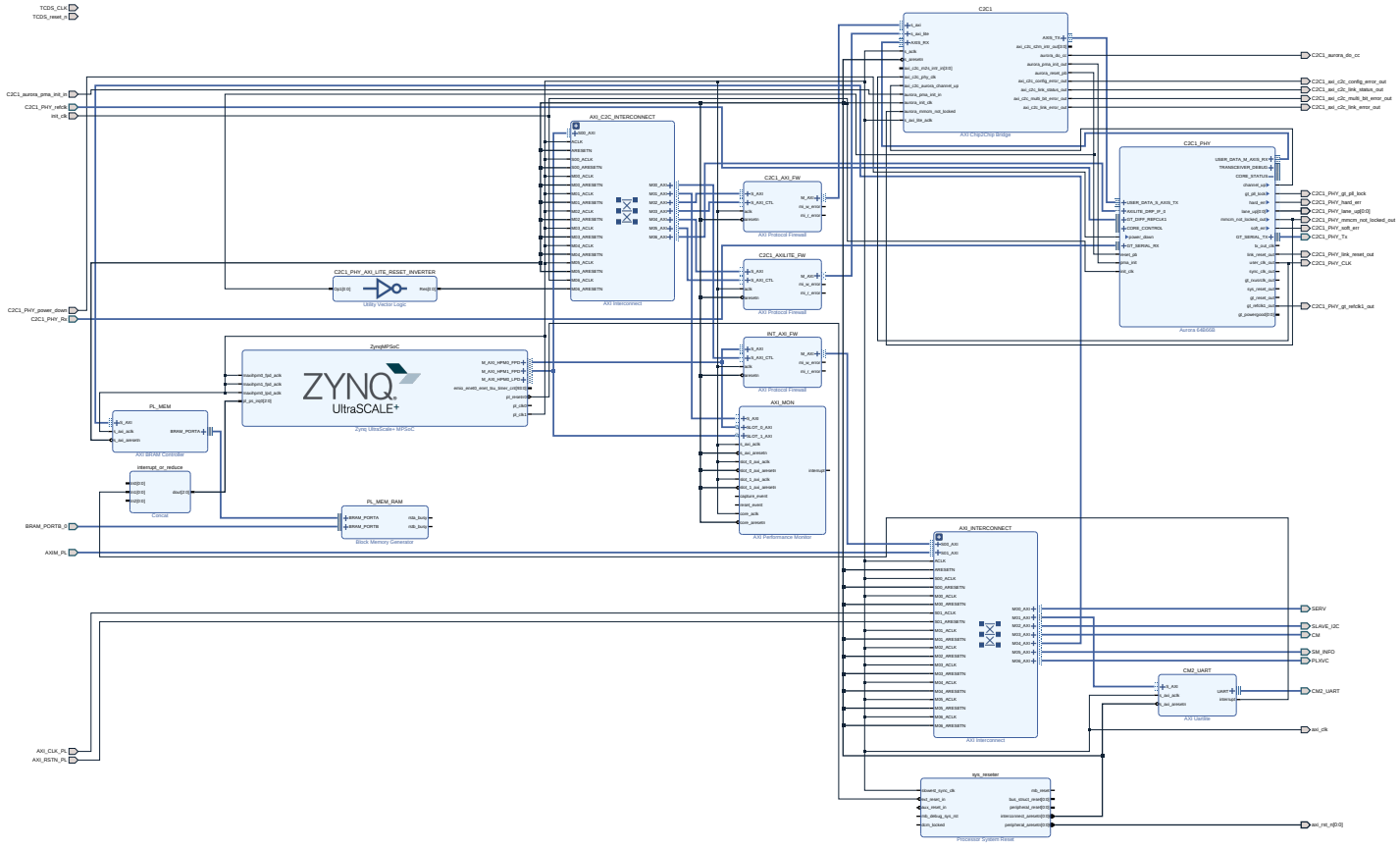
TCDS_CLK
TCDS_reset_n
C2C1_aurora_gma_init_in
C2C1_PHY_refclk
init_clk
C2C1_PHY_power_down
C2C1_PHY_Rx
BRAM_PORTB_0
AXIM_PL
AXI_CLK_PL
AXI_ISTN_PL
C2C1
AXI CHIpsChip Bridge
C2C1_PHY
Aurora 64B66B
AXI_C2C_INTERCONNECT
AXI Interconnect
C2C1_AXI_FW
AXI Protocol Firewall
C2C1_AXILITE_FW
AXI Protocol Firewall
INT_AXI_FW
AXI Protocol Firewall
AXI_MON
AXI Performance Monitor
C2C1_PHY_AXI_LITE_RESET_INVERTER
Utility Vector Logic
ZynqMPSoC
Zynq UltraScale+ MPSoC
PL_MEM
AXI BRAM Controller
interrupt_or_reduce
Concat
PL_MEM_RAM
Block Memory Generator
AXI_INTERCONNECT
AXI Interconnect
CM2_UART
AXI Uartlite
sys_reseter
Processor System Reset
C2C1_aurora_dio_cc
C2C1_axi_c2c_config_error_out
C2C1_axi_c2c_link_status_out
C2C1_axi_c2c_multi_bit_error_out
C2C1_axi_c2c_link_error_out
C2C1_PHY_gt_pll_lock
C2C1_PHY_hard_err
C2C1_PHY_lane_up[0:0]
C2C1_PHY_mmcm_not_locked_out
C2C1_PHY_soft_err
C2C1_PHY_Tx
C2C1_PHY_link_reset_out
C2C1_PHY_CLK
C2C1_PHY_gt_refclk1_out
SERV
SLAVE_I2C
CM
SM_INFO
PLXVC
CM2_UART
axi_clk
axi_rst_n[0:0]