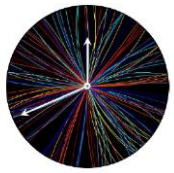


TCLink

MGT recommended reset procedure

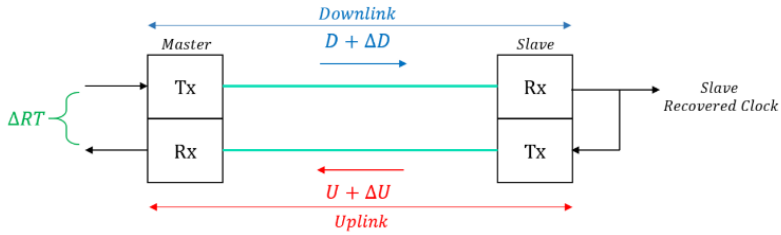
28/01/2021

Eduardo Mendes

Jeroen Hegeman

Introduction

- The recommendation for resetting the TCLink lpGBT link is the following:
  1) Reset Tx master
  2) Reset Rx slave
  3) Reset Tx slave
  4) Reset Rx master



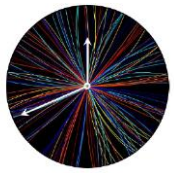
More details on exact signals in example design quick start guides

- Under certain conditions, if a Rx reset is issued before the incoming serial data is stable, the transceiver may recover invalid data.
  - Limitation known to Xilinx (confirmed by Paolo Novellini) and related to CDR and equalizer initializations.
  - The Xilinx IPs contain a retrial timeout to reset the Rx periodically if data is not ‘consistent’ (protocol-dependent) to ensure automatic re-lock.

- An example of such reset procedure is integrated in the core with a Finite State Machine (FSM) which was designed by Jeroen Hegeman.
  - Available in ‘tclink/tclink_channel_controller.vhd’.

- This design note shows an overview of the FSM implementation and how to activate and use it.

FSM overview



- In the record *core_ctrl_i* of the TCLink lpGBT core, the following signals control the FSM:

- *channel_controller_reset:* reset FSM.
- *channel_controller_enable:* enable FSM operation.
- *channel_controller_gentle:* gentle reset is applied. Recommended to set to 0 only for first reset and to 1 for subsequent resets.

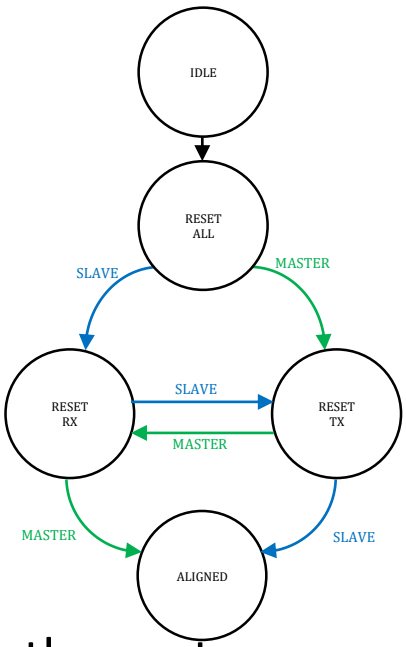
- In the record *core_stat_o,* the following signals output the status of the FSM:

- *channel_controller_running:* FSM is activated.
- *channel_controller_state:* hot-one encoded FSM state for debugging. More details in next page.
- *channel_ready:* FSM operation is completed.

- The principle of the state machine is shown in the diagram below.

- The generic *g_QUAD_LEADER* is used to describe if a master channel is connected to the Xilinx transceiver quad PLL resets

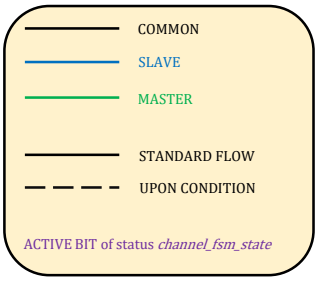
- Please note that the slave reset and master sequences are different

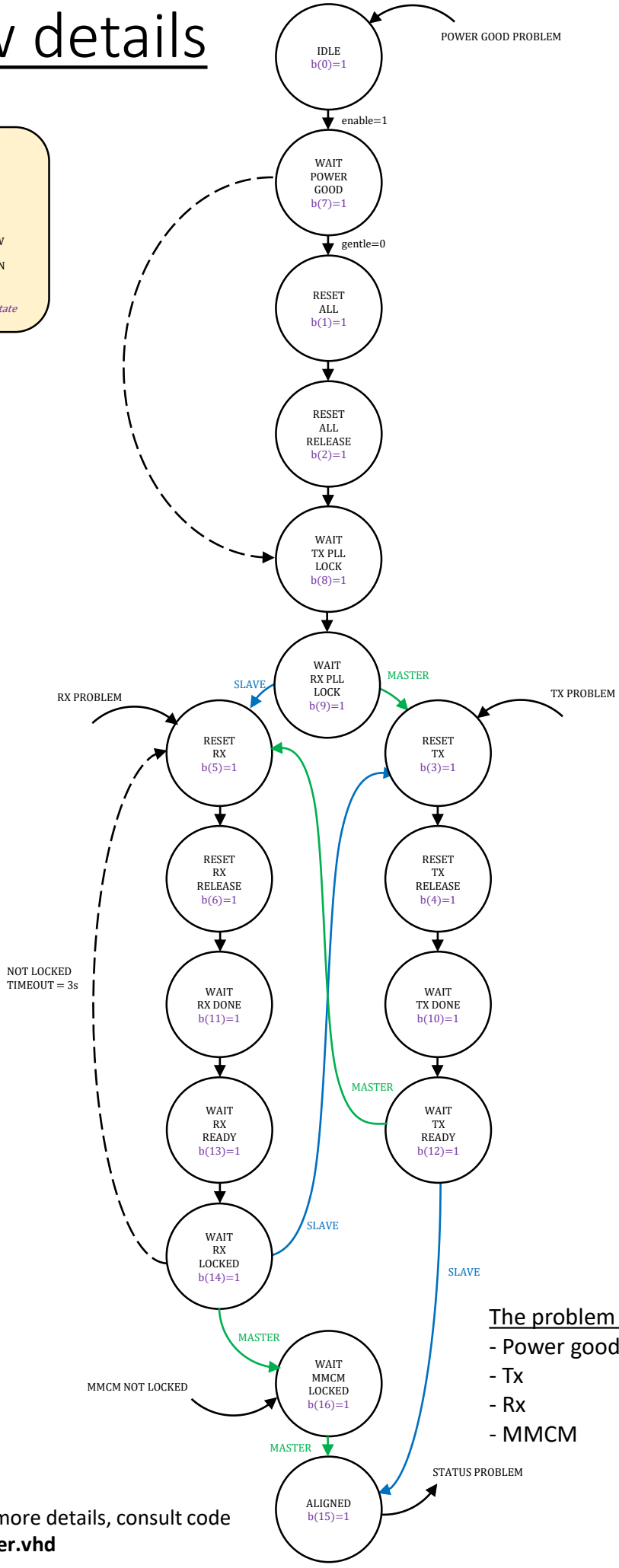


- More details in the FSM operation in the next page.

Ilustrative diagram. For more details, consult code **tclink_channel_controller.vhd**

FSM flow details





The problem order of priority is:

- Power good
- Tx
- Rx
- MMCM

Ilustrative diagram. For more details, consult code **tclink_channel_controller.vhd**