

# Yashwant Marathe

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## CONTACT

2C-801, Akme Harmony  
Apartments  
Bellandur, Bangalore - 560103  
India

marathe.yashwant@gmail.com  
(+91) - 9481882949

## OBJECTIVE

Seeking an entry level full-time position as a Design/Verification Engineer.

## WORK EXPERIENCE

Broadcom India Private Limited

July 2013 — Present

IC Design Engineer

As an IC Design Engineer at Broadcom, I was primarily involved in the following activities.

- Verification of the Modem clock distribution network - Performed functional verification of each individual component (clock gates, clock dividers) of the clock distribution network.
- Verification of the Modem RF Base Band module - Performed functional verification of the RF Base Band module by designing directed testcases in C/SV. Primarily verified Automatic Frequency Correction and event scheduling capabilities.
- Owner of Memory libraries and Leaf Level Power Management module of the Modem IP.
- I was partially involved in the following activities.
  - Automation of SoC integration using Atrenta GenSys tool
  - Gate Level Simulation and debugging of the Modem IP
  - Memory daisy chaining checks of the Modem IP
  - Microarchitecture and design of the AXI - APB bridge.

Broadcom India Private Limited

May 2012 — July 2012

Intern

- Converted various RTL designs into corresponding virtual prototypes using Carbon SoC Designer and performed functional verification on them.
- Benchmarked Carbon SoC Designer and Palladium based on various parameters.

## EDUCATION

B.Tech in Electronics and  
Communications Engineering

July 2009 — May 2013

National Institute of Technology Karnataka, Surathkal

Graduated with a CGPA of 9.38/10.

## TECHNICAL SKILLS

Strong background in digital and VLSI design by virtue of working in the semiconductor industry, and also through projects and coursework. Notable skills include -

- Programming Languages - C, C++, Python, Perl, Octave
- Hardware Description Languages - Verilog, System Verilog and VHDL
- Markup Languages - LaTeX