

IB Paper 8 Electrical Engineering

Lecture 12 Fabricating Devices: Etching

https://www.vle.cam.ac.uk/course/view.php?id=69961

Introduction

- We have seen that, using photolithography, it is possible to form a patterned polymer layer on the surface of a sample
 - However, we require some means by which this pattern can be transferred to the sample itself
 - This usually requires the removal of surface layers of material – known as surface micromachining – or of large amounts of the substrate itself – known as bulk micromachining
 - Material must therefore be etched away in a controlled fashion to create the desired structures
- Etching divides very neatly into two well defined categories:

1. Wet etching

Immersion of the substrate in a liquid

2. Dry etching

Exposure to reactive species in the gas phase

Wet Etching

- The wet etching of microstructures by immersion in a reactive chemical mixture involves three main steps
 - 1. Transportation of reactants to the surface to be etched
 - 2. Chemical reaction between the reactants and the surface
 - 3. Transportation of reactant products away from the surface
- If step 1 is the rate limiting step in the process then the reaction is said to be *mass transfer limited*, whist if step 2 is the rate limiting step, then the process is said to be *reaction rate limited*
- Etching is characterised by:
 - Etching rate
 - Etch selectivity
 - Etch uniformity

Isotropic Etching

- Most wet chemical etches are isotropic in nature
 - In other word, they etch all crystal planes of a material at the same rate, and so a single etch rate can be used to describe the process
 - Therefore, assuming that the masking material is completely resistant to the etch (we will return to this assumption shortly), isotropic wet etching tends to produce a very characteristic undercut profile



- Isotropic etching is widely used for
 - Removal of work damaged surfaces
 - Rounding of sharp, anisotropically etched corners which can be a source of stress concentrations
 - Removal of roughness created by dry or anisotropic etches
 - Simple pattering
 - Creation of free standing structures by undercutting
- It is of particular importance in the last two cases that only desired regions are actually etched
 - For this reason, it is important that the etching rate of the masking material is much slower than that of the material to be etched
 - A high degree of *selectivity* is therefore required
- A large number of wet etches have been characterised for a range of MEMS materials, allowing a sensible choice of etchant for a particular system

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The center and bottom values are the	low and high etch i	ates obser	rved by th	e author a	and others	in the U	CB Micro	lab using	fresh and	used solu	itions, clea	an and "di	rty" chan	nbers, etc.			
ETCHANT			1	1	1				MA	TERIAL		4			V	(V)	
EQUIPMENT	TARGET	SC Si	Poly	Poly	Wet	Dry	LTO	PSG	PSG	Stoic	Low-σ	Al/	Sput	Court	Court	ocg	0"
CONDITIONS	MATERIAL	<100>	n*	undop	Ox	Ox	undop	unanl	annld	Nitrid	Nitrid	2% Si	Tung	Sput Ti	Sput Ti/W	820PR	Olin HntPl
Concentrated HF (49%) Wet Sink	Silicon		0	-	23k	F	>14k	F	36k	140	52	42		F	-	PO	P
Room Temperature	oxides				18k 23k					1	30	0		100			
10:1 HF	Silicon		7	0		230	340	15k	4700	11	52	42	-		-		
Wet Sink Room Temperature	oxides		7.0			2.50	340	1.5%	4700	11	3	2500 2500	0	11k	<70	0	
25:1 HF	O.U.		-	-								12k					
Wet Sink	Silicon		0	0	97	95	150	w	1500	6	1	W	0			0	
Room Temperature	Oxides																
5:1 BHF	Silicon		9	2	1000	1000	1200	6800	4400	9	4	1400	<20	F	1000	0	
Wet Sink Room Temperature	oxides				900		100000	100000	3500		3	1400	0.25		1000	U	
Phosphoric Acid (85%)	Silicon	-	7		0.7	0.0			4400	-	4	-	20				
Heated Bath with Reflux	nitrides	1	1 '		u.r	0.8	<1	37	24	28 28	19	9800				550	39
160°C							10000		24	42	42						
Silicon Etchant (126 HNO ₃ : 60 H ₂ O: 5 NH ₄ F)	Silicon	1500	3100	1000	87	w	110	4000	1700	2	3	4000	130	3000		0	
Wet Sink Room Temperature			1200										1	115			
KOH (1 KOH : 2 H ₃ O by weight)	<100> Silicon	141-	6000	12	22												
Heated Stirred Bath	Croop anicon	14k	>10k	F	77		94	W	380	0	0	F	0	(40	- 3	F	1
80°C					77												
Aluminum Etchant Type A (16 H ₃ PO ₄ : 1 HNO ₃ : 1 HAc: 2 H ₂ O)	Alumnium	-	<10	<9	0	0	0		<10	0	2	6600		0			
Heated Bath									410		-	2600		0		0	
50°C									1 (5 (5 (6)			6600					
Titanium Etchant (20 H ₂ O : 1 H ₂ O ₂ : 1 HF)	Titanium		12		120	W	w	W	2100	8	4	W	0	8800		0	
Wet Sink Room Temperature							700		55,000	30		1 000	0	000000			
H ₂ O ₂ (30%)	Tuesday		-	-	-								<10				
Wet Sink	Tungsten		0	0	0	0	0	0	0	0	0	<20	190	0	60	<2	(
Room Temperature													190		60		19
Piranha (~50 H ₂ SO ₄ : 1 H ₂ O ₂)	Cleaning off		0	0	0	0	0		0	0	0	1000	1000	2400	150	-	
Heated Bath	metals and			- 50	"			ं	U	0	0	1800		2400		F	
120°C	organics		-					-									
Acetone Wet Sink	Photoresist		0	0	0	0	0		0	0	0	0		0		>44k	>399
Room Temperature	_									-							-37
F ₄ +CHF ₅ +He (90:30:120 sccm)	Silicon	w	1900	2100	1700	***	4400			0.222							
Lam 590 Plasma	oxides	"	1400	1500	4700 2400	w	4500	7300	6200	1800	1900		w	W	W	2200	2000
450W, 2.8T, gap=0.38cm, 13.56MHz	Oxides		1900	2100	4800			3000 7300	2500 7200								
F ₄ +CHF ₃ +He (90:30:120 seem)	Silicon	W	2200	1700	6000	W	6400	7400	6700	4200	2000		111				-
Lam 590 Plasma	oxides	1000	2200	1700	2500	20075	6000	5500	5000	4000	3800		W	W	W	2600	2900
850W, 2.8T, gap=0.38cm, 13.56MHz		1	2700	2100	7600		6400	7400	6700	6800						2600 6700	720
F ₆ +He (13:21 sccm)	Silicon	300	730	670	310	350	370	610	480	820	620		w	w	w	690	63
Technics PE II-A Plasma	nitrides	300	730	670					230		550					690	
100W, 250mT, gap≈2.6cm, 50kHz sq. wave F ₄ +CHF ₃ +He (10:5:10 secm)	C.E.	1000	800	760					480		800				-	830	
Technics PE II-A Plasma	Silicon	1100	1900	w	730	710	730	w	900	1300	1100		W	W	w	690	60
200W, 250mT, gap=2.6cm, 50kHz sq. wave	nitrides																
F ₆ +He (175:50 sccm)	Thin	W	6400	7000	300	w	280	530	510	1200	070			-			
Lam 480 Plasma	silicon		0100	2000	220	"	200	330	540	1300 830	870		w	w	w	1500	1400
150W, 375mT, gap=1.35cm, 13.56MHz	nitrides			7000	400					2300				. 1		1300 1500	
F ₆ +He (175:50 sccm)	Thick	w	8400	9200	800	w	770	1500	1200	2800	2100		w	w	w	3400	3100
Lam 480 Plasma	silicon				~		5,000,00	1000000	0.00000	2100	17.00		- 12			3100	310
250W, 375mT, gap=1.35cm, 13.56MHz F _c (25 secm)	nitrides									4200						3400	
Tegal Inline Plasma 701	Thin	w	1700	2800	1100	W	1100	1400	1400	2800	2300		W	w	W	3400	3100
125W, 200mT, 40°C	silicon nitrides				1100					2800						2900	
F_+CHF_+He (45:15:60 secm)	Si-rich	w	350	360	1600 320	w	220	620	450	2800						3400	
Tegal Inline Plasma 701	silicon	"	330	300	320	w	320	530	450	760	600		W	w	w	400	360
100W, 300mT, 13.56MHz	nitrides															- 1	
1 ₂ +He (180:400 sccm)	Silicon	w	5700	3200	8		60	230	140	560	530	w	w	-	-	2000	200
Lam Rainbow 4420 Plasma	2.000	5000	3400	3200	8			2.50	140	300	330				-	3000	2700
275W, 425mT, 40°C, gap=0.80cm, 13.56MHz		5000	6300	3700	380											2400 3000	
Br+Cl ₂ (70:70 sccm)	Silicon	W	450	460	4		0	0	0	870	26	w	W			350	300
Lam Rainbow 4420 Plasma			450		4								. 72			350	
200W, 300mT, 40°C, gap=0.80cm, 13.56MHz l ₂ +BCl ₃ +CHCl ₃ +N, (30:50:20:50 secm)			740		10								to second			500	
Lam 690 RIE	Aluminum	w	4500	w	680	670	750	W	740	930	860	6000	W			6300	6300
250W, 250mT, 60°C, 13.56MHz												1900				3700	3300
F _a (80 sccm)	Tungsten	w	5800	5400	1200	w	1200	1800	1500	3600	2200	6400	2000			6300	6100
Tegal Inline Plasma 701			2000	5400	2000	""	1200	1000	1500	2600	2300 1900		2800	W	w	2400	2400
200W, 150mT, 40°C, 13.56MHz					2000						2300		2800 4000			2400 4000	
	Descumming		0	0	0	0	0	0	0	0	0	0	0	0		350	300
2 (51 secm)	photoresist					- 200			18	- 300				-	1000	200	300
2 (51 seem) Technics PE II-A Plasma																	
t(51 secm) Technics PE II-A Plasma 50W, 300mT, gap=2.6cm, 50kHz sq. wave				0	0	0	0	0	0	0	0	0	0	0		3400	3600
(51 seem) Technics PE II-A Plasma 50W, 500mT, gap=2.6cm, 50kHz sq. wave (51 seem)	Ashing		0	~ 1	7,850,85							0.70					
(51 seem) Technics PE II-A Plasma 50W, 300mT, gap=2.6cm, 50kHz sq. wave (51 seem) Technics PE II-A Plasma	Ashing Photoresist	•	0	_ [
(51 seem) Technics PE II-A Plasma 50W, 300mT, gap=2.6cm, 50kHz sq. wave (51 seem) Technics PE II-A Plasma 400W, 300mT, gap=2.6cm, 50kHz sq. wave	Photoresist					W	700	2100	1602								
, (51 seem) Technics PE II-A Plasma 50W, 300mT, gap=2.6cm, 50kHz sq. wave , (51 seem) Technics PE II-A Plasma 400W, 300mT, gap=2.6cm, 50kHz sq. wave F Vapor I cm over plastic dish	Photoresist Silicon		0	0	660	w	780	2100	1500	10	19	A	0	A		P 0	P 0
, (51 seem) Technics PE II-A Plasma 50W, 300mT, gap=2.6cm, 50kHz sq. wave , (51 seem) Technics PE II-A Plasma 400W, 300mT, gap=2.6cm, 50kHz sq. wave F Vapor I em over plastic dish Room temperature and pressure	Photoresist	•				w	780	2100	1500	10				A		P 0	
, (51 seem) Technics PE II-A Plasma 50W, 300mT, gap=2.6cm, 50kHz sq. wave , (51 seem) Technics PE II-A Plasma 400W, 300mT, gap=2.6cm, 50kHz sq. wave F Vapor I cm over plastic dish	Photoresist Silicon	4600				w	780	2100	1500	10				A 290		P 0	

Notation: - =test not performed; W=not performed, but known to Work (≥ 100 Å/min); F=not performed, but known to be Fast (≥ 10 kÅ/min);
P=some of film Peeled during etch or when rinsed; A=film was visibly Attacked and roughened.
Rates measured are rounded to two significant figures.
Etch areas are all of a 4-inch wafer for the transparent films and half of the wafer for single-crystal silicon and the metals.
Etch rates will vary with temperature and prior use of solution or plasma chamber, area of exposure of film, other materials present (e.g., photoresist), film impurities and microstructure, etc. Some variation should be expected.

- By way of an example, let us consider how we might create a freestanding silicon cantilever using only wet chemistry
 - We will need to find a sacrificial material that can be removed from underneath the cantilever without attacking the Si
 - A good candidate is silicon oxide that is readily attacked by buffered hydrofluoric acid (bHF)
 - SiO₂ dissolves in HF according to the reaction
 SiO₂ + 6HF → H₂SiF₆ + 2H₂O
 - H₂SiF₆ is soluble in water, and so may be transported away from the reaction surface
 - bHF does not significantly etch Si, so we will be able to undercut a cantilever structure, however, we require some means of patterning a continuous layer of Si

- The most common etchants for silicon are mixtures of HF with an oxidising agent, such as nitric acid (HNO₃) and either water or acetic acid (CH₃COOH)
- Initially silicon is oxidised in the presence of holes by

$$Si + 2H^+ \rightarrow Si^{2+} + H_2$$

Water is dissociated in the solution,

$$H_2O \rightarrow (OH)^- + H^+$$

 and the hydroxyl ions combine with the positively charged silicon ions to form silicon oxide,

$$Si^{2+} + 2(OH)^{-} \rightarrow Si(OH)_{2}$$

 $Si(OH)_{2} \rightarrow SiO_{2} + H_{2(gas)}$

- The surface layer of SiO₂ formed on the silicon is then etched by the HF through reaction 10.1
- We can then construct the full fabrication process

Step 1

Start with a 'silicon-on-insulator' (SOI) wafer consisting of a 10 µm thick layer of silicon oxide on a silicon with a 0.5 µm layer of Si on top. A 2 µm thick layer of photoresist is added.



Step 2

The photoresist is patterned to protect the cantilever, and a HNO₃:HF:CH₃COOH etch used to remove the unwanted poly-Si.



Step 3

A bHF etch is then used to undercut the cantilever.



Step 4

Finally, the remaining photoresist is removed by acetone. Acetone has a low surface tension, and so in drying does not cause the cantilever to collapse.

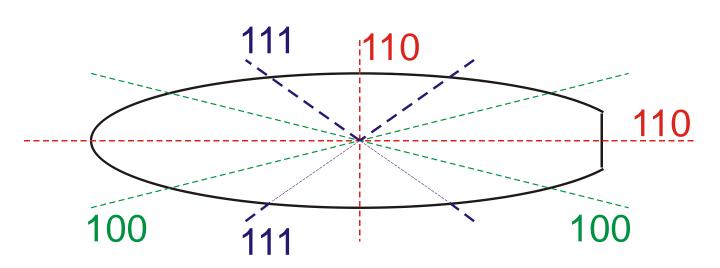


Anisotropic Etching

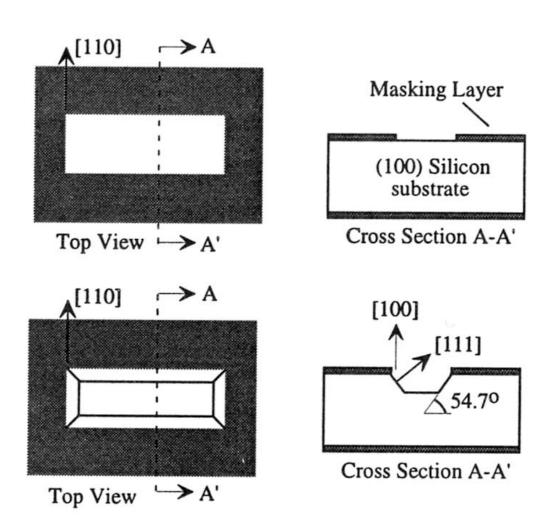
- Whilst most wet etches are isotropic, in some cases the wet chemical etch rate varies with crystallographic orientation, resulting in anisotropy
 - In the case of silicon, the most common anisotropic etchants are strong bases
 - 1. Aqueous potassium hydroxide (KOH) (sometimes with isopropyl alcohol, IPA)
 - 2. Tetramethylammoniumhydroxide (TmAH)
 - 3. Ethylene diamine pyrochatecol (EDP)

			Etch Rate [μm hr ⁻¹]		
Etchant	Temper- ature [°C]	Si(100)	Si(110)	Si(111)	
KOH: H ₂ O	80	84	126	0.21	
КОН	75	25-42	39-66	0.5	
EDP	110	51	57	1.25	
N ₂ H ₄ H ₂ O	118	176	99	11	
NH ₄ OH	75	24	8	1	

- Orientation dependence is a consequence of the fact that different crystalline surfaces will have varying structures
 - The (111) surface of c-Si is particularly stable as a silicon atom on the surface will only have one of its four bonds pointing out of the surface with the other three pointing back into the bulk of the material
 - This results in a stable surface with a high surface density of atoms
 - As KOH etching, for example, proceeds by the insertion of an OH group into a Si—Si bond, the etch rate of the Si(111) surface is suppressed



- The result of this is that if a masking pattern is produced on the surface of a Si(100) wafer with sides in the <110> directions, then a groove will be etched with sides at an angle of 54.7° with respect to the surface plane
 - For short etching times, rectangular features will yield U-shaped grooves with (111) oriented sidewalls and a (100) oriented base



- The etch will proceed with time until only stable (111) surfaces remain
 - Rectangular features will produce v-grooves, whilst square patterns will produce inverted pyramids

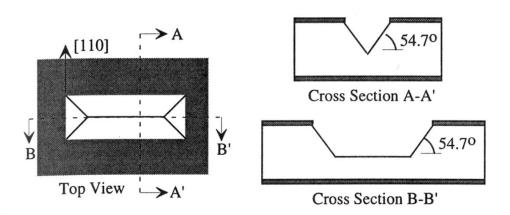


Figure 3.21. If the structure of Fig. 3.20 is allowed to continue, a self-terminating V-groove is formed, with all surfaces bounded by {111} planes.

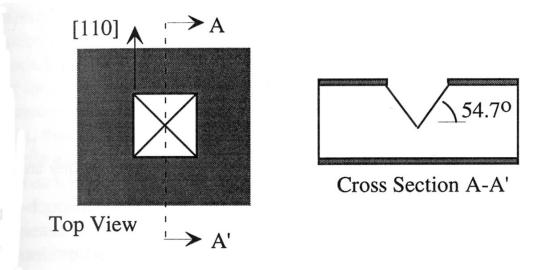
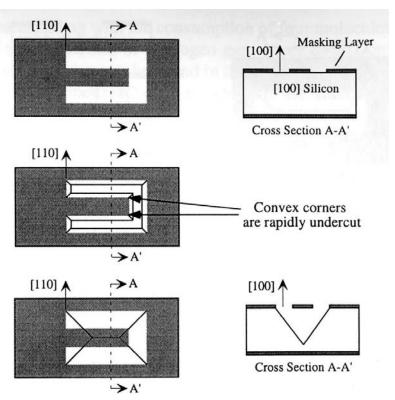
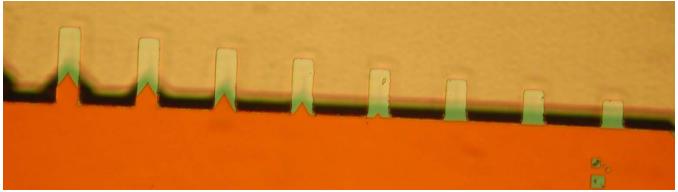


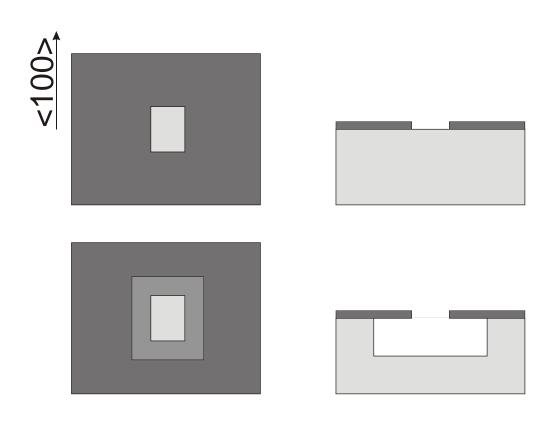
Figure 3.22. A square <110>-oriented mask feature results in a pyramidal pit.

- So far, all the edges between (111) planes have been concave, and these edges are essentially stable in the KOH etch
- However, convex edges are not stable and are efficiently undercut
- The allows the fabrication of free standing structures without the need for a sacrificial layer between the superstructure and the substrate





- Alternatively, structures with vertical sidewalls may be produced by orienting rectangular sides with the <100> directions
 - In this case, the initial etching into the silicon bulk will reveal (100) sidewalls as well as the (100) base
 - All surfaces will be etched at the same rate
 - Therefore, the surface mask will be undercut on all four sides, with the undercut distance being the same as the etch depth to a good first approximation
 - Unlike the previous example, so stable (111) facets are exposed, so this process is not self-limiting



- The following points should be noted regarding anisotropic etching using KOH
 - 1. The highest etch rate is achieved for a 20% solution at ~85° C
 - 2. KOH will efficiently remove most photoresists, and so it is necessary to use a 'hard mask'
 - This involves using a material on the surface of the silicon, such as silicon nitride or silicon oxide, which is first patterned using a standard photoresist
 - 3. KOH will slowly etch most hard mask materials, so if a deep silicon etch is being performed, the hard mask material must be of sufficient thickness to survive the etching process (see Slide 6)

Etch Stops

- If a wet etching process has been well characterised, then it should be possible to etch features of a certain depth knowing the etching rate
 - In practice, this is more difficult than it sounds
 - The effective concentration of the etchant may decrease with use
 - When does the etch begin and end?
 - Some wetting time may be necessary and certainly some etchant removal time
 - Therefore, if the depth of a feature is a critical parameter, some method of precisely controlling the end of an etch – an *etch stop* process – will be necessary

Dielectric etch stop

- Dielectrics, such as silicon nitride, tend to have a reduced etch rate compared to silicon
- A layer may then be introduced underneath the layer to be etched to ensure that the etch terminates at the correct depth
- However, this requires the use of an extra material (and hence deposition step) in the process

• Doping selective etching (DSE)

- Silicon which has been heavily doped with boron to a concentration of ~10²⁶ m⁻³ has a significantly reduced anisotropic etch rate
- Therefore, an etch of a low doped p-type or n-type silicon layer will naturally halt on a heavily boron doped layer, resulting in a very smooth surface
- However, the addition of boron tends to cause a significant intrinsic stress in the silicon, which limits the use of these layers as mechanical components

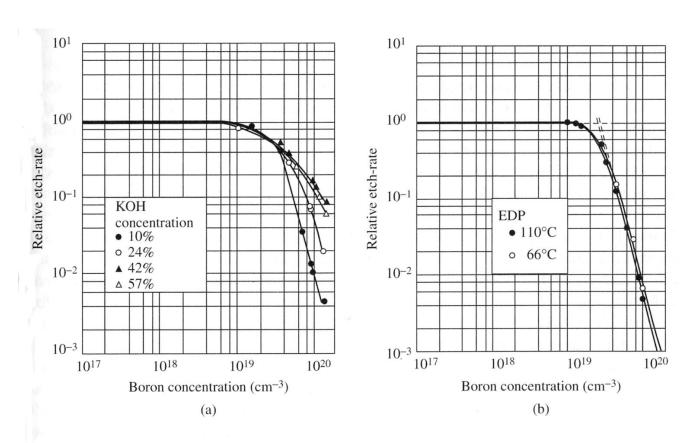
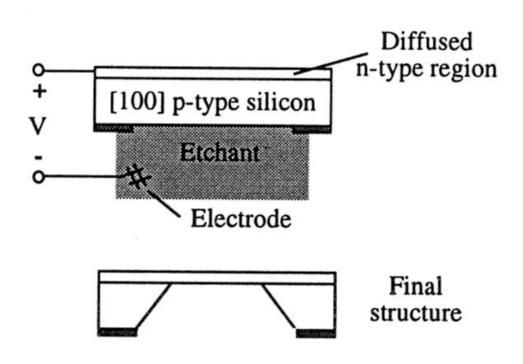


Figure 5.8 Boron etch-stop properties for (a) KOH and (b) EDP etchants

• Bias selective etching (BSE)

- This is otherwise known as an electrochemical etch stop
- A positively biased silicon wafer will be oxidised in an etchant solution to form a protective oxide layer which will prevent etching
- A current is required for the oxide to form, therefore, a reverse biased pn junction in the solution will not be able to form a passivation layer until all of the p or ntype material has been removed
- At this point a current may flow, and the silicon surface will quickly oxidise, stopping the etch at the change in doping density



Dry Etching

- An alternative to wet etching of materials is the use of gas phase etchants
 - These so-called dry etching processes have the advantage that the use of a continuous flow of gas naturally removes unwanted reaction products from the surface
 - It also ensures a constant etch rate, as used etchant is constantly replaced
 - The etching process may be quickly terminated by pumping away the reactant gases, allowing a more accurate determination of etch time
 - Residual gas analysis of the reaction products may be used to determine when a particular layer has been fully etched
 - The danger of surface tension in a liquid breaking mechanical micro-components is removed

Vapour Etching

- Xenon difluoride (XeF₂) is a highly selective vapour etchant for silicon
 - It requires no excitation, and does not etch silicon dioxide or most metals
 - It is an isotropic etch and so may be used in conjunction with sacrificial polycrystalline silicon to produce released surface structures
 - The reaction proceeds according to

$$2XeF_2 + Si \rightarrow 2Xe + SiF_4$$

- Etching normally takes place under a clean vacuum as XeF₂ will react with water, and so the sample should also be dehydrated prior to etching
- The etch takes place at a pressure between 1Torr and the vapour pressure of XeF₂ (~3.8 Torr at 25° C)
- Silicon can be etched at a rate of ~300 nm min⁻¹

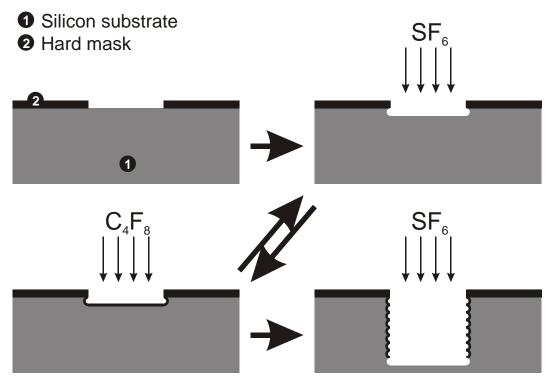
- Reactive Ion Etching (RIE)
- In RIE, the reactant gas is excited to form a plasma which contains the reactive species required to perform the etch
 - The bombardment of the surface top be etched by ions from the plasma can lead to sputter enhancement of the etch rate
 - Although there are many plasma sources for performing RIE, the most common is rf-RIE
 - This system is identical to an rf-PECVD system (as used for a-Si:H deposition – see Lecture 9, Slide 17) however, the substrate is placed on the rf-driven electrode, as the energy of ions impacting this electrode is greater due to its negative self-bias with respect to earth

Material Etch Gas
c-Si, a-Si, poly-Si CF₄, SF₆
Silicon oxide CF₄/H₂
Silicon nitride CF₄/O₂
Organics O₂, O₂/CF₄, SF₆
Aluminium BCl₃

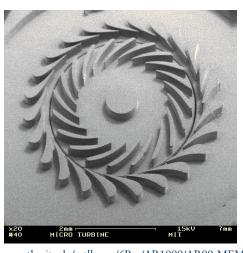
- At high pressures, ions crossing the plasma sheath undergo many collisions, and so strike the etch surface with a broad range of incident angles, and a fairly isotropic etch results
 - SF₆ makes a particularly good isotropic etch for silicon
 - The high pressure also means that the flux of reactant species is high and the etch rate is also increased
- At low pressures, ions are accelerated across the sheath without collision, and so tend to hit the etch surface at close to normal incidence
 - Side walls are therefore only weakly etched, and an anisotropic etch results
 - CF₄ makes a particularly good anisotropic etch for silicon as it also coats the side walls with a protective fluorine polymer, which is only removed by ion bombardment
 - A thin fluorine polymer layer may sometimes be left even on the etched faces at the end of a CF₄ plasma etch, and so O₂ is often added to the gas mixture to remove this polymer layer

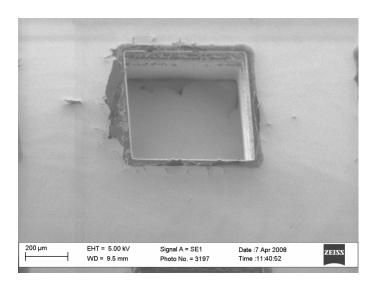
Deep Reactive Ion Etching (DRIE)

- Standard RIE tends to produce etch rates between 10 and 100 nm min⁻¹
 - Whilst this is sufficient for surface micromachining, it is far to slow to allow a layer hundreds of µm thick to be etched
 - DRIE received an impetus thanks to research carried out at Bosch, where a cyclic process involving two important stages was developed for deep isotropic etching
 - In the first stage of the BOSCH process, a dense SF₆
 plasma is used to etch a thin layer of silicon
 - In the second stage, a C₄F₈ plasma is used to deposit a thin fluorine polymer on the etched surface
 - When SF₆ is reintroduced, it preferentially removes the polymer from the bottom of the etch structure, exposing the silicon in this region and allowing the etch to proceed
 - The sidewalls, however, remain protected and are not etched



- In this way, deep structures may be produced with vertical sidewalls at an etch rate of up to 20 μm min⁻¹ in bulk c-Si
- DRIE has enabled the production of a range of new 3D microsystem structures, including the MIT microturbine





http://www-mtl.mit.edu/mtlhome/6Res/AR1999/AR99-MEM.pdf

Other Etching Techniques

- Both dry and wet etching techniques require some means of protecting certain areas of a sample which must not be etched, and this normally requires photolithography
 - However, several techniques exist for removing material without the need for prior patterining
- In ion milling systems, a focussed beam of Ar (or other suitable) ions is directed at a substrate allowing material to be locally removed by sputtering
- In *laser micromachining* systems, a high power laser pulse is focussed on the material to be removed
 - The material is locally heated and sublimes, allowing a structure to be formed
- Whilst such techniques are good for prototyping, direct writing of patterns is slow and not commercially acceptable