

IB Paper 5: Analysis of circuits

Prof C Durkan
cd229@cam.ac.uk

Handout 1 – lectures 1-4
1 *The Bipolar transistor*

The Handout...

Sections marked with an asterisk (*) are included in the course as background/context. Detailed knowledge is not expected.

Recommended Course Books

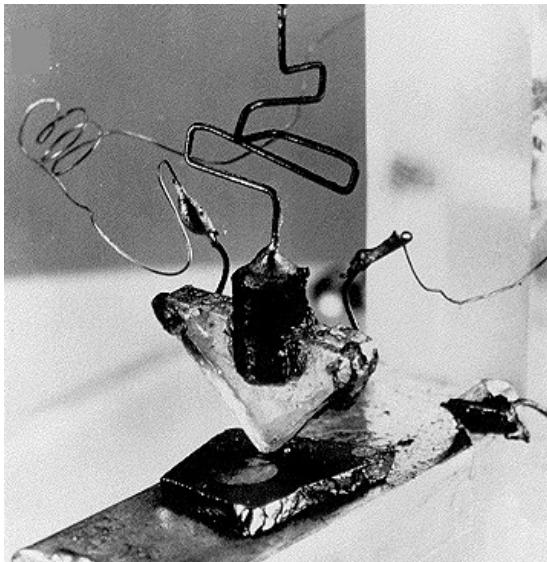
R J Smith & R C Dorf, *Circuits, devices and systems (5th Edition)*, (J.Wiley)

H Ahmed & P J Spreadbury, *Analogue and Digital Electronics for Engineers*, (Cambridge University Press)

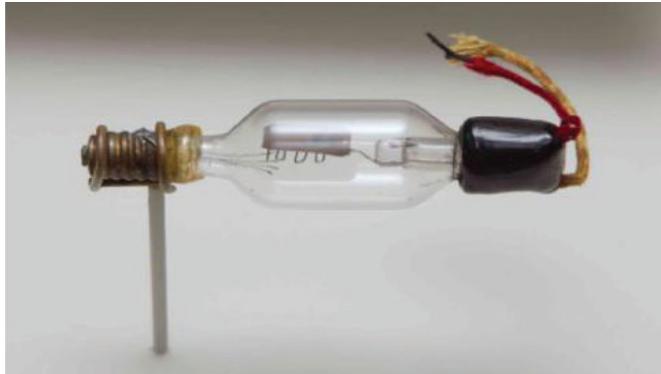
P Horowitz & W Hill, *The Art of Electronics (2nd Edition)*, (Cambridge University Press)

Session 1 - The Bipolar Transistor: Background and DC Properties

The first semiconductor transistor



<http://www.ece.umd.edu/class/enee312-2.S2005/>



The original transistor
“Audion” – 1906

Image courtesy Gregory F. Maxwell

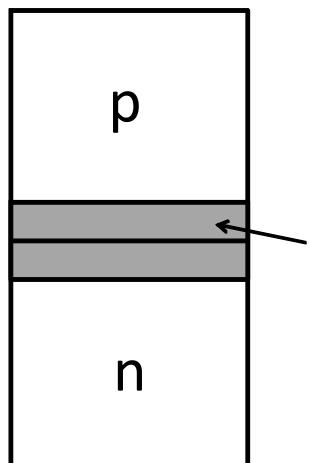
The bipolar transistor was the first solid-state semiconductor transistor, invented on 23 December 1947 by Bardeen, Brattain and Shockley at Bell Laboratories in New Jersey. Experiments with two adjacent diodes showed that a small change in the current in one could induce a large change of current in the other. Interestingly, Bardeen and Brattain had initially been set the task of discovering why earlier attempts to construct a field effect transistor (FET) had failed. In fact many years were to elapse before the fabrication of satisfactory FETs. The transistor was publicly announced in a short article in the 'New York Times' in July 1948 and was described as having 'several applications in radio where a vacuum tube is normally employed'.

The p-n junction -recap

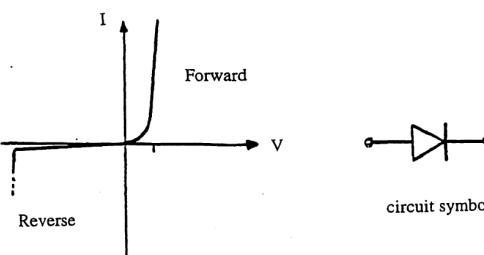
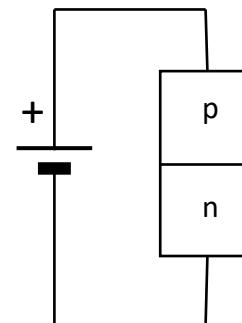
A p-n junction diode is formed by bringing together p-type and n-type silicon. Note that n-type silicon is made by substituting some silicon atoms with atoms of a Group V element. Four of the outer electrons are used in bonding but the fifth is relatively free. Consequently, at room temperature there are many electrons available for conduction in n-type silicon. Arsenic is a commonly used donor impurity.

Similarly, p-type silicon is made by substituting silicon atoms with those of a Group III element. The Group III atoms, having only three electrons in the outer shell, readily accept electrons, leading to a large concentration of 'holes', or absences of electrons, available for conduction. Boron is the normally used acceptor impurity. Silicon contains about 10^{29} atoms/m³ and doping levels range from 10^{23} to 10^{27} atoms/m³.

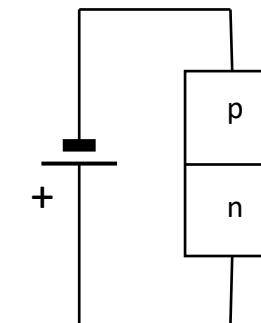
In the region of the junction, holes and electrons recombine to leave a region without any free carriers, known as the depletion region. The charge distribution associated with donor and acceptor atoms in the depletion region that have lost their electrons or holes results in a potential barrier which prevents further flow of holes and electrons into the depletion region.



With forward bias, that is **p-side positive**, the applied field forces majority carriers through the depletion region. The depletion width narrows and current flows, consisting mostly of majority carriers.



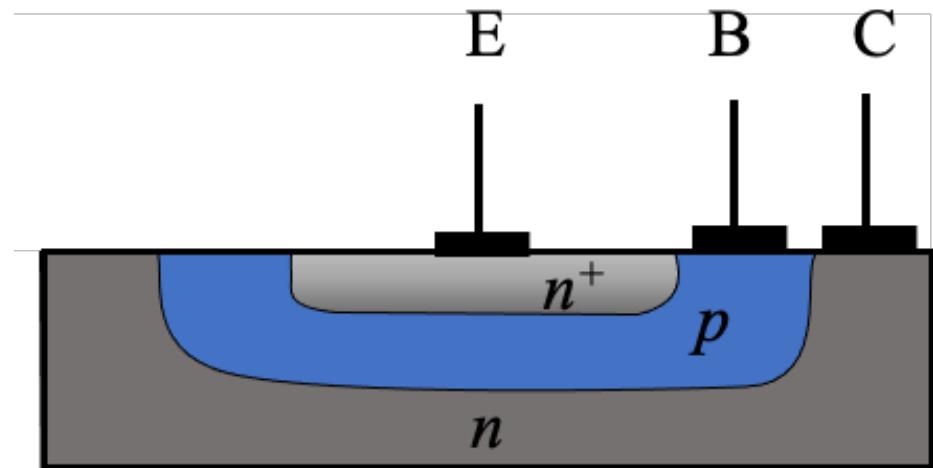
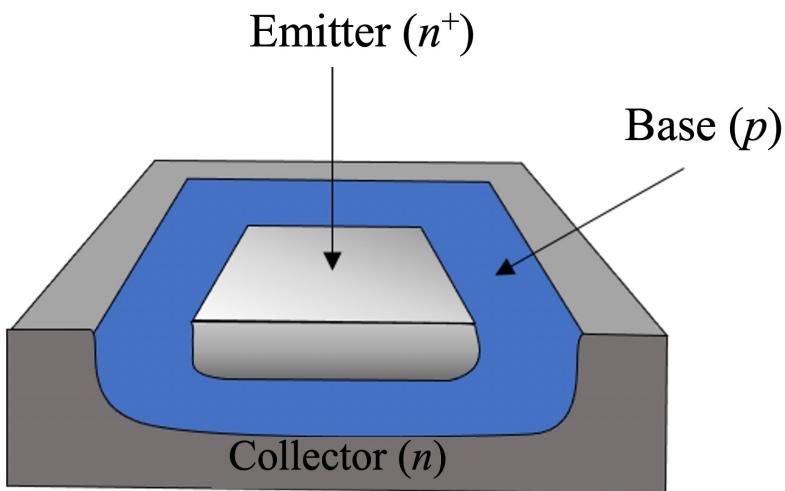
Forward Bias



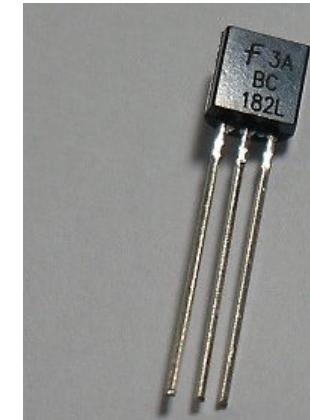
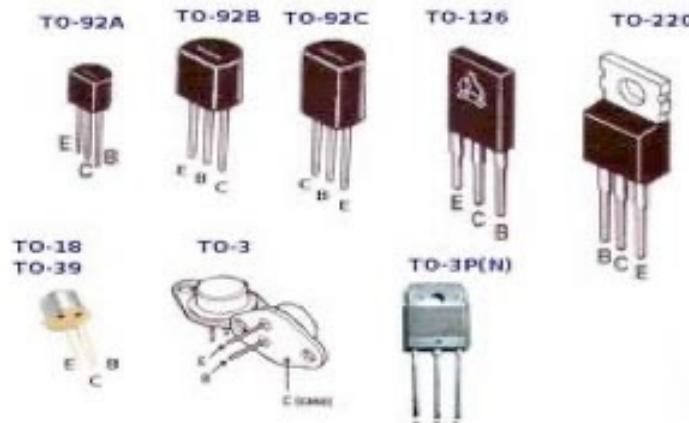
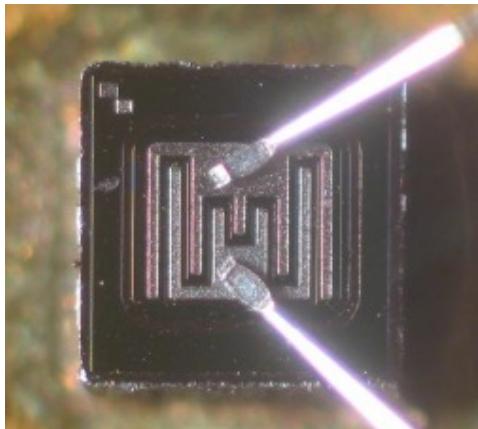
Reverse Bias

Under reverse bias, that is p-side negative, the majority carriers are repelled from the junction and the depletion width widens. A flow of minority carriers, generated thermally, results in a small leakage current. Remember that electrons are the majority carriers in the n-type material and holes are the majority carriers in p-type material.

Construction of the Bipolar Transistor

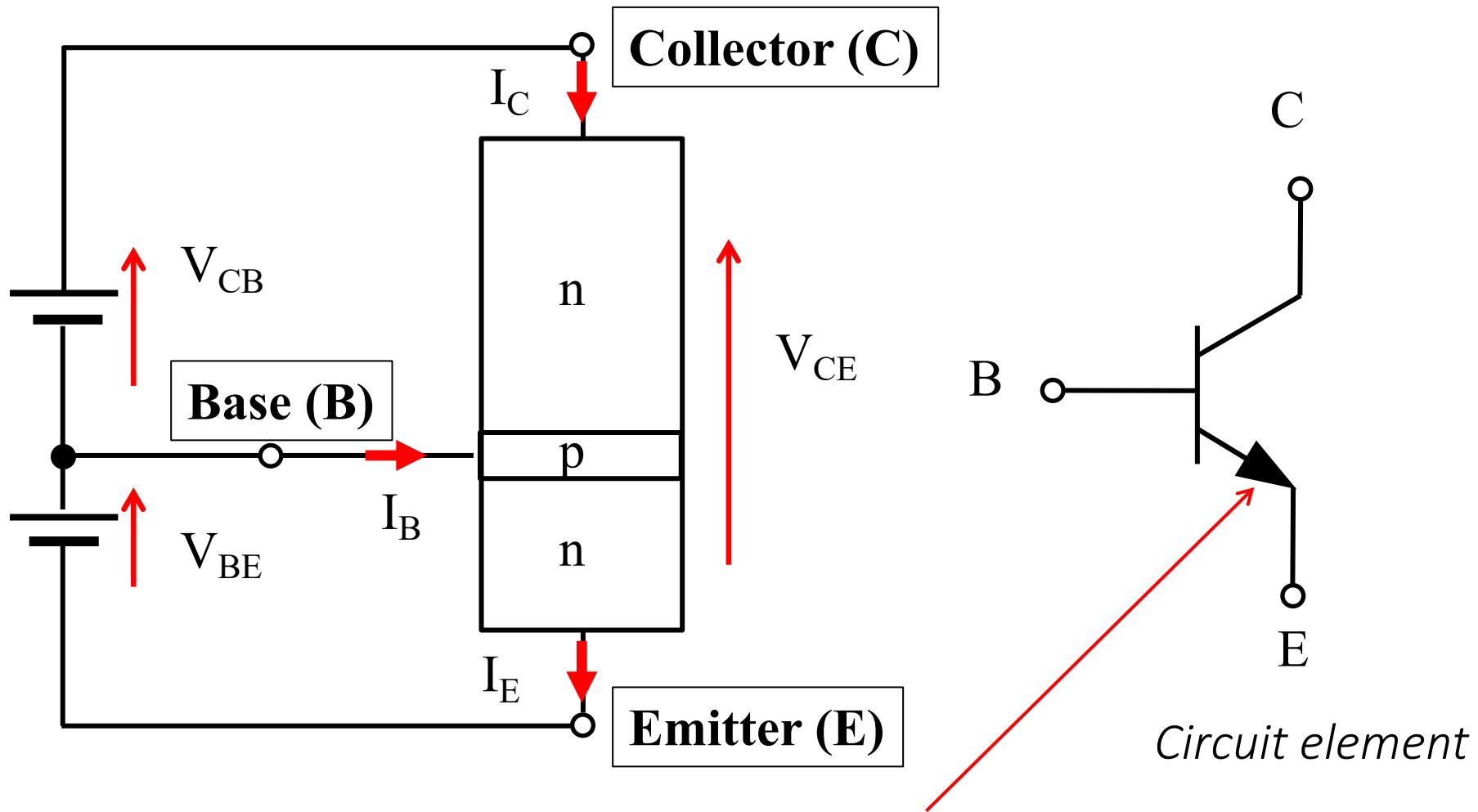


Emitter is **most** heavily doped
Collector is **least** heavily doped



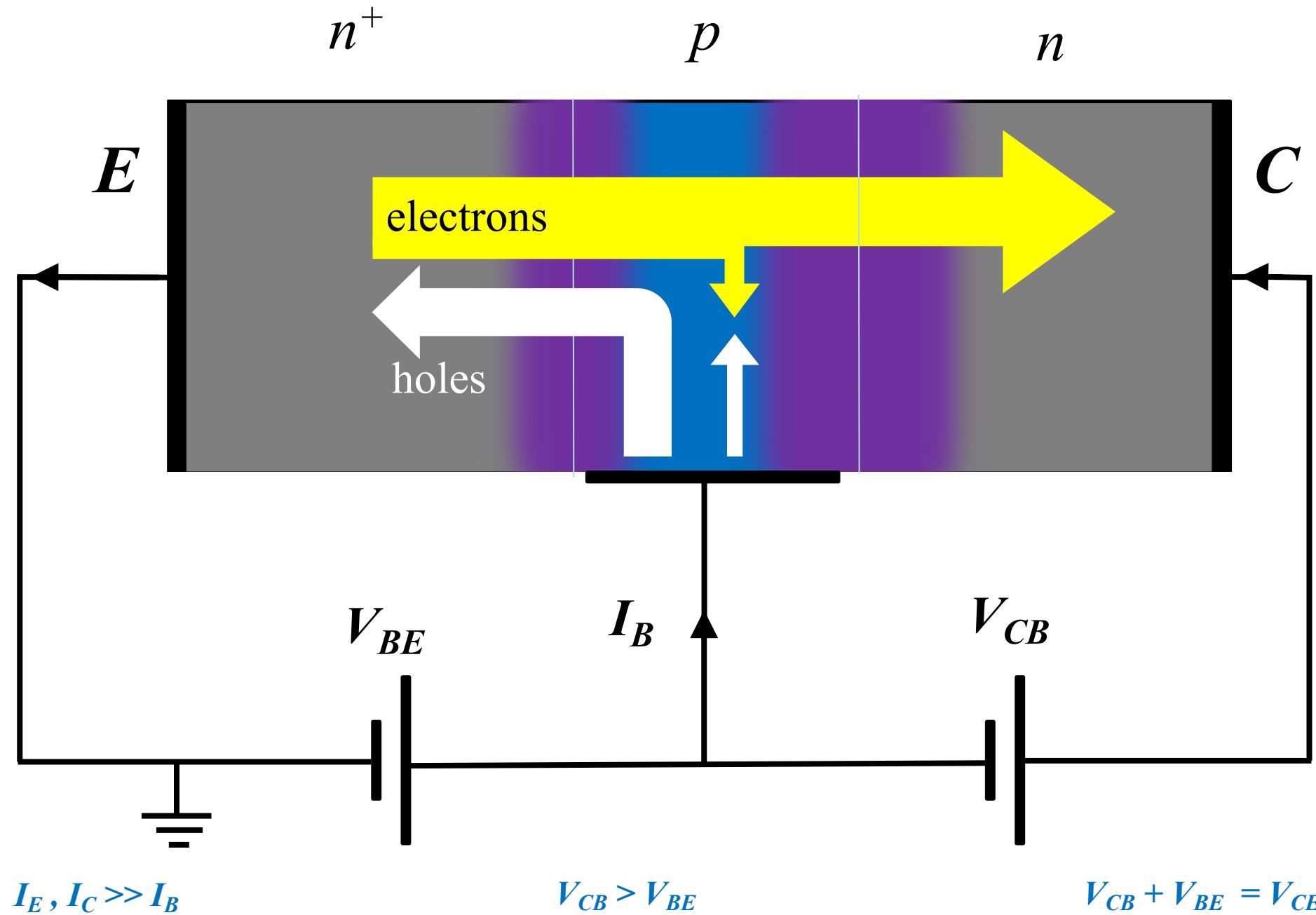
Basics of the Bipolar Transistor

Two diodes back to back ($n - p / p - n$) = npn



The arrow shows the direction of conventional current.
Also can have pnp .

Operation of the Bipolar Transistor



A small change in base voltage, and hence base current, causes a large change in collector current. The collector current *almost* equals the emitter current

The current equations:

$$I_C = \alpha I_E$$

where α is the fraction of I_E reaching the collector. α is called the *common base current gain* and ranges from 0.9 to 0.999.

By Kirchoff

$$I_E = I_C + I_B$$

$$I_C = \frac{\alpha}{1-\alpha} I_B = \beta I_B = h_{FE} I_B$$

$$h_{FE} = \frac{I_C}{I_B}$$

Where β is the (dc) *current gain*, often called h_{FE} .

The current gain, h_{FE} , may range from **20** for a power transistor to **500** for a small-signal device

There is a large degree of uncertainty in this value due to

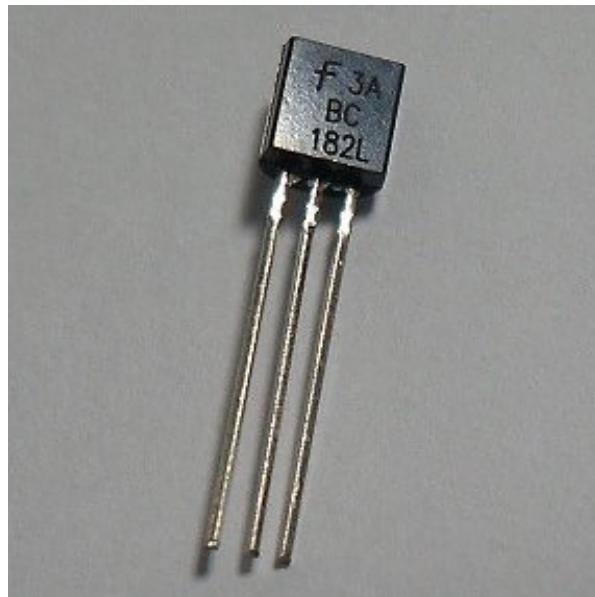
-
-

Please note the use of upper case subscripts to denote dc properties.

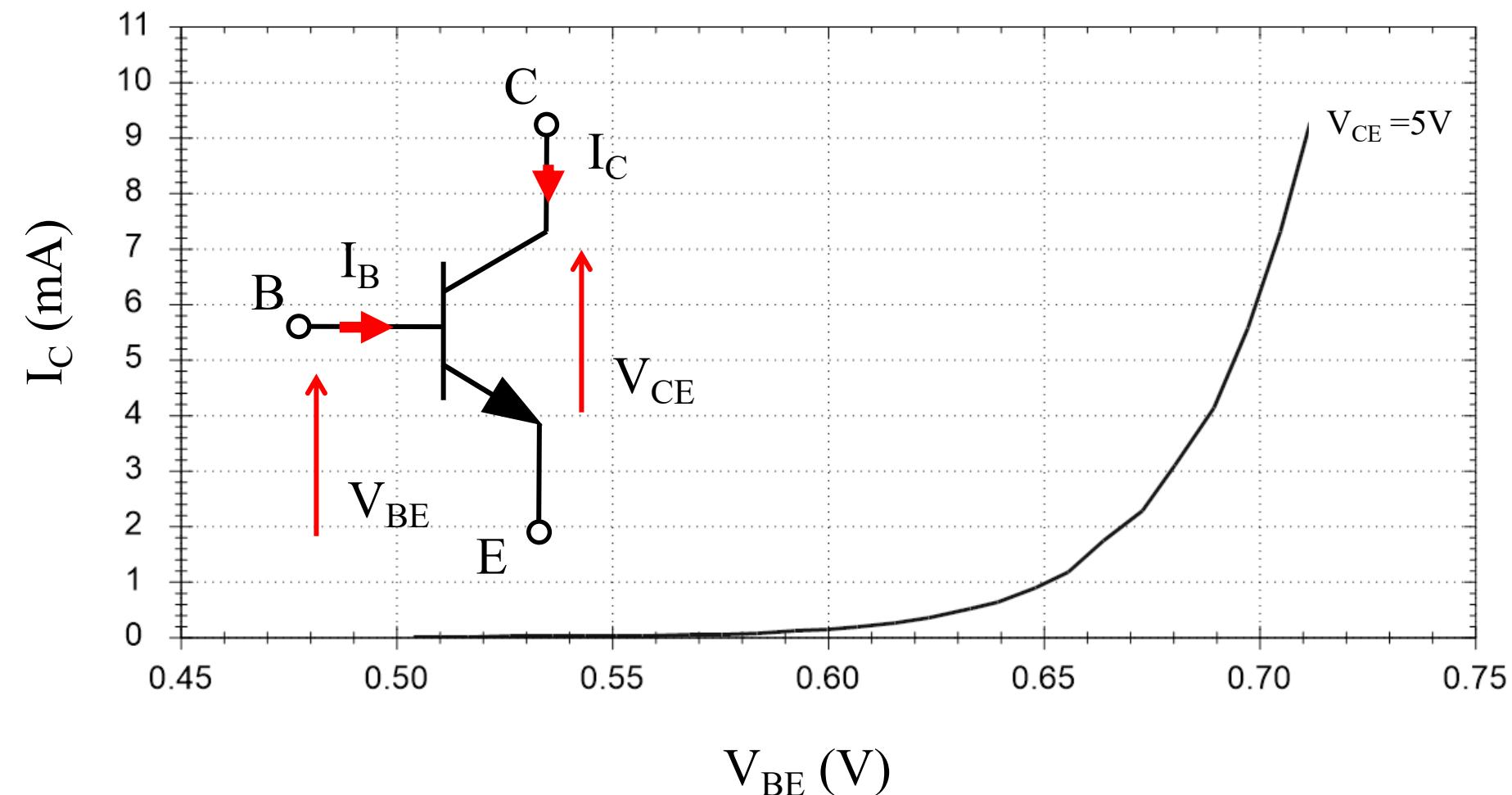
Characteristics of the Bipolar Transistor

There are a series of equations (Ebers-Moll) which govern the dc operation of the transistor, but it is often easiest to represent them in graphical form.

The ones we are using here are for the common npn silicon transistor the BC182L (in the databook)

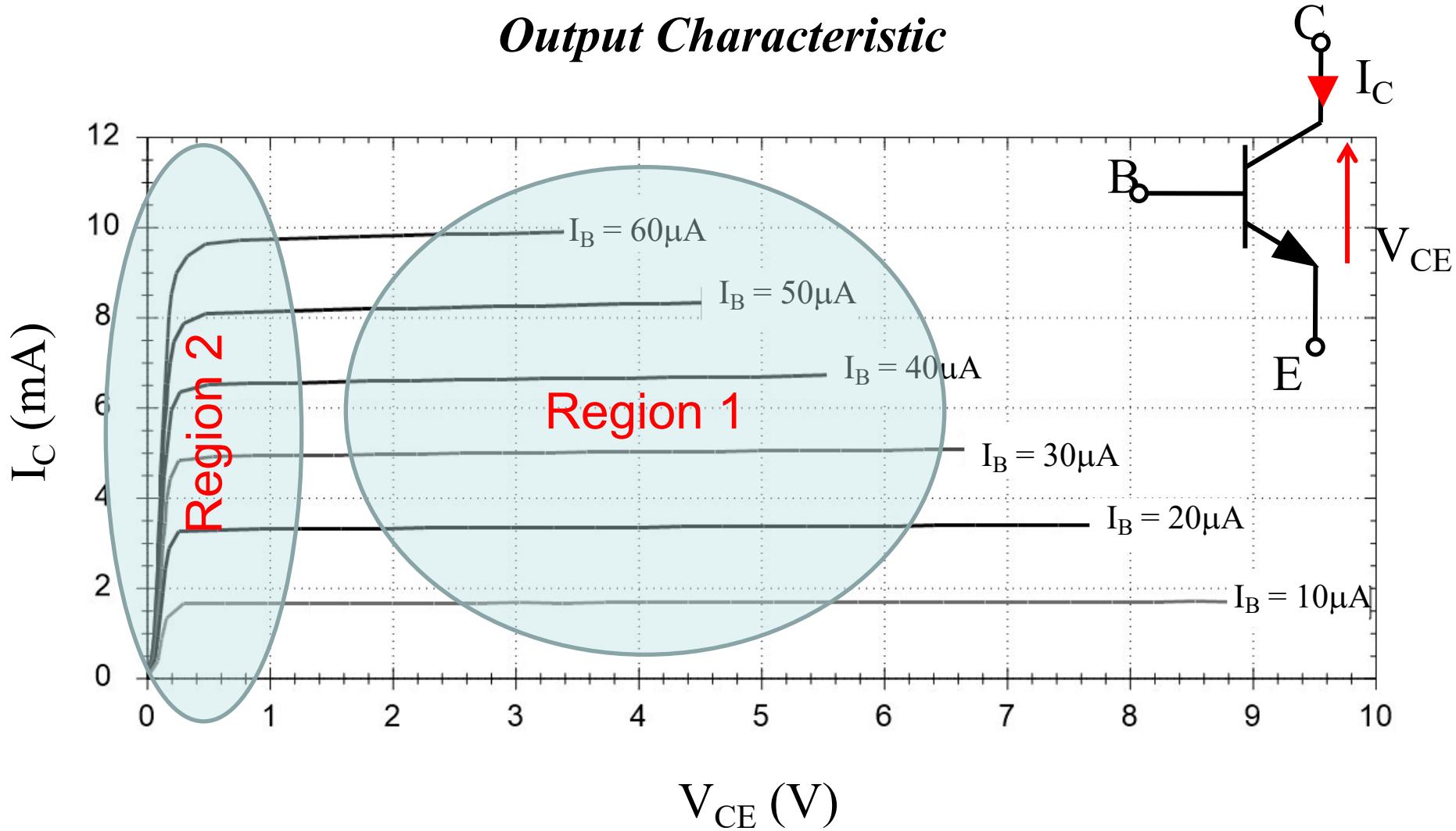


BC182L Input Characteristic



The base-emitter junction begins to conduct at $V_{BE} \sim 0.7V$

Output Characteristic



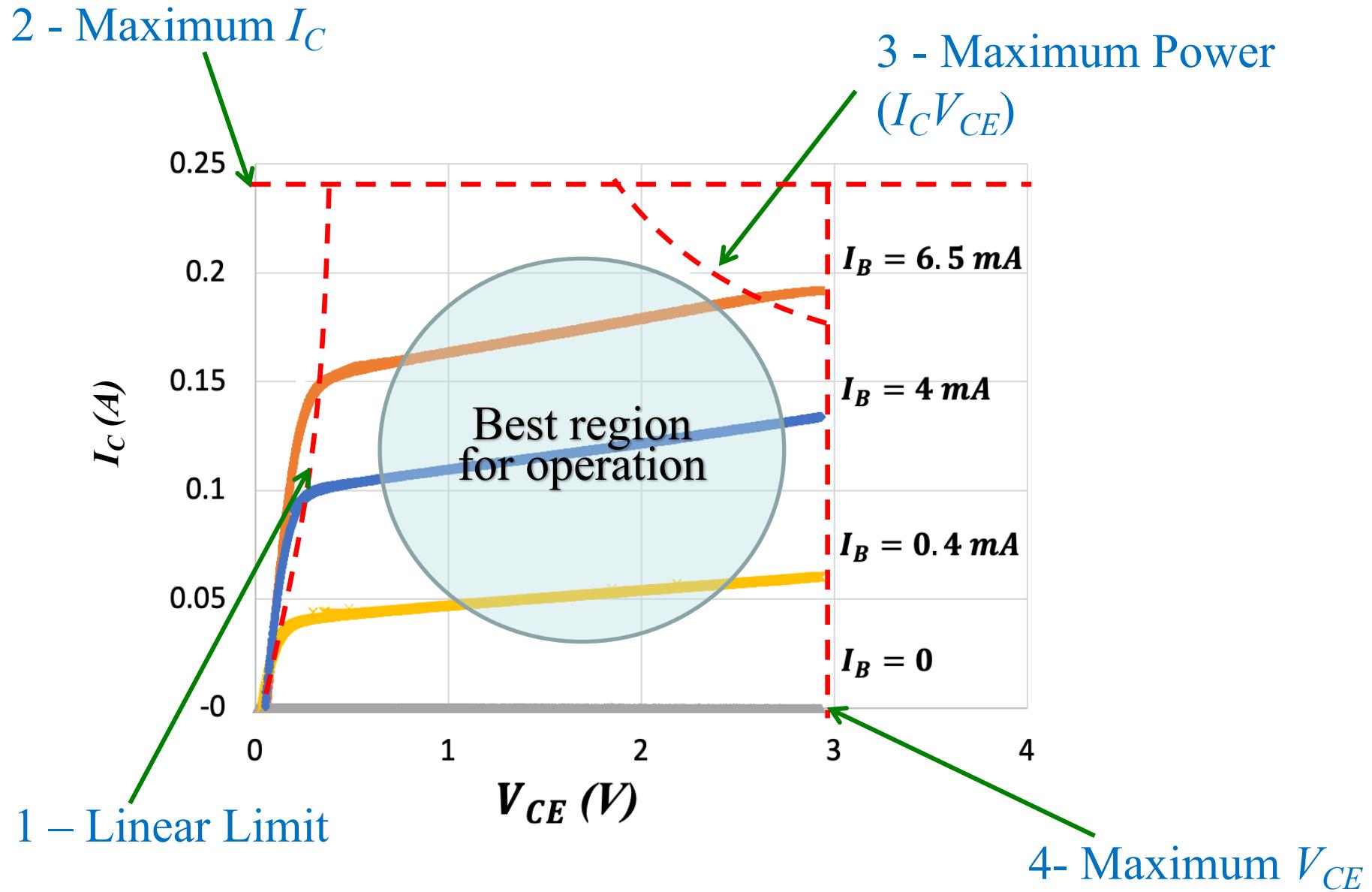
Region 1 I_C depends mainly on I_B and hardly on V_{CE} for $V_{CE} > 2$ V. There is a small rise in I_C with V_{CE} as the collector becomes more efficient

‘Linear’ region - good

Region 2 For $V_{CE} < 2$ V, I_C depends strongly on V_{CE}

‘Nonlinear’ region - bad

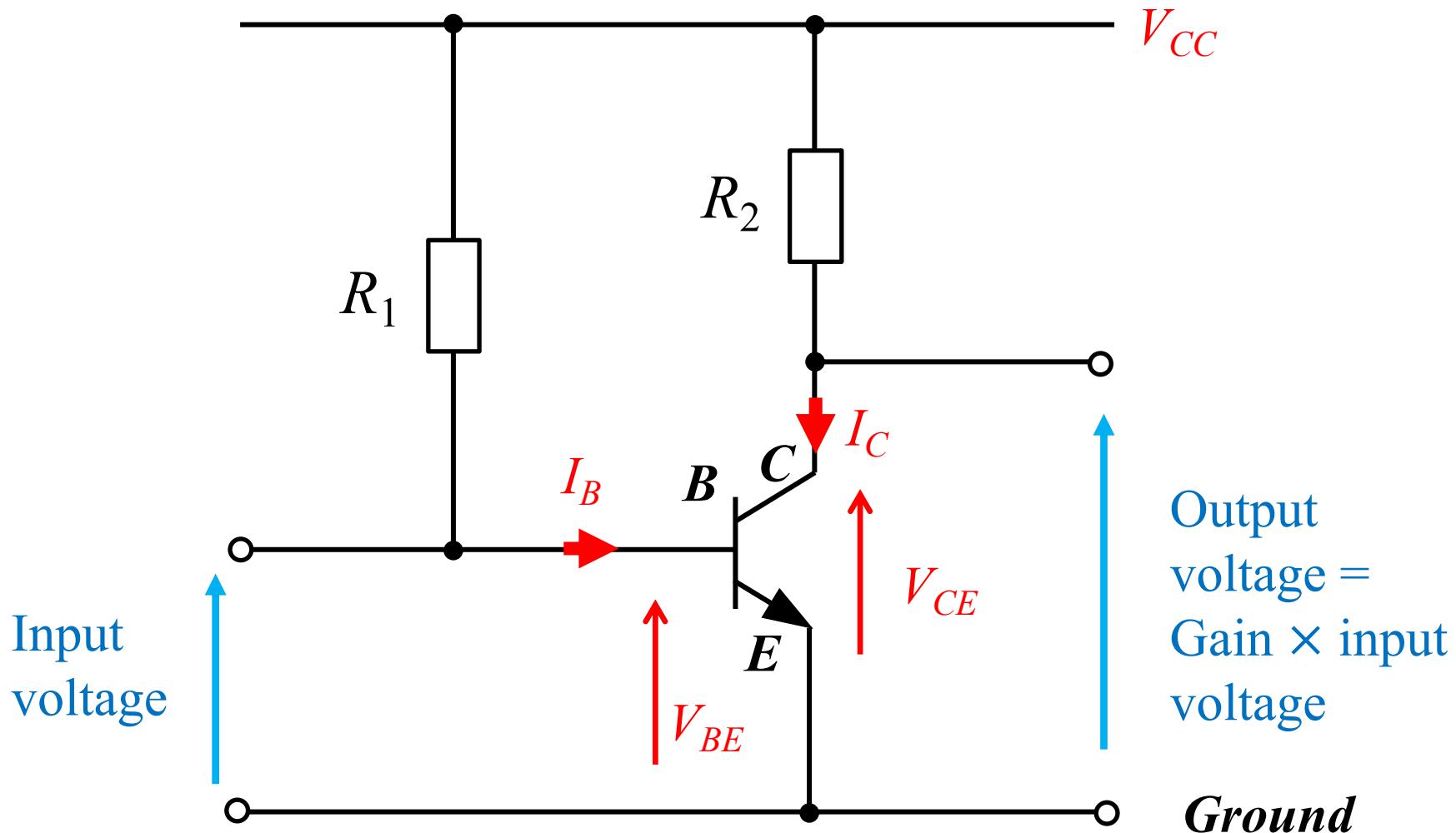
Performance Limits of the Bipolar Transistor



Operating Point for the Bipolar Transistor

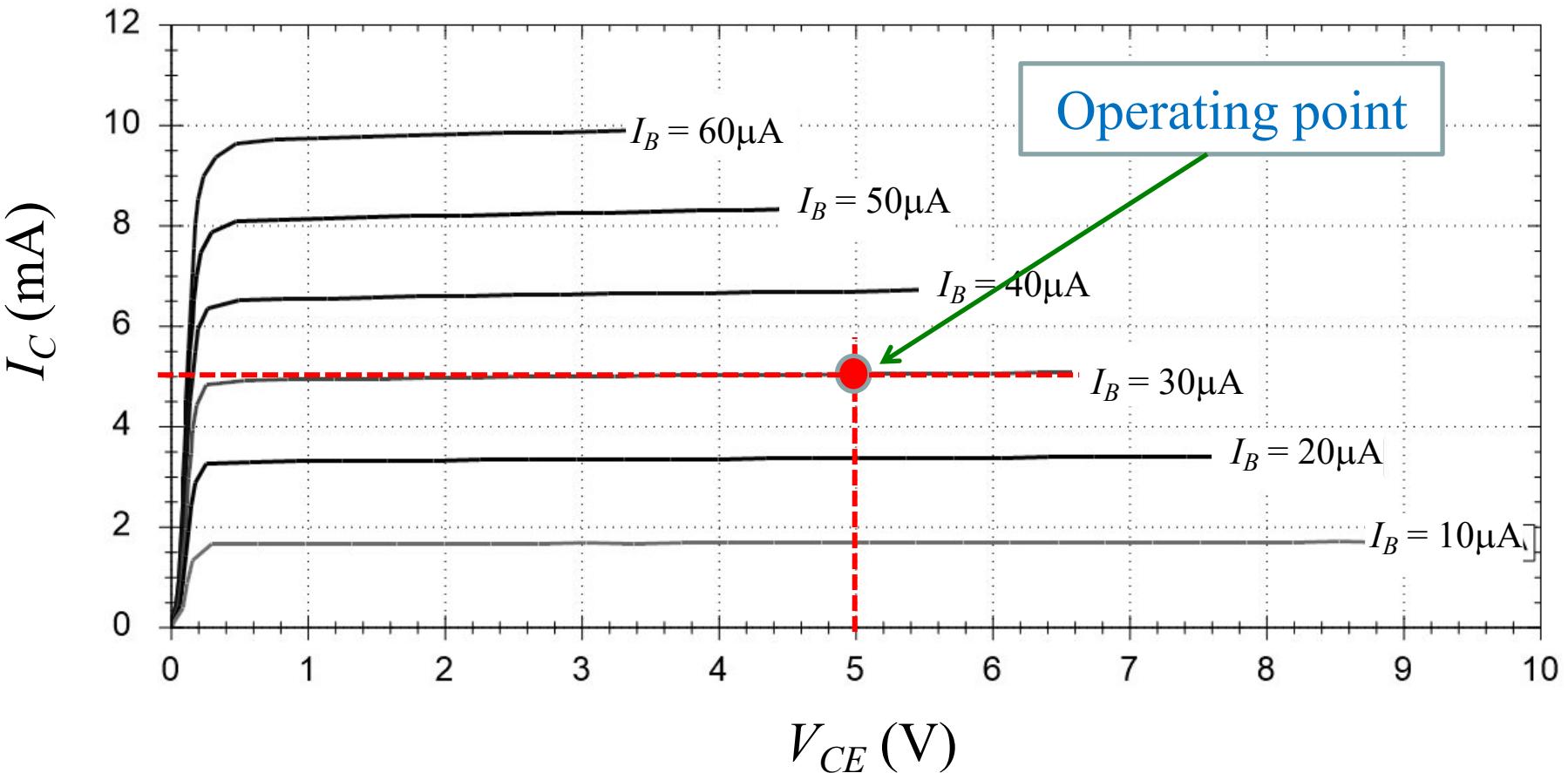
(biasing or *quiescent* – no signals)

Common emitter amplifier:



We choose V_{CE} , I_C and I_B accordingly for linear region

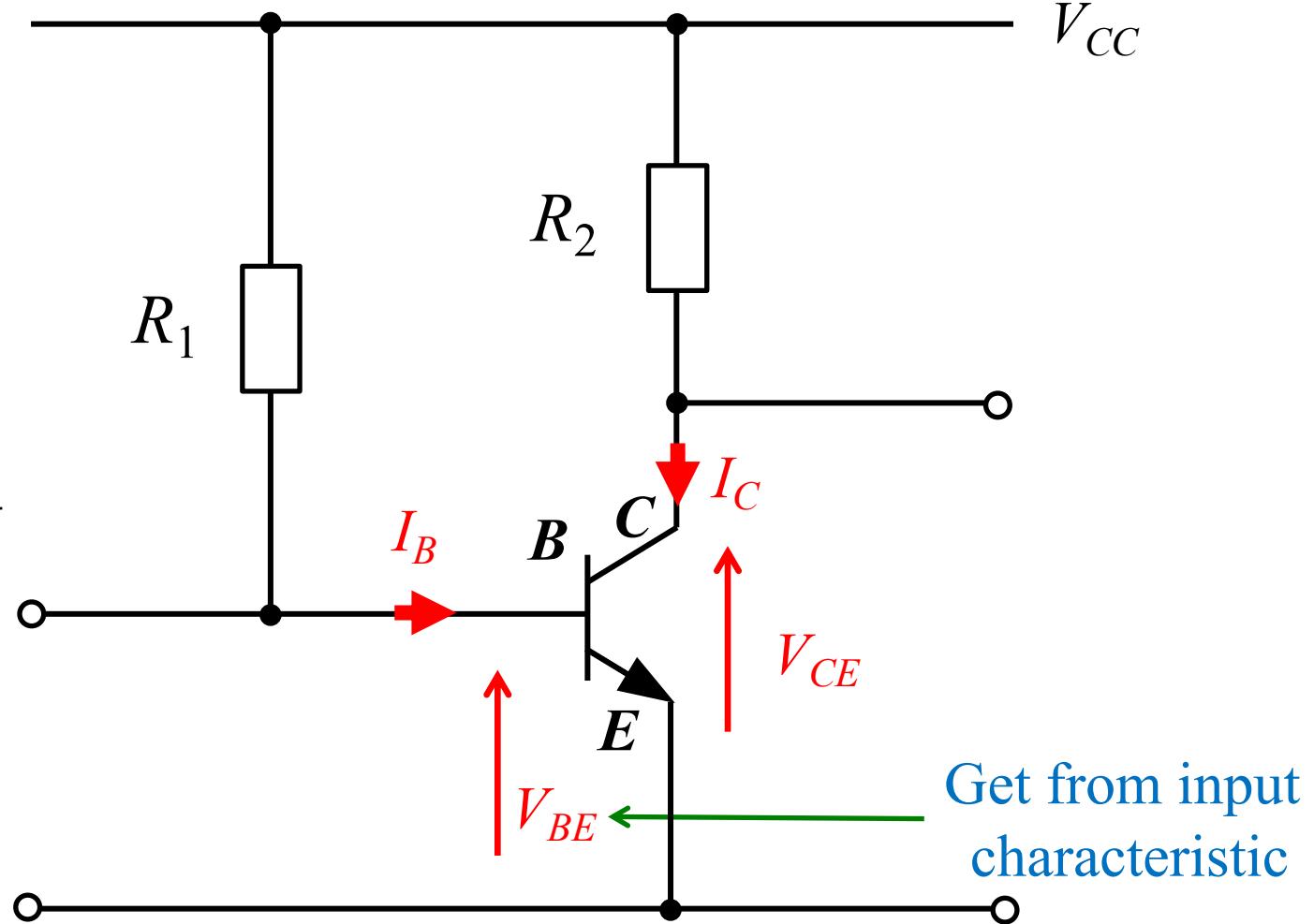
For a $V_{CC} = 10V$, choose operating point
 $I_C = 5mA$, $V_{CE} = 5V$, $I_B = 30\mu A$



From operating point can calculate R_1 and R_2 .

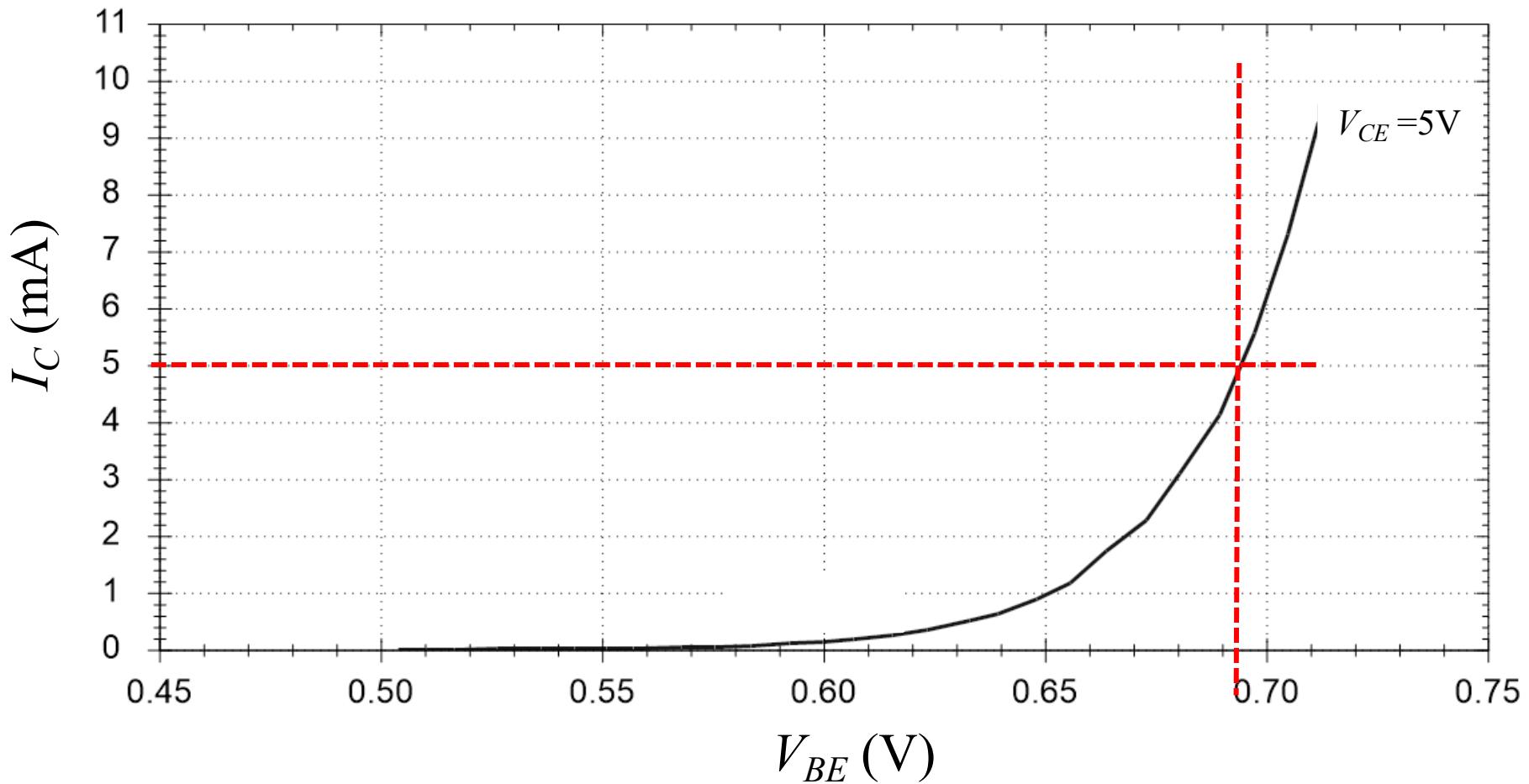
$$R_1 = \frac{V_{CC} - V_{BE}}{I_B}$$

$$R_2 = \frac{V_{CC} - V_{CE}}{I_C}$$



The Input characteristic allows us to calculate V_{BE}

Operating point on input characteristic ($I_C = 5\text{mA}$)

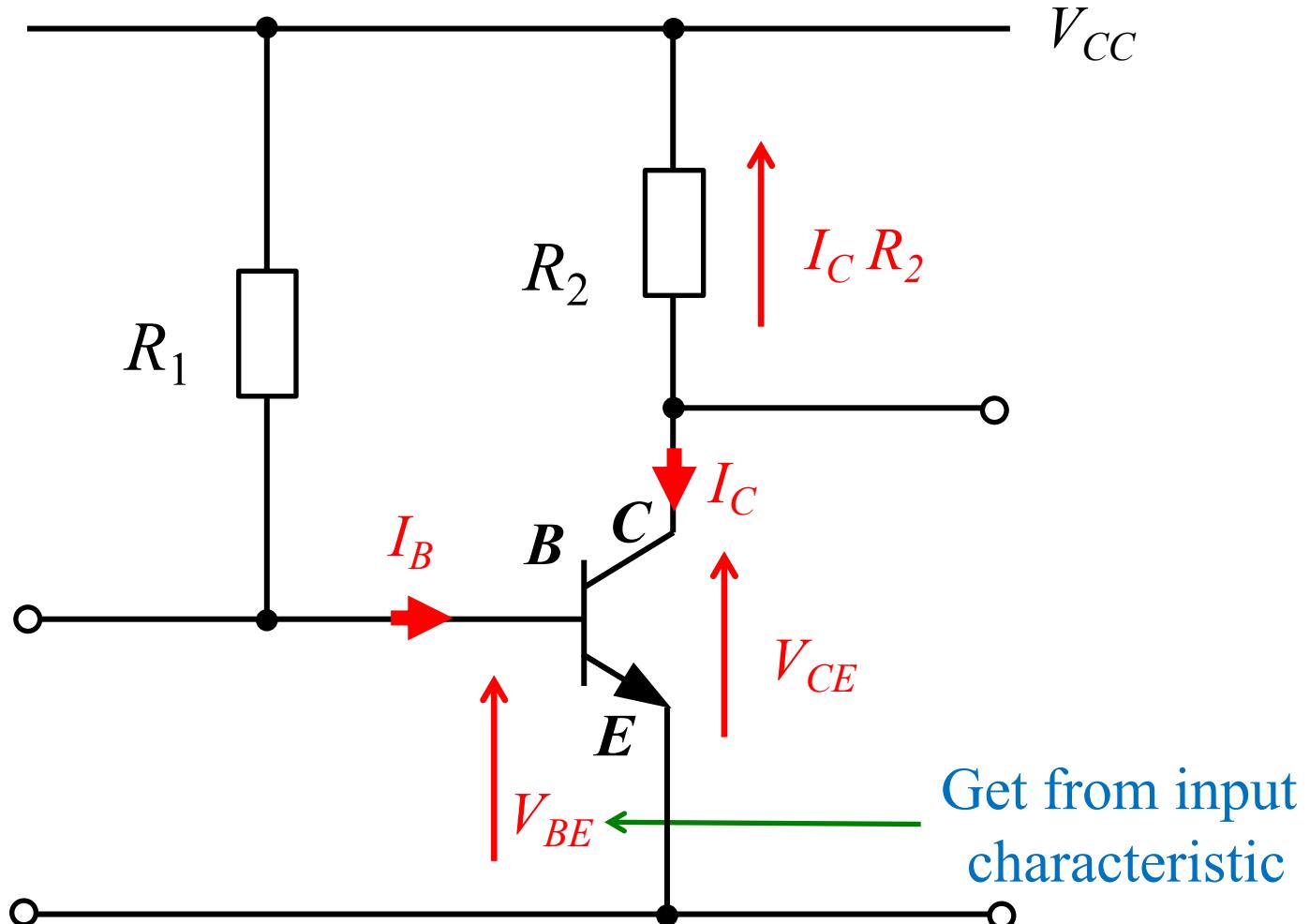


Gives $V_{BE} = 0.69$ (approx) = input voltage

From operating point can calculate R_1 and R_2

$$R_1 = \frac{V_{CC} - V_{BE}}{I_B}$$

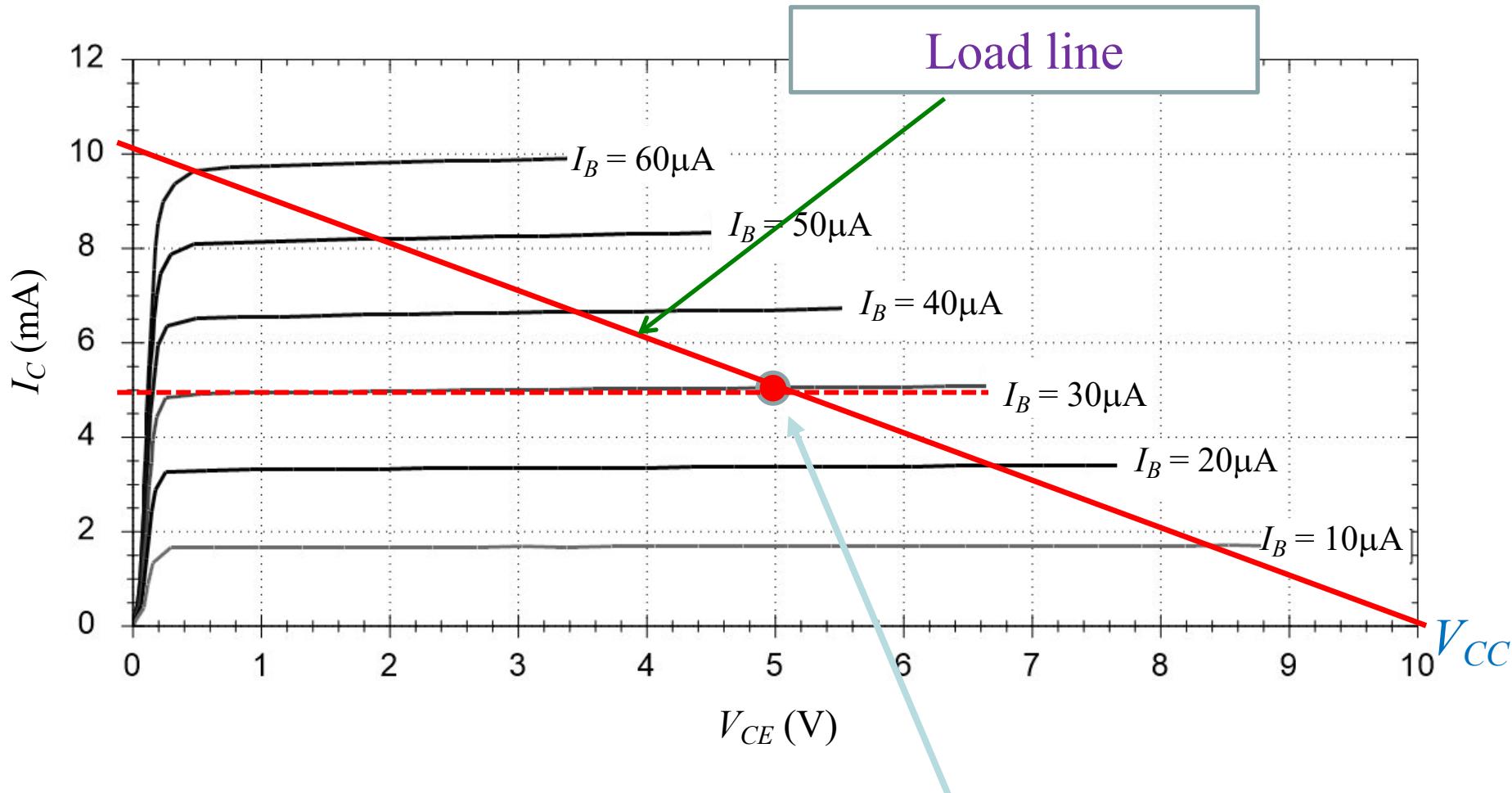
$$R_2 = \frac{V_{CC} - V_{CE}}{I_C}$$



$$I_C R_2 + V_{CE} = V_{CC}$$

Plot load line on the output characteristic (I_C vs V_{CE})

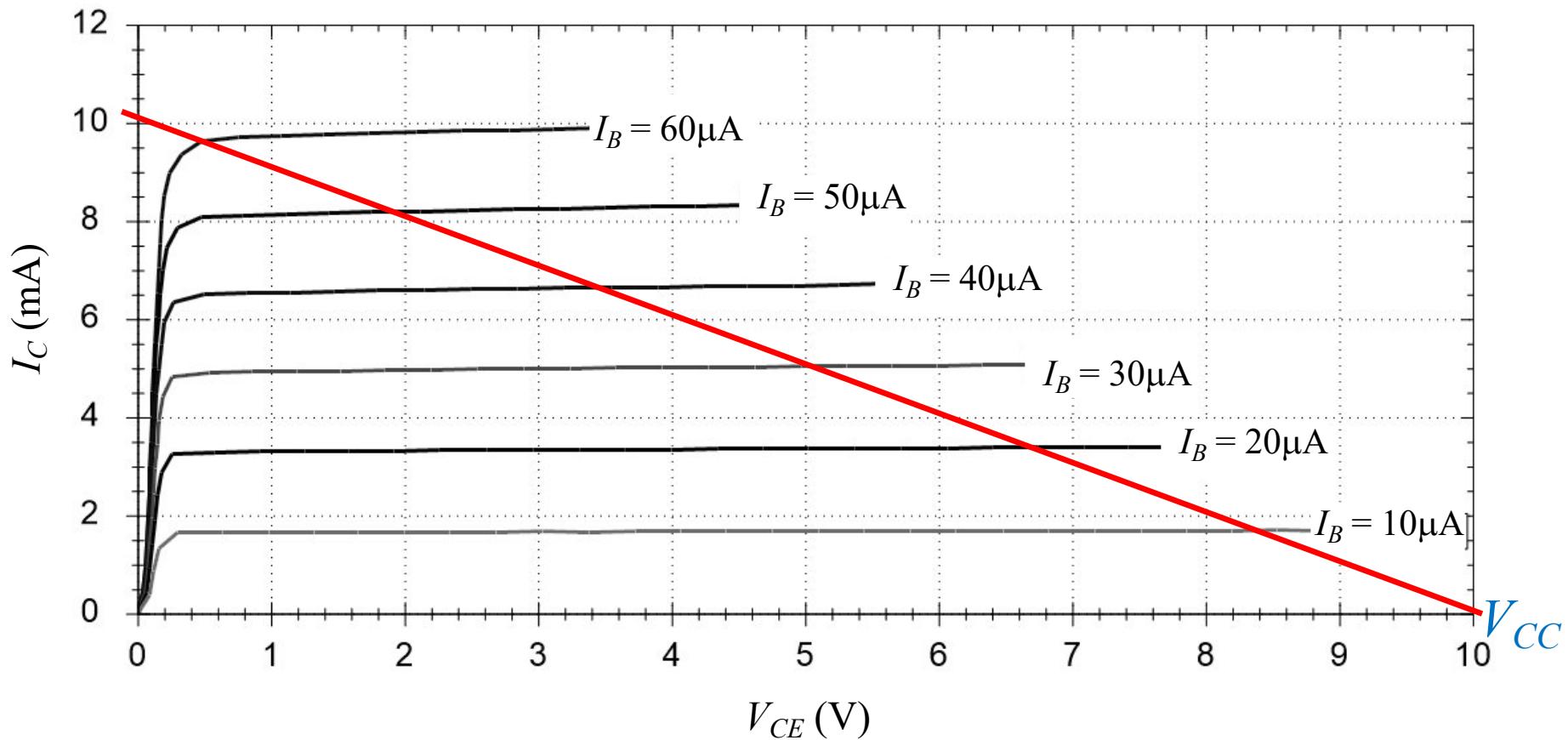
e.g. For $V_{CC} = 10V$, choose operating point
 $I_C = 5mA$, $V_{CE} = 5V$, $I_B = 30\mu A$



$$I_C R_2 = V_{CC} - V_{CE}$$

Operating point, P

Can now graphically estimate the gain

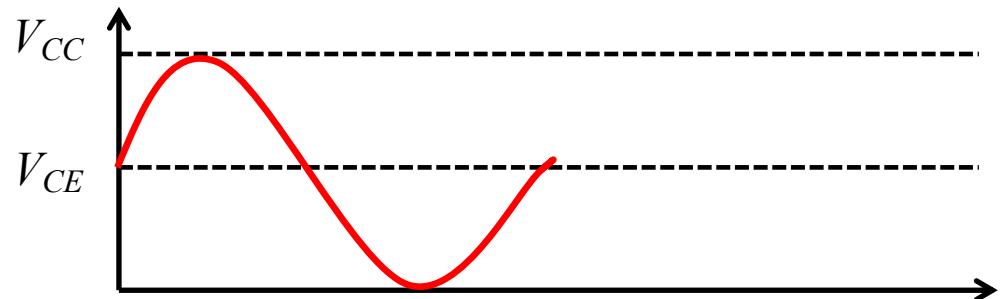


Current gain $\left(\frac{\Delta I_C}{\Delta I_B}\right)$ Vs voltage gain $\left(\frac{\Delta V_{CE}}{\Delta V_{BE}}\right)$

General procedure for the selection of an operating point:

1. Stay within safe limits
2. Ensure that the maximum permitted value of I_C is not exceeded.
3. Choose the highest allowable V_{CC}
4. Try to set V_{CE} as close to $V_{CC}/2$ as possible
5. Draw the load line to have the maximum length in the linear region.

V_{CE} = output voltage



It is usual for this procedure to be iterative. In the present example the value of the load resistor, R_2 , is obtained from choice of I_C at point P.

At the operating point $I_B = 30 \mu\text{A}$

$$R_2 = \frac{V_{CC} - V_{CE}}{I_C} = 1 \text{ k}\Omega$$

From the input characteristic $V_{BE} = 0.69 \text{ V}$



To find the base resistance, R_1 , note that

<https://www.sparkfun.com/products/13760>

$$R_1 = \frac{V_{CC} - V_{BE}}{I_B} = 277 \text{ k}\Omega$$

(E12 Value 270 k Ω)

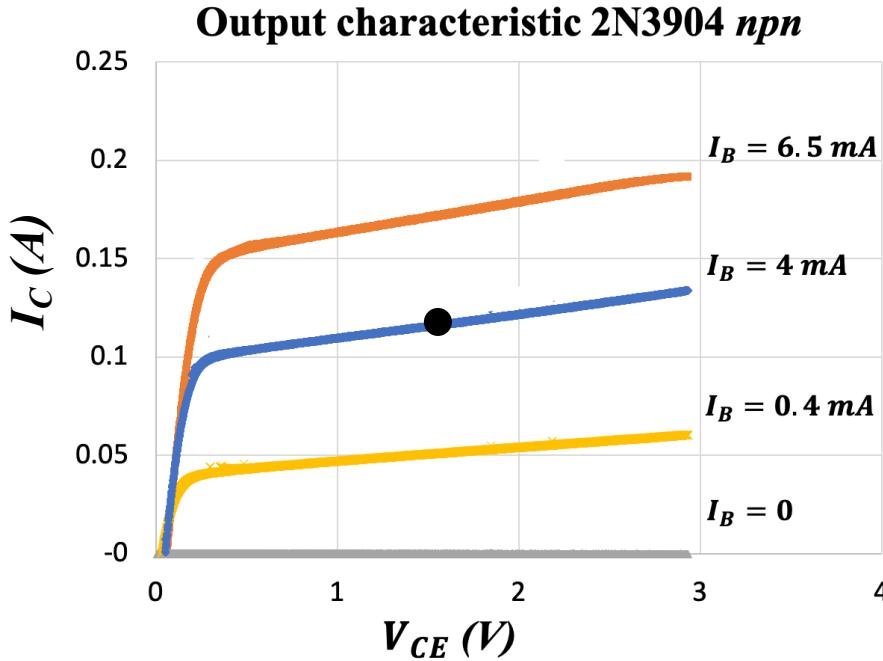
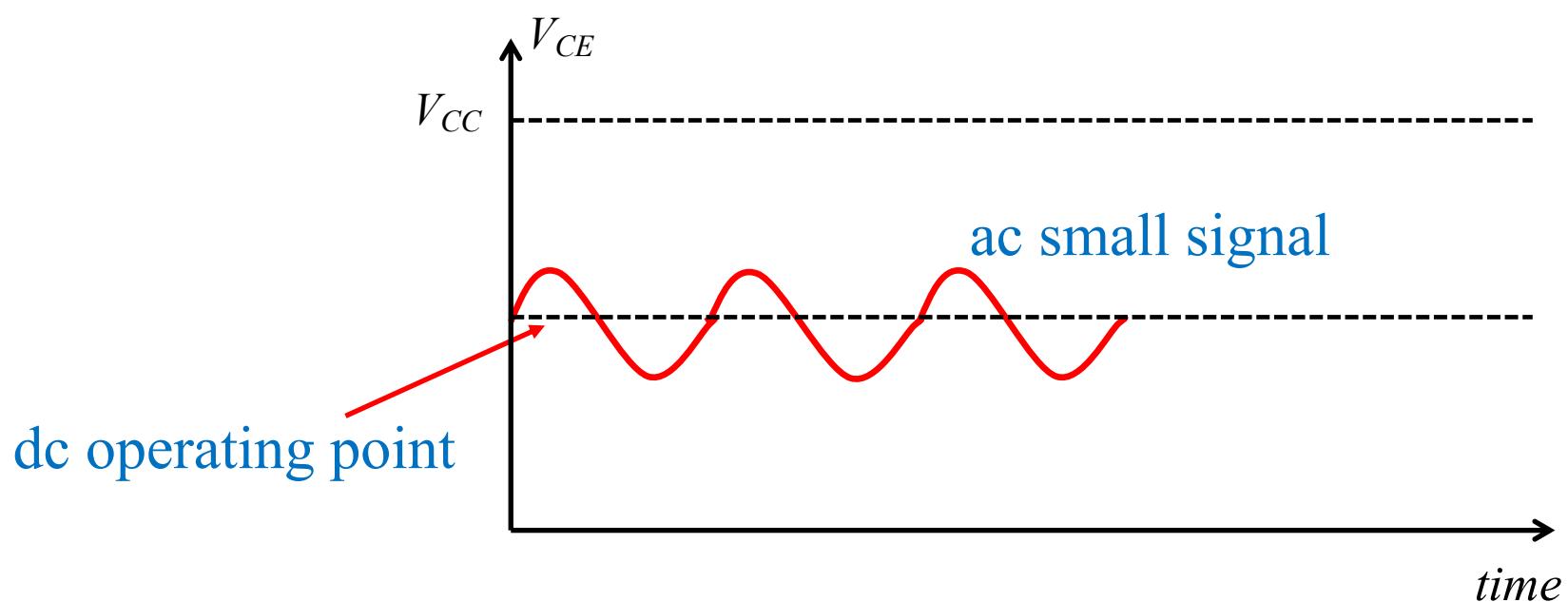
Now try
Example
Paper 1
Q1 & Q5
(i)-(ii)



IB Paper 5: Analysis of circuits

Prof C Durkan
cd229@cam.ac.uk

2 *Small-signal model of the BJT*



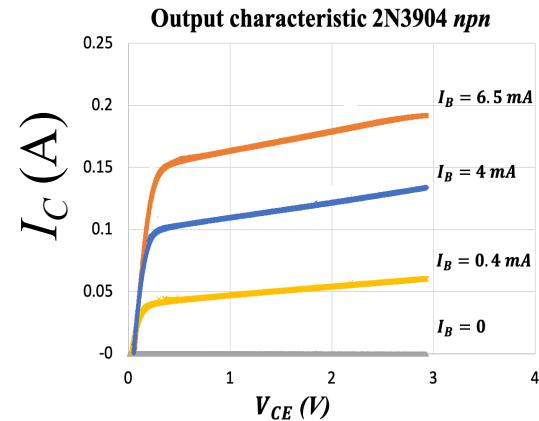
I_C changes when we change V_{CE} and I_B .

We want a linear model for the transistor to be able to analyse circuits. The device characteristics are linear for small changes about an operating point P. Therefore we can use values of parameters appropriate to that operating point and forget the actual dc conditions at the operating point. Graphical techniques are ok for the output but not accurate enough for small changes at the input.

NB lower case subscripts denote small signal (ac) quantities

At the **output** Small change in I_C due to I_B and V_{CE}

$$\partial I_C = i_c = \frac{\partial I_C}{\partial I_B} \Big|_{V_{CE}} \partial I_B + \frac{\partial I_C}{\partial V_{CE}} \Big|_{I_B} \partial V_{CE}$$



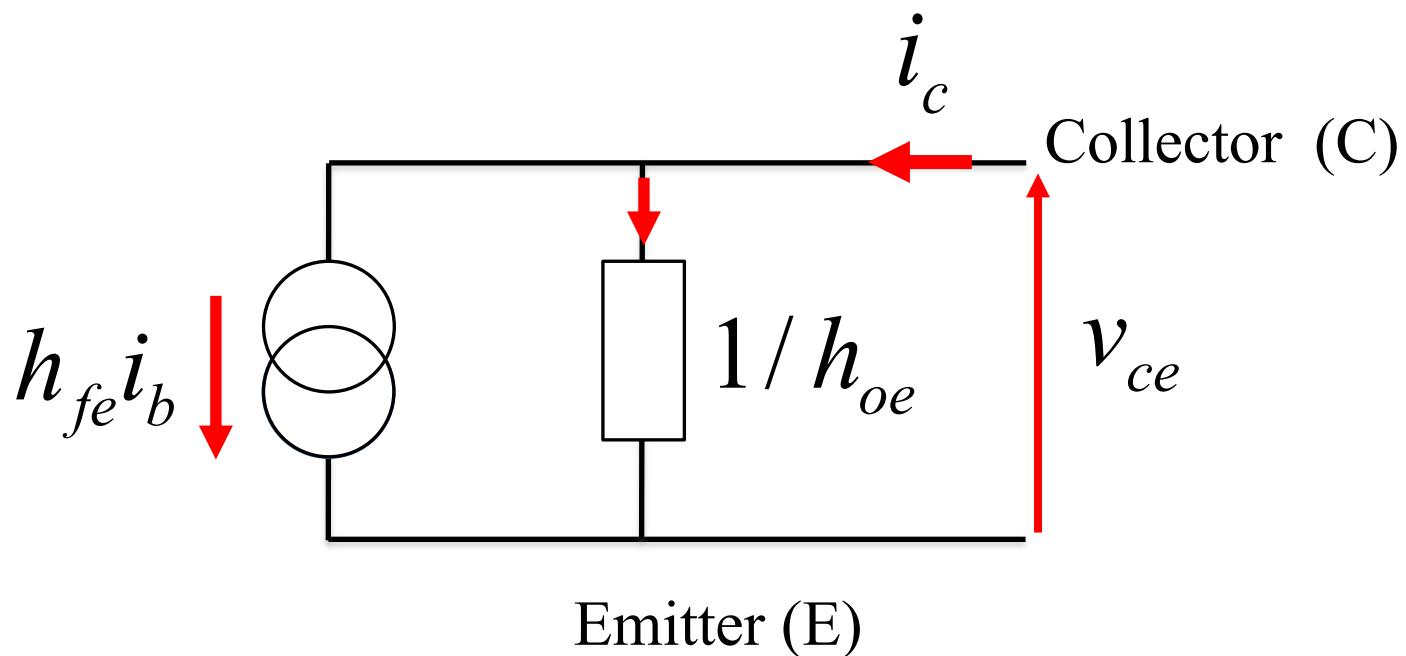
Where $\frac{\partial I_C}{\partial I_B} \Big|_{V_{CE}}$ is the current gain at constant V_{CE} $= h_{fe}$

and $\frac{\partial I_C}{\partial V_{CE}} \Big|_{I_B}$ is the output admittance at constant I_B $= h_{oe}$
1/impedance

We can write this as:

$$i_c = h_{fe} i_b + h_{oe} v_{ce}$$

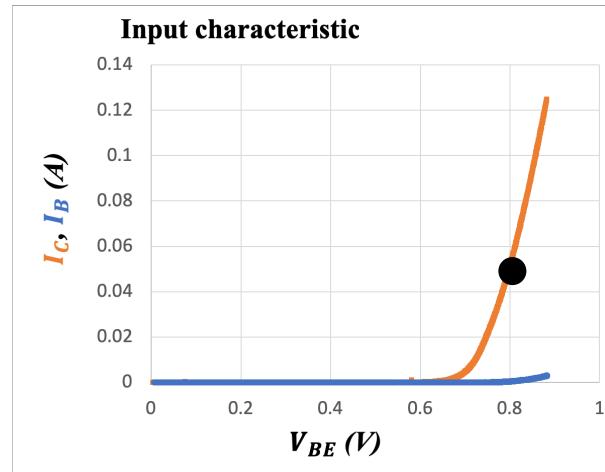
Which suggests a model with a current generator and a conductance



In a good transistor, $h_{oe} \sim 0$

The input is applied to the base-emitter junction which has the characteristic of a forward-biased diode. The exact shape of the characteristic varies a little with V_{CE}

$$\partial V_{BE} = v_{be} = \frac{\partial V_{BE}}{\partial I_B} \Big|_{V_{CE}} \partial I_B + \frac{\partial V_{BE}}{\partial V_{CE}} \Big|_{I_B} \partial V_{CE}$$



V_{BE} changes when we change I_B and V_{CE} .

$\left. \frac{\partial V_{BE}}{\partial I_B} \right|_{V_{CE}}$ is the input resistance at constant V_{CE} = h_{ie}

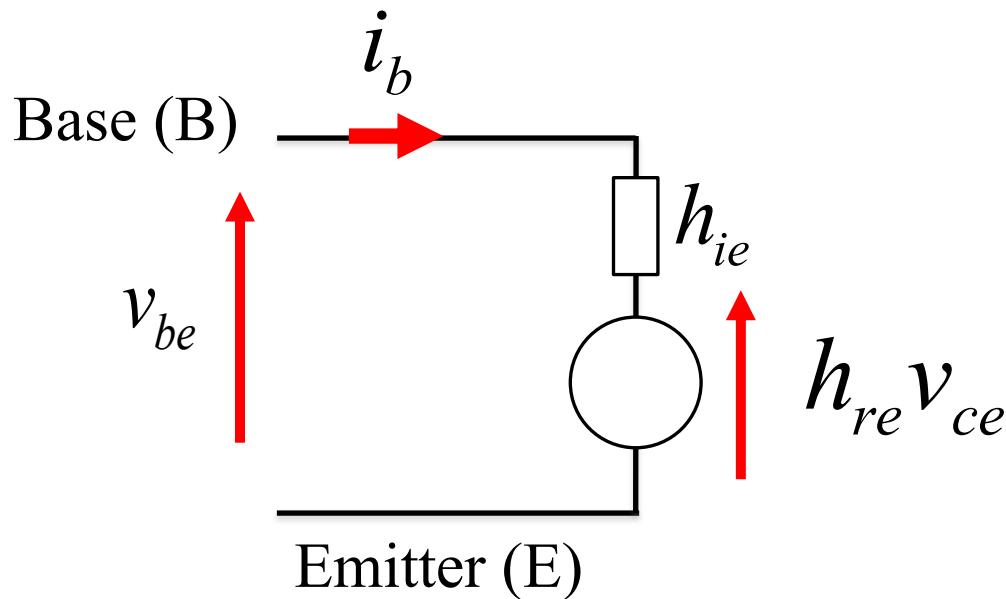
$\left. \frac{\partial V_{BE}}{\partial V_{CE}} \right|_{I_B}$ is the reverse voltage transfer ratio at constant I_B = h_{re}

(Usually negligible)

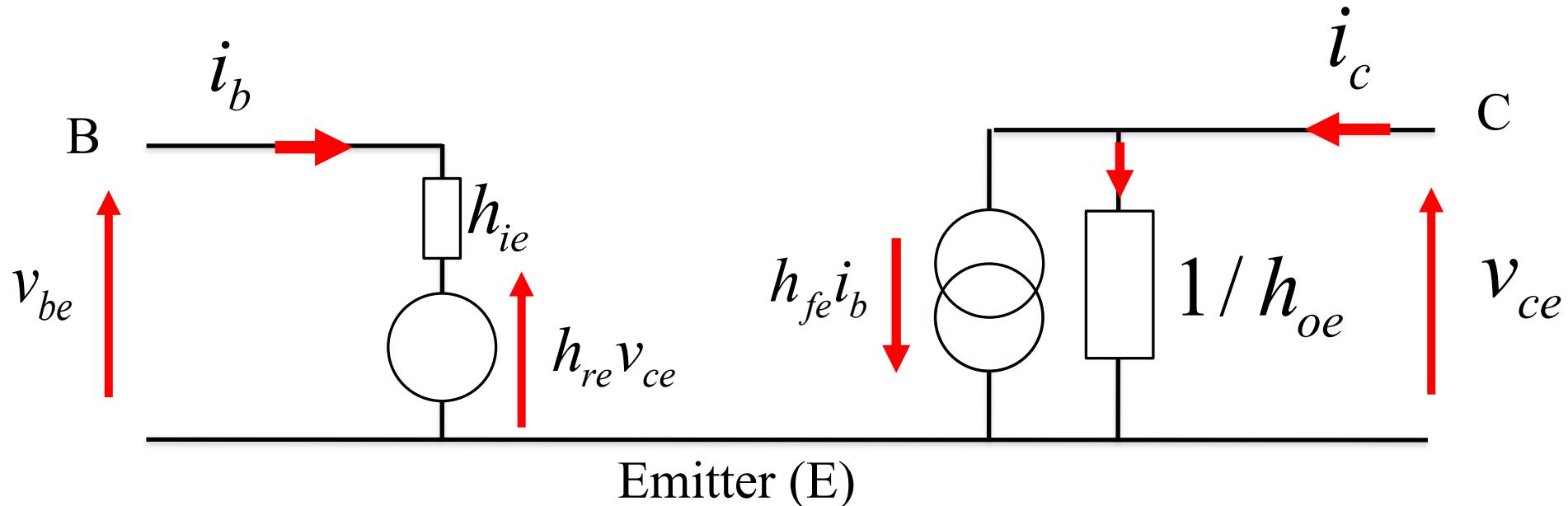
We can write this as:

$$v_{be} = h_{ie} i_b + h_{re} v_{ce}$$

Which suggests a model involving a resistance and a voltage generator.



Overall small signal circuit (as in the Electrical Data Book)



h_{ie} input resistance a few $\text{k}\Omega$

h_{re} reverse voltage transfer ratio negligible (~ 0)

h_{fe} forward current gain (50 – 600)

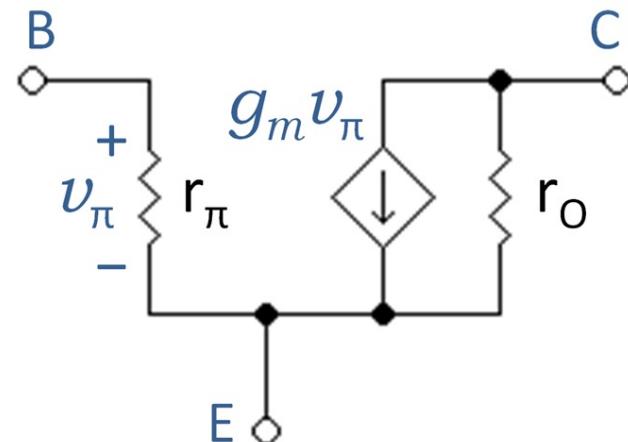
h_{oe} output conductance $1/h_{oe} \sim 50 - 200\text{k}\Omega$

Also works for *pnp* – everything is reverse polarity

The reverse voltage transfer ratio, h_{re} is almost invariably ignored.

All parameters are loosely specified, particularly the forward current gain, h_{fe} , could range from 100 to 500.

Other models are available (ie hybrid π)



Two steps... just like FETs

- (i) Set a correct dc operating point for safe operation
- (ii) Draw small signal model (ssm) & solve

Basic Common Emitter Amplifier

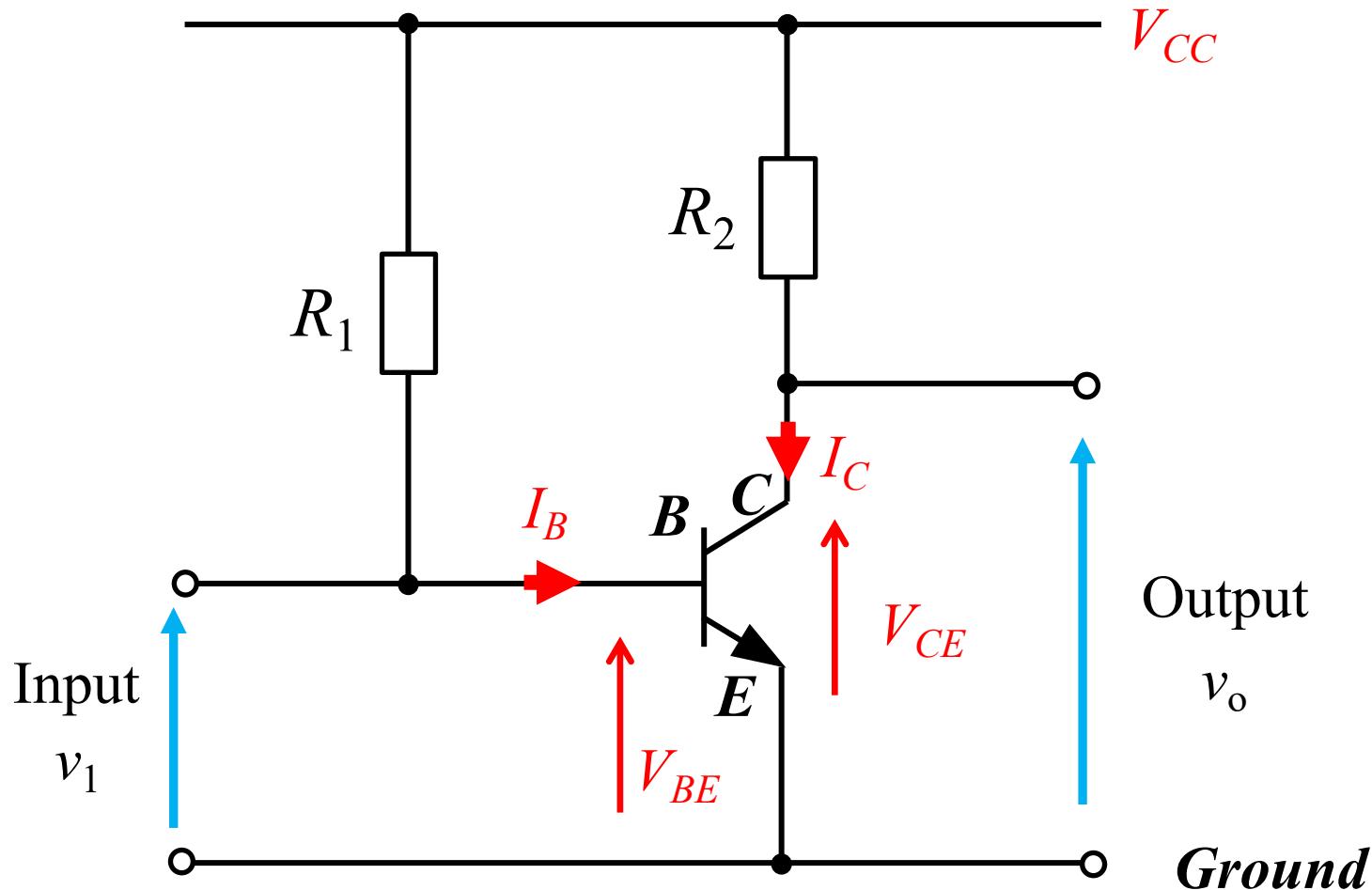
Setting the operating point

We need to bias the transistor to our desired operating point for it to amplify small signals.

Making V_{CE} nominally half V_{cc} is usual.

The load resistance R_2 can vary over a wide range depending on circuit conditions, say 1 k Ω to 47 k Ω .

Basic Common Emitter Amplifier



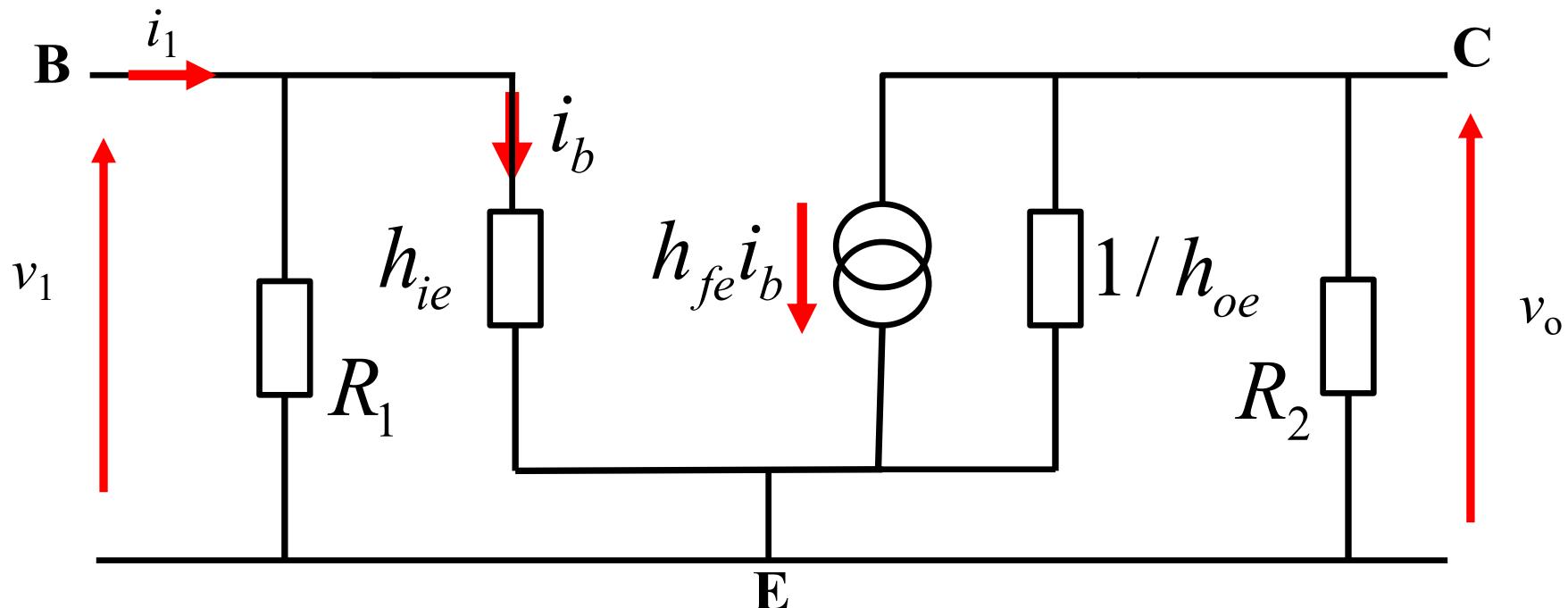
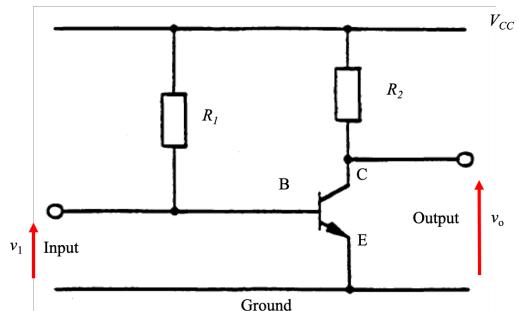
v_1 modulates I_B by an amount i_b

This leads to a modulation of I_C by an amount i_c

In turn : V_{CE} changes by an amount $v_{ce} = v_o$

Small signal equivalent circuit (or model) - ssm

Want to calculate gain (G),
input resistance R_{in} and output
resistance R_o



- Neglect h_{re} unless told otherwise
- dc power supplies (V_{CC}) are ground

- ***Input resistance, R_{in}***

$$R_{in} = \frac{v_1}{i_1} = R_1 // h_{ie} = \frac{R_1 h_{ie}}{R_1 + h_{ie}}$$

To find the gain, G

At the output

$$v_o = -h_{fe} i_b (R_2 // 1/h_{oe}) = -h_{fe} i_b \frac{R_2}{1 + R_2 h_{oe}}$$

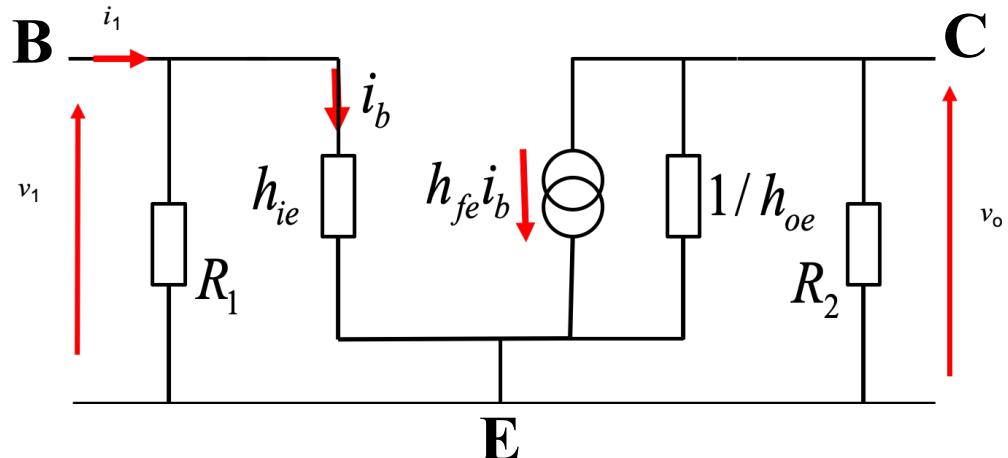
At the input

$$v_1 = h_{ie} i_b$$

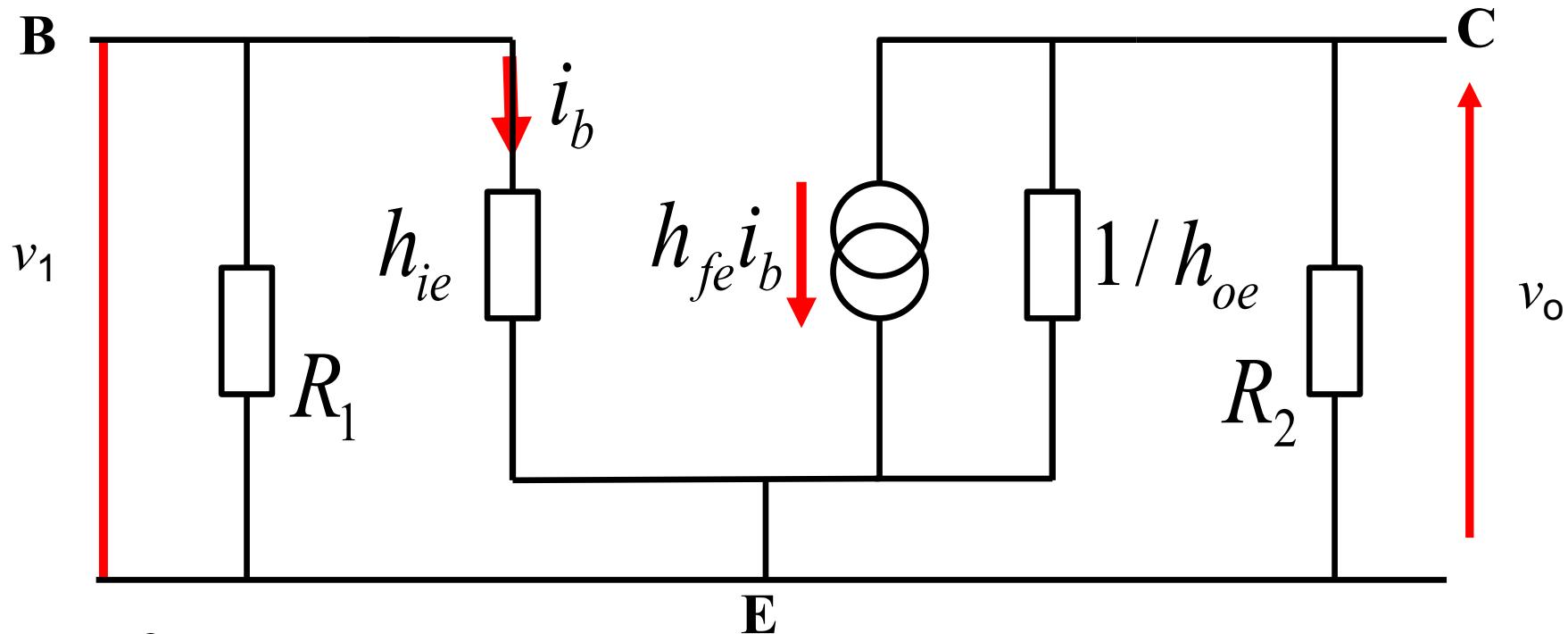
(note : inverting amplifier)

Combining gives

$$G = \frac{v_o}{v_1} = -\frac{h_{fe}}{h_{ie}} \left(\frac{R_2}{1 + R_2 h_{oe}} \right)$$



Output resistance (with input short-circuited), R_o



$$v_I = 0$$

$$i_b = 0$$

$$h_{fe} i_b = 0$$

$$R_o = R_2 \parallel 1/h_{oe} = \frac{R_2}{1 + R_2 h_{oe}}$$

Be careful! Always check if $h_{fe} i_b = 0$

A Worked Example

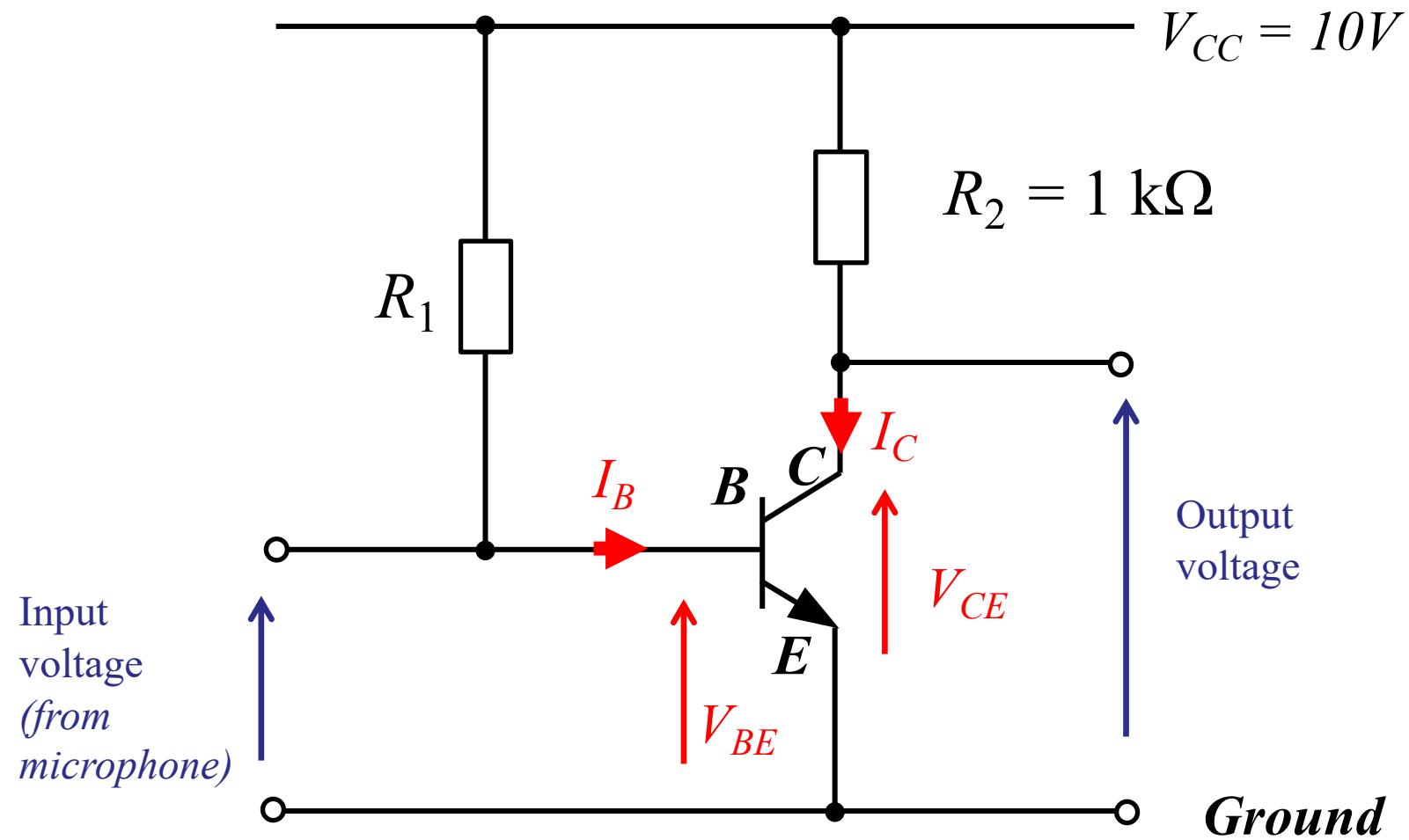
A common emitter amplifier using a type BC182L general-purpose *npn* transistor is to be used as microphone amplifier.

The supply voltage V_{CC} is 10 V, and the collector resistance is to be 1 k Ω .

The transistor has $h_{FE} = 170$ and small signal parameters $h_{ie} = 1 \text{ k}\Omega$, $h_{fe} = 250$, $h_{oe} = 300 \mu\text{S}$ and $h_{re} = 0$.

Find the gain, input and output resistances.

Biasing (setting the operating point for dc)



Supply voltage of 10 V, set V_{CE} to be 5 V. We can now find I_C

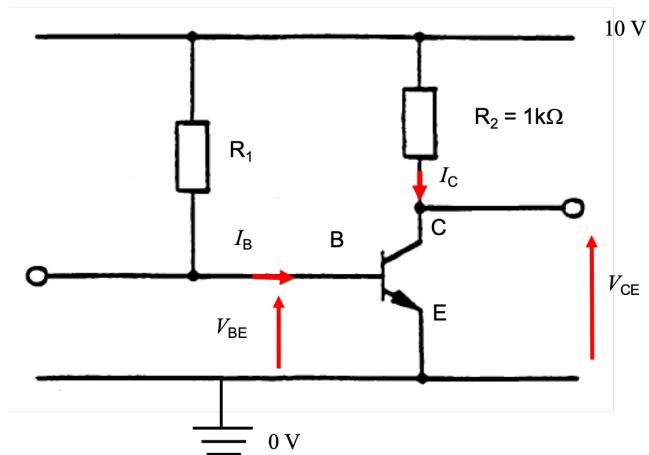
$$I_C = \frac{V_{CC} - V_{CE}}{R_2} = 5 \text{ mA}$$

We can now find I_B using h_{FE}

$$I_B = \frac{I_C}{h_{FE}} = 29 \mu\text{A}$$

Assuming V_{BE} is 0.7 V we can find R_1

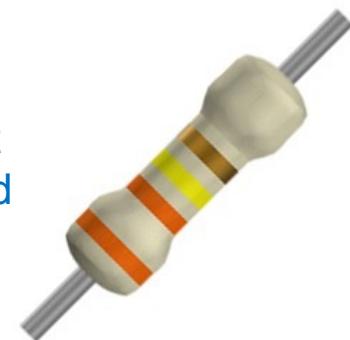
$$R_1 = \frac{V_{CC} - V_{BE}}{I_B} = 321 \text{ k}\Omega$$



$$h_{FE} = 170$$

(or use input graph)

(330 kΩ
Is the
nearest
standard
value)



Circuit analysis (from earlier sections)

$$R_{in} = \frac{R_1 h_{ie}}{R_1 + h_{ie}} = 1 \text{ k}\Omega$$

A bit low – usually want R_{in} to be high so as not to draw too much power from source

The gain G is

$$G = -\frac{h_{fe}}{h_{ie}} \frac{R_2}{1 + R_2 h_{oe}} = -153$$

Higher than the gain of typical FET-based amplifiers

The output resistance R_o is

$$R_o = \frac{R_2}{1 + R_2 h_{oe}} = 769 \text{ }\Omega$$

A bit high – not all voltage out will reach load

IB Paper 5: Analysis of circuits

Prof C Durkan
cd229@cam.ac.uk

3 *More stable BJT circuits*

The effect of variations in transistor parameters on the operating point

For the BC182L, h_{FE} has a nominal (average) value of 250 but can vary between 100 and 500.

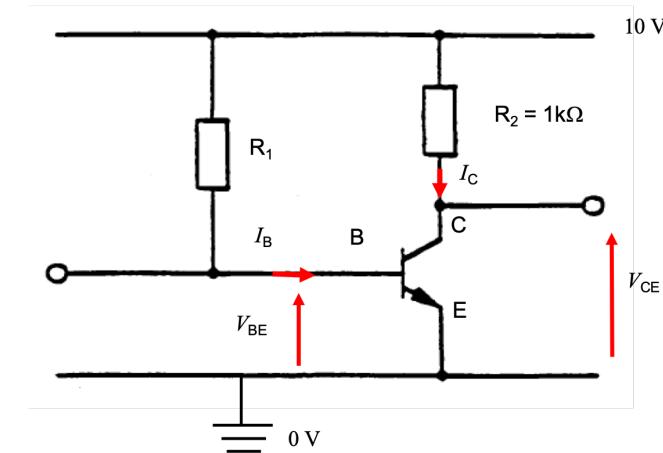
We can find the range of resulting operating points.

I_B is insensitive to changes in V_{CE} so it can be taken as constant at 40 μA .

For $h_{FE}=100$

$$I_C = 100I_B = 4 \text{ mA}$$

$$V_{CE} = 6 \text{ V}$$



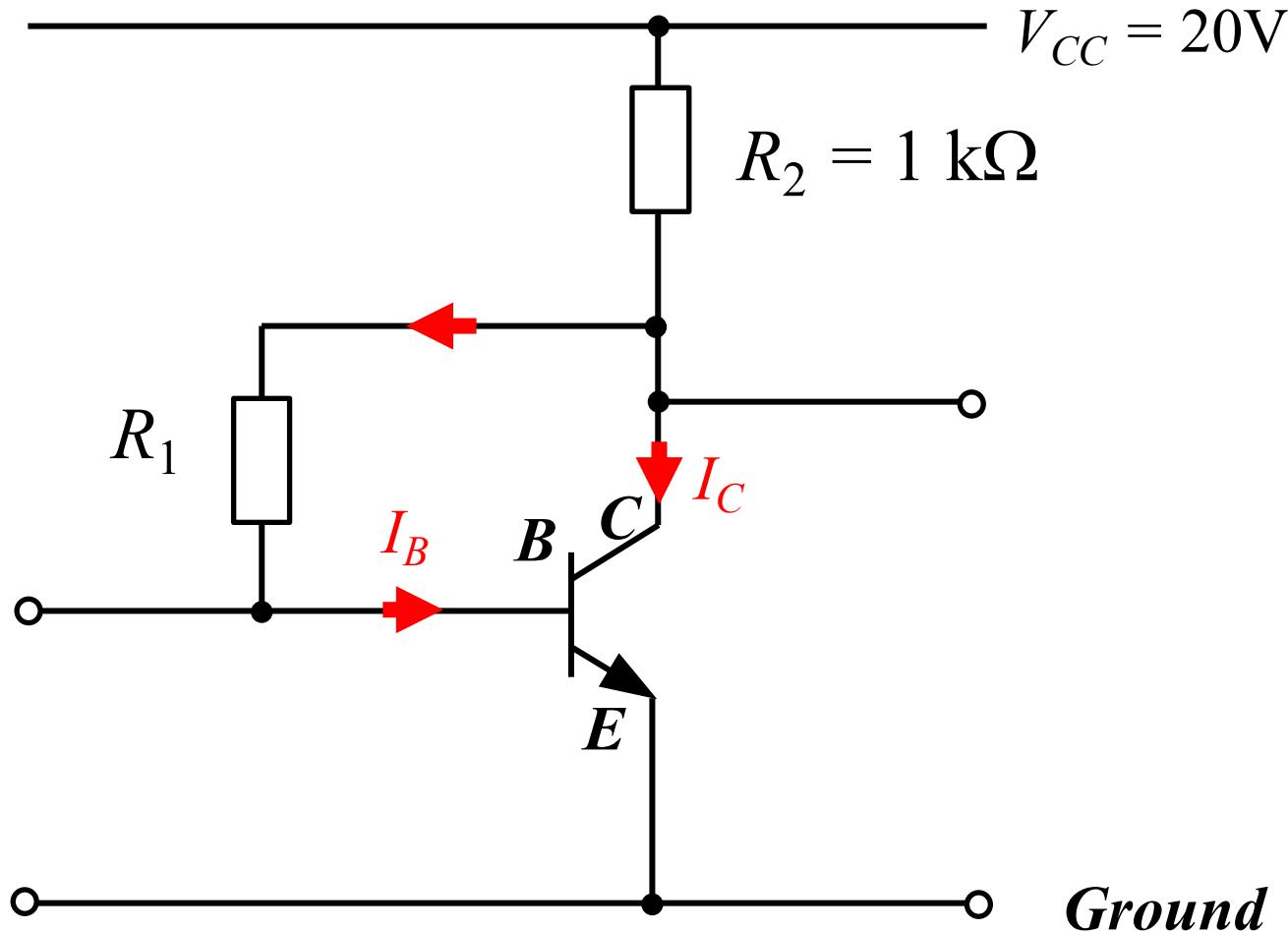
For $h_{FE}=500$

$$I_C = 500I_B = 20 \text{ mA}$$

$$V_{CE} = 0 \text{ V}$$

The variation in operating point is obviously unacceptable, even before variations of parameters with temperature is considered.

Connecting R_1 to the collector rather than V_{CC} improves the stability of the biasing



If h_{FE} is above nominal, V_{CE} is lower which reduces I_B , giving a degree of self-compensation.

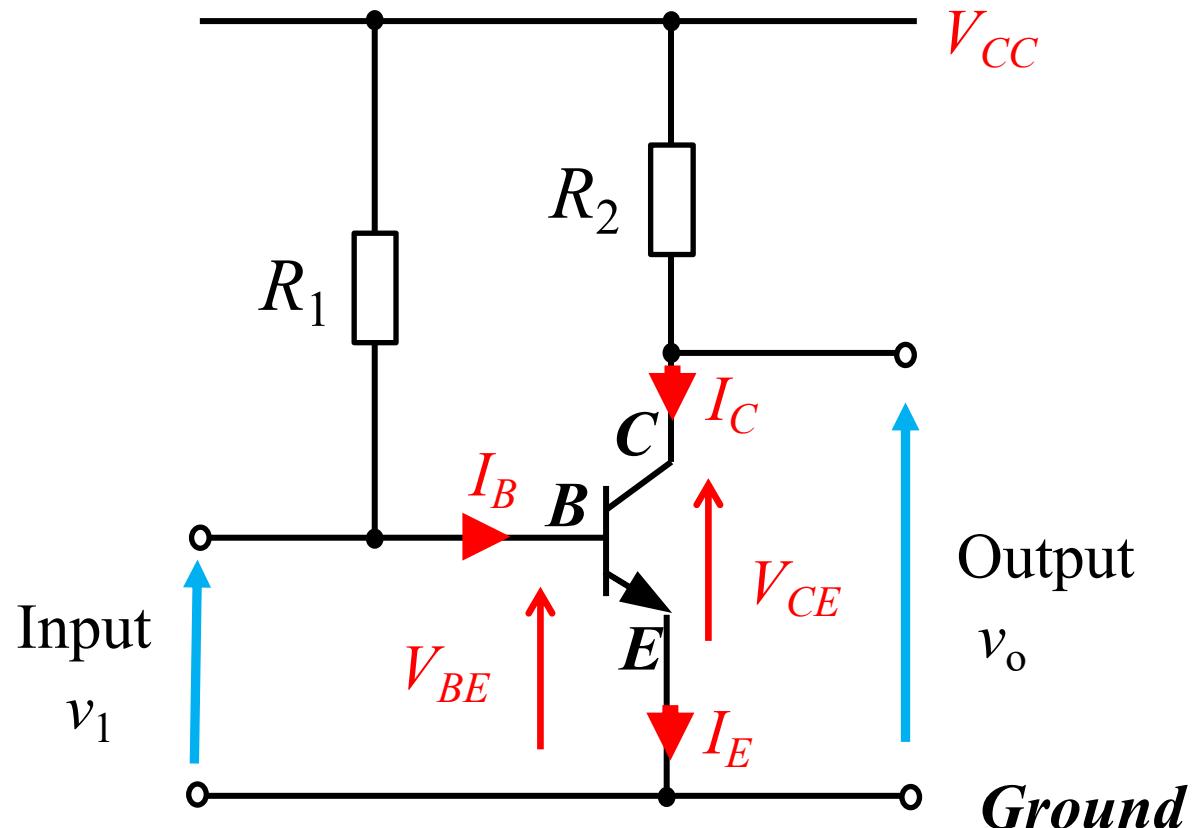
Similarly, if h_{FE} is below nominal, the higher V_{CE} leads to an increase in I_B .

(See Ex sheet 1
Q2)

The Bipolar Transistor - Circuit Design

A bias circuit with emitter resistance

Recap of common-emitter amplifier:

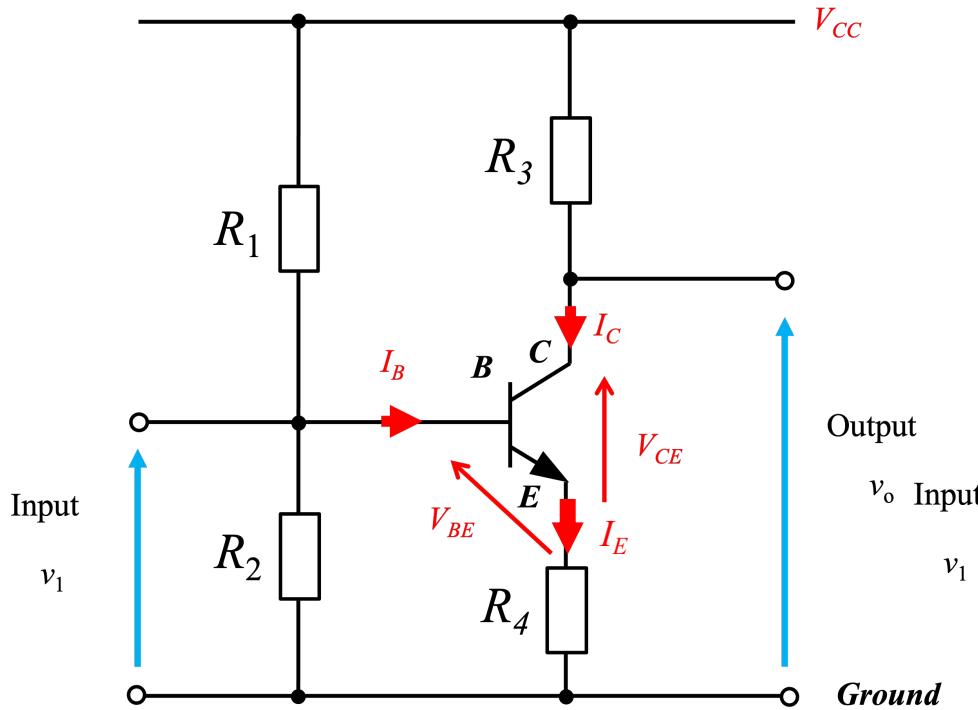


Including a resistance in the emitter circuit enables a stable operating point to be achieved, albeit at the expense of circuit complexity.

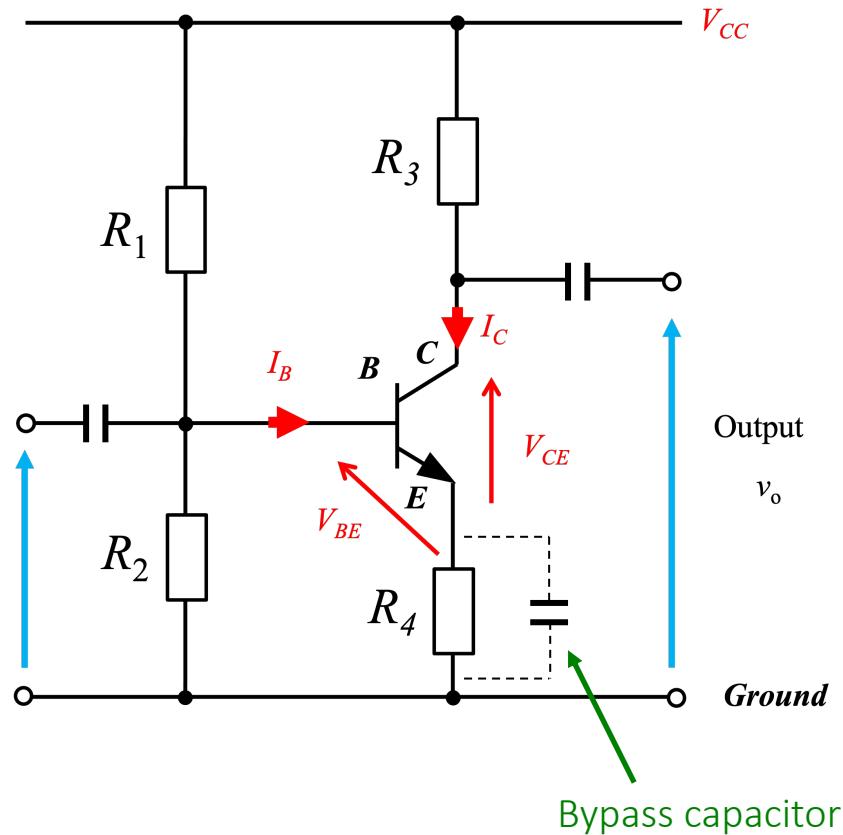
$$G = \frac{v_o}{v_1} = -\frac{h_{fe}}{h_{ie}} \left(\frac{R_2}{1 + R_2 h_{oe}} \right)$$

Note the strong dependence on transistor properties

Now add the emitter resistance

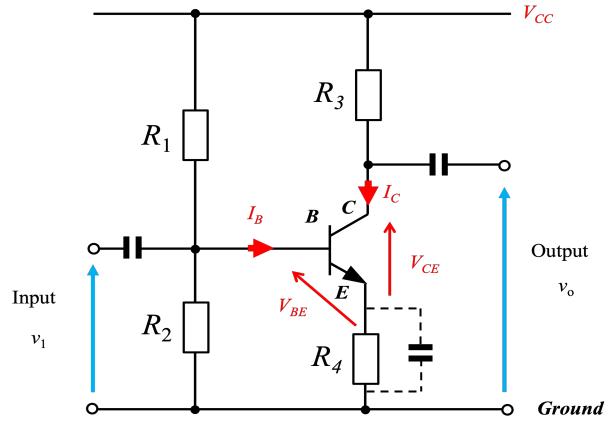
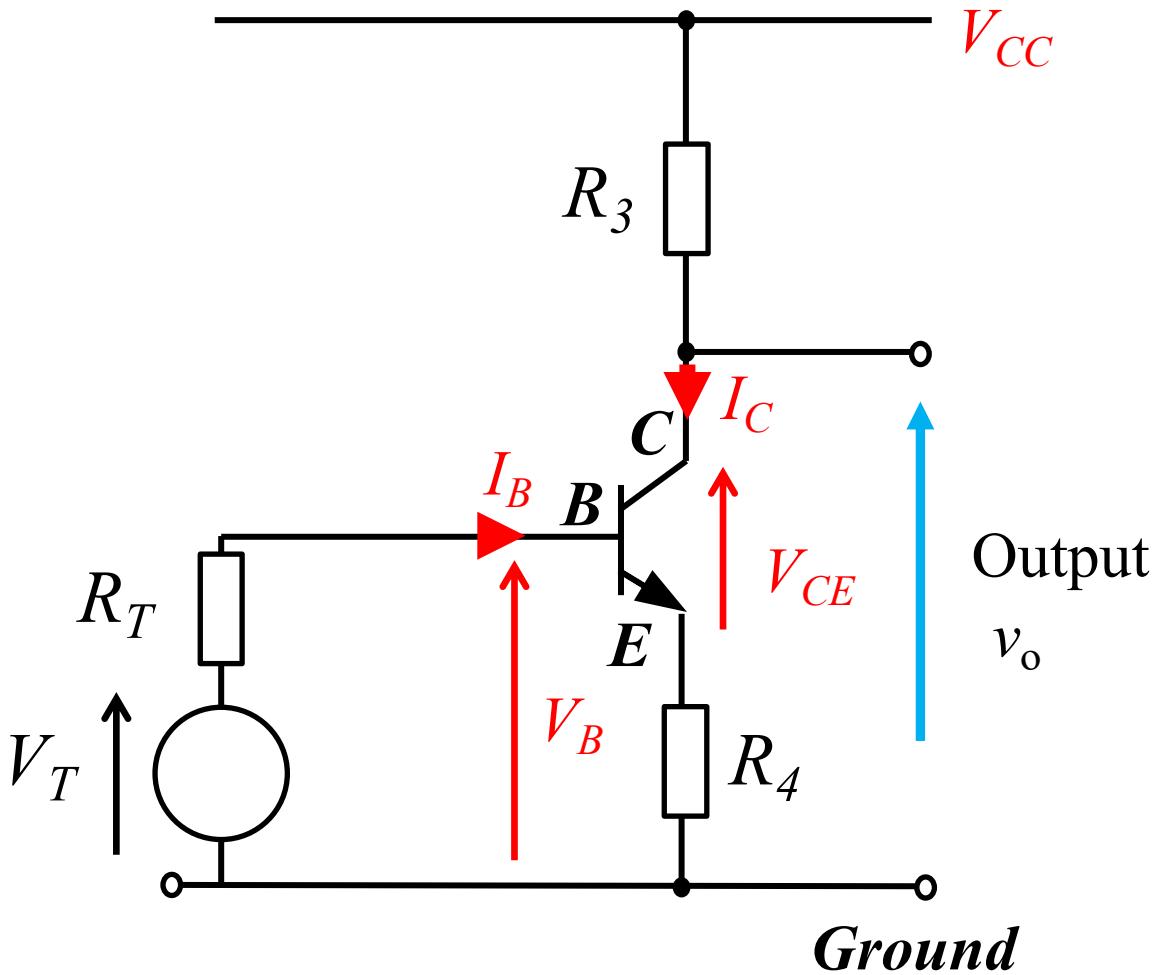


Don't forget coupling (decoupling) capacitors



- The potential divider formed by R_1 and R_2 sets V_B constant if I_B is small compared with the current through the divider.
- Provided that V_B is several times greater than V_{BE} , a constant voltage is maintained across R_4 thereby setting a constant I_E .
- If I_B is small then I_C will be constant, maintaining a fixed operating point.

Use a Thévenin equivalent for the potential divider supplying the base - Replace R_1 and R_2 network with V_T and R_T equivalents



$$V_T = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$R_T = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Mesh analysis around the circuit

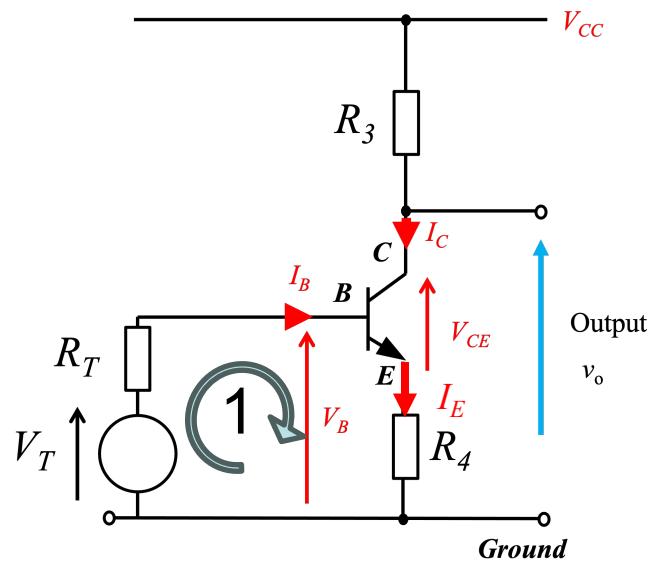
$$V_T = R_T I_B + \underbrace{V_{BE} + (I_C + I_B) R_4}_{V_B} + I_E R_4$$

...around loop 1

By definition, $I_C = h_{FE} I_B$

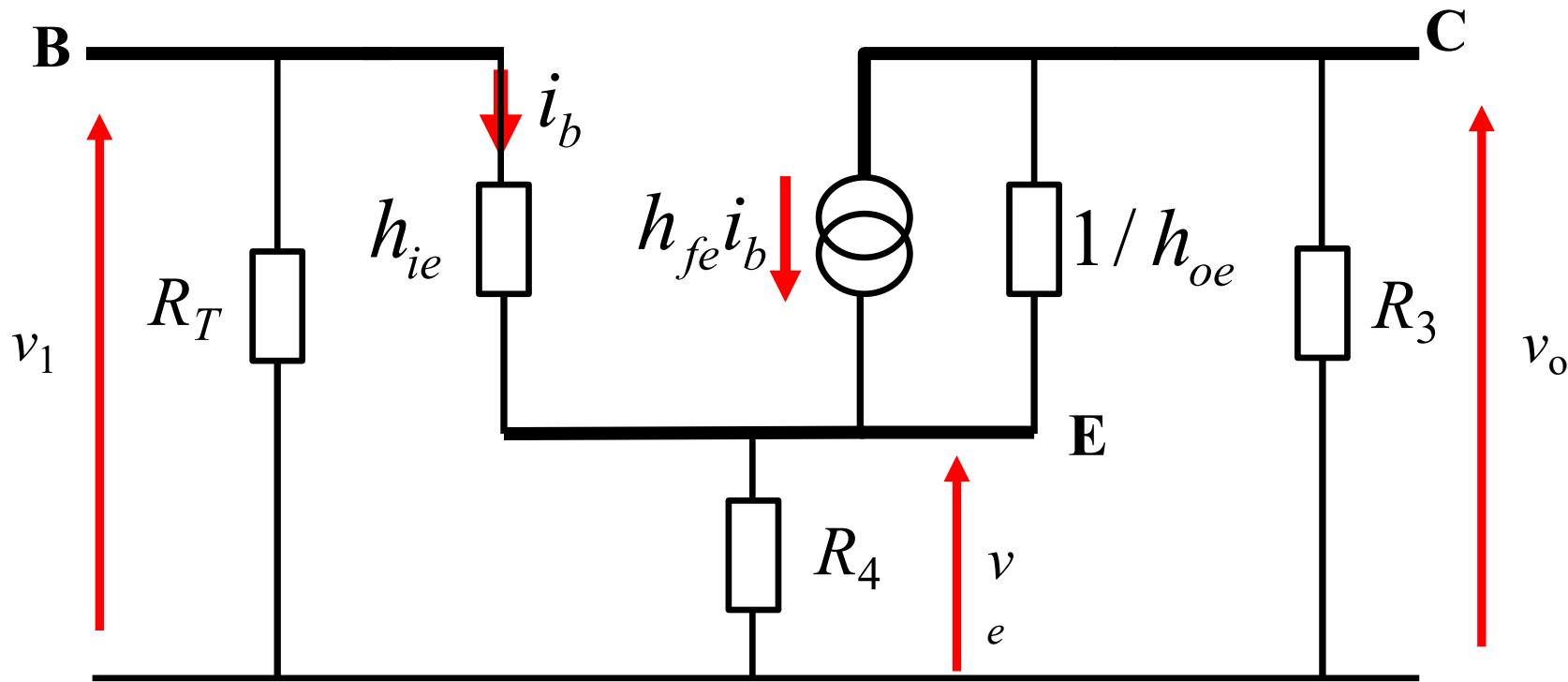
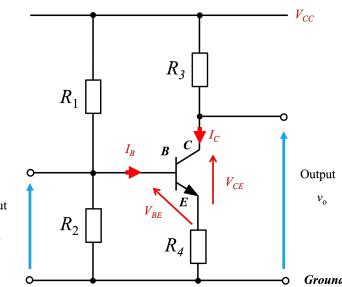
Combining and rearranging:

$$I_C = \frac{h_{FE} (V_T - V_{BE})}{R_T + R_4 (1 + h_{FE})}$$



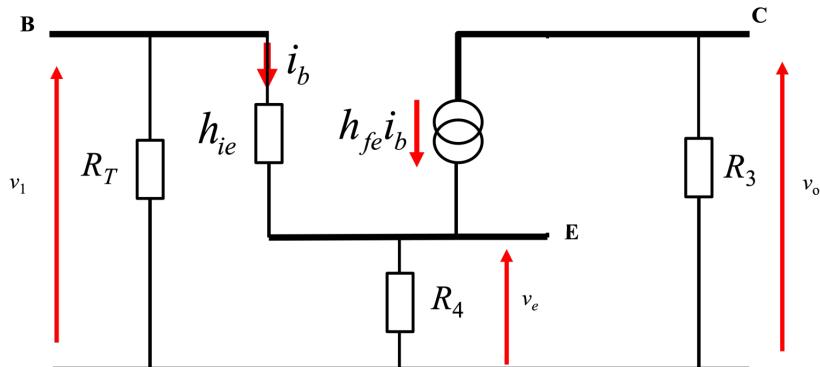
Analysis of the Effect of the Emitter Resistor

The emitter resistor R_4 which has been incorporated to increase the stability of the operating point also affects the gain of the circuit.



- Neglect h_{re} . Assume that $1/h_{oe}$ is much greater than R_3 as this is often the case
- Assume any coupling capacitors have negligible reactances (i.e. shorted-out), as we are at mid-band frequencies.

At the output $v_o = -h_{fe}i_b R_3$



At the input

$$v_1 = h_{ie}i_b + v_e = h_{ie}i_b + (1 + h_{fe})i_b R_4$$

Eliminating i_b and rearranging gives

$$\frac{v_o}{v_1} = \frac{-h_{fe}R_3}{h_{ie} + \underbrace{(1 + h_{fe})R_4}_{\text{Extra term reduces gain}}}$$

Extra term reduces gain

Without R_4 , we would obtain:

$$\frac{v_o}{v_1} = -\frac{h_{fe}R_3}{h_{ie}}$$

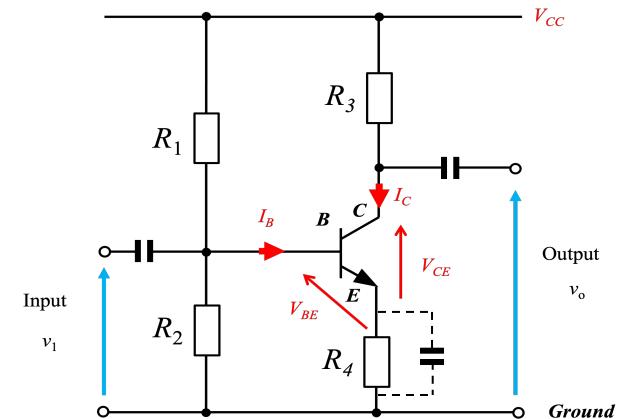
For $R_4 = 0$, the gain is the same as for the common emitter amplifier.

For $R_4 = 200 \Omega$, and other values unchanged, the gain is reduced by a factor of **51** (*assuming previous component values*)

i.e. The gain falls from -153 to -3.

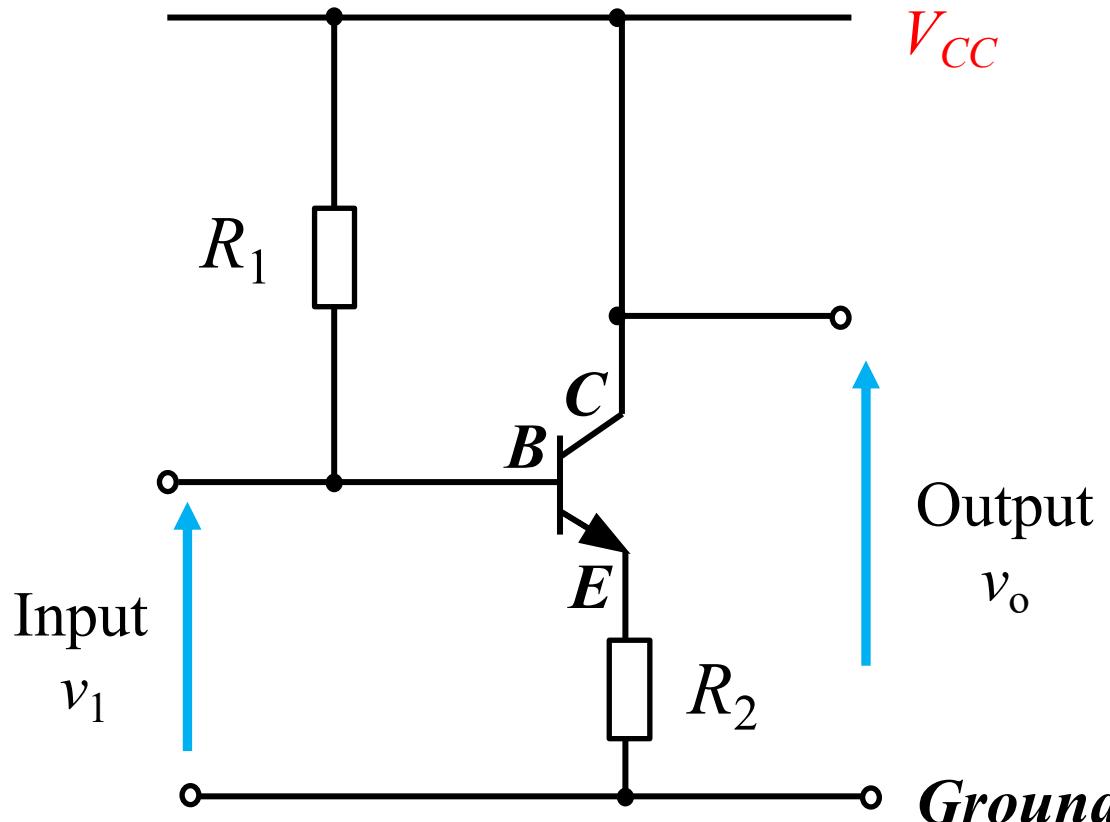
The reduction in gain can be overcome by bypassing R_4 with a capacitor – brings us back to the common emitter amplifier. The function of R_4 is then purely to help set and stabilise the DC operating point

It is therefore common to have the configuration below, where R_4 is included to set the DC operating point, but it is bypassed with a capacitor in order to achieve the larger midband gain



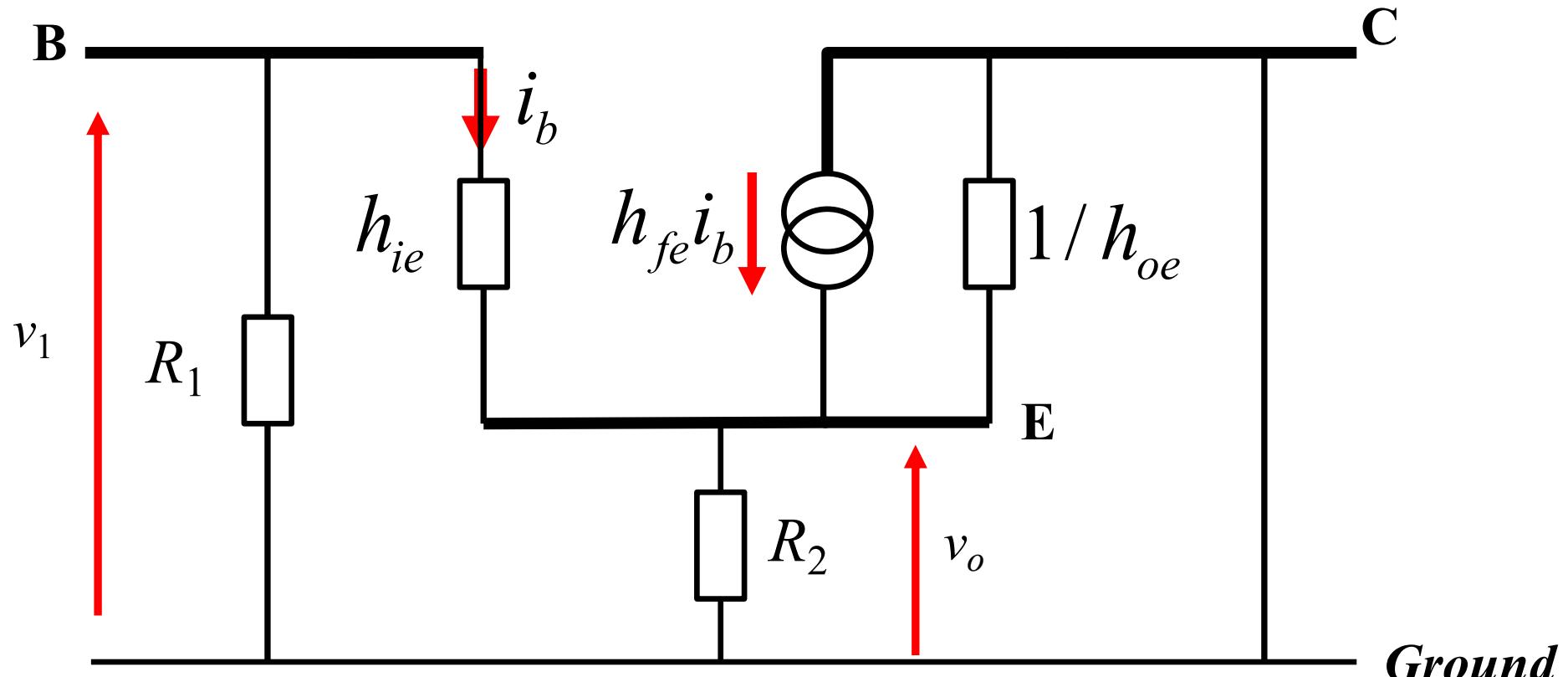
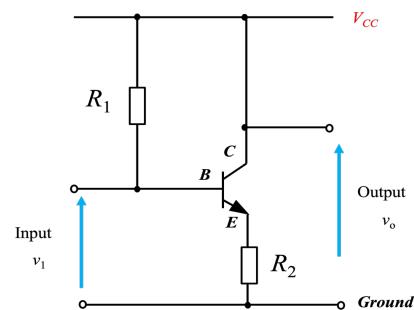
The Emitter Follower – a buffer

Although the gain of the emitter follower is just less than unity, hence the name, the circuit is very valuable where a low output impedance, a high input impedance or both are needed.



R_1 provides base current which sets the operating point. The stability of the operating point is reasonable because of the presence of R_2 .

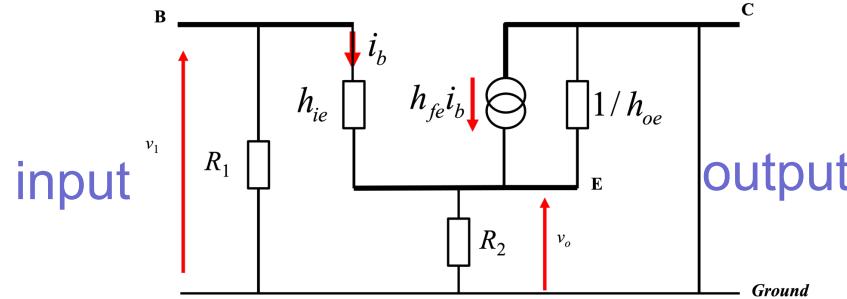
Small signal circuit of the emitter follower



To find the gain we set up equations at the input and output, both involving i_b , and then eliminate i_b

Voltage Gain of the Emitter Follower

At the input $v_1 = h_{ie} i_b + v_o$



Summing currents at the emitter

$$(1 + h_{fe})i_b = \frac{v_o}{R_2} + \frac{v_o}{1/h_{oe}}$$

Eliminate i_b

$$G = \frac{v_o}{v_1} = \frac{1}{1 + \left(\frac{h_{ie}/R_2 + h_{oe}h_{ie}}{1 + h_{fe}} \right)}$$

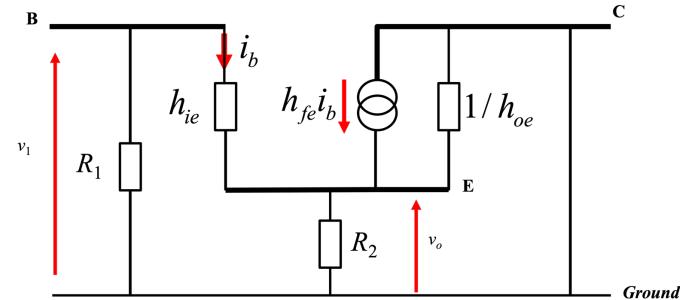
e.g. BC182L, $h_{ie} = 1 \text{ k}\Omega$, $h_{oe} = 300 \mu\text{S}$, $h_{fe} = 250$. If $R_2 = 2 \text{ k}\Omega$,
 $R_1 = 500 \text{ k}\Omega$

$$G = 0.997$$

The Input and Output Resistances of the Emitter Follower

Input resistance

$$R_{IN} = \frac{v_i}{i_1} \quad i_1 = \frac{v_1}{R_1} + \frac{v_1 - v_o}{h_{ie}}$$



$$\Rightarrow R_{IN} = \frac{1}{\frac{1}{R_1} + \frac{(1-G)}{h_{ie}}} \text{ using } G = \frac{v_o}{v_1}$$

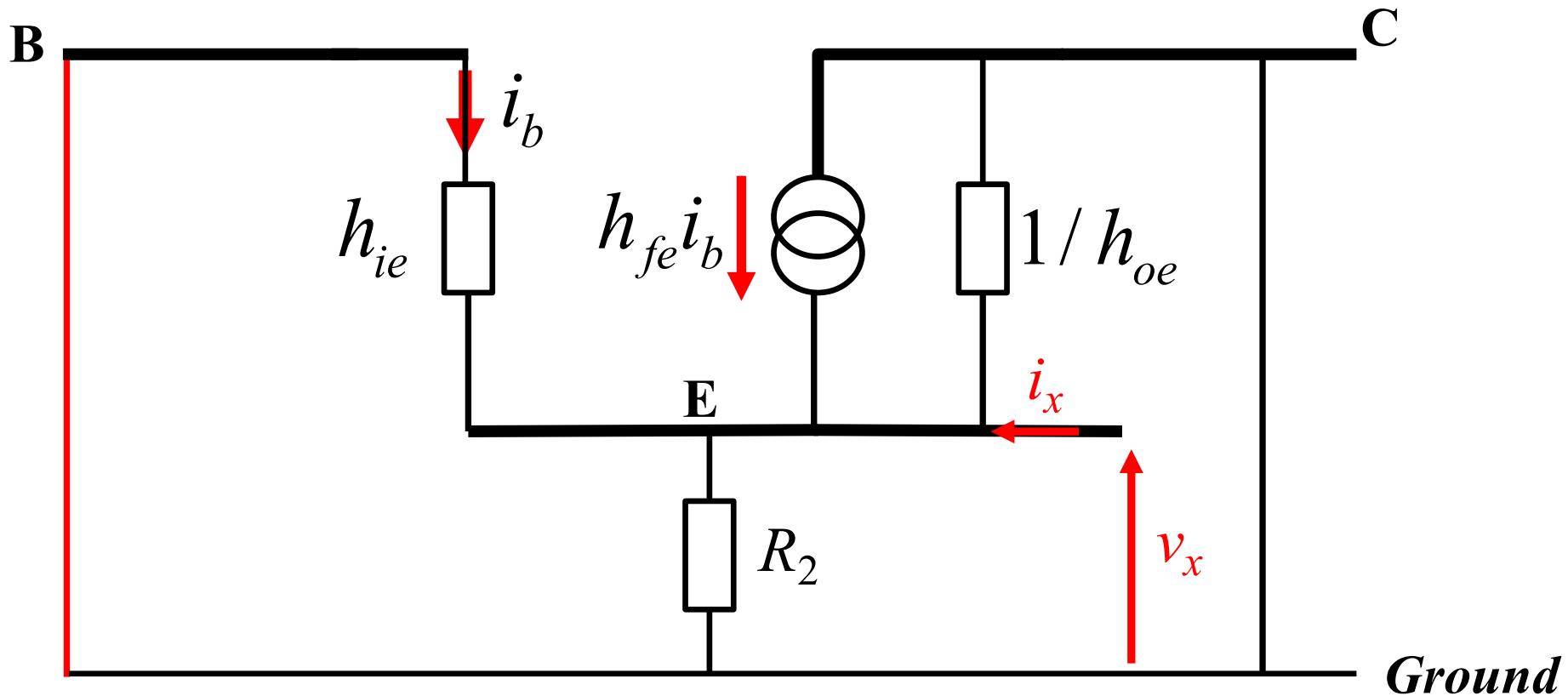
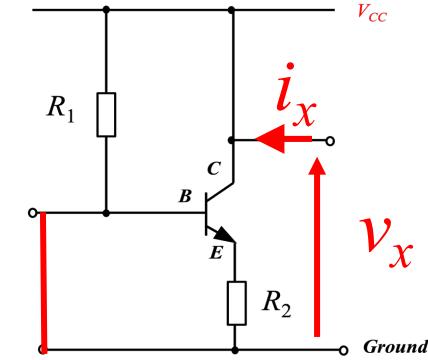
$R_{IN} \sim 200 \text{ k}\Omega$ - fairly high, but reduced from $\sim 300 \text{ k}\Omega$ by R_1

Output Resistance

Always check if $h_{fe}i_b = 0$

Apply a test voltage v_x which causes a current i_x to flow.

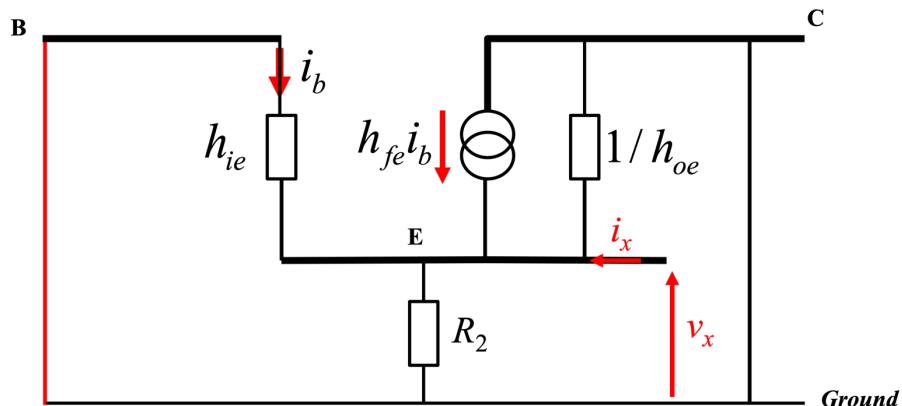
The input terminals are **shorted**.



Firstly, find the base current i_b

$$i_b = \frac{0 - v_x}{h_{ie}} = -\frac{v_x}{h_{ie}}$$

Sum currents at the emitter



$$(1 + h_{fe})i_b + i_x = \frac{v_x}{R_2} + \frac{v_x}{1/h_{oe}}$$

Eliminate i_b and re-arrange to get output resistance,

$$R_o = \frac{v_x}{i_x} = \frac{1}{\frac{1}{R_2} + h_{oe} + \left(\frac{h_{fe}+1}{h_{ie}}\right)}. \quad \text{i.e. all three resistances in parallel}$$

For the circuit above, $R_o = 4\Omega$

Compare to common-emitter amplifier, or any previous circuit – R_o typically several 100s of Ω

IB Paper 5: Analysis of circuits

Prof C Durkan
cd229@cam.ac.uk

4 *Differential amplifiers*

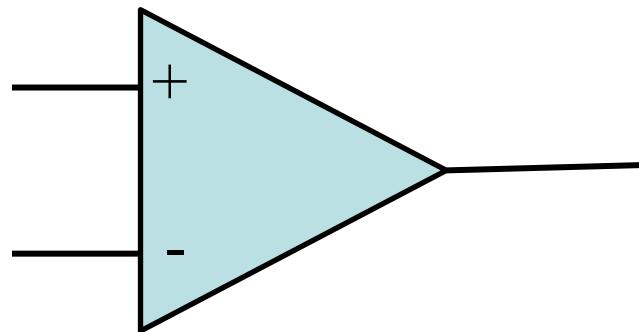
Topic 4 - Differential Amplifiers

As we have already seen with the FET and BJT, analogue circuit design can be analysed through building blocks or 'models' used to represent their inherent behaviour.

The next stage is to use more complicated models to represent and analyse different combinations of transistor circuits.

One of the most fundamental and useful circuits is the ***differential amplifier***, this in turn then leads us to the most useful building block in any analogue circuit, the ***Operational Amplifier or Op-Amp***.

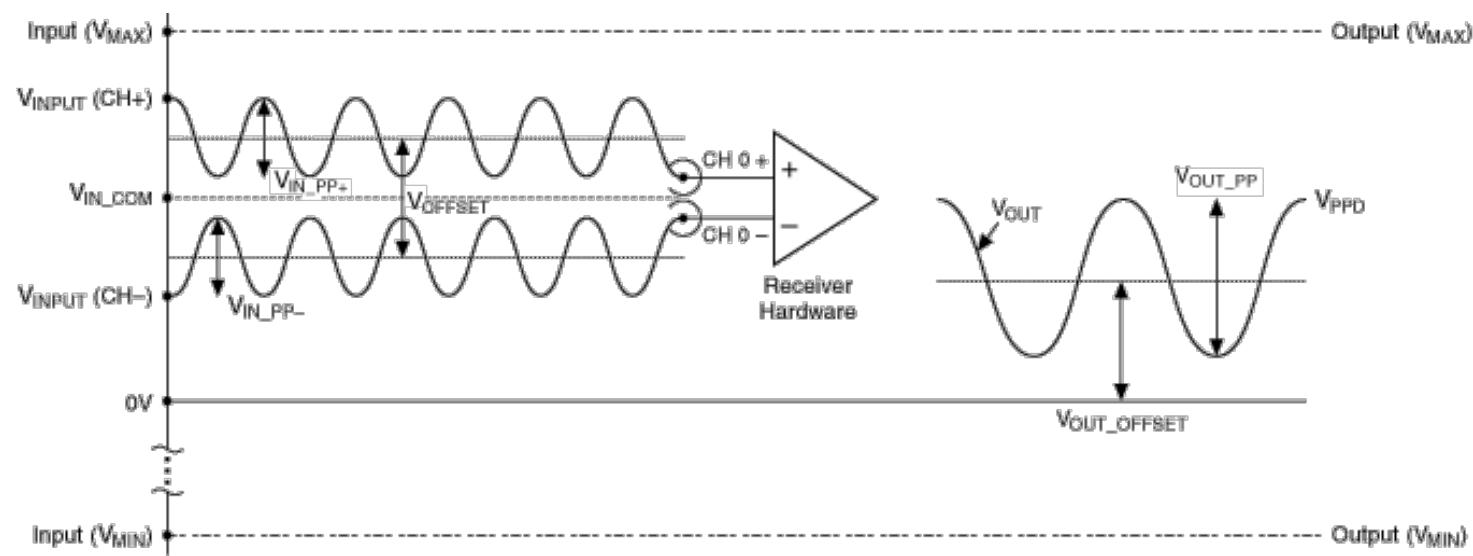
Op-Amps may contain hundreds of individual transistors, but by choosing the appropriate model, we can analyse its function using only three basic parameters – input resistance, open-loop gain and output resistance. In the ideal case, the analysis can be simplified even further to give a very powerful and versatile circuit element that is used in many circuits.



Although there are many different types of operational amplifier, almost all use the same basic circuit structure.

We begin by studying the input circuit of an Op-Amp, the differential amplifier or 'long tailed pair'.

The input circuit uses an emitter (BJT) or source (FET) coupled pair of transistors to amplify the *difference* between the voltages at the two separate inputs.



Differential amplifier using FETs

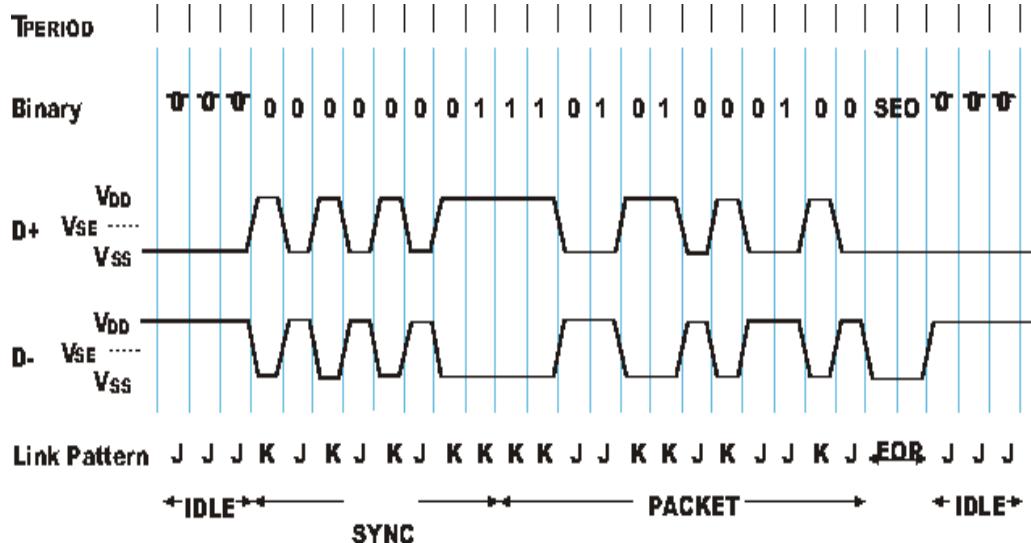
Note, the rules of analysis and terminology in the following sections are the same if using bipolar junction transistors (see Examples sheet), only the small signal model of the transistor changes.

The design of a differential amplifier implies that the input will be supplied from two voltage (or current) sources and the signal that we want to amplify is defined by the difference between these two sources.

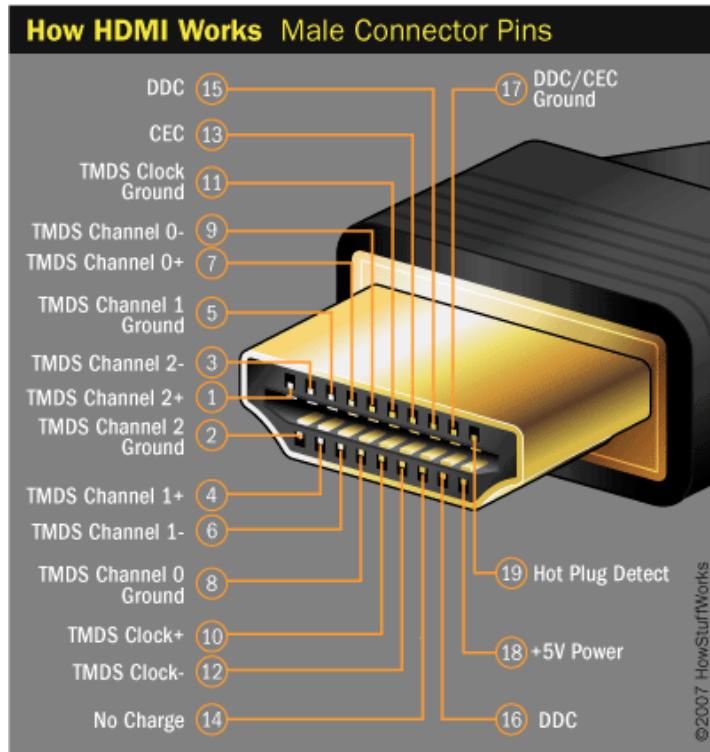
Many applications where external noise is a problem will use differential (or balanced) inputs.

Common scenarios include audio signals for musical concerts or sensors systems, where there is a small signal generated in a noisy environment.

High-Definition Multimedia Interface



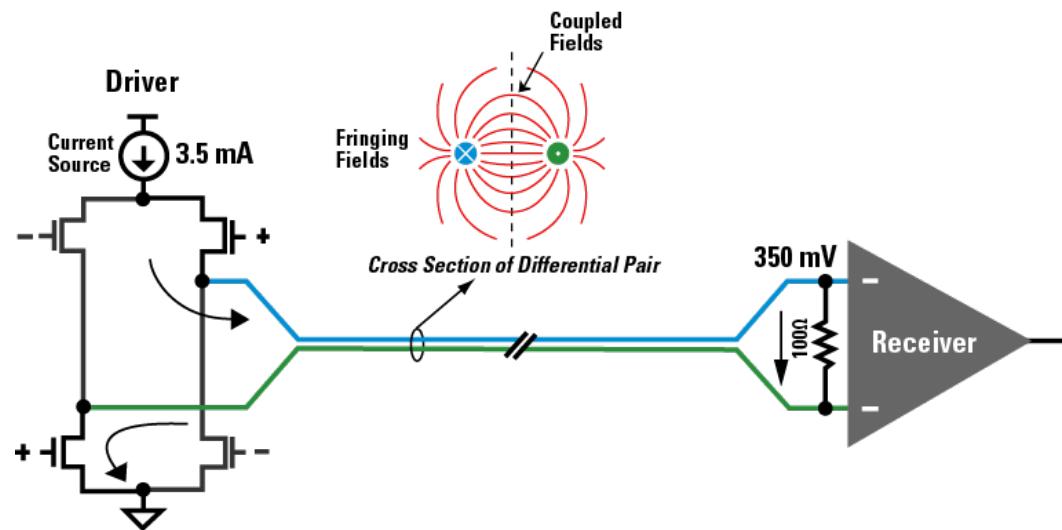
<http://www.networktechinc.com/usb-prots.html>



<http://electronics.howstuffworks.com/hdmi2.htm>



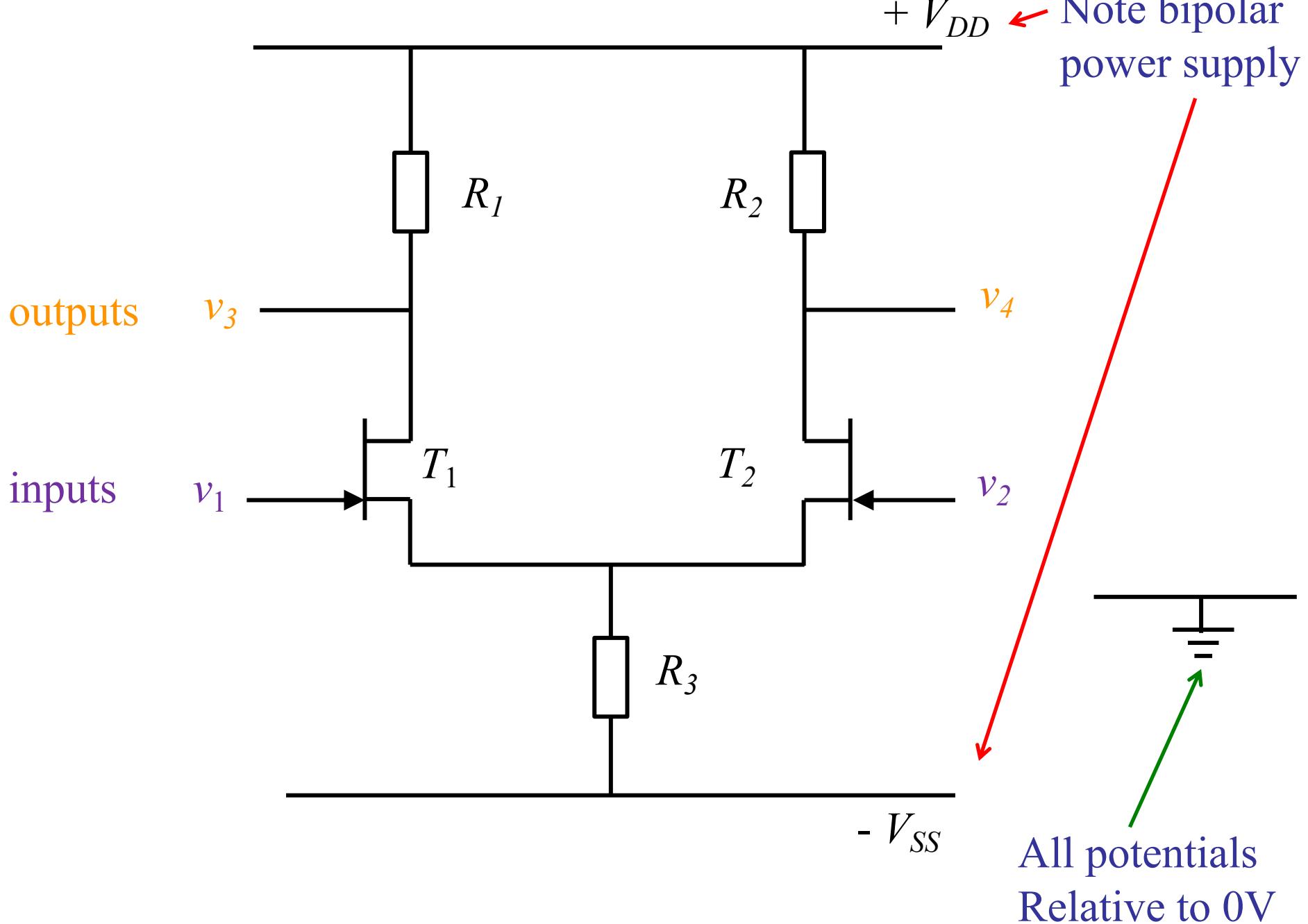
Universal Serial Bus (USB)

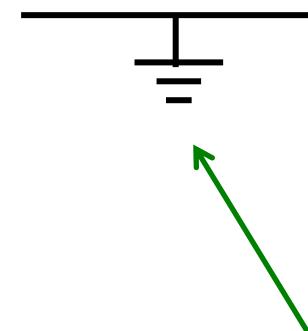
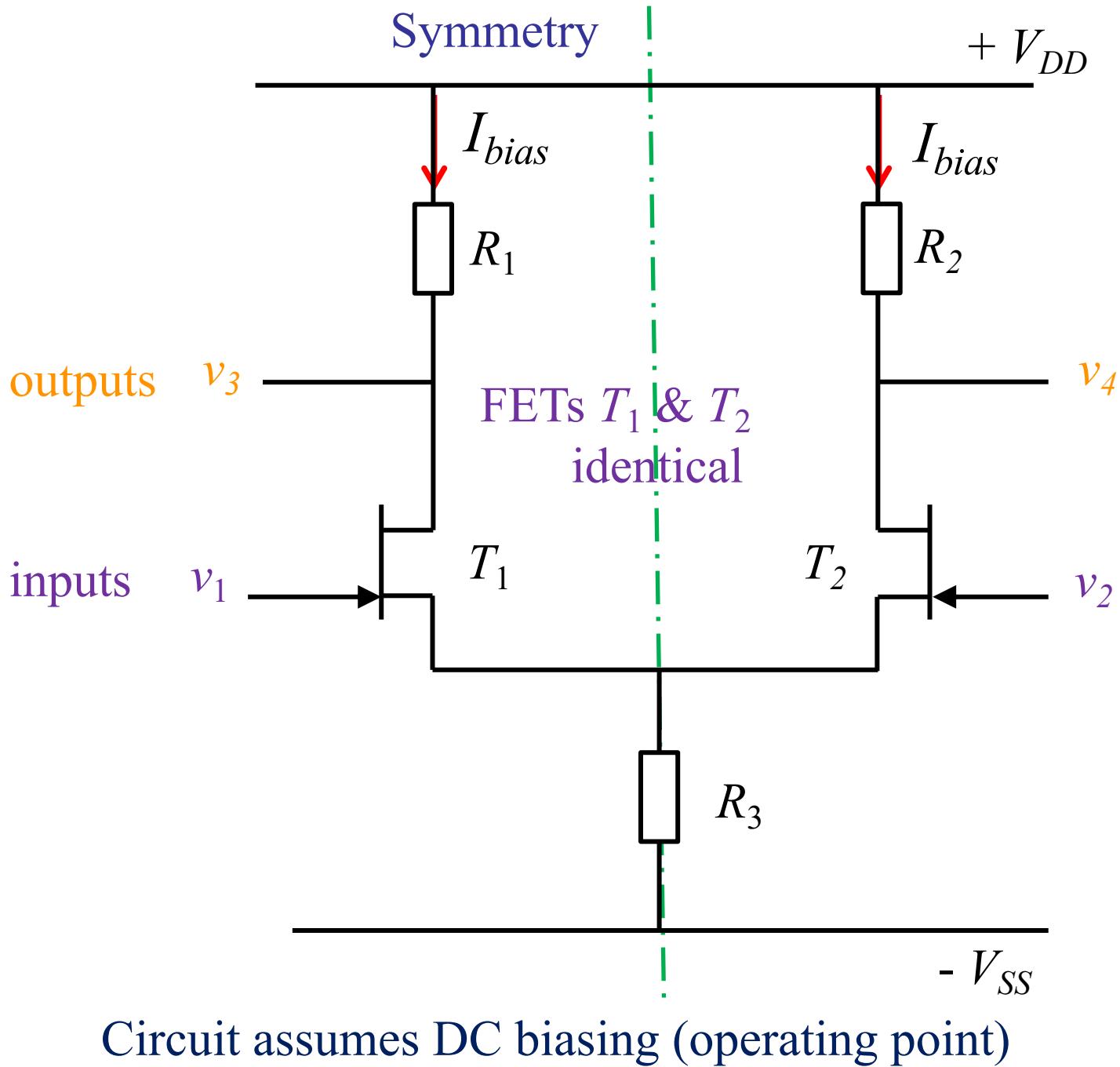


Low-voltage differential signaling (LVDS)

https://en.wikipedia.org/wiki/Low-voltage_differential_signaling

The “Long-tailed pair” – a differential amplifier





All potentials
Relative to 0V

The two inputs to the amplifier are labelled v_1 and v_2 and the outputs labelled v_3 and v_4 .

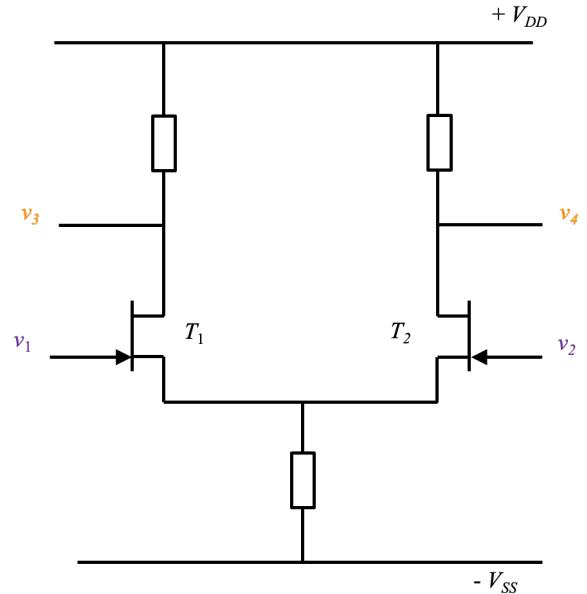
We define a *common mode* input

$$v_I = v_2$$

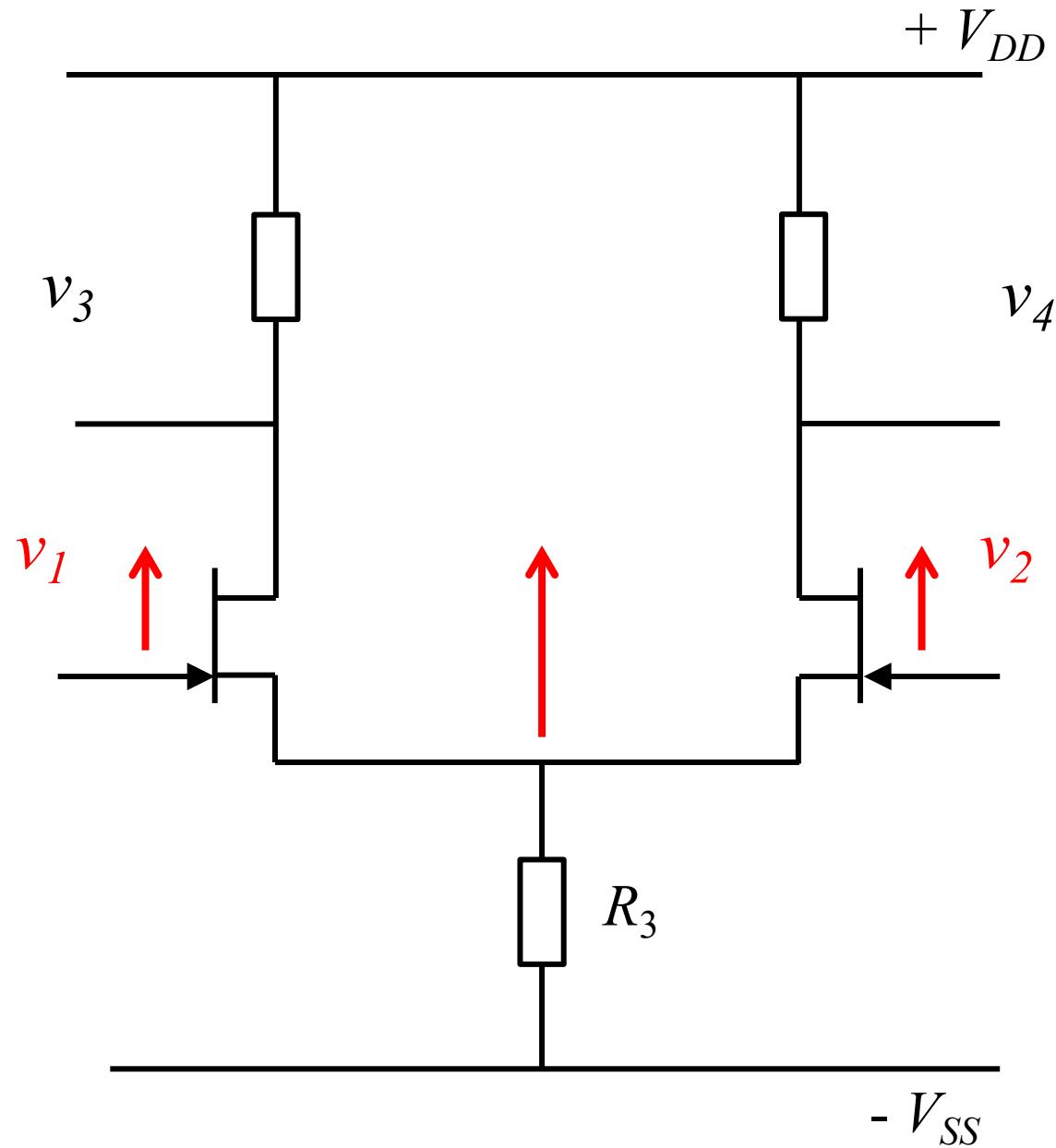
If v_1 and v_2 increase together then the currents through R_1 and R_2 will rise and so will the current through R_3 .

The voltage at both FET sources rises, reducing the gate-source voltages of T_1 and T_2

As a result, the gain (output/input) v_3/v_I (or v_4/v_2) will be small.



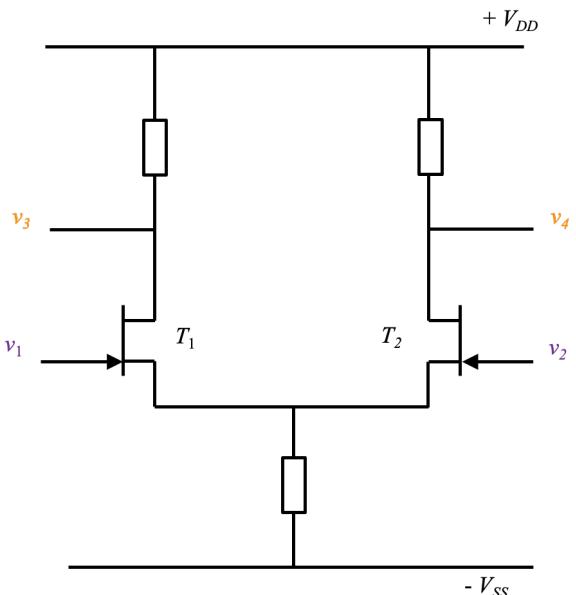
Common mode



In differential circuits the input signal is defined as the difference between the two inputs ($v_1 - v_2$).

We can therefore define a *differential mode* input signal

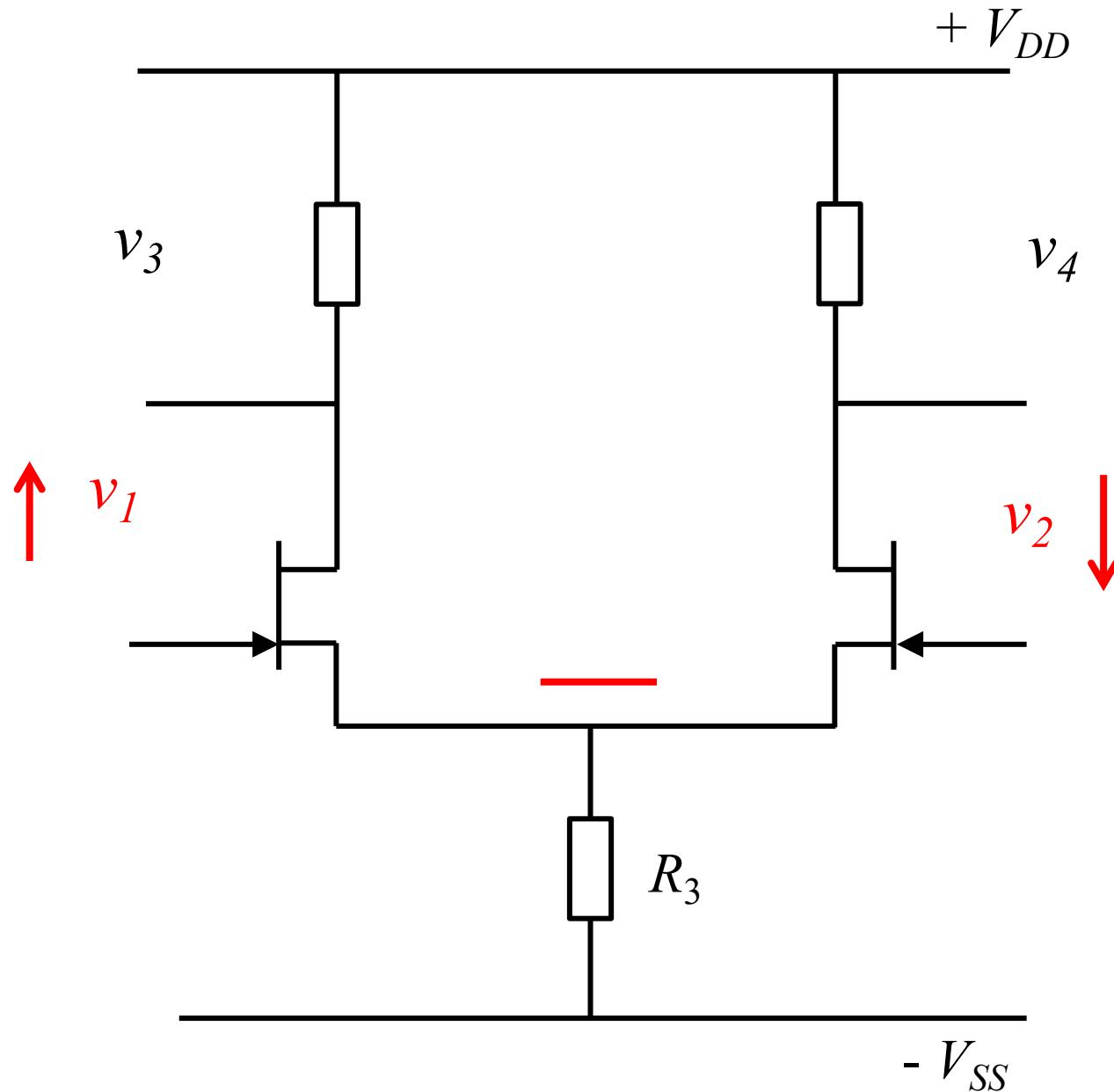
$$v_1 = -v_2$$



Increasing v_1 increases the current through R_3 and T_1 and the voltage v_2 decreases, causing an equal fall in current through R_4 and T_2 .

The current through R_3 will remain constant and the voltage across R_3 will remain constant.

Differential mode



Common Mode Rejection Ratio (CMRR)

CMRR is a measure of performance of a differential amplifier and is defined as

$$\frac{\text{Gain for differential mode signals}}{\text{Gain for common mode signals}}$$

Large

Small

To find the CMRR, we need to find the gains for ***common mode*** and ***differential mode*** signals.

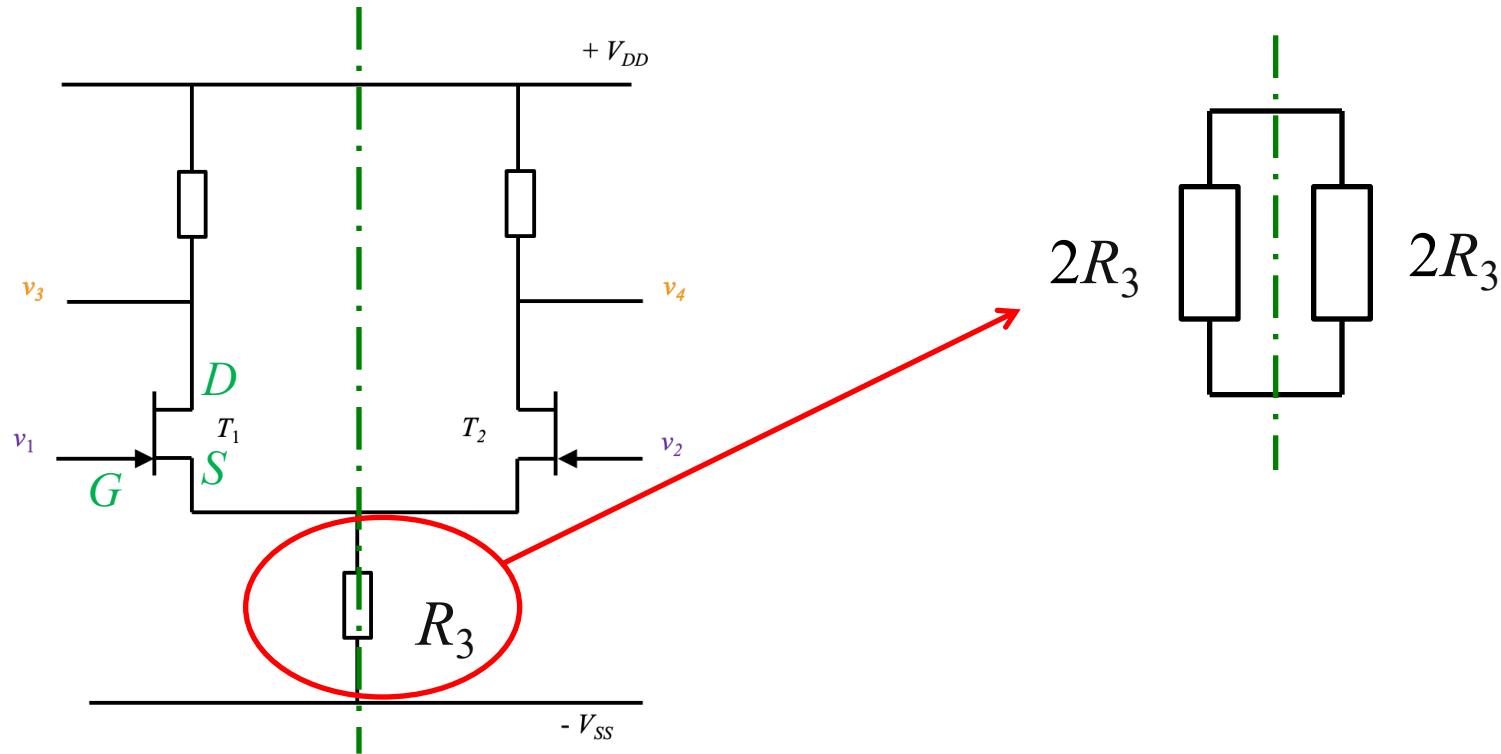
Conveniently, signals can always be reduced to common mode and differential components.

We can also use the symmetric nature of the circuit about R_3 to reduce the analysis to a single transistor.

Common Mode Gain

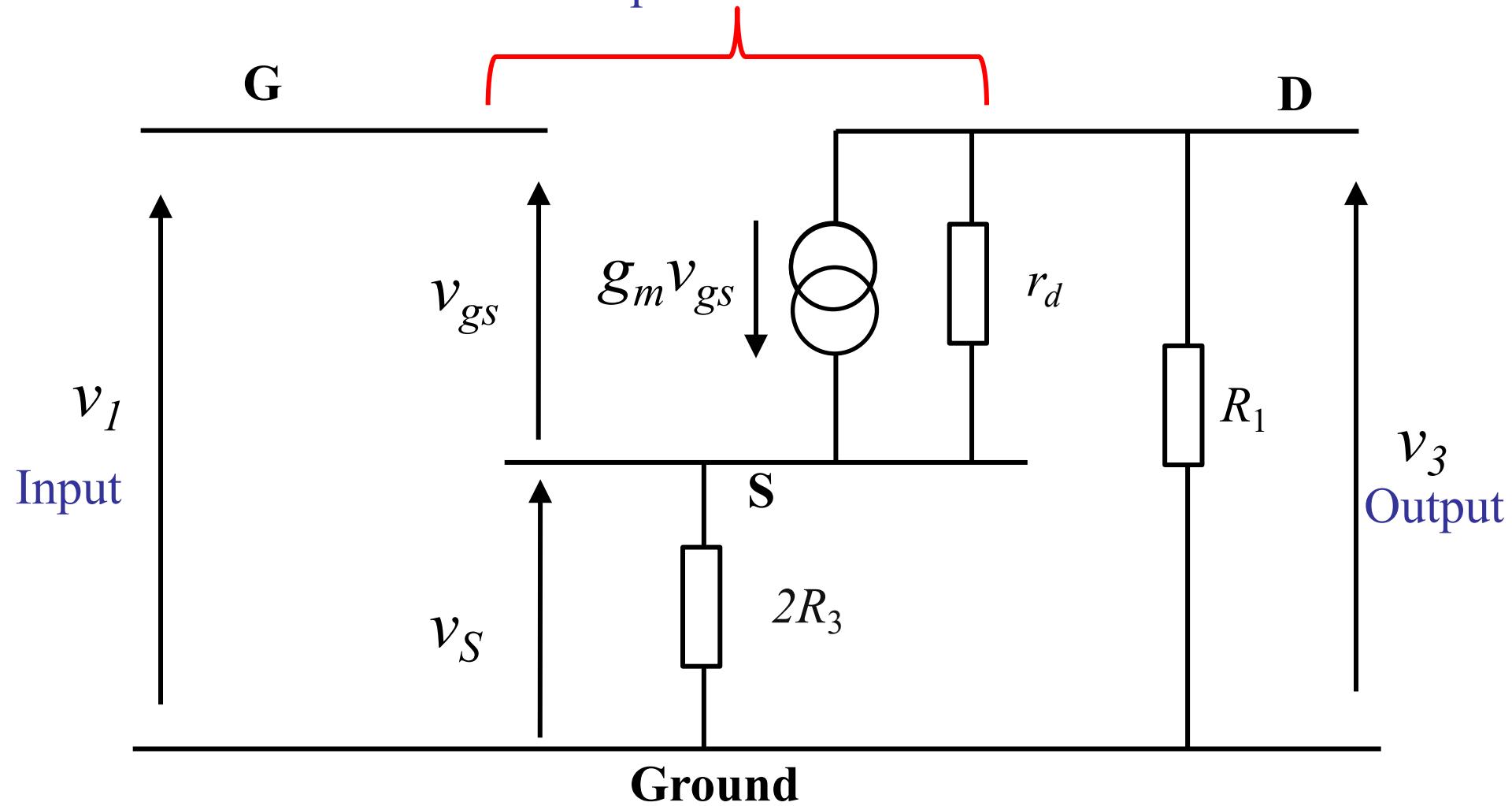
As $v_1 = v_2$, the same changes are occurring in on both sides of the circuit, hence we can use the 'half circuit approach'.

This involves splitting R_3 into two parallel resistors each of value $2R_3$



Small signal model

Can swap with BJT



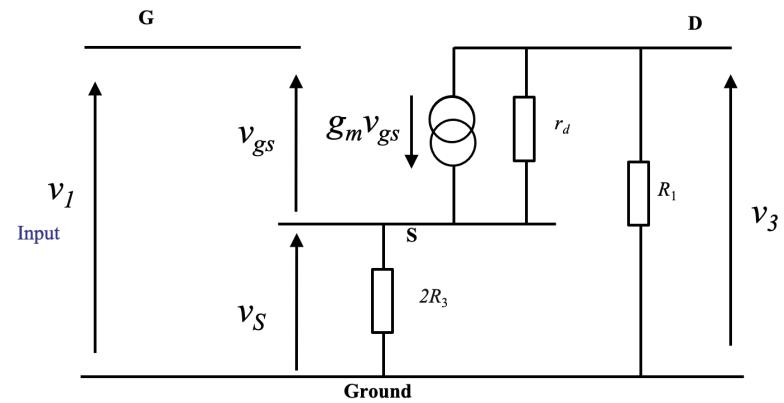
Sum voltages and currents at input and output to eliminate v_{gs}

Sum currents at the source

$$g_m v_{gs} + \frac{v_3 - v_S}{r_d} + \frac{0 - v_S}{2R_3} = 0$$

Sum currents at the drain

$$\frac{v_3}{R_1} + g_m v_{gs} + \frac{v_3 - v_S}{r_d} = 0$$



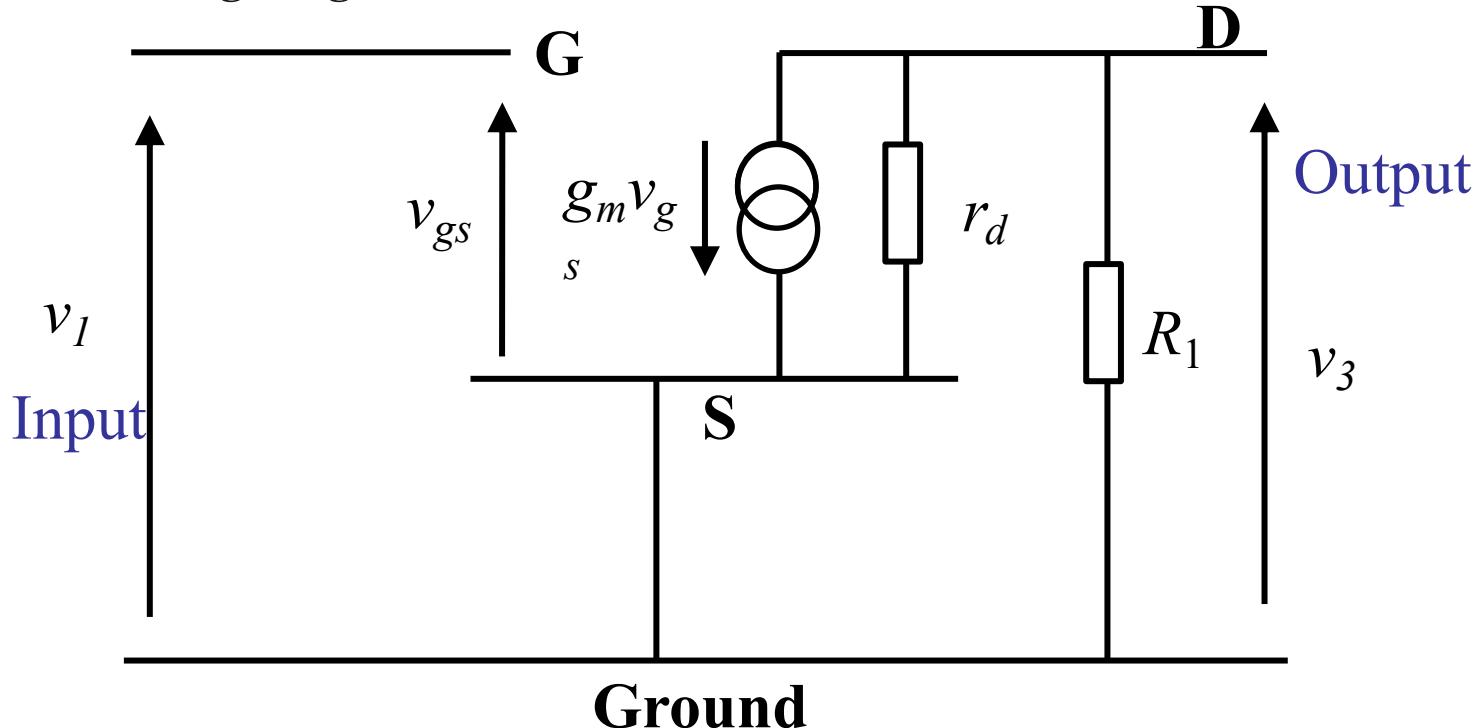
Using $v_{gs} = v_I - v_s$ leads to an expression for common-mode gain

$$\frac{v_3}{v_1} = - \frac{g_m R_1}{1 + 2g_m R_3 + 2 \frac{R_3}{r_d} + \frac{R_1}{r_d}}$$

Similar result for $\frac{v_4}{v_2}$

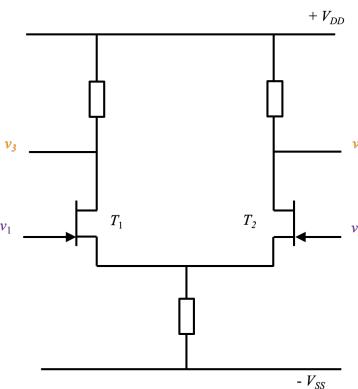
Note the presence of R_3 in the bottom line - increasing R_3 reduces the gain.

Differential gain - Small signal circuit – R_3 experiences no change in voltage – small signal ground



Sum currents at the drain

$$\frac{v_3}{R_1} + g_m v_{gs} + \frac{v_3}{r_d} = 0$$



For differential (often referred to as **balanced**) signals the change in current through one transistor is matched by an equal and opposite change in the current through the other. Hence the current through R_3 is constant, so v_s is constant also and therefore is effectively at earth potential for small signals (ie it looks like a DC source).

As $v_{gs} = v_I$, the expression for gain becomes

$$\frac{v_3}{v_1} = -\frac{g_m}{\frac{1}{r_d} + \frac{1}{R_1}}$$

This result can also be obtained by putting $R_3 = 0$ in the expression for common mode gain.

The CMRR is the ratio of differential to common-mode gain.

We want the differential gain to be as large as possible and the common mode gain to be as small as possible.

Therefore, the higher the CMRR of a differential amplifier the better it is.

$$\text{CMRR} = \frac{\text{Differential gain}}{\text{common - mode gain}} = \left| \frac{-\frac{g_m}{\frac{1}{r_d} + \frac{1}{R_3}}}{1 + 2g_mR_3 + 2\frac{R_3}{r_d} + \frac{R_1}{r_d}} \right|$$

$$= \frac{1 + 2g_mR_3 + 2\frac{R_3}{r_d} + \frac{R_1}{r_d}}{1 + \frac{R_3}{r_d}} \approx 2g_mR_3$$

Note – the bigger R_3
the bigger the **CMRR**

Example: $r_d = 100 \text{ k}\Omega$, $g_m = 5 \text{ mS}$ (5 mA/V), $R_3 = 10 \text{ k}\Omega$ and $R_1 = R_2 = 1 \text{ k}\Omega$

$$\text{CMRR} = 100.2 \text{ (exact value)}$$

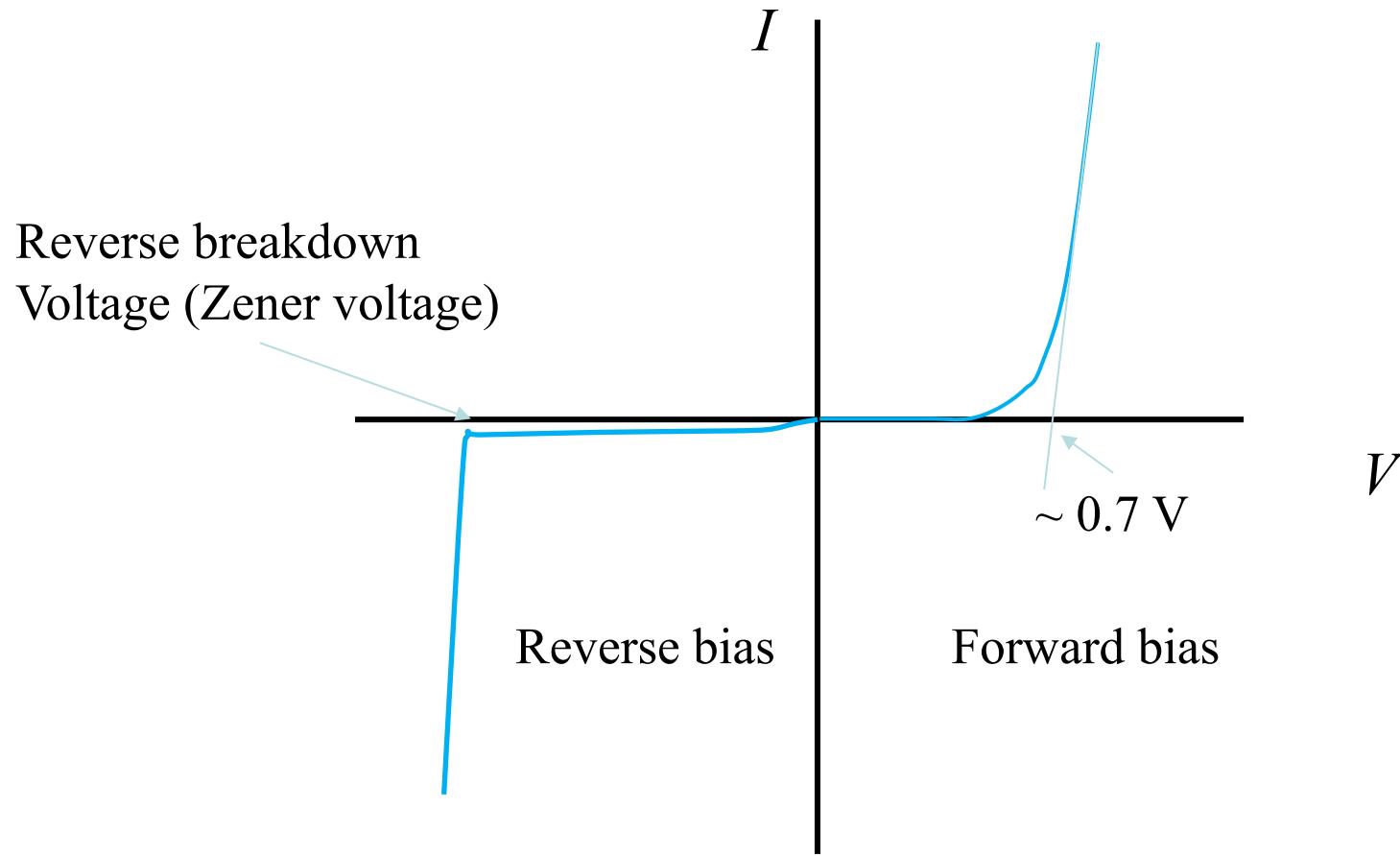
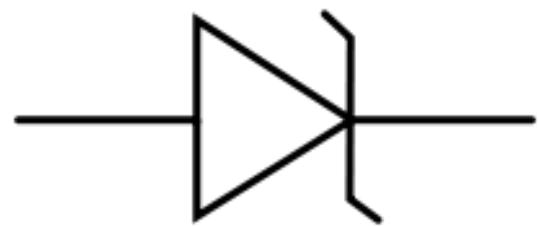
$$\text{CMRR} = 100 \text{ (approx value from CMRR} = 2 g_m R_3)$$

R_3 plays a critical role in setting the CMRR and has to be as large as possible, giving rise to the name 'long-tailed pair'.

However, to maintain a reasonable dc bias current flow through R_3 , the negative supply voltage ($-V_{ss}$) increases with increasing R_3 , soon reaching an absurd value.

An effective answer is the electronic current source, as described later.

The Zener diode



Zener effect: based on Quantum tunneling

Use of a Current Source with the Differential Amplifier

DC opera

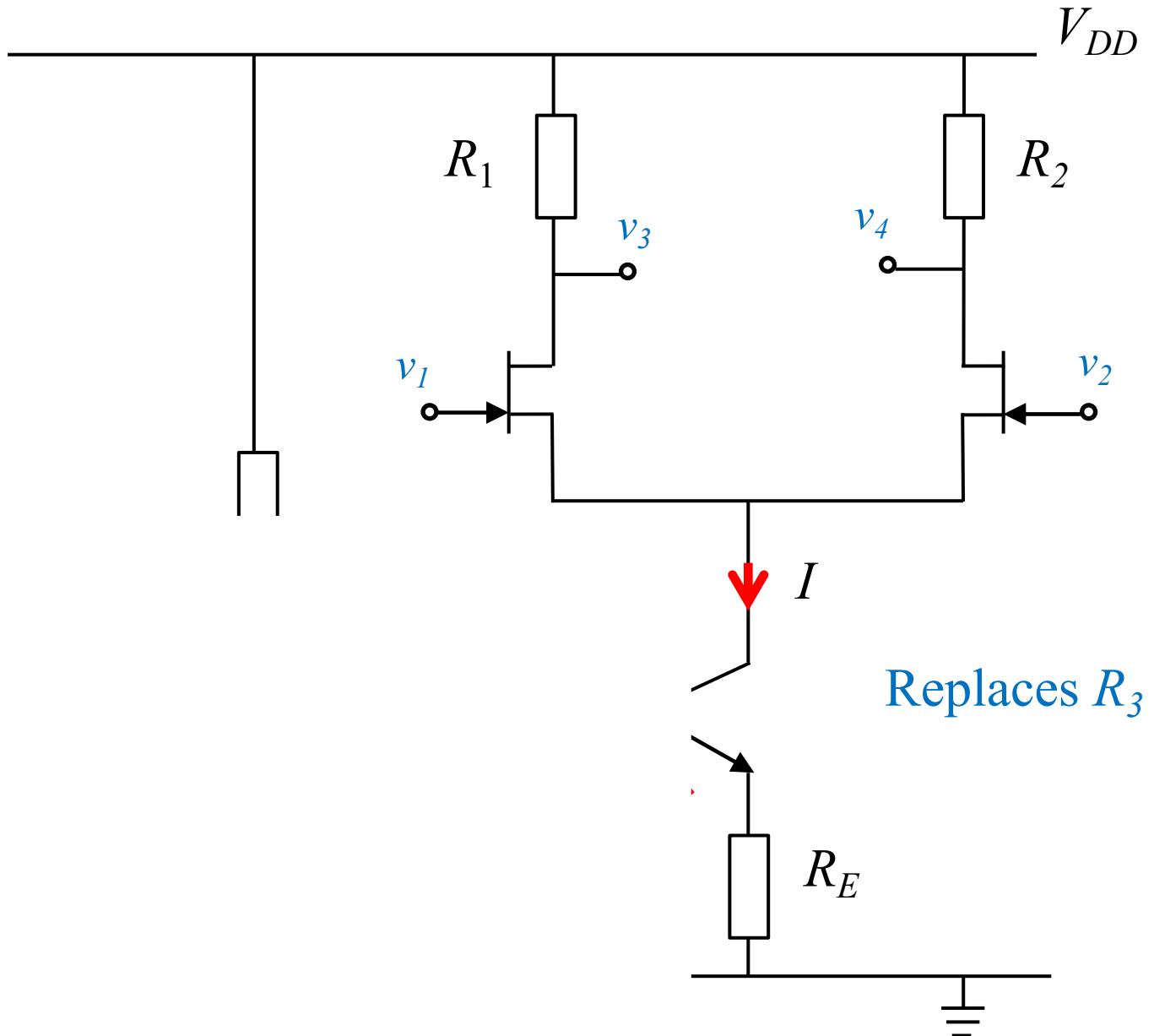
$$I_Z > I_B$$

$$V_Z = 5.7\text{V}$$

$$V_{BE} = 0.7\text{V}$$

$$R_E = 1\text{k}\Omega$$

$$I = 5\text{mA}$$



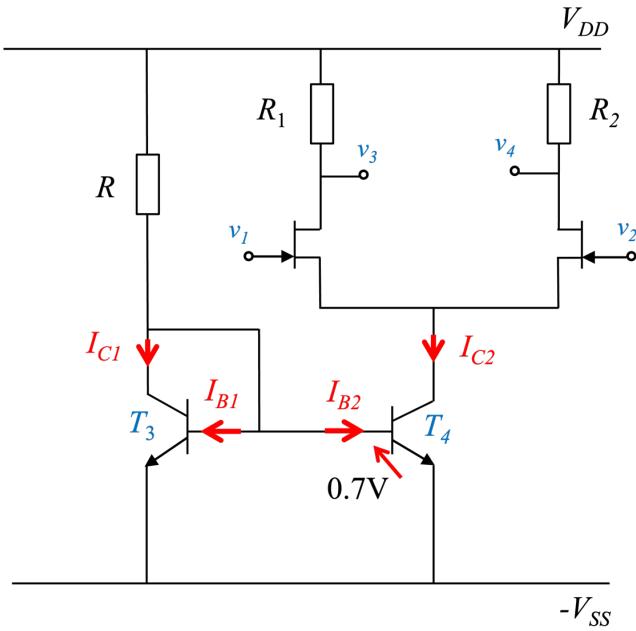
The Zener diode Z has an essentially constant voltage drop over a range of currents, in this case flowing through R . The current through R is set to be much greater than the base current of the transistor. If the voltage across the Zener diode is several times the base-emitter voltage (V_{BE}), the voltage across the emitter resistor R_E will be essentially constant, even if there are small changes in V_{BE} . The emitter current is therefore constant, and as the base current is usually a very small fraction of the emitter current, the collector current I_C is constant also. Of course, for correct operation the collector operating point must remain in the linear region of the transistor's characteristics.

The small-signal impedance looking into the collector of the transistor is very high.

For example $20\text{ M}\Omega$ is typical for an operational amplifier such as the LM709.

Hence the CMRR of the LM709 is typically 10^5 (100 dB) which is much greater than could be achieved with a resistor.

The Current Mirror Circuit



For T_3 $V_{BE} = V_{CE} = 0.7$ V and if T_3 and T_4 are transistors with a high h_{FE} (> 100) then the base currents I_{B1} and I_{B2} are small and can be ignored.

If T_3 and T_4 are identical transistors and $V_{BE1} = V_{BE2}$ and the collector currents I_{C1} and I_{C2} will be equal (they “mirror” each other).

The current mirror can be used as a load for the long-tailed pair instead of resistors R_3 and R_4 . As well as providing a single output as is usually desired in operational amplifiers, combining the difference of the outputs from the two transistors increases the differential gain while greatly reducing the common mode gain, thereby increasing the common-mode rejection ratio.

This is a convenient way of fixing the current through a load (between v_3 & v_4)

In making operational amplifiers as integrated circuits it is easy to make transistors and relatively easy to make resistors over a limited range of resistance. However, it is inconvenient to include components such as Zener diodes. An elegant solution to the problem of providing current sources in operational amplifiers is a circuit known as the current mirror.