

# IB Paper 8: Electrical elective

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Sections 7 & 8

*Calculating I-V characteristics, MOSFETS, TFTs,  
Scaling laws and Displays*

# Contents

- Charges -> electrostatics ->  $I$ - $V$  characteristics
- Recap on Gauss's law -> Poisson's equation
- Some examples

Starting point: in a large parallel plate capacitor, if the insulator is ideal, the middle regions of the capacitor (not including fringe effects from edges) can be said to have uniform field (i.e. field line density is uniform in space). If the voltage across the capacitor is  $V_a$  and the thickness of the insulator is  $L$ , the electric field in the insulator is  $V_a / L$ .

But what happens if the insulator has charges present in it? Or if the insulator is replaced by a semiconductor? In general, (i.e. stepping outside the specific example of the parallel plate capacitor) how do we identify electric fields in a material that has charges present?

# Poisson's equation

Gauss's law tells us that the flux of electric field,  $E$  through any closed surface,  $S$  is proportional to the amount of charge,  $Q$  enclosed by that surface.

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In integral form:

$$\oint\!\!\!\oint E \cdot dS = \frac{Q}{\epsilon}$$

Making use of the divergence theorem, i.e.

$$\oint\!\!\!\oint E \cdot dS = \iiint \nabla \cdot E dv$$

We can express the charge,  $Q$  as an integral over a charge density,  $\rho$

$$i.e. Q = \iiint \rho dv$$

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This leads us to:

Therefore, for any volume:

$$\iiint \nabla \cdot E dv = \iiint \frac{\rho}{\epsilon} dv$$

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$$\nabla \cdot E = \frac{\rho}{\epsilon}$$

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Denote potential by  $\varphi$ :

$$E = -\frac{d\varphi}{dx} \implies \nabla \cdot E = -\frac{d^2\varphi}{dx^2}$$

Combining:

$$\frac{d^2\varphi}{dx^2} = -\frac{\rho}{\epsilon}$$

# Example 1: Electrostatics in a Semiconductor

Here we have an insulator in a parallel plate capacitor. The insulator has no charges (mobile or fixed). One end ( $x = 0$ ) is at potential  $V_a$  while the other end ( $x = L$ ) is at 0 (or ground) potential. What is the field and potential variation in the insulator?

**Boundary conditions:**

$$\varphi(x = 0) = V_a \quad \varphi(x = L) = 0$$

**Gauss's law:**

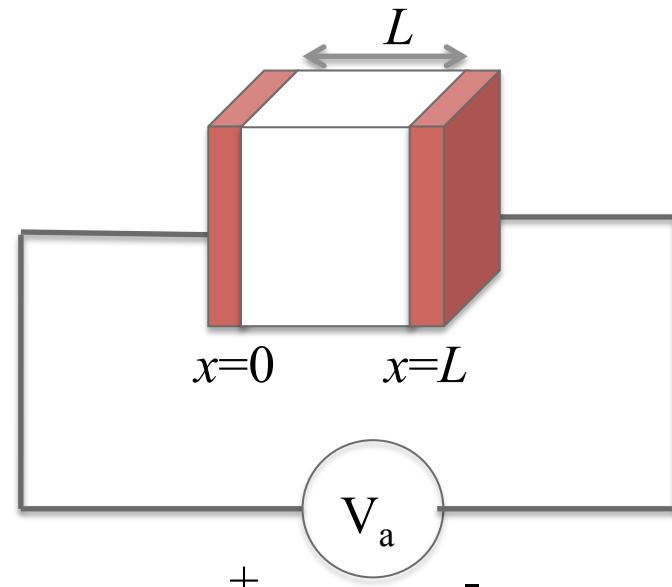
$$\frac{dE}{dx} = \frac{\rho}{\epsilon} = 0 \Rightarrow E = C \text{ (constant)}$$

$$\Rightarrow E = -\frac{d\varphi}{dx} = C$$

$$\Rightarrow \varphi = -Cx + D \text{ (both } C \text{ & } D \text{ are constants)}$$

**Using the Boundary conditions:**

$$D = V_a \quad C = \frac{V_a}{L}$$



$$\Rightarrow E = \frac{V_a}{L} ; \varphi = V_a - \frac{V_a}{L}x$$

# Electrostatics in a Semiconductor

Generally in semiconductors there can be two kinds of charges:

## 1.) Mobile Charges: e.g. electrons and holes.

They will respond to any electric field and move about. Therefore their concentration will depend on the potential in the semiconductor (Boltzmann distribution)

## 2.) Fixed Charges: eg. Dopant ions

After doping, the dopants are ionized. This means that:

(i) The n-type donor dopant has given up its extra electron and is therefore positively charged. i.e.  $\text{Donor} \rightarrow \text{Donor}^+ + e^-$ . Here  $\text{Donor}^+$  is the positively charged donor ion.

(ii) The p-type acceptor dopant has given up its hole and is therefore negatively charged. i.e.  $\text{Acceptor} \rightarrow \text{Acceptor}^- + p^+$ . Here  $\text{Acceptor}^-$  is the negatively charged acceptor ion.

Note that by doping, the semiconductor is still neutral.

Sometimes a region in a semiconductor might be *depleted*. i.e. it is nearly void of mobile carriers. If this region is doped, the only charges present will be the dopant ions.

## Example 2: Electrostatics in a Semiconductor

Consider a p-doped semiconductor with acceptor dopant concentration of  $N_A$  per unit volume. The region from  $x = 0$  to  $x = d$  in the semiconductor is depleted. Find the electric field profile in this region if the electric field at  $x \geq d$  is zero. Also, find the potential difference between the points  $x = 0$  and  $x = d$ .

Charge density in a semiconductor:

$$\rho = q(N_D + p - N_A - n)$$

Depletion region, p-type:  $\rho = -qN_A$

$$\frac{dE}{dx} = \frac{\rho}{\epsilon} = -\frac{qN_A}{\epsilon}$$

$$\Rightarrow E = -\frac{qN_A}{\epsilon}x + C$$

Boundary conditions: @  $x = d$ ,  $E = 0$

$$\Rightarrow C = \frac{qN_A}{\epsilon}d$$

$$\Rightarrow E = \frac{qN_A}{\epsilon}(d - x)$$

$$E = -\frac{d\varphi}{dx} \Rightarrow \varphi = \int_0^d \frac{qN_A}{\epsilon}(x - d)dx \\ \Rightarrow \varphi = \frac{qN_A}{\epsilon} \left( \frac{x^2}{2} - xd \right)$$

Integration limits then being used tell us:

$$\varphi_{0 \rightarrow d} = -\frac{qN_A}{\epsilon} \frac{d^2}{2}$$

## Example 2b: With some numbers

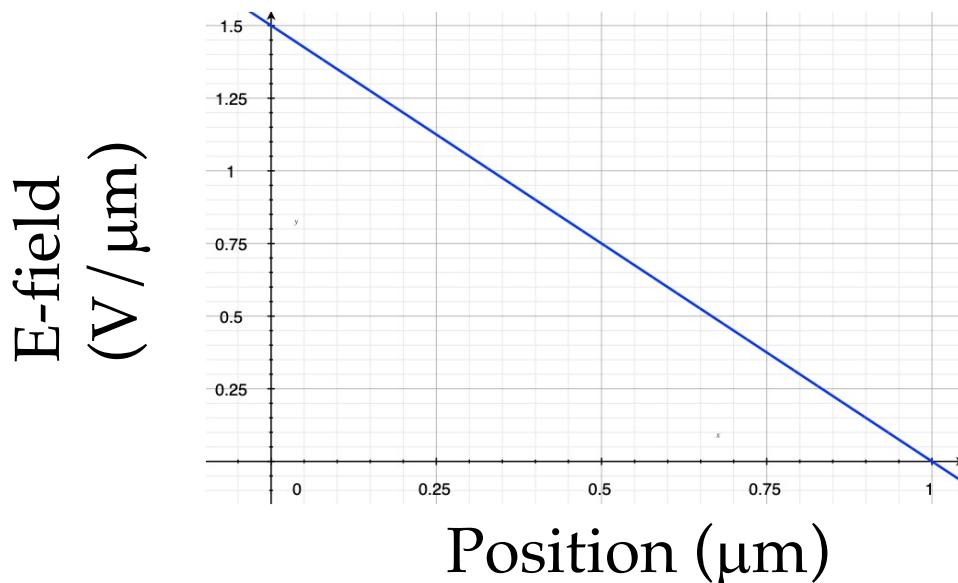
Assume the relative permittivity of the material is 12;  $N_A = 1 \times 10^{21} / \text{m}^3$ ;  $d = 1 \mu\text{m}$ . Plot the Electric field and calculate the potential across the depletion region.

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Electric field

$$E = \frac{qN_A}{\varepsilon}(d - x)$$

Numerically,  $E = 1.5 \times 10^6 (1 - x) \text{ V/m}$ ,  
with  $x$  in  $\mu\text{m}$



Potential

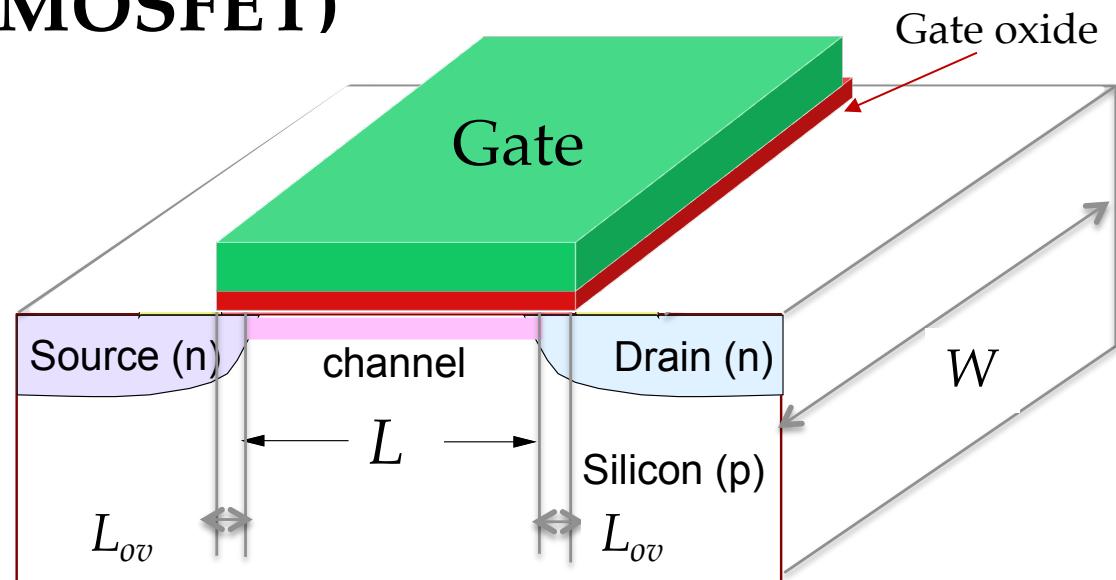
$$\varphi_{0 \rightarrow d} = -\frac{qN_A d^2}{\varepsilon} \frac{1}{2}$$

Numerically,  $\varphi = 0.375 \text{ V}$

# Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

*Electrodes:* Gate (**G**), Source (**S**) and Drain (**D**).

A 4th terminal (not shown) called the **body contact** connects to the bulk silicon (the p silicon in the figure). The MOSFET shown in the figure is a n-type or n-channel MOSFET. It will have n-doped S and D contacts.



**Channel length, Channel Width, Aspect Ratio and Overlap Length:** The distance between the Source and Drain is called the *channel length*  $L$ . The width of the MOSFET as indicated is the *channel width*,  $W$ . The ratio  $W/L$  is called the *aspect ratio*. Since the 1990s,  $L$  has been gradually reduced leading to faster electronics. The scaling down of the MOSFET feature size is a key step towards improvement – Moore's Law – number of transistors in an area of a dense integrated circuit doubles every year.

The gate typically overlaps the source and drain contacts by an *overlap length*  $L_{ov}$ .

# Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

## *Metal-Insulator-Semiconductor Stack and Basic Operation*

The key element of the MOSFET is the metal-insulator-semiconductor interface (MIS). Since silicon oxide has been predominantly used as the insulator, the MIS was called the MOS. However, an equivalent name is Metal Insulator Semiconductor Field Effect Transistor (MISFET).

During operation, a channel of desirable resistance is created between source to drain. This permits the signals at the source to be communicated to the drain when the channel resistance is low. When the channel disappears or when the channel resistance is made very high, the drain and source are open circuited and lose contact.

The gate controls the resistance of the channel via *field effect* i.e via the application of a voltage on the gate, the electric field due to the gate is felt in the channel. The insulator prevents any current to flow from the gate to the semiconductor. Hence an ideal MOSFET has very large gate impedance.

# Depletion & Enhancement-mode MOSFET

## Depletion Mode MOSFET:

This is normally in the ON state when the gate voltage is zero. This is achieved by doping the semiconductor at the semiconductor insulator interface. The application of a gate voltage is then used to turn off the transistor (i.e. open circuit the source-drain).

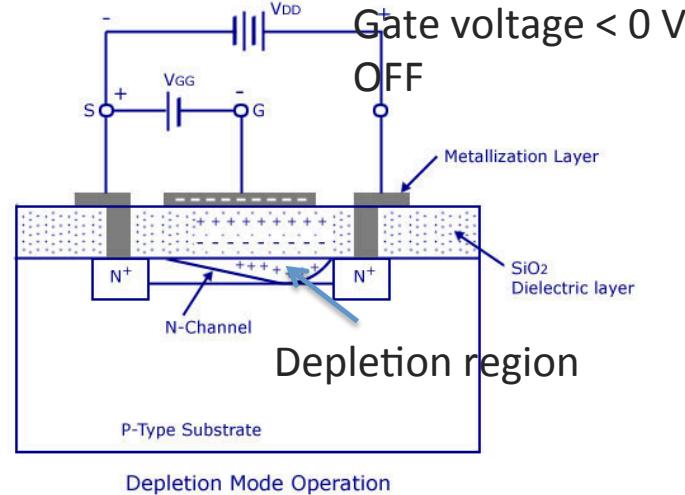
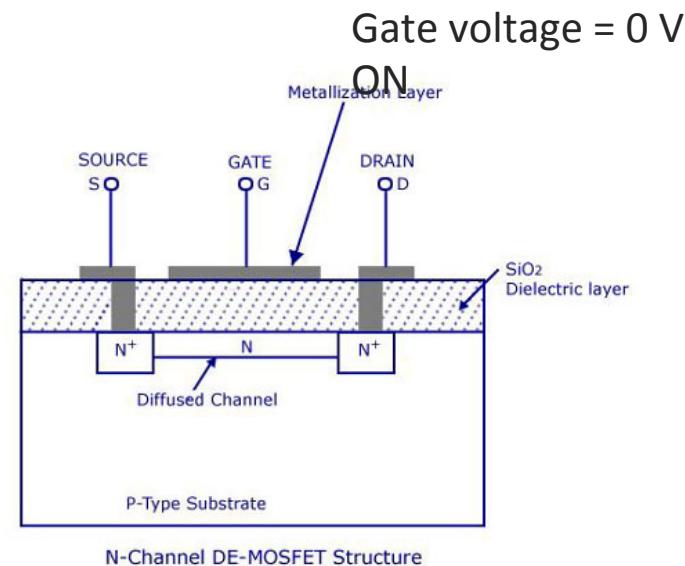
For example, for an n-channel MOSFET, the interface is doped n-type. The channel therefore has excess electrons and the resistance can be calculated as discussed before. The channel is normally on and short circuits the source and drain.

To open circuit the source and drain, a -ve gate voltage is applied. The -ve voltage pushes the electrons away from the interface thereby creating a depletion region (a region void of free carriers). This adds a large resistor in between the source and drain and open circuits it.

Intermediate control of the gate voltage permits only a portion of the channel to be depletion and can control the resistance (analog operation).

The gate voltage needed to move from off to on state is called the *threshold voltage*. The threshold voltage for a n-depletion MOSFET is therefore -ve.

Operation is symmetric for p-MOSFET



## Enhancement Mode MOSFET:

This is normally in the OFF state when the gate voltage is zero.

The application of a gate voltage is then used to turn on the transistor (i.e. short circuit the source-drain).

An n-channel enhancement mode MOSFET has a p-type body.

Note that the interface is **not** doped n-type.

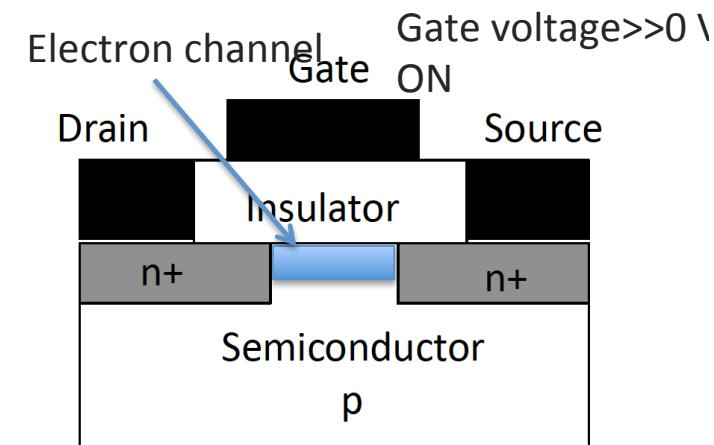
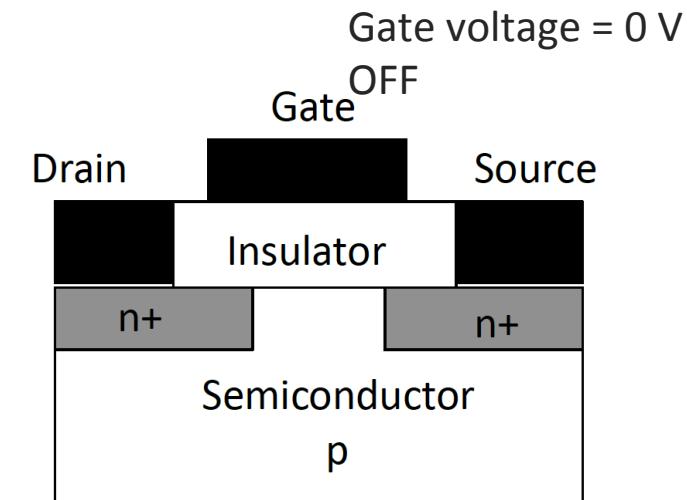
When the gate voltage is made  $>0$ , the holes near the interface are pushed away and the interface is depleted. This operation regime is called 'depletion' mode.

However as the gate voltage is made more and more positive, electrons (thermally generated) begin to appear near the interface due to the highly positive gate voltage. Since the electrons are the minority carriers (p-type body implies more holes than electrons, holes are in the majority), the interface is said to be 'inverted' with carriers of the opposite type as the majority carriers. The region is called the 'inversion' mode of operation.

It is the electron channel that now short circuits the drain-source and turns on the MOSFET.

Intermediate control of the gate voltage controls the electron concentration and therefore the resistance (analog operation). The gate voltage needed to move from off to on state is called the *threshold voltage*. The threshold voltage for a n-enhancement MOSFET is therefore +ve.

This is the most commonly used MOSFET. Operation is symmetric for p-MOSFET.



# Depletion mode MOSFET

At what gate voltage,  $V_g$ , will the doped region be fully depleted? Let us call that gate voltage,  $V_p$  (pinchoff voltage). Let us assume the entire n-doped implant is at potential  $V_c$  and a voltage  $V_{ox}$  is dropped across the oxide.

Therefore when a partial depletion of thickness,  $x=x_d$  occurs at some gate voltage  $V_g$ , the potential at  $x=0$  is  $V_g - V_{ox}$ . When full depletion occurs, i.e. when the width of the depletion region  $x_d = D$ , the gate voltage is  $V_p$  and the potential at  $x=0$  is  $V_p - V_{ox}$ .

To model this, we need to apply Poisson's equation:

$$\frac{dE}{dx} = \frac{\rho}{\epsilon} = \frac{qN_D}{\epsilon} \quad \Rightarrow \quad E = \frac{qN_D}{\epsilon}x + C \quad \text{..Within the Depletion region}$$

Boundary conditions: @  $x = x_d$ ,  $E = 0$

$$\Rightarrow C = \frac{qN_D}{\epsilon}x_d \quad \Rightarrow \quad E = \frac{qN_D}{\epsilon}(x - x_d)$$

$$E = -\frac{d\varphi}{dx} \quad \Rightarrow \quad \varphi = \frac{qN_D}{\epsilon} \left( x_d x - \frac{x^2}{2} \right) + C$$

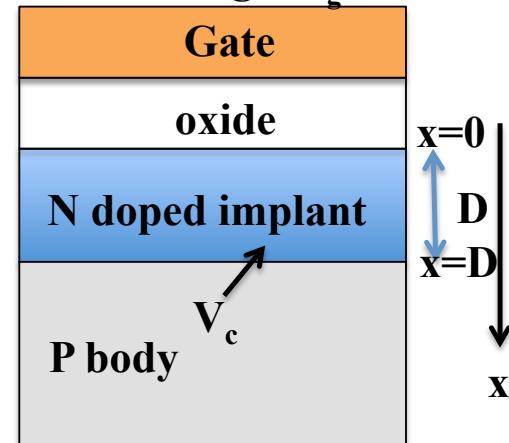
$$\varphi_{0 \rightarrow x_d} = -\frac{qN_D}{\epsilon} \frac{x_d^2}{2}$$

$$\text{But, } \varphi(x_d) = V_c \quad \Rightarrow \quad \varphi(0) = -\frac{qN_D}{\epsilon} \left( \frac{x_d^2}{2} \right) + V_c = V_g - V_{ox}$$

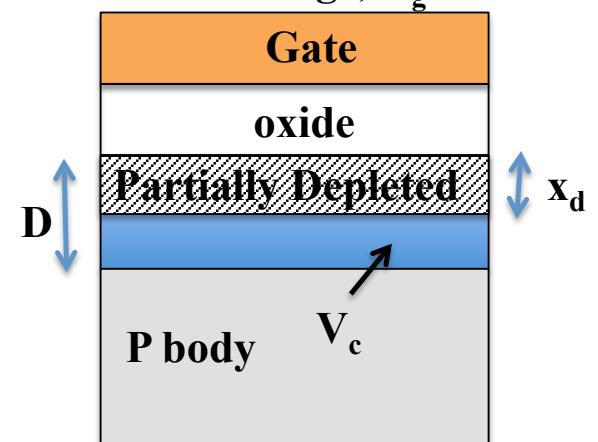
Full depletion happens when  $x_d = D$

$$\Rightarrow \varphi(0) = -\frac{qN_D}{\epsilon} \left( \frac{D^2}{2} \right) + V_c \Rightarrow V_p = -\frac{qN_D}{\epsilon} \left( \frac{D^2}{2} \right) + V_c + V_{ox}$$

Gate voltage,  $V_g = 0$



Gate voltage,  $V_g < 0$



# Depletion Mode MOSFET

(not for examination)

## More correct situation

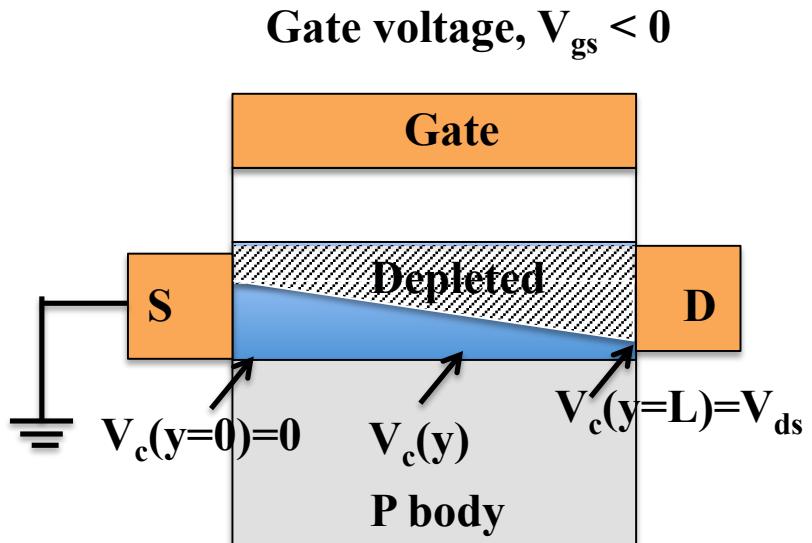
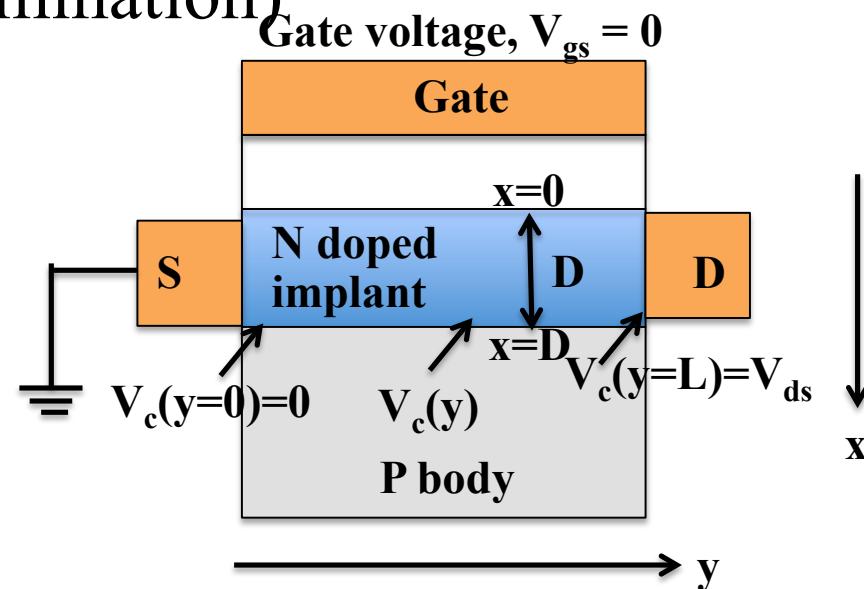
We now apply a gate and drain voltage. The source is at ground and all voltages are with respect to the source.

$$\begin{aligned} \text{Gate voltage} &= V_{gs} \\ \text{Drain voltage} &= V_{ds} \end{aligned}$$

The width of the device is  $W$  (going into the page - not shown)

We define an  $x$ -direction that goes into the device.  
 $x=0$  is the insulator-doped implant interface  
The doped implant has thickness  $D$

We define the  $y$ -direction from source to drain.  
 $y=0$  is the source and  $y=L$  is the drain.  
Since the n-doped implant connects source-drain, it has a potential (called the channel potential)  $V_c(y)$  that varies from 0 to  $V_{ds}$  as  $y$  goes from 0 to  $L$ .



# Depletion Mode MOSFET

(not for examination)

At some point  $y$ , a section of length  $dy$  will tell us that the depletion width is  $x_d(y)$ . The voltage drop across this section is  $dV_c$ .

The resistance at that section is

$$dR = \frac{1}{q\mu_n N_D} \frac{dy}{(D - x_d(y))W}$$

If the current from drain to source is  $I_{ds}$

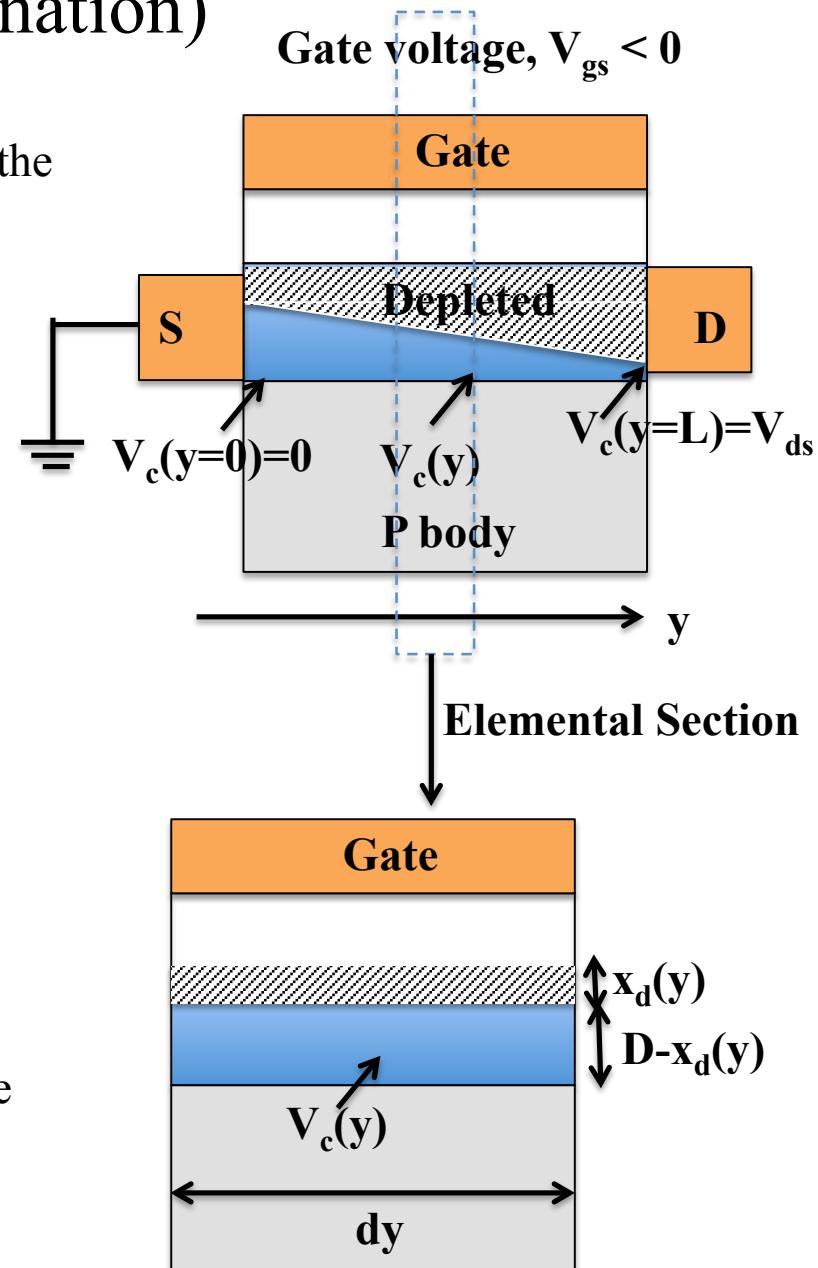
$$dV_c = I_{ds}(dR) = \frac{I_{ds}}{q\mu_n N_D} \frac{dy}{(D - x_d(y))W}$$

From the solution to Poisson's equation we know

$$\varphi(0) = -(qN_D / \epsilon)(x_d^2 / 2) + V_c = V_{gs} - V_{ox}$$

$$\Rightarrow x_d = (2\epsilon(V_{ox} + V_c - V_{gs}) / qN_D)^{1/2}$$

We substitute this in the above expression and solve the differential equation to identify the current voltage characteristics.



# Transit Time and Maximum Current

How long does it take for the electron to go from source to drain?

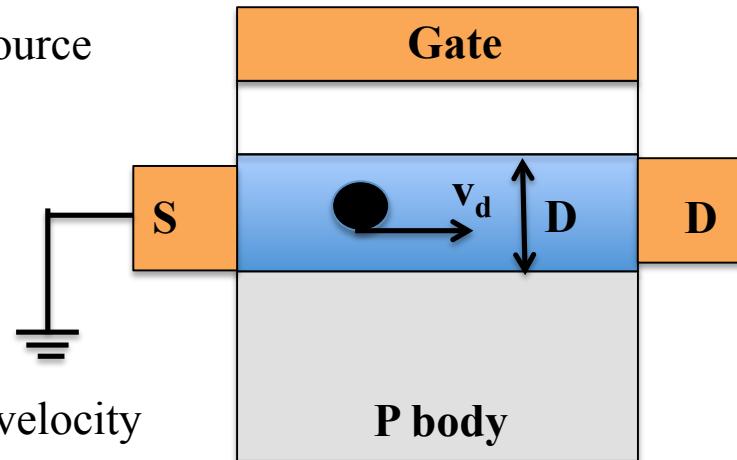
At low electric fields,

$$v_d = \mu E$$

At high fields, velocity saturates

Thus, *transit time*  $t$  is limited by scattering limited velocity

$$v_s = 10^5 \text{ m/s}$$



$$I_{sat} = \frac{Q}{t} = \frac{qN_D WDL}{t} = qN_D WD v_s$$

# Thin Film Transistors (TFTs)

Transistors built by depositing thin films on substrates (e.g. glass, plastic). Thin Film Transistors (TFTs) are the building blocks of large area electronic systems such as displays. Their current-voltage characteristics are similar to **enhancement mode** MOSFETs, but with some differences due to the nature of the materials used.

At  $V_{gs} = 0$ , there is no channel.

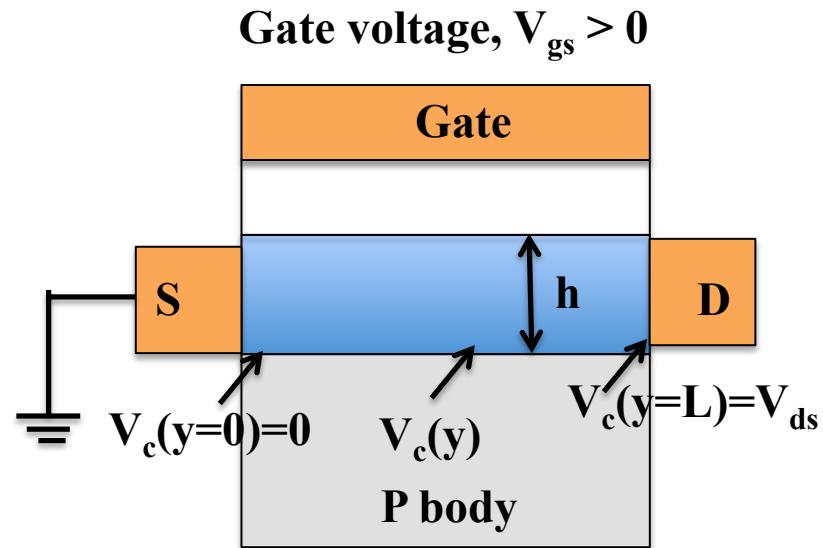
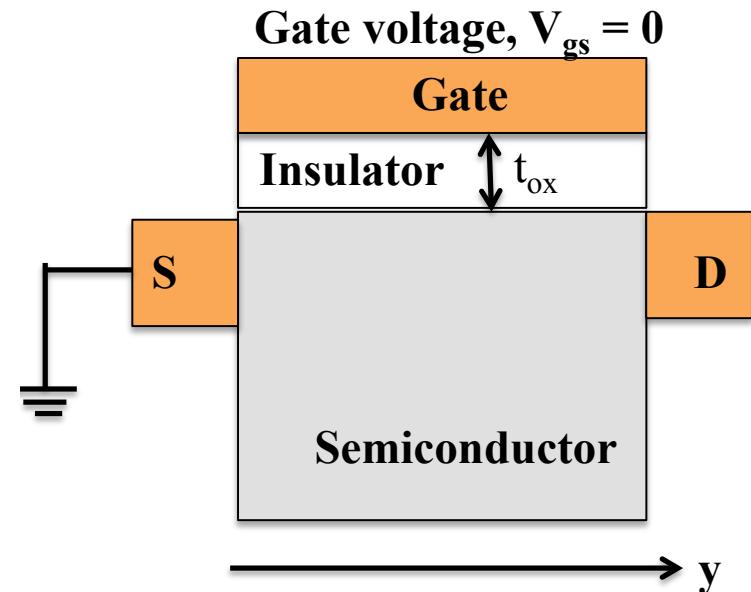
At  $V_{gs} > 0$ , threshold voltage,  $V_T$ , there is a conductive channel of electrons between the source and drain. The potential within the channel,  $V_c(y)$  varies from source to drain. If we imagine the channel to be a sheet of electrons of thickness  $h$ , the current from source to drain,  $I_{ds}$ , is

$$\frac{I_{ds}}{Wh} = qn v_d = qn \mu E = qn \mu \frac{\partial V_c}{\partial y}$$

What is  $qn$ , i.e. the channel charge per unit volume?

If  $C_{ox} = \epsilon_{ox}/t_{ox}$  is the insulator capacitance per unit area,

$$qn = \frac{C_{ox} (V_{gs} - V_T - V_c(y))}{h}$$



# Thin Film Transistors

Therefore

$$I_{ds} = qn\mu \frac{dV_c}{dy}(Wh) = \frac{C_{ox}(V_{gs} - V_T - V_c)}{h} \mu \frac{dV_c}{dy}(Wh) = \mu WC_{ox}(V_{gs} - V_T - V_c) \frac{dV_c}{dy}$$

Solve the differential equation

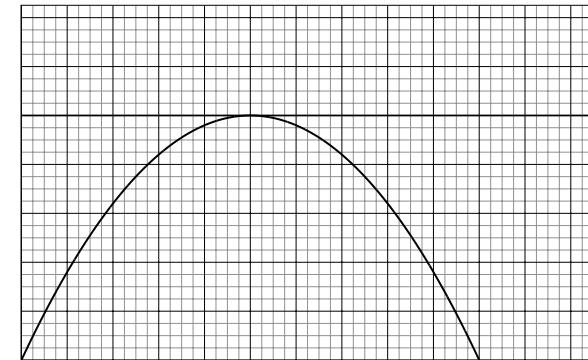
$$\int_0^L I_{ds} dy = \int_0^{V_{ds}} \mu WC_{ox}(V_{gs} - V_T - V_c) dV_c \Rightarrow I_{ds} = \mu \frac{W}{L} C_{ox} ((V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2})$$

The above expression is true only if  $V_{ds} < V_{gs} - V_T$  (**Linear operation**). In linear operation, the transistor behaves like a resistor.

If  $V_{ds} \geq V_{gs} - V_T$ , there will be a region near the drain where the channel cannot exist.

This is called ‘pinch off’. When  $V_{ds} \geq V_{gs} - V_T$ , the current saturates and becomes independent of  $V_{ds}$  (**Saturation operation**). In saturation operation the transistor behaves like a gate controlled current source (independent of  $V_{ds}$ ). Therefore to calculate the current in saturation, we substitute  $V_{ds} = V_{gs} - V_T$ . Therefore we have,

$$I_{ds} = \begin{cases} \mu \frac{W}{L} C_{ox} ((V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}) & \text{When } V_{ds} < V_{gs} - V_T, \text{ Linear Operation} \\ \frac{\mu W}{2} C_{ox} (V_{gs} - V_T)^2 & \text{When } V_{ds} \geq V_{gs} - V_T, \text{ Saturation Operation} \end{cases}$$

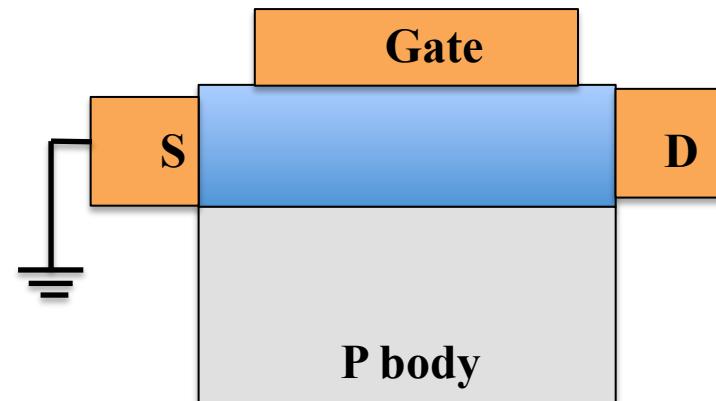


# Metal Semiconductor Field Effect Transistor (MESFET)

Key difference between MESFET and MOSFET is that there is no insulator between Gate Metal and Semiconductor.

When a metal (M) interfaces with a semiconductor (S) there are two kinds of contacts that can be made:

- (i) Ohmic contact
- (ii) Schottky or Rectifying contact



An Ohmic contact will ensure a M-S junction that behaves like a resistor (to some extent). This is the kind of junction you want when you want to inject current from metal-semiconductor or vice-versa.

A Schottky junction forms a diode like contact. It results in the semiconductor interface with the metal being depleted of free carriers (forms a depletion region).

A MESFET uses a gate metal that forms a Schottky contact with the semiconductor. The resulting depletion region can be controlled to control the current between source-drain.

The MESFET is used for very high frequency operations (microwave communication and radar).

# Scaling of Transistors

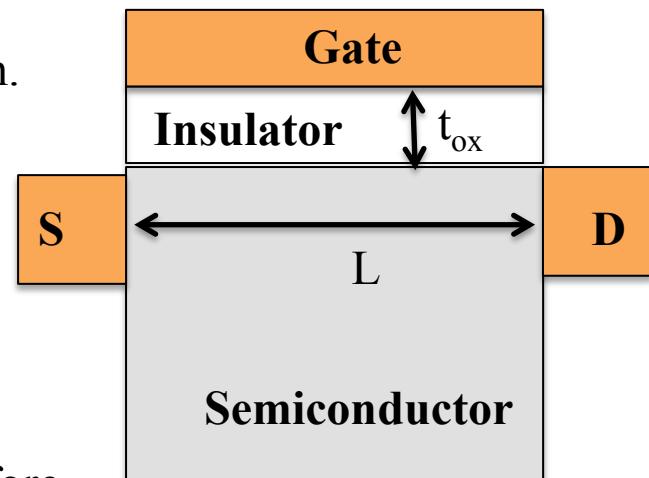
To reduce the size of the integrated circuit chips, reduce power consumption and increase speed, the MOSFETs are scaled down.

1970 - 2250 transistors in Intel 4004

2015 – 10000000000 transistors in SPARC M7

1970 – 10 microns channel length

2015 – 40nm channel length



Scaling implies: Reduce  $L$ ,  $W$  and  $t_{ox}$  by a factor of  $\alpha$ .

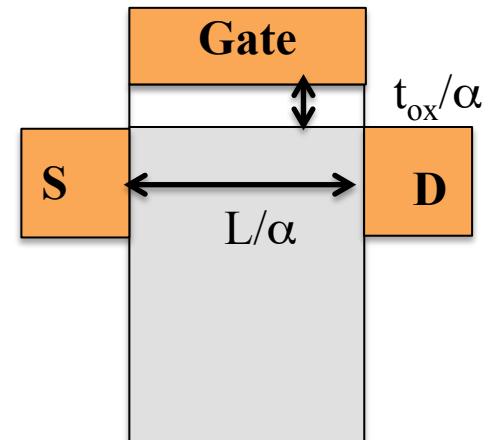
NOTE: Scaling down  $t_{ox}$  will increase tunnelling current. Therefore, we increase the permittivity of the dielectric and not change the oxide thickness. Therefore high permittivity dielectric are important. But let us keep this option aside for the moment.

How do we scale down?

There are two methods of scaling:

(i) Constant field scaling:

Need to keep field constant. If we scale down  $L$ ,  $W$  and  $t_{ox}$ , we should scale down applied voltages. Voltage levels not compatible with previous versions.



(i) Constant voltage scaling

Power supply voltage not reduced, therefore compatible with previous versions. But field becomes very large in the device.

# Scaling of Transistors

Parameter	Symbol	Constant Field Scaling	Constant Voltage Scaling
Gate length	$L$	$1/\alpha$	$1/\alpha$
Gate width	$W$	$1/\alpha$	$1/\alpha$
Field	$\mathcal{E}$	1	$\alpha$
Oxide thickness	$t_{ox}$	$1/\alpha$	$1/\alpha$
Substrate doping	$N_a$	$\alpha^2$	$\alpha^2$
Gate capacitance	$C_G$	$1/\alpha$	$1/\alpha$
Oxide capacitance	$C_{ox}$	$\alpha$	$\alpha$
Voltage	$V$	$1/\alpha$	1
Current	$I$	$1/\alpha$	$\alpha$
Power	$P$	$1/\alpha^2$	$\alpha$

# Materials

The choice of material plays a significant role in the development of MOSFETs.

Si – Best for general purpose MOSFET. It is a very well established technology and therefore can result in low cost electronics. Easy to get high purity wafers without defects.

GaAs – Very good for high frequency applications. It is also possible to make use of the phenomena like the Gunn effect to build devices. MESFETs are generally based on GaAs to supplement their high speed advantage. However, the crystals are quite defective.

GaN – Stable wide band gap semiconductor. Excellent material for high voltage applications. High performance optoelectronic materials for short wavelength (eg. blue and UV LEDs) are based on GaN. The very high breakdown voltages, high mobility of GaN has also made it an ideal candidate for high-power and high-temperature microwave applications.

For TFTs – Organic electronics based on ink jet printing is possible on a variety of substrates. This makes possible ideas such as wearable electronics, roll-roll manufactured electronics, flexible electronics (bendable displays etc).

# IB Paper 8: Electrical elective

Easter term 2023

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## 8. *Displays*

# Active Matrix Displays

**Active Matrix Display:** Pixel Control Transistors + Light Emitting Material + External Drivers

## LIGHT MODULATORS:

### Display Elements based on Modulating External Light:

Constant external light source.

Material Acts as a ‘Valve’ to modulate intensity. The modulation is achieved by mechanically moving the material by the application of external electric fields.

Eg. Liquid crystal displays (LCD), e-ink display

External light source for LCD: backlight (LCD modulates the light transmitted)

External Light source for e-ink: ambient light (-ink modulates the light reflected.)

### Display Elements based on Generating Light:

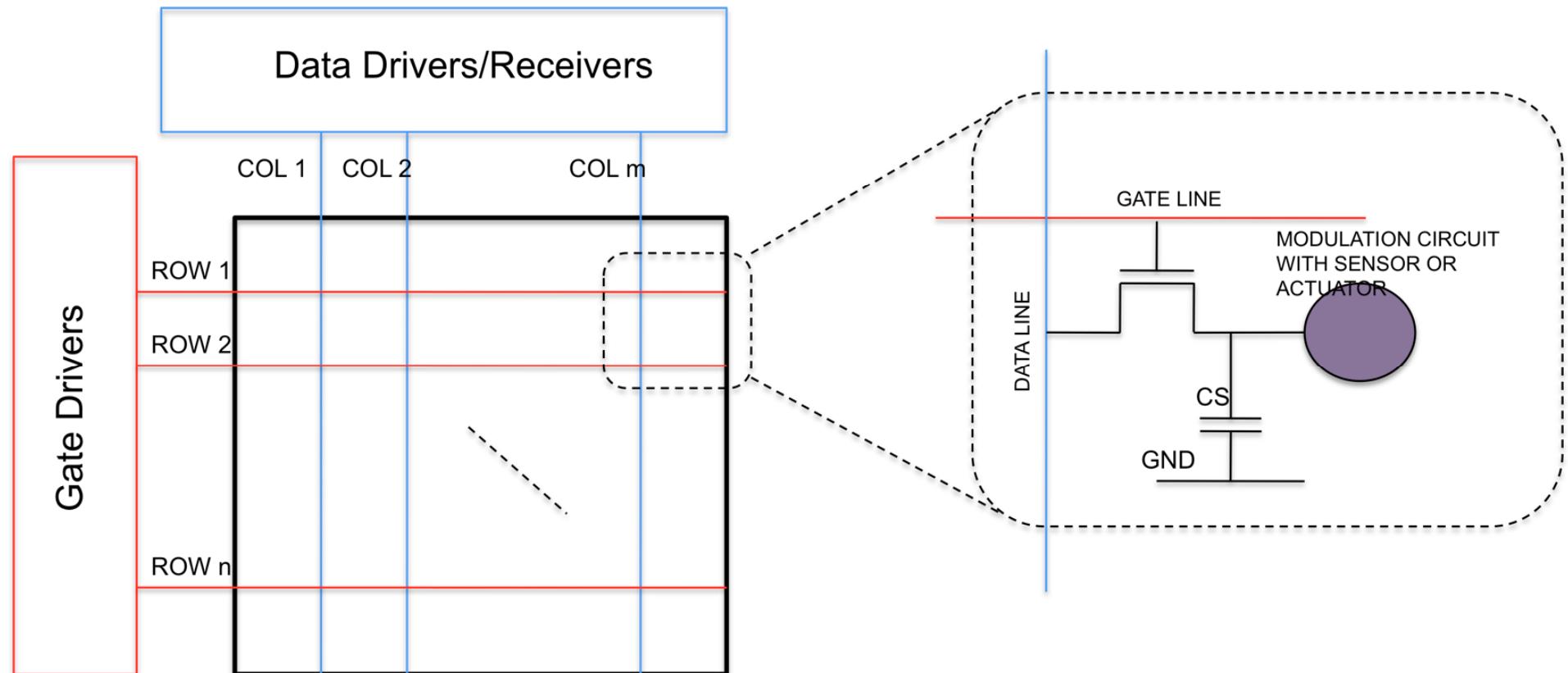
Material itself generates light. The light intensity is controlled by adjusting the current through the material or voltage across the material.

Eg. Light emitting diodes (LEDs)

## PIXEL CONTROL TRANSISTOR:

**Usually a TFT:** Need large area electronics.

# Active Matrix Display Architecture



# Light Modulators: Liquid Crystals

Liquid crystals: Phase of matter between liquid and crystal.

Rod shaped molecules  $\sim 25 \text{ \AA}$  length.

Nematic ('Threadlike') Phase: 1 D ordered

Smectic ('Soap like') Phase: 2 D ordered (slip planes)

Twisted Nematic: When the LC is placed along two 'aligning guide'/crystals it will direct itself along the guide. Can use this idea to obtain a twist using two polarizers aligned perpendicular to each other.

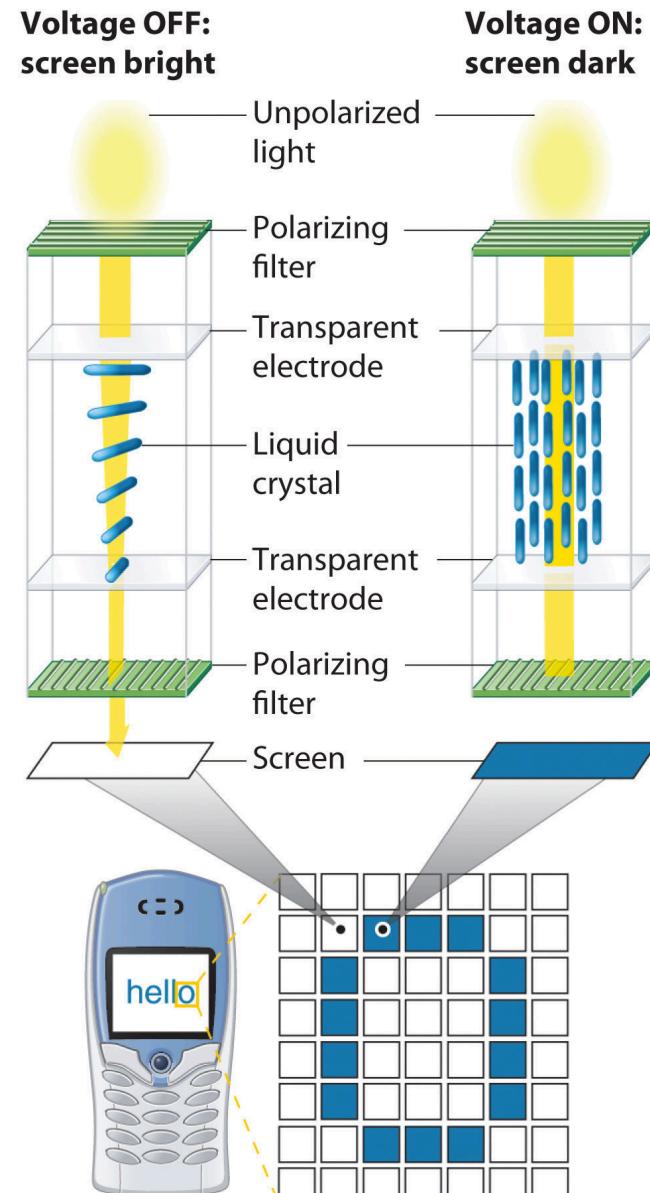
The orientation can now be controlled with applied electric fields (torque on the LC).

This idea can be used to modulate a back light.

No Applied Electric Field: The unpolarized backlight  $\rightarrow$  polarized to 0deg  $\rightarrow$  slowly twisted by the LC to polarized 90deg  $\rightarrow$  appears out of second polarizer

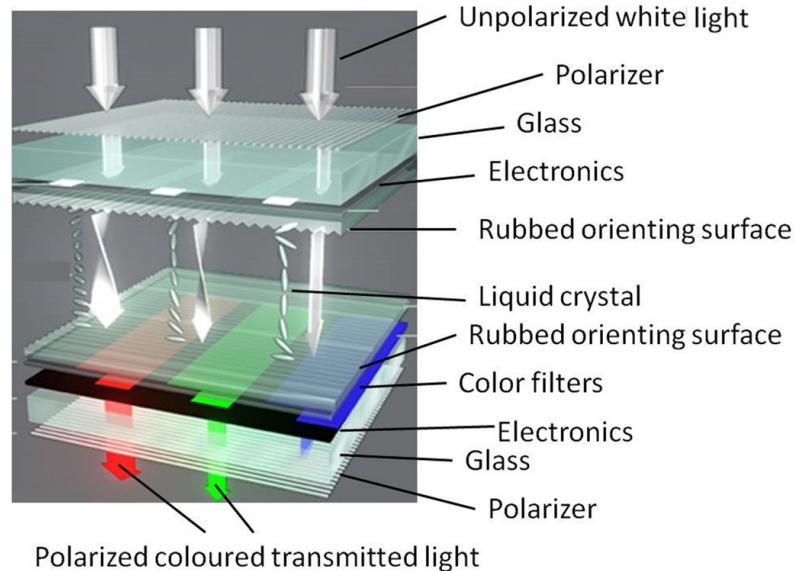
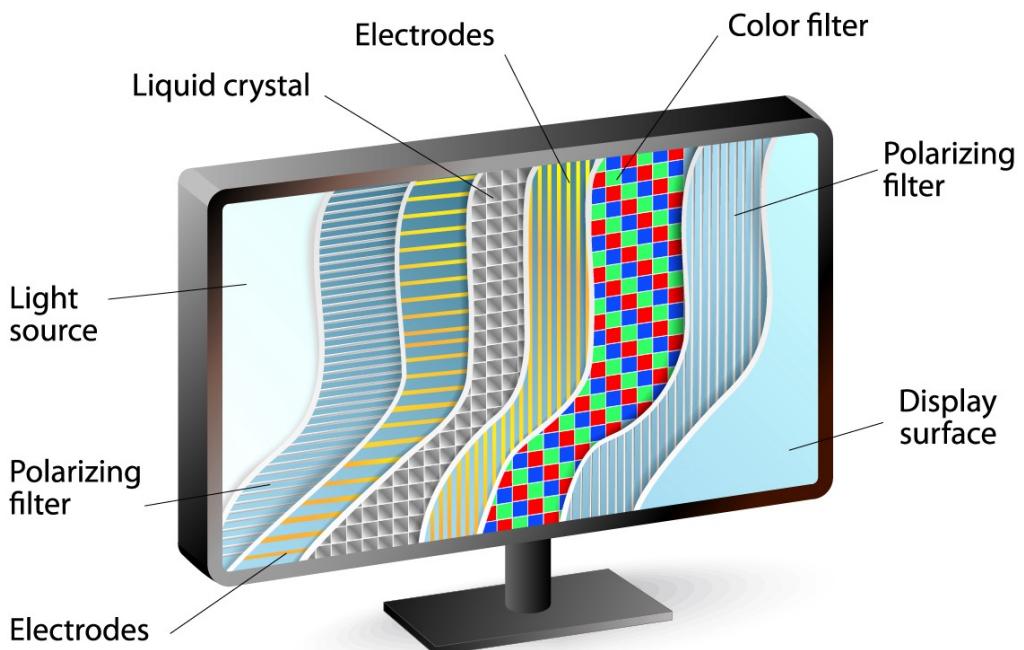
Electric field applied: aligns all the LC.

The unpolarized backlight  $\rightarrow$  polarized to 0deg  $\rightarrow$  not twisted by the LC and remains at 0deg  $\rightarrow$  does not appear out of second polarizer



[Link to Source of Picture](#)

# Anatomy of a display



<https://www.flexenable.com/blog/how-lcds-work/>

[http://www.merck.de/de/unternehmen/entdecke\\_merck/lcd\\_explorer.html](http://www.merck.de/de/unternehmen/entdecke_merck/lcd_explorer.html)

# Light Modulators: E-ink

E-ink uses reflected light – very much like printed paper in a book.

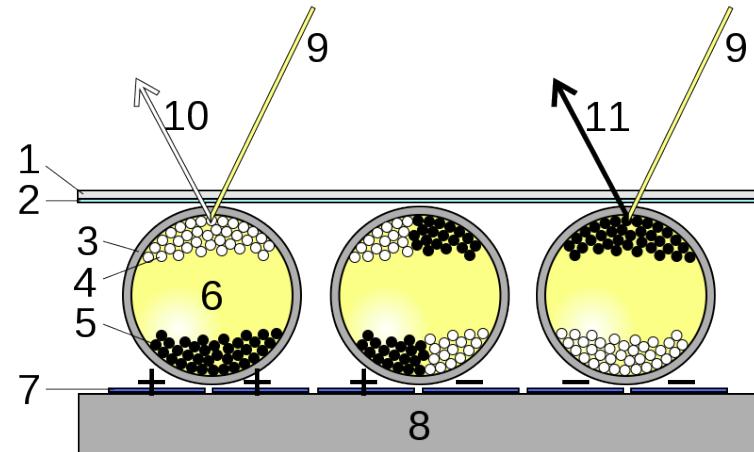
White pigments are positively charged  
Black pigments are negatively charged

They are enclosed in transparent microcapsules

The micro capsules are sandwiched between transparent conductive electrodes.

Depending on the field, we have the black/white particles on top. This implies poor/good reflection of ambient light.

The field is applied by applying a suitable voltage.



- 1 Upper layer
- 2 Transparent electrode layer
- 3 Transparent micro-capsules
- 4 Positively charged white pigments
- 5 Negatively charged black pigments
- 6 Transparent oil
- 7 Electrode pixel layer
- 8 Bottom supporting layer
- 9 Ambient Light
- 10 Reflected (White)
- 11 Not Reflected (Black)

Source: Wikipedia

# Light Modulators: Light Emitting Diodes

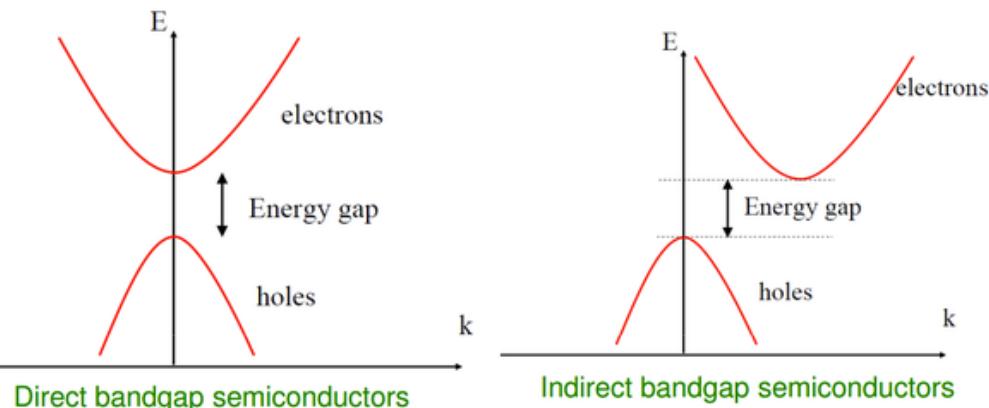
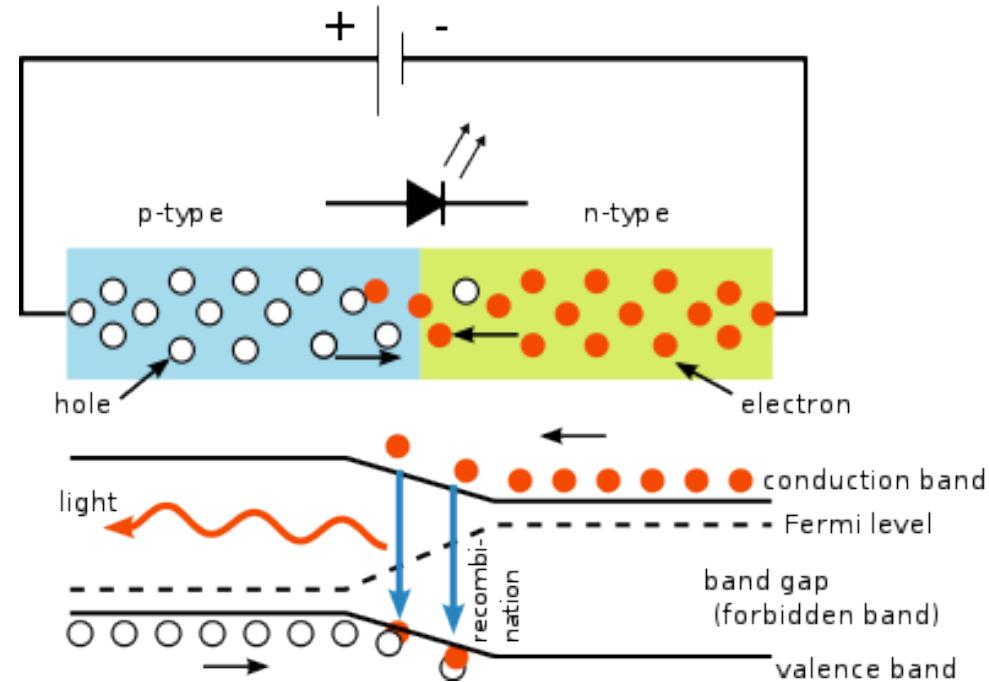
Uses p-n junction diodes. When the diode is ‘forward biased’ i.e. p-side is at a higher voltage compared to the n-side, the built in potential barrier is lowered and majority carriers ‘diffuse’ across the junction.  
The current voltage relation is:

$$I = I_0(e^{qV_a/kT} - 1)$$

NOTE: We have studied drift current.  
Another mechanism of charge transport is diffusion – this current is due to a concentration gradient.

The diffusion of electrons from n to p side and holes from p to n side leads to an increase in recombination of electrons and holes producing light. The light intensity therefore depends on the current.

GaAs - 850nm-940nm, GaAsP – 630nm – 650nm, SiC – 430nm-505nm, GaInN – 450 nm. Direct Band gap materials preferred



Source of Pictures: Wikipedia

# Pixel Circuit

## Voltage Programmed Pixel Circuit

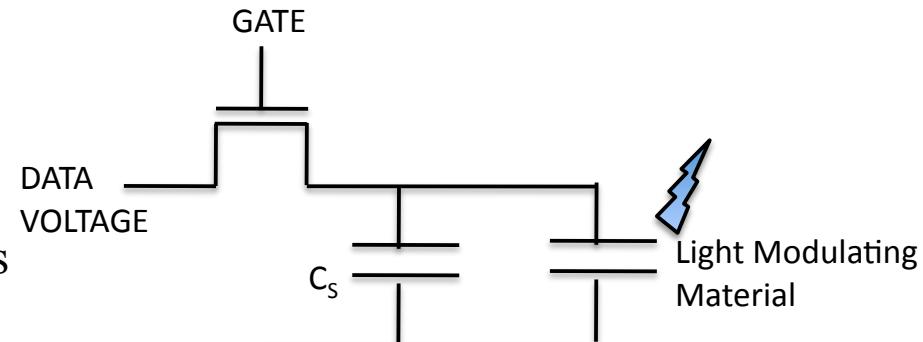
Typically used for LCD or E-ink.

TFT is used as a switch.

The “Data Voltage” is submitted to the drain. It is the voltage needed to apply the correct electric field to modulate the light modulating material.

The resistance of the switch is decided by the Gate voltage.

The TFT switch must therefore be biased in Linear operation (where the TFT behaves like a resistor)



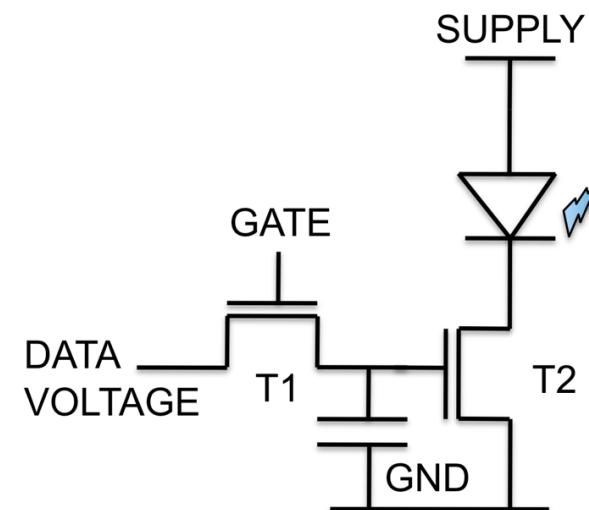
## Current Programmed Pixel Circuit

Typically used for LED Displays.

2 TFTs needed. One is used as a switch (T1). The second is used as a current source (T2).

The “Data Voltage” is submitted to the drain of T1. It is the gate voltage needed for T2 to drive the appropriate current.

T1 will operate in Linear bias. T2 will operate in Saturation mode current source with the current depending only on gate voltage).



# Pixel Circuit

## Resistor-Capacitor Circuit

Consider the circuit of the TFT-capacitor with the data voltage being written onto the capacitor. This is like an RC circuit with the TFT behaving like a resistor and operating in linear mode. What is the time constant?

The small signal resistance of the TFT when  $V_{ds}$  (the data voltage)  $\ll V_{gs} - V_T$  is:

$$\frac{dV_{ds}}{dI_{ds}} \approx \frac{1}{\mu C_{ox}(W/L)(V_{gs} - V_T)} = R_{TFT}$$

$$\text{Time Constant} = R_{TFT}C_S$$

## TFT as a current source in current programmed pixel circuits

When the TFT is used as a current source in current programmed circuits (eg. TFT T2 driving the LED), the TFT is biased in saturation operation. The gate voltage  $V_{gs}$  of the TFT is then equal to the data voltage (which is now stored on the storage capacitor). The current is therefore (see the derivation of the current voltage characteristics of the TFT):

$$I_{ds} = \frac{\mu C_{ox}(W/L)}{2} (V_{gs} - V_T)^2$$