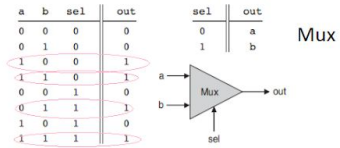
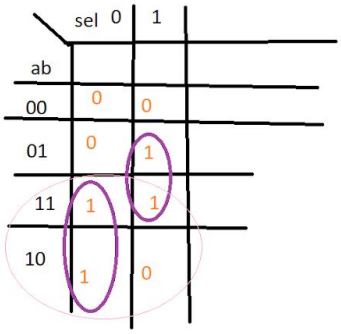
Mux



a	b	sel	out
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	1

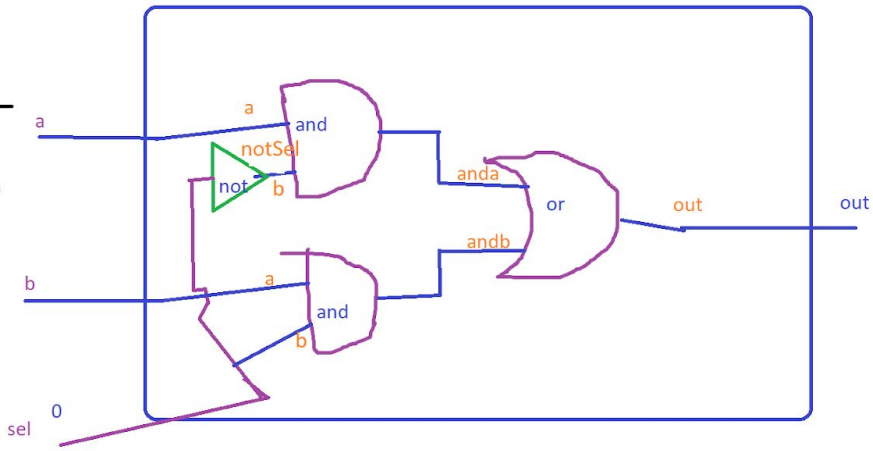
sel	out
0	a
1	b

Mux



(a notSel) (sel b) 4 chips

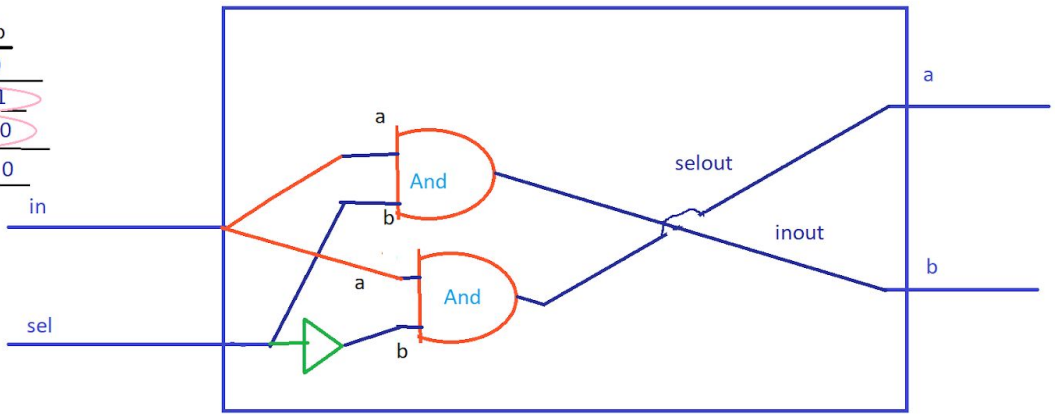
Nand(a = , b = , out =);
Nand(a = b, b = sel, out = andb);



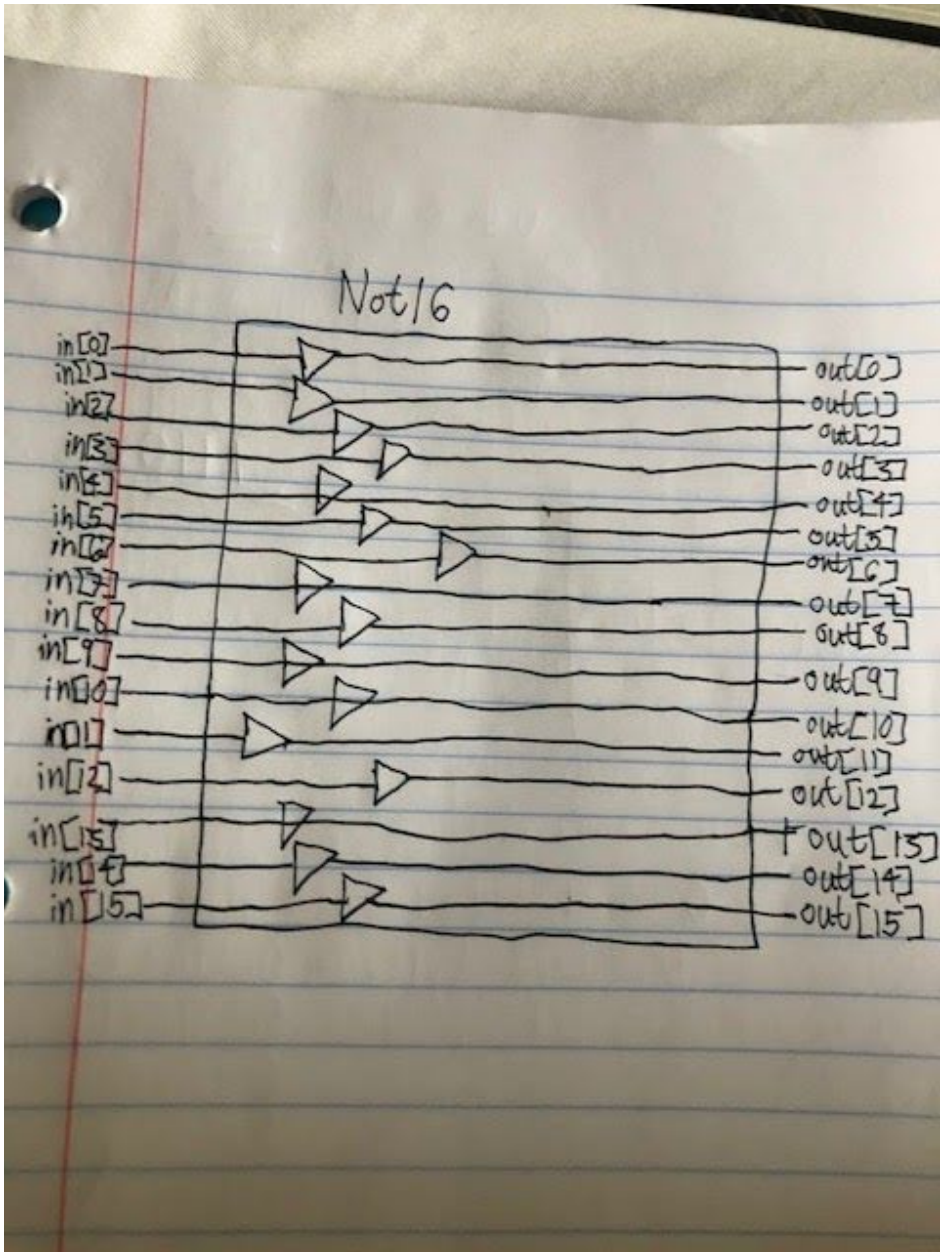
DMux

DMux

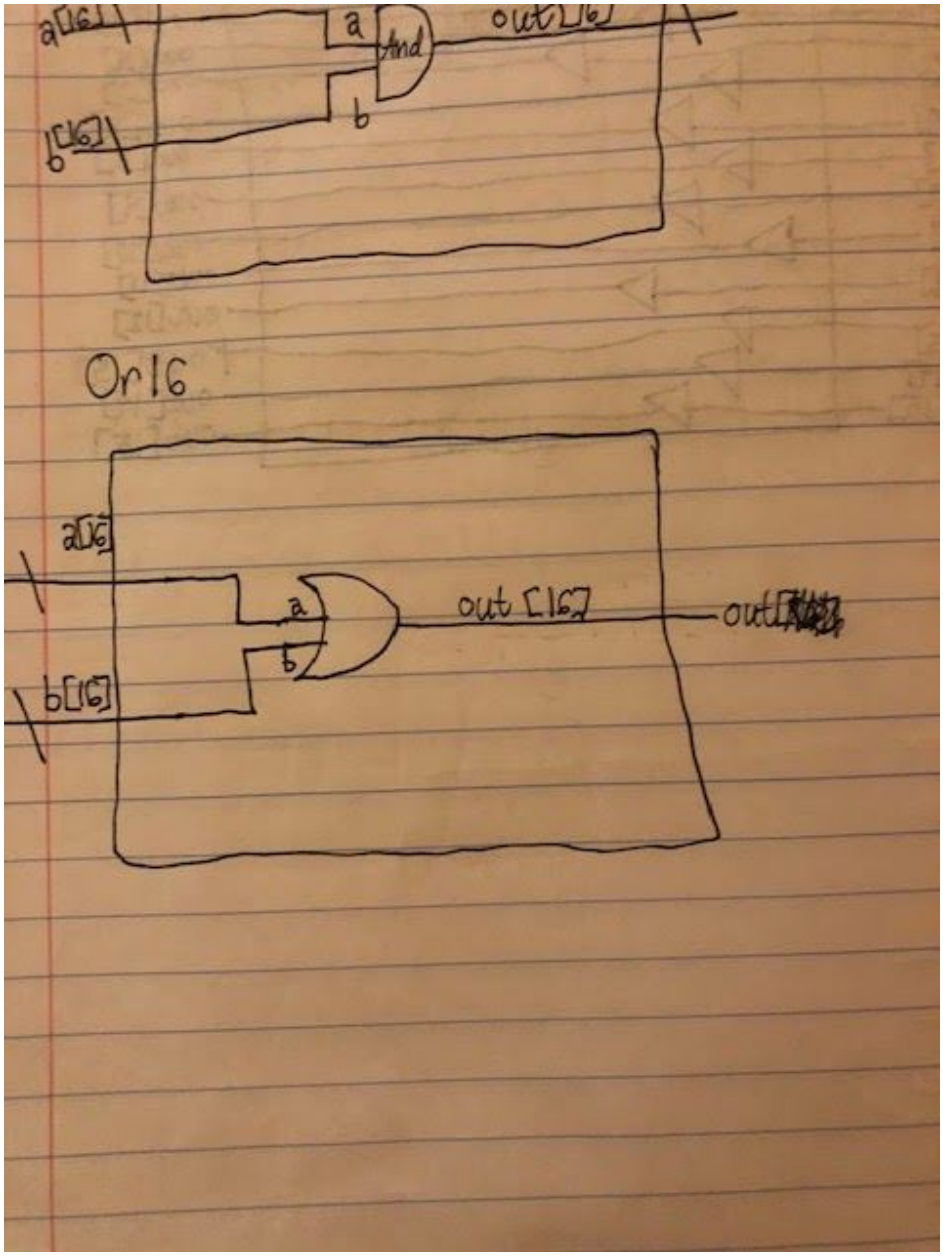
in	sel	a	b
0	0	0	0
1	1	0	1
1	0	1	0
0	1	0	0



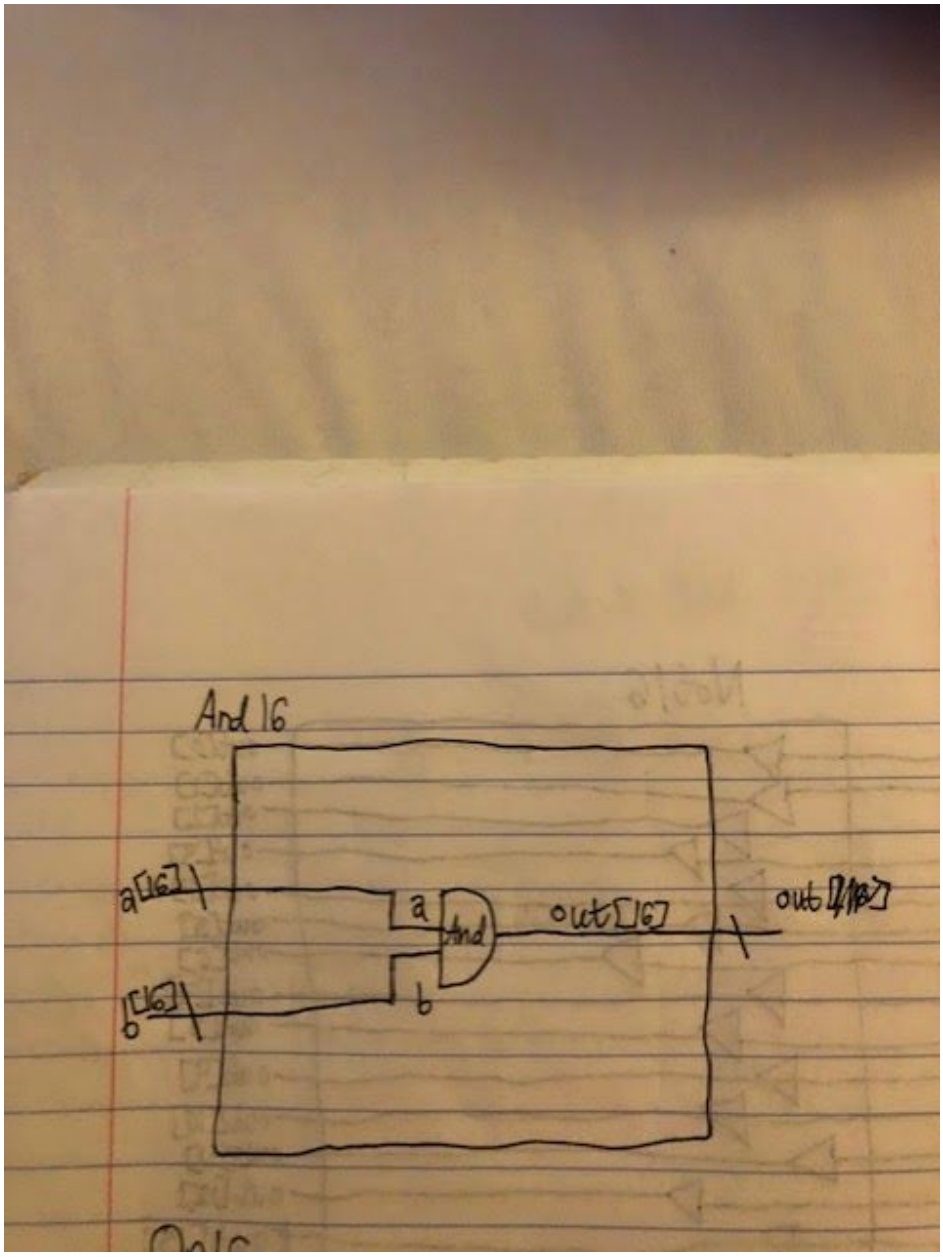
Not16


Not16
in[0]
in[1]
in[2]
in[3]
in[4]
in[5]
in[6]
in[7]
in[8]
in[9]
in[10]
in[11]
in[12]
in[13]
in[14]
in[15]
out[0]
out[1]
out[2]
out[3]
out[4]
out[5]
out[6]
out[7]
out[8]
out[9]
out[10]
out[11]
out[12]
out[13]
out[14]
out[15]

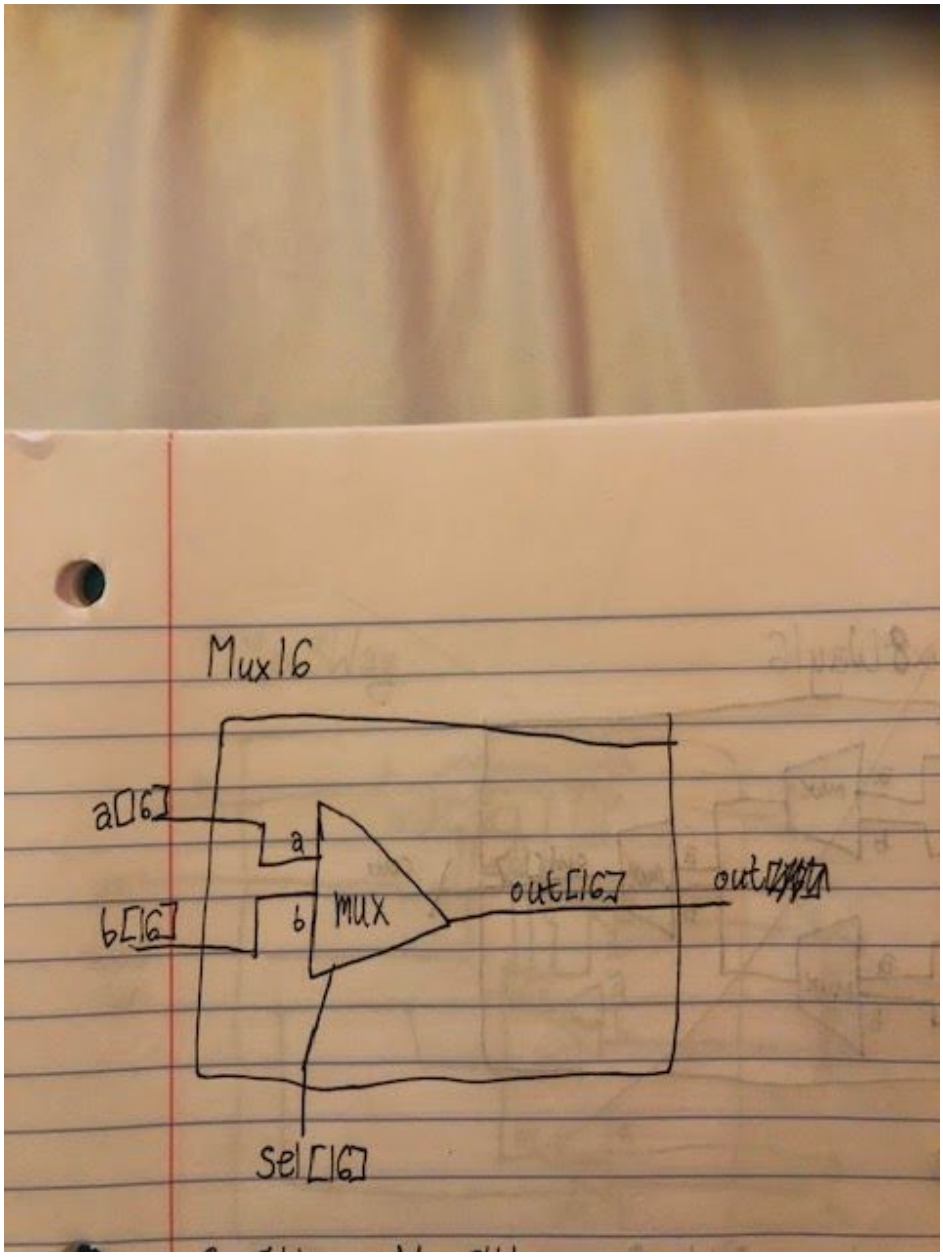
Or16



And16

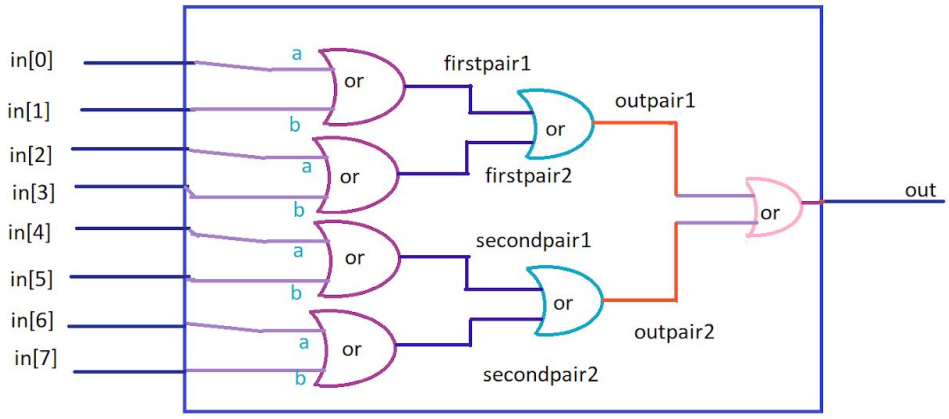


Mux16



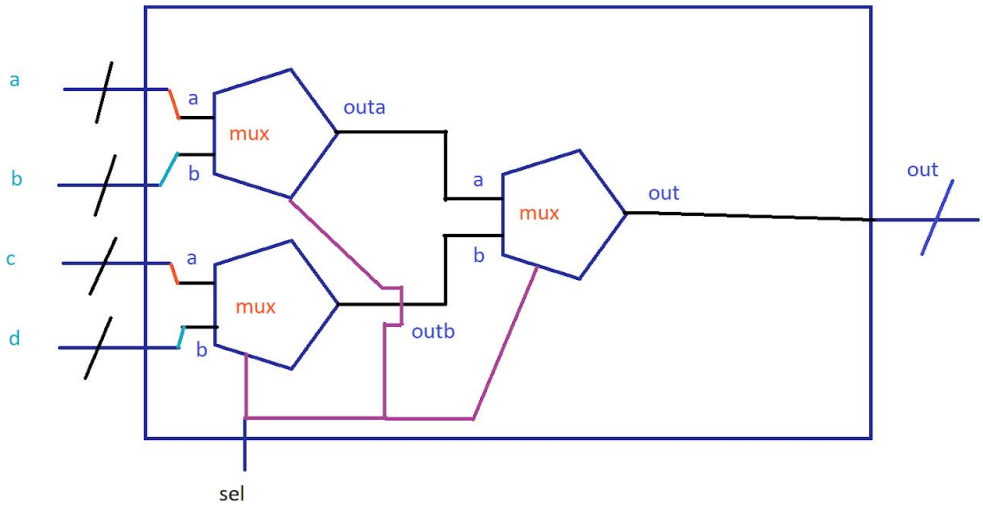
Or8Way

Or8Way

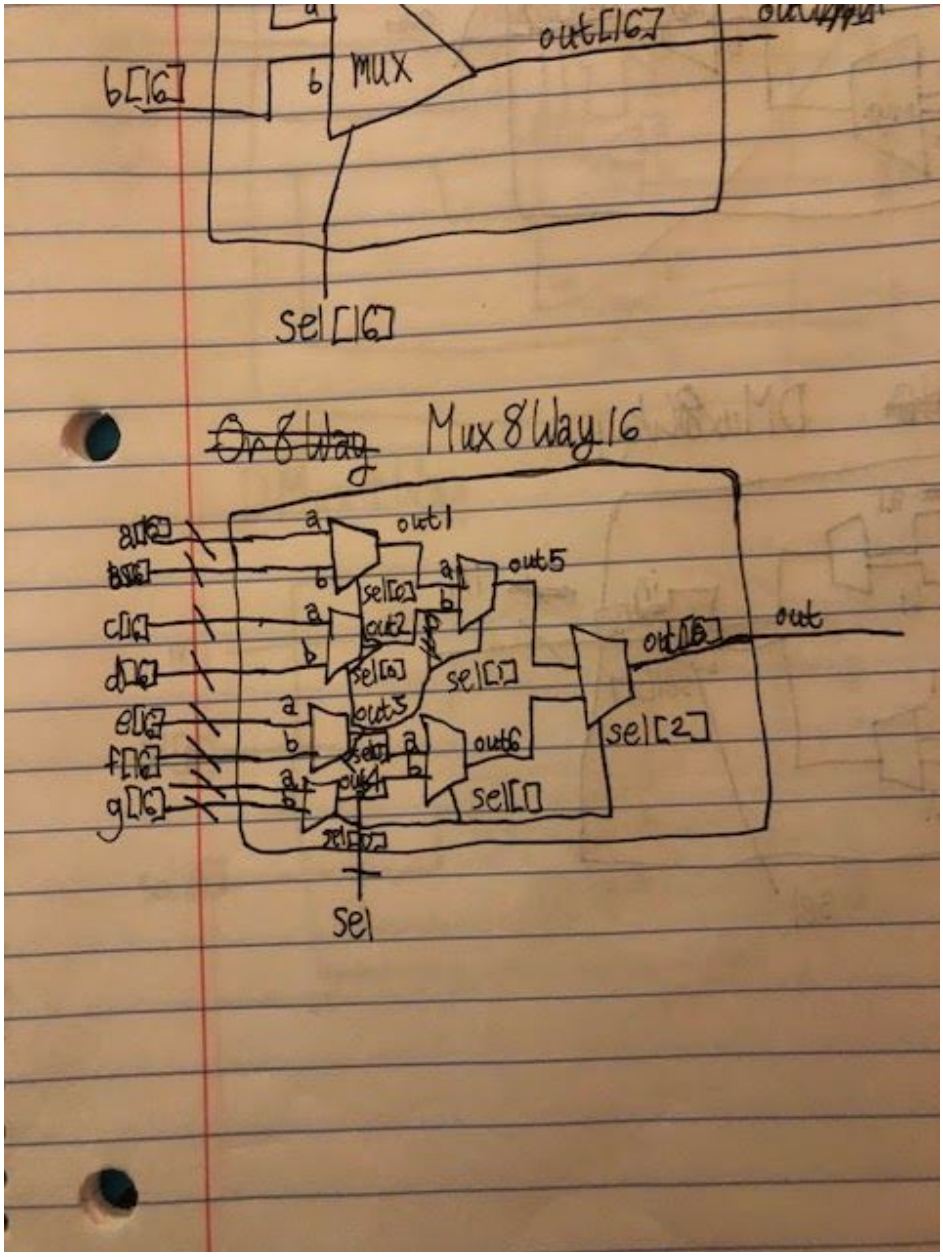


Mux4Way16

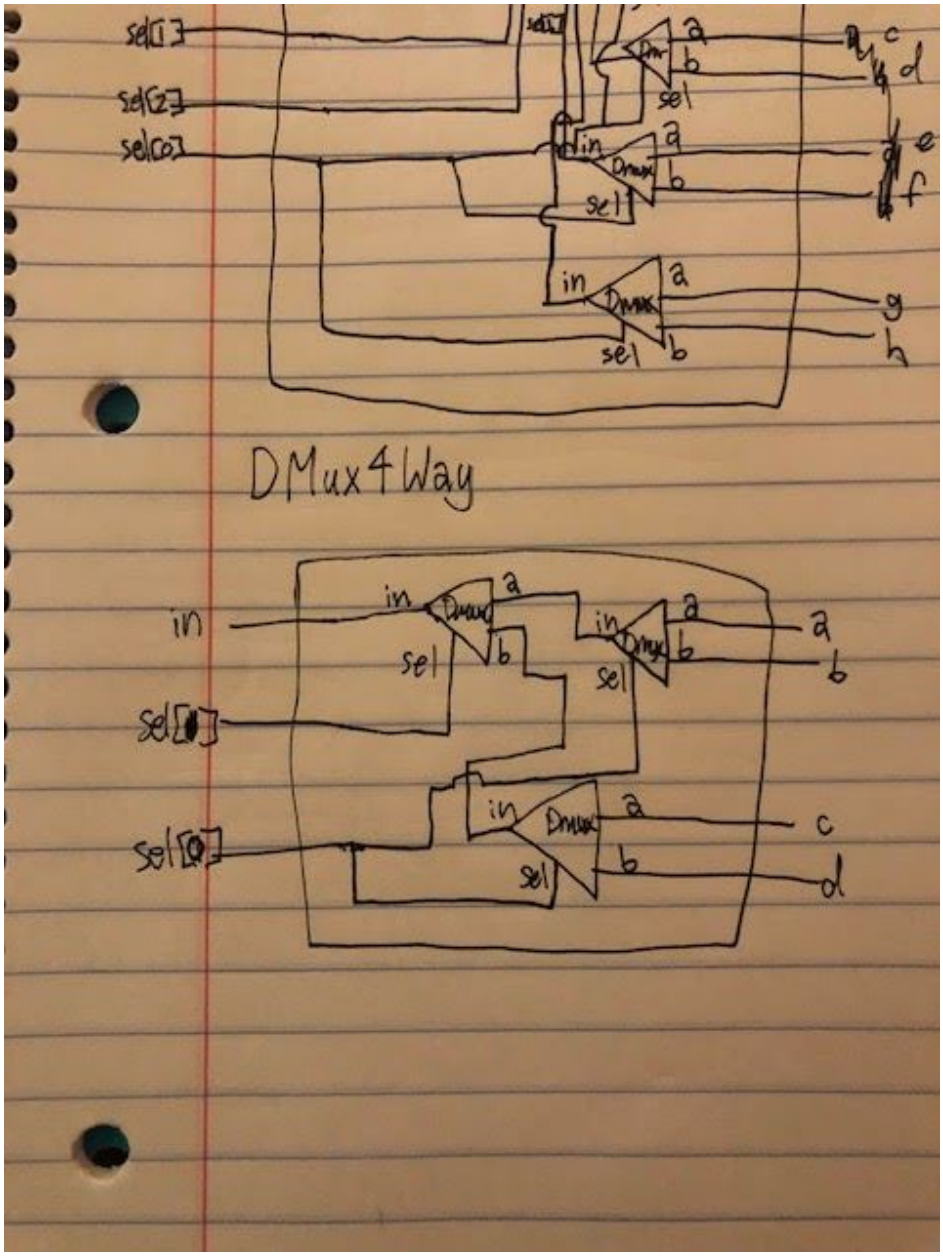
Mux4Way16



Mux8Way16


b[16]
MUX
out[16]
sel[16]
~~Or8Way~~ Mux8Way16
a[16]
b[16]
c[16]
d[16]
e[16]
f[16]
g[16]
out1
out5
out2
out3
out6
out4
out
sel[0]
sel[1]
sel[2]
sel[]
sel

DMux4Way



DMux8Way