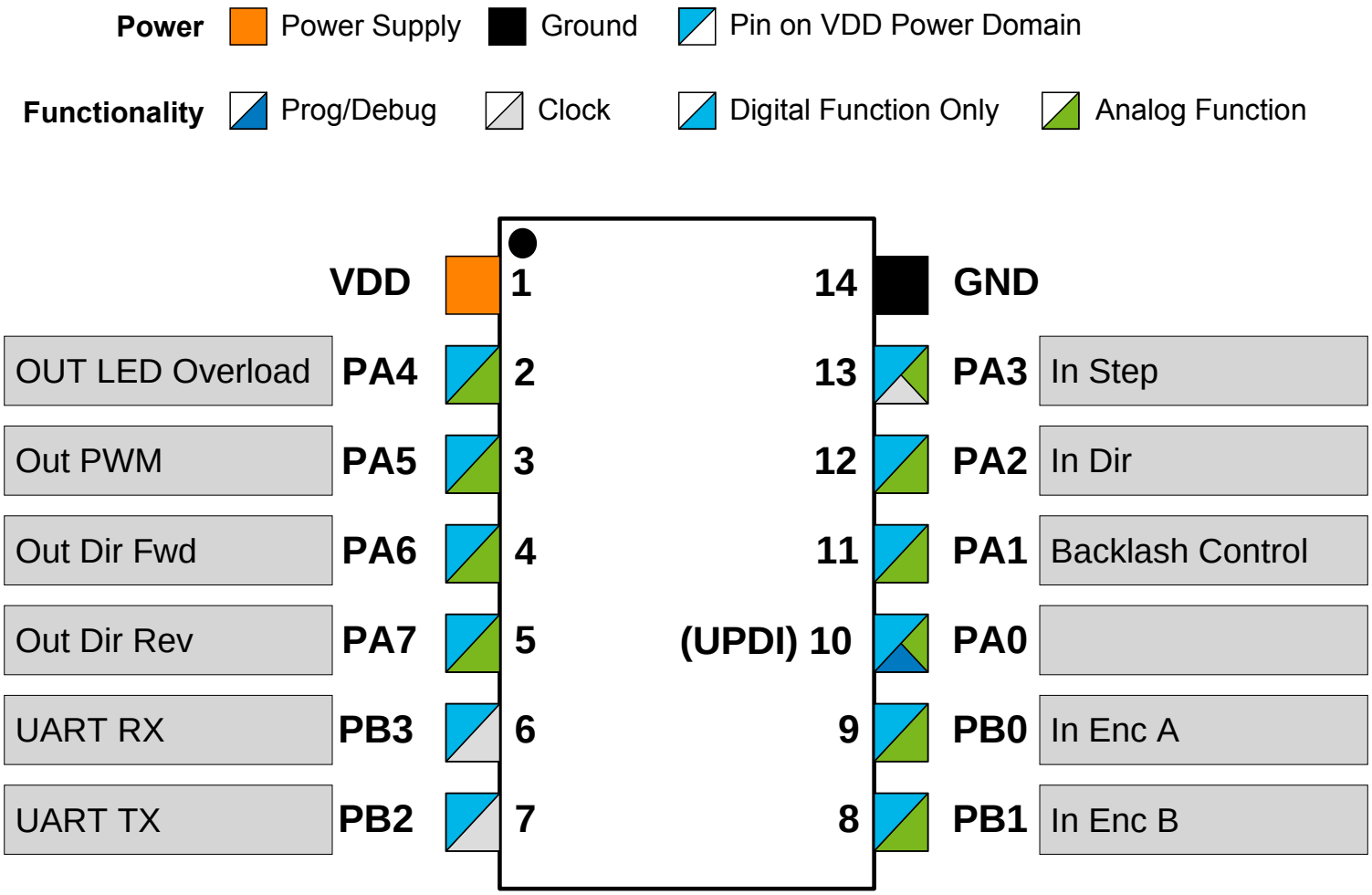

Table 5-1. PORT Function Multiplexing

VQFN 24-Pin	VQFN 20-Pin	SOIC 20-Pin	SOIC 14-Pin	Pin Name (1,2)	Other/Special	ADC0	PTC(4)	AC0	DAC0	USART0	SPI0	TWI0	TCA0	TCB0	TCD0	CCL
23	19	16	10	PA0	$\overline{\text{RESET}}$/ UPDI	AIN0										LUT0-IN0
24	20	17	11	PA1		AIN1				TxD(3)	MOSI	SDA(3)				LUT0-IN1
1	1	18	12	PA2	EVOUT0	AIN2				RxD(3)	MISO	SCL(3)				LUT0-IN2
2	2	19	13	PA3	EXTCLK	AIN3				XCK(3)	SCK		WO3			
3	3	20	14	GND												
4	4	1	1	VDD												
5	5	2	2	PA4		AIN4	X0/Y0			XDIR(3)	$\overline{\text{SS}}$		WO4		WOA	LUT0-OUT
6	6	3	3	PA5		AIN5	X1/Y1	OUT					WO5	WO	WOB	
7	7	4	4	PA6		AIN6	X2/Y2	AINN0	OUT							
8	8	5	5	PA7		AIN7	X3/Y3	AINP0								LUT1-OUT
9				PB7												
10				PB6												
11	9	6		PB5	CLKOUT	AIN8		AINP1					WO2(3)			
12	10	7		PB4		AIN9		AINN1					WO1(3)			LUT0-OUT(3)
13	11	8	6	PB3	TOSC1					RxD			WO0(3)			
14	12	9	7	PB2	TOSC2, EVOUT1					TxD			WO2			
15	13	10	8	PB1		AIN10	X4/Y4			XCK		SDA	WO1			
16	14	11	9	PB0		AIN11	X5/Y5			XDIR		SCL	WO0			
17	15	12		PC0							SCK(3)			WO(3)	WOC	
18	16	13		PC1							MISO(3)				WOD	LUT1-OUT(3)
19	17	14		PC2	EVOUT2						MOSI(3)					
20	18	15		PC3							$\overline{\text{SS}}$(3)		WO3(3)			LUT1-IN0
21				PC4									WO4(3)			LUT1-IN1
22				PC5									WO5(3)			LUT1-IN2

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