Wednesday	EE 671: VLSI Design	Due on
Oct.31, 2018	Assignment 4	Nov. 09, 2018

Assume the following delay values for half and full adders:
Half adder: carry (AND gate) = 40 ps, sum (XOR) = 70 ps.
Full adder: carry (AB + BC + CA) = 80 ps, sum (A XOR B XOR C) = 120 ps.

Describe and simulate a Dadda 8x8 Multiply and Accumulate circuit in verilog, (Icarus verilog – a public domain verilog simulator will be used for this assignment).

Half adders and full adders can be used as behaviourally described building blocks with delays as specified above. The accumulator should be 16 bits wide. Use a carry select adder for the final addition, assuming the carry select mux delay to be 50 ps. A flag output indicating overflow in the accumulator register should be provided.

Notice that the sum and carry delays are not equal. Make design choices for allocation of wires to specific adders and sizes of sub adders in the final carry select adder to reduce the overall worst case delay.

Simulate the design with 16 random test vectors for multiplicand, multiplier and initial content of the accumulator register. Also simulate for multiplication of FF by FF with the initial value of the accumulator being 0F0F