**Report**

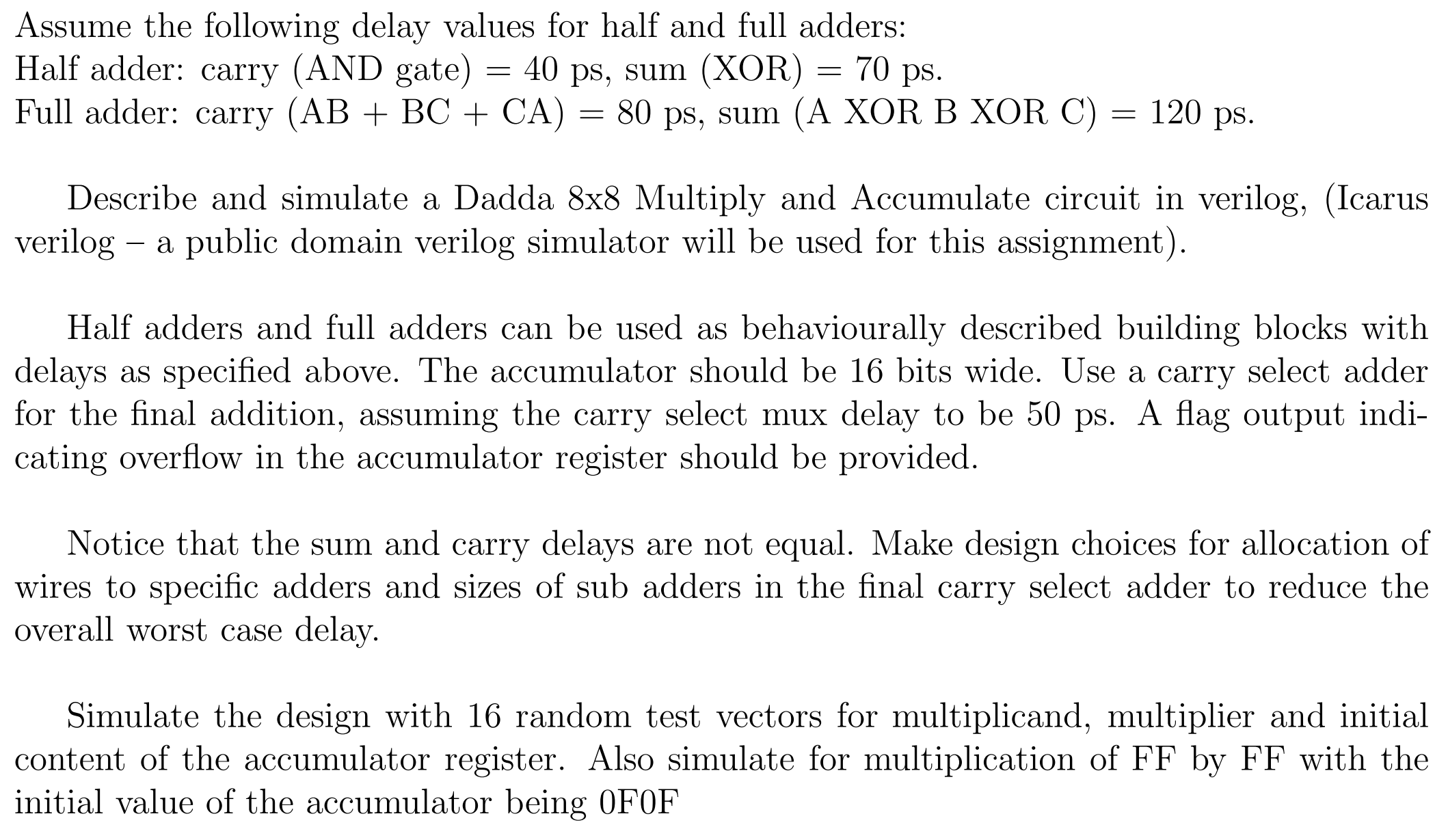
**On**

**Design and Timing analysis of**

**Dadda Multiplier**

**Date: Dec’18**

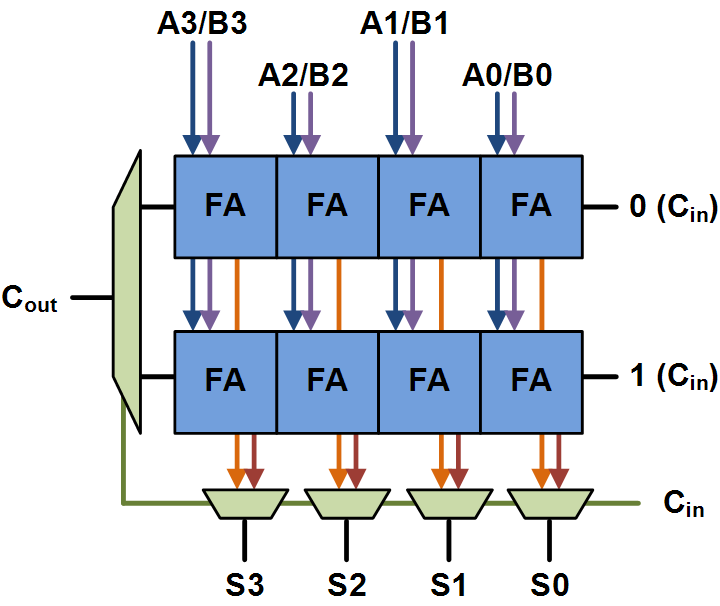
Problem statement



Dadda Multiplier

Dadda multipler is a hardware multiplier design which reduces number of partial products by stages of half adders and full adders until we are left with at most two bits of each weight. Final result is added with conventional adder.

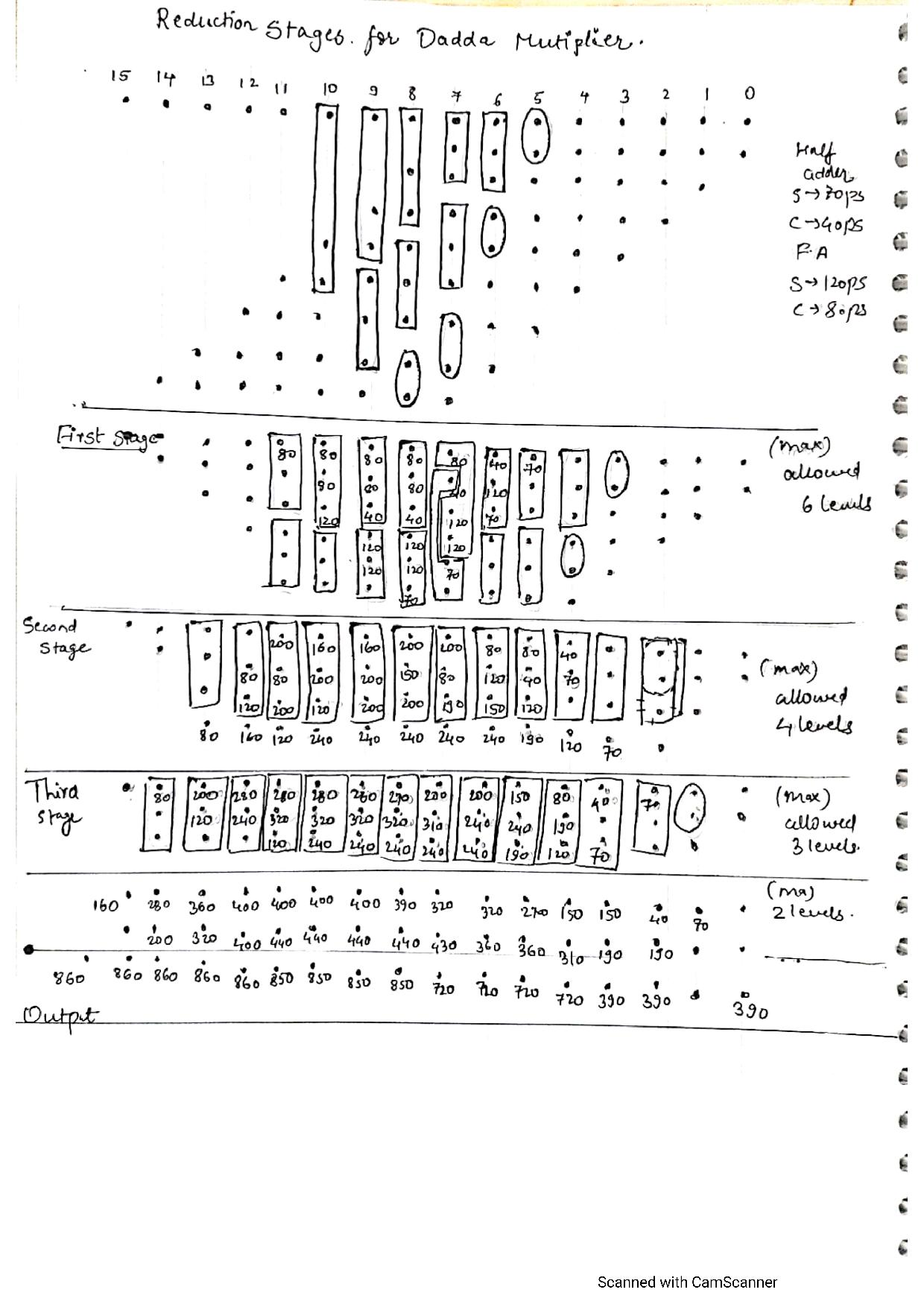
In our problem statement we are using carry select adder as the final adder. The block diagram of carry select adder is as shown below.



Carry Select adder

The following diagrams shows the reduction stages for Dadda multiplier.

The delays for sum and carry for half adder and full adder is given in problem statement.



Reduction diagram

The code for Dadda multiplier is written in verilog and simulated in Modelsim.

The simulated outputs for 16 random test vectors is shown and also the output for FF\*FF with accumulator contents 0F0F is also shown.



Output waveform