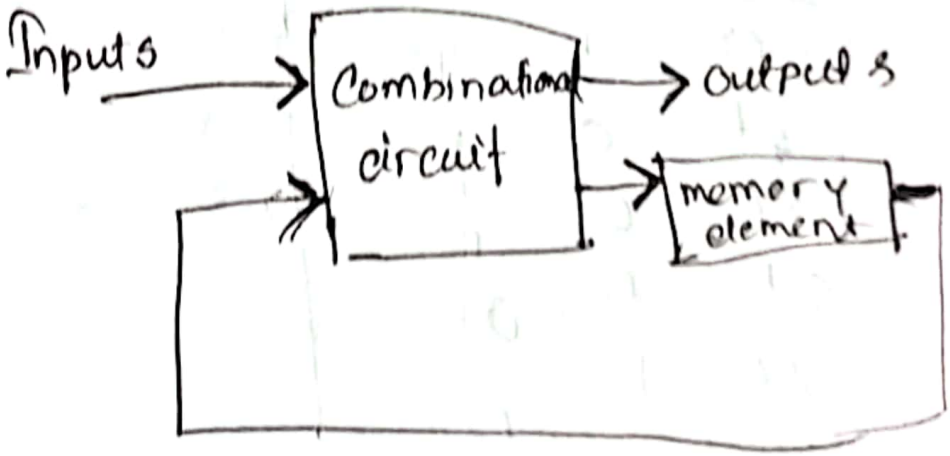
Chapter 06
Sequential logic

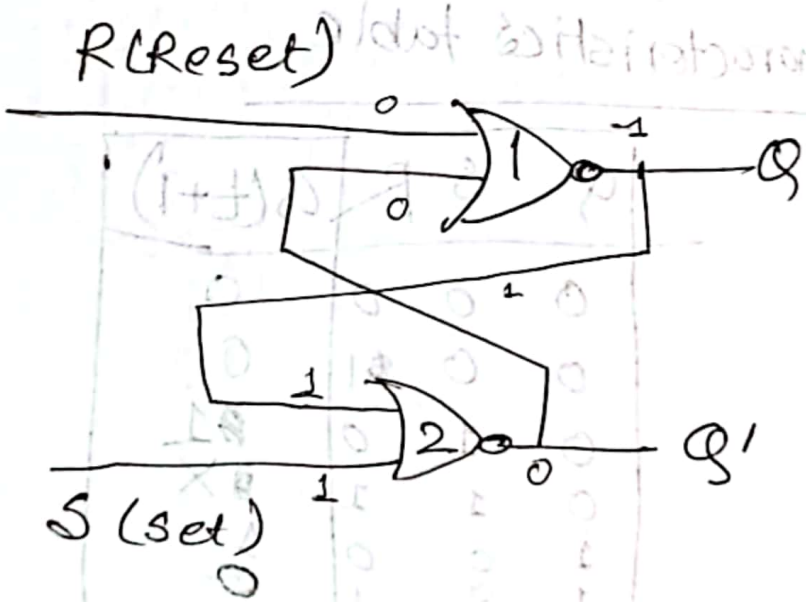
Sequential circuit: A sequential circuit consists of a combinational circuit with memory elements to form a feedback path. This memory elements are capable of storing binary information. The stored binary information defines the state of sequential circuit. Sequential circuit receives information from external input along with the present state of memory elements it determines the output.



Flip-flop (FF):

A flip-flop circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states.

Basic FF circuit : A FF circuit can be constructed from two NAND or two NOR gate.



Indeterminate state →
S=1
R=1

S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

Indeterminate state →

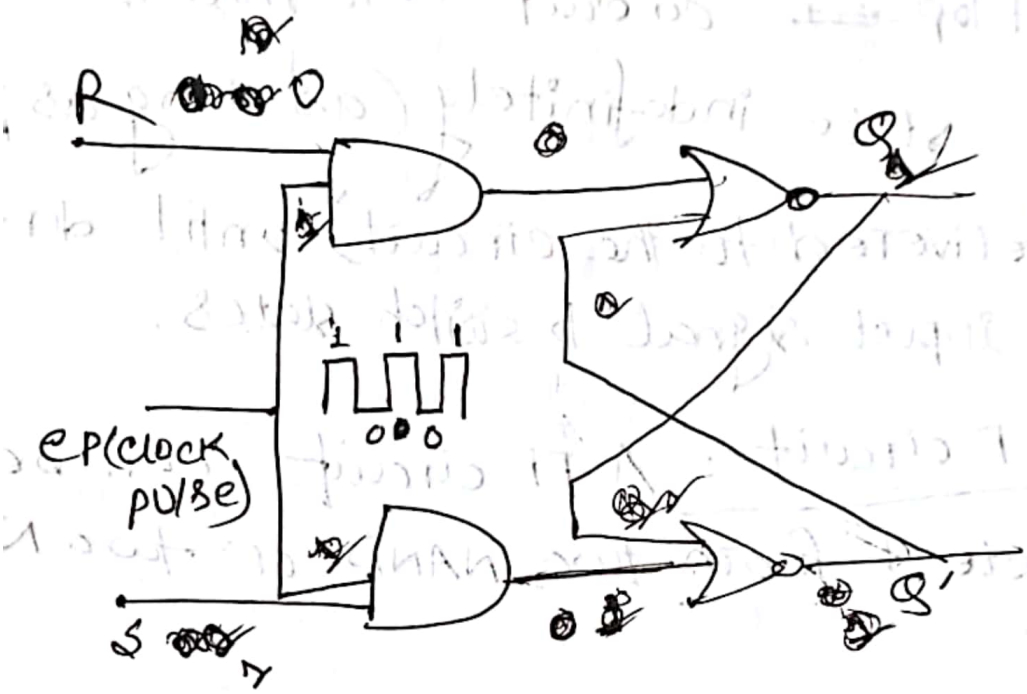
(after S=1, R=0)

(after S=0, R=1)

NOR

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

Clocked RS flip flop

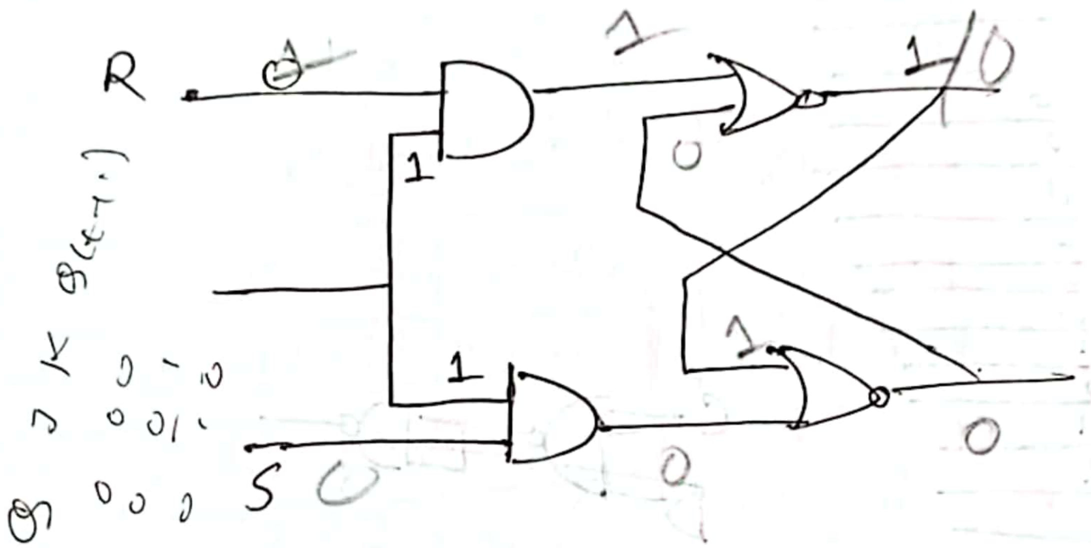


Characteristics table

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

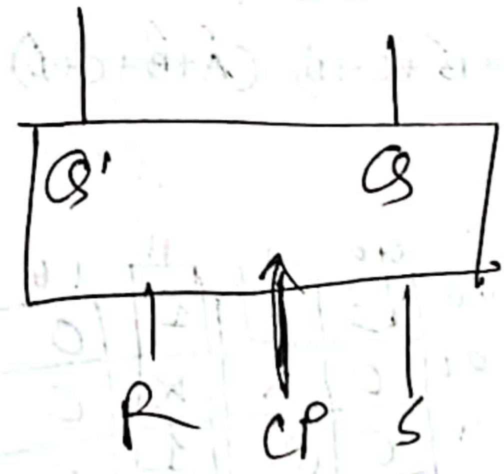
S=R=1 = Indeterminant

Indeterminant state



Q \ SR	00	01	11	10
0	0	0	X	1
1	1	0	X	1

$Q(t+1) = S + QR'$



(1) Q When both inputs are 0 (R=0, S=0), then $Q(t+1) = Q$.

(2) R=0, S=1, then $Q(t+1) = 1$.

(3) R=1, S=0, then $Q(t+1) = 0$,

state

JK flipflop

1. JK flipflop is the refinement of RS flipflop because the indeterminate state is removed

2. For J=1, K=1 the flip flop switches to its Complement state.

   if Q=1, it becomes 0 or

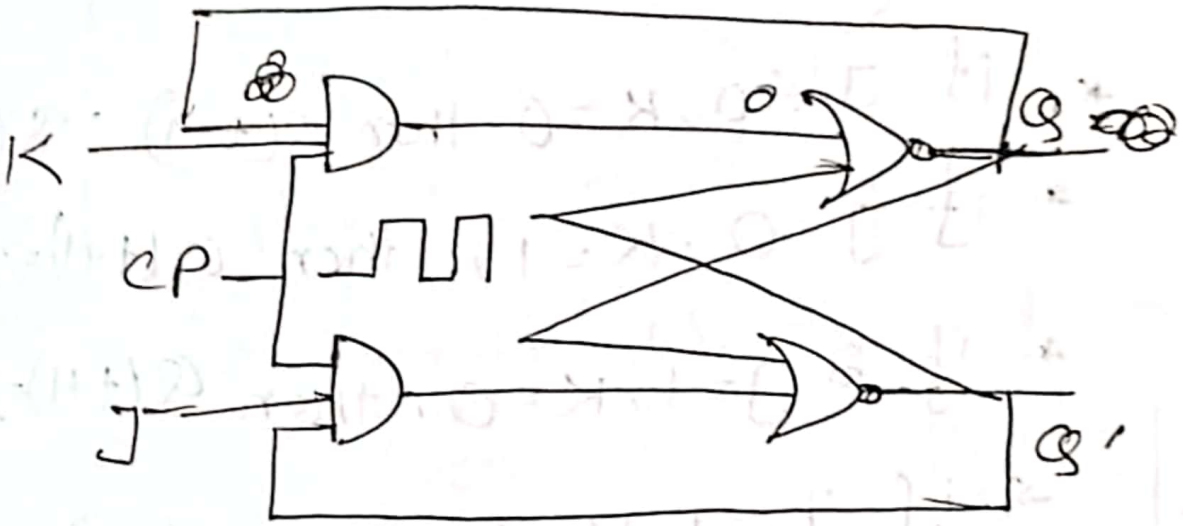
   if Q=0, it becomes 1.

3. ~~Two level J;~~

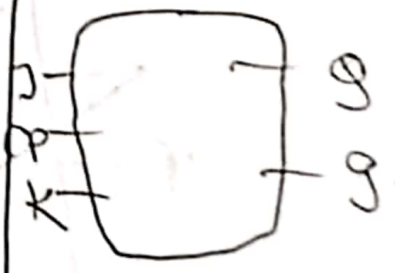
3. The letter J is for set and K is for clear.

4. The output Q is ANDed with K and CP input so that the flipflop is cleared during a clock pulse only if Q is previously 1.

⑤ Similarly for Q' is ANDed with J.



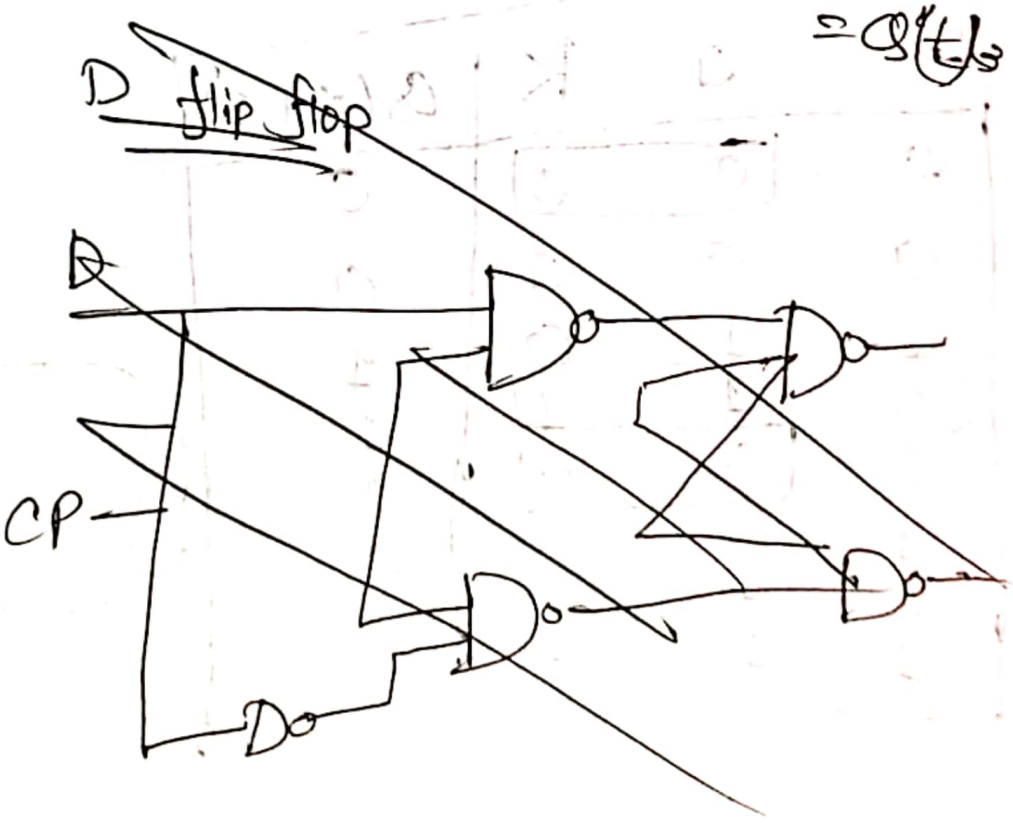
Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



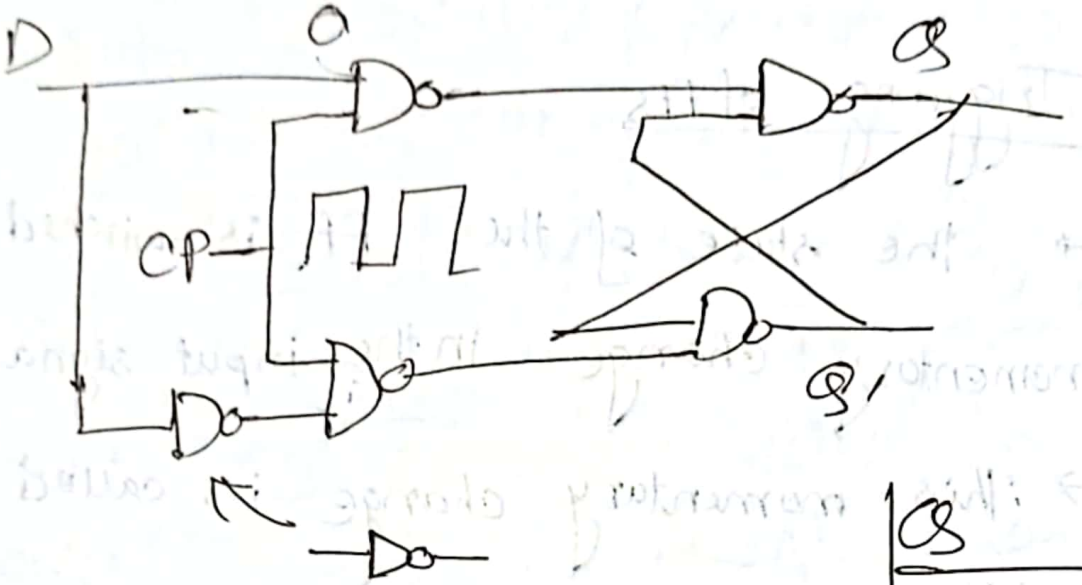
Q \ JK	00	01	11	10
0	0	0	1	1
1	1	0	0	1

* if J=0, K=0 then Q(t+1) = Q(t)
* if J=0, K=1, then Q(t+1)=0
* if J=1, K=0; then Q(t+1)=1
* if J=1, K=1, then Q(t+1) = Q'(t)

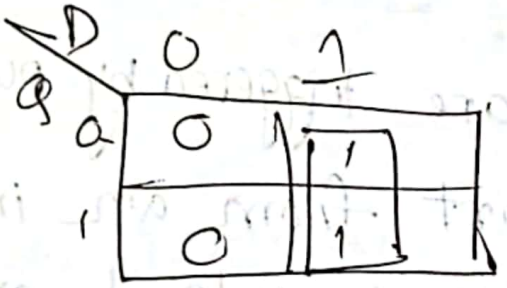
D flip flop



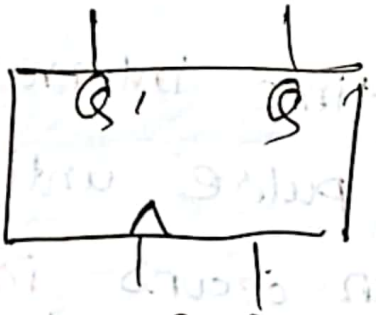
D flip flop



Q	D	D'
0	0	0
0	1	1
1	0	0
1	1	1



$Q(t+1) = D$



T flip-flop

Triggering of FFs

→ the state of the FF is switched by a momentary change in the input signal.

→ This momentary change is called trigger.

→ Clocked FFs are triggered by pulse.

→ pulse ~~that~~ start from an initial value of 0, goes momentary to 1 and after a short time it returns to its initial value 0

→ The time interval from the application of the pulse until the ~~code~~ output transition occurs is a a critical factor that needs further investigation.

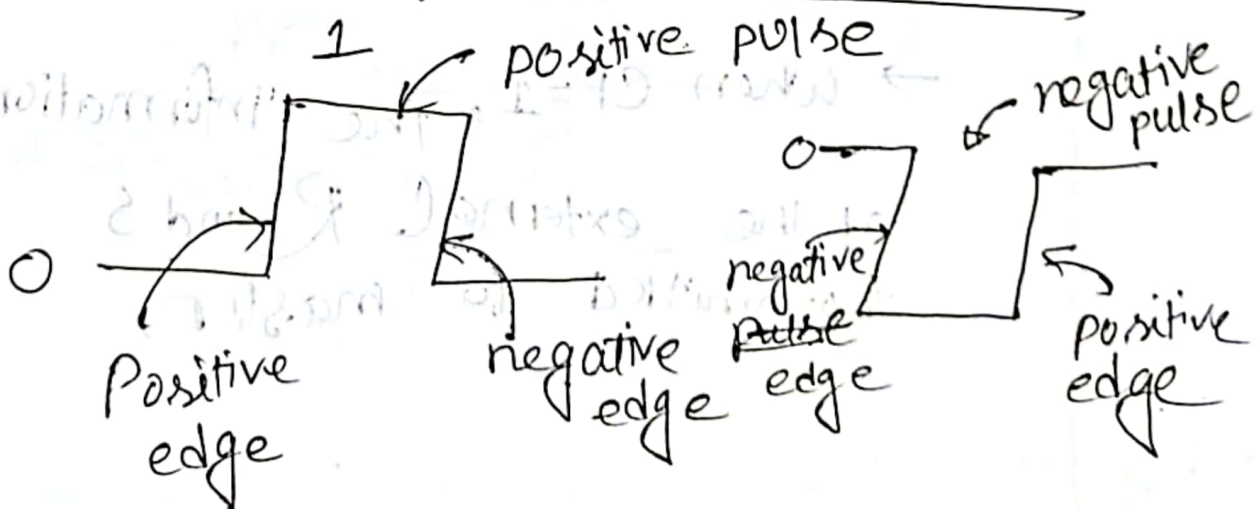
→ Timing problem can be prevented if outputs of the FFs do not start changing until the pulse input has returned to 0.

→ To ensure such an operation a FF must have propagation delay from input to output in access of the pulse duration.

→ Very critical to maintain propagation delay.

→ Pulse transition can be used rather than pulse duration.

Positive and negative edge transition

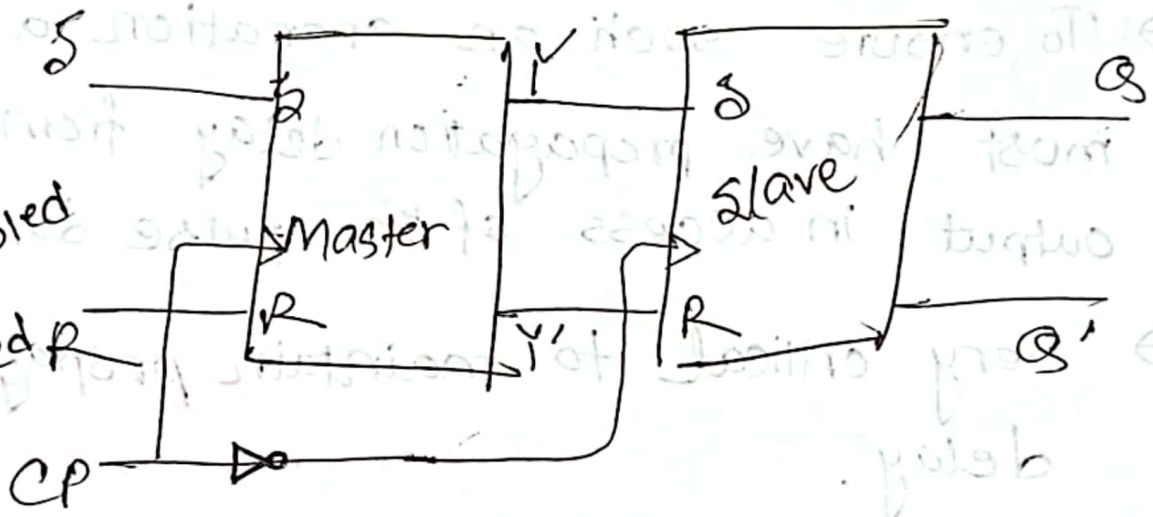


* Negative edge trigger
Positive edge trigger } Questions
Pulse duration

Master-Slave FF

CP=1 → Master enabled, slave disabled

CP=0, Master disabled, slave enabled



→ CP = 0, inverter = 1; output of the slave is 1 so, output Q = Y, Q' = Y'.

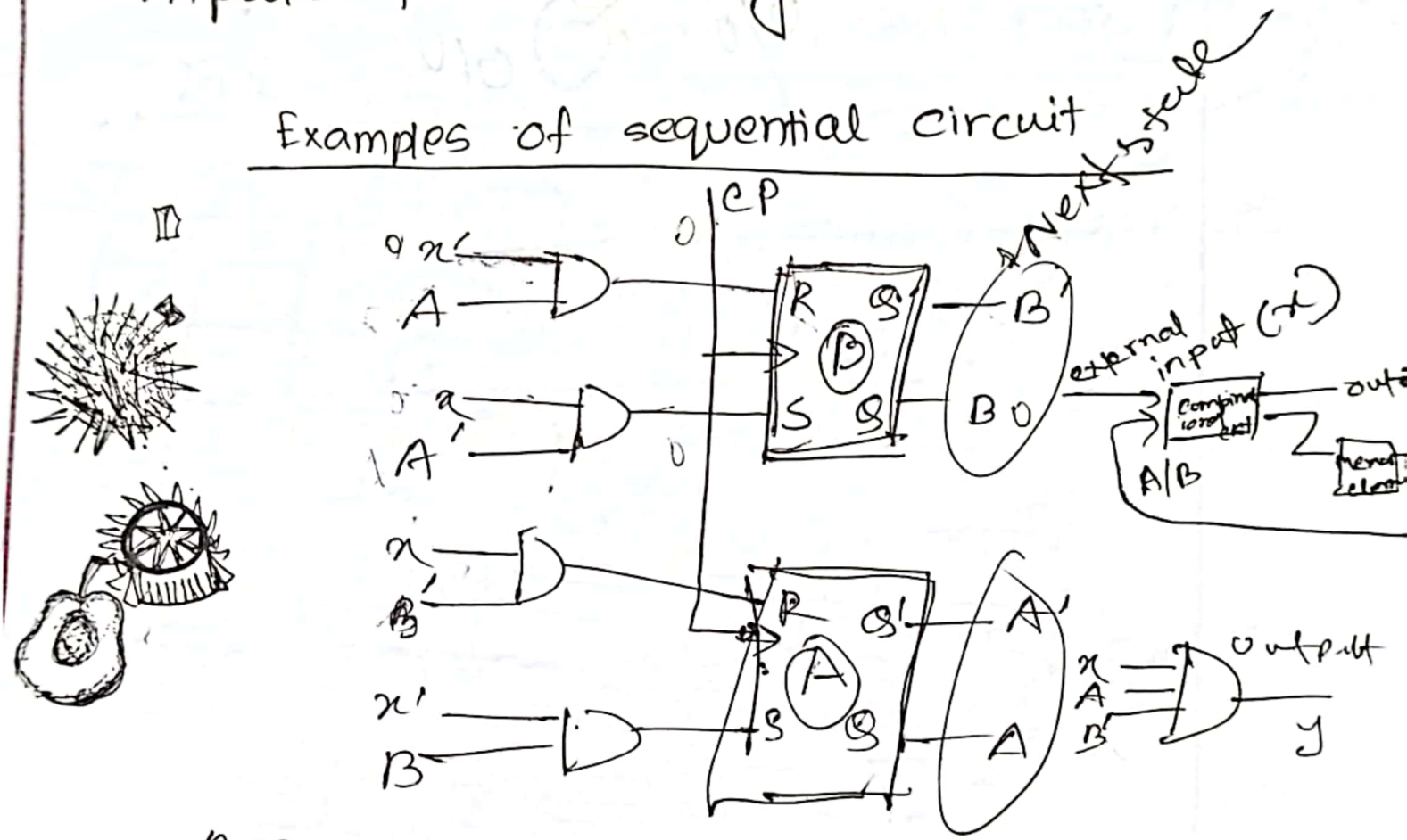
→ master is disabled, because CP = 0.

→ when CP = 1, the information at the external R and S transmitted to master.

→ Slave is isolated as long as the pulse is at its 1. Level because the output of the inverter is 0.

→ When pulse return to 0 the master is isolated which prevents the external inputs from affecting it.

Examples of sequential circuit



Present state	Next state		Output	
	$x=0$	$x=1$	$x=0$	$x=1$
AB	AB	AB	y	y
0 0	0 0	0 1	0	0
0 1	1 1	0 1	0	0
1 0	1 0	0 0	0	0

21/12/23

Present state	Next state		Output	
AB	x=0 AB	x=1 AB	x=0 y	x=1 y
0 0	0 0	0 1	0	0
0 1	1 1	0 1	0	0
1 0	1 0	0 0	0	1
1 1	1 0	1 1	0	0

$A(t) \rightarrow A(t+1) = (A'B + AB' + AB)x' + (AB)x$

$B(t) \rightarrow B(t+1) =$

$(A'B)x' + (A'B' + A'B + AB)x$

State equation — A state equation is an algebraic expression that specifies the condition for a FF state transition.

FF Characteristics Table

S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	?

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

FF Excitation table

During the design process we usually know the transition from present state to next state and we wish to find the flip flop ~~cont~~ input condition. For this reason we need a table that lists the required inputs for a given

Characteristic table (RS)

Q(t)	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	x
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	x

Excitation table

Q(t)	Q(t+1)	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Characteristics table (JK)

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

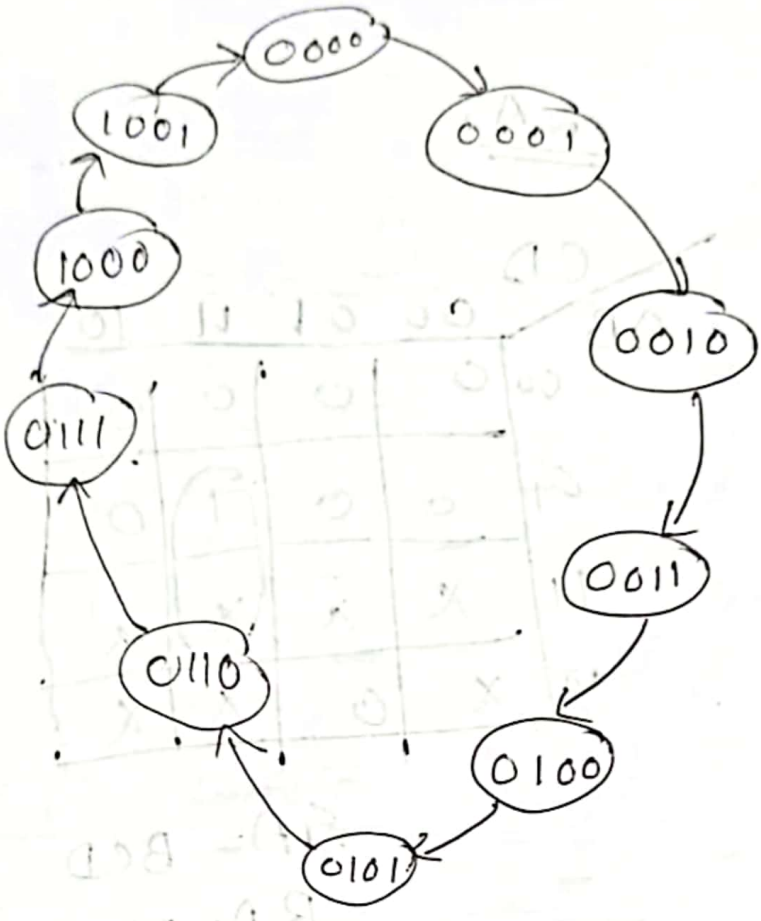
Excitation table

Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Design a BCD counter using RS flip-flop

Present state Next state

Present state	Next state	S_A R_A	S_B R_B	S_C R_C	S_D R_D
A B C D	A B C D				
0 0 0 0	0 0 0 1	0 x	0 x	0 x	1 0
0 0 0 1	0 0 1 0	0 x	0 x	1 0	0 1
0 0 1 0	0 0 1 1	0 x	0 x	x 0	1 0
0 0 1 1	0 1 0 0	0 x	1 0	0 1	0 1
0 1 0 0	0 1 0 1	0 x	x 0	0 x	1 0
0 1 0 1	0 1 1 0	0 x	x 0	1 0	0 1
0 1 1 0	0 1 1 1	0 x	x 0	x 0	1 0
0 1 1 1	1 0 0 0	1 0	0 1	0 1	0 1
1 0 0 0	1 0 0 1	x 0	0 x	0 x	1 0
1 0 0 1	0 0 0 0	0 1	0 x	0 x	1 1



Q(t)	Q(t+1)		
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

SA:

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	0	X	X

$S_A = BCD$

$R_D = AD$

$S_B = CD$

$R_B = D$

$S_C = A'B$

$R_C = B$

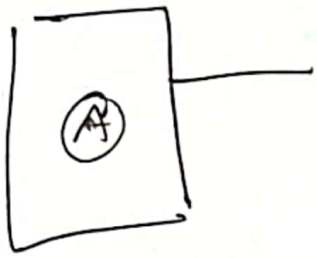
$S_D = C'$

$R_D = C$

6.23 (JK) – 6.24

6.24 (T)

2 4 21 → RS flip flop



7.4. Ripple counter

Binary Ripple Counter

→ A binary ripple counter consists of a series of complementing flip-flops with the output of each flip-flop connected to the CP input of the next higher order flip flop.

– The flip-flop holding the least significant bit receives the incoming count pulses.

A_0 A_1 A_2 A

A_4 A_3 A_2 A_1 → counts (0 to 15)

Modify to make it (0 to 9)

0 0 0 0

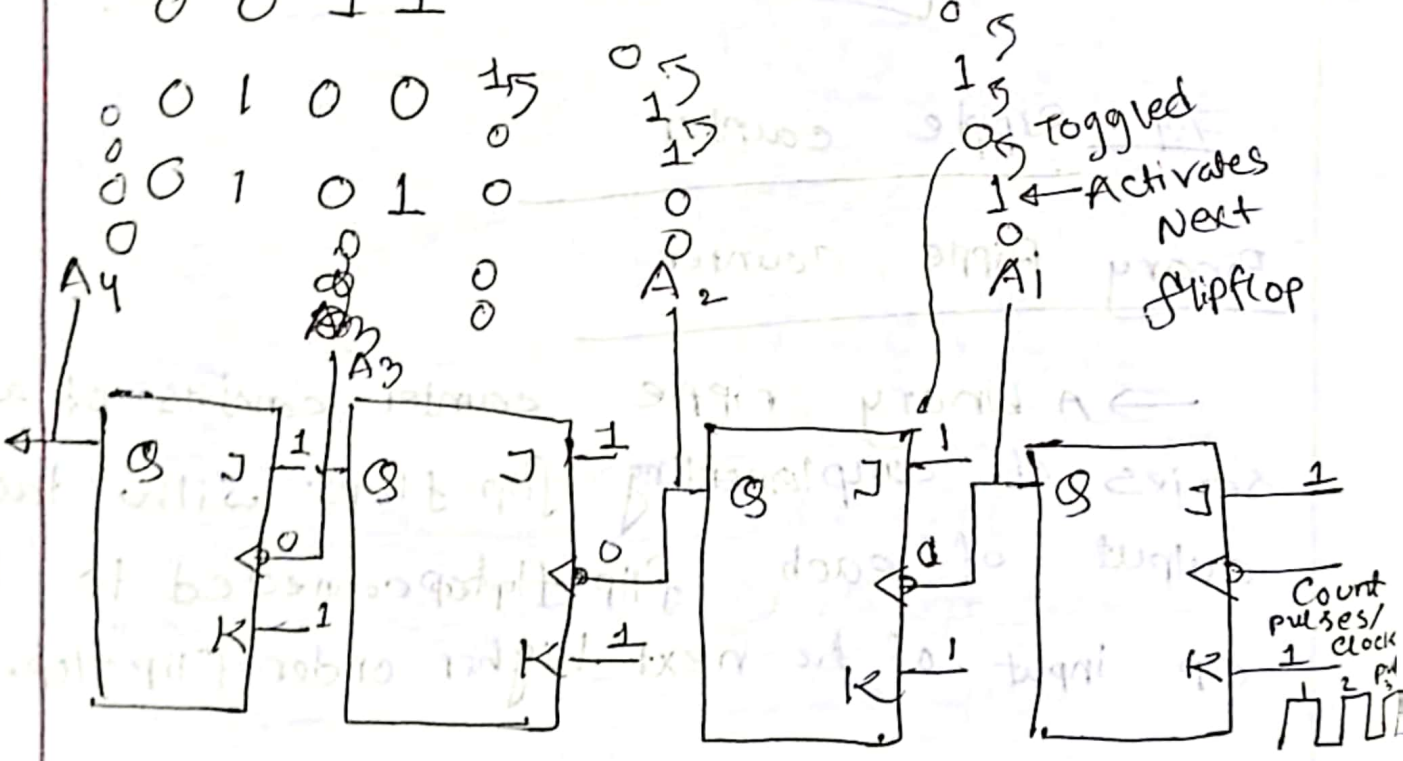
0 0 0 1

0 0 1 0

0 0 1 1

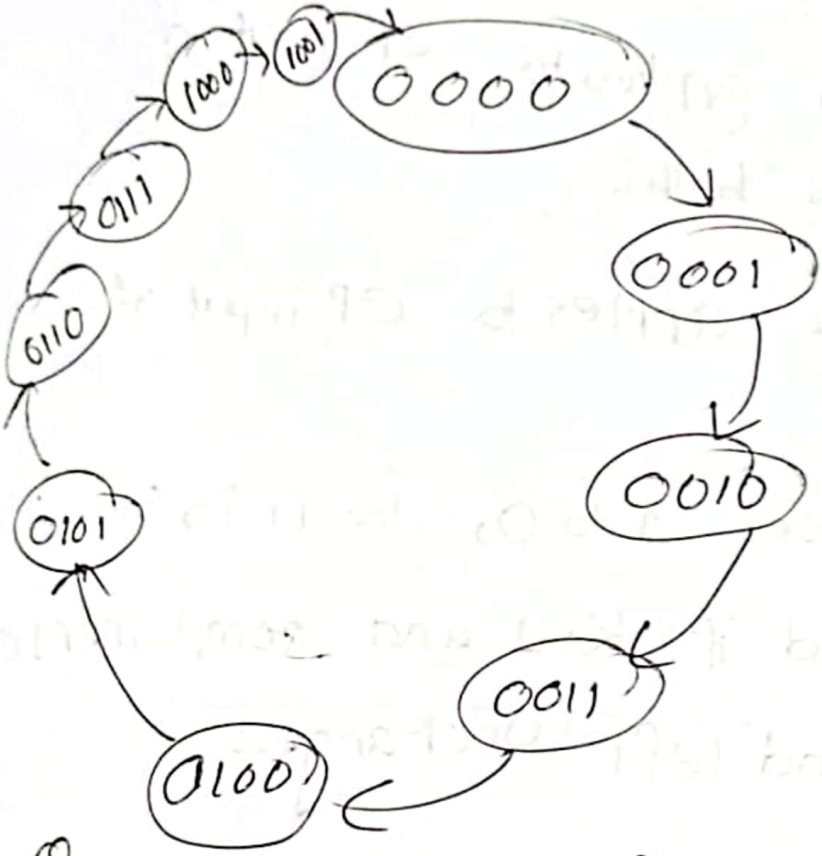
0 1 0 0

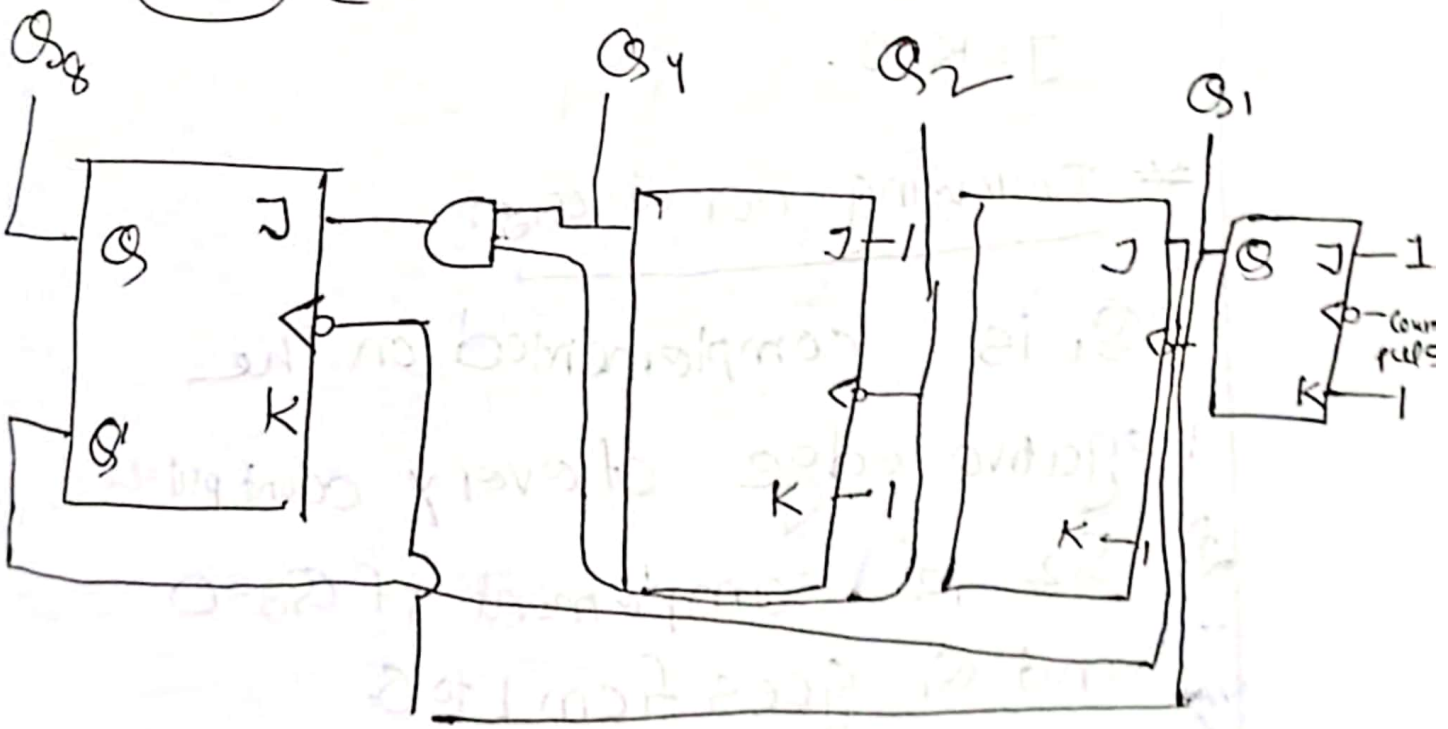
0 1 0 1



BCD ripple counter (0 to 9) (9 to 0).

BCD Ripple Counter





* The FF trigger on negative edge when CP goes from 1 to 0.
* Output of Q_1 applies to CP input of Q_2 and Q_8 both.
* Output of Q_2 applies to CP input of Q_4.
* CP input goes 1 to 0, the FF is set if J=1 is cleared if K=1 and complemented J=K=1 and left unchanged if J=K=0.

* Following conditions:

1) Q_1 is complemented on the negative edge of every count pulse.
2) Q_2 is complement if $Q_8=0$ and Q_1 goes from 1 to 0.

3. Q_4 is complemented when Q_2 goes from 1 to 0.

4. Q_8 is complemented when $Q_4 Q_2 = 11$ and Q_1 goes from 1 to 0.

$Q_2: 1 \to 0$ → $Q_8 = 0$, $Q_1 = 1 \to 0$

Q_8	Q_4	Q_2	Q_1	
0	0	0	0	↓ complement
0	0	0	1	↓
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
0	0	0	0	

2의 보수

$J = K = 1$ Q_1

Q_4

$Q_8 = 1$