Toronto Metropolitan University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Title:	System On Chip Design
Course Number:	COE 838
Semester/Year (e.g.F2016)	W2024

Instructor:	Dr. Gul Khan

Assignment/Lab Number:	
Assignment/Lab Title:	NoC Project Summary

Submission Date:	
Due Date:	

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SystemC based NoC (Network-on-Chip) Modelling
Course Project Summary
COE 838/EE8221: Systems-on-Chip Design

For this project, I will be developing a Network-on-Chip (NoC) simulator using SystemC, a powerful hardware description language that is capable of developing and simulating SoC Designs. The goal is to create a simulator that mimics the communication framework of NoC architectures, which are crucial for efficient data transfer among processing elements in multi-core systems (Multi-Core Processors).

To get started, I will need to implement various modules like source, sink, router,etc., where each module is simulating a specific function within the NoC. For example, the source module will generate packets with specific attributes such as data payload, source and destination IDs, and packet timing to mimic real-world packet generation. On the other hand, the sink module will record important information about incoming packets, allowing me to analyse packet delivery and latency.

The control unit of the simulator lies in the router module, which will manage packet routing based on destination addresses. This module will utilise other sub-modules like FIFO buffers, crossbars, and arbiters to efficiently direct traffic within the simulated NoC. Setting up the simulation environment will involve defining module interfaces, establishing connections between modules, and configuring simulation parameters such as packet size, network topology, and routing algorithms.

By running simulations with different configurations, I will be able to evaluate the performance of the NoC architecture in terms of throughput, latency, power consumption, area utilisation and other such parameters. Using the project manual provided on d2l, I will configure the simulation environment, execute simulations, and interpret the generated trace files to gain insights into NoC behaviour and performance characteristics. Overall, this project will provide me with valuable hands-on experience in designing and analysing on-chip communication systems.