



# Project IceStorm





2017-08-19: Released support for LP8K chips (in all package variants).

**2016-02-07:** Support for all package variants of LP1K, LP4K, LP8K and HX1K, HX4K, and HX8K.

**2016-01-17:** First release of IceTime timing analysis.

Video: <https://youtu.be/IG5CpFJRnOk>

**2015-12-27:** Presentation of the IceStorm flow at 32C3 ([Video on Youtube](#)).

**2015-07-19:** Released support for 8k chips. Moved IceStorm source code to GitHub.

**2015-05-27:** We have a working fully Open Source flow with Yosys and [Arachne-pnr](#)! Video: <http://youtu.be/yUiNlmvVOq8>

**2015-04-13:** Complete rewrite of IceUnpack, added IcePack, some major documentation updates

**2015-03-22:** First public release and short YouTube video demonstrating our work: <http://youtu.be/u1ZHcSNDQMM>

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## What is Project IceStorm?

Project IceStorm aims at documenting the bitstream format of Lattice iCE40 FPGAs and providing simple tools for analyzing and creating bitstream files. The IceStorm flow (Yosys, [Arachne-pnr](#), and IceStorm) is a fully open source Verilog-to-Bitstream flow for iCE40 FPGAs.

The focus of the project is on the iCE40 LP/HX 1K/4K/8K chips. (Most of the work was done on HX1K-TQ144 and HX8K-CT256 parts.) The iCE40 UltraPlus parts are also supported, including DSPs, oscillators, RGB and SPRAM. iCE40 LM, Ultra and UltraLite parts are not yet supported.

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