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Definition of hart #822

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Phantom1003 commented on Feb 22 • edited

I didn't find a clear definition of Hart in the manual, combine with [13] [14] and #607, I think hart is a high-level abstract above the hardware thread in Hyper-Threading Technology, which is the hardware ISA execute engine together with some machine state context (the environment), like privilege mode.

And as described in plic, a hart context is a privilege mode in a hardware execution thread.
For example, for a 4 Machine-Supervisor-User core system with 2-way SMT, we have 8 harts: core 0 M mode hart, core 0 S mode hart, core 1 M mode hart, core 1 S mode hart, core 2 M mode hart, core 2 S mode hart, core 3 M mode hart, core 3 S mode hart.

But the manual mixes up hart and software threads, and there are some words that confuse me a lot:

riscv-isa-manual/src/intro.tex
Lines 165 to 166 in 35a8890

```
165     Some EEIs support the creation and destruction of additional harts,
166     for example, via environment calls to fork new harts.
```

How can hart be created? We can only create software thread by fork system call. And as the example above, the hart is fixed with privilege mode supported and hardware thread in SMT, I think the accurate description should be:

```
Some EEIs support allocating and releasing harts.
```

Do I understand hart correctly and please give a detailed example.

Assignees

No one assigned

Labels

Projects

None yet

Milestone

No milestone

Development

No branches or pull requests

1 participant