I was too specific about AVRxt only, I need list of specials for ALL the variants of AVR starting by AVRxt

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Sure, here are the special instruction opcodes for all the variants of AVR starting with AVRxt:

1. AVRxt:
    - LPM (Load Program Memory)
    - ELPM (Extended Load Program Memory)
    - SPM (Store Program Memory)
    - ICALL (Indirect Call)
    - IJMP (Indirect Jump)
2. AVR1:
    - MOVW (Move Word)
    - MULS (Multiply Signed)
    - MULSU (Multiply Signed with Unsigned)
    - FMUL (Fractional Multiply)
    - FMULS (Fractional Multiply Signed)
    - FMULSU (Fractional Multiply Signed with Unsigned)
3. AVR2:
    - DES (Data Encryption Standard)
    - MOVW (Move Word)
    - MULS (Multiply Signed)
    - MULSU (Multiply Signed with Unsigned)
    - FMUL (Fractional Multiply)
    - FMULS (Fractional Multiply Signed)
    - FMULSU (Fractional Multiply Signed with Unsigned)
4. AVR3:
    - DES (Data Encryption Standard)
    - MOVW (Move Word)
    - MULS (Multiply Signed)
    - MULSU (Multiply Signed with Unsigned)
    - FMUL (Fractional Multiply)
    - FMULS (Fractional Multiply Signed)

FMULSU (Fractional Multiply Signed with Unsigned)

5. AVR4:
    AES (Advanced Encryption Standard)
    DES (Data Encryption Standard)
    MOVW (Move Word)
    MULS (Multiply Signed)
    MULSU (Multiply Signed with Unsigned)
    FMUL (Fractional Multiply)
    FMULS (Fractional Multiply Signed)
    FMULSU (Fractional Multiply Signed with Unsigned)

Note that this is not an exhaustive list, and there may be other special instructions in these processors that are not listed here. However, these are some examples of special instructions that may require special handling or mapping to your new assembler syntax.
