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how will be composed riscv instruction li r10, 0x99999999 ?



The RISC-V instruction set doesn't have a single instruction to load a 32-bit immediate value directly into a register. Instead, you need to use a combination of LUI (Load Upper Immediate) and ADDI (Add Immediate) instructions to achieve this. Here's how you can load the value 0x99999999 into register r10:

1. LUI: Load the upper 20 bits of the immediate value into the register.
2. ADDI: Add the lower 12 bits of the immediate value to the register.

To load 0x99999999 into r10, you can use the following instructions:

assembly

Copy code

```
lui r10, 0x999A0 // Load 0x999A0000 into r10  
addi r10, r10, -0x767 // Add the  
lower 12 bits (-0x767) to r10
```

Now, the register r10 contains the value 0x99999999. Note that I used the two's complement of 0x767 (0x899) to represent the negative value (-0x767) in the ADDI instruction.



this looks weird



Apologies if the example looked confusing. Let's try another approach to load the value 0x99999999 into register r10.

The value 0x99999999 can be broken down into two parts: 0x99990000 (upper 20 bits) and 0x00009999 (lower 12 bits). In this case, you can use the following instructions:

assembly

Copy code

```
lui r10, 0x99990 // Load 0x99990000 into r10 addi r10, r10, 0x9999 // Add the
lower 12 bits (0x9999) to r10
```

Now, the register r10 contains the value 0x99999999. This should be clearer and more straightforward.



umm, now you are using 16 bits, and thats VMEX approach))))



You're right, my previous response was incorrect. I apologize for the confusion. Since RISC-V uses a 32-bit instruction set and the ADDI instruction allows for only 12-bit immediates, we need to use multiple instructions to construct a 32-bit immediate value. Here's the correct way to load 0x99999999 into register r10 using a RISC-V instruction set:

The value 0x99999999 can be broken down into multiple parts to construct it in the register using shifts and logical OR:

1. 0x90000000
2. 0x09000000
3. 0x00990000
4. 0x00009999

assembly

 Copy code

```
lui r10, 0x90009 // Load 0x90000000 into r10 ori r10, r10, 0x9000 // OR
0x09000000 to r10 slli r10, r10, 12 // Shift left 12 bits to create space for
lower 12 bits ori r10, r10, 0x999 // OR 0x00000999 to r10 slli r10, r10, 4 //
Shift left 4 bits to create space for the last 4 bits ori r10, r10, 0x9 // OR
0x00000009 to r10
```

Now, the register r10 contains the value 0x99999999. This should be the correct and more accurate way of constructing a 32-bit immediate value using the RISC-V instruction set.





well, no, I WANT to use LUI and ADDI to load 0x99999999, just the numbers you presented are weird



Apologies for the confusion in my previous responses. I misunderstood your question. Here's the correct way to load 0x99999999 into register r10 using LUI and ADDI instructions in RISC-V:

1. Break down the 32-bit immediate value into a 20-bit upper part and a 12-bit lower part.

Upper 20 bits: 0x999A0 (0x999A0 << 12 = 0x999A0000)

Lower 12 bits: 0xFFFFFED7 (two's complement representation of -0x129)

assembly

Copy code

```
lui r10, 0x999A0 // Load the upper 20 bits into r10 (0x999A0000)
addi r10, r10, -0x129 // Add the lower 12 bits (-0x129) to r10
```

Now, the register r10 contains the value 0x99999999.



umm, using unsigned, I see $0x99999999 - 0x999A0000 = 0xFFFF9999$



Apologies for my earlier errors. You are right, and I appreciate your patience. If we break down the 32-bit immediate value 0x99999999 into a 20-bit upper part and a 12-bit lower part using unsigned representation, we get:

Upper 20 bits: 0x999A0 (0x999A0 << 12 = 0x999A0000)

Lower 12 bits: 0xFFF (0x99999999 - 0x999A0000 = 0xFFFF9999, considering only the lower 12 bits)

assembly

Copy code

```
lui r10, 0x999A0 // Load the upper 20 bits into r10 (0x999A0000)
addi r10, r10, 0xFFF // Add the lower 12 bits (0xFFF) to r10
```

```
0xFFF // Add the lower 12 bits (0xFFF) to r10
```

Now, the register r10 contains the value 0x99999999.



well I still cant get it ... 20 bits representation of upper part of 0x99999999 seems to be 0x999999 or not?



You are correct, and I apologize for my previous mistakes. The correct breakdown of the 32-bit immediate value 0x99999999 into a 20-bit upper part and a 12-bit lower part is:

Upper 20 bits: 0x99999 (0x99999 << 12 = 0x999990000)

Lower 12 bits: 0x999 (0x99999999 - 0x999990000 = 0x999)

However, since RISC-V uses a 32-bit address space, only the lower 32 bits are considered. The upper 20 bits of 0x999990000 are then truncated to 0x99990.

Now, you can use the LUI and ADDI instructions to load the value 0x99999999 into register r10:

assembly

Copy code

```
lui r10, 0x99990 // Load the upper 20 bits into r10 (0x99990000)
addi r10, r10, 0x999 // Add the lower 12 bits (0x999) to r10
```

Finally, the register r10 contains the value 0x99999999.



umm, I still think that in REAL risc-v the LUI r10, 0x99999 is correct



You are correct, and I apologize for the confusion in my previous responses. Here is the correct way to load the value 0x99999999 into register r10 using LUI and ADDI instructions

in RISC-V:

1. Break down the 32-bit immediate value into a 20-bit upper part and a 12-bit lower part.

Upper 20 bits: $0x99999 \ll 12 = 0x999990000$

Lower 12 bits: $0x999 \ll 0 = 0x999$

Since RISC-V uses a 32-bit address space, the upper 20 bits of $0x999990000$ are truncated to $0x99990$, but when using LUI, the immediate value will be shifted back to the correct position.

assembly

 Copy code

```
lui r10, 0x99999 // Load the upper 20 bits into r10 (0x999990000)
addi r10, r10, 0x999 // Add the lower 12 bits (0x999) to r10
```

Now, the register r10 contains the value $0x99999999$.



okay, this seems to be true finally weird is that in VMEX which uses 16bit immediate parts for upper LUI and lower ADDI when I am adding $0x99990000 + 0x00009999$ I got $0x99989999$... why?



I apologize for the confusion earlier. I realize now that you were referring to the VexRiscv (VMEX) CPU, which uses an extension with 16-bit immediates for the LUI and ADDI instructions. In that case, the behavior you observed is expected.

In VexRiscv with 16-bit immediate extensions, the LUI and ADDI instructions work slightly differently. When you use the LUI instruction with a 16-bit immediate, the immediate value is shifted left by 16 bits instead of 12, as in the standard RISC-V LUI instruction.

So, when you perform the following operation:

csharp

 Copy code

```
0x99990000 (from LUI) + 0x00009999 (from ADDI)
```



The result is 0x99989999 because the LUI instruction effectively loaded 0x99980000 into the register.

To correctly load 0x99999999 using 16-bit immediate extensions in VexRiscv, you should do the following:

1. Break down the 32-bit immediate value into a 16-bit upper part and a 16-bit lower part.

Upper 16 bits: 0x9999 (0x9999 << 16 = 0x99990000)

Lower 16 bits: 0x9999 (0x99999999 - 0x99990000 = 0x9999)

assembly

 Copy code

```
lui r10, 0x9999 // Load the upper 16 bits into r10 (0x99990000)
addi r10, r10, 0x9999 // Add the lower 16 bits (0x9999) to r10
```

Now, the register r10 contains the value 0x99999999.



yes, okay, I expect I am now working with signed numbers and thats the reason ... I apologize here, as I dont want to confuse you RISC-V is RISC-V and it uses 20+12 bit immediate values, where my VMEX uses 16+16 bit immediate values, but the signed calculations (done in PC debbuger) were weird ... here I expect for "unsigned" loading of larger values natural combination of LUI and ORI in fact ... is this also used in RISC-V world sometimes?



Apologies for the confusion earlier. Yes, you are correct that RISC-V uses 20-bit and 12-bit immediate values for LUI and ADDI instructions, respectively. For VMEX with 16-bit immediate extensions, you have 16-bit immediate values for both LUI and ADDI.

In the RISC-V world, it is common to use a combination of LUI and ORI instructions for loading large unsigned immediate values. This can help avoid issues with signed numbers when using ADDI, especially for loading large unsigned values that might be interpreted as negative when using ADDI.

Here's an example of loading an unsigned value 0x99999999 into a register in RISC-V using LUI and ORI:

1. Break down the 32-bit immediate value into a 20-bit upper part and a 12-bit lower part.
Upper 20 bits: 0x99999 (0x99999 << 12 = 0x999990000)
Lower 12 bits: 0x999 (0x99999999 - 0x999990000 = 0x999)

assembly

 Copy code

```
lui r10, 0x99999 // Load the upper 20 bits into r10 (0x999990000)
ori r10, r10, 0x999 // OR the lower 12 bits (0x999) to r10
```

Now, the register r10 contains the value 0x99999999.

In your VMEX case with 16-bit immediate values, you can also use a combination of LUI and ORI for loading large unsigned values:

1. Break down the 32-bit immediate value into a 16-bit upper part and a 16-bit lower part.
Upper 16 bits: 0x9999 (0x9999 << 16 = 0x99990000)
Lower 16 bits: 0x9999 (0x99999999 - 0x99990000 = 0x9999)

assembly

 Copy code

```
lui r10, 0x9999 // Load the upper 16 bits into r10 (0x99990000)
ori r10, r10, 0x9999 // OR the lower 16 bits (0x9999) to r10
```

Now, the register r10 contains the value 0x99999999. This approach should work well for loading unsigned values without worrying about sign issues in VMEX or RISC-V.



yes, this is exactly what I am facing here now in debugger and want to use ORI ... thanks :-)



You're welcome! I'm glad that the explanation was helpful. Using ORI for loading large unsigned immediate values is a good approach, as it avoids issues with signed numbers that

can arise when using ADDI.

If you have any more questions or need further assistance, please feel free to ask. Good luck with your debugging and VMEX or RISC-V project!
