riscv / **riscv-isa-manual** Public

Code Issues 75 Pull requests 16 Actions Projects Security Insigh

New issue

Jump to bottom

Considerations about Volume 1 Instruction Listings: "RV32/64G" or "Unprivileged"? #816

Open **a4lg** opened this issue on Jan 23 · 0 comments

a4lg commented on Jan 23 Contributor

Attachment

Annotated Chapter 26 of the ISA Manual, Volume 1 (based on `9181ac0b74a6` + riscv/riscv-opcodes@ `f2f4583551fe` on page 146)

This attached PDF file corresponds "Relevant Text: How do we deal with it?" chapter below.

Background

The ISA Manual, Volume 1 has "RV32/64G Instruction Set Listings" section (Chapter 24 in ratified 20191213, Chapter 26 in the latest draft) but it contains more than "RV32/64G" instructions.

```
Shortcut: G = IMAFD_Zicsr_Zifencei
```

1. commit `66bed24` : Version 20191213 has instructions in `Q` extension (added in commit `8b7b607`). Since then,
2. commit `feee60d` : **@aswaterman** added `Zfh` / `Zfhmin` instructions
3. commit `ad5f04d` : ...and `Zihintpause` hint instruction `PAUSE` (along with `FENCE.TSO` , a backward-compatible `FENCE` extension without any extension name)

I am merging this chapter with riscv/riscv-opcodes and...

1. riscv/riscv-opcodes@ `f573c7aec070` : I added `Zicbom` , `Zicbop` and `Zicboz` unprivileged cache management instructions (manually deleted in riscv-isa-manual; see **Update Instruction Tables based on riscv-opcodes** #815)
2. riscv/riscv-opcodes@ `f2f4583551fe` : ... and I ported **@aswaterman**'s `Zfh` / `Zfhmin` work to riscv/riscv-opcodes (with minor modifications).

Current Status

There are four extensions not in "RV32/64G" (in the current ISA Manual, Volume 1):

1. `Q`
2. `Zfh`
3. `Zfhmin`
4. `Zihintpause` (hint instruction only)

... and three more if we entirely use riscv/riscv-opcodes-generated tables.

5. `Zicbom`
6. `Zicbop` (hint instructions only)
7. `Zicboz`

Relevant Text: How do we deal with it?

I (personally) think chapter name "RV32/64G Instruction Set Listings" is outdated and should be changed to "RISC-V Unprivileged Instruction Set Listings". *On the other hand,* some sentences in this chapter clearly describes about RV32/64G or "base ISA" and *just* replacing the chapter name (and endlessly adding unprivileged instructions to this chapter) might not be the best idea.

Of course, there are alternatives such as separating "RV32/64G" and other (specialized) unprivileged instructions.

I list all relevant references:

RV-1. Chapter Name

> RV32/64G Instruction Set Listings

Should be changed if we reorganize this chapter as "RISC-V Unprivileged Instruction Set Listings".

RV-2. Reference to Instruction Listings

> This chapter presents opcode maps and instruction-set listings for RV32G and RV64G.

Should be changed if we reorganize this chapter as "RISC-V Unprivileged Instruction Set Listings".

RV-3. Caption of Table (26).1

> Table 26.1: RISC-V base opcode map, inst[1:0]=11

We can keep the text.

RV-4. Reference to Table (26).1

> Table 26.1 shows a map of the major opcodes for RVG.

Unless we don't add new major opcodes such like OP-V or OP-P, we can keep this text.

RV-5. Caption of Table (26).2

> Table 26.2: Instruction listing for RISC-V

We can keep the text.

RV-6. RISC-V ISA Base and Further Extensions

> As we move beyond IMAFDC into further instruction-set extensions, the added instructions tend to be more domain-specific and only provide benefits to a restricted class of applications, e.g., for multimedia or security. Unlike most commercial ISAs, the RISC-V ISA design clearly separates the base ISA and broadly applicable standard extensions from these more specialized additions. Chapter 27 has a more extensive discussion of ways to add extensions to the RISC-V ISA.

This is the reason I think that just changing the chapter name might not be a good idea. If we did change all wrong, we might spoil the entire intention of this chapter.

G-1. Definition of RVG

> For this purpose, we define a combination of a base ISA (RV32I or RV64I) plus selected standard extensions (`IMAFD` , `Zicsr` , `Zifencei`) as a “general-purpose” ISA, and we use the abbreviation `G` for the `IMAFDZicsr Zifencei` combination of instruction-set extensions.

We must preserve the text (at least, the main intention must be preserved).

G-2. Optional RVGC

> We believe RV32G and RV64G provide simple but complete instruction sets for a broad range of general-purpose computing. The optional compressed instruction set described in Chapter 18 can be added (forming RV32GC and RV64GC) to improve performance, code size, and energy efficiency, though with some additional hardware complexity.

This says about RVG with compressed instructions.

Assignees

No one assigned

Labels

None yet

Projects

Projects

None yet

Milestone

No milestone

Development

No branches or pull requests

1 participant