RISC-V Reference Card

An unofficial reference sheet for RISC-V, the free and libre ISA from Berkeley. (**PDF**).

What's inside?

- The base ISA (RV32I), with opcode values and C-like descriptions
- Standard ISA extensions (most but not all yet)
- Register aliases and calling conventions
- Pseudoinstructions

Other information from the more official reference cards not specific to the ISA, like the stack/heap memory layout, IEEE 754 floating-point layout, and size prefixes, have been omitted.

Why?

In RISC tradition, the assembly reference for MIPS and RISC-V fits onto a single double-sided 'Green Sheet'.

When I took CS 61C at UC Berkeley in 2017, we were the first semester taught using RISC-V, and our reference card scans from our RISC-V textbook were low-quality. I wanted a card I didn't have to squint at, so I typeset it in LaTeX.

The latest Berkeley course reference card is also available.

This little reference has grown well past a double-sided page, but if you still want the original you can print the first and last pages for the asm opcodes and calling convention.

Contributing

This repository is not actively developed, but pull requests are accepted for fixes, new ISA standard extensions, style improvements, or other such changes. Please include a rebuilt PDF binary in your pull request.

Print-friendly format is preferred, when possible: legible font sizes, clean page breaks and full letter page width usage. (A4 support may be a good thing to check.)

Some ideas if you are truly motivated:

- Multiple outputs (pdfs) for different domains / ISA extension sets, or for 32 / 64-bit support
- Directly parsing the spec, banishing typos forever
- Build system to select binary or hex instruction opcodes
- Other ISA support? (probably only feasible for RISC ISAs)

Licensing

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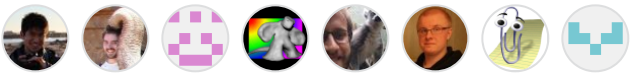

Languages

- **TeX** 100.0%