New issue

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Instruction-address-misaligned exceptions v.s. compressed instructions #856

Open **SimonSapin** opened this issue on Jun 18 · 1 comment

SimonSapin commented on Jun 18 • edited

riscv-isa-manual/src/rv32.tex
Lines 813 to 821 in 4a01cbb

```
813     The JAL and JALR instructions will generate an
814     instruction-address-misaligned exception if the target address is not
815     aligned to a four-byte boundary.
816
817     \begin{commentary}
818     Instruction-address-misaligned exceptions are not possible on machines
819     that support extensions with 16-bit aligned instructions, such as the
820     compressed instruction-set extension, C.
821     \end{commentary}
```

This normative paragraph and this commentary seem to contradict each other. I suspect that the former should read instead:

> [...] if the target address is not aligned to an IALIGN-bit boundary.

aswaterman commented on Jun 19 Member

The quoted normative statement is true for the base ISA, which has IALIGN=32. This constraint is relaxed by extensions that reduce IALIGN. But it might be clearer to express the constraint in terms of IALIGN here.

Assignees

No one assigned

Labels

Labels

None yet

Projects

None yet

Milestone

No milestone

Development

No branches or pull requests

2 participants