can you please list uncommon special instructions of AVRxt, PIC16, PIC18, PIC24, 8080, Z80, 6502? I am not interested in regular common instruction, only in the conceptual differences between the processors to obtain SET of pseudoinstructions I will need to implement in my assembly language, thanks

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Sure, here are some of the uncommon special instructions for each of the processors you mentioned:

1. AVRxt:
    - LPM (Load Program Memory)
    - ELPM (Extended Load Program Memory)
    - SPM (Store Program Memory)
    - ICALL (Indirect Call)
    - IJMP (Indirect Jump)
2. PIC16:
    - MOVLB (Move Literal to BSR)
    - CALLW (Call Subroutine, 24-bit address)
    - TBLRD (Table Read)
    - TBLRD*+ (Table Read with Auto-Increment)
    - TBLWT*+ (Table Write with Auto-Increment)
3. PIC18:
    - ADDFSR (Add to FSR Register)
    - BRA (Branch Unconditionally)
    - CALL (Call Subroutine, 24-bit address)
    - GOTO (Jump Unconditionally, 24-bit address)
    - MOVLB (Move Literal to BSR)
4. PIC24:
    - ADDFSR (Add to FSR Register)
    - BRA (Branch Unconditionally)
    - CALL (Call Subroutine, 24-bit address)
    - GOTO (Jump Unconditionally, 24-bit address)
    - MOV.D (Move Double Word)
5. 8080:

CPIR (Compare and Increment Repeatedly)
IN (Input Data from Port)
OUT (Output Data to Port)
XTHL (Exchange H and L Registers with Stack Top)
XRI (Exclusive OR Immediate)

6. Z80:
   IN (Input Data from Port)
   OUT (Output Data to Port)
   DJNZ (Decrement and Jump if Not Zero)
   LD A,I (Load A Register from Interrupt Page Address)
   LD A,R (Load A Register from Refresh Register)
7. 6502:
   BRK (Software Interrupt)
   JSR (Jump to Subroutine)
   JMP (Jump to Address)
   NOP (No Operation)
   RTI (Return from Interrupt)

Note that this is not an exhaustive list, and there may be other uncommon instructions in these processors that are not listed here. However, this should give you an idea of the types of instructions that may require special handling or mapping to your new assembler syntax.