

# **About SpinalHDL**

### SpinalHDL is:

- A language to describe digital hardware
- Compatible with EDA tools, as it generates VHDL/Verilog files
- Much more powerful than VHDL, Verilog, and SystemVerilog in its syntax and features
- Much less verbose than VHDL, Verilog, and SystemVerilog
- Not an HLS, nor based on the event-driven paradigm
- Only generates what you asked it in a one-to-one way (no black-magic, no black box)
- Not introducing area/performance overheads in your design (versus a hand-written VHDL/Verilog design)
- Based on the RTL description paradigm, but can go much further
- Allowing you to use Object-Oriented Programming and Functional Programming to elaborate your hardware and verify it
- Free and can be used in the industry without any license

## Links

- Documentation https://spinalhdl.github.io/SpinalDoc-RTD/
- Chinese documentation https://thucgra.github.io/SpinalHDL\_Chinese\_Doc/

- API reference https://spinalhdl.github.io/SpinalHDL/dev/spinal/index.html
- Presentation of the language https://spinalhdl.github.io/SpinalDoc-RTD/master/SpinalHDL/Getting%20Started/presentation.html
- SBT base project https://github.com/SpinalHDL/SpinalTemplateSbt
- Gradle base project https://github.com/SpinalHDL/SpinalTemplateGradle
- Jupyter bootcamp https://github.com/SpinalHDL/Spinal-bootcamp
- Workshop https://github.com/SpinalHDL/SpinalWorkshop
- Google group https://groups.google.com/forum/#!forum/spinalhdl-hardware-description-language
- Donation channel https://opencollective.com/spinalhdl

```
English: chat on gitter 中文: chat on gitter
```

# Get it

SpinalHDL is simply a set of Scala libraries. Include them into your project and you're good to go! If you're unsure about what to do, simply clone one of our example projects (see links above).

# SBT (Scala build tool)

```
scalaVersion := "2.11.12"

libraryDependencies ++= Seq(
   "com.github.spinalhdl" % "spinalhdl-core_2.11" % "latest.release",
   "com.github.spinalhdl" % "spinalhdl-lib_2.11" % "latest.release",
   compilerPlugin("com.github.spinalhdl" % "spinalhdl-idsl-plugin_2.11" % "latest.release")
)
```

You can force SBT to pick a specific SpinalHDL version by replacing latest.release with a specific version. See the SpinalHDL SBT Template project's build.sbt file for a full SBT example.

### Gradle

```
repositories {
          mavenCentral()
}
dependencies {
          compile group: 'com.github.spinalhdl', name: 'spinalhdl-core_2.11', version: '1.6.4'
```

```
compile group: 'com.github.spinalhdl', name: 'spinalhdl-lib_2.11', version: '1.6.4'
}
```

## Mill(Build Tool)

```
import mill._
import mill.scalalib._

object MySpinalModule extends ScalaModule {
  def scalaVersion = "2.11.12"

  def ivyDeps = Agg(
    ivy"com.github.spinalhdl::spinalhdl-core:1.6.4",
    ivy"com.github.spinalhdl::spinalhdl-lib:1.6.4",
  )

  def scalacPluginIvyDeps = Agg(ivy"com.github.spinalhdl::spinalhdl-idsl-plugin:1.6.4")
}
```

#### **JAR**

https://oss.sonatype.org/content/groups/public/com/github/spinalhdl/spinalhdl-core\_2.11/https://oss.sonatype.org/content/groups/public/com/github/spinalhdl/spinalhdl-lib\_2.11/

The files are available on Mayen as well.

# **Change logs**

https://github.com/SpinalHDL/SpinalHDL/tags

## License

The SpinalHDL core is using the LGPL3 license while SpinalHDL lib and others are using the MIT license. That's for the formalities. But there are some practical statements implied by those licenses:

Your freedoms are:

- You can use SpinalHDL core and lib in your closed/commercial projects.
- The generated RTL is yours (.vhd/.v files)
- Your hardware description is yours (.scala files)

Your obligations (and my wish) are:

• If you modify the SpinalHDL core (the compiler itself), please, share your improvements.

README.md

### Releases 16



+ 15 releases

# Sponsor this project



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## **Packages**

No packages published

## Contributors 83





















+ 72 contributors

### Environments 1

github-pages (Active)



## Languages

• Scala 75.5%

Verilog 11.7%Python 4.3%

• VHDL 2.7% • SystemVerilog 2.3% • C++ 2.0% • Other 1.5%