

GPIO — General purpose input/output

The general purpose input/output pins (GPIOs) are grouped as one or more ports with each port having up to 32 GPIOs.

The number of ports and GPIOs per port may vary with product variant and package. Refer to [Registers](#) and [Pin assignments](#) for more information about the number of GPIOs that are supported.

GPIO has the following user-configurable features:

- Up to 32 GPIO pins per GPIO port
- Configurable output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- All pins can be individually mapped to interface blocks for layout flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register
- Support for secure and non-secure attributes for pins in conjunction with the system protection unit ([SPU — System protection unit](#))

GPIO port and the GPIO pin details illustrates the GPIO port containing 32 individual pins, where PIN0 is illustrated in more detail as a reference. All signals on the left side in the illustration are used by other peripherals in the system and therefore not directly available to the CPU.

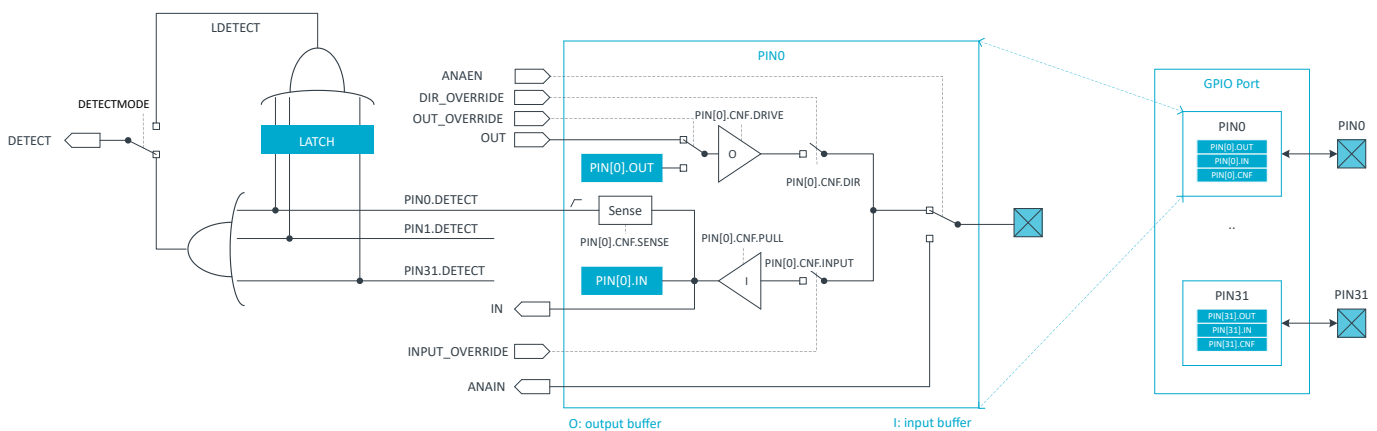


Figure 1. GPIO port and the GPIO pin details

Parent topic: [Peripherals](#)

Pin configuration

The GPIO port peripheral implements up to 32 pins, PIN0 through PIN31. Each of these pins can be individually configured in the PIN_CNF[n] registers (n=0..31).

The following parameters can be configured through these registers:

- Direction
- Drive strength
- Enabling of pull-up and pull-down resistors
- Pin sensing
- Input buffer disconnect
- Analog input (for selected pins)

Note: All write-capable registers are retained registers, see [POWER — Power control](#) for more information.

The input buffer of a GPIO pin can be disconnected from the pin to enable power savings when the pin is not used as an input, see [GPIO port and the GPIO pin details](#). Inputs must be connected to get a valid input value in the [IN](#) register, and for the sense mechanism to get access to the pin.

Other peripherals in the system can connect to GPIO pins and override their output value and configuration, or read their analog or digital input value. See [GPIO port and the GPIO pin details](#).

Selected pins also support analog input signals, see ANAIN in [GPIO port and the GPIO pin details](#). The assignment of the analog pins can be found in [Pin assignments](#).

The following delays should be taken into considerations:

- There is a delay of 2 CPU clock cycles from the GPIO pad to the [IN](#) register.
- The GPIO pad must be low (or high depending on the SENSE polarity) for 3 CPU clock cycles after DETECT has gone high to generate a new DETECT signal.

Note: When a pin is configured as digital input, care has been taken to minimize increased current consumption when the input voltage is between V_{IL} and V_{IH} . However, it is a good practice to ensure that the external circuitry does not drive that pin to levels between V_{IL} and V_{IH} for a long period of time.

Pin sense mechanism

Pins sensitivity can be individually configured, through the SENSE field in the PIN_CNF[n] register, to detect either a high level or a low level on their input.

When the correct level is detected on any such configured pin, the sense mechanism will set the DETECT signal high. Each pin has a separate DETECT signal. Default behavior, defined by the DETECTMODE register, is that the DETECT signals from all pins in the GPIO port are combined into one common DETECT signal that is routed throughout the system, which then can be utilized by other peripherals. This mechanism is functional in both System ON and System OFF modes.

DETECTMODE and DETECTMODE_SEC are provided to handle secure and non-secure pins. DETECTMODE_SEC register is available to control the behavior associated to pin marked as secure, while the DETECTMODE register is restricted to pin marked as non-secure. Please refer to [GPIO security](#) for more details.

Make sure that a pin is in a level that cannot trigger the sense mechanism before enabling it. The DETECT signal will go high immediately if the SENSE condition configured in the PIN_CNF registers is met when the sense mechanism is enabled. This will trigger a PORT event if the DETECT signal was low before enabling the sense mechanism.

The DETECT signal is also used by power and clock management system to exit from System OFF mode, and by GPIOTE to generate the PORT event. In addition GPIOTE_SEC is used for PORT event related to secure pins). See [POWER — Power control](#) and [GPIOTE — GPIO tasks and events](#) for more information about how the DETECT signal is used.

When a pin's PINx.DETECT signal goes high, a flag will be set in the [LATCH](#) register. For example, when the PIN0.DETECT signal goes high, bit 0 in the [LATCH](#) register will be set to '1'. If the CPU performs a clear operation on a bit in the [LATCH](#) register when the associated PINx.DETECT signal is high, the bit in the [LATCH](#) register will not be cleared. The [LATCH](#) register will only be cleared if the CPU explicitly clears it by writing a '1' to the bit that shall be cleared, i.e. the [LATCH](#) register will not be affected by a PINx.DETECT signal being set low.

The LDETECT signal will be set high when one or more bits in the [LATCH](#) register are '1'. The LDETECT signal will be set low when all bits in the [LATCH](#) register are successfully cleared to '0'.

If one or more bits in the [LATCH](#) register are '1' after the CPU has performed a clear operation on the [LATCH](#) registers, a rising edge will be generated on the LDETECT signal. This is illustrated in [DETECT signal behavior](#).

Note: The CPU can read the [LATCH](#) register at any time to check if a SENSE condition has been met on one or more of the the GPIO pins, even if that condition is no longer met at the time the CPU queries the [LATCH](#) register. This mechanism will work even if the LDETECT signal is not used as the DETECT signal.

The LDETECT signal is by default not connected to the GPIO port's DETECT signal, but via the DETECTMODE register it is possible to change from default behavior to DETECT signal being derived directly from the LDETECT signal instead. See [GPIO port and the GPIO pin details](#). [DETECT signal behavior](#) illustrates the DETECT signal behavior for these two alternatives.

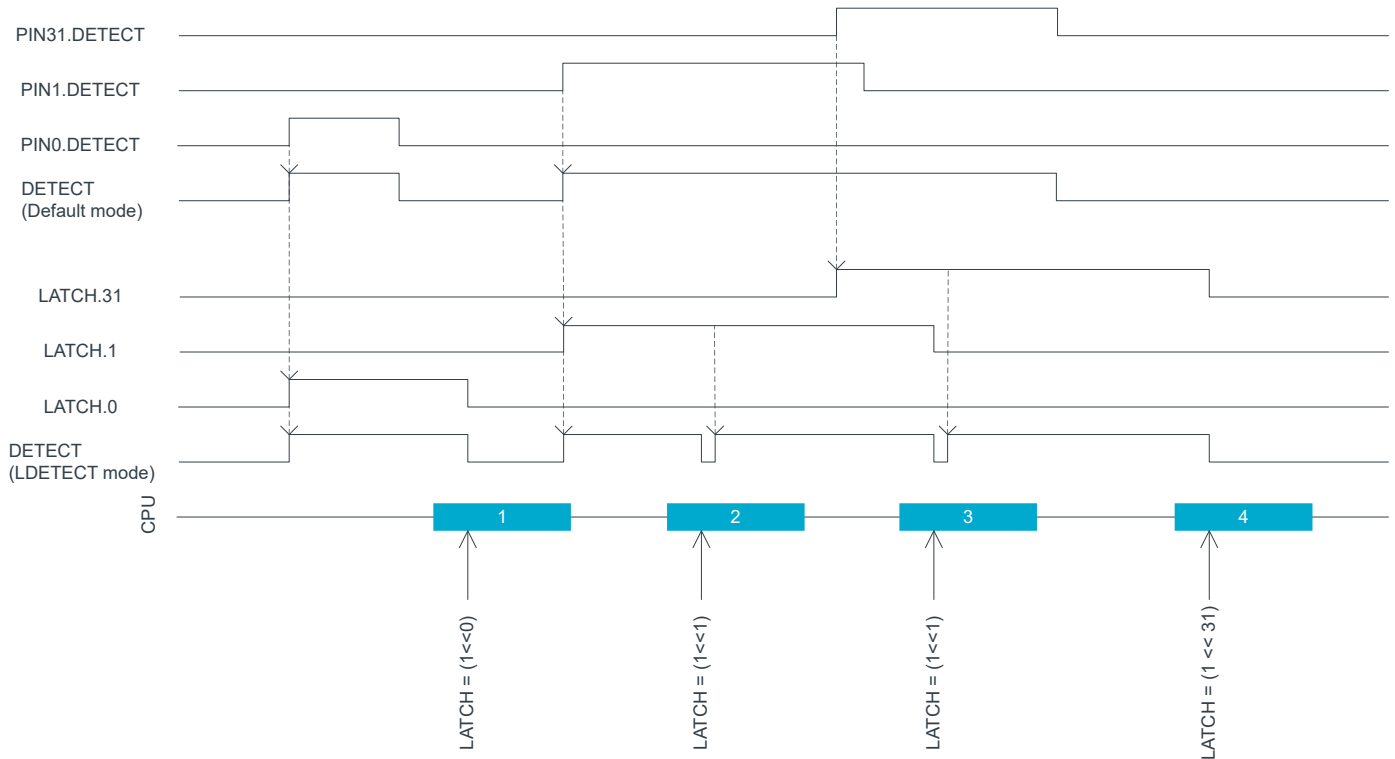


Figure 2. DETECT signal behavior

GPIO security

The general purpose input/output (GPIO) peripheral is implemented as a *split-security* peripheral. If marked as non-secure, it can be accessed by both secure and non-secure accesses but will behave differently depending on the access type.

A non-secure peripheral access will only be able to configure and control pins defined as non-secure in the system protection unit (SPU) GPIOPORT.PERM[] register(s).

A non-secure access to a register or a bitfield controlling a pin marked as secure in GPIO.PERM[] register(s) will be ignored. Write access will have no effect and read access will return a zero value.

No exception is triggered when a non-secure access targets a register or bitfield controlling a secure pin. For example, if the bit *i* is set in the SPU.GPIO.PERM[o] register (declaring Pin Po.i as secure), then

- non-secure write accesses to OUT, OUTSET, OUTCLR, DIR, DIRSET, DIRCLR and LATCH registers will not be able to write to bit *i* of those registers
- non-secure write accesses to registers PIN[i].OUT and PIN_CNF[i] will be ignored
- non-secure read accesses to registers OUT, OUTSET, OUTCLR, IN, DIR, DIRSET, DIRCLR and LATCH will always read a '0' for the bit at position *i*
- non-secure read accesses to registers PIN[i].OUT, PIN[i].OUT and PIN_CNF[i] will always return 0

The GPIO.DETECTMODE and GPIO.DETECTMODE_SEC registers are handled differently than the other registers mentioned before. When accessed by a secure access, the DETECTMODE_SEC register control the source for the DETECT_SEC signal for the pins marked as secure. When accessed by a non-secure access, the DETECTMODE_SEC is read as zero and write accesses are ignored. The GPIO.DETECTMODE register controls the source for the DETECT_NSEC signal for the pins defined as non-secure.

The DETECT_NSEC signal is routed to the GPIOTE peripheral, allowing generation of events and interrupts from pins marked as non-secure. The DETECT_SEC signal is routed to the GPIOTESEC peripheral, allowing generation of events and interrupts from pins marked as secure. [Principle of direct pin access](#) illustrates how the DETECT_NSEC and DETECT_SEC signals are generated from the GPIO PIN[].DETECT signals.

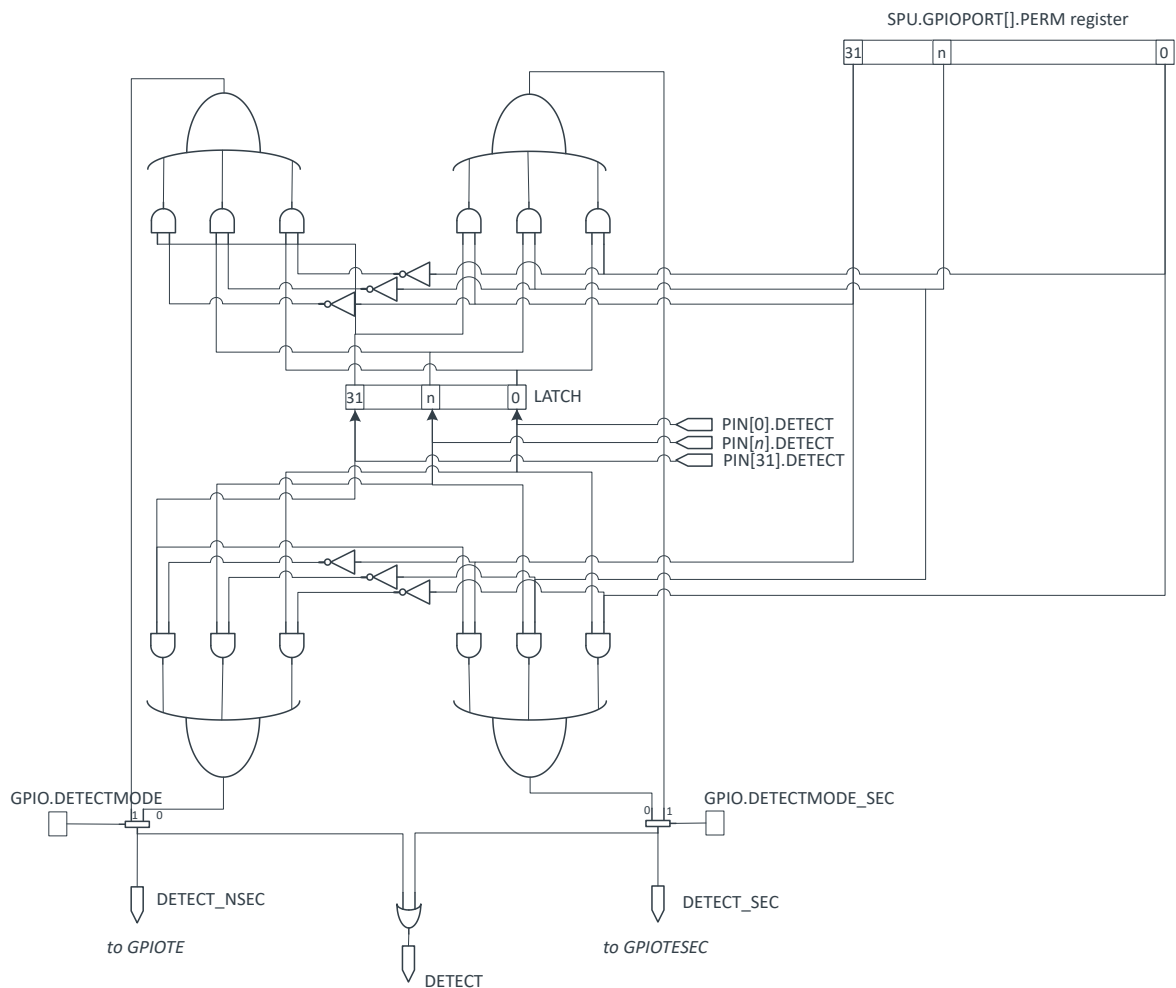


Figure 3. Principle of direct pin access

Registers

| Base address | Peripheral | Instance | Secure mapping | DMA security | Description | Configuration |
|--------------------------|------------|-------------------|----------------|--------------|----------------------------------|---------------|
| 0x50842500 0x40842500 | GPIO | P0 : S P0 : NS | SPLIT | NA | General purpose input and output | |

Table 1. Instances

| Register | Offset | Security | Description |
|--------------------------------|--------|----------|---|
| OUT | 0x004 | | Write GPIO port This register is retained. |
| OUTSET | 0x008 | | Set individual bits in GPIO port |
| OUTCLR | 0x00C | | Clear individual bits in GPIO port |
| IN | 0x010 | | Read GPIO port |
| DIR | 0x014 | | Direction of GPIO pins This register is retained. |
| DIRSET | 0x018 | | DIR set register |
| DIRCLR | 0x01C | | DIR clear register |
| LATCH | 0x020 | | Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers This register is retained. |
| DETECTMODE | 0x024 | | Select between default DETECT signal behavior and LDETECT mode (For non-secure pin only) This register is retained. |
| DETECTMODE_SEC | 0x028 | | Select between default DETECT signal behavior and LDETECT mode (For secure pin only) This register is retained. |
| PIN_CNF[n] | 0x200 | | Configuration of GPIO pins This register is retained. |

Table 2. Register overview

Parent topic: [nRF9160 Product Specification](#)

OUT (Retained)

Address offset: 0x004

Write GPIO port

This register is retained.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|-----|---------------------|----------|-------|----|----|----|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID | R/W | Field | Value ID | Value | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A- f | RW | PIN[i] (i=0..31) | | | | | | Pin i | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Low | 0 | | | | Pin driver is low | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | High | 1 | | | | Pin driver is high | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Parent topic: [nRF9160 Product Specification](#)

OUTSET

Address offset: 0x008

Set individual bits in GPIO port

Note: Read: reads value of OUT register.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| ID | R/W | Field | Value ID | Value | Description |
|----|-----|-----------|----------|-------|---|
| A- | RW | PIN[i] | | | Pin i |
| f | | (i=0..31) | | | |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |
| | | | Set | 1 | Write: writing a '1' sets the pin high; writing a '0' has no effect |

Parent topic: [nRF9160 Product Specification](#)

OUTCLR

Address offset: 0x00C

Clear individual bits in GPIO port

Note: Read: reads value of OUT register.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

| ID | R/W | Field | Value ID | Value | Description |
|----|-----|-----------|----------|-------|--|
| A- | RW | PIN[i] | | | Pin i |
| f | | (i=0..31) | | | |
| | | | Low | 0 | Read: pin driver is low |
| | | | High | 1 | Read: pin driver is high |
| | | | Clear | 1 | Write: writing a '1' sets the pin low; writing a '0' has no effect |

Parent topic: [nRF9160 Product Specification](#)

IN

Address offset: 0x010

Read GPIO port

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| ID | R/W | Field | Value ID | Value | Description |
|----|-----|-------|----------|-------|-------------|
|----|-----|-------|----------|-------|-------------|

| | | | | | |
|----|---|-----------|------|---|-------------------|
| A- | R | PIN[i] | | | Pin i |
| f | | (i=0..31) | | | |
| | | | Low | 0 | Pin input is low |
| | | | High | 1 | Pin input is high |

Parent topic: [nRF9160 Product Specification](#)

DIR (Retained)

Address offset: 0x014

Direction of GPIO pins

This register is retained.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| ID | R/W | Field | Value ID | Value | Description |
|----|-----|-----------|----------|-------|-------------------|
| A- | RW | PIN[i] | | | Pin i |
| f | | (i=0..31) | | | |
| | | | Input | 0 | Pin set as input |
| | | | Output | 1 | Pin set as output |

Parent topic: [nRF9160 Product Specification](#)

DIRSET

Address offset: 0x018

DIR set register

Note: Read: reads value of DIR register.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| ID | R/W | Field | Value ID | Value | Description |
|---------|-----|---------------------|----------|-------|--|
| A- f | RW | PIN[i] (i=0..31) | | | Set as output pin i |
| | | | Input | 0 | Read: pin set as input |
| | | | Output | 1 | Read: pin set as output |
| | | | Set | 1 | Write: writing a '1' sets pin to output; writing a '0' has no effect |

Parent topic: [nRF9160 Product Specification](#)

DIRCLR

Address offset: 0x01C

DIR clear register

Note: Read: reads value of DIR register.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| ID | R/W | Field | Value ID | Value | Description |
|---------|-----|---------------------|----------|-------|---|
| A- f | RW | PIN[i] (i=0..31) | | | Set as input pin i |
| | | | Input | 0 | Read: pin set as input |
| | | | Output | 1 | Read: pin set as output |
| | | | Clear | 1 | Write: writing a '1' sets pin to input; writing a '0' has no effect |

Parent topic: [nRF9160 Product Specification](#)

LATCH (Retained)

Address offset: 0x020

Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers

This register is retained.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| ID | R/W | Field | Value ID | Value | Description |
|---------|-----|---------------------|------------|-------|---|
| A- f | RW | PIN[i] (i=0..31) | | | Status on whether PIN[i] has met criteria set in PIN_CNF[i].SENSE register. Write '1' to clear. |
| | | | NotLatched | 0 | Criteria has not been met |
| | | | Latched | 1 | Criteria has been met |

Parent topic: [nRF9160 Product Specification](#)

DETECTMODE (Retained)

Address offset: 0x024

Select between default DETECT signal behavior and LDETECT mode (For non-secure pin only)

This register is retained.

Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID A
Reset 0x00000000 0

| ID | R/W | Field | Value ID | Value | Description |
|----|-----|------------|----------|-------|--|
| A | RW | DETECTMODE | | | Select between default DETECT signal behavior and LDETECT mode |
| | | | Default | 0 | DETECT directly connected to PIN DETECT signals |
| | | | LDETECT | 1 | Use the latched LDETECT behavior |

Parent topic: [nRF9160 Product Specification](#)

DETECTMODE_SEC (Retained)

Address offset: 0x028

Select between default DETECT signal behavior and LDETECT mode (For secure pin only)

This register is retained.

Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID A
Reset 0x00000000 0

| ID | R/W | Field | Value ID | Value | Description |
|----|-----|------------|----------|-------|--|
| A | RW | DETECTMODE | | | Select between default DETECT signal behavior and LDETECT mode |
| | | | Default | 0 | DETECT directly connected to PIN DETECT signals |
| | | | LDETECT | 1 | Use the latched LDETECT behavior |

Parent topic: [nRF9160 Product Specification](#)

PIN_CNF[n] (n=0..31) (Retained)

Address offset: 0x200 + (n × 0x4)

Configuration of GPIO pins

This register is retained.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|---|-------|----------|-------|--|--|--|--|--|--|--|--|--|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ID | E E D D C C B A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset 0x00000002 | 0 1 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ID | R/W | Field | Value ID | Value | | | | | | | | | | Description | | | | | | | | | | | | | | | | | |

| | | | | | |
|---|----|-------|------------|---|--|
| A | RW | DIR | Input | 0 | Pin direction. Same physical register as DIR register |
| | | | Output | 1 | Configure pin as an input pin |
| | | | | | Configure pin as an output pin |
| B | RW | INPUT | Connect | 0 | Connect or disconnect input buffer |
| | | | Disconnect | 1 | Connect input buffer |
| | | | | | Disconnect input buffer |
| C | RW | PULL | | | Pull configuration |
| | | | Disabled | 0 | No pull |
| | | | Pulldown | 1 | Pull down on pin |
| | | | Pullup | 3 | Pull up on pin |
| D | RW | DRIVE | | | Drive configuration |
| | | | S0S1 | 0 | Standard '0', standard '1' |
| | | | H0S1 | 1 | High drive '0', standard '1' |
| | | | S0H1 | 2 | Standard '0', high drive '1' |
| | | | H0H1 | 3 | High drive '0', high 'drive '1'' |
| | | | D0S1 | 4 | Disconnect '0', standard '1' (normally used for wired-or connections) |
| | | | D0H1 | 5 | Disconnect '0', high drive '1' (normally used for wired-or connections) |
| | | | S0D1 | 6 | Standard '0', disconnect '1' (normally used for wired-and connections) |
| | | | H0D1 | 7 | High drive '0', disconnect '1' (normally used for wired-and connections) |
| E | RW | SENSE | | | Pin sensing mechanism |
| | | | Disabled | 0 | Disabled |
| | | | High | 2 | Sense for high level |
| | | | Low | 3 | Sense for low level |

Parent topic: [nRF9160 Product Specification](#)

Electrical specification

Parent topic: [nRF9160 Product Specification](#)

GPIO Electrical Specification

Note: VDD in the following table refers to VDD_GPIO.

| Symbol | Description | | | | Min. | Typ. | Max. | Units | |
|---------------|--|--|--|--|---------------------|------|---------------------|-------|--|
| V_{IH} | Input high voltage | | | | $0.7 \times V_{DD}$ | | V_{DD} | V | |
| V_{IL} | Input low voltage | | | | V_{SS} | | $0.3 \times V_{DD}$ | V | |
| $V_{OH,SD}$ | Output high voltage, standard drive, 0.5 mA, $V_{DD} \geq 1.7$ V | | | | $V_{DD}-0.4$ | | V_{DD} | V | |
| $V_{OH,HDH}$ | Output high voltage, high drive, 5 mA, $V_{DD} \geq 2.7$ V | | | | $V_{DD}-0.4$ | | V_{DD} | V | |
| $V_{OH,HDL}$ | Output high voltage, high drive, 3 mA, $V_{DD} \geq 1.7$ V | | | | $V_{DD}-0.4$ | | V_{DD} | V | |
| $V_{OL,SD}$ | Output low voltage, standard drive, 0.5 mA, $V_{DD} \geq 1.7$ V | | | | V_{SS} | | $V_{SS}+0.4$ | V | |
| $V_{OL,HDH}$ | Output low voltage, high drive, 5 mA, $V_{DD} \geq 2.7$ V | | | | V_{SS} | | $V_{SS}+0.4$ | V | |
| $V_{OL,HDL}$ | Output low voltage, high drive, 3 mA, $V_{DD} \geq 1.7$ V | | | | V_{SS} | | $V_{SS}+0.4$ | V | |
| $I_{OL,SD}$ | Current at $V_{SS} + 0.4$ V, output set low, standard drive, $V_{DD} \geq 1.7$ V | | | | 1 | 2 | 4 | mA | |
| $I_{OL,HDH}$ | Current at $V_{SS} + 0.4$ V, output set low, high drive, $V_{DD} \geq 2.7$ V | | | | 6 | 10 | 15 | mA | |
| $I_{OL,HDL}$ | Current at $V_{SS} + 0.4$ V, output set low, high drive, $V_{DD} \geq 1.7$ V | | | | 3 | | | mA | |
| $I_{OH,SD}$ | Current at $V_{DD} - 0.4$ V, output set high, standard drive, $V_{DD} \geq 1.7$ | | | | 1 | 2 | 4 | mA | |
| $I_{OH,HDH}$ | Current at $V_{DD} - 0.4$ V, output set high, high drive, $V_{DD} \geq 2.7$ V | | | | 6 | 9 | 14 | mA | |
| $I_{OH,HDL}$ | Current at $V_{DD} - 0.4$ V, output set high, high drive, $V_{DD} \geq 1.7$ V | | | | 3 | | | mA | |
| $t_{RF,15pF}$ | Rise/fall time, standard drive mode, 10 to 90%, 15 pF load ¹ | | | | 6 | 9 | 19 | ns | |
| $t_{RF,25pF}$ | Rise/fall time, standard drive mode, 10 to 90%, 25 pF load ¹ | | | | 10 | 13 | 30 | ns | |
| $t_{RF,50pF}$ | Rise/fall time, standard drive mode, 10 to 90%, 50 pF load ¹ | | | | 18 | 25 | 61 | ns | |

| Symbol | Description | | | | Min. | Typ. | Max. | Units | |
|------------------------------|--|--|--|--|------|------|------|------------|--|
| $t_{\text{HRF},15\text{pF}}$ | Rise/Fall time, high drive mode, 10 to 90%, 15 pF load ¹ | | | | 2 | 4 | 8 | ns | |
| $t_{\text{HRF},25\text{pF}}$ | Rise/Fall time, high drive mode, 10 to 90%, 25 pF load ¹ | | | | 3 | 5 | 11 | ns | |
| $t_{\text{HRF},50\text{pF}}$ | Rise/Fall time, high drive mode, 10 to 90%, 50 pF load ¹ | | | | 5 | 8 | 19 | ns | |
| R_{PU} | Pull-up resistance | | | | 11 | 13 | 16 | k Ω | |
| R_{PD} | Pull-down resistance | | | | 11 | 13 | 16 | k Ω | |
| C_{PAD} | Pad capacitance | | | | | 3 | | pF | |

Parent topic: [nRF9160 Product Specification](#)

¹ Rise and fall times based on simulations