New issue

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A spec from 2019 is on your website with incomplete status all over the place while chips are being sold. #867

Open **TimBandTech** opened this issue on Jul 11 · 1 comment

TimBandTech commented on Jul 11

I can't help but wonder who is stifling the specification process?
To quote you on your own spec:
"To date, no parts of the standard have been officially ratified by the RISC-V Foundation, but the components labeled “frozen” above are not expected to change during the ratification process beyond resolving ambiguities and holes in the specification."

- risc-spec-20191213.pdf

I know several parties that would like to see your project fail.
Engineers are easily spooked.
We've seen far too much vaporware over the years.
Are you working in a half baked system? Is RISC-V for real?
I come in from the sidelines occasionally to review the status of RISC-V and am in no way involved with any RISC-V projects.
I will have to say that at the very least you are not keeping up appearances. I respect that.
Still, let's not forget the selling out of ARM in all of this.
Let's not forget the nature of a project that wants to compete with Intel, AMD, and ARM from an open stance.
Of course I am rooting for this project.
Should it be an FPGA capable design? I think so.
I suspect a mini version of your project was probably the right way to begin.
The business class should insulate investors from engineers at the least.
Where the tech pubs come in; hah!.
Possibly the project is very far along and this manual sits withering on the vine cut short and wounded.
Possibly you are so badly infiltrated that the wrenches coming into the gears from every angle start to make the gears look like wrenches.
Possibly a time to isolate into small competitive groups and go out on branches.
Simply eliminate the broken branches.

jnk0le commented on Jul 11

that text is in "Preface to Document Version 2.2", the newer prefaces are ratified ones. Although some new extensions got frozen/ratified since 2019

Assignees

No one assigned

Labels

None yet

Projects

None yet

Milestone

No milestone

Development

No branches or pull requests

2 participants