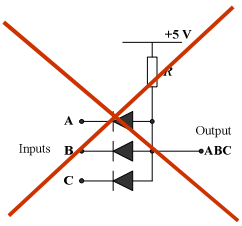
CHAPTER 5

DTL and TTL LOGIC

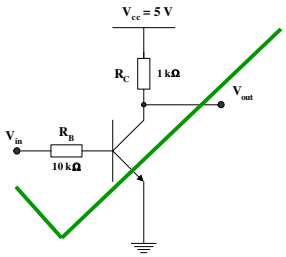
Diode Based Logic

Cannot implement logic using diodes.



Transistor Based Logic

- Can use bipolar transistors



Bipolar Transistor Gate

- Consider a bipolar transistor in logic circuits
  - ⇒ It is operated in either two states
  - ⇒ produces the two logic levels

fully conducting state **saturated/turned on**

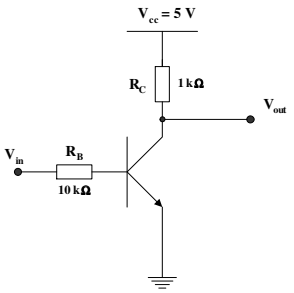
or

fully non-conducting state **cut-off state**

Bipolar Transistor Gate

- **Example 1:** Solve for the simple but very practical logic inverter with

$V_{BE(ON)} = 0.7V$
$V_{BE(SAT)} = 0.8V$
$V_{CE(SAT)} = 0.1V$



Bipolar Transistor Gate

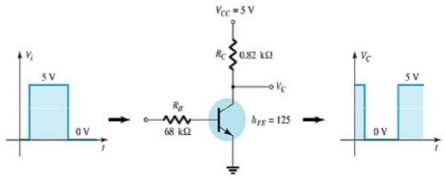
1. Can be calculated that when V_{in} is less than the turn on voltage $V_{BE(ON)}$ for the transistor
   ⇒ collector current will essentially be zero
   ⇒ output voltage $V_{out} = V_{CC}$ *(cutoff)*

2. When the input voltage is increased above $V_{BE(ON)}$
   ⇒ transistor turns ON
   ⇒ enter the forward active region
   ⇒ collector current $I_C = h_{FE}I_B$ (in DC conditions)

3. As input voltage ↑ ⇒ Output voltage ↓
   $V_{out} = V_{CC} - I_C R_C$

Transistor Switching Networks

Transistors with only the DC source applied can be used as electronic switches.



Switching Circuit Calculations

Saturation current:

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

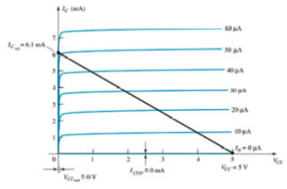
To ensure saturation:

$$I_B > \frac{I_{Csat}}{\beta_{dc}}$$

Emitter-collector resistance at saturation and cutoff:

$$R_{sat} = \frac{V_{CEsat}}{I_{Csat}}$$

$$R_{cutoff} = \frac{V_{CC}}{I_{CEO}}$$



Solution for Example 1:

- For the given network, when V_i = 5V, the resulting level of I_B is

$$I_B = \frac{V_i - 0.7\text{V}}{R_B} = \frac{5\text{V} - 0.7\text{V}}{68k\Omega} = 63\mu\text{A}$$

- and $$I_{Csat} = \frac{V_{CC}}{R_C} = \frac{5\text{V}}{0.82k\Omega} \cong 6.1\text{mA}$$

- Testing the saturation condition gives

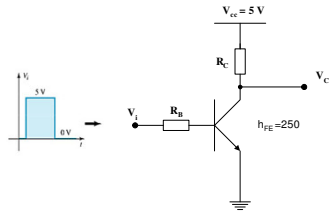
$$I_B = 63\mu\text{A} > \frac{I_{Csat}}{\beta_{dc}} = \frac{6.1\text{mA}}{125} = 48.8\mu\text{A}$$

- which is satisfied. Certainly, any level of I_B greater than 60μA will pass through a *Q*-point on the load line that is very close to the vertical axis.

- When the transistor is in the saturation region, we will assume that $V_{CE} = V_{CE_{sat}} = 0\text{V}$ rather than the typical 0.1- to 0.3-V level.
- For V_i = 0V, I_B = 0μA, and because we are assuming that $I_C = I_{CEO}$ = 0mA, the voltage drop across R_C as determined by $V_{R_C} = I_C R_C$ = 0V, resulting in V_C = +5V for the response as indicated in the given figure above.

Example 2:

Determine R_B and R_C for the transistor inverter for the given figure if I_{Csat}= 10mA.



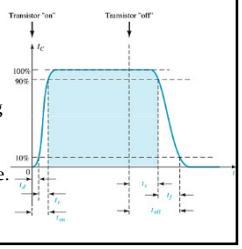
Switching Time

There are transistors that are referred to as *switching transistors* due to the speed with which they can switch from one voltage level to the other. In the figure below the periods of time defined as t_s, t_d, t_r, and t_f are provided versus collector current. Their impact on the speed of response of the collector output is defined by the collector current response given in the figure.

The total time required for the transistor to switch from the "off" the "on" state is designated as t_{on} and is defined by

$$\mathbf{t_{on} = t_r + t_d}$$

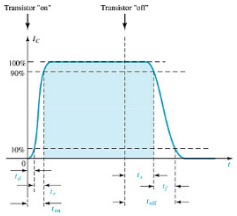
with t_d the delay time between the changing state of the input and the beginning of a response at the output. The time element t_r is the rise from 10% to 90% of the final value.



The total time required for the transistor to switch from the "on" the "off" state is designated as t_{off} and is defined by

$$t_{off} = t_s + t_f$$

where t_s is the storage time and t_f the fall time from 90% to 10% of the initial state.



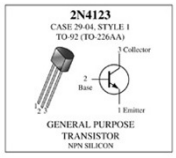
Transistor Specification Sheet

MAXIMUM RATINGS

Rating	Symbol	2N4123	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W



- For the general-purpose transistor 2N4123 at I_C = 10mA, we find that
  - t_s = 120ns
  - t_d = 25ns
  - t_r = 13ns
  - t_f = 12ns

so that

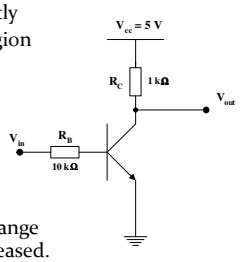
- $t_{on} = t_r + t_d$ = 13ns + 25ns = **38ns**
- $t_{off} = t_s + t_f$ = 120ns + 12ns = **132ns**

- Comparing the values above with the following parameters of a BSV52L switching transistor reveals one of the reasons for choosing a switching transistor when the need arises:
  - t_{on} = **12ns** and t_{off} = **18ns**

Bipolar Transistor Gate

With sufficient input voltage

- output voltage has fallen sufficiently
- transistor enters the saturation region

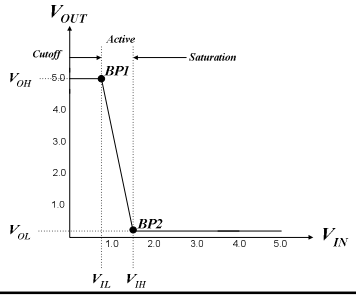


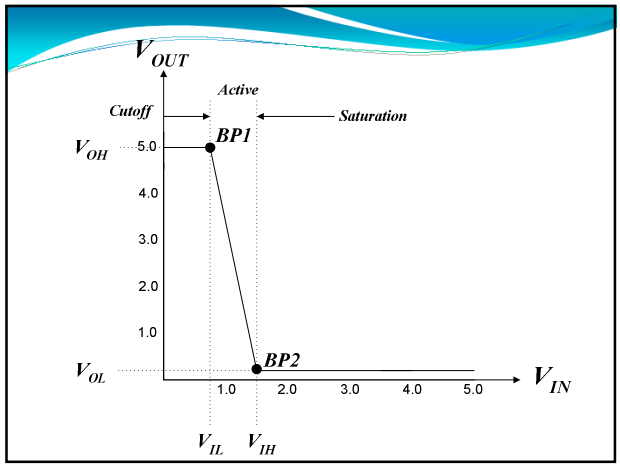
When in the saturation region

- output voltage shows very little change as the input voltage is further increased.

Voltage Transfer Characteristic

- One of the principal properties of interest in any digital circuit is the voltage-transfer characteristic.
  - relates the output voltage to the input voltage under steady-state or low frequency conditions.





Voltage Transfer Characteristic

At Breakpoint 1 (BP1)

- input voltage is just at the point of turning on the transistor

But

- output voltage is still very close to the cut-off value
  - collector current very small

At Breakpoint 2 (BP2)

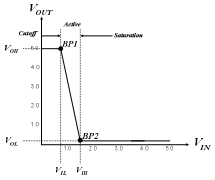
- input voltage sufficient so that the transistor is at the edge of saturation region

- collector current nearly at **maximum** value
  - since any further increase in the input voltage results in hardly any change the output voltage.

Voltage Transfer Characteristic

- These breakpoints separate the following 3 regions of operation
  - Cut-off, Active and Saturation

The co-ordinates of BP1 and BP2 are



BP1	V_{IL}, V_{OH}
BP2	V_{IH}, V_{OL}

V_{IL} input low voltage
MAX value of V_{IN} to guarantee that $V_{OUT} = V_{OH}$

V_{IH} input high voltage
MIN value of V_{IN} to guarantee that $V_{OUT} = V_{OL}$

Voltage Transfer Characteristic

- **Example 3:** Obtain numeric values for these quantities from circuit analysis.

$V_{BE(ON)} = 0.7$ V
$V_{BE(SAT)} = 0.8$ V
$V_{CE(SAT)} = 0.1$ V

1. V_{OH} is equivalent to V_{CE} with the transistor at edge of cut-off region, i.e. V_{CC}

$$\mathbf{V_{OH} = V_{CC}}$$

2. V_{OL} is equivalent to V_{CE} with transistor at the edge of saturation region. i.e. $V_{CE(SAT)}$

here in this example $V_{CE(SAT)} = 0.1$ V

$$\Rightarrow \quad \mathbf{V_{OL} = V_{CE(SAT)}}$$

Voltage Transfer Characteristic

3. V_{IL} which is the input voltage just sufficient to turn on the transistor.

In this example $V_{BE(ON)} = 0.7$ V

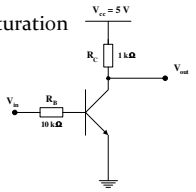
$$\Rightarrow \quad \mathbf{V_{IL} = V_{BE(ON)}}$$

4. V_{IH} is the input voltage just sufficient to saturate the transistor

With the transistor just at the edge of saturation

$$\Rightarrow \quad I_C = I_{CEO}$$

$$I_{CEO} = \frac{V_{CC} - V_{CE(SAT)}}{R_C}$$



Voltage Transfer Characteristic

But also at the edge of the active region

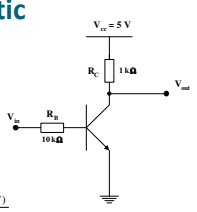
$$\Rightarrow \quad I_{CEO} = h_{FE} I_{BEO}$$

Thus where the input is V_{IH}

$$\Rightarrow \quad I_{BEO} = \frac{V_{IH} - V_{BE(SAT)}}{R_B}$$

$$V_{IH} = V_{BE(SAT)} + \frac{R_B}{R_C} \cdot \frac{V_{CC} - V_{CE(SAT)}}{h_{FE}}$$

$$V_{IH} = 0.8 + \frac{10k\Omega}{1k\Omega} \cdot \frac{5 - 0.1}{70} = 1.5V$$



$\Rightarrow$ BP1 co-ordinates are $V_{IN} = 0.7$ V and $V_{OUT} = 5.0$ V
$\Rightarrow$ BP2 co-ordinates are $V_{IN} = 1.5$ V and $V_{OUT} = 0.1$ V

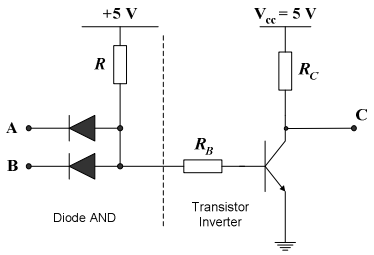
Bipolar Digital Gate Circuits

- The first forms of the digital ICs to receive general usage were BJT inverter circuits in earlier 1960s.
  - Circuits consisted of only resistors and transistors,
  - named ***resistor-transistor logic (RTL)***.
- IC development a short time later consisted of a diode AND circuit followed a bipolar transistor inverter.
  - termed ***diode-transistor logic (DTL)***

Diode Transistor Logic

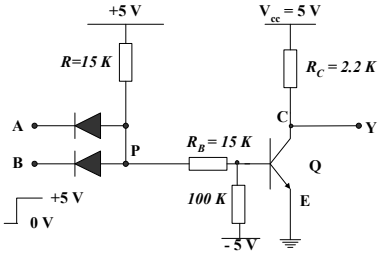
A diode AND network can be merged with an inverter

- Forms a diode-transistor NAND gate



Example 4

- (a) Verify that the circuit shown below is a NAND gate for the binary levels 0 and +5V. Neglect source impedance and junction saturation voltages and diode voltages in the forward direction. Find the minimum h_{FE}. (b) If the drop across a conducting diode is 0.7V and if the sum of source and diode resistances is 1 kΩ, is the NAND logic satisfied? (c) Will the circuit operate properly if the inputs are obtained from the outputs of similar NAND gates? Assume silicon transistors and diodes and neglect collector saturation resistance and diode forward resistance.



Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Solution

- (a) If any inputs is at 0V, then the junction point *P* of the diodes is at 0V, because a diode conducts and clamps this point to V(0) = 0. The base voltage of the transistor is then

$$V_B = -(5\text{V})\frac{15k\Omega}{115k\Omega} = -0.652\text{V}$$

- Hence *Q* is cutoff and *Y* is at 5V, or *Y* = 1. This result confirms the first three rows of the truth table.
- If all the inputs are at V(1) = 5V, assume that all diodes are reverse biased and that the transistor is in saturation. We shall now verify that these assumptions are indeed correct. If *Q* is in saturation, then with V_{BE} = 0, the voltage at *P* is (5V)(15K/30K)= 2.5V. Hence with 5V at each input, all diodes are reverse-biased by 2.5V. Since the diodes are nonconducting, the two 15K resistors are in series and the base current of *Q* is

$$\frac{5V}{30k\Omega} - \frac{5V}{100k\Omega} = 0.17\text{mA} - 0.05\text{mA} = 0.12\text{mA}$$

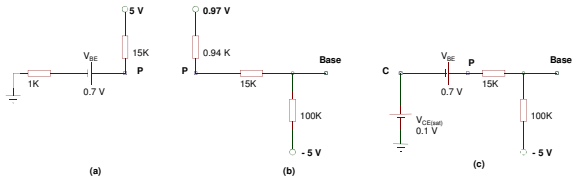
- Since the collector current is

$$I_C = \frac{5\text{V}}{2.2k\Omega} = 2.27\text{mA} \quad \text{and} \quad (h_{FE})_{\min} = \frac{2.27\text{mA}}{0.12\text{mA}} = 19$$

- then *Q* will be indeed in saturation if $h_{FE} \geq 19$. Under these circumstances the output is at ground, or *Y*=0. This result confirms the last row of the truth table.
- (b) The transistor must be OFF if at least one input is at 0. The worst case occurs when all diodes except one are reverse-biased, because then the voltage at P is

$$(5\text{V})\left(\frac{1k\Omega}{16k\Omega}\right) + (0.7\text{V})\left(\frac{15k\Omega}{16k\Omega}\right) = 0.3125 + 0.65625 \cong 0.97\text{V}$$

in series with a resistance of (1×15)/16 = 0.94kΩ. The open-circuit voltage at the base of the transistor is, from Fig.(b),



$$V_B = -(5\text{V})\left(\frac{15.94k\Omega}{115.94k\Omega}\right) + (0.97\text{V})\left(\frac{100k\Omega}{115.94k\Omega}\right) \cong -0.15\text{V}$$

This voltage is more than adequate to reverse-bias Q, and hence NAND logic is satisfied.

- (c) If the inputs are HIGH, the situation is exactly as in part a. With respect to keeping the base node at a low voltage when there is no coincidence, the worst situation occurs when all but one input are HIGH. The LOW input now comes from a transistor in saturation, and $V_{CE,sat} \approx 0.1\text{V}$. The open-circuit voltage at the base of Q is, from Fig. (c),

$$V_B = -(5\text{V})\left(\frac{15k\Omega}{115k\Omega}\right) + (0.8\text{V})\left(\frac{100k\Omega}{115k\Omega}\right) \cong -0.044\text{V}$$

which cuts off Q and Y = 1, as it should.

Bipolar Digital Gate Circuits

- Choice of logic family for design of a specific digital system is influenced by many factors.
  - Need for low power
  - High speed
  - Availability of more complex functions (MSI)
  - Compatibility with other parts of the system
  - Cost
- Many system designs mix logic families
  - e.g. TTL and CMOS

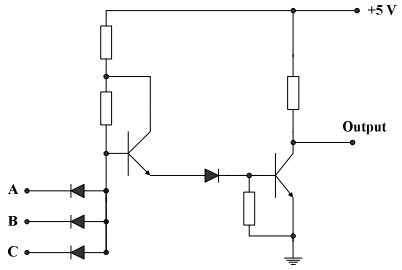
Development of bipolar digital IC has been evolutionary rather than revolutionary.

TTL

- In the mid – late 1960's use of resistors, diodes and transistors began to disappear
  - Discrete components phased out due to new fabrication processes
  - Processes where entire circuits could be made onto one chip
- The first to appear were small scale integration SSI
  - 1 to 10 gates or memory elements packaged as a unit
  - packaged as DIL package
- MSI medium scale integration
  - 10 to 100 gates or memory elements packaged as a unit
- LSI large scale integration
  - 100 to 10000 gates or memory elements packaged as a unit
- For MSI and LSI the popular logic family is TTL

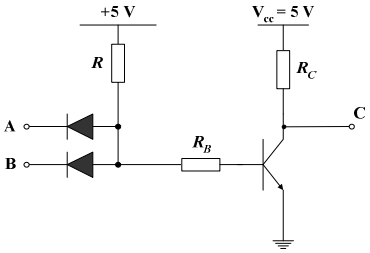
Integrated DTL NAND

- Can introduce TTL by relating it to the DTL family.
- The integrated version of the DTL NAND :



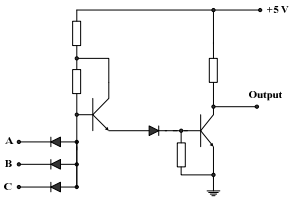
DTL NAND

- Compare with the original circuit.



DTL

- The extra transistor adds amplification to increase fan-out
  - kept in the **active region** when output transistor is saturated
- Modified circuit can supply large amount of base current to the output transistor.
  - Thus output transistor can now draw a large amount of collector current before it goes out of saturation.

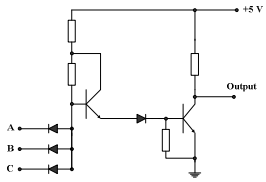


DTL

- Part of the collector current comes from the conducting diodes in the loading gates (when the output transistor is saturated).

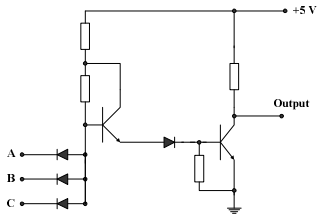
  ⇒ an increase in allowable collector saturated current allows more loads to be connected to the output.

  ⇒ increase fan-out capability.



DTL

- Extra **diode** is used to provide biasing for output transistor
  - Avoids use of resistors
  - and also the need for separate negative power supply



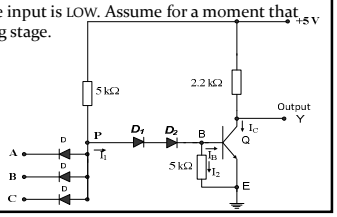
Example 5

(a) For the transistor in the figure assume that $V_{BE(SAT)}$ = 0.8 V, V_y = 0.5 V, and $V_{CE(SAT)}$ = 0.2 V. The drop across a conducting diode is 0.7 V and V_y (diode) = 0.6 V. The inputs of this switch are obtained from the outputs of similar gates. Verify that the circuit functions as a positive NAND and calculate $h_{FE(min)}$.

(b) Will the circuit operate properly if D_2 is not used?

(c) If all inputs are HIGH, what is the magnitude of the noise voltage at the input which will cause the gate to malfunction?

(d) Repeat part (c) if at least one input is LOW. Assume for a moment that Q is not loaded by a following stage.



Solution

- (a) The logic levels are $V_{CE(SAT)}$ = 0.2 V for the 0 state and V_{CC} = 5 V for the 1 state. If at least one input is in the 0 state, its diode conducts and V_P = 0.2 + 0.7 = 0.9 V. Since, in order for D_1 and D_2 to be conducting, a voltage of 2×0.7V = 1.4V is required, these diodes are cutoff, and V_{BE} = 0 V. Since the cutin voltage of Q is V_y = 0.5 V, the Q is OFF, the output rises to 5 V, and Y = 1. This confirms the first three rows of the NAND truth table.
- If all inputs are at $V(1)$ = 5 V, then we shall assume that all input diodes are OFF, that D_1 and D_2 conduct, and that Q is in saturation. If these conditions are true, the voltage at P is the sum of the two diode drops plus $V_{BE(SAT)}$, or V_P = 0.7 + 0.7 + 0.8 = 2.2 V. The voltage across each input diode is 5 - 2.2 = 2.8 V in the reverse direction, thus justifying the assumption that D is OFF. We now find $h_{FE(min)}$ to put Q into saturation.

$$I_1 = \frac{V_{CC} - V_P}{5k\Omega} = \frac{(5-2.2)V}{5k\Omega} = 0.56\ mA$$

$$I_2 = \frac{V_{BEsat}}{5k\Omega} = \frac{0.8V}{5k\Omega} = 0.16\ mA$$

$$I_B = I_1 - I_2 = 0.56 - 0.16 = 0.40\ mA$$

$$I_C = \frac{V_{CC} - V_{CEsat}}{2.2k\Omega} = \frac{(5-0.2)V}{2.2k\Omega} = 2.18\ mA$$

and

$$h_{FE(min)} = \frac{I_C}{I_B} = \frac{2.18\ mA}{0.40\ mA} = 5.5$$

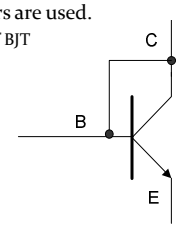
- If $h_{FE} > h_{FE(min)}$, then $Y = V(0)$ for all inputs at $V(1)$, thus verifying the last line in the truth table.
- (b) If at least one input is at $V(0)$, then V_P = 0.2 + 0.7 = 0.9 V. Hence, if only one diode D_1 is used between P and B, then V_{BE} = 0.9 - 0.6 = 0.3 V, where 0.6 V represent the diode cutin voltage. Since the cutin base voltage is V_y = 0.5 V, then theoretically Q is cut off. However, this is not a conservative design because a small (> 0.2 V) spike of noise will turn Q ON. An even more conservative design uses three diodes in series, instead of the two indicated in the given figure.

- (c) If all inputs are HIGH, then from part (a), $V_P = 2.2$ V and each input diode is reverse-biased by 2.8 V. A diode starts to conduct when it is forward-biased by 0.6 V. Hence a negative noise spike in excess of 2.8 + 0.6 = 3.4 V must be present at the input before the circuit malfunctions. Such a large noise voltage is improbable.

- (d) If at least one input is LOW, then from part (a), $V_P = 0.9$ V and Q is OFF. If a noise spike takes Q just into its active region, $V_{BE} = V_\gamma = 0.5$ V and V_P must increase to 0.5 + 0.6 + 0.6 = 1.7 V. Hence the noise margin is 1.7 – 0.9 = 0.8 V. If only one diode D_1 were used, the noise voltage would be reduced by 0.6 V (the drop across D_2 at cutin) to 0.8 – 0.6 = 0.2 V. This confirms the value obtained in part (b).

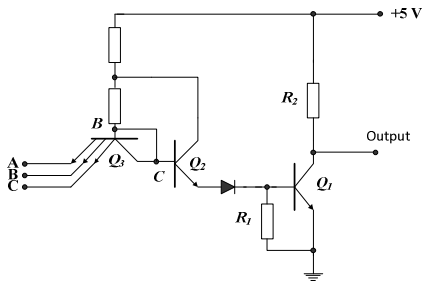
DTL → TTL

- The first change from DTL to TTL:
  - In IC's it is easier to fabricate transistors than diodes.
  - When diodes are required, transistors are used.
    - ⇒ Usual to use the base-emitter junction of BJT
    - ∴ base serving as the anode
    - ∴ emitter serving as the cathode
    - ∴ collector tied to the base



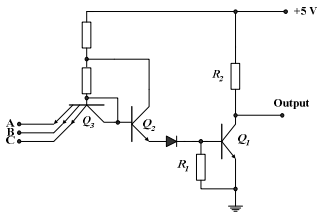
TTL: Multi-Emitter Transistor

- Note anodes of the input diodes are common
  - Thus can be realised in the form of a multiple-emitter transistor



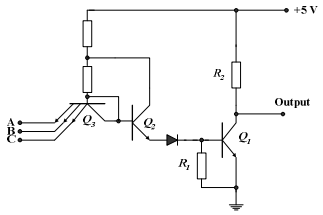
TTL : Increase Switching Speed

- The remaining changes in the evolution from DTL to TTL made to achieve increased speed.
- When circuit is to switch from a LOW-output to a HIGH-output state,
  - Q_1 must go from ***saturation to cut-off***
  - Requires removal of charge from base of Q_1



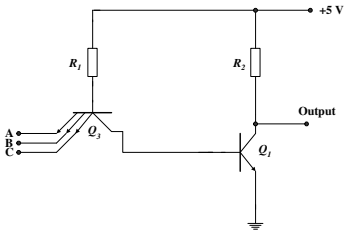
TTL : Increase Switching Speed

- Therefore this switching action is brought about by Q_2
  - Q_2 going from ***saturation to cut-off***
- The only path for discharging the base of Q_1 is through resistor R_1.
- Speed of discharge is limited by time constant of circuit.



TTL: Faster Switching

- To obtain faster switching
  - Take advantage of input diodes being realised in terms of transistors
  - change the circuit to the following



- Now the charge on the base of Q_1 is removed through transistor Q_3
  - Results in a considerable reduction in the saturation delay time t_s.

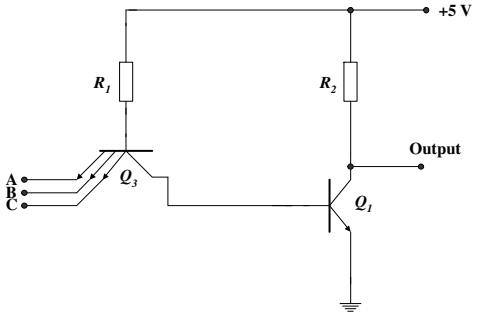
TTL : Collector Capacitance

- Another factor limiting transition speed is the **collector capacitance** which is called the capacitive load, consisting of the capacitances of the reverse-biased diodes of the fan-out gates and any stray wiring capacitance.
  - Must be charged as output voltage switches from LOW to HIGH value (i.e. output changes from ***saturation to cutoff***)
  - only path for charging capacitance is via the collector resistor R_2
  - Can reduce value of R_2
  - ⇒ increases charging speed

but also increases power dissipation

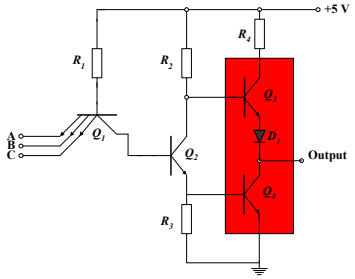
- Output circuit of this form known as ***passive pull-up circuit***.
  - Output capacitance is "pulled-up" via passive element R_2.

Passive Pull up Circuit



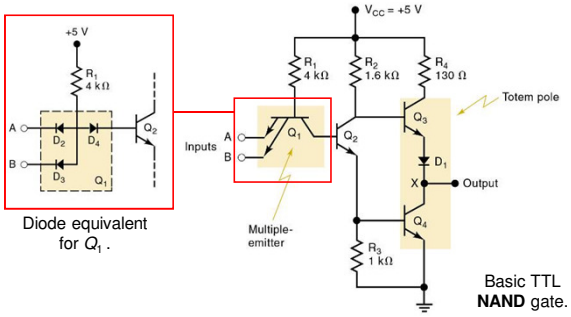
TTL: Active Pull Up Circuit

- An alternative which provides faster charging **without** increased power dissipation is
  - the ***active pull-up circuit***.



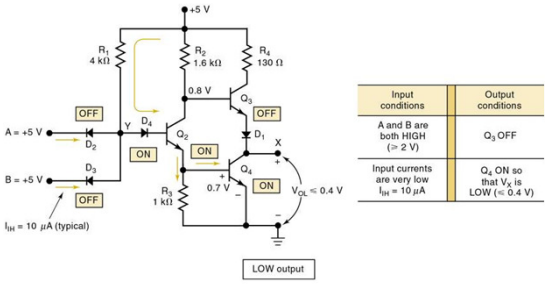
The TTL Logic Family

The basic TTL logic circuit is the NAND gate.



The TTL Logic Family

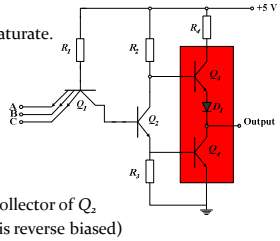
TTL NAND gate LOW output



Input conditions	Output conditions
A and B are both HIGH (≥ 2 V)	Q_3 OFF
Input currents are very low I_{IH} = 10 μA	Q_4 ON so that V_X is LOW (≤ 0.4 V)

NAND Gate Output Low condition

- The phase splitter transistor Q_2 is in saturation
- The saturation current through R_3 is large enough to cause positive voltage drop
  - ⇒ This positive voltage causes Q_4 to saturate.



- Base of Q_3 is at 0.8 V
  - due to V_{BE} of Q_4 at 0.7 V
  - and V_{CE} of Q_2 at 0.1 V
- Because of D_1,
  - emitter of Q_3 is more positive than collector of Q_2
  - ⇒ Q_3 is off (i.e. base-emitter junction is reverse biased)

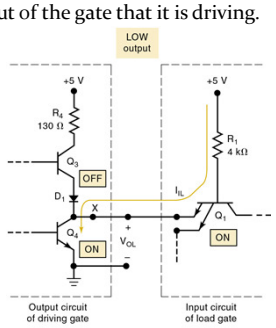
D_1 is in the circuit to ensure that Q_3 is cut-off when Q_4 is saturated.

NAND Gate Output Low condition

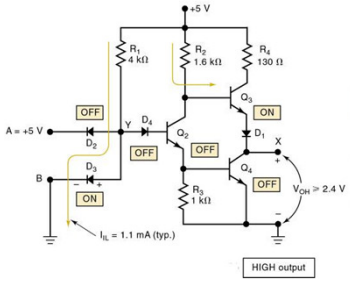
- A TTL output acts as a current sink in the LOW state because it *receives* current from the input of the gate that it is driving.

Transistor Q_4 of the driving gate is ON and essentially "shorts" point *X* to ground. Q_4 performs a **current-sinking** action and is called the **pull-down transistor.**

LOW voltage at *X* forward-biases the emitter–base junction of Q_1 & current flows back through Q_4.



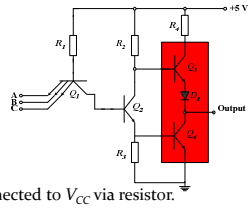
TTL NAND gate HIGH output



Input conditions	Output conditions
A or B or both are LOW (≤ 0.8 V)	Q_4 OFF
Current flows back to ground through LOW input terminal. I_{IL} = 1.1 mA	Q_3 acts as emitter-follower and $V_{OH} \geq 2.4$ V, typically 3.6 V

NAND Gate Output High condition

- Output HIGH due to one of the inputs dropping LOW
  ⇒ Q_2 and Q_4 go into cut-off
- However output remains momentarily low
  - as voltage across load capacitance cannot change instantaneously



- As soon as Q_2 turns off
  ⇒ Q_3conducts as its base is connected to V_{CC} via resistor.
- Current needed to charge load capacitance causes Q_3 to momentarily saturate
  ⇒ output voltage rises with a time constant RC

NAND Gate Output High condition

- But as the resistance *R* is typically :

Collector resistance of 130Ω +
resistance of the diode + saturation resistance of Q_3 = 150Ω

- The value of *R* is << passive pull-up resistance used in the open collector circuit

Transition from Low to High is much faster

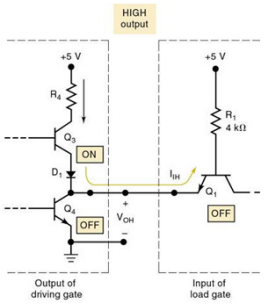
NAND Gate Output High condition

- A TTL output acts as a current source in the HIGH state—a small reverse-bias leakage current.

Transistor Q_3 is supplying the input current (I_{IH}) required by Q_1 of the load gate.

Q_3 is often called the **current-sourcing** or **pull-up transistor**.

In more modern TTL series, the pull-up circuit is made up of two transistors.



NAND Gate Input and Output Conditions (Short Summary)

- V_{OH}, V_{OL}

  V_{CC} = **+5 V** but due to voltage drops in the output circuit

  ⇒ V_{OL} = **0.2 V** (V_{CE} of Q_4)

  ⇒ V_{OH} = **3.6 V** (V_{CC}- (V_{BE} of Q_3 +D_1))

Speed

- standard TTL is 3 times faster than DTL

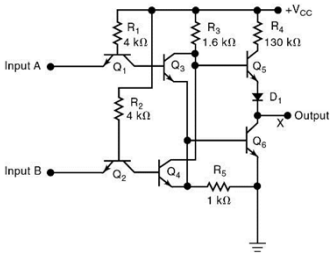
Fan-out

- 8-10

NOTE

- HIGH inputs at A, B and C will have to supply a small diode leakage current , I_{IH} = 10 µA
- If one or more inputs are LOW, substantial current will flow through input terminal to ground, I_{IL} = 1 mA

Internal circuit for a TTL NOR gate.



- The **NOR** circuit does *not* use a multiple-emitter transistor.
- Each input is applied to the emitter of a separate transistor.
- The **NOR** circuit uses the same totem-pole arrangement as the **NAND** circuit on the output side

The TTL Logic Family (Brief Review)

- Most TTL circuits have a similar structure
  - **NAND** and **AND** gates use multiple-emitter transistor or multiple diode junction inputs.
  - **NOR** and **OR** gates use separate input transistors.
- The input will be the cathode of a P-N junction
  - A HIGH input will turn off the junction.
    - Only a leakage current is generated.
  - A LOW input turns on the junction.
    - Relatively large current is generated.
- Most TTL circuits have some type of totem-pole output configuration.

Advantages of the Totem Pole Output Stage

1. Same output could be generated without Q_3 and D_1 and connecting resistor to collector of Q_4.

However

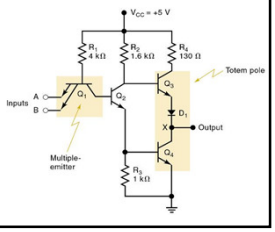
$\Rightarrow Q_4$ would conduct a fairly large current in saturation state

$$\frac{+5\text{ V}}{\text{Collector Resistance}} = \frac{5\text{V}}{130\Omega} \approx 40\text{mA}$$

with Q_3 in circuit

$\Rightarrow$ no current through collector resistance in LOW state

$\Rightarrow$ keeps power dissipation in circuit low.



Advantages of the Totem Pole Output Stage

2. In the HIGH state

- Q_3 acts as an emitter follower (i.e. common collector configuration) with associated low o/p impedance (10 Ω).
- **Note:** Input impedance R_i of an emitter follower is very high – hundreds of kΩ's – and the o/p resistance R_o is very low – tens of ohms.
- Provides a short time constant for charging capacitive load on the output.
- This action, known as active pull-up provides faster switching times.

Disadvantages of the Totem Pole Output Stage

In transition from LOW – HIGH output state

- Q_4 turns off much faster than Q_3 turns on

$\Rightarrow$ for a few nanoseconds **BOTH** conduct.

- relatively high current 30 –40 mA will be drawn from supply.
- current spike generates noise on power supply distribution line
- if change in state is frequent (fast switching)

$\Rightarrow$ power dissipation increases.

Digital Integrated Circuits (ICs)

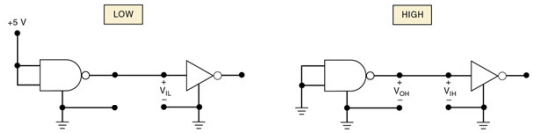
- Digital IC technology has advanced rapidly from integrations which can consist of 1 million or more gates.
- ICs pack more circuitry in a small package, so overall size of almost any system is reduced.
  - Cost is reduced because of the economies of mass-producing large volumes of similar devices.
- ICs have made digital systems more reliable by reducing the number of external interconnections from one device to another.
  - Protected from poor soldering, breaks or shorts in connecting paths on a circuit board, and other physical problems.

- ICs cannot handle very large currents or voltage.
  - Heat generated in such small spaces would cause temperatures to rise beyond acceptable limits.
    - For higher power levels, an interfacing circuit will be needed—typically of components or special power ICs.
- ICs can't easily implement certain devices such as inductors, transformers, and large capacitors.
  - Principally used to perform low-power circuit operations—commonly called *information processing*.
- Various logic families differ in major components in their circuitry.
  - TTL and ECL use *bipolar* transistors as their major circuit element.
  - PMOS, NMOS, and CMOS use unipolar MOSFET transistors.

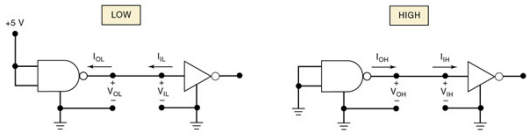
Digital IC Terminology

IC nomenclature & terminology is fairly standardized.

- V_{IH}**(min)—High-Level Input Voltage.** The minimum voltage level required for a logical 1 at an *input*. Any voltage below this level will not be accepted as a HIGH by the logic circuit.
- V_{IL}**(max)—Low-Level Input Voltage.** The maximum voltage level required for a logic 0 at an *input*. Any voltage above this level will not be accepted as a LOW by the logic circuit.
- V_{OH}**(min)—High-Level Output Voltage.** The minimum voltage level at a logic circuit *output* in the logical 1 state under defined load conditions.



Digital IC Terminology

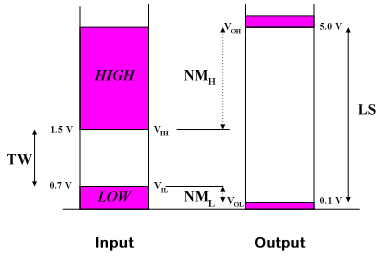


- V_{OL}**(max)—Low-Level Output Voltage.** The maximum voltage level at a logic circuit *output* in the logical 0 state under defined load conditions.
- I_{IH}**—High-Level Input Current.** The current that flows into an input when a specified high-level voltage is applied to that input.
- I_{IL}**—Low-Level Input Current.** The current that flows into an input when a specified low-level voltage is applied to that input.
- I_{OH}**—High-Level Output Current.** The current that flows from an output in the logical 1 state under specified load conditions.
- I_{OL}**—Low-Level Output Current.** The current that flows from an output in the logical 0 state under specified load conditions.

Digital IC Terminology

Logic Levels

Positive Logic



Digital IC Terminology

- Between the two levels (V_{IL} and V_{IH}) the transistor is in the active region,
  - output level is not uniquely determined
  - where because of the loose control on the transistor parameters.

Hence this is a forbidden region $V_{IH} - V_{IL}$

The difference between V_{IH} and V_{IL} is the ***Transition Width***.

$$TW = V_{IH} - V_{IL}$$
$$= 1.5 - 0.7$$
$$= 0.8\,V$$

- ***Logic Swing*** is defined as the difference between the two output voltage levels

$$LS = V_{OH} - V_{OL}$$
$$= 5.0 - 0.1$$
$$= 4.9\,V$$

Digital IC Terminology – Noise

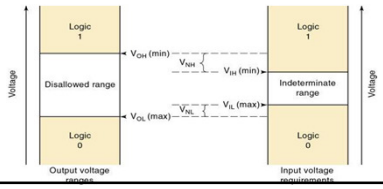
- Stray electric/magnetic fields can induce voltages on the connecting wires between logic circuits
  - Called *noise*, these unwanted, spurious signals can sometimes cause unpredictable operation.
- **Noise immunity** refers to the circuit's ability to tolerate noise without changes in output voltage.
  - A quantitative measure is called **noise margin**.

High-state noise margin:

$V_{NH} = V_{OH}(\text{min}) - V_{IH}(\text{min})$
$= 2.4\text{ V} - 2.0\text{ V} = 0.4\text{ V}$

Low-state noise margin:

$V_{NL} = V_{IL}(\text{max}) - V_{OL}(\text{max})$
$= 0.7\text{ V} - 0.1\text{V} = 0.6\text{ V}$



Digital IC Terminology - Noise

- ***Noise Margins for the inverter circuit we have analyzed previously are:***

$$NM_H = V_{OH} - V_{IH}$$
$$= 5.0 - 1.5$$
$$= 3.5\,V$$

$$NM_L = V_{IL} - V_{OL}$$
$$= 0.7 - 0.1$$
$$= 0.6\,V$$

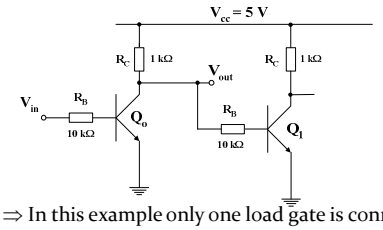
Digital IC Terminology – Fan In

- Fan-in is a term that defines the maximum number of digital inputs that a single logic gate can accept. Most transistor-transistor logic (TTL) gates have one or two inputs, although some have more than two. A typical logic gate has a fan-in of 1 or 2.
- In some digital systems, it is necessary for a single TTL logic gate to drive several devices with fan-in numbers greater than 1. If the total number of inputs a transistor-transistor logic (TTL) device must drive is greater than 10, a device called a buffer can be used between the TTL gate output and the inputs of the devices it must drive. (A buffer is a logic gate used as a signal amplifier.) A logical inverter (also called a NOT gate) can serve this function in most digital circuits.

Digital IC Terminology – Fan Out

- A logic-circuit output is generally required to drive several logic inputs.
  - Sometimes all ICs are from the same logic family.
    - But many systems have a mix of various logic families.
  - The **fan-out**—*loading factor*—is the *maximum* number of logic inputs an output can drive reliably.

Example 6: Fan Out



⇒ In this example only one load gate is connected.

⇒ The fan out from the driver Q_o is 1.

- Noted that V_{OH} for the individual inverter is V_{CC}=+5V and the High noise margin NM_H=3.5V.
  - In all of these discussions the load was zero

Fan Out

Now the load is 1.

- V_{OH} at V_{OUT} is due to voltage divider action of R_C and R_B.

$$V_{OH} = V_{BE(SAT)} + \frac{R_B}{R_C + R_B}\left(V_{CC} - V_{BE(SAT)}\right) \qquad \text{Eqn. 1}$$

$$= 0.8 + \frac{10}{1+10}(5.0 - 0.8)$$

$$= 4.6\text{V}$$

This is due to the application of one load gate

⇒ V_{OH} has been reduced from 5.0V to 4.6V.

Consequently NM_H is also reduced to

$$\Rightarrow \quad NM_H = V_{OH} - V_{IH}$$

$$= 4.6 - 1.5$$

$$= 3.1\text{V}$$

Fan Out

- Thus, the question becomes:
- *What is the maximum number of load gates that can connected to the output F ?*
  - *What is maximum Fan-out ?*

The answer found from finding the limit when NM_H=0.

$$NM_H = 0$$

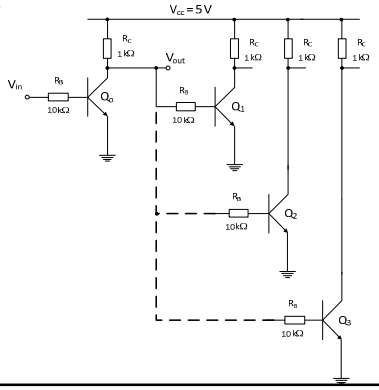
$$\Rightarrow V_{OH} = V_{IH} \qquad \text{Eqn. 2}$$

Note from the circuit, that when:

Q_o is OFF and with a load of N gates connected

- There are N base resistors R_B
- All effectively connected in parallel to $V_{BE(SAT)}$

Fan Out



Fan Out

- Change Eqn. 1 to take account of N load gates and then combining it with Eqn. 2.

  $\Rightarrow$ Solving for N in this quantity, we have the maximum number of load gates

$$V_{BE(SAT)} + \frac{R_B/N}{R_C + R_B/N}\left(V_{CC} - V_{BE(SAT)}\right) = V_{BE(SAT)} + \frac{R_B}{R_C}\left(\frac{V_{CC} - V_{CE(SAT)}}{h_{FE}}\right)$$

$$N \le h_{FE}\frac{V_{CC} - V_{BE(SAT)}}{V_{CC} - V_{CE(SAT)}} - \frac{R_B}{R_C}$$

Fan Out

- Using the numeric values

$$N \le 70\frac{5 - 0.8}{5 - 0.1} - \frac{10}{1}$$
$$= 50$$

- Since a fractional gate load is impractical

  $\Rightarrow$ All fan-out problems we conservatively round down

  $\Rightarrow$ 53.8 $\rightarrow$ 50

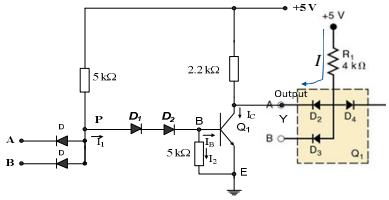
- Since NM_H =0 this gives the absolute maximum number of load gates for the fan-out
- One could also solve this problem by letting NM_H=NM_L

Fan-out Determination Hints

- Fan-out refers to the load drive capability of an IC output
  - A TTL output has a limit on how much current it can sink in the LOW state, or source in the HIGH state.
  - Exceeding these currents will result in output voltage levels outside specified ranges.
- **Determining fan out**
  - Add the I_{IH} for all inputs connected to an output.
    - Sum must be *less* than the output I_{OH} specification.
  - Add the I_{IL} for all inputs connected to an output.
    - Sum must be *less* than the output I_{OL} specification.

Fan-out

- If the NAND gate drives N similar gates, we say that the *fan-out* is N. The output transistor now acts as a *sink* for the current in the input to the gates it drives. In other words, when Q_1 is in saturation (Y=0), the input current I of a following stage adds to the collector current of Q_1. Assume that all the input diodes to a following stage (which is now considered to be a current source) are HIGH except the one driven by Q_1.



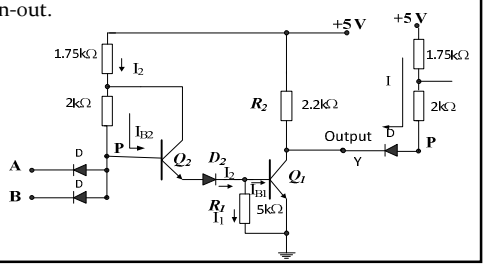
Then the current in this diode is $I = (V_{CC} - V_p)/5\text{k}\Omega = 0.82$ mA. This current is called *a standard load*. The total collector current of Q_1 is now $I_C = 0.82N + 2.18$ mA, where 2.18 mA is the unloaded collector current found in part a of the preceding example (Ex. 5 on page 40). Since the base current is almost independent of loading, I_B remains at its previous value of 0.40 mA. If we assume a reasonable value of $h_{FE(min)}$ of 30, the fan-out is given by $I_C = h_{FE} I_B$, or

- $I_C = 0.82N + 2.18 = (30)\ (0.40) = 12.0$ mA

and N = 12. Of course, the current rating of Q_1 must exceed 12.0 mA if we are to drive 12 gates.

- The fan-out may be increased considerably by replacing D_1 by a transistor Q_2. When Q_2 is conducting, it is in its active region and *not* in saturation. This statement follows from the fact that the current in the resistor which supplies the base current of Q_2 is in the direction to reverse-bias the collector junction of the *npn* transistor Q_2.

- Since the emitter current of Q_2 supplies the base current of Q_1, then Q_1 is driven by a much higher base current than is Q_1 in the prececing figure with D_1 connected. For the same $h_{FE(min)}$ of the output transistors in both configurations, the latter circuit (below) has larger collector current, and hence larger fan-out.



Example 7:

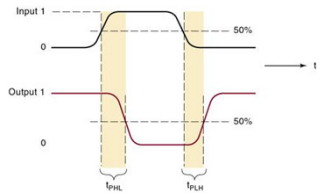
- If $h_{FE(min)}$ = 30, calculate the fan-out N for the NAND gate of the above circuit configuration. $V_{BE,active}$ = 0.7V.
- **Solution**
- As with the previous integrated DTL circuit in Ex. 5, if any inputs is LOW, then V_p = 0.9 V, and both Q_2 and D_1 are OFF. Hence $V_{BE2} = 0$, Q_1 is OFF, and Y = 1.
- If, however, all inputs are HIGH, the input diodes are OFF, Q_1 goes into saturation, and
- $V_p = V_{BE2,active} + V_{D2} + V_{BE1,sat} = 0.7\text{V} + 0.7\text{V} + 0.8\text{V} = 2.2\text{V}$
- Since Q_2 is in its active region, $I_{C2} = h_{FE} I_{B2}$. The current in the 2kΩ resistor is I_{B2} and the current in the 1.75kΩ resistor is $I_2 = I_{B2} + I_{C2} = (1 + h_{FE}) I_{B2}$. Applying KVL between V_{CC} and V_p, we have, for h_{FE} = 30
- $5 - 2.2 = (1.75)(31)\ I_{B2} + 2\ I_{B2}$
- or

- I_{B2} = 0.050 mA I_2 = (31)(0.050) = 1.55 mA
- I_1 = 0.8 V / 5kΩ =0.16 mA I_{B1} = 1.55 - 0.16 = 1.39 mA
- The unloaded collector current of Q_1 is (5 – 0.2)/2.2kΩ = 2.18mA. For *each* gate which it drives, Q_1 must sink a standard load of
- $I = \frac{5-0.7-0.2}{1.75+2} = 1.10$ mA
- Since the maximum collector current is $h_{FE}\, I_{B1}$, then
- I_{C1} = (30)(1.39 mA) = 1.10N + 2.18 mA = 41.7 mA
- and N = 36. The fan-out has been increased to 36 for the same h_{FE} which resulted in only 12 for the circuit of Ex. 5.
- The above calculations assumes that the current rating of Q_1 is at least 41.7 mA. On the other hand, if $I_{C1(max)}$ is limited to, say, 15 mA, then 1.10N + 2.18 mA = 15 mA, or $N \approx 11$. To drive the 11 gates requires that $h_{FE(min)} = I_{C1}/I_{B1}$ = 15/1.39 = 10.8, which is a very small number.

Digital IC Terminology – Propagation Delay

- A logic signal always experiences a delay going through a circuit.
  - The two propagation delay times are defined as:

t_{PLH}: Delay time in going from logical 0 to logical 1 state (LOW to HIGH)
t_{PHL}: Delay time in going from logical 1 to logical 0 state (HIGH to LOW)



Propagation delays.

Digital IC Terminology – Power Requirements

- Every IC requires a certain amount of electrical power to operate.
  - Supplied by one or more power-supply voltages connected at V_{CC} (TTL) or V_{DD} (MOS devices).
  - For many ICs, current drawn from the supply varies depending on logic states of the circuits on the chip.
- The amount of power an IC requires is determined by the current, I_{CC} (or I_{DD}) it draws from the supply.
  - Actual power is the product I_{CC} x V_{CC} (I_{DD} x V_{DD}).

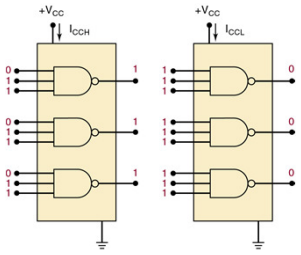
Digital IC Terminology – Power Requirements

In some logic circuits, average current is computed based on the assumption that gate outputs are LOW half the time and HIGH half the time.

$$I_{CC}(\text{avg}) = \frac{I_{CCH} + I_{CCL}}{2}$$

can be rewritten to calculate average power dissipated:

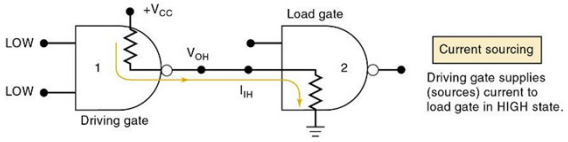
$$P_D(\text{avg}) = I_{CC}(\text{avg}) \times V_{CC}$$



Digital IC Terminology – Invalid Voltage

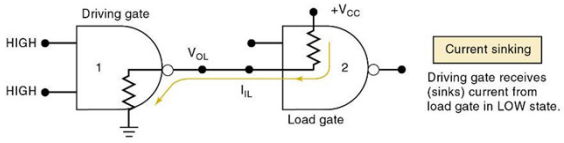
- For proper operation, logic circuit input voltage levels must be kept out of the indeterminate range.
  - Lower than V_{IL}(max) or higher than V_{IH} (min).
    - *Invalid* voltage will produce unpredictable output.
- It is important to know valid voltage ranges for the logic family being used so invalid conditions can be recognized when testing or troubleshooting.
- Logic families can be described by how current flows between the output of one logic circuit and the input of another.

Digital IC Terminology – Current Sourcing/Sinking



- **Current-sourcing** action.
  - When the output of gate 1 is HIGH, it supplies current I_{IH} to the input of gate 2.
    - Which acts essentially as a resistance to ground.
  - The output of gate 1 is acting as a *source* of current for the gate 2 input.

Digital IC Terminology – Current Sourcing/Sinking



- **Current-sinking** action.
  - Input circuitry of gate 2 is represented as a resistance tied to $+V_{CC}$—the positive terminal of a power supply.
  - When gate 1 output goes LOW, current will flow from the input circuit of gate 2 back through the output resistance of gate 1, to ground.
    - Circuit output that drives the input of gate 2 must be able to *sink* a current, I_{IL} , coming from that input.

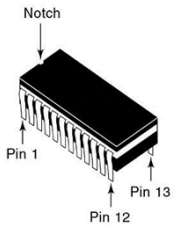
Digital IC Terminology – IC Packages

- There are many IC packages, differing in physical size, environmental & power consumption conditions, and circuit board mounting.

The DIP (dual-in-line package) has pins (leads) down the two long sides of the rectangular package.

The notch on one end, is used to locate pin 1.

Some DIPs use a small dot to locate pin 1.



24-pin DIP

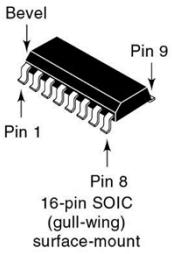
Digital IC Terminology – IC Packages

- Current manufacturing methods use surface-mount technology (SMT), which places an IC onto conductive pads on the surface of the board.

Held in place by a solder paste, and the entire board is heated to create a soldered connection.

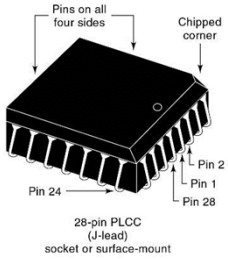
Precision machine placement allows for very tight lead spacing.

Leads are bent out from the plastic case, providing adequate surface area for the solder joint.



Digital IC Terminology – IC Packages

- Need for more connections to a complex IC has resulted in another very popular package with pins on all four sides of the chip.



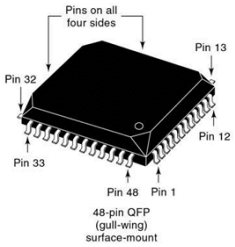
The PLCC has J-shaped leads that curl under the IC.

These devices can be surface-mounted to a circuit board—but can also be placed in a special socket.

Commonly used for components likely to need to be replaced for repair or upgrade.

Digital IC Terminology – IC Packages

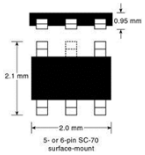
- Need for more connections to a complex IC has resulted in another very popular package with pins on all four sides of the chip.



QFP and TQFP packages have pins on all four sides in a gull-wing surface-mount package.

Digital IC Terminology – IC Packages

Logic gates are available in individual surface-mount packages containing one, two, or three gates, and as few as five or six pins (power, ground, two to three inputs, and an output)



Abbreviation	Package Name	Height	Lead Pitch
DIP	Dual-in-line package	200 mils (5.1 mm)	100 mils (2.54 mm)
SOIC	Small outline integrated circuit	2.65 mm	50 mils (1.27 mm)
SSOP	Shrink small outline package	2.0 mm	0.65 mm
TSSOP	Thin shrink small outline package	1.1 mm	0.65 mm
TVSOP	Thin very small outline package	1.2 mm	0.4 mm
PLCC	Plastic leaded chip carrier	4.5 mm	1.27 mm
QFP	Quad flat pack	4.5 mm	0.635 mm
TQFP	Thin quad flat pack	1.6 mm	0.5 mm
LFBGA	Low-profile fine-pitch ball grid array	1.5 mm	0.8 mm
LGA	Land grid array	0.9 mm	0.8 mm

The Standard TTL series Characteristics

1964 Texas Instruments introduced first line of standard TTL IC's.

- 54/74 series
- one of the most widely used series
- known as the 74 series (54 wider temperature range)

Many semiconductor IC manufactures now produce TTL IC's

- Fortunately all use the same numbering system
- Allowing interchanging of components

SN74	***Texas Instruments 74 Series***
DM74	***National Semiconductor 74 Series***
S74	***Signetics 74 Series***

⇒ e.g. a quad 2-input NAND ⇒ 00 SN7400

The Standard TTL series Characteristics

- Several other TTL series have been developed since the introduction of the 74 standard series.
  - 74LS, 74S etc.
- Provide a wide choice of speed and power characteristics

NOTE

- whenever we use TTL we mean the 74 series.

The Standard TTL series Characteristics

The propagation delay of a transistor which goes into saturation.

- depends on two factors
- Saturation delay (storage time delay)
- RC time constant

By reducing resistor values

- reduces RC time constant
- decreases propagation delay

Trade-off is high power dissipation

- lower resistance draws more current from the power supply

$$\text{Speed of gate} \propto \frac{1}{\text{Propagation Delay}}$$

Low Power, 74L series

Similar as standard TTL

But all resistor values have been **increased**.

⇒ low power dissipation **1 mW**
⇒ greater propagation delay 33 ns

- good for applications with low frequency, battery operated circuits
  - calculators etc.

High Speed, 74H series

Similar as standard TTL

But all resistor values have been **reduced**.

- Emitter follower has been replaced by a double emitter follower (Darlington Pair)

⇒ faster switching ⇒ propagation delay **6 ns**

but

⇒ increased power dissipation **23 mW**

How to increase speed ?

Whatever is done to the value of the resistors

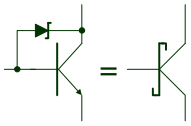
- Speed is ultimately limited by the time required to pull the output transistors out of saturation.
- 74, 74L and 74H series all operate with saturated switching
  - many of the transistors, when conducting will be in a saturated condition
- As has been seen this causes a saturation delay (storage delay), when switching from ON to OFF
  - limits the circuit's switching speed.

Schottky TTL, 74S series

Can this be improved ?

In Schottky TTL (STTL)

- Transistors kept out of saturation by using Schottky barrier diodes (SD)
- Formed by a junction of a metal and semiconductor
  - conventional diode with a junction of *p*-type and *n*-type semiconductor material
  - SD connected between the base and the collector
  - Do not allow the transistors to go as deeply into saturation
  - SD has a forward voltage drop of 0.4V



Schottky TTL, 74S series

- When the Collector-Base junction becomes forward biased at the on-set of saturation

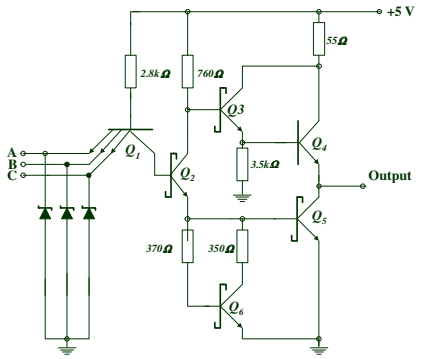
  ⇒ SD will conduct, diverting some input current away from base.

  ⇒ this has effect of reducing the excess base current.

  ⇒ decreases saturation (storage time) delay at turn-off

- 74S00 NAND has average propagation delay of 3 ns
  - twice as fast as the 74H00
  - makes the 74H series redundant nowadays

Schottky TTL, 74S series



Schottky TTL, 74S series

- Schottky Transistor used
  - 3 Schottky diodes inserted to limit negative inputs values
  - no diode in the Totem-pole output
- Circuit also uses smaller resistor values to improve switching times
- Improves the circuit average power dissipation to 20 mW

NOTE

All transistor are Schottky Transistors.

- Q4 is not required to be a Schottky as it does not saturate but stays in active region

Schottky TTL, 74S series

- New combination of Q3 and Q6 still gives the two V_{BE} drops
  - necessary to prevent Q4 from conducting when the output is low.
- Combination comprises a double-emitter follower (Darlington pair)
  - Provides high current gain and extremely low resistance
  - needed during the low-to high swing of the output
  - rapid output rise time when switching ON-to-OFF

⇒ Results in a decrease in propagation delay.

Low Power Schottky TTL, 74LS series

74 LS is a low powered version of the 74S series

- uses Schottky clamped configuration
- but with larger resistor values then 74S

Low circuit power requirements

but at the expense of increase in switching times.

- Power Dissipation 2 mW
- Propagation Delay 9.5 ns

This is the mainstay of the TTL family

- Found in nearly all new designs that do not require max speed.

Advanced Schottky TTL, 74AS series

- As a result of the recent development in IC design and manufacturing process
  - High speed Schottky diodes
- Power Dissipation **8 mW**
- Propagation Delay **1.7 ns**

Advanced Low-Power Schottky TTL, 74ALS series

Improvement in both power and speed.

- Power Dissipation **1.2 mW**
- Propagation Delay **4 ns**

This series has

- the lowest speed-power product of the TTL series
- very close to the lowest gate power dissipation (c.f. 74L)

This **will eventually** replace 74LS as the most widely used TTL series.

Comparison of TTL Series Characteristics

		74	74L	74H	74S	74LS	74AS	74 ALS
Performance Ratings	Propagation Delay (nSec)	9	33	6	3	9.5	1.7	4
	Power Dissipation (mW)	10	1	23	20	2	8	1.2
	Speed Power (pJ)	90	33	138	60	19	13.6	4.8
	Max Clock rate (MHz)	35	3	50	125	45	200	70
	Fan-out (same series)	10	20	10	20	20	40	20
Voltage Parameters	VOH(min)	2.4	2.4	2.4	2.7	2.7	2.5	2.5
	VOL(max)	0.4	0.4	0.4	0.5	0.5	0.5	0.4
	VIH(min)	2.0	2.0	2.0	2.0	2.0	2.0	2.0
	VIL(max)	0.8	0.7	0.8	0.8	0.8	0.8	0.8

All of the performance ratings are for a NAND gate in each series.

Speed Power (picoJoules)

- low value required.

The **Maximum Clock Rate** :

- specified as the maximum frequency that can be used to toggle a J-K flip-flop.
- Gives a measure of the frequency range over which each series can be operated.

Differences in TTL family are not in Logic Levels

- **But in internal construction of the basic NAND gate.**