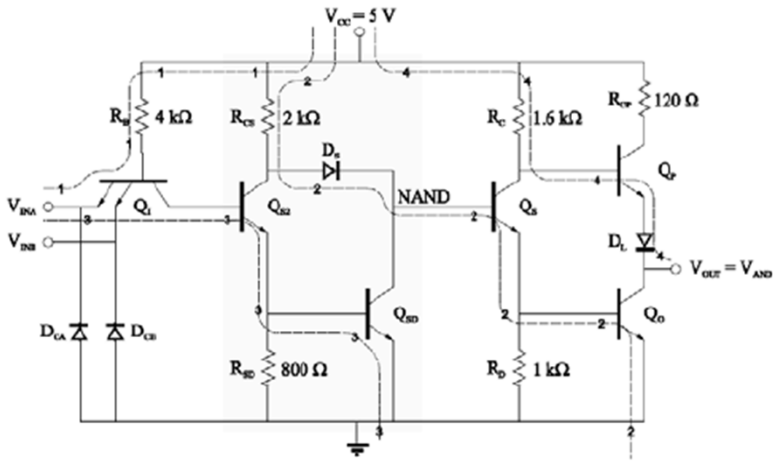
Chapter 6
Bipolar Logic Circuits

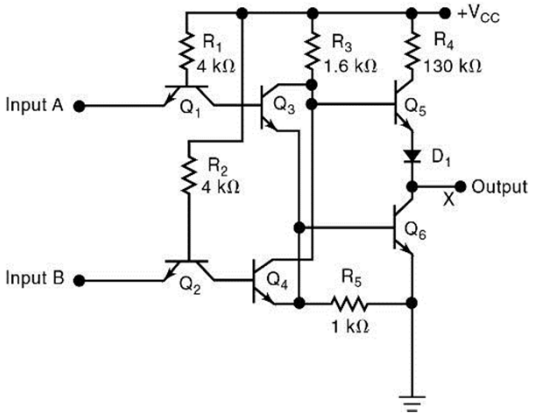
Other TTL Gates
Emitter-Coupled Logic (ECL) and
Resistor Transistor Logic (RTL)

TTL AND GATE



2

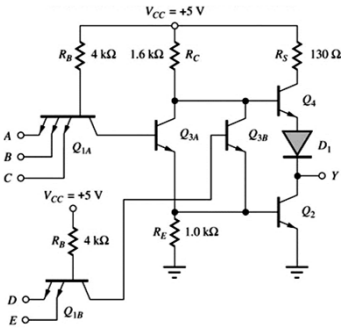
TTL NOR GATE



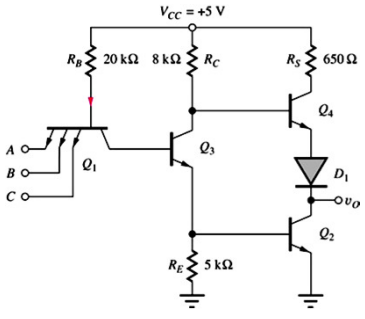
- The **NOR** circuit does *not* use a multiple-emitter transistor.
- Each input is applied to the emitter of a separate transistor.
- The **NOR** circuit uses the same totem-pole arrangement as the **NAND** circuit on the output side

3

Other TTL Gates



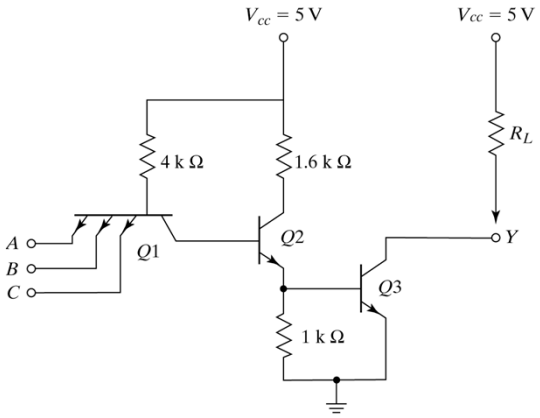
TTL AND-OR-Invert



Low-power TTL NAND gate

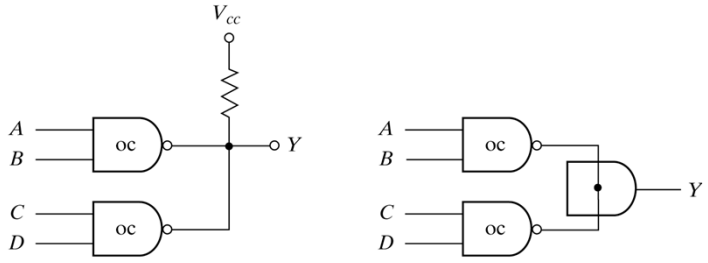
4

Open-collector TTL Gate



5

Wired-AND of Two Open-Collector



(a) Physical connection (b) Wired-logic graphic symbol

Fig. 10-12 Wired-AND of two Open-Collector (oc) Gates, $Y = (AB + CD)'$

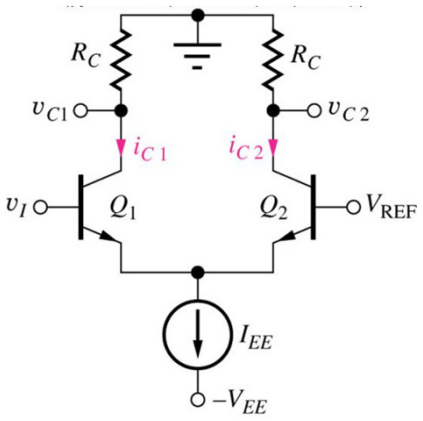
6

Emitter-Coupled Logic (ECL)

- Nonsaturated digital logic family
- Propagation rate as low as 1-2ns
- Used mostly in high speed circuits
- Noise immunity and power dissipation is the worst of all logic families.
- High level -0.8V, Low level -1.8V
- Including
  - Differential input amplifier
  - Internal temperature and voltage compensated bias network
  - Emitter-follower outputs

7

The Current Switch (Emitter-Coupled Pair)

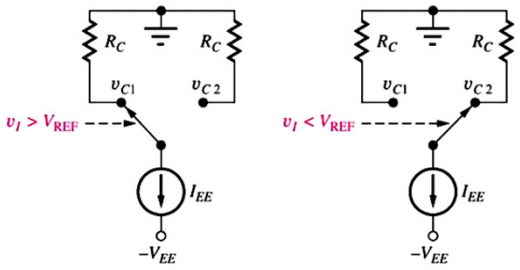


- The building block of emitter-coupled logic (ECL) is the current switch circuit which consists of matched components

8

The Current Switch

- Depending on how much higher or lower the input voltage v_I is compared to V_{REF}, the reference current will switch to one of the legs creating a voltage v_{C1} or v_{C2}.



9

Mathematical Model for Static Behavior of the Current Switch

- The previous figure showed the ideal case for switching the currents between the two legs, but in real BJTs current will be present in both legs depending upon v_{BE} of each BJT in the pair

- The collector current difference is given by:

$$i_{C1} - i_{C2} = \alpha_F I_{EE} \tanh\left(\frac{v_{BE1} - v_{BE2}}{2V_T}\right)$$

10

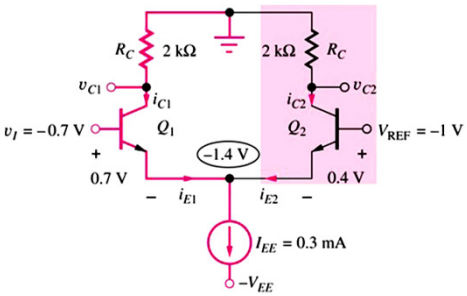
Typical npn Transistor Parameters

Region	V_{BE} (V)	V_{CE} (V)	Current Relation
Cutoff	< 0.6	Open circuit	$I_B=I_C=0$
Active	0.6-0.7	> 0.8	$I_C = h_{FE}I_B$
Saturation	0.7-0.8	0.2	$I_B \geq I_C/h_{FE}$

11

Current Switch Analysis for $v_I > V_{REF}$

- Given the circuit shown under the given bias conditions (v_I is 300mV larger than V_{REF}), the majority of current will flow in the left leg.

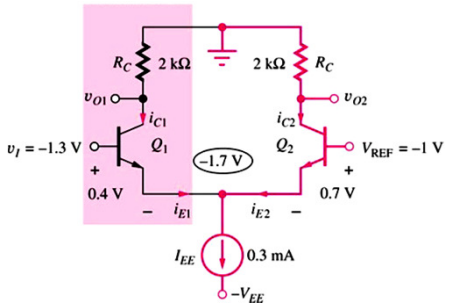


$$i_{E1} \cong I_{EE}$$
$$i_{E2} \cong 0$$
$$v_{C1} = -i_{C1}R_C \cong -\alpha_F i_{E1}R_C \cong -\alpha_F I_{EE}R_C$$
$$v_{C2} = -i_{C2}R_C \cong -\alpha_F i_{E2}R_C \cong 0$$

12

Current Switch Analysis for $v_I < V_{REF}$

- Given the circuit shown under the given bias conditions (v_I is 300mV less than V_{REF}), the majority of current will flow in the right leg

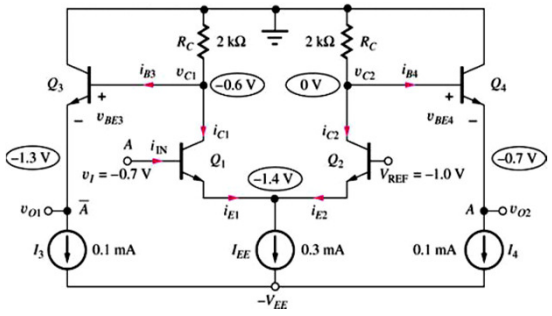


$$i_{E1} \cong 0$$
$$i_{E2} \cong I_{EE}$$
$$v_{C1} = -i_{C1}R_C \cong -\alpha_F i_{E1} R_C \cong 0$$
$$v_{C2} = -i_{C2}R_C \cong -\alpha_F i_{E2} R_C \cong -\alpha_F I_{EE} R_C$$

13

The Emitter-Coupled Logic (ECL) Gate

- The outputs of the previous current switch have the value of either 0V or –0.6V
- The difference of the input and output of the current switch is exactly one base-emitter voltage drop
- For a complete ECL gate, the voltages are shifted by a base-emitter drop as shown in the figure.



14

ECL Gate Summary

v_I	v_{O1}	v_{O2}	I_{IN}
V_{REF} + 0.3V = -0.7V	-1.3V	-0.7V	+14.3μA
V_{REF} - 0.3V = -1.3V	-0.7V	-1.3V	0

$$i_{IN} = i_{B1} = \frac{i_{EE}}{\beta_F + 1} \qquad \text{For } v_I = -0.7\text{V}$$

$$i_{IN} = 0 \qquad \text{For } v_I = -1.3\text{V}$$

$$V_{REF} = \frac{V_H + V_L}{2}$$

15

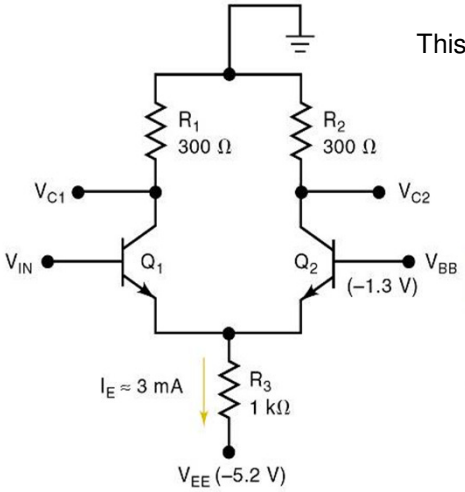
ECL Gate Benefits

- ECL gates produce both true and complemented outputs
- ECL gates are fast since the BJTs are always in forward active mode, and it only takes a few tenths of a volt to get the output to change states, hence reducing the dynamic power
- ECL gates provide near constant power supply current for all states thereby generating less noise from the other circuits connected to the supply

16

The ECL Digital IC Family

Basic ECL circuit – differential amplifier



This circuit produces complementary outputs: V_{OUT1}, equal to $\overline{V_{IN}}$, and V_{OUT2}, equal to V_{IN}.

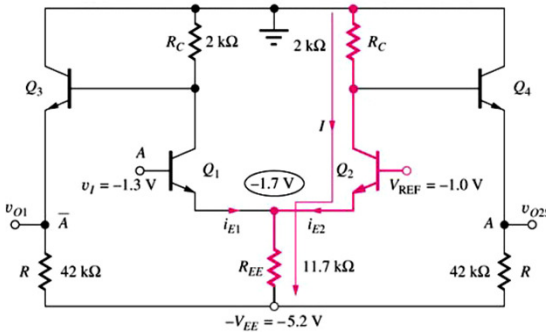
Operating States

V_{IN}	Outputs	
–1.7 V (logic 0)	V_{C1} = 0 V V_{C2} = –0.9 V	Q_2 conducts
–0.8 V (logic 1)	V_{C1} = –0.9 V V_{C2} = 0 V	Q_1 conducts

17

Current Source Implementation

- Instead of using actual current sources for the current biasing in an ECL gate, resistors can be used as shown below

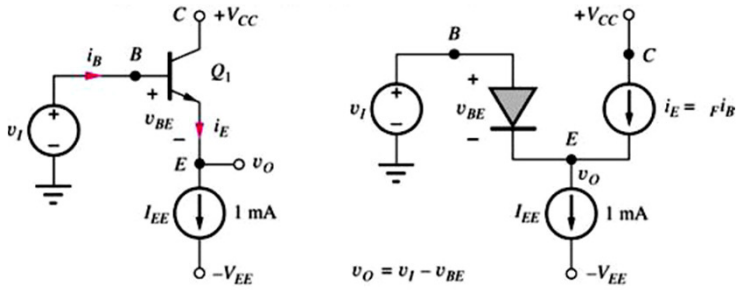


Note that the currents in the emitter-follower legs will not be equal since the output voltages will be different. This will instead be looked at as an average value between the two legs.

18

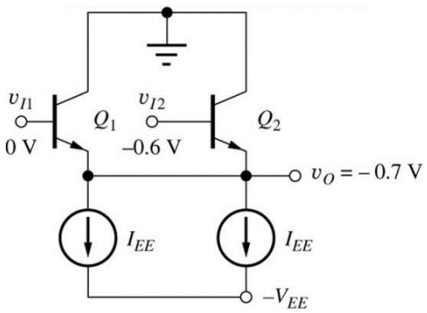
The Emitter Follower

- The main purpose of the emitter follower in ECL gates is to create a level shift in the output
- The figure shows both the circuit and its transport model for the forward- active region



19

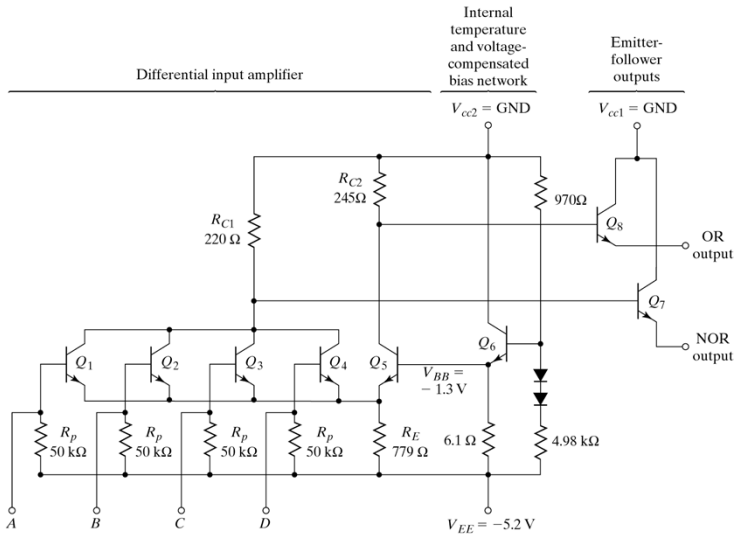
"Emitter Dotting" or "Wired-OR" Logic



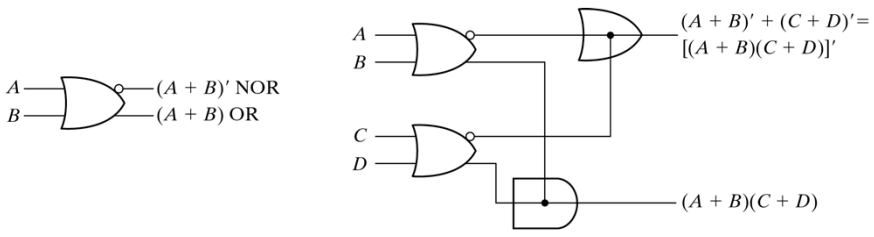
- The circuit shown in the figure exhibits two emitter followers in parallel with a common output
- The result for the shown bias condition implies that Q_2 is cutoff and Q_1 has to handle $2I_{EE}$

20

ECL Basic OR/NOR Gate



Graphic Symbols of ECL Gates



(a) Single gate

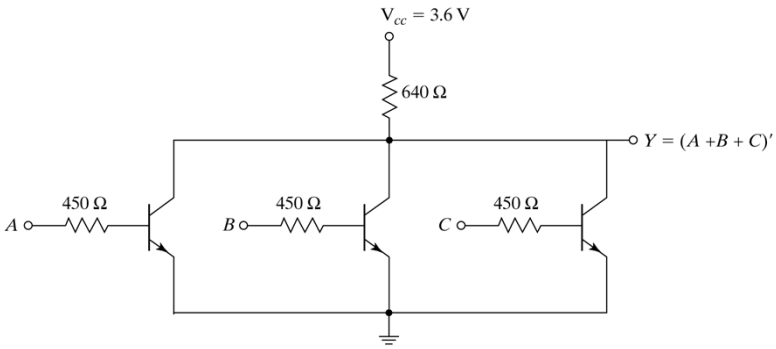
(b) Wired combination of two gates

ECL characteristics

- Very fast switching with typical propagation delay of 360ps — faster than TTL or CMOS.
- The standard ECL logic levels are nominally -0.8 V and -1.7 V for logical 1 and 0 respectively.
- Worst-case noise margins approximately 150 mV.
- ECL logic gates usually produce an output and its complement, eliminating the need for inverters.
- Current flow remains constant, eliminating noise spikes.

23

RESISTOR-TRANSISTOR LOGIC (RTL)



An RTL NOR Gate with 3 inputs.

24

RTL NOR

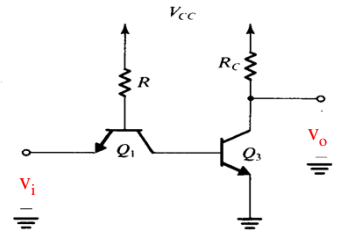
- The 3-input positive NOR gate operates as follows:
- If any input is HIGH, the corresponding transistor is driven into saturation and the output is LOW, $v_o = V_{CE,sat} \approx 0.2V$. If all inputs are LOW, then all input transistors are cut off by $V_\gamma - V(0) = 0.5 - 0.2 = 0.3V$ and the output v_o is HIGH.
- The value of v_o depends upon the fan-out. For example, if N = 5, then the output of the NOR gate is loaded by five 450-Ω resistors in parallel (or 90Ω), which is tied to $V_{BE,sat} \approx 0.8V$. Under these circumstances (using superposition),
- $v_0 = \frac{3.6 \times 90}{90+640} = 1.14V$
- This voltage must be large enough so that the base current can drive each of the five transistors into saturation. Since
- $I_B = \frac{1.14-0.8\ V}{0.45k\Omega} = 0.755\ mA \qquad I_C = \frac{3.6-0.2\ V}{0.64k\Omega} = 5.31\ mA$

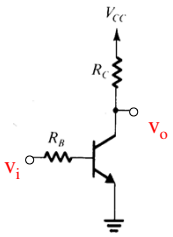
25

- then the circuit will operate properly if $h_{FE} > h_{FEmin} = 5.31/0.76 = 7$.
- **Resistor-transistor logic uses the minimum space (for a standard digital function) on a silicon wafer, and hence is very economical.**
- **The disadvantages are, low noise immunity, low switching speed and sensitivity to temperature variations.**

26

Simplified TTL vs. RTL





* **Logic levels and noise margins**

- **Noise Margin for Low State**
  - **$NM_L = V_{IL} - V_O = 0.6\ V - 0.1\ V = 0.5V$**
- **Noise Margin for High State**
  - **$NM_H = V_{OH} - V_{IH} = 5\ V - 0.7\ V = 4.3\ V$**
- **Unequal noise margins for high and low states.**

- **Propagation delays**
  - **Output going low** $t_{PHL} = 0.55\ n\text{sec}$
  - **Output going high** $t_{PLH} = 16\ n\text{sec}$
  - **Propagation delay** $t_P = 8.3\ n\text{sec}$

* Logic levels and noise margins

→ Noise Margin for Low State

★ $NM_L = V_{IL} - V_O = 0.7\ V - 0.2\ V = 0.5\ V$

→ Noise Margin for High State

★ $NM_H = V_{OH} - V_{IH} = 5\ V - 0.8\ V = 4.2\ V$

→ Unequal noise margins for high and low states.

* Propagation delays

→ Output going low $t_{PHL} = 12\ n\text{sec}$

→ Output going high $t_{PLH} = 100\ n\text{sec}$

→ Propagation delay $t_P = 56\ n\text{sec}$

27