DIGITAL TO ANALOG CONVERTERS

Binary Weighted Input DAC
R/2R Ladder DAC
Integrated Circuit DAC

Digital Basics

- **Digital to Analog Converter**
  - **Takes a digital input and converts it to an analog voltage output.**

Digital Input:	**0 – 255 (00 – FF)**
Analog Output:	**0 – 2.55V**
Resolution:	**10 mV**

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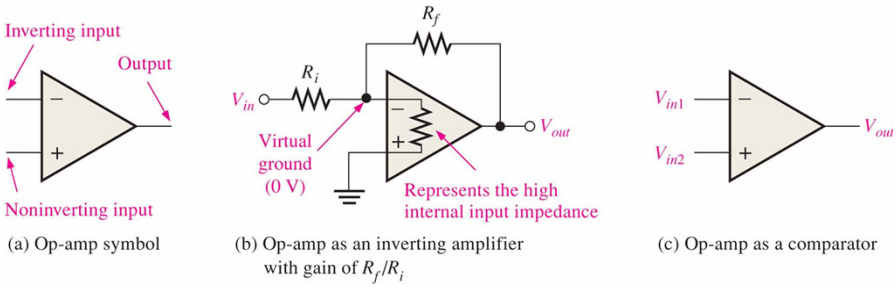
The operational amplifier (op-amp).

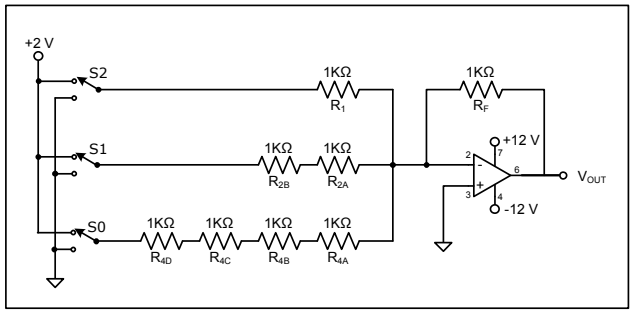


(a) Op-amp symbol

(b) Op-amp as an inverting amplifier with gain of R_f/R_i

(c) Op-amp as a comparator

Current Summing DAC



S2	S1	S0	Expected V_{OUT}
0	0	0	- 0.0 V
0	0	1	- 0.5 V
0	1	0	- 1.0 V
0	1	1	- 1.5 V

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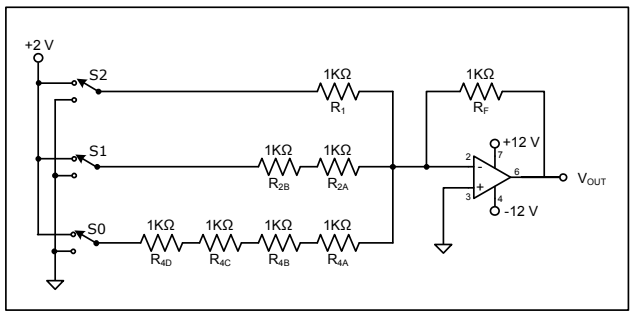
Current Summing DAC



S2	S1	S0	Expected V_{OUT}
1	0	0	- 2.0 V
1	0	1	- 2.5 V
1	1	0	- 3.0 V
1	1	1	- 3.5 V

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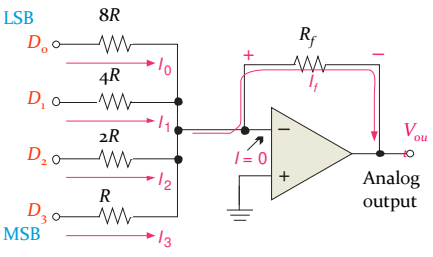
Digital-to-Analog Conversion Methods

Binary-weighted-input DAC:

The binary-weighted-input DAC is a basic DAC in which the input current in each resistor is proportional to the column weight in the binary numbering system. It requires very accurate resistors and identical HIGH level voltages for accuracy.

The MSB is represented by the largest current, so it has the smallest resistor. To simplify analysis, assume all current goes through R_f and none into the op-amp.



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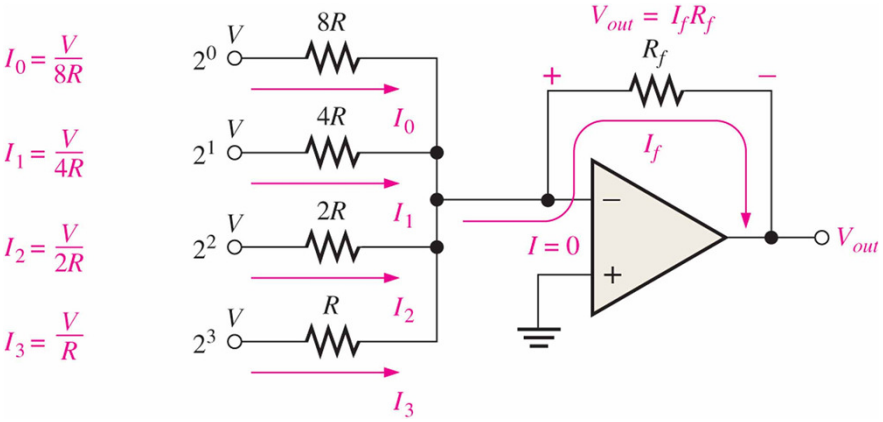
A 4-bit DAC with binary-weighted inputs.



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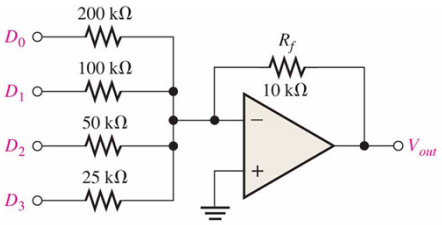
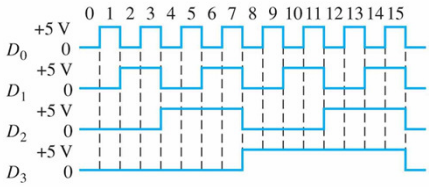
EXAMPLE

The digital signal shown in Fig. (b) are applied to the inputs of the DAC circuit in Fig.(a). Draw the input/output curve.



(a)



(b)

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SOLUTION

- First, the input currents are calculated according to the digital inputs for logic 1 states. Using superposition theorem and Ohm's law, we have

$$I_0 = \frac{5\,V}{200\,K} = 0{,}025\,mA$$

$$I_1 = \frac{5\,V}{100\,K} = 0{,}05\,mA$$

$$I_2 = \frac{5\,V}{50\,K} = 0{,}1\,mA$$

$$I_3 = \frac{5\,\mathrm{V}}{25\,\mathrm{K}} = 0{,}2\,\mathrm{mA}$$

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- As the OPAMP input resistance is very high, the current through the inverting input is almost zero. Thus, all of the input currents will flow through the feedback resistor R_f. The output voltage is equal to the product of the feedback resistor R_f and the sum of the input currents. The effect of each input current to the output voltage is calculated independently. For the digital inputs which are logic 1, the voltages are added, but for the digital inputs which are logic 0, the voltages are not added to find the resulting output voltage.

$$V_{\text{ÇIKIŞ}(D0)} = (10\,k\Omega)(-0{,}025\,mA) = -0{,}25\,V$$

$$V_{\text{ÇIKIŞ}(D1)} = (10\,\mathrm{k\Omega})(-0{,}05\,\mathrm{mA}) = -0{,}5\,V$$

$$V_{\text{ÇIKIŞ}(D2)} = (10\,\mathrm{k\Omega})(-0{,}1\,\mathrm{mA}) = -1\,V$$

$$V_{\text{ÇIKIŞ}(D3)} = (10\,\mathrm{k\Omega})(-0{,}2\,\mathrm{mA}) = -2\,V$$

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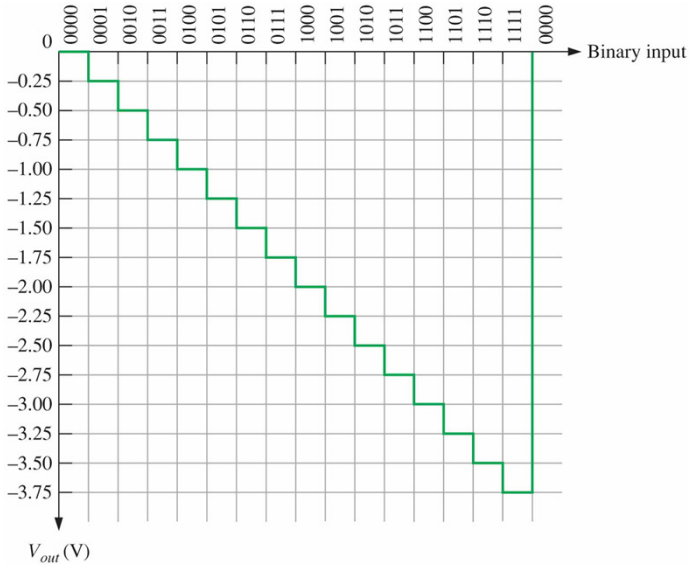
Output of the DAC



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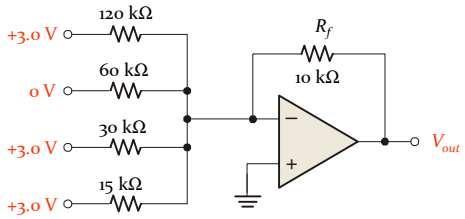
Example A certain binary-weighted-input DAC has a binary input of 1101. If a HIGH = +3.0 V and a LOW = 0 V, what is V_{out}?



Solution

$$I_{out} = -(I_0 + I_1 + I_2 + I_3)$$

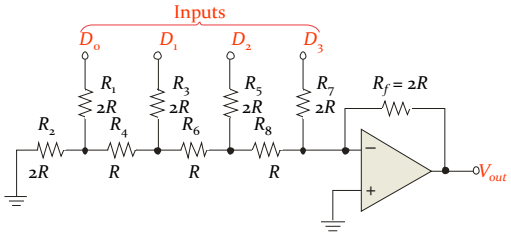
$$= -\left(\frac{3.0\text{ V}}{120\text{ k}\Omega} + 0\text{ V} + \frac{3.0\text{ V}}{30\text{ k}\Omega} + \frac{3.0\text{ V}}{15\text{ k}\Omega}\right) = -0.325\text{ mA}$$

$$V_{out} = I_{out} R_f = (-0.325\text{ mA})(10\text{ k}\Omega) = -3.25\text{ V}$$

R-2R ladder:

The *R-2R* ladder requires only two values of resistors. By calculating a Thévenin equivalent circuit for each input, you can show that the output is proportional to the binary weight of inputs that are HIGH.

For accuracy, the resistors must be precise ratios, which is easily done in integrated circuits.



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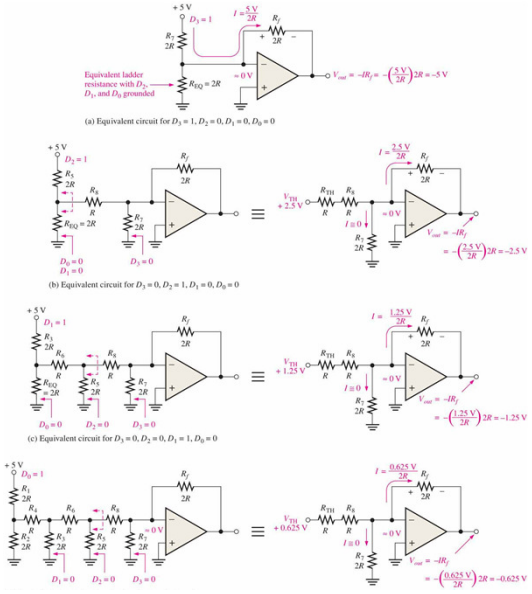
Analysis of the *R*/2*R* ladder DAC.



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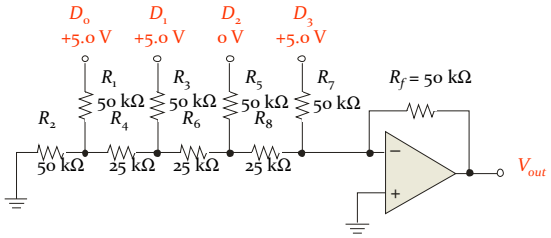
Example An *R-2R* ladder has a binary input of 1011. If a HIGH = +5.0 V and a LOW = 0 V, what is V_{out}?



Solution

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Resolution

- One definition for resolution is the number of steps in the output/input characteristic curve. For an *n*-bit DAC:
- resolution = 2^n or $(2^n - 1)$ (10-1a)
- There is another definition of resolution: *Resolution equals the value of 1 LSB:*
- resolution = value of 1 LSB (10-1b)

DAC Output-Input Equation

- The characteristic output/input equation of a DAC is
- V_o = (value of 1 LSB)D (10-2)
- where V_o is the analog output voltage, and D is the decimal value of the digital input word.
- Full-scale output results when the digital input code is a maximum of all 1's.
- Full-scale output = (value of 1 LSB) $(2^n - 1)$ (10-3)

R/2R ladder currents

- The working principle of the *R/2R* resistance ladder lays on the equally splitting currents between nodes (3, 2, 1 & 0). It is clear that we see a resistance of *R* to ground looking (right) into any node. Any current entering this node sees two paths of equal resitance. One path is *2R*, via the bit switch; the other path is also *2R*, via one of the three horizontal *R* resistors in series with an *R* resistance looking right into the next node.

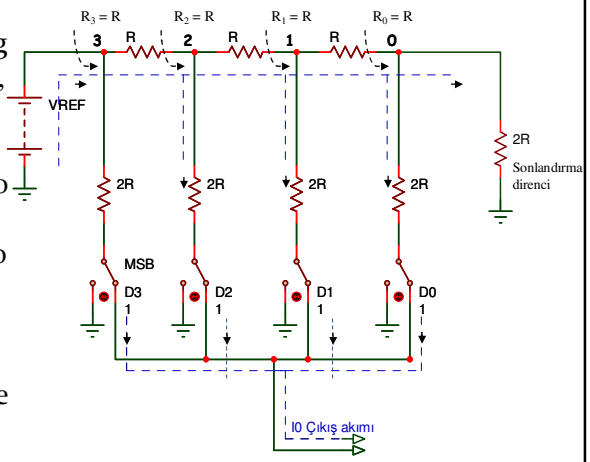

Fig.10-1

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- The current path of the *R-2R* network is found as follows:

1. Input current to the ladder is set by

$$I = \frac{V_{ref}}{R} \qquad (10\text{-}4)$$

2. Current I splits equally into two parts at node 3. One part (vertical) is bit 3 output current $I_3 = I/2$. The second part (horizontal) flows toward node 2, where it will also divide into two equal parts of $I_2 = I_3/2 = I/4$.
3. As the circuit current is designed to equally divide into two at each node, current I_1 is also equal to $I_2/2 = I/8$. I_1 is also divided into two as $I_0 = I_1/2 = I/16$ and half of it flows through *2R* resistor as the output current of bit 0, and the other half flows through the terminate resistor *2R* to the ground. As a result, in the *R-2R* ladder DAC there is always a loss of $I/2^n$ part of the reference current.

- The ladder output currents are constant and found from:

$$I_3 = \frac{I}{2}\ ;\ I_2 = \frac{I_3}{2} = \frac{I}{4}\ ;\quad I_1 = \frac{I_2}{2} = \frac{I}{8}\ ;\ I_0 = \frac{I_1}{2} = \frac{I}{16} = LSB \qquad (10\text{-}5)$$

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Output Currents

- Ladder output current I_{out} is the *sum* of each ladder current flowing to the output. When the D_0 swith is closed, a current value of 1 LSB enters the output bus. If D_1 is "1", a current of 2 LSB enters the output bus. D_2 can output 4 LSB and D_3 can output 8 LSB. Output current is then found in terms of the digital input by
- I_{out} = (current value of 1 LSB) × D (10-6a)
- where
- current value of 1 LSB = I_0, (10-6b)
- but Eq.(10-4) shows that the user determines I_0 by choosing V_{ref} and R. Substituting Eq.(10-4) into Eqn.(10-6b) gives us
- current value of 1 LSB = $\left(\frac{V_{REF}}{R}\right)\left(\frac{1}{2^n}\right) = I_0$ (10-6c)

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VOLTAGE OUTPUT DAC

- An op amp can be added to the very basic DAC of Fig. 10-1. The result is the voltage output DAC shown in the Fig.10-2. Output current is converted to a voltage V_0 by feedback resistor R_F and the op amp.
- $V_0 = -I_{out}R_F = -$(current value of 1 LSB) × $R_F D$ (10-7a)
- Multiply Eq. (10-6c)by R_F to obtain the resolution of our voltage output DAC:
- $resolution =$ (voltage value of 1 LSB) $= \left(\frac{V_{ref}}{R}\right)\left(\frac{1}{2^n}\right)R_F$ (10-7b)
- Combine Eqs. (10-7b) and (10-7b) to obtain V_0 in terms of the digital input and circuit components.
- V_0 = - (resolution)D (10-7c)

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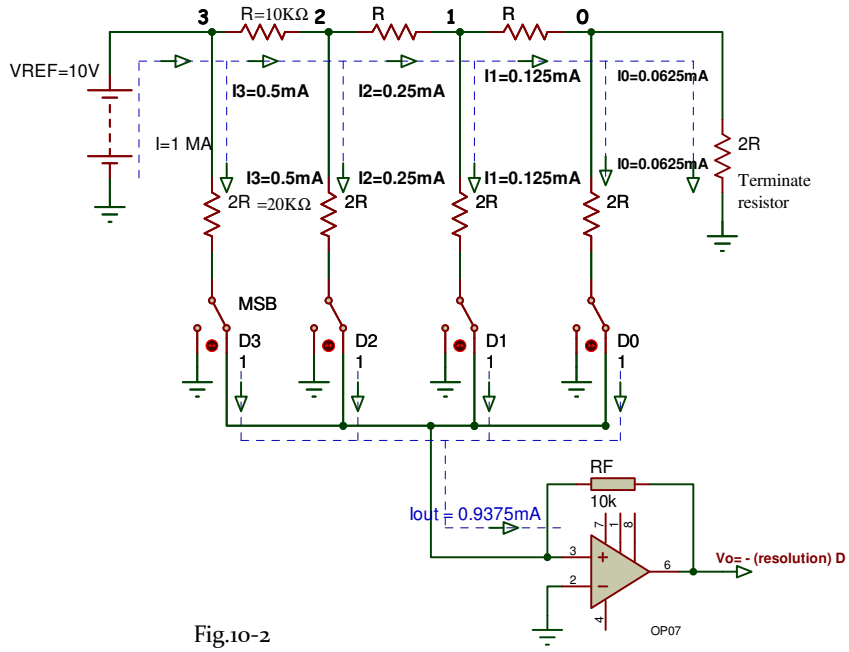

Fig.10-2

Example:

- Refer to the 4-bit DAC of the Fig. 10-2. Find (a) its voltage resolution and (b) the output voltage when the digital input is 1111 (i.e. full-scale voltage).
- **SOLUTION (a)** From Eq. (10-7b),
- resolution = $\left(\frac{10V}{10k\Omega}\right)\left(\frac{1}{2^4}\right)(10k\Omega) = \frac{10V}{16} = 0.625V/bit$
- **(b)** The value of D is 15 for an input of 1111. From Eq. (10-7c),
- $V_o = V_{FS} = -(0.625V)(15) = -9.375$ V.

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A SAMPLE DAC

- DAC0830/0832 DAC has 8 binary inputs. Each bit, produces an output current that is proportional to the binary weight of the digital input. In an 8-bit binary system, the least significant bit has a binary weight of 1, second 2, third 4 and others have binary weight of 8, 16, 32, 64, 128 respectively. This digital-to-analog converter uses *R-2R* ladder current network. The functional block diagram is given in Fig. 10-3.

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DAC 0830/0832
8-Bit µP Compatible, Double-Buffered DAC

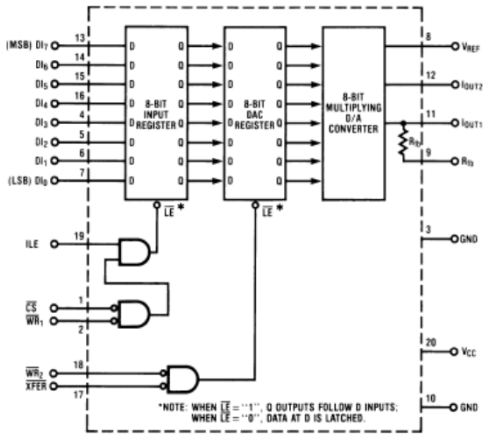

Fig.10-3 DAC0830 Functional Diagram.

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General Description

- The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z80®, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.
- Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.
- The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DACs (MICRO-DAC™).

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Features

- Double-buffered, single-buffered or flow-through digital data inputs.
- Direct interface to all popular microprocessors
- Linearity specified with zero and full scale adjust only—NOT BEST STRAIGHT LINE FIT.
- Works with ±10V reference-full 4-quadrant multiplication
- Can be used in the voltage switching mode
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Operates “STAND ALONE” (without µP) if desired
- Available in 20-pin small-outline or molded chip carrier package

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Key Specifications

- Current settling time: 1 μs
- Resolution: 8 bits
- Linearity: 8, 9, or 10 bits (guaranteed over temp.)
- Gain Tempco: 0.0002% FS/°C
- Low power dissipation: 20 mW
- Single power supply: 5 to 15 V_{DC}

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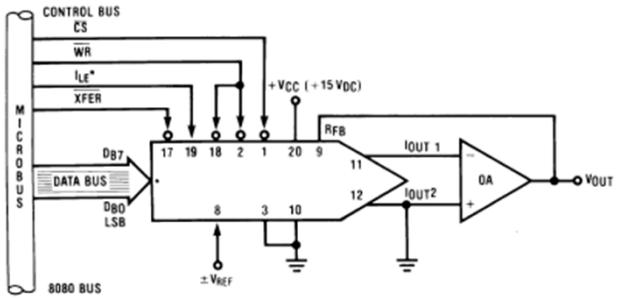
Typical Application



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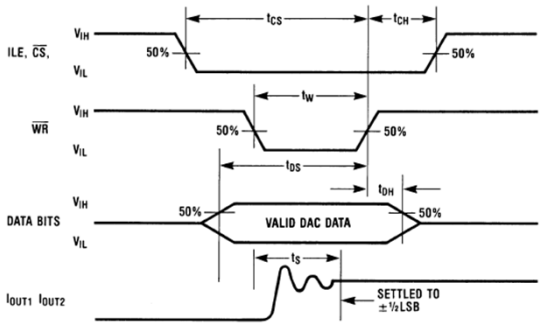
Switching Waveform



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Definition of Package Pinouts

- **Control Signals**
- (All control signals level actuated)
- **CS: Chip Select** (active low). The CS in combination with ILE will enable WR1.
- **ILE: Input Latch Enable** (active high). The ILE in combination with CS enables WR1.
- **WR1: Write 1.** The active low WR1 is used to load the digital input data bits (DI) into the input latch. The data in the input latch is latched when WR1 is high. To update the input latch–CS and WR1 must be low while ILE is high.
- **WR2: Write 2** (active low). This signal, in combination with XFER, causes the 8-bit data which is available in the input latch to transfer to the DAC register.
- **XFER: Transfer control signal** (active low). The XFER will enable WR2.

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- **Other Pin Functions**
- **DIo-DI7: Digital Inputs.** DIo is the least significant bit (LSB) and DI7 is the most significant bit (MSB).
- **I_{OUT1}: DAC Current Output 1.** I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all o's in DAC register.
- **I_{OUT2}: DAC Current Output 2.** I_{OUT2} is a constant minus I_{OUT1} , or I_{OUT1} + I_{OUT2} = constant (I full scale for a fixed reference voltage).
- **R_{fb}: Feedback Resistor.** The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.
- **V_{REF}: Reference Voltage Input.** This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of +10 to –10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.
- **V_{CC}: Digital Supply Voltage**. This is the power supply pin for the part. V_{CC} can be from +5 to +15V_{DC}. Operation is optimum for +15V $_{DC}$
- **GND:** The pin 10 voltage must be at the same ground potential as I_{OUT1} and I_{OUT2} for current switching applications.

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Definition of Terms

- **Resolution:** Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC0830 has 2^8 or 256 steps and therefore has 8-bit resolution.
- **Linearity Error:** Linearity Error is the maximum deviation from a straight line passing through the endpoints of the DAC transfer characteristic. It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.
- **Power Supply Sensitivity:** Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.
- **Settling Time:** Settling time is the time required from a code transition until the DAC output reaches within ±1/2LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

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- **Full Scale Error:** Full scale error is a measure of the output error between an ideal DAC and the actual device output.
- Ideally, for the DAC0830 series, full scale is V_{REF} –1LSB. For V_{REF} = 10V and unipolar operation, $V_{FULL\text{-}SCALE}$ = 10,0000V–39mV 9.961V. Full-scale error is adjustable to zero.
- **Differential Nonlinearity:** The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB to differential nonlinearity.
- **Monotonic:** If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. An 8-bit DAC which is monotonic to 8 bits simply means that increasing digital input codes will produce an increasing analog output.

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ANALOG CONSIDERATIONS

- The fundamental purpose of any D to A converter is to provide an accurate analog output quantity which is representative of the applied digital word. In the case of the DAC0830, the output, I_{OUT_1}, is a current directly proportional to the product of the applied reference voltage and the digital input word. For application versatility, a second output, I_{OUT_2}, is provided as a current directly proportional to the complement of the digital input. Basically:

$$I_{OUT1} = \frac{V_{REF}}{15\ k\Omega} \times \frac{\text{Digital Input}}{256};$$

$$I_{OUT2} = \frac{V_{REF}}{15\ k\Omega} \times \frac{255 - \text{Digital Input}}{256}$$

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Resolution and Accuracy of DACs

The *R-2R* ladder is relatively easy to manufacturer and is available in IC packages. DACs based on the *R-2R* network are available in 8, 10, and 12-bit versions. The **resolution** is an important specification, defined as the reciprocal of the number of steps in the output.

Question What is the resolution of the BCN31 *R-2R* ladder network, which has 8-bits?

Answer $2^8 - 1 = 255$ $1/255 = 0.39\%$

The **accuracy** is another important specification and is derived from a comparison of the actual output to the expected output. For the BCN31, the accuracy is specified as ±½ LSB = 0.2%.

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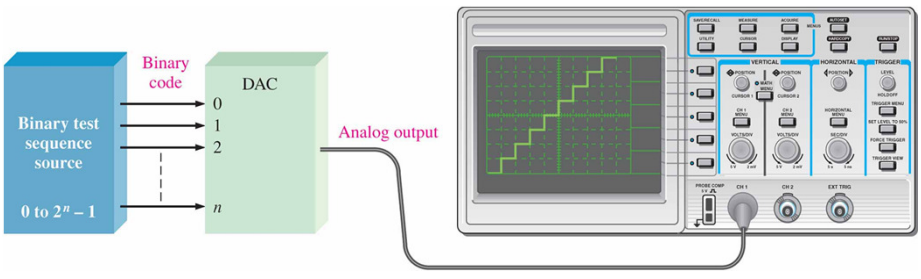
Basic test setup for a DAC.



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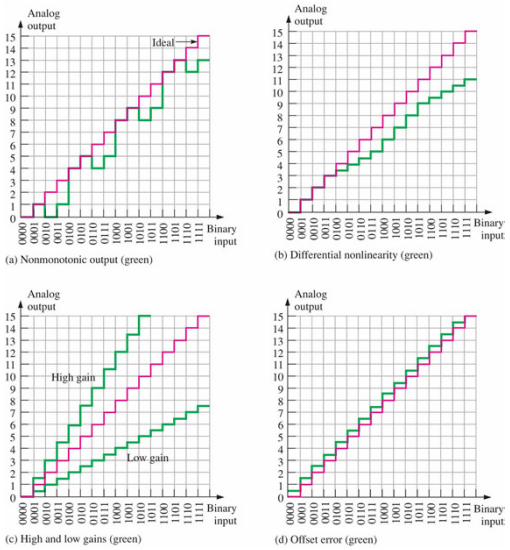
Illustrations of several digital-to-analog conversion errors



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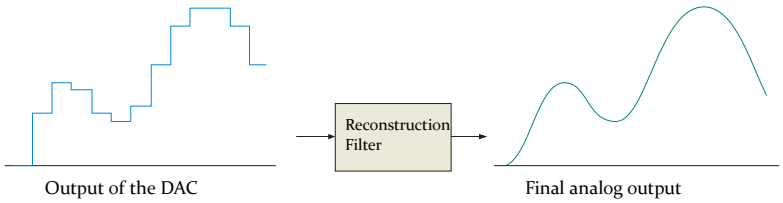
Reconstruction Filter

After converting a digital signal to analog, it is passed through a low-pass "reconstruction filter" to smooth the stair steps in the output.



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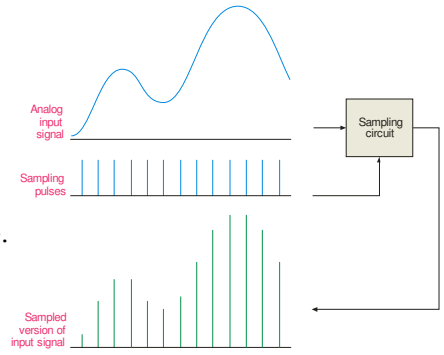
ANALOG TO DIGITAL CONVERTERS

FLASH ADC
DUAL SLOPE ADC
SAR ADC
IC ADC (ADC0804)

Sampling

Most input signals to an electronic system start out as analog signals. For processing, the signal is normally converted to a digital signal by sampling the input.

Before sampling, the analog input must be filtered with a low-pass anti-aliasing filter. The filter eliminates frequencies that exceed a certain limit that is determined by the sampling rate.



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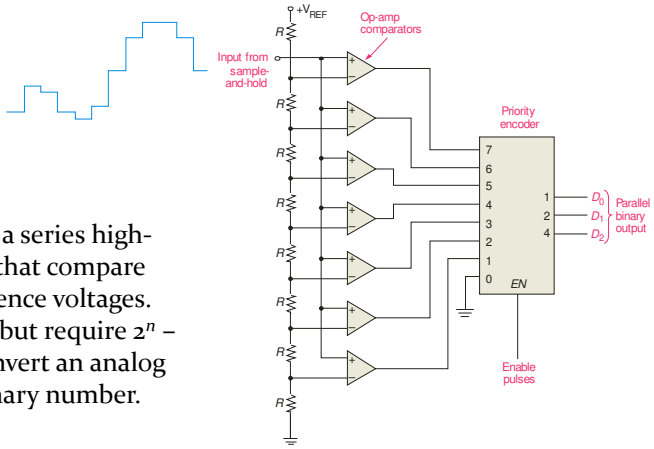
A 3-bit flash ADC

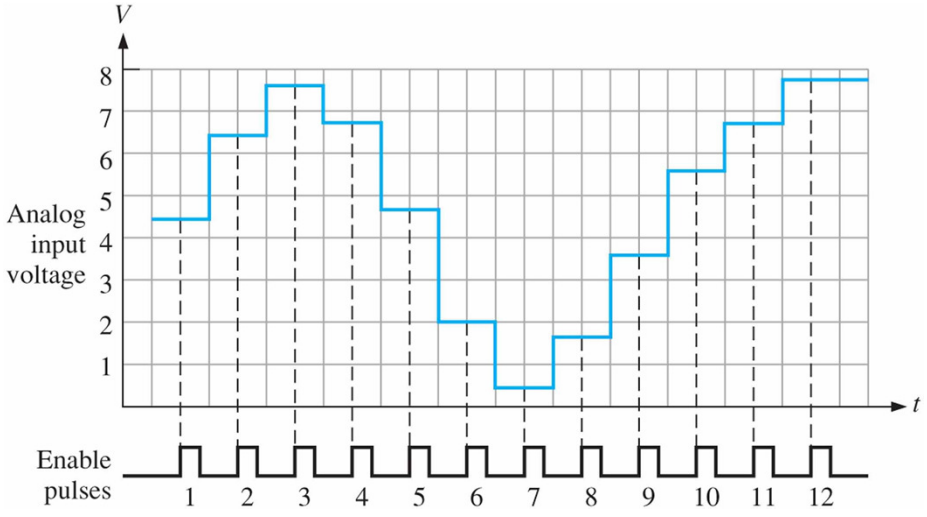


The flash ADC uses a series high-speed comparators that compare the input with reference voltages. Flash ADCs are fast but require $2^n - 1$ comparators to convert an analog input to an n-bit binary number.

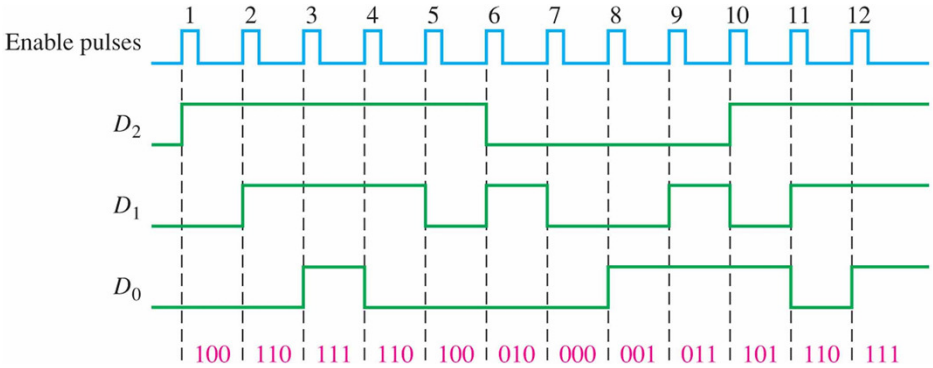
Question How many comparators are needed by a 10-bit flash ADC?

Answer 1023

Sampling of values on a waveform for conversion to binary code.



Resulting digital outputs for sample-and-hold values. Output D_0 is the LSB of the 3-bit binary code.



Basic dual-slope ADC

1. The dual-slope ADC integrates the input voltage for a fixed time while the counter counts to *n*.
2. Control logic switches to the V_{REF} input.
2. A fixed-slope ramp starts from $-V$ as the counter counts. When it reaches 0 V, the counter output is latched.

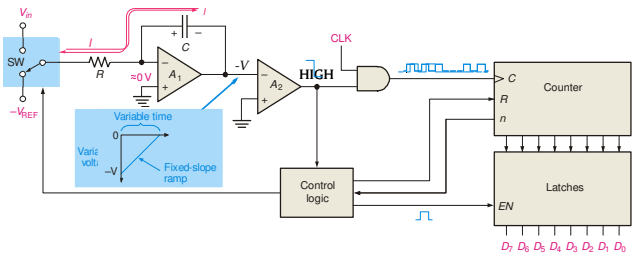
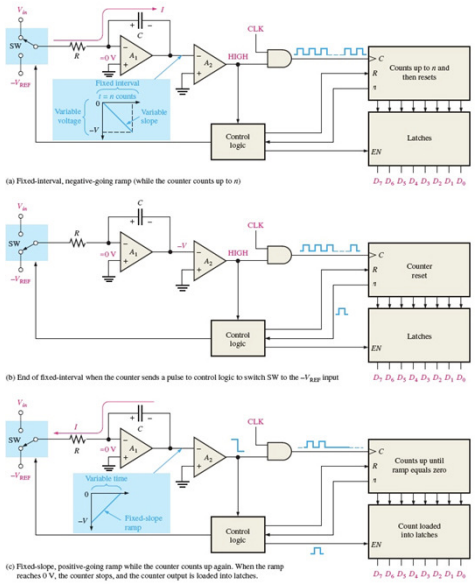


Illustration of dual-slope conversion



(a) Fixed-interval, negative-going ramp (while the counter counts up to n)

(b) End of fixed-interval when the counter sends a pulse to control logic to switch SW to the $-V_{REF}$ input

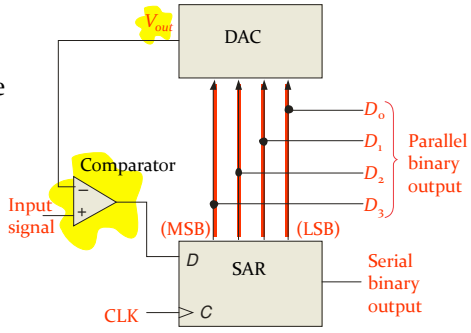
(c) Fixed-slope, positive-going ramp while the counter counts up again. When the ramp reaches 0 V, the counter stops, and the counter output is loaded into latches.

Successive-approximation ADC

1. Starting with the MSB, each bit in the successive approximation register (SAR) is activated and tested by the digital-to-analog converter (DAC).

2. After each test, the DAC produces an output voltage that represents the bit.

3. The comparator compares this voltage with the input signal. If the input is larger, the bit is retained; otherwise it is reset (0).



The method is fast and has a fixed conversion time for all inputs.

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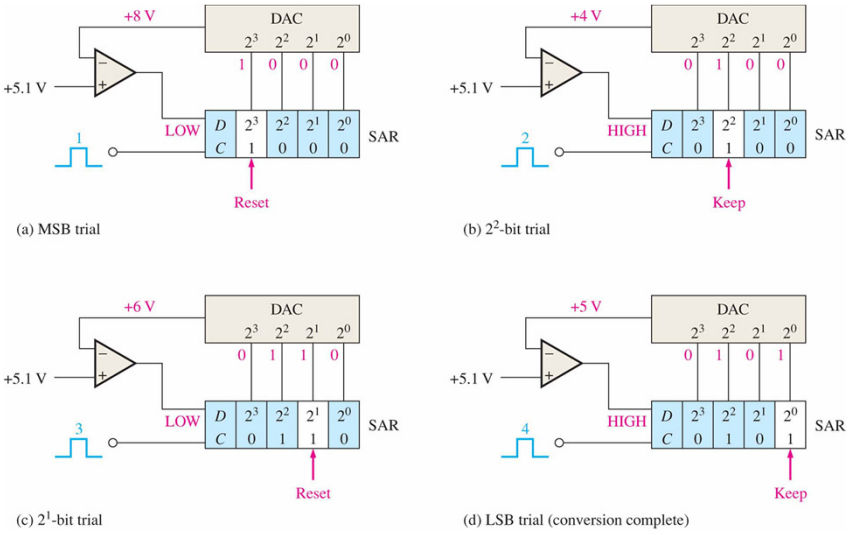
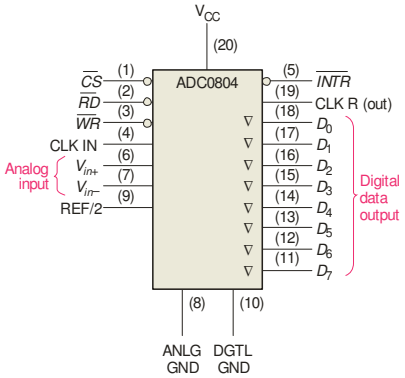
Illustration of the successive-approximation conversion process.



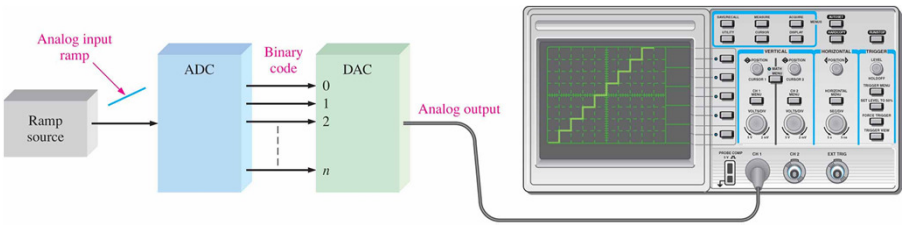
The ADC0804 analog-to-digital converter.

An integrated circuit successive approximation ADC is the ADC804. This popular ADC is an 8-bit converter that completes a conversion in 64 clock periods (100 μs).

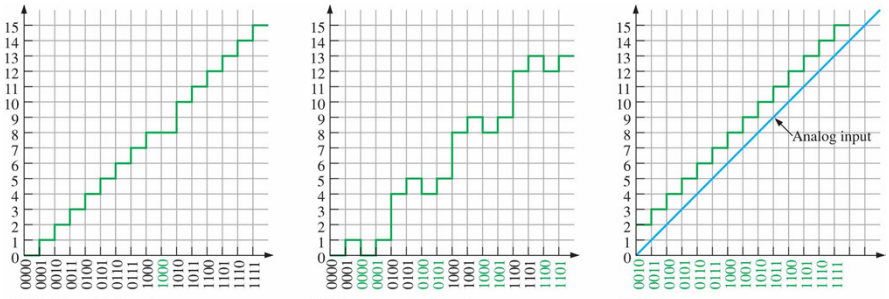


The completion is signaled by the $\overline{INTR}$ line going LOW.

A method for testing ADCs



Illustrations of analog-to-digital conversion errors.



(a) Missing code (green)
(b) Incorrect codes (green)
(c) Offset