FİNAL SORULARI

1. RISC ve CISC mimarilerini karşılaştırınız.
2. EPIC felsefesini açıklayınız.
3. Give information about the RAID architecture. What are the advantages of RAID architecture? (10)
4. Explain how processor level parallelism can be achieved? (10)
5. P4, Sparc III ve 8051 ISA mimarilerini instruction yapısı ve instructionları açısından değerlendirin.
6. Compare Pentium II, Ultra Sparc II and PicoJava architectures in terms of their instruction formats. (10)
7. Explain the purpose of and the methods for branch prediction. (10)
8. Why is a two-pass strategy followed by the assembler? (10)
9. What is the importance of ISA level? (10)
10. Explain the concept 'bus arbitration' and the mechanisms used for bus arbitration in detail. (25)
11. Explain the situations in which Assembly Language is preferred? (10)
12. Pentium-II ve UltraSparc 3 işlemcilerini, CPU Türü(RISC, CISC), bellek kullanılımı ve işlemlerin gerçekleştirildiği bit sayıları konusunda karşılaştırınız.
13. Bilgisayarlar neden seviyeler halinde tasarlanırlar? Bugünkü seviyeli mimari tarihsel olarak nasıl bir süreçten geçerek evrimleşmiştir?
14. Out-of-order ve Register renaming mimarisi neden yapılmıştır?
15. P4 Sparc3 ve Itanium2 işlemcilerini ISA seviyesi yönünden karşılaştırın?
16. What are the advantages of using interpreters over hardware processors. (10)
17. Explain the function of the ISA layer. What considerations should be taken into account when designing the ISA level (10)
18. What are the problems of speculative executions? How can they be solved? (10)
19. Explain how a 3 bus architecture and latches in front of and after ALU unit could improve the performance of MIC-1 architecture. (25)
20. Draw and explain the architecture of a Pentium II bus system. (20)
21. Linker nedir? Başlıca görevleri?
22. What are the possible bindings time for a program? Which possibility is the best. Why? (10)
23. Explain how linkers generate an executable binary program from a collection of independently translated source procedures. (10)
24. Design an expanding opcode to allow all the following to be encoded in a 36-bit instruction: (15)
    - 7 instructions with two 15-bit addresses and one 3 bit register number
    - 500 instructions with one 15-bit address and one 3-bit register number
    - 50 instructions with zero registers
25. List the levels of contemporary machines. Differentiate the levels which use interpretation and translation. (15)
26. İşletim sistemi seviyesinin katmanlı mimarideki yeri ve işletim sistemi seviyesinin temel özelliği nedir?
27. Sembol tablosu nedir? Nasıl oluşturulur? Amacı nedir?

28. Katmanlarla ilgili ve her katman için kısaca açıklama yapınız.
29. Assembly ve yüksek düzeyli dillerden birisi birlikte kullanılarak program geliştirilebilir. Bu ne gibi avantajlar sağlar?
30. Mikromimari seviyesinin görevi nedir? Bu seviyenin karmaşıklığı neye bağlıdır.
31. ISTORE isimli IJVM komutu yığıttan bir kelimeyi(word) çıkararak lokal bir değişkene atar. Bu komutu izleyen bir byte'lık bir operand, yığıtın en üstündeki saklanacağı lokal değişkenin yığıttaki konumunu gösteren + bir değerdir. ISTORE komutuna karşılık gelen mikrokomut dizisini yazınız. Bir örnek üzerinde herbir mikrokomutun nasıl çalıştırıldığını gösteriniz.
32. Explain the following terms: virtual machine, microprogramming, Moore's law. (15)
33. Assume we have a superscalar machine. An instruction is decoded in cycle n and execution starts in cycle n+1. For a simple instruction, such as addition and subtraction, the writeback to destination register occurs at the very end of cycle n+2. For a more complicated instruction such as multiplication, the writeback occurs at cycle n+3. The decoder unit issues up to 2 instructions Per clock cycle. Explain how the following code should be executed using out of order execution and register renaming. (15)

    R3=R0*R1
    R4=R0+R2
    R5=R0+R1
    R6=R1+R4
    R7=R1*R2
    R1=R0-R2
    R3=R3*R1
    R1=R4+R4
34. Compare the levels above and below the Operating System Level in a multilevel machine. (10)
35. What are the design principles for modern Computers? (10)
36. Explain the following terms: assembly process, linking, binding, tuning. (20)

VİZE SORULARI

1. Explain the term virtual machine and why computers are designed in levels. (15)
2. State Moore's law. What is the impact of Moore's law on computer technology. (10)
3. Compare RISC and CICS architectures. (10)
4. Explain how processor level parallelism is achieved in computer systems. (10)
5. Give information about the bus types that are used in computer systems. Draw a diagram that shows the integration of those bus types in a Pentium system. (10)
6. Draw a logical pinout of a generic CPU. Explain briefly the purpose of the pins of a CPU. (15)
7. Explain how the address of the next microinstruction is calculated with Mic-1 architecture? (10)
8. Explain the microinstruction sequence for wcmd instruction given in Listing 1. Some architectural modifications have been performed on Mic-1 and the microinstruction sequence given in Listing 1 has been converted to the microinstruction sequence given in Listing 2. Explain the necessary architectural modifications on Mic-1 to obtain the sequence given in Listing 2. (20)

```
Main 1  PC=PC+1; fetch, goto (MBR)


cmd1    H=LV
cmd2    MAR=MBRU+H
cmd3    MDR=TOS; wr
cmd4    SP=MAR=SP-1;rd
cmd5    PC=PC+1,fetch
```

```
cmd1    MAR=LV+MBR1U
cmd2    MDR=TOS; wr
cmd3    MAR=SP=SP-1;rd
cmd4
cmd5    TOS=MDR; goto (MBR1)


wcmd1 MAR=LV+MBR2U; rd; goto
```

9. Explain the concept of virtual machine. (15)
10. Explain in what sense hardware and software are equivalent and not equivalent. (10)
11. What is the idea behind superscalar architecture? In what circumstances does this architecture become useless? (10)
12. Explain the following terms: striping, SCSI, IDE, UNICODE. (10)
13. Draw and explain the architecture of a bus system consisting of ISA, PCI, USB and SCSI buses. (10)
14. Draw and explain the logical pinout of a generic CPU. (15)
15. What is the function of the microarchitecture level? (5)
16. IJVM instruction ISTORE pops a word from stack and stores it in a local variable. ISTORE has a byte following the opcode. This byte is used as an unsigned index to identify the word in the local variable space to which the value on top of the stack to be stored. List the sequence of microinstructions that correspond to ISTORE operation. Explain the execution of the instruction sequence with an example. (10)

17. Explain the control path of MIC-1 architecture. How is the next address is calculated? (15)