** Design a counter which counts the binary numbers with the sequence 1, 2, 5, 7 and again 1.*

** Design a synchronous counter that counts the sequence 0 ,4 ,8 ,2 ,6 and repeats.*

** A 8-bit binary counter with parallel load facilities, is available as an IC package. Draw the block diagram for the IC, showing all the inputs and outputs clearly. Write the function table, that such a counter may have. Draw the block diagram of a 40-bit binary counter with parallel load constructed with these 8 bit counters.*

** Design a counter that counts between 1 and 24 by using a binary counter with paralel load.*

** Design a counter that counts the sequence 1,6,2,7,4,3,0 and repeats. Is the counter you designed self correcting?*

** Draw the block diagram of a 2 bit shift register with parallel load. The function table for the register is the following:/ 2 bitlik Paralel yüklemeli bir kayıtçının blok diyagramını çiziniz. Kayıtçı için fonksiyon tablosu aşağıdadır:*

Shift	Load	Operation
0	0	No change
0	1	Load paralel data
1	X	Shift down

** Implement the following register transfers by using a) Single bus b)Three-state-bus*

CA: R0 ← R1, R2←R1

CB: R0←R1, R3←R1

CC: R1←R2, R3 ←R2

CD: R2←R0

** Implement the following register transfer operations by using a) single multiplexer b) three-state bus*

C_a: R0← R1, R2←R1
C_b: R1← R0
C_c: R2←R0, R1←R0

** A register may be loaded from 50 registers in the following manner. Draw the block diagram of the hardware that implements these register transers. Your solution will use minimum number of components and the registers will not be connected eachother directly.*

C0: RD←R0
C1: RD←R1
C2: RD←R2
…
…
C49: RD←R49

** Implement the following register transfer operations*

C1 : R1←R1+1
C1'.C2 : R1←R1-R2

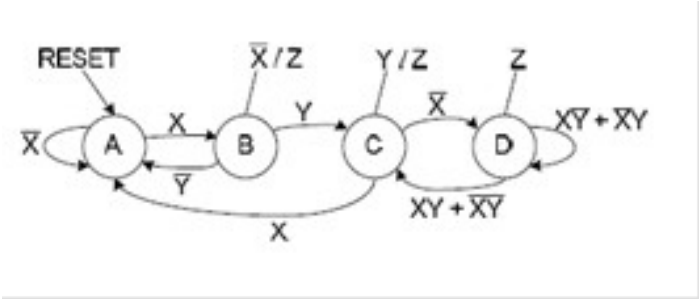
** Implement the following register transfer operations by using registers and dedicated multiplexers method. Only one variable can be equal to 1 at a time.*

C1: R2←R0, R1←R0
C2: R2 ←R1
C3: R1←R2, R0←R1

** By using registers and a single multiplexer, design a system that performs the following register transfers. At most 1 of the control signals among X_0, X_1, X_2 and X_3 can be 1 at any instant. When they are all 0 no loading will be performed at all.*

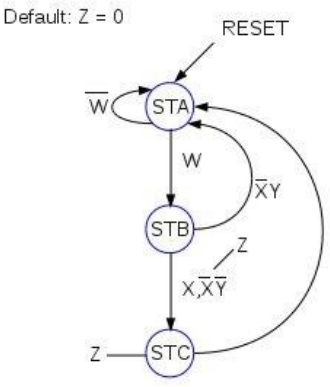
X_0: R4← R0
X_1: R4← R1
X_2: R4← R2
X_3: R4← R3

** Obtain the flip flop input equations and output equations for the control unit with the state machine diagram given below. Use one-hot state method.*

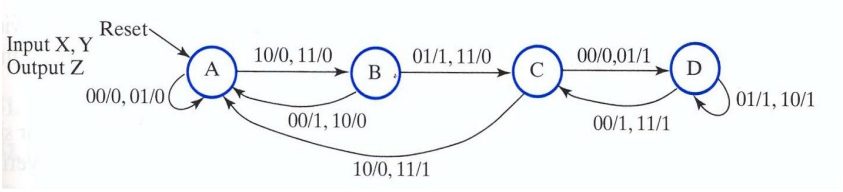


** Find the response for the state machine diagram in the following figure for the following sequence of inputs. (Assume that the initial state is STA). Find the state table for the corresponding circuit*

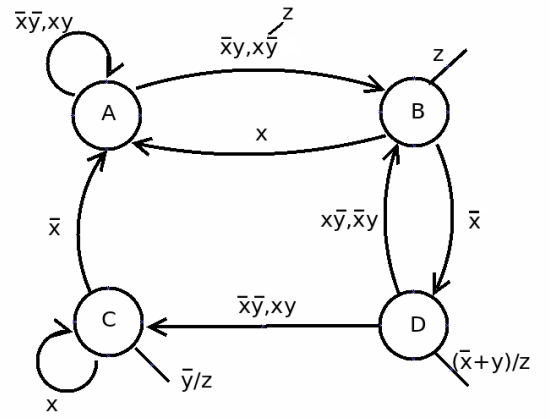
W:	0	1	1	0	1	1	0	1
X:	1	1	0	1	0	1	0	1
Y:	0	1	0	1	0	1	0	1
State:	STA							
Z:								



* *Draw the state machine diagram and state table for the circuit for the following state diagram.*



* *The state machine diagram for a circuit is given below. Obtain the state table for the circuit. Design the control unit hardware. Use one hot state assignment method.*



**What are the differences between static and dynamic RAMs?*

* *For a RAM chip, the width of the address bus is 20 and the width of the data bus is 16 bits. What is the capacity of this RAM?*

* *How many 128Kx8 RAM chips are needed to provide a memory capacity of 2Mx16? How many address and data lines are needed? How many of the address lines are connected to the address inputs of all chips? Show how chip select inputs of the RAM chips are provided?*

* *Construct a 256K x 32 RAM by using 64K x 8 RAM chips and a decoder.*

* *A DRAM with 24 address pins has column adresses 4 bits shorter than its row adress. How many addresses does the DRAM have?*

* *How many 256Kx16 RAM chips are required to obtain a memory of 1Mx32 RAM? Show how CS (chip select) inputs of such a RAM array are obtained by drawing a simple figure.*

* *How many address lines and data lines are needed for a memory of a) 64Kx8 b) 128M x16 and c)2Gx32.*

* *A 256Kx 16 RAM chip uses coincident decoding. The RAM cell array is square. How many decoders are needed? What are the size of the decoder(s)?*

**How many address lines and input-output data lines are needed for the memories 64Kx32 and 4Gx8?*

** A computer system has a main memory with a capacity of 2^{32} bits. Row addresses are 8 bits longer than the column addresses. What is the width of the address bus in this computer system?*

**A 128K x 8 RAM chip uses coincident decoding by splitting the internal decoder into row select and column select. Assuming that the RAM cell array is square, what is the size of each decoder?*

** A DRAM has 16 address pins and its row adress is 2 bits longer than its column address. How many addresses, total, does the DRAM have?*

** Assume that the largest decoder that can be used in an mx1 RAM has 13 address pins and that 'Coincident decoding' is employed. What is the value of m? How many chips are required to obtain a 512 M x 1 RAM?*