** Draw the hardware diagram for the implementation of the following register transfer operations:*

K1.K2 : if (R1< R2) R3←R1
K1.K2' : R3←R1+R2

** Implement the following register transfer operations (a) by using an adder and external gates (b) by using an adder and a 4 bit counter with parallel load*

K1: R1←R1+R2
K1'.K2 : R1←R1+1

** Implement the following transfers bu using (a) Registers and dedicated multiplexers (b) One multiplexer based bus and one direct connection from one register to another instead of dedicated multiplexers. Don't forget to determine LOAD inputs of the registers and the selections of multiplexers.*

K1: R2←R0, R1←R2
K2: R0←R2
K3: R0←R1, R2←R1

** Construct a register that performs the following operations:*

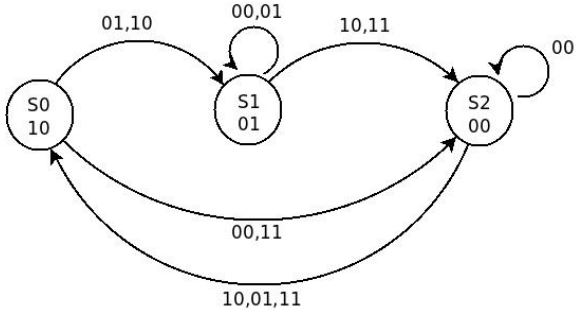
S2	S1	S0	
0	0	0	No change
0	0	1	Load paralel data
0	1	0	Shift up
0	1	1	Shift down
1	0	0	Complement

** Serial output of a 4 bit shift right register is complemented and supplied to the serial input ofthat register. Assume the initial value stored in the register is 0000. Show the followingstates until the register returns to 0000.*

** Design a synchronous counter that counts the sequence 5, 3, 7, 2, 4 and repeats. Is the counter self correcting?*

** Design a counter that counts between 2 and 7 by using a binary counter with parallel load.*

** Draw the state machine diagram and state table for the circuit for the following state diagram.*



** Obtain the flip flop input equations and output equations for the control unit with the state machine diagram given below.*