DATA SHEET

GPY0030C

Audio Driver

Jun 26, 2013

Version 1.1

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AUDIO DRIVER

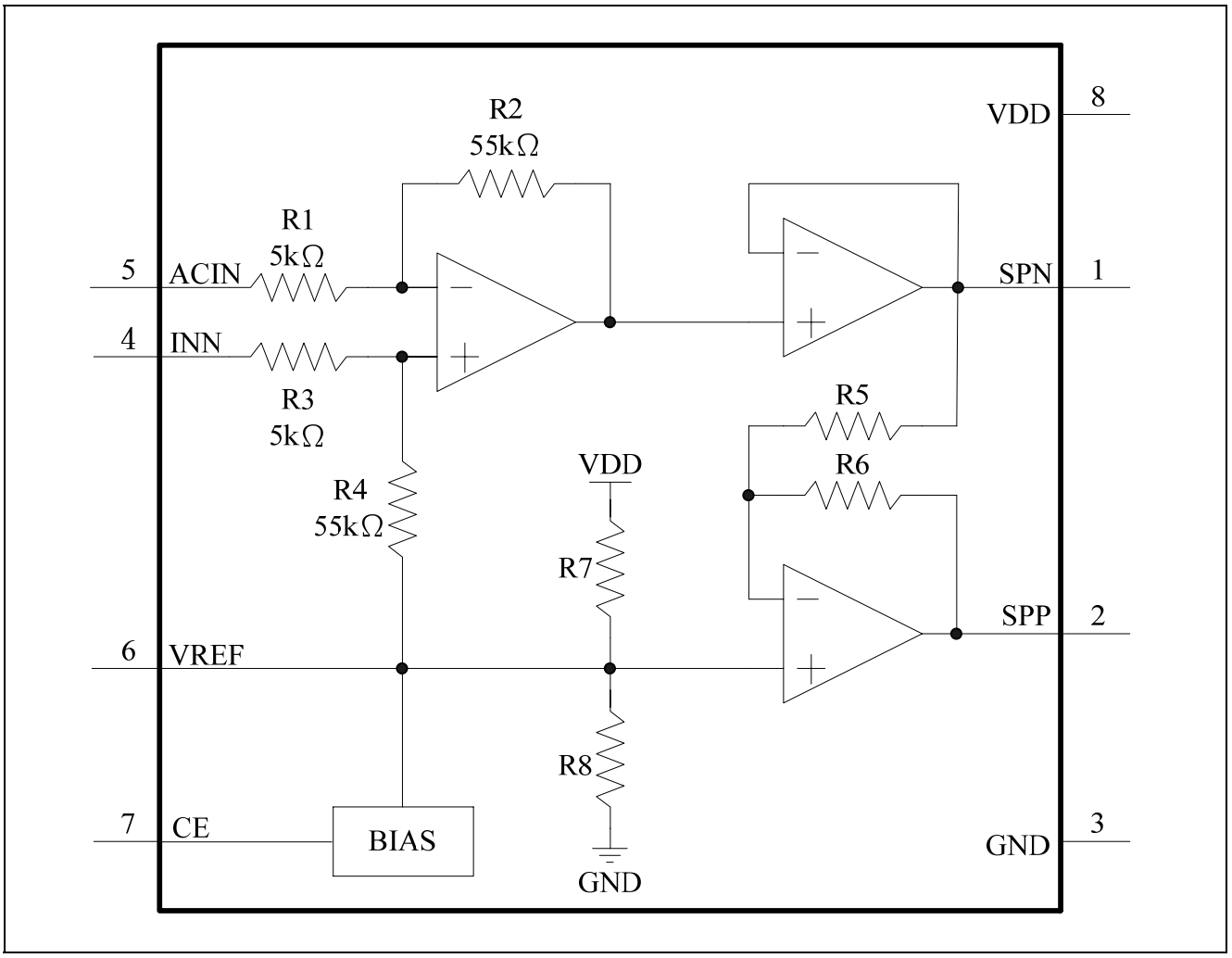
1. GENERAL DESCRIPTION

The GPY0030C is an audio driver whose gain can be adjusted by external resistor (Maximum gain is 20) and embedded the de-pop circuit to minimize the turn-on and turn-off pop noise. Normally, it is applied for GPC series, GPF series, GPL series and other GENERALPLUS products. The GPY0030C is easily to be used in variety of applications and products.

2. FEATURES

- Wide operating range: 2.4V – 6.8V
- Bridge-Tied Load
- Low distortion: THD+N = 0.15% (Typ.)
  (For VDD = 5.0V, R_L = 8.0Ω & P_{out} = 500mW)
- High output power: P_{OUT} = 825mW
  (For VDD = 5.0V, THD+N =1.0%, f =1.0KHz & R_L = 8.0Ω)
- Low standby current: 1.0μA
- Minimize the turn-on and turn-off pop noise

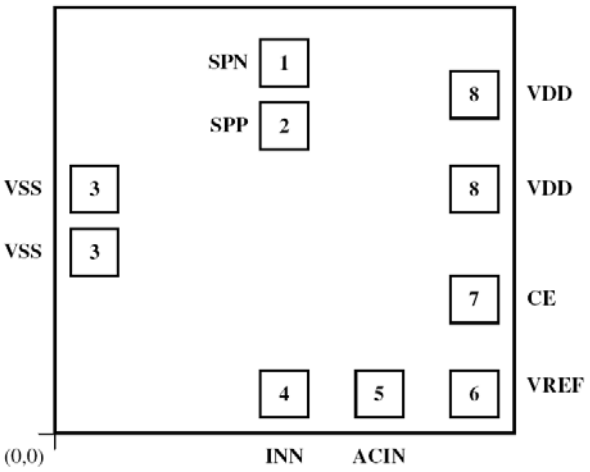
3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description	Electrical Characteristics
SPN	1	O	Audio output negative	-
SPP	2	O	Audio output positive	-
VSS	3	I	Power VSS	-
INN	4	I	Signal input negative	-
ACIN	5	I	Signal input positive	-
VREF	6	O	Reference voltage	VDD/2
CE	7	I	Chip enable	-
VDD	8	I	Power VDD	2.4V - 6.8V

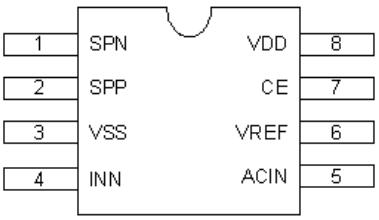
4.1. PAD Assignment



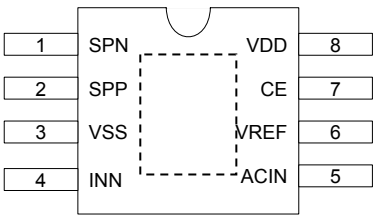
This IC substrate should be connected to VSS

Note: To assure IC operates properly, please bond all of VDD and VSS pins.

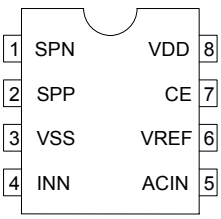
4.2. Package Pin Assignment



SOP-8



SOP-8-P



PDIP-8

= Thermal PAD

(Connected to GND plane for better heat dissipation)

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to + 60℃
Operating junction Temperature Range	T_J	-40℃ to + 150℃
Storage Temperature	T_{STO}	-50℃ to + 150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

5.2. Thermal Characteristics

Characteristics	Symbol	Value	Unit
SOP-8 Package Thermal Resistance	R_{THJA}	160	℃/W
SOP-8-P Package Thermal Resistance	R_{THJA}	60	℃/W
COB Package Thermal Resistance	R_{THJA}	160~200	℃/W
DIP-8 Package Thermal Resistance	R_{THJA}	110	℃/W

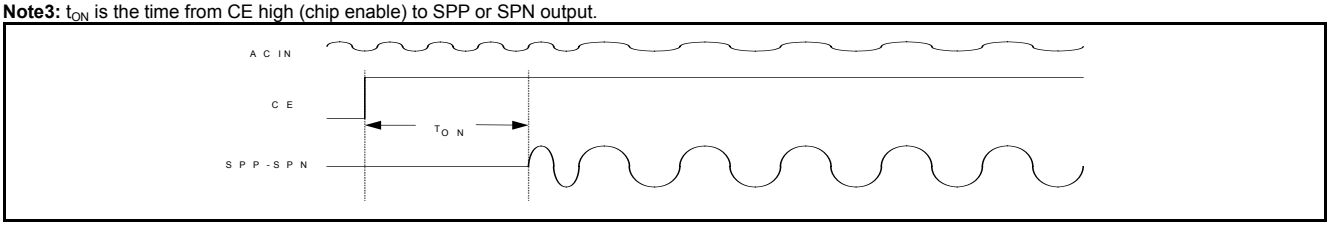
5.3. DC Characteristics (T_A = 25℃)

Item	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Operation Voltage		V_{DD}	2.4	-	6.8	V
Shutdown Current	CE=V_{SS}	I_{STBY}	-	0.1	1.0	uA
Operating Current	V_{DD} = 5.0V, CE=V_{DD}, No Load	I_{DD}	-	2.5	-	mA
Reference Voltage	V_{DD}=5.0V	V_{REF}	-	V_{DD} /2	-	V
Input Resister(CE)	CE=V_{DD}	R_{CE}	-	40	-	kΩ
Input Current(CE)	CE=2.3V at V_{DD}=5.0V	I_{CE}	-	85	-	uA
Total Harmonic Distortion + Noise	V_{DD} = 5.0V, R_L = 8.0Ω, P_{OUT} = 500mW	THD+N	-	0.15	-	%
Output Power (Note2)	V_{DD} = 5.0V, THD+N = 1%, f = 1.0KHz & R_L = 8.0Ω	P_{OUT}	-	825	-	mW
	V_{DD} = 5.0V, THD+N = 10%, f = 1.0KHz & R_L = 8.0Ω	P_{OUT}	-	1000	-	mW
Output Offset Voltage	V_{IN}=0V	V_{OS}	-	30	-	mV
Power Rejection Ratio	f = 1kHz	PSRR	-	70	-	dB
Enable Time	V_{DD} = 5.0V, CIN=1.0uF, CVREF=4.7uF	T_{ON}	-	50	90	ms
	V_{DD} = 5.0V, CIN=1.0uF, CVREF=2.2uF		-	32	60	ms
Shutdown Time	V_{DD} = 5.0V, CIN=1.0uF, CVREF=4.7uF	T_{OFF}	-	40	80	ms
	V_{DD} = 5.0V, CIN=1.0uF, CVREF=2.2uF		-	25	50	ms

Note1: Output power = $(V_{O(PEAK)})^2/2/R_L$; $V_{O(PEAK)}$ = $(V_{I(PEAK)})$*GAIN; So we can get the input range from output power, output loading and audio driver's gain.

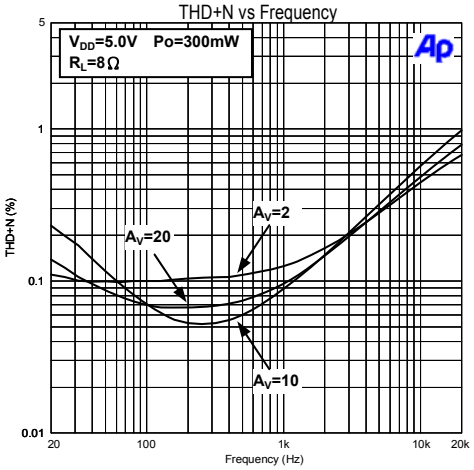
Note2: Proper thermal dissipation must be considered for desired output power and operating voltage. Please refer to Table-2.

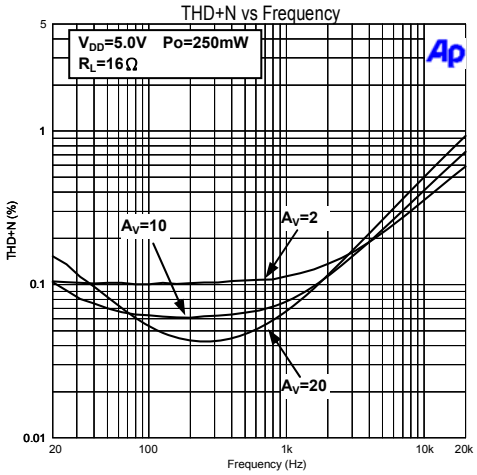
Note3: t_{ON} is the time from CE high (chip enable) to SPP or SPN output.

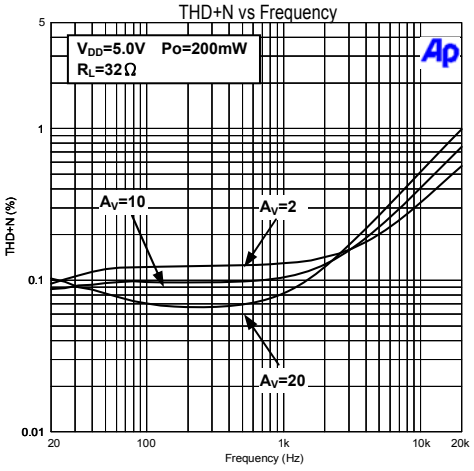


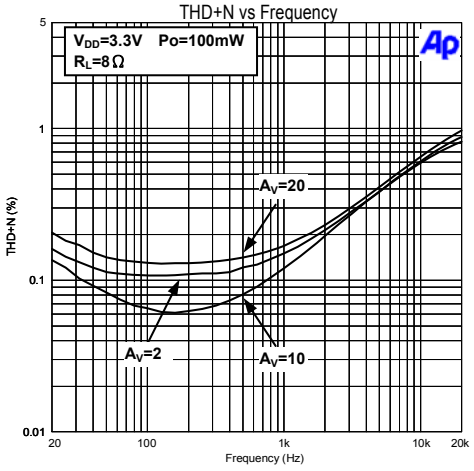
5.4. Typical Performance Characteristics

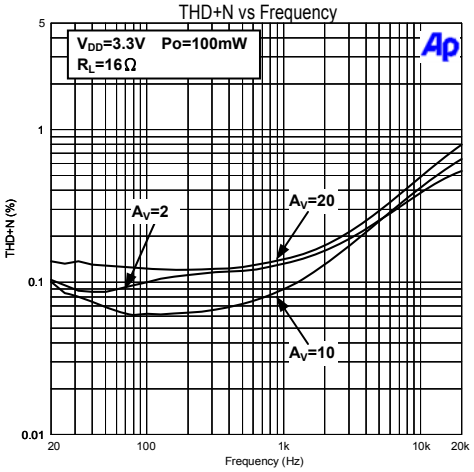
5.4.1. THD+N vs. Frequency

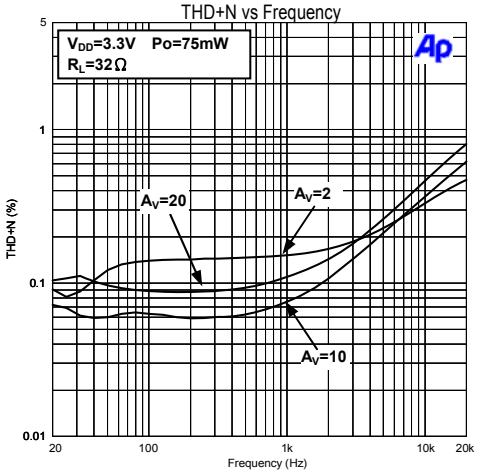




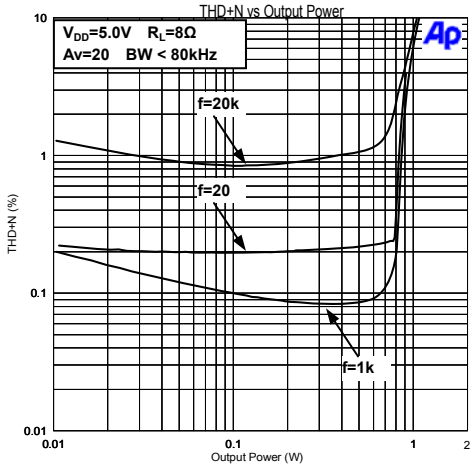


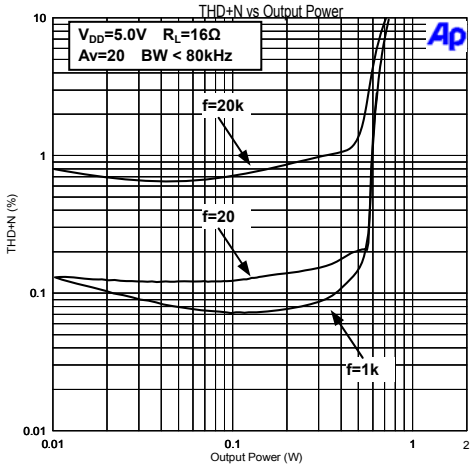


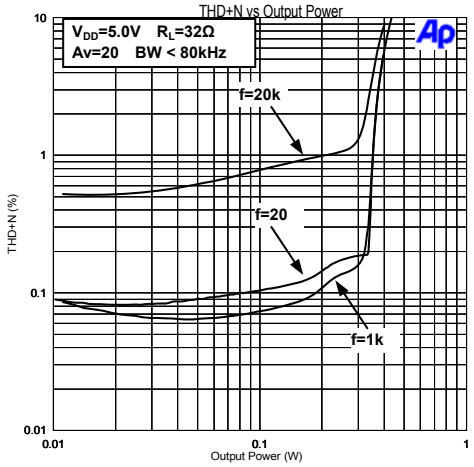


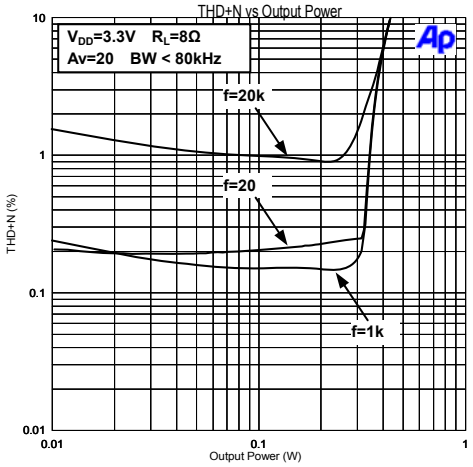


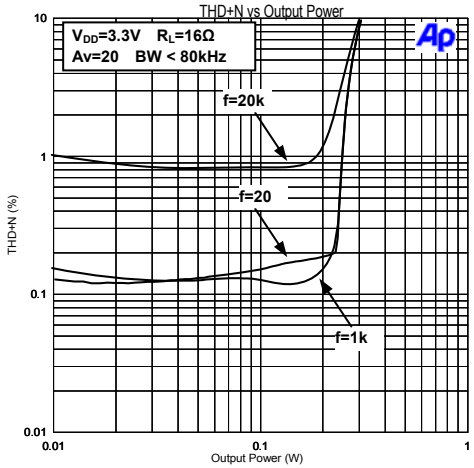
5.4.2. THD+N vs. Output Power

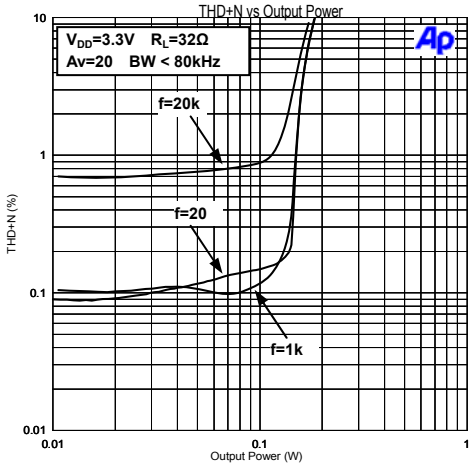




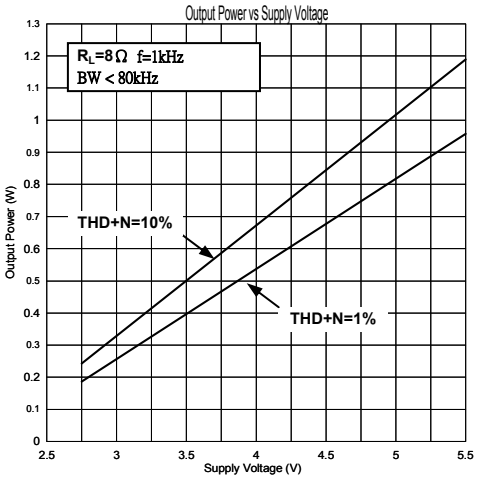


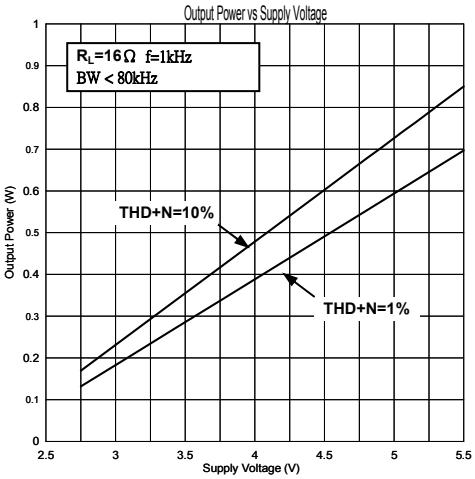


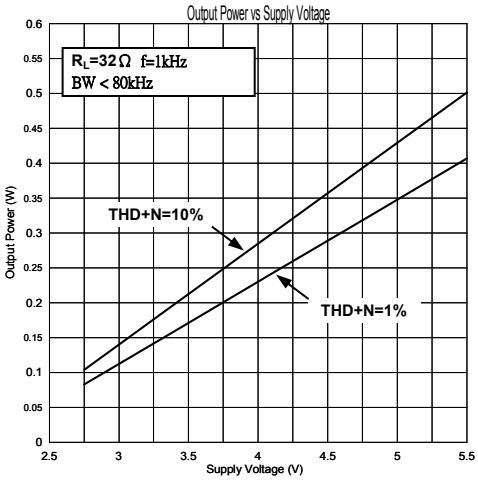




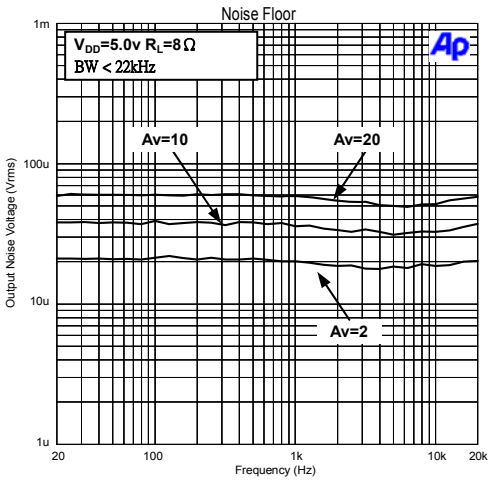
5.4.3. Output Power vs. Supply Voltage

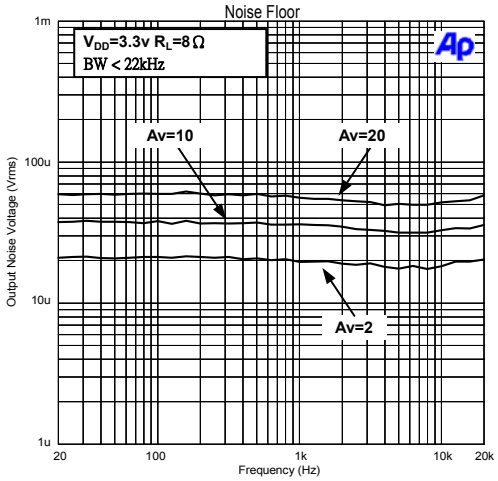






5.4.4. Noise

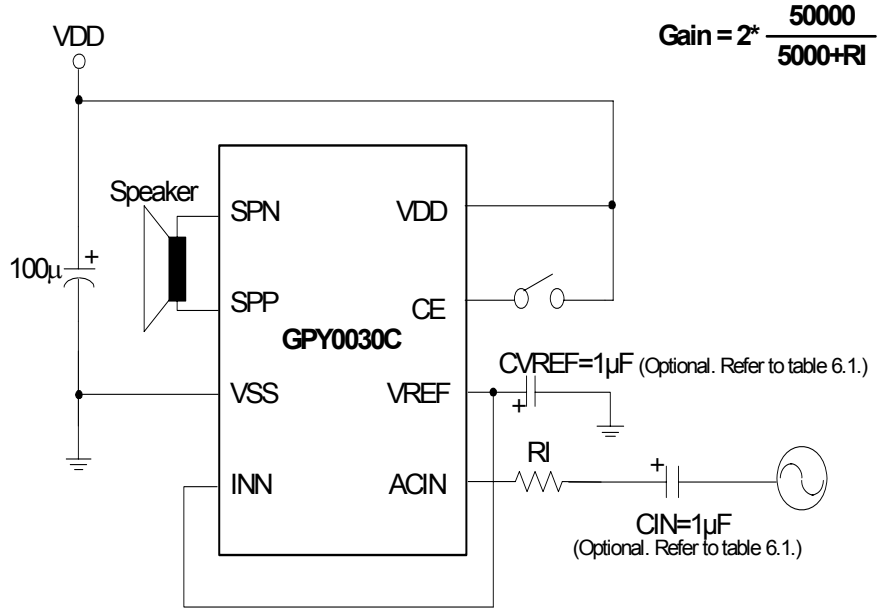




6. APPLICATION CIRCUIT

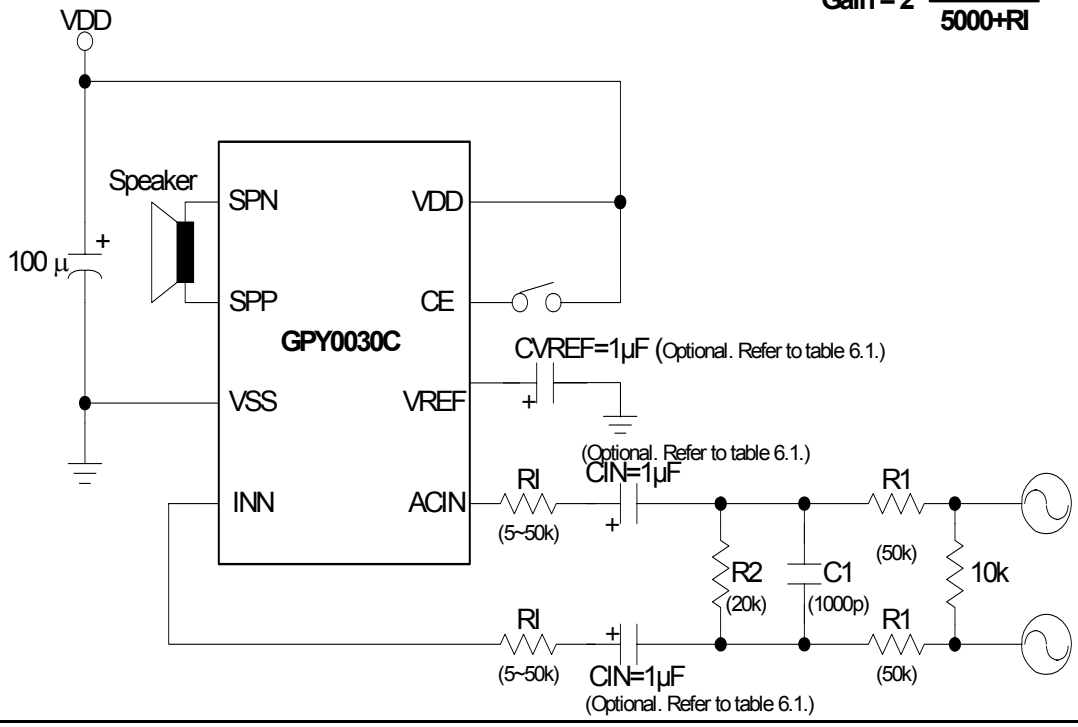
1. Double-end

$$Gain = 2^* \frac{50000}{5000+RI}$$



2.PWM

$$Gain = 2^* \frac{50000}{5000+RI}$$



6.1. BTL Amplifier Efficiency

The following equations are basis for amplifier efficiency calculation.

$$\text{Efficiency} = \frac{\text{Output Power}}{\text{Input Power}} = \frac{P_{OUT}}{P_{SUP}} \quad (1)$$

Where

$$P_{OUT} = \frac{V_{O.RMS}^2}{R_L} = \frac{V_P^2}{2R_L} \quad (2)$$

$$V_{O.RMS} = \frac{V_P^2}{\sqrt{2}} \quad (3)$$

$$P_{SUP} = V_{DD} \times I_{DD.AVG} = V_{DD} \times \frac{2V_P}{\pi R_L} \quad (4)$$

Efficiency of a BTL configuration:

$$\frac{P_{OUT}}{P_{SUP}} = \frac{\pi V_P}{4V_{DD}} \quad (5)$$

$$P_D = P_{SUP} - P_{OUT} \quad (6)$$

Table-1 Efficiency vs. Output Power in 3.3V 8Ω BTL System

P_{OUT} (W)	Efficiency (%)	V_P (V)	P_D (W)
0.125	33.6	1.41	0.26
0.250	47.6	2.00	0.29
0.375	58.3	2.45*	0.28

* High-peak voltage values cause the THD to increase.

6.2. Power Dissipation

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. Equation 7 states the maximum power dissipation point for a single-ended mode operating at a given supply voltage and driving a specified output load.

$$P_{D.MAX} = (V_{DD})^2/(2\pi^2 R_L) \quad \text{Single-Ended (7)}$$

However, a direct consequence of the increased power delivered to the load by bridge amplifier is an increment in internal power dissipation point for a bridge amplifier operating at the same condition.

$$P_{D.MAX} = 4(V_{DD})^2/(2\pi^2 R_L) \quad \text{Bridge-Mode (8)}$$

Since the GPY0030C has two operational amplifiers in one package, the maximum internal power dissipation is four times that of a single-end amplifier. The maximum power dissipation from equation 8 must not be greater than the power dissipation that results from the equation 9.

$$P_{D.MAX} = (T_{J.MAX}-T_J)/\theta_{JA} \quad (9)$$

For SOP-8 package with and without thermal pad, the thermal resistance (θ_{JA}) is equal to 60°C/W and 160°C/W, respectively.

Since the maximum junction temperature ($T_{J.MAX}$) of GPY0030C is 150°C and ambient temperature (T_A) is defined by the power system design, the maximum power dissipation which the IC package is able to handle from equation 9. Once the power dissipation is greater than the maximum limit ($P_{D.MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased, or the θ_{JA} must be reduced with heat-sink.

Example: V_{DD}=6.0V, Load=8Ω, T_A=30°C, GPY0030C SOP-8 without thermal pad (θ_{JA}=160°C/W).

From equation 9:

$P_{D.MAX} = (150-30)/160 = 0.75W < 4(V_{DD})^2/(2\pi^2 R_L) = 0.913W$

Decrease Power Voltage V_{DD} to 5V.

$P_{D.MAX} = (150-30)/160 = 0.75W > 4(V_{DD})^2/(2\pi^2 R_L) = 0.634W$

6.3. Thermal Pad Considerations

The thermal pad must be connected to ground. The package with thermal pad of the GPY0030C requires special attention on thermal design. If the thermal design issues are not properly addressed, the temperature beyond which damage occurs to the GPY0030C (150°C). The GPY0030C may not function or meet expected performance at this temperature.

Thermal pad on the bottom of the GPY0030C should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the GPY0030C junction temperature below maximum junction temperature (150°C).

Table-2 Output Power vs. Junction Temperature in BTL System (T_A=25°C)

Output Power P_{OUT} (W)	Efficiency (%)	Internal Dissipation P_D (W)	Power From Supply P_{SUP} (W)	V_{OUT} Peak-to-Peak V_P (V)	Junction Temperature T_J (°C)			
					SOP-8	SOP-8-P	COB	DIP-8
V_{DD} = 3.3V, Load=8Ω System								
0.25	47.6	0.28	0.53	2.00	69.8	41.8	70.0	55.8
0.4	60.2	0.26	0.66	2.53	66.6	40.6	71.8	53.6
0.55	70.7	0.22	0.77	2.97	60.2	38.2	64.6	49.2
V_{DD} = 5V, Load=8Ω System								
0.5	44.4	0.63	1.13	2.83	125.8	62.8	138.4	94.3
1	62.8	0.59	1.59	4.00	119.4	60.4	131.2	89.9
1.27	70.7	0.52	1.79	4.50	108.2	56.2	118.6	82.2
V_{DD} = 6.8V, Load=8Ω System								
0.15	17.9	0.69	0.84	1.55	135.4	66.4	149.2	100.9
0.75	39.8	1.12	1.87	3.45	**204.2***	92.2	**226.6***	148.2
1.18	50.2	1.17	2.35	4.35	**212.2***	95.2	**235.6***	**153.7***
2.33	70.4	0.98	3.31	6.10	**181.8***	83.8	**201.4***	132.8

*** T_J must be less than $T_{J.MAX}$ (150°C).**

**** $T_J = \theta_{JA} \times P_D + T_A$; θ_{JA}(SOP-8) = 160°C/W ; θ_{JA}(SOP-8-P) = 60°C/W ; θ_{JA}(COB) = 180°C/W ; θ_{JA}(DIP-8) = 110°C/W**

7. PACKAGE/PAD LOCATIONS

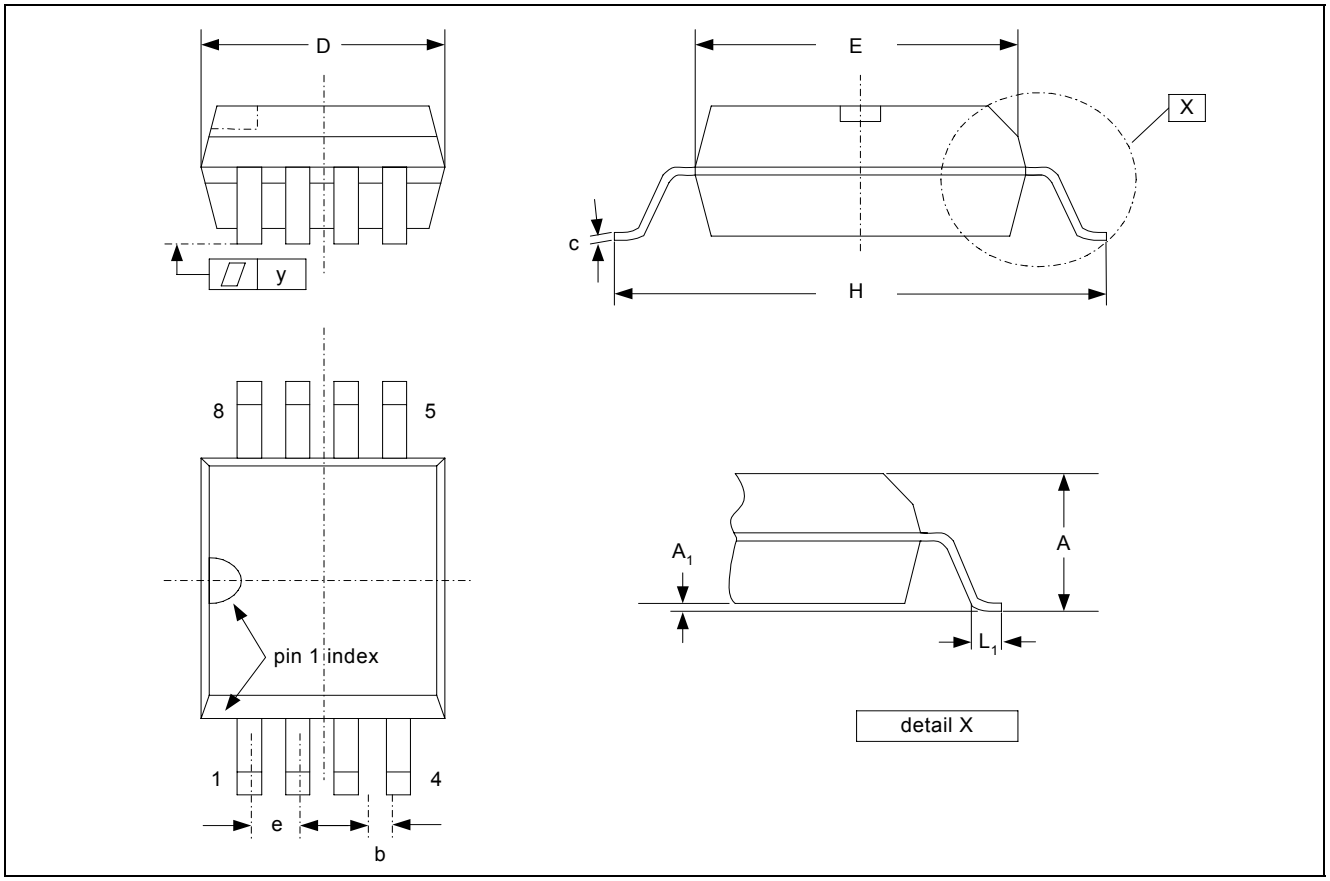
7.1. Ordering Information

Product Number	Package Type
GPY0030C - C	Chip form
GPY0030C - HS01x	Green Package – SOP-8 (150mil)
GPY0030C - HS14x	Green Package – SOP-8-P With Thermal PAD (150mil)
GPY0030C - HD01x	Green Package – PDIP-8 (300mil)

Note: Package form number (x = 1 - 9, serial number).

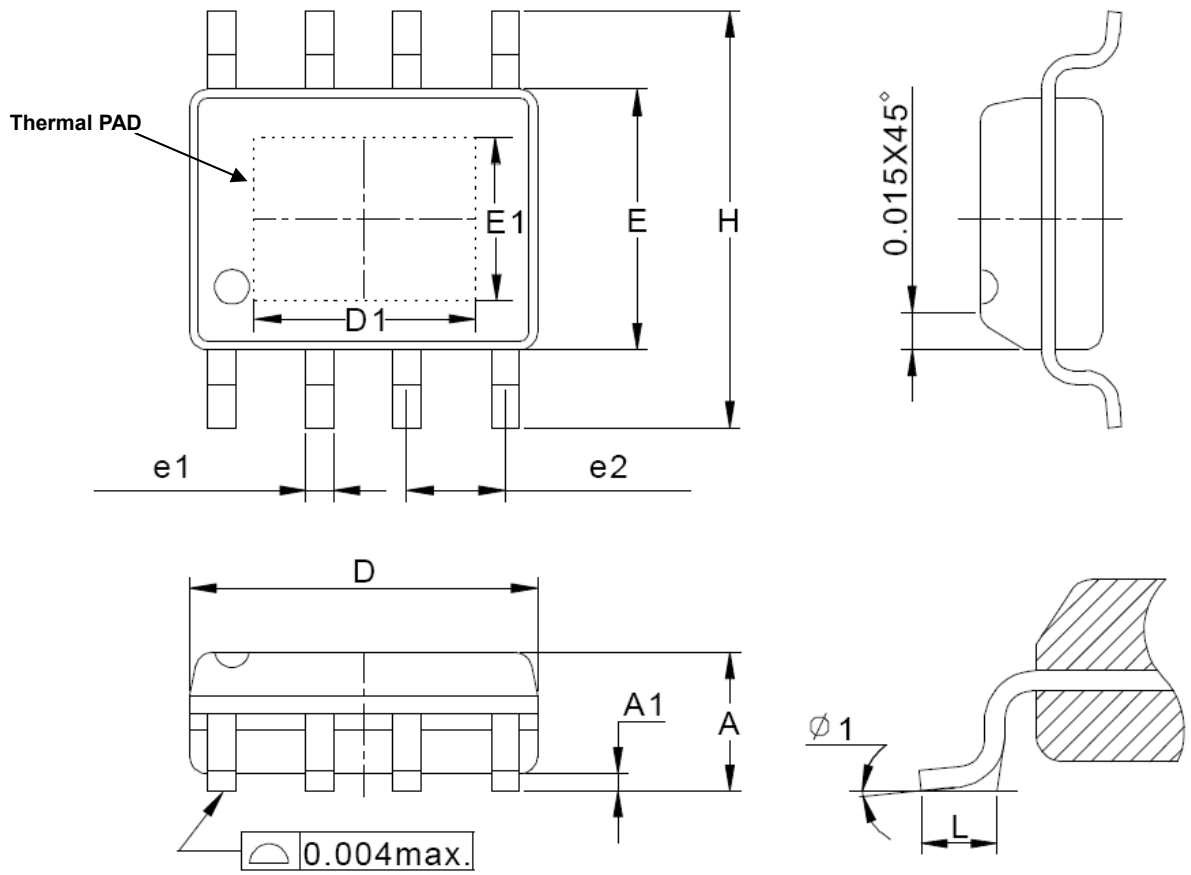
7.2. Package Information

7.2.1. SOP-8



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	0.053	-	0.069
A_1	0.004	-	0.010
b	-	0.016	-
D	0.189	-	0.196
E	0.150	-	0.157
e	-	0.050	-
H	0.228	-	0.244
L_1	0.016	-	0.050
y	-	-	0.004

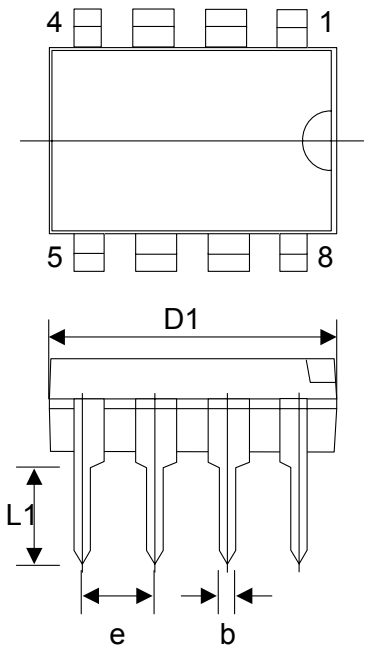
7.2.2. SOP-8-P

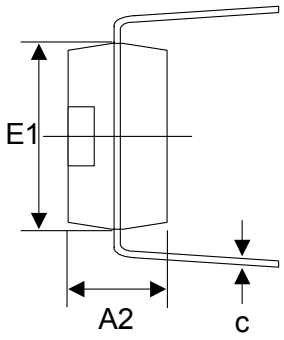


UNIT: INCH

Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	0.053	-	0.067
A1	0.000	-	0.006
D	0.189		0.196
D1	0.077	-	0.090
E	0.150	-	0.157
E1	0.077	-	0.090
H	0.228	-	0.244
L	0.016	-	0.050
e1	-	0.016	-
e2	-	0.050	-
Φ1	8°		

7.2.3. PDIP-8





Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
374±10	250±4	130±5	130±15	18±2	10Typ	100Typ

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-8-300

8. DISCLAIMER

The information appearing in this publication is believed to be accurate.

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9. REVISION HISTORY

Date	Revision #	Description	Page
Jun. 26, 2013	1.1	Modify 7.1 Ordering Information.	12
Mar. 12, 2013	1.0	Modify section 6.3.	16
Oct 11, 2012	0.1	Original	16