Proceedings of the American Control Conference
Arlington, VA June 25-27, 2001

Automatic Gain Control ASIC for MEMS Gyro Applications

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Abstract. Vibratory gyroscopes exploit a coriolis force coupling between two degrees of freedom internal to the sensor for detection of the sensor's angular rotation rate. Vibratory gyroscopes provide ubiquitous opportunities for local feedback compensation to achieve harmonic excitation of selected modes, disturbance rejection, and tuning of the sensor's dynamics. This paper describes the design and preliminary testing of an application specific integrated circuit (ASIC) that performs some of these control tasks in addition to the signal demodulation required for the detection of the rate-induced response.

1. Introduction

The basic equations of motion for a vibratory gyro consist of two coupled oscillators

$$M\ddot{x} + \Omega S\dot{x} + D\dot{x} + Kx = F,$$

where M, D, and K are 2×2 positive definite inertia, damping, and stiffness matrices, respectively. The angular velocity of the sensor is denoted by Ω and S is a skew symmetric matrix. Electronic pick-offs that detect motion of the sensor's elastic structure define the coordinates, x, in which the equations of motion are written. Forces are applied through the 2×1 vector F. Let $x = [x_1 \quad x_2]^T$. Two common control tasks in vibratory gyroscopes are the excitation of x_1 to a constant-amplitude sinusoidal response, and the regulation of x_2 to zero. The first task achieved with a *drive loop* control, and the second task with a *sense rebalance loop*. In this scheme, an angular rotation rate of the sensor produces a sinusoidal sense loop restoring force at the drive loop frequency and whose amplitude is proportional to Ω. Detection of Ω is accomplished by demodulating the sense rebalance loop signal with a measurement of the drive loop response (x_1). Thus, in addition to the two primary feedback control loops, there are other signal processing tasks to perform in vibratory gyros. The paper by Lynch [1] provides good generic background on vibratory gyro principles.

This paper describes our design of an ASIC that implements the drive loop control, sense rebalance loop, and signal demodulation, and thus provides a single, compact, low-power control and signal processing solution. This ASIC was developed for use with the Jet Propulsion Laboratory (JPL) microgyro [4,5,6] and is currently being integrated with this sensor for final system-level testing.

The JPL microgyro is a silicon MEMS sensor and its current design, fabrication and packaging method produce slight sensitivity of sensor properties, such as sensor modal frequencies, to temperature. Therefore it is desirable to use a drive loop control method that can track small shifts in modal frequency. This may be accomplished in several ways, but a variant of *automatic gain control* (AGC) has shown promise in experiments. The AGC has already been successfully implemented using standard analog circuitry [4] and, more recently, we have reported a commercial DSP solution [2,3]. The analog circuit AGC represents an relatively efficient, yet inflexible, solution whereas the DSP implementation provides a powerful, but power-inefficient, computational platform. The ASIC retains the computational advantages of the DSP since general filters may be implemented for control and signal processing purposes, however, its power consumption is very low.

The idea underlying the AGC is simple: an estimate of the velocity of the mode that selected for excitation is fed back to "actuators" which drive that mode. The sign and gain of the velocity measurement is used to add energy (i.e., destabilize) or dampen the modal response until the desired amplitude is attained. In its simplest incarnation the AGC uses a rectifier and filter for signal amplitude detection, a comparator for generation of an error signal, a proportional-integrator block to drive the amplitude error to zero, and a multiplier to adjust the velocity feedback gain. In real sensors, however, there are other degrees of freedom that may be excited by the AGC unless care is taken to

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shape the loop phase properly. Our rigorous stability and performance analysis of the JPL microgyro with a DEC Alpha/DSP implementation of the AGC are reported in [3].

2. ASIC details

The current DSP implementation, however, is not a long-term solution because large power requirements (several watts), inherited from the general-purpose floating-point architecture, prevents its use in missions such as interplanetary spacecraft navigation. To address this shortcoming and to retain the flexibility of an all-digital architecture that permits effortless reconfiguration of control filters and customization for a wide variety of sensor prototypes, we have completed the design and fabrication of an application specific integrated circuit (ASIC) for use with the JPL microgyro.

The ASIC block diagram is shown in Figure 1. In this figure, K_1 through K_8 represent programmable gains, and the FIR blocks are fully programmable 128-tap finite impulse response filters (all computations are fixed precision). The A and B input channels represent the two 18-bit precision sensing pick-off signals that measure deflections of the proof mass in the JPL sensor. These measurements are blended to isolate the drive mode and the sense mode into the upper and lower signal paths, respectively, in Figure 1. The drive loop phase is shaped by FIR1. Tracing out the top portion of the diagram shows that the drive mode signal is rectified and passed through a low-pass filter (FIR2) to produce an estimate of the drive mode response amplitude. Next, the error signal is produced after comparison with the programmable reference level, R. The PI controller output modulates the drive mode signal until the amplitude error is zeroed. The PI controller unit has built-in programmable limiters. The modulated drive signal is then appropriately split using K_3 and K_4 so that the drive signal is applied only to the drive mode.

The sense mode measurement is processed through the lower section of the signal path in Figure 1. The phase of this measurement is adjusted by FIR3 and mixed with the drive loop output after scaling by K_7 and K_8. The gains K_1 through K_8 are merely static input-output scales that roughly diagonalize the microgyro transfer function such that the drive mode and sense mode represent different I/O channels. FIR3 is designed so that the sense rebalance loop is essentially a high-gain velocity feedback loop that nulls the sense mode measurement. The sense mode feedback signal (the post-FIR3 signal) contains the so-called *in-phase* and *quadrature* signals from which the sensor rate can be detected. The quadrature and in-phase terms are separated using phase sensitive detection: the drive mode feedback signal is demodulated with respect to the drive mode measurement and a 90°-phase shifted (performed by FIR5) copy of this signal. FIR6 and FIR7 are low-pass filters whose outputs are the demodulated in-phase and quadrature terms, respectively.

Other selected features of the chip in addition to the programmable, variable-length FIR filters and the programmable scaling factors are: 18 bit input/output data precision; 22 bit internal data precision; a bit-serial, asynchronous external interface; 18 bit coefficient precision; 20 bit internal data precision; and 24 bit data precision in the accumulator (integrator).

The ASIC design was fabricated in November 2000 by MOSIS. The final physical implementation details are listed in Table 1. The layout is shown in Figure 2, and the final packaged ASIC is shown next to the JPL microgyro in Figure 3. Preliminary testing was performed on the ASIC to determine power consumption and clock speed versus the core voltage. These results are presented in Table 2 and Figure 5. Figure 5 is interpreted in the following manner: select a voltage level for the core; of the two graphs on the figure, the uppermost graph defines the fastest clock speed at with ASIC can run (use the y-scale on the left hand side of the graph); the lower graph defines the power consumption in μW per FIR tap per servo loop frequency in kHz. Thus, if the chip is run at 2.5 V, the maximum clock rate, which defines the speed of the multiplies in the FIRs, is about 37 MHz. Since each FIR filter has its own multiplier, the maximal length computation path consists of three FIR filters, each with 128 coefficients (for example, FIR3 must finish computing before its output is processed by FIR4, FIR4 must finish computing before its output is processed by FIR6, etc.). Thus, the maximum servo rate, as defined by the heaviest computational burden, is 96 kHz at core voltage of 2.5V. This is well above the 25 kHz used in the DSP implementation. The power consumption is determined using the lower graph in Figure 5 (right-hand y-scale). In the scenario where 128 coefficients are required in all seven FIR filters, the power consumption of the chip running at a 25 kHz servo rate is an incredibly low 7 mW (2.5 V

core supply). This value is several orders of magnitude below that of commercial digital signal processors.

Final performance results and power requirements will be reported when integration of the ASIC and JPL microgyro is completed.

Acknowledgements: The authors gratefully acknowledge the technical support of Professor Babak Daneshrad (UCLA) and Dorian Challoner (Boeing Satellite Systems).

References:

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Name	Value	Units
Technology	0.25	μm
Power Supply	< 2.5	V
Core Area	2.8	mm^2
Die Area	6.67	mm^2
Inputs/Outputs	20	
Power pins	8	
System Gates	26,000	
Transistor Count	650,000	

Table 1. Physical implementation details of the ASIC

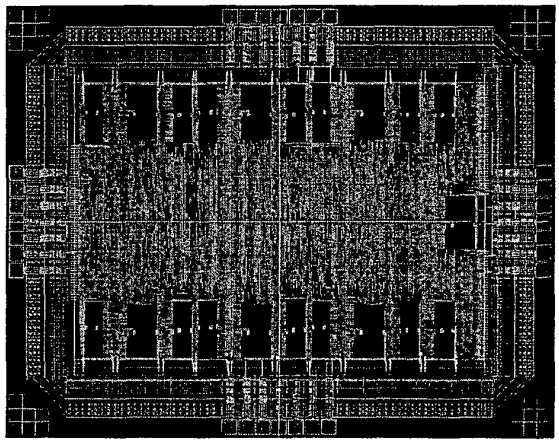

Figure 2. Final layout

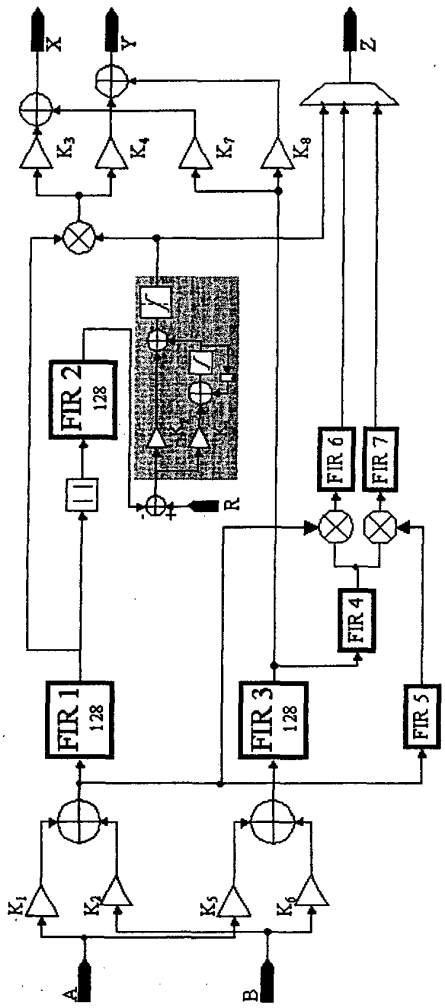

Figure 1. Block diagram of the μgyro ASIC

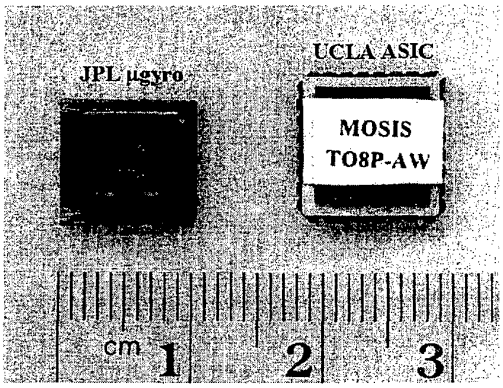

Figure 3. JPL microgyro (left) and the ASIC in its 28 pin LCC package

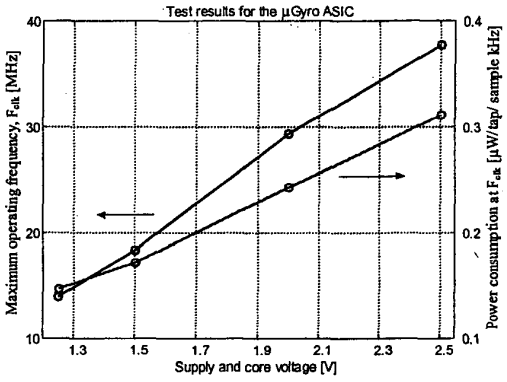

Figure 4. Speed and power measurements on the ASIC

Parameter	Symbol	Conditions	min	Typ	max	Units
Power Supply IO	PVDD		1.25		2.5	V
Power Supply CORE	CVDD	CVDD ≤ PVDD	1.25		2.5	V
Power Dissipation IO	P_{IO}	VDD=2.5V		0.13		μW/tap/ kHz
Power Dissipation CORE	P_{CORE}			0.18		
Input High Voltage	V_{IH}		PVDD			V
Input Low Voltage	V_{IL}		0			V
Master Clock Frequency	F_{CLK}	VDD=2.5V	0		37	MHz
Interface Clock Frequency	F_{CLK_INT}		≤ $F_{CLK}/2$			MHz
Supply at F_{CLK}=20MHz	VDD		1.6			V

Table 2. Tested electrical characteristics