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FPGA-Based Advanced Digital Signal Inspector for Internal Signals of Pin-limited Systems-on-Package

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Abstract - **The paper presents an Advanced Digital Signal Inspector (ADSI) used for acquisition and analysis of the internal digital of a System on Package (SoP) with a limited number of pins. The system is made of a commercial FPGA-board, connected to the module for data sampling and controlled by PC via USB; a suited graphical interface allows for configuration, multi trace real time data display and post processing. The proposed platform can be used to extract and monitor simultaneously up to 4 digital signals, and an ADC is used to monitor one additional analog signal. The ADSI has been successfully applied for the characterization of an automotive SoP based on a MEM gyro sensor interfaced to an ASIC for proper signal conditioning. The ADC was connected to an external accelerometer to evaluate the module behaviour when applying mechanical shocks.**

I. Introduction

Many automotive smart modules are based on complex systems where a sensor [1-4] (accelerometer, pressure, position, velocity, flow to name but a few) is interfaced to electronic circuitry for driving and signal conditioning. An effective cost reduction, together with area and power consumption, is achieved when the circuitry is represented by a System-on-Chip (SoC) with enough computational power and flexibility in order to manage low-cost and low-performance sensors [5]. Additional benefits in terms of reliability, costs and yield are obtained by technology means: Micro Electro Mechanical (MEM) sensors assembled together with the ASIC in the same package (System-on-Package SoP) represent a prominent approach. Despite the above mentioned advantages, the verification and characterization phases of such a module are very critical: from one side the automotive applications require that the module withstands mechanical, thermal and electromagnetic stresses. This means that a proper inspection of the internal signals is needed to analyze transients, noise and disturbance values in the critical nodes, especially where digital processing takes place (this helps also the identification of the best set of configurable system parameters). On the other side, the access to the internal digital busses is limited by the pin availability of the package, which usually hosts the minimum number of wires for its functionality. After this introduction Section 2 briefly compares the state of art and the requirements. Section 3 presents the architecture of the proposed ADSI. The graphical interface to control the ADSI is discussed in Section 4. Experimental results are discussed in Section 5 and finally, conclusions are drawn in Section 6.

II. Requirements and State of Art

Nowadays, for digital systems realized on FPGA the use of ICE (In-Circuit Emulator) is widespread. This means that the VHDL code includes a module able to emulate the microcontroller; this solution allows monitoring, for debugging, all signals available to the microcontroller.

Several kinds of ICE are available on the market and RealView MultiICE [6] is just an example. This product allows executing a real-time emulation interacting with the registers and the memories. The user can set breakpoints selecting the trigger events for starting and stopping analysis. A graphic interface running on Microsoft Windows provides to the extracted data using a parallel communication. The main limitation of RealView MultiICE, and generally of all the ICEs, is that they can debug only the digital signal of the microcontroller. This solution differs from the company target, where the most relevant info is localized in Digital Signal Processing blocks, as well as in the status registers.

The solution generally used for these types of systems is the implementation in the chip of a probing unit that intercepts the internal signals and makes them accessible through dedicated pins. Temento Systems DiaLite [7], MAMon developed by Mälardalen University of Västeras (Sweden) [8] and Serial Wire Debug provided by ARM [6], are three examples of this solution.

DiaLite is a tool used to verify and debug ASIC, SoC and complex FPGA. The chip includes a block (or IP, Intellectual Property) that brings out the signals and provides three different application modes:

- external trigger;
- external RAM for data storage;
- display of signals using external instrumentation.

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MAMon is a monitoring system that can both monitor the logic-level and the system-level in single/multiprocessor SoCs. A small hardware, called Probe Unit, is integrated in the SoC design and connects to a host-based monitoring tool environment via parallel port. The Probe unit collects all events in the system under test in run-time and timestamps them with a resolution of 1µs. The events are then stored in a database on the host for further processing. The event detector is made of a multiplexer connected to the available internal signals and a comparator; a MMU (Memory Management Unit) manages the data storing in an external or internal RAM.

This approach is interesting but doesn't match the company requirements since the use of an external RAM needs a considerable number of pins, while the internal one is not suited for high-volume (it is not a part of functional mode with a cost on area occupancy); moreover the high time resolution could be deprecated if compared with value of DSP sampling frequency in the range of 30-50kHz for the in-house SoP systems. Finally, the hardwired list observed signals, featured by both MAMon and DiaLite, might represent a limitation in case different tests, and hence accessed signals, are required. Serial Wire Debug should represent the better solution for our needing since it uses just two pins but this approach appears to be overestimated in terms of silicon area and capabilities: several functionalities in fact are not needed here such as bidirectional communication.

The Advanced Digital Signal Inspector (ADSI) proposed in this paper is suited to observe the internal digital signals of a complex SoP by using only two pins. This is achieved implementing a simple block in the chip and connecting it to the external hardware ADSI, which is configurable by PC with a user-friendly graphical interface (see Fig.1).

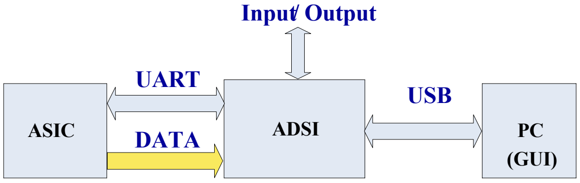


Fig. 1. The connection between ADSI, ASIC and PC.

The connection between ASIC and ADSI can also foresee further wires, the ones used by the ASIC during the normal functioning mode (such as standard UART), just to simplify the connections, while the PC and the ADSI can be connected by an USB cable, which is a common standard nowadays. The ADSI is also directly interfaced with the user by several leds and push buttons to control end check the basic functionalities of the architecture.

The proposed ADSI is referred as "Advanced" because, with respect to a previous version limited to SoP-related signals only, it is able to acquire and perform analysis on one analog signal by using a dedicated ADC [9].

III. Architecture and Implementation of ADSI

The proposed architecture consists of two hardware parts, APB Digital Monitoring Unit and ADSI as shown in Fig. 2.

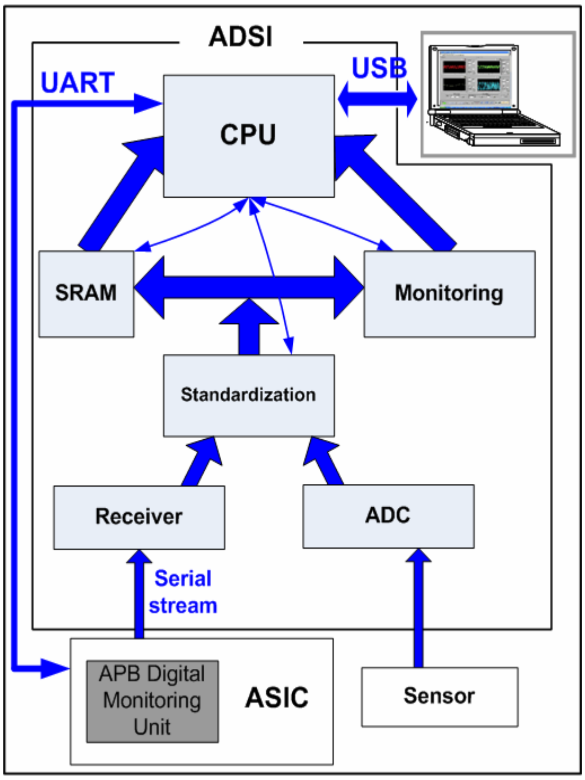


Fig. 2. Implemented connection between FPGA and DUT.

The APB Digital Monitoring Unit is a module implemented in the ASIC which can intercept the signals of every IP plugged in the AMBA-APB bus and serially transfers up to 8 channels in a 32-bit format. The complexity of such a block is limited (<1k equivalent gate) since the AMBA core is already present for other purposes.

All these channels can be read from the external ADSI by using only two pins, clock and data-stream, which implements a simple communication made of start-of-frame – message – end-of-frame.

The ADSI hardware is FPGA-based, and consists of a customized CPU8051 which controls five units: Receiver, Standardization block, Monitoring block, SRAM controller and ADC.

The receiver block inside ADSI receives the stream and parallelizes the data. The generic channel represents a signal coded in 2's complement, module with sign, unsigned or status register; moreover it can be represented on a different number of bits, so a standardization block that provides to expand 32 bits data in 2's complement is needed.

The ADC can be directly connected to an analog SoP pin or to a sensor output in order to monitor the analog signal evolution. The ADC is a standard SAR with 14-bit resolution and 48 ksample/s of maximum sampling frequency and features also an amplifier to set the gain. Both the ADC and amplifier are configurable through the PC, to obtain the correct display of the monitored signals. The standardization block is needed again to expand 32 bits data coming from the ADC in 2's complement.

The ADSI can work in two functioning modes: it act as Virtual Oscilloscope and Snapshot.

The Virtual Oscilloscope mode is suited to have a quick and coarse-resolution picture of a group of signals (analog or digital), in order to help identifying and verifying the right signal selection and configuration; the output format is a set of windows continuously updated and triggered on a specific event, if needed. After the selected trigger event, 256 samples for each trace are acquired and then transferred to PC for their display. This is possible thanks to a dual-port RAM implemented in the FPGA that is simultaneously written and read; the monitoring capability is up to 4 signals in parallel, constrained on 8-bit to speed up the transmission towards the PC.

The Snapshot mode allows acquiring data of a temporal window in correspondence of a trigger event writing 32-bit data in an external SRAM and serializing them to the PC for final post processing; the SRAM size for the actual implementation is 1MB, so up to 218 samples can be stored with a sampling rate which can be easily customized. The user can select the channels list to be analyzed and then set three different kinds of triggers; in addition to that, there is the possibility to select the time range of observation configuring the number of samples to be acquired before and after the trigger event. The CPU configures the system by writing in appropriate registers, sets the ASIC to make available the interested signals and sends data to the PC by using a USB connection (the USB is used as a 1Mbit/sec UART to simplify the hardware and the protocol between PC and ADSI). The CPU executes just a limited number of operations; nevertheless it has been preferred to a simpler state machine for its bigger flexibility, allowing modifications of the firmware instead of the hardware, in case of subsequent modifications and/or improvements. The CPU used in the ADSI is an 8051 customized accordingly to the requirements of the project.

The ADSI has been mapped on a commercial Spartan-3 LC development board which provides a 400K-gate Xilinx Spartan-3 device (XC3S400-4PQ208CES) [10] (see Fig. 3), and uses a P160 expansion module [11] (see Fig. 4).

This module support 1MB SRAM memory for the snapshot and feature the 14-bit SAR ADC used for analog signal monitoring.

The main characteristics of the selected development board are:

- RS-232 port (via a USB link);
- FPGA Spartan 3 family with 400Kgates;
- Dimensions 100x135 cm;
- Low-cost (less than 200 euro).

The 400kgates device is enough to implement the whole ADSI hardware, since the architecture occupies the 95% of the available area; the clock frequency for this system has been set to 20 MHz in order to make the CPU fast enough for the ADSI application (even if the final timing analysis reported a maximum working frequency of 47MHz).

IV. Using the ADSI: Graphic Interface

Two possible solutions have been taken into considerations during the firmware development. The first one was to implement all firmware in the ADSI so the user can select one of the available configurations provided.

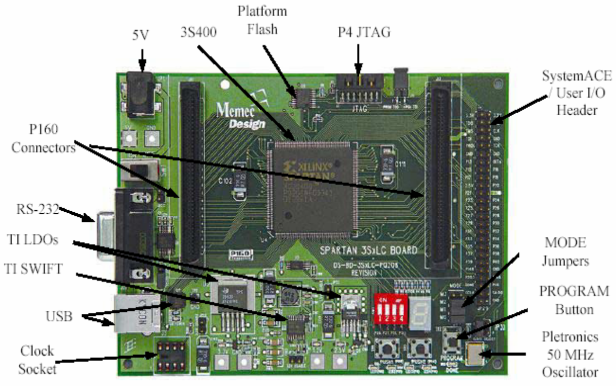


Fig. 3. The used Memec Spartan 3-LC development board.

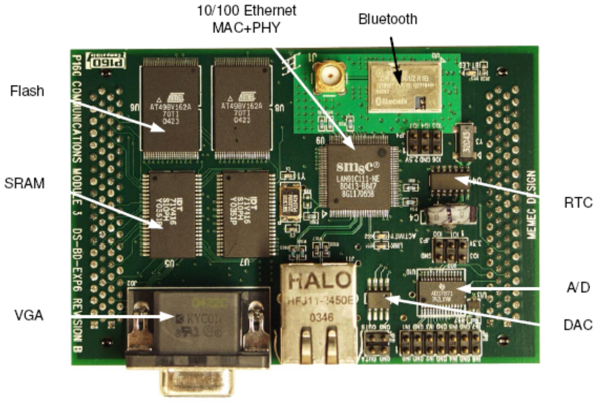


Fig. 4. P160 communication module 3.

The second one was to simplify the firmware in the ADSI but to develop full-capability software running in the PC which can control the ADSI with a dedicated communication protocol.

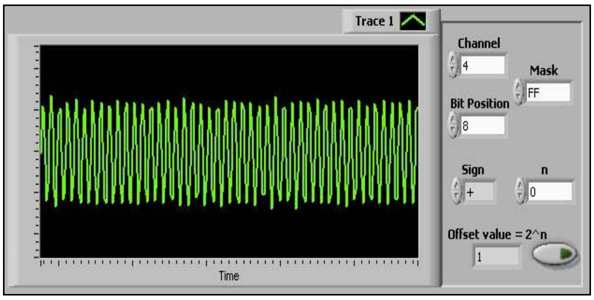
This second solution has been chosen since it is easy to modify and user friendly. When the CPU of the ADSI receives a frame (composed by operation code and data), the frame is examined and processed; as soon as the execution of the operation is accomplished, the answer is sent back to the PC. The language used to develop the graphical interface in the PC-side is LabVIEW.

The ASIC implements the same protocol used by PC side and this represents a simplification when managing the configurations of the 2 systems (ASIC and ADSI). The set-up operations of the ADSI are:

- Configuration of the ASIC, by setting the list of the interested channels that will be sent as serial frames;
- Configuration of the ADSI, by setting the same list of the channel that will be received, specifying also their arithmetic.

After the set-up operations, the ADSI is able to send to the PC the interested signal list. The two function modes are manageable by the simple graphic interface as described below.

Virtual Oscilloscope mode allows the on-screen signals monitoring. The user can set gain, offset, trigger of the waveform and several other standard settings which a standard physical scope provides. In Figure 5 is shown a detail of the front panel of the graphic interface, a trace of virtual scope with its settings. Figure 6 shown the ADSI while is working in Virtual Oscilloscope mode.



Trace 1

Channel 4

Mask FF

Bit Position 8

Sign +

n 0

Offset value = 2^n 1

Fig. 5. Detail of virtual oscilloscope.

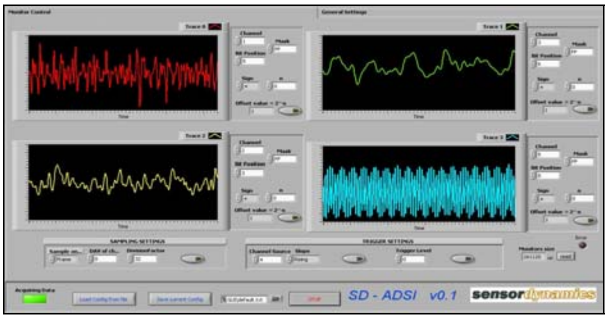


Fig. 6. Virtual Oscilloscope front panel.

Snapshot mode allows storing the signal values in an external SRAM. They are sent under request to the PC and their output is already formatted in order to be directly processed by adequate tools (the Matlab language has been chosen for this implementation).

In Figure 7 and Figure 8 are shown two plots related to data acquired in Snapshot mode. The first one refers to the acquisition of samples after the trigger event, the second one to the acquisition of samples both before and after the trigger event.

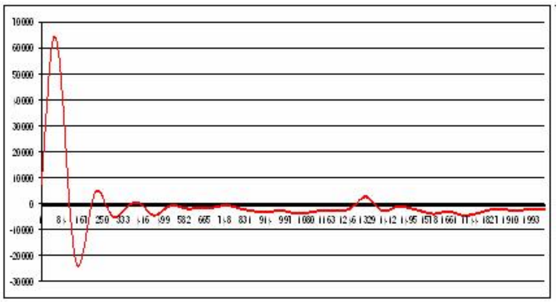


Fig. 7. Acquisition of 2048 samples after trigger event.

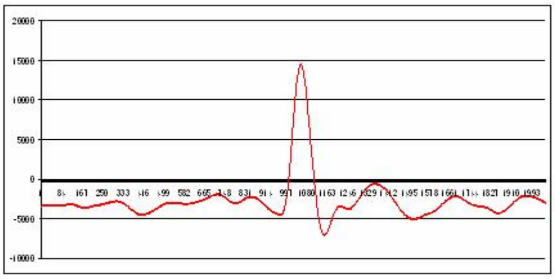


Fig. 8. Acquisition of 1024 samples before and 1024 after trigger event.

V. Application Case

The system ADSI has been widely used to characterize the behavior of an engineering sample of a gyro module in terms of noise and sensitivity in case of mechanical disturbances. The module is represented by a SoP where a MEM gyro sensor, for angular rate measurements, and an ASIC for signal conditioning are assembled together on a pin-limited package. The gyro sensor is a resonant device and needs controlled driving (for frequency and amplitude stabilization) as depicted in Fig. 9; the mechanical angular rate is transferred to the sensor according to Coriolis effect and hence sensed and processed by suited circuitry.

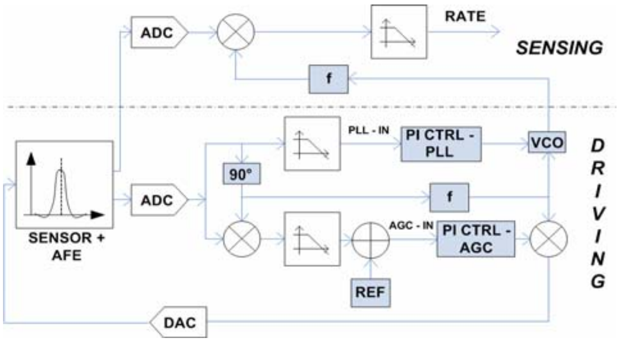


Fig. 9. Gyro-system architecture.

Its first application is related to the automotive Electronic Stability Program (ESP) field and hence it has to satisfy almost tight requirements in teems of temperature range, noise floor and sensitivity against external disturbances. The complexity of this hybrid system is so high that, despite the help given by the several tools/languages available for design and verification, the effects like the ones mentioned above can be just roughly estimated; this means that their impact on the module can be fully understood under the real environment, while effective countermeasures and settings can be derived only by data extracted from all relevant internal nodes at the same time.

The ASIC in the module under test was implementing the Digital Monitoring Unit and has been configured with different settings for power-on sequence (transient acquisitions conditions) and noise evaluations (stead state conditions). The power-on sequence has been acquired using the Virtual Scope, with the trigger set on the phase error of the digital PLL (needed for frequency stabilization). The power-on sequence has been acquired using the Virtual Scope, with the trigger set on the phase error of the digital PLL (needed for frequency stabilization); the sequence is depicted on Figure 10. These acquisitions allowed the refinement of the power-on sequence in order to improve the startup-time.

The second example is represented by the steady-state measurements in order to carry on spectrum analysis with different resolutions: Fig. 11 represents the spectra of two modulated signals (217 samples @ 30 kHz sampling rate), while Fig. 12 shows the same once demodulated in base band (215 samples @ 1 kHz sampling rate). This analysis has been very useful to trim the several configurable parameters in order to optimize the noise level of the final rate signal.

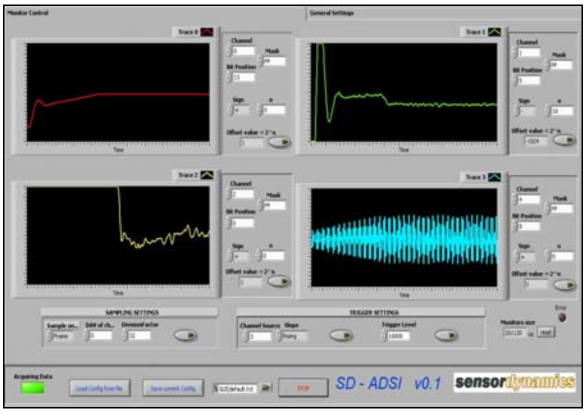


Fig. 10. Virtual scope acquisition during transient.

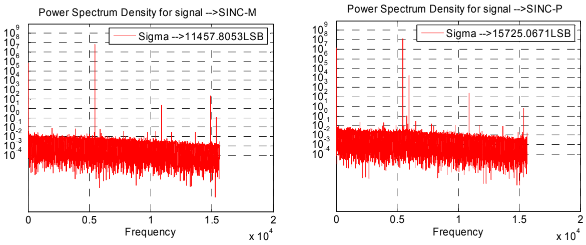


Fig. 11. Spectra of modulated signals.

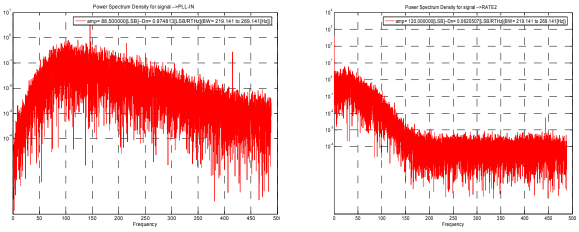


Fig. 12. Spectra of base-band signals.

The expansion board developed for the SoP under test features also an accelerometer which may be used to reveal the mechanical movements applied to the board along the interested axis. So, as further application, the ADSI has been used to monitor the SoP internal signals behavior while applying several shocks on the expansion board, whose entity could be measured by the accelerometer. In this set-up the accelerometer signal has been slightly conditioned to fulfill ADC input requirements and the ADSI was set to acquire the accelerometer signal (through ADC) and SoP internal digital signals together. Fig. 13 shows the more interesting results of this application. The displayed spikes in the measured rate come from the mechanical shocks applied to the expansion board: their amplitude allowed the extraction of the sensor sensitivity against mechanical shocks.

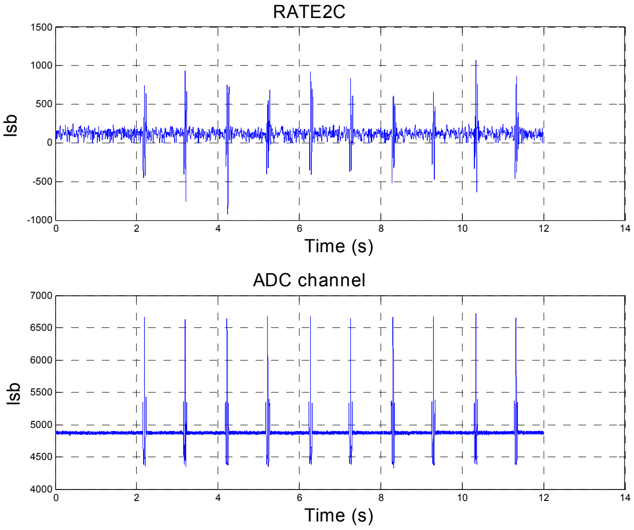


Fig. 13. Behaviour of rate and acceleration signals during external stimuli

In Figure 14 is showed the whole architecture during these tests execution. The connection between the expansion board and the ADSI are only the two pin aforementioned, which implements the simple communication described in Section III. The angular rate measured by the SoP is normally provided via RS-232 during its normal functioning mode, so we found useful to merge the four data cable in a DB9 connector to simplify the connections. The result is a compact and portable object.

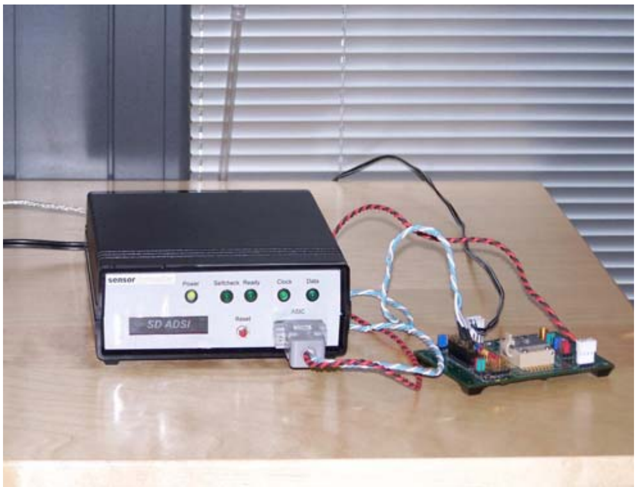


Fig. 14. The ADSI connected to the expansion board of the SoP.

VI. Conclusions

An advanced digital signal inspector (ADSI) to monitor and analyze digital internal signals of a module has been here presented. It gives the possibility to characterize prototypes and final versions of pin-limited system on package by using only two pins used in a custom serial communication. The ADSI supports also one analog signal input; it can be connected to an external circuitry in order to evaluate at the same time the behavior the digital internal signal of the SoP and the analog source itself, and possibly calculate existing correlations.

The main characteristic of the system are:

- USB standard connection with the PC;
- architecture based on low-cost commercial FPGA on-board;
- response time suitable for real-time observation;
- two operational modes, real-time virtual scope and snapshot, available;
- configurable trigger events, signal list and adjustable dynamic;
- 14 bit SAR ADC with 48 ksample/s maximum sampling frequency for analog signals.

A user friendly interface developed in LabVIEW is responsible for the communication (and settings) with the ASIC and the ADSI at the same time.

The support received during the verification of in-house SoP, together with the poor area occupancy of the serializer, makes the ADSI approach suited for the company and will be re-used in upcoming projects.

Acknowledgments

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