Laboratory 2: Time-Division Multiplexor and Clock Divider

Objectives

1. Get students to familiar with the synthesis tool (Vivado)
2. Synthesis FPGA
3. Able to explain time-division multiplexor
4. Able to design simple counter and clock divider
5. Able to use language template.

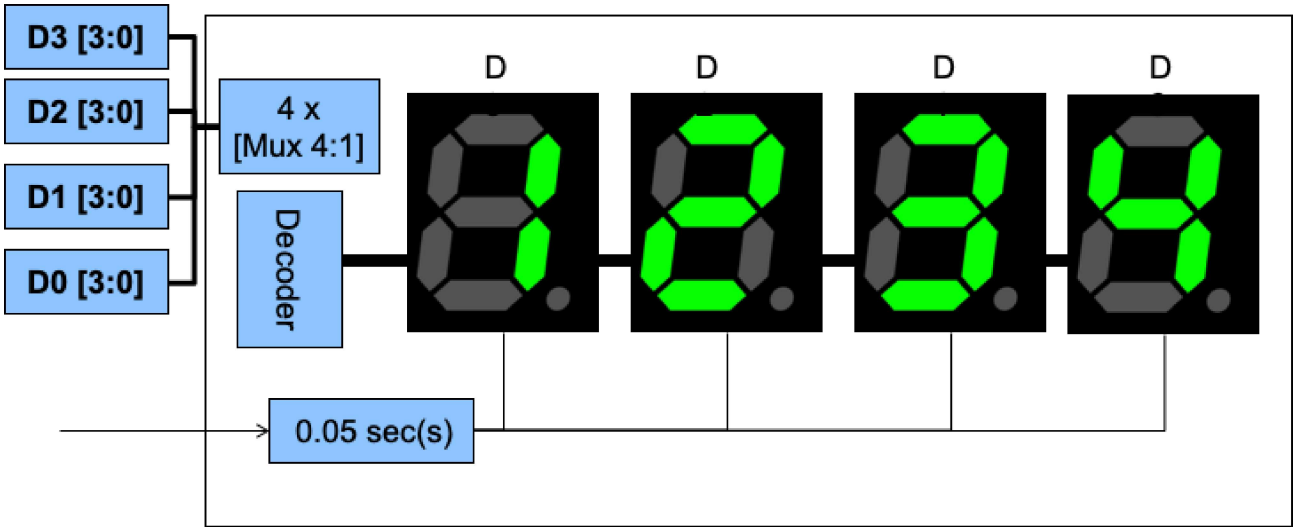
Background

TDM

To drive a seven-segment display (whether it is common anode or common cathode), each digit would requires 9 wires (a to g, dot, common ground or common vcc). With several digits of seven-segment display, the number of wires would intuitively multiplied. For examples, 4 digits of seven-segment displays may require up to 33 wires (a to g and dot for each digits with a sharing common wire). It is not practical to have so many wires. To share (reduce) physical wires, Time-Division Multiplexor is introduced.

With time-division multiplexor, we can share 8 wires (a to g and dot) among the displays. Only a digit will be active at a time. If the segments turn on and off at the appropriate rate (I.e. 15 frames per second or more), the observer would see it as if all segments are on at the same time.--hence the term time-division multiplexor. This way, four digits of seven-segment displays can be connected with only 12 wires (8 from a to g and dot + 4 for activating digits) .

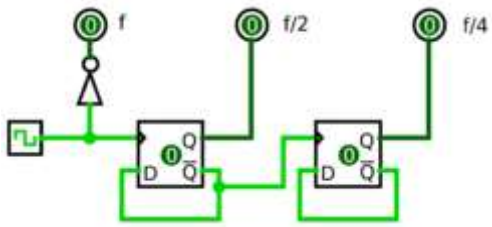
4



For more details about time-division multiplexor, please watch the demonstration video.

Clock Division

There several ways to divide high frequency clock into slower clock. A simple solution is to cascade D flipflops (or event T flipflops) together by feeding ~Q0 to D0 and feed Q0 as a clock for D1 (and so on). Nonetheless, this is just one implementation of the clock division. You may use a counter to set and clear a bit as a clock division as well.



5

Language Templates

Vivado IDE tool comes bundled with language templates. Language templates are basically code snippet for HDL. You may access the language templates from menu > Tools > Language Templates. A language template that might be useful for this lab is 7-segment encoding.

[4] Picture is taken from the archive of Krerk Piromsopa, Ph.D.
[5] Picture is taken from wikipedia https://upload.wikimedia.org/wikipedia/commons/thumb/a/a0/Frequency_divider_animation.gif/250px-Frequency_divider_animation.gif

Exercises

1. Use your knowledge from clock division and time-division multiplexor to display a 4-digit hexadecimal number (0x1234) to the seven-segment display of the BASYS 3 board. Your design should be modularized (You can save the component for reuse later). There should be at least 3 modules: clock divider, hex (or bcd) to 7-segment encoder and 7-segment TDM.

2. Please answer the following questions and submit (in PDF format) to CourseVille on Friday before 23:59 (midnight).

    a. Is the 4-digit seven-segment displays on the BASYS 3 board is a common anode for common cathode? Please explain.

    b. From the wiring of the board, which logic do you have to assign to the 7-segment pins (a to g and dot) to turn the LED on.

    c. Given that the clock of the BASYS3 is around 10ns, how many bits do you have to divide the clock with get the appropriate clock for the TDM. Please provide you analysis (calculation).

    Hint
    1. Use the BASYS 3 XDC[6] file as a base constraint file.
    2. Read the datasheet to determine the interconnection in the board.
    3. Use the language templates for 7-segment encoder

[6] https://mis.cp.eng.chula.ac.th/krerk/teaching/2018s2-HaWSynLab/downloads/Basys-3-Master.xdc