EE 113 – Intro to Electrical Engg Practice: 2021-22/I

Solutions to the Problem Sheet – 5: Digital Electronics

(updated on Jan 2,2022)

Topics: Sequential Circuits – NAND latch, SR Flip-flop, JK flip-flop, D-flip-flop, Ripple counters (Asynchronous counters), Synchronous counters

Part A– Latches and Flip-flops

1. NAND latch – students to try on their own.
2. SR latch (level sensitive or level triggered Clock) - – students to try on their own.
3. b) Go through the reference material uploaded on Moodle and find at least two major applications of the D flip-flop.
   Please Sec 5.8 and Sec 5.9 (Pages 280-282) of the REF material "REF-4-EXTRA-Tocci-12e-pp256-295-Latches-FlipFlops.pdf" uploaded in the folder: "Lect8-Dec21-DigitalElectronics". You will be able to see some applications.
   In addition, the following are also common applications:
   a) Shift register (which is just a cascade of D-flip-flops. Shift registers are extensively used for several applications, such as serial-to-parallel and parallel-to-serial conversion of data, code generation etc).
   b) D flip-flops can also be used for implementing counters and other sequential circuits, instead of JK flip-flops. From the actual implementation point of view D flip-flops will give simpler solutions. You will study more of this next year.
4. a) and b) – note that the clock signal has now been modified. In level-triggered flip-flops, feedback like the one showed in the figure will give rise to problems. The solution is to use a very small width pulse as now given (width less than the total propagation delay of two gates). That way by the time the feedback ($\bar{Q}$) comes to the D input the clock level is no more high.

   Both (a) and (b) with the Clock as now given will give a mod-2 or a divide-by-2 counter. Frequency of Q will be half of the clock frequency. The interesting feature here is: irrespective of the width of the high pulse (as long as it is lower than the propagation delay of two gates), will give Q outputs which have the same frequency, which will be half the frequency of the clock frequency. Also, the outputs will be square wave outputs.

5 (a) and (b) will give you the same outputs, i.e. the frequency of the waveform at the Q outputs will be the same.

(c) The outputs will give the same output as in problem 4. Hardly any noticeable difference.

e) Advantage in using edge-triggered flip-flops instead of level sensitive flip-flops:

In an edge-triggered flip-flop there are far less restrictions on the inputs, i.e. inputs should not change just before the active clock edge (+ve or -ve edge, as the case may be) by the 'setup time' and should be steady after the active clock edge for a time period of 'hold time'. For example, if the setup time and hold time of a +ve edge-triggered flip-flop is 5 ns, then the flip-flop inputs should be steady 5 ns before the +ve edge of the clock and after the +ve edge it should be steady for 5 ns more. Anywhere else the inputs can change. But in a level sensitive flip-flop, the inputs should be steady before the active level and should be steady for the entire duration of the active level. No input changes are allowed during the active clock level. For example, if you have a flip-flop which is 'High' level sensitive, then the inputs should be steady just before the 'High' level and should stay steady throughout the 'High' period and should change only after the 'High' interval is over.

Hence, edge-triggered flip-flops have far less restrictions for input changes. They are almost always preferred over level sensitive flip-flops. (Refer to 'REF-4-Mano-pp190-204-Latches-Flipflops.pdf' uploaded in the folder: "Lect8-Dec21-DigitalElectronics").

6. The JK flip-flop will work as a toggle flip-flop. Q output waveform will have half the frequency of the Clock. Here Q output frequency = 5 kHz.

7 a) A latch circuit commonly used for generating manual clock is shown below, where a spring-loaded single-pole double-throw (SPDT) push button switch is used. This switch has three contacts, viz. Common (COM), Normally-Open (NO), and Normally-closed (NC).

i) In the switch position is as shown in the figure, what will be the Q output and the state of the LED (ON or OFF)?

With switch position as shown, $\bar{Q} = 1$. Hence the LED will be OFF.

ii) In the switch position as shown, what will be the currents flowing into the Std TTL NAND gate inputs connected to NO and NC? Std TTL gate current specifications: I_{OH} = 400 μA, I_{OL} = 16 mA, I_{IH} = 40 μA, I_{IL} = 1.6 mA.

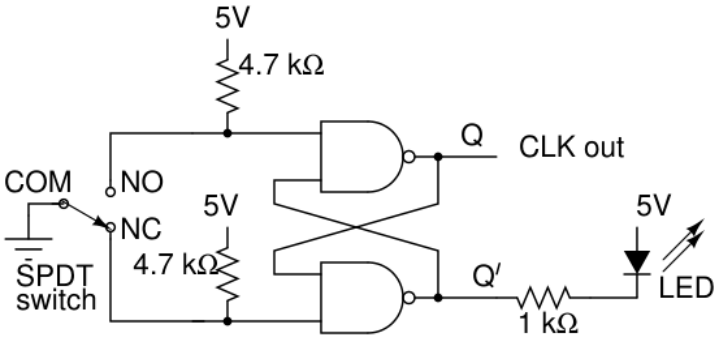
NAND input connected to NO: Input = +5 V, hence the input current is: I_{IH} = 40 μA

NAND input connected to NC: Input = 0 V, hence the input current is: I_{IL} = 1.6 mA

iii) Why is such a latch circuit required for generating clock manually with each press; instead why not just use the switch (with connections to +5V) for generating clock pulse with each press?

All mechanical switches, such as the one used here are spring-loaded. Hence, if the switches are used directly, there will be chattering or bouncing, i.e. there will be multiple pulses as there will be multiple contacts made by the switch due to the spring and the mechanical action of pressing.

By connecting the NAND latch to the switch, as soon as a '0' is detected at the first instant, the corresponding NAND gate output would go to '1'. Subsequent chattering/bouncing/contacts will have no effect. Hence, we will get only one pulse for every press of the switch.



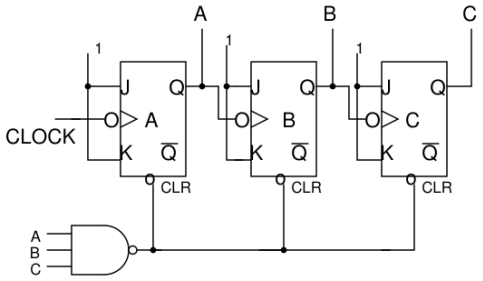
Part B – Ripple Counters (Asynchronous Counters)

8. The circuit diagram of a Ripple Counter is shown below. It uses –ve edge-triggered JK flip-flops. The JK flip-flops have active-low asynchronous clear inputs (i.e. irrespective of the Clock, when CLR = '0' the flip-flop is reset).

a) Analyze the circuit and write the stable sequence of states (CBA), where C is the MSB and A is the LSB.

b) Based on your answer in (a) classify the counter as a Mod-N UP counter or a Mod-N DOWN counter.

c) Sketch the A, B and C outputs of the counter with respect to the Clock for at least 8 Clock periods.



Ripple counter

a) It is a ripple counter made by cascading –ve edge triggered JK flip flops (connected in the toggle mode), with Q output of a fli-flop connected as the CLOCK of the next stage. Hence it is an UP counter.

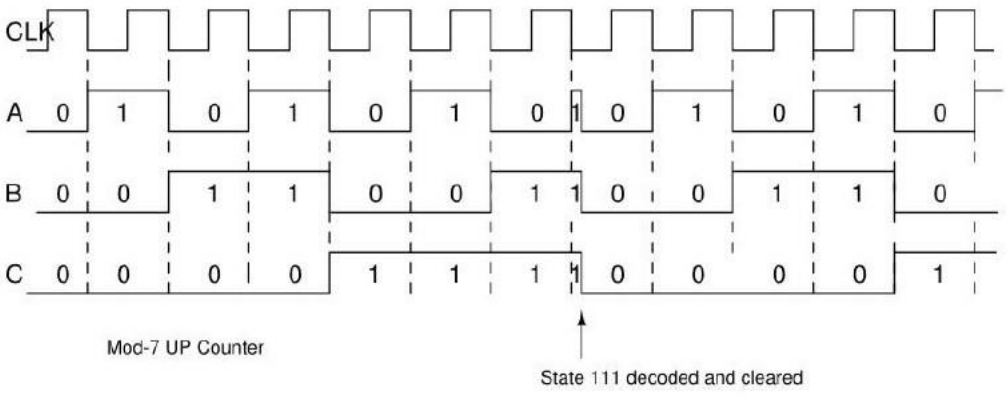
Let us assume the starting state (CBA) is: 000. It will count UP to 001, 010, 011, 100, 101, and 110. But once the count reaches 111, the NAND gate would produce a '0' at its output which is connected to the CLR inputs of the flip-flops. The flip-flop outputs will all now clear to 000. At the next –ve edge of the Clock, once again the counter will count up. This process continues for ever.

Note that state 111 is an unstable state.

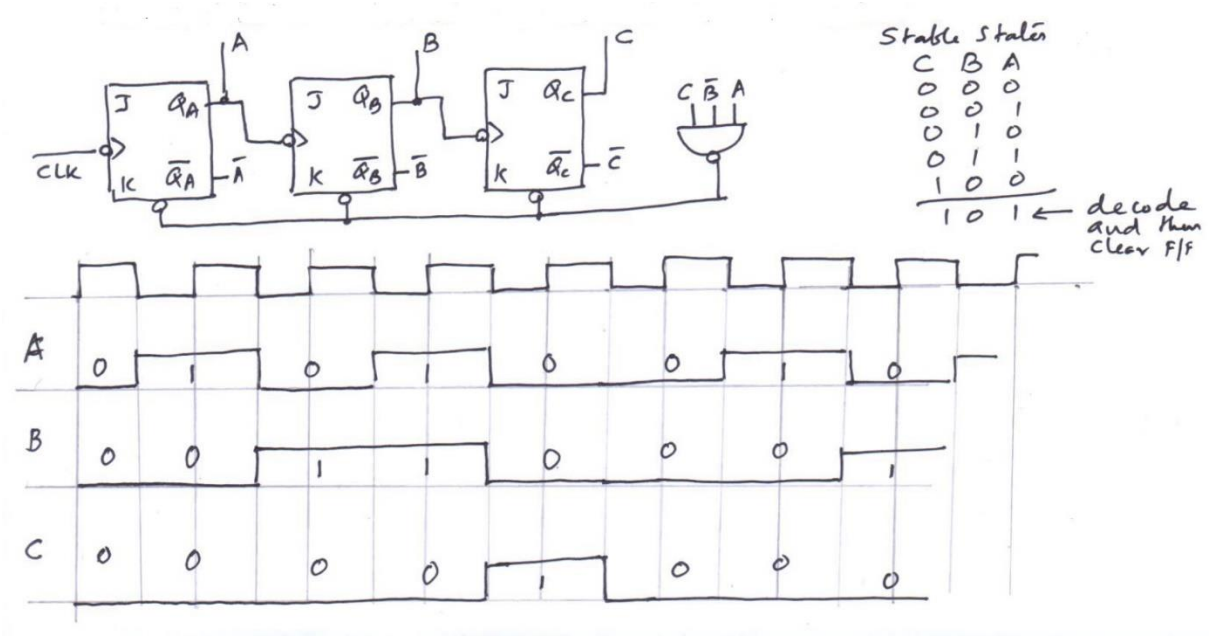
Therefore the stable sequence of states (CBA) are: 000, 001, 010, 011, 100, 101, 110

b) It is therefore a Mod-7, UP ripple counter.

c) A, B, and C outputs with respect to the Clock are sketched below:



9. Design a modulo-5 Ripple UP counter using –ve edge triggered JK flip flops and one extra gate (any type of one gate with any number of inputs). Assume that each JK flip-flop has both Q and Q' outputs and also an active-low asynchronous Clear input (i.e. when the Clear input = '0', the Q output will be '0' irrespective of the Clock). Draw a clear circuit diagram and sketch the timing diagram showing the CBA outputs (C is the MSB) with respect to the Clock for at least eight Clock periods.



Part C – Synchronous Counters

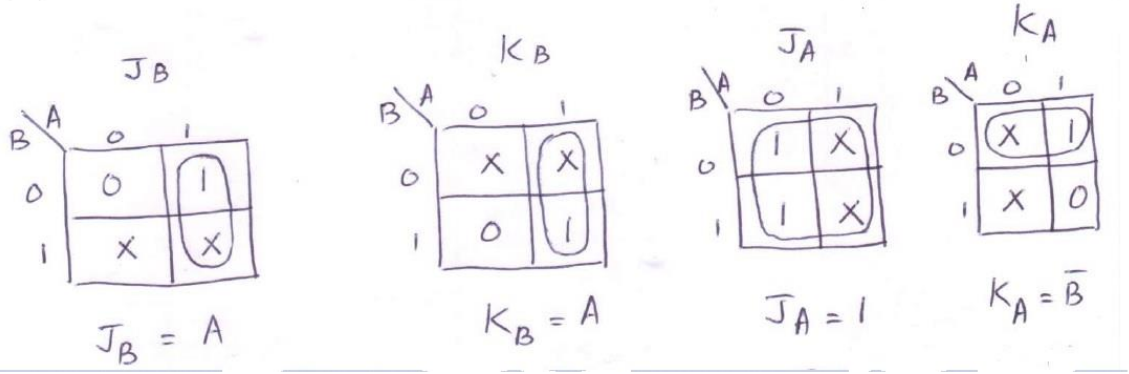
10. Design a modulo-3 synchronous UP counter using +ve edge triggered JK flip-flops, with the sequence of states (BA): 01, 10, 11, 01, …. If the unused state 00 comes, the next state should be 01. Give all the design steps, i.e. the table of present states, next states, the required JK inputs for the next state, and the K map minimizations for the J and K inputs of the flip-flops. Draw the final circuit diagram.

Solution: Note that in the solution shown below, only the present states are shown in Col 1 and 2. It would be better for students to have another two more columns, say 3 and 4, giving the next states, as asked in the question. The given solution has omitted the extra two columns for the sake of brevity.

B	A	J_B	K_B	J_A	K_A
0	1	1	X	X	1
1	0	X	0	1	X
1	1	X	1	X	0
0	1				
0	0	0	X	1	X
0	1				

Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



11. Design a modulo-6 synchronous DOWN counter using +ve edge triggered JK flip-flops, with the following sequence of states (CBA): 111, 110, 101, 100, 011, 010, 111, …. If any of the unused states, i.e. if states (CBA): 001 or 000 comes, the next state should be 111.

Give all the design steps, i.e. the table of present states, next states, and the required JK inputs for the next state, and the K map minimizations for the J and K inputs of the flip-flops. No need to draw the final circuit diagram.

Solution: Instead of the Present states and Next states, the sequence of states alone is written in Col 1 and 2, just for brevity of the table. But in the beginning it is better to have as was done in the lecture.

Mod-6 Synchronous DOWN counter

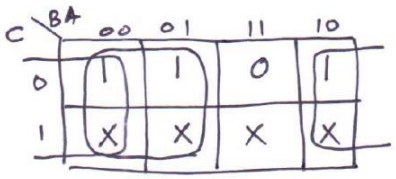
Transition Table for a JK flip-flop

Q_n	Q_{n+1}		J	K
0	0		0	X
0	1		1	X
1	0		X	1
1	1		X	0

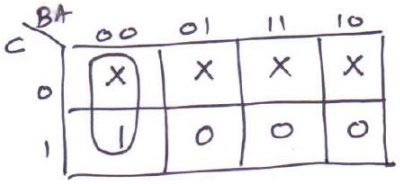
Design Table: Sequence of states, and required J,K inputs

C	B	A		J_C	K_C	J_B	K_B	J_A	K_A
1	1	1		X	0	X	0	X	1
1	1	0		X	0	X	1	1	X
1	0	1		X	0	0	X	X	1
1	0	0		X	1	1	X	1	X
0	1	1		0	X	X	0	X	1
0	1	0		1	X	X	0	1	X
1	1	1							
0	0	1		1	X	1	X	X	0
1	1	1							
0	0	0		1	X	1	X	1	X
1	1	1							

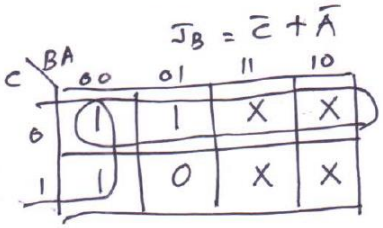
$J_C = \bar{B} + \bar{A}$



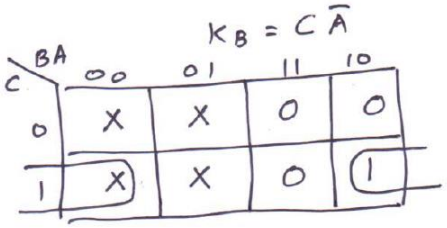
$K_C = \bar{B}\bar{A}$



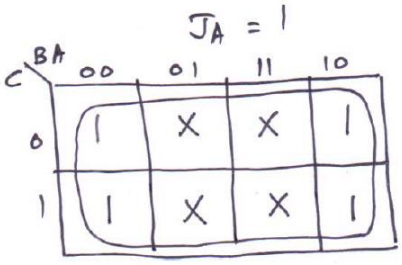
$J_B = \bar{C} + \bar{A}$



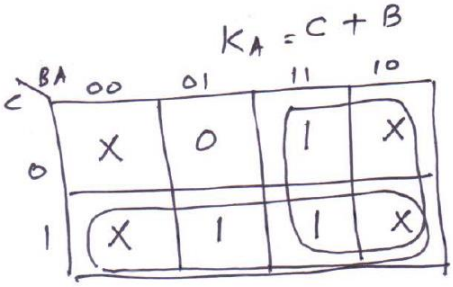
$K_B = C\bar{A}$



$J_A = 1$



$K_A = C + B$



12. a) Design a mod-7 synchronous counter having the sequence of states (CBA): 000, 001, 010, 011, 100, 101, 110, 000,… using -ve edge triggered JK flip-flops. If the unused state (CBA): 111 appears at the start, the next state should be 000.

Give all the design steps, i.e. the table of present states, next states, and the required JK inputs for the next state, and the K map minimizations for the J and K inputs of the flip-flops. No need to draw the final circuit diagram.

Solution:

C	B	A		J_C	K_C		J_B	K_B		J_A	K_A	
0	**0**	**0**		**0**	**X**		**0**	**X**		**1**	**X**	
0	**0**	**1**		**0**	**X**		**1**	**X**		**X**	**1**	
0	**1**	**0**		**0**	**X**		**X**	**0**		**1**	**X**	
0	**1**	**1**		**1**	**X**		**X**	**1**		**X**	**1**	
1	**0**	**0**		**X**	**0**		**0**	**X**		**1**	**X**	
1	**0**	**1**		**X**	**0**		**1**	**X**		**X**	**1**	
1	**1**	**0**		**X**	**1**		**X**	**1**		**0**	**X**	
0	**0**	**0**										
1	**1**	**1**		**X**	**1**		**X**	**1**		**X**	**1**	
0	**0**	**0**										

Do the K-map entries and verify that the minimized J, K inputs are:

$J_C = BA$; $K_C = B$

$J_B = A$; $K_B = C + B$

$J_A = \bar{C} + \bar{B}$; $K_A = 1$

Optional design verification step

Verify the results for one or two cases (i.e. check for a sequence of states with the designed J,K values). This can be done by having another table, where the ordering of the columns is as shown. (In the solution shown below, all the entries are verified – which is not required in actual design, provided the K-map entries and minimizations are done carefully).

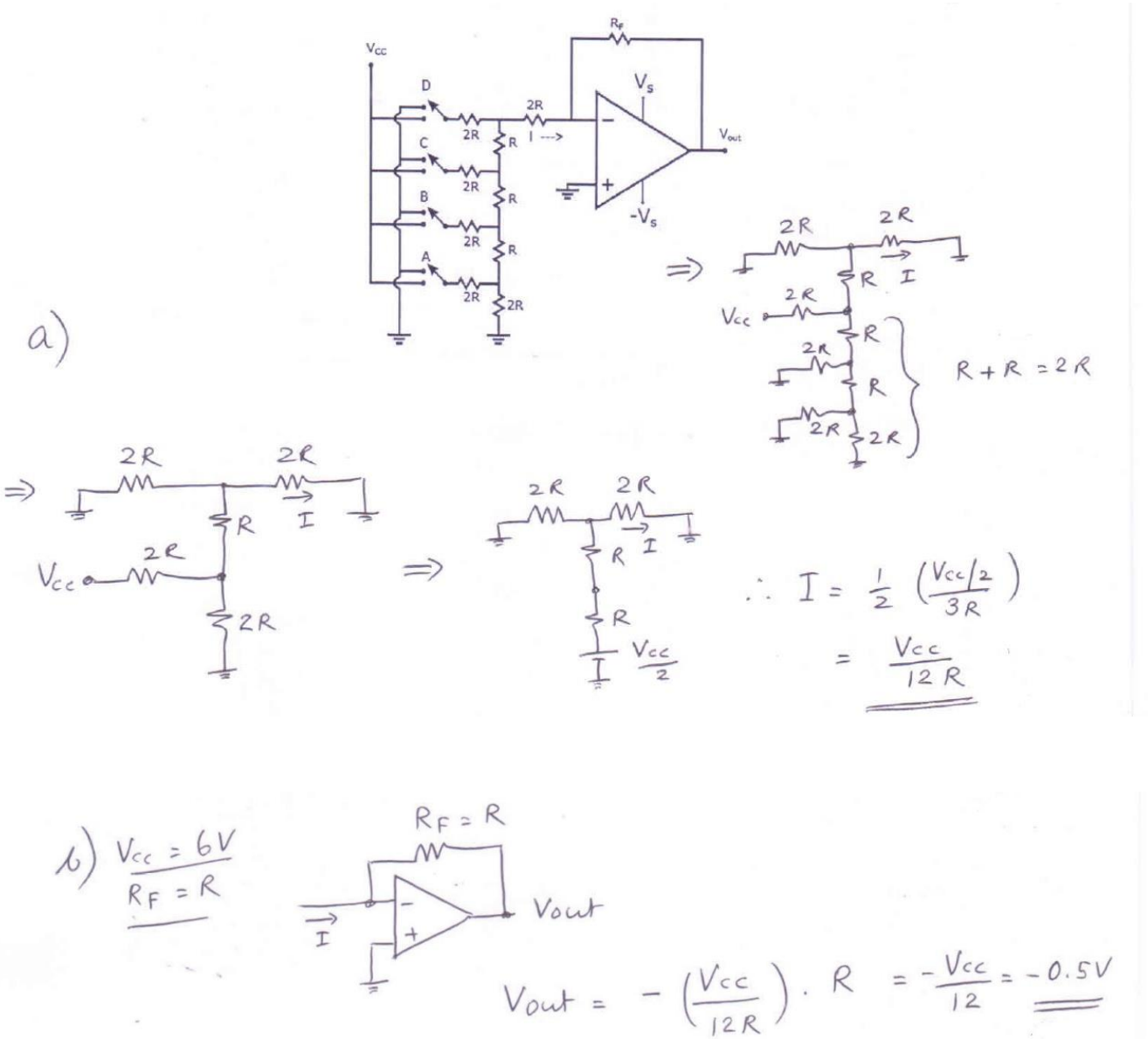
Present state													Next state		
C	B	A		J_C	K_C		J_B	K_B		J_A	K_A		C	B	A
0	**0**	**0**		**0**	**0**		**0**	**0**		**1**	**1**		**0**	**0**	**1**
0	**0**	**1**		**0**	**0**		**1**	**0**		**1**	**1**		**0**	**1**	**0**
0	**1**	**0**		**0**	**1**		**0**	**0**		**1**	**1**		**0**	**1**	**1**
0	**1**	**1**		**1**	**1**		**1**	**1**		**1**	**1**		**1**	**0**	**0**
1	**0**	**0**		**0**	**0**		**0**	**1**		**1**	**1**		**1**	**0**	**1**
1	**0**	**1**		**0**	**0**		**1**	**1**		**1**	**1**		**1**	**1**	**0**
1	**1**	**0**		**0**	**1**		**0**	**1**		**0**	**1**		**0**	**0**	**0**
1	**1**	**1**		**1**	**1**		**1**	**1**		**0**	**1**		**0**	**0**	**0**

Part D – R-2R ladder, DAC and ADC

13. Circuit diagram of a Digital-to-Analog Converter is shown below. Assume that switches A, B and D are in the 'GND' position, while switch C is in the 'V_{cc}' position.

    a) Obtain an expression for the current I in terms of V_{cc} and R.

    b) If V_{cc} = 6 Volts and R_F = R, calculate V_{out} (for the switch positions as mentioned above).



14. Circuit diagram of a Digital-to-Analog Converter is shown below.

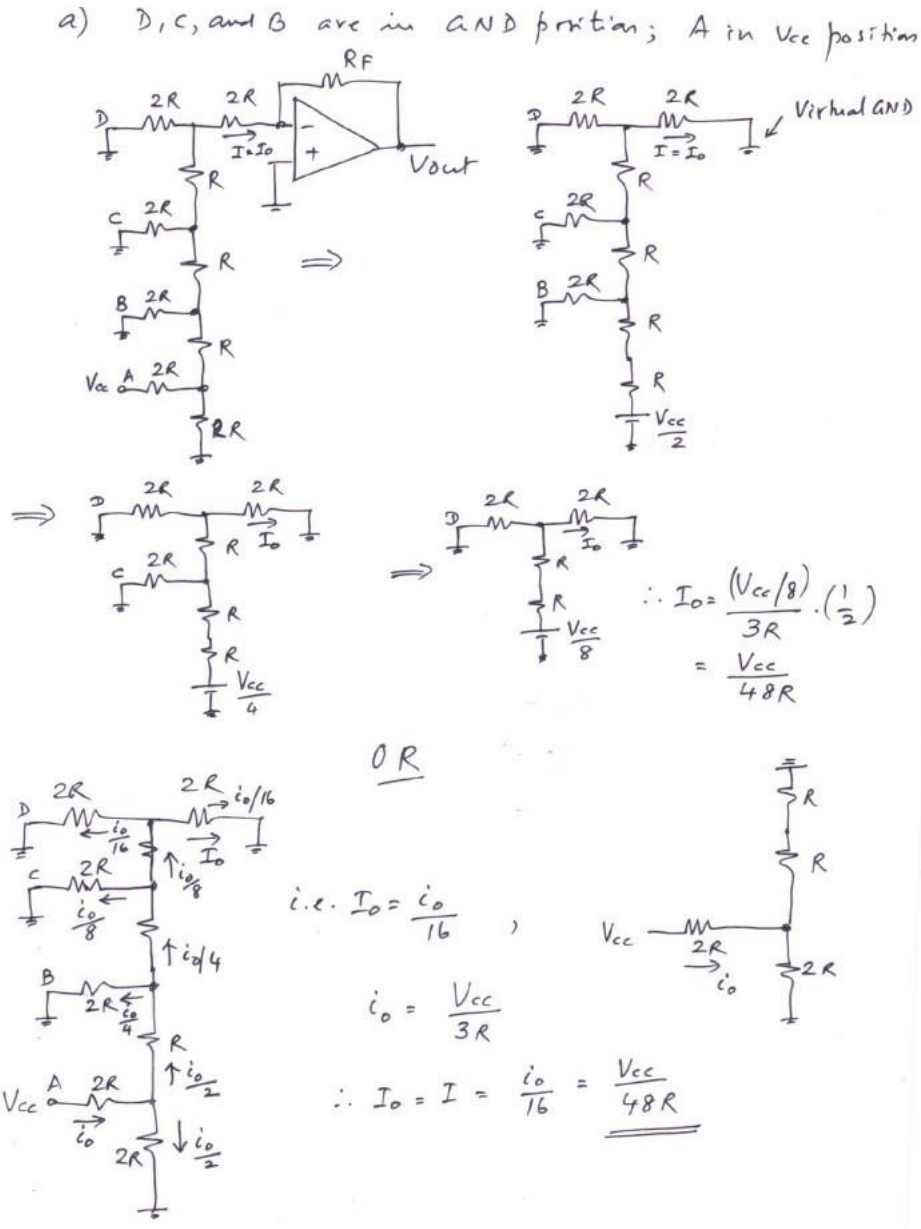
a) Assuming that switches D, C and B are in the 'GND' position, while switch A is in the 'V_{cc}' position, write current I (as indicated in the figure) in terms of V_{cc} and R.

b) Assuming that switches D, C and A are in the 'GND' position, while switch B is in the 'V_{cc}' position, write current I (as indicated in the figure) in terms of V_{cc} and R.

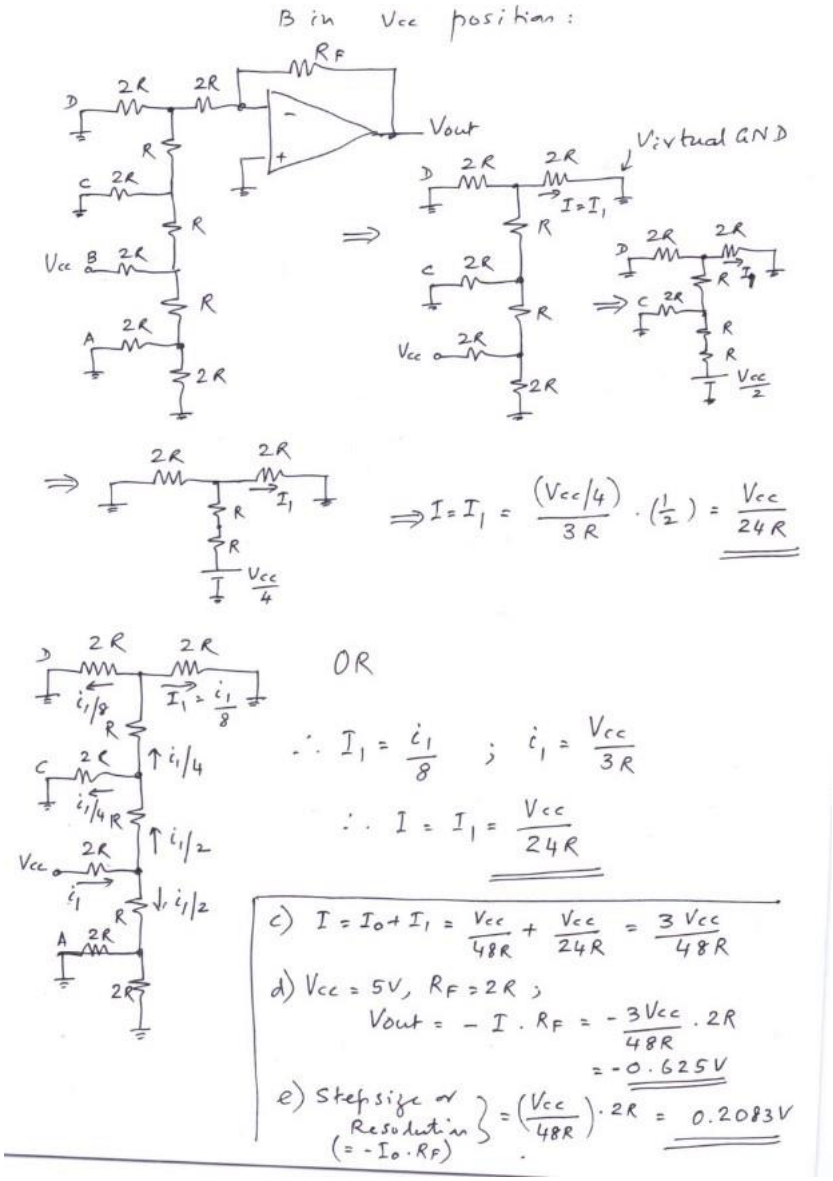
c) Based on the expressions you obtained in (a) and (b) above, write I (as indicated in the figure) in terms of V_{cc} and R assuming switches D and C are in the 'GND' position, while switches B and A are in the 'V_{cc}' position.

d) For case (c) calculate V_{out} assuming V_{cc} = 5 V and R_F = 2R.

e) What is the 'step-size' or 'resolution' (in Volts) of the given DAC?



b) D, C and A are in the 'GND' position, while switch B is in the 'V_{cc}' position

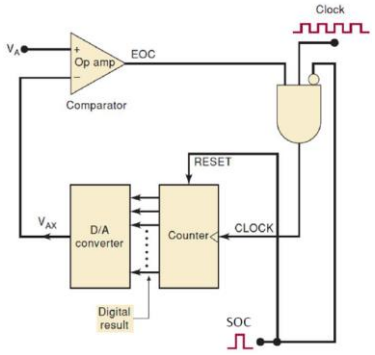


15. Block diagram of a simple analog-to-digital converter (ADC) is given below. Assume that the ADC is 4-bit with digital outputs D, C, B and A, where D is the MSB and A the LSB. The Opamp comparator output EOC gives '1' when $V_A > V_{AX}$, else '0'. The digital-to-analog converter (DAC) output V_{AX} is given by:

$$V_{AX} = V_{REF} [D(1/2) + C(1/4) + B(1/8) + A(1/16)]$$

It is assumed that, each time a valid input voltage V_A is applied to the ADC input, a short SOC pulse is applied to the circuit as shown, which resets the Binary counter and starts the ADC operation, giving a 4-bit digital value corresponding to the given analog input V_A.
Assume $V_{REF} = 5V$ and the Clock frequency is 20 kHz.

a) What is the step-size (or resolution) of this ADC in Volts?
b) What range of V_A values can be digitized by this ADC?
c) For $V_A = 3$ V, what will be the digital output (DCBA)?
d) What will be the time taken (in µsec, i.e. micro seconds) to get the digital output for the ADC operation in (c). You may neglect the delays caused by the Opamp comparator, DAC and the AND gate.
e) What will be the maximum time taken (in µsec) to digitize the highest V_A value?



Solution:

$V_{XD} = V_{ref} [D(0.5) + C(0.25) + B(0.125) + A(0.0625)]$

$V_{ref} = 5V$

a) Step-size or resolution

$= V_{ref} \cdot (0.0625) = 0.3125\ V$ (5V)

b) Max. range of ADC $= (V_{ref} - LSB)$

Since $V_{ref} [0.5 + 0.25 + 0.125 + 0.0625]$

$= 5 \times 0.9375 = 4.6875\ V$ (Ideally, max range should be within 4.375 and 4.6875 V)

Range of ADC $= \dfrac{0 - 4.6875\ V}{0 < V_A < 4.6875\ V} \rightarrow \dfrac{75}{16}$

c) $V_A = 3V$

Digitization is completed when $V_{AX} > V_A$

Step Size = 0.3125

# of Steps = $\frac{3V}{0.3125} = 9.6 \Rightarrow 10$ steps

$\therefore$ DCBA output is : 1010

d) Time taken = (10 steps) $\times \left(\frac{1}{20kHz}\right) = 500\mu s$

e) Maximum time taken = $15 \times 50\mu s = 750\mu s$