



STM32 CubeMX

1. Description

1.1. Project

Project Name	nuh755ziq_board_test
Board Name	custom
Generated with:	STM32CubeMX 6.16.0
Date	12/14/2025

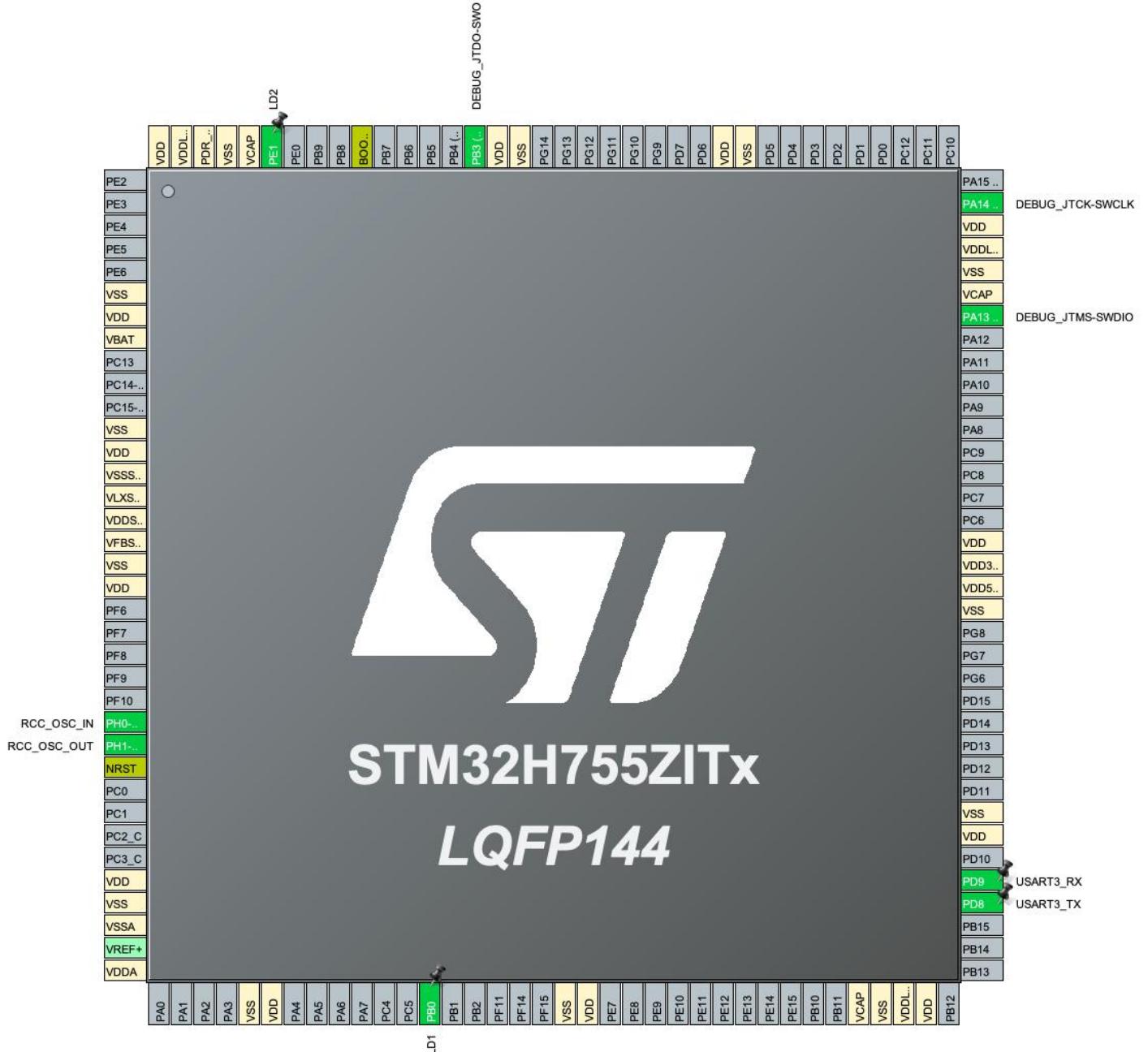
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H745/755
MCU name	STM32H755ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	ARM Cortex-M7 ARM Cortex-M4
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2. Pinout Configuration



3. Pins Configuration

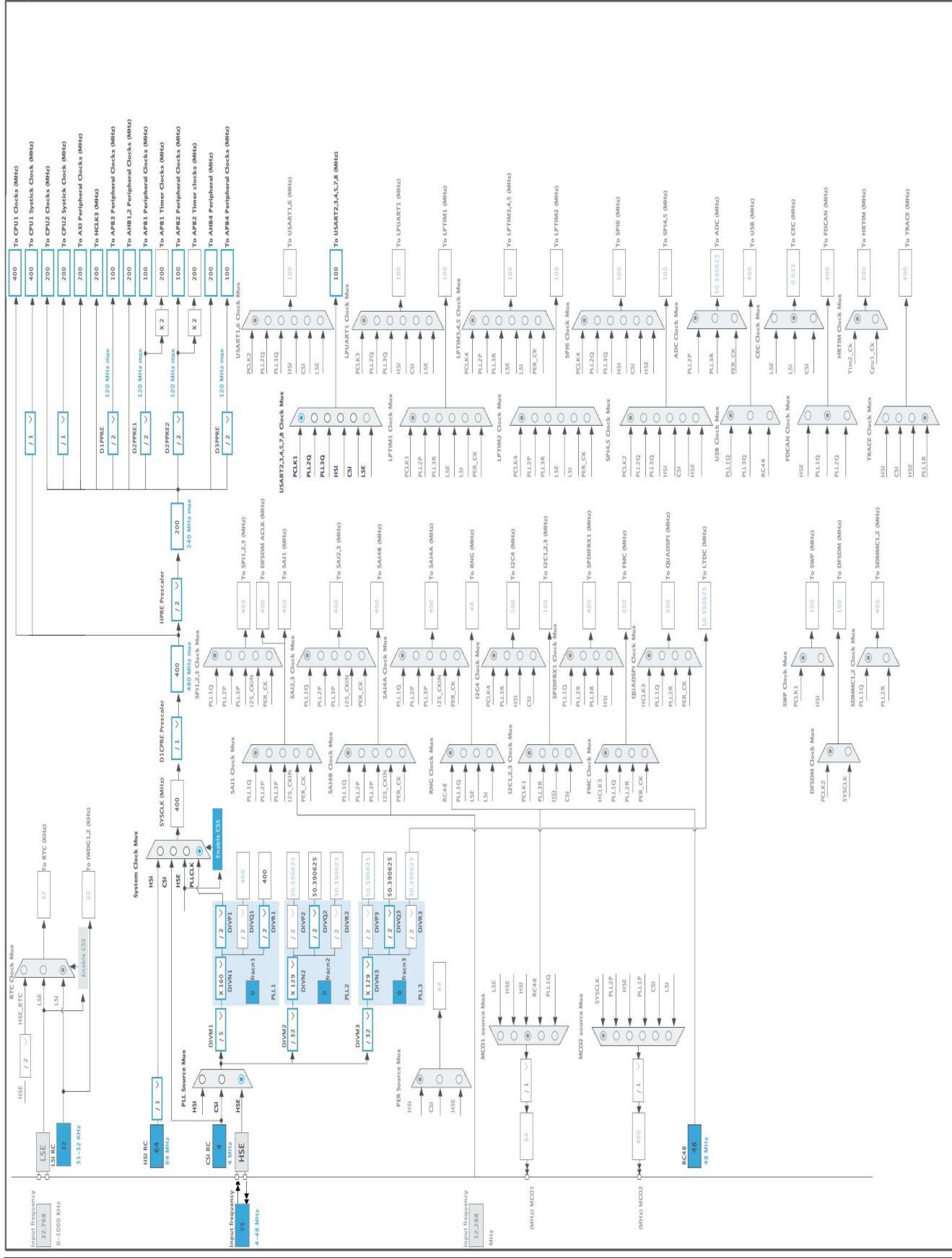
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VSS	Power		
7	VDD	Power		
8	VBAT	Power		
12	VSS	Power		
13	VDD	Power		
14	VSSSMPS	Power		
15	VLXSMPS	Power		
16	VDDSMPS	Power		
17	VFBSMPS	Power		
18	VSS	Power		
19	VDD	Power		
25	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
26	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
27	NRST	Reset		
32	VDD	Power		
33	VSS	Power		
34	VSSA	Power		
36	VDDA	Power		
41	VSS	Power		
42	VDD	Power		
49	PB0 *	I/O	GPIO_Output	LD1
55	VSS	Power		
56	VDD	Power		
68	VCAP	Power		
69	VSS	Power		
70	VDDLDO	Power		
71	VDD	Power		
76	PD8	I/O	USART3_TX	
77	PD9	I/O	USART3_RX	
79	VDD	Power		
80	VSS	Power		
89	VSS	Power		
90	VDD50_USB	Power		
91	VDD33_USB	Power		
92	VDD	Power		
102	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	

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Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
103	VCAP	Power		
104	VSS	Power		
105	VDDLDO	Power		
106	VDD	Power		
107	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
118	VSS	Power		
119	VDD	Power		
128	VSS	Power		
129	VDD	Power		
130	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
135	BOOT0	Boot		
139	PE1 *	I/O	GPIO_Output	LD2
140	VCAP	Power		
141	VSS	Power		
142	PDR_ON	Power		
143	VDDLDO	Power		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H745/755
MCU	STM32H755ZITx
Datasheet	DS12919_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

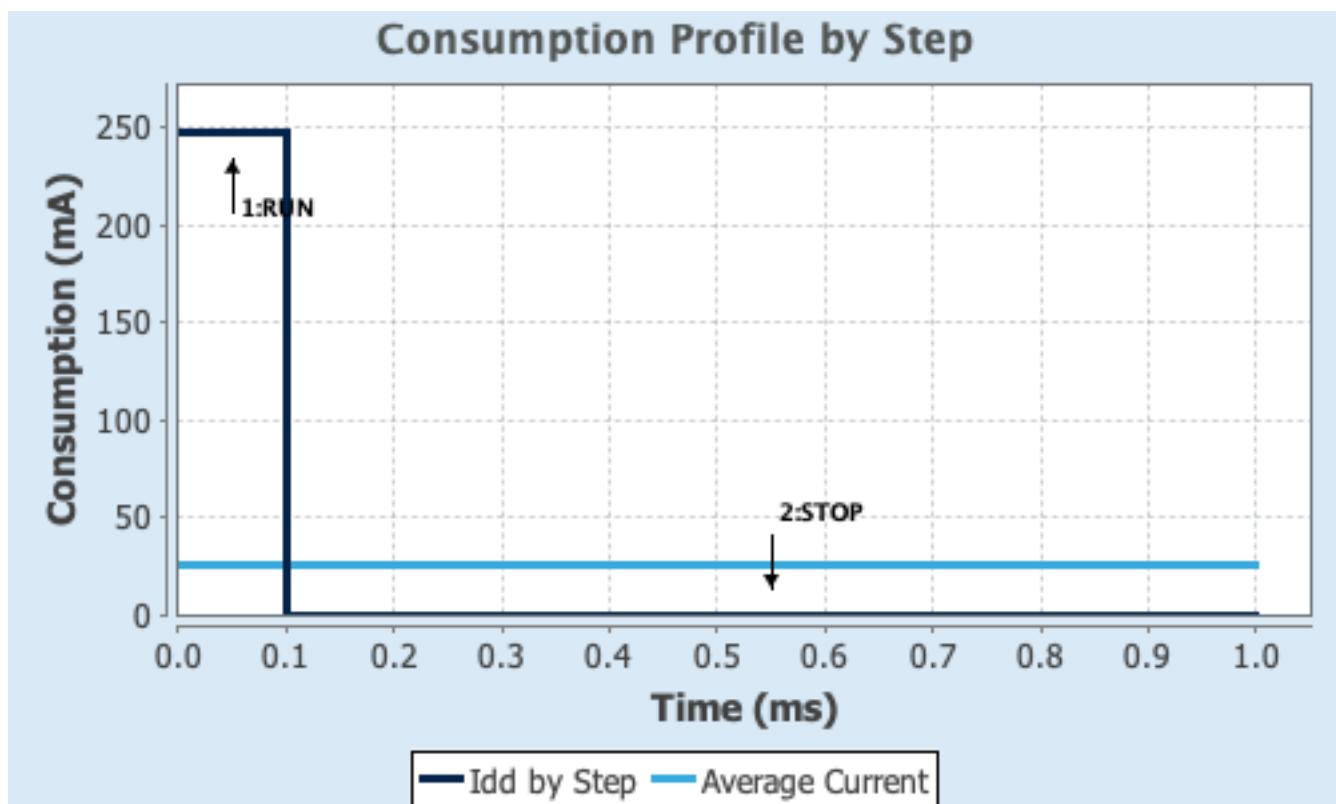
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN/CRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	CM7: ITCM/Cache / CM4: FLASH_B/ART	CM7: NA / CM4: NA
CM7 Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL IPs ON	LSE Flash-ON
CM4 Frequency	240 MHz	0 Hz
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	247 mA	145 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	24.83 mA
Battery Life	1 month, 29 days, 21 hours	Average DMIPS	1027.2001 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	nuh755ziq_board_test
Project Folder	/Users/sata/STM32CubeIDE/workspace_2.0.0/nuh755ziq_board_test
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.12.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls ARM Cortex-M7

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_TIM13_Init	TIM13

2.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_TIM14_Init	TIM14
3	MX_USART3_UART_Init	USART3

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3. Peripherals and Middlewares Configuration

3.1. CORTEX_M7

3.1.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Speculation default mode Settings:

Speculation default mode	Enabled *
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Cortex Interface Settings:

CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers
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Cortex Memory Protection Unit Region 0 Settings:

MPU Region	Enabled
MPU Region Base Address	0x0 *
MPU Region Size	4GB
MPU SubRegion Disable	0x87 *
MPU TEX field level	level 0
MPU Access Permission	ALL ACCESS NOT PERMITTED
MPU Instruction Access	DISABLE
MPU Shareability Permission	ENABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 2 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 3 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 4 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 5 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 6 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region Disabled

3.2. DEBUG

Debug: Trace Asynchronous Sw

3.2.1. Core(s) Settings:

Context(s): Cortex-M7

 Cortex-M4

Initialized Context: Cortex-M7

Power Domain:

3.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

3.3.1. Parameter Settings:

Core(s) Settings:

Context(s): Cortex-M7

Cortex-M4

Initialized Context:

Cortex-M7

Power Domain:

D3

Power Parameters:

SupplySource	PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
CSI Calibration Value	32
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)
Product revision	rev.V

PLL range Parameters:

PLL1 clock Input range	Between 4 and 8 MHz
PLL1 clock Output range	Wide VCO range

3.4. SYS_M4

Timebase Source: SysTick

3.4.1. Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	

3.5. SYS

Timebase Source: SysTick

3.5.1. Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	

3.6. TIM13

mode: Activated

3.6.1. Parameter Settings:

Core(s) Settings:

Context(s): Cortex-M7
Initialized Context: Cortex-M7
Power Domain: D2

Counter Settings:

Prescaler (PSC - 16 bits value) 199 *
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division
auto-reload preload Disable

3.7. TIM14

mode: Activated

3.7.1. Parameter Settings:

Core(s) Settings:

Context(s): Cortex-M4
Initialized Context: Cortex-M4
Power Domain: D2

Counter Settings:

Prescaler (PSC - 16 bits value) 199 *
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division
auto-reload preload Disable

3.8. USART3

Mode: Asynchronous

3.8.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PB3 (JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
GPIO	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4

* Initialized context

4.2. DMA configuration

nothing configured in DMA service

4.3. BDMA configuration

nothing configured in DMA service

4.4. MDMA configuration

nothing configured in DMA service

4.5. NVIC configuration

4.5.1. NVIC1

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD and AVD interrupts through EXTI line 16		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
TIM8 update interrupt and TIM13 global interrupt		unused	
CM4 send event interrupt for CM7		unused	
FPU global interrupt		unused	
HSEM1 global interrupt		unused	
Hold core interrupt		unused	

4.5.2. NVIC1 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

4.5.3. NVIC2

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0

Interrupt Table	Enable	Preenemption Priority	SubPriority
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD and AVD interrupts through EXTI line 16		unused	
Flash global interrupt		unused	
USART3 global interrupt		unused	
TIM8 trigger and commutation interrupts and TIM14 global interrupt		unused	
CM7 send event interrupt for CM4		unused	
FPU global interrupt		unused	
HSEM2 global interrupt		unused	
Hold core interrupt		unused	

4.5.4. NVIC2 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

The screenshot shows the 'Category view' of the System View. At the top, there are tabs: 'Category view' (which is selected), 'Context Execution view', 'Context Initialization view', and 'Power Domain view'. Below these tabs are three filter sections:

- '... by Context Execution': Contains checkboxes for 'Cortex-M7' (unchecked) and 'Cortex-M4' (unchecked).
- '... by Context Initialization': Contains radio buttons for 'Cortex-M7' (unchecked), 'Cortex-M4' (unchecked), and 'None' (checked).
- '... by Power Domain': Contains radio buttons for 'D1' (unchecked), 'D2' (unchecked), 'D3' (unchecked), and 'None' (checked).

In the center, there is a large empty box labeled 'Middleware'.

Below the filter sections, there is a navigation bar with categories: System Core, Analog, Timers, Connectivity, Multimedia, Security, Computing, Trace and Debug, Power and Thermal, Utilities, and Other. Under 'System Core', several components are listed with checkboxes:

- BDMA (checked)
- CORTEX_M4 (unchecked)
- CORTEX_M7 (checked)
- DMA (unchecked)
- GPIO (checked)
- MDMA (unchecked)
- NVIC1 (checked)
- NVIC2 (checked)
- RCC (checked)
- SYS_M4 (checked)
- SYS_M7 (checked)

Under 'Timers', two components are listed with checkboxes:

- TIM13 (checked)
- TIM14 (checked)

Under 'Connectivity', one component is listed with a checkbox:

- USART3 (checked)

Under 'Trace and Debug', one component is listed with a checkbox:

- DEBUG (checked)

5.1.2. Without filters

The screenshot shows the NXP i.MX 755 Configuration tool interface. At the top, there are four navigation tabs: "Category view" (selected), "Context Execution view", "Context Initialization view", and "Power Domain view". Below these are three filter sections: "... by Context Execution" (checkboxes for Cortex-M7 and Cortex-M4, both unchecked), "... by Context Initialization" (radio buttons for Cortex-M7, Cortex-M4, and None, with None selected), and "... by Power Domain" (radio buttons for D1, D2, D3, and None, with None selected). A large empty box labeled "Middleware" is present. The main content area is the "System Core" tab, which lists the following components:

System Core
BDMA
CORTEX_M4
CORTEX_M7 (✓)
DMA
GPIO (✓)
MDMA
NVIC1 (✓)
NVIC2 (✓)
RCC (✓)
SYS_M4 (✓)
SYS_M7 (✓)

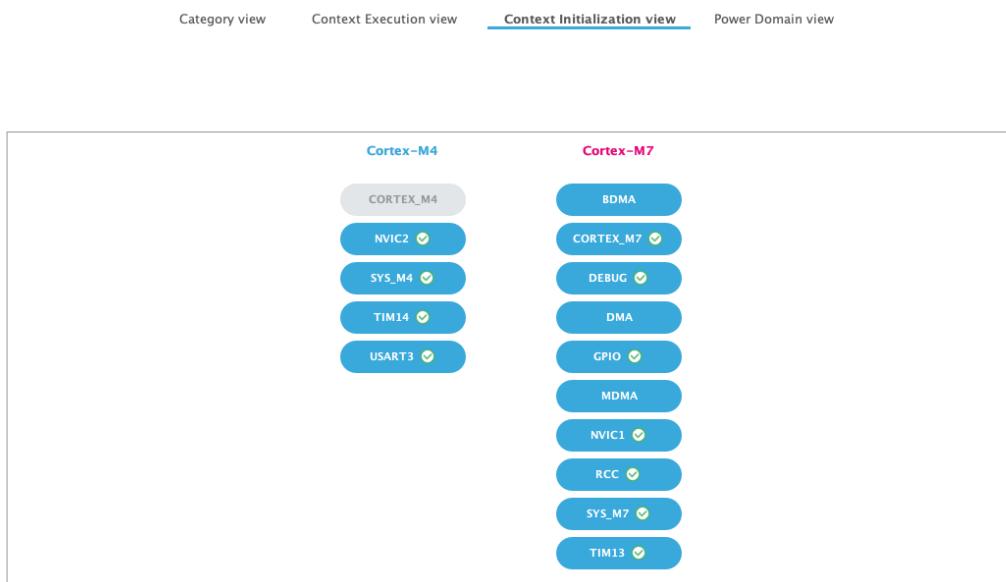
Below the System Core tab, there are other tabs: Analog, Timers, Connectivity, Multimedia, Security, Computing, Trace and Debug, Power and Thermal, Utilities, and Other. Under the Timers tab, components TIM13 and TIM14 are listed. Under the Connectivity tab, USART3 is listed. Under the Computing tab, DEBUG is listed.

5.2. Context Execution view

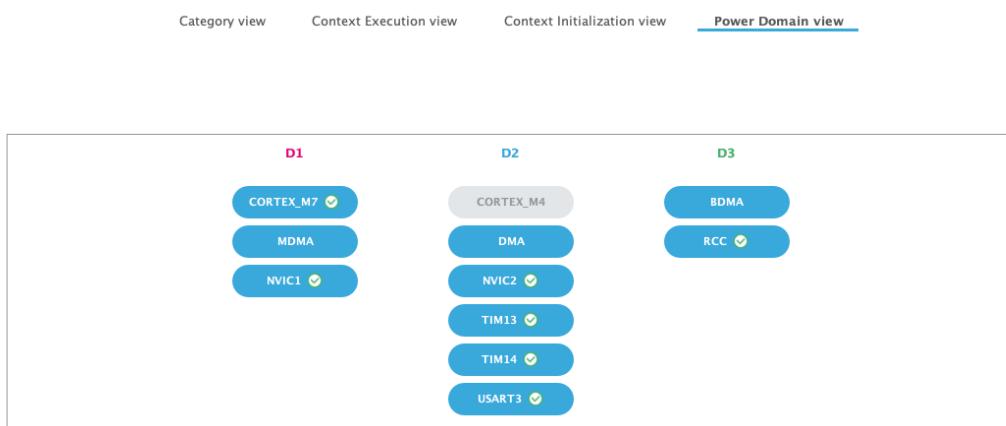
Category view Context Execution view Context Initialization view Power Domain view



5.3. Context Initialization view



5.4. Power Domain view



6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View	https://www.st.com/resource/en/svd/stm32h7-svd.zip
Description	
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32h7rs.pdf
Security Bulletin	https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf
Security Bulletin	https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-

guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4539-hrtim-cookbook-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4839-level-1-cache-on-stm32f7-series-and-stm32h7-series-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4990-getting-started-with-sigmadelta-digital-interface-on-applicable-stm32-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5027-interfacing-pdm-digital-microphones-using-stm32-mcus-and-mpus-stmicroelectronics.pdf

- Application Notes https://www.st.com/resource/en/application_note/an5033-stm32cube-mcu-package-examples-for-stm32h7-series-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5073-receiving-spdif-audio-stream-with-the-stm32f4f7h7-series-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5286-stm32h7x5x7-dualcore-microcontroller-debugging-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5354-getting-started-with-the-stm32h7-series-mcu-16bit-adc-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5557-stm32h745755-and-stm32h747757-lines-dualcore-architecture-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5617-stm32h745755-and-stm32h747757-lines-interprocessor-communications-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4899-stm32-microcontroller-gpio-hardware-settings-and-lowpower-consumption-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5612-esd-protection-of-stm32-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5293-migration-guide-from-stm32f7-series-to-stmh74x75x-stm32h72x73x-and-stmh7a37bx-devices-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4991-how-to-wake-up-an-stm32-microcontroller-from-lowpower-mode-with-the-usart-or-the-lpuart-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4838-introduction-to-memory-protection-unit-management-on-stm32-mcus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5927-i3c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5225-introduction-to-usb-typec-power-delivery-for-stm32-mcus-and-mpus-stmicroelectronics.pdf
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error-correction-code-ecc-management-for-internal-memories-protection-on-stm32-mcus-stmicroelectronics.pdf

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