



1. Description

1.1. Project

Project Name	Zadanie1
Board Name	custom
Generated with:	STM32CubeMX 6.14.0
Date	10/31/2025

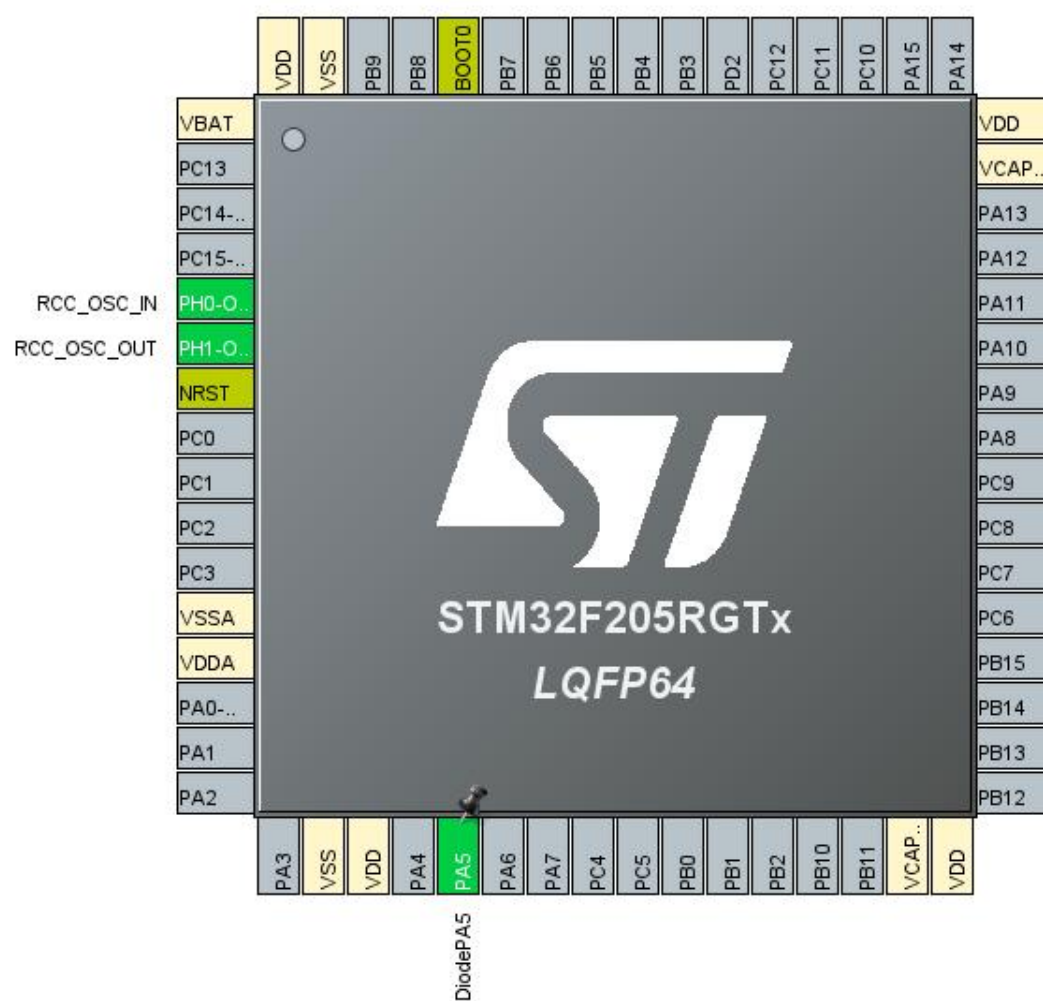
1.2. MCU

MCU Series	STM32F2
MCU Line	STM32F2x5
MCU name	STM32F205RGTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M3
---------	---------------

2. Pinout Configuration

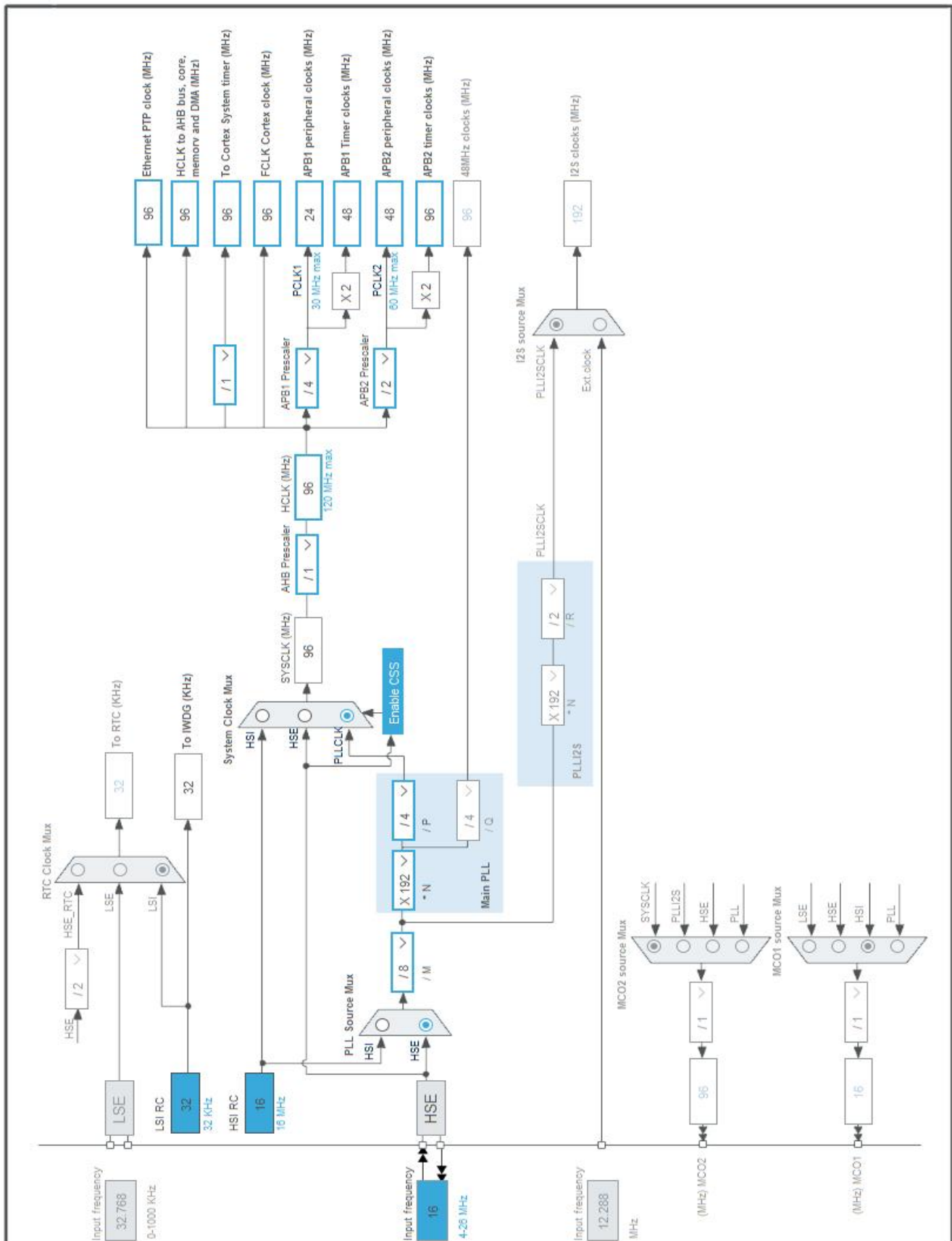


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
18	VSS	Power		
19	VDD	Power		
21	PA5 *	I/O	GPIO_Output	DiodePA5
31	VCAP_1	Power		
32	VDD	Power		
47	VCAP_2	Power		
48	VDD	Power		
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F2
Line	STM32F2x5
MCU	STM32F205RGTx
Datasheet	DS6329_Rev15

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

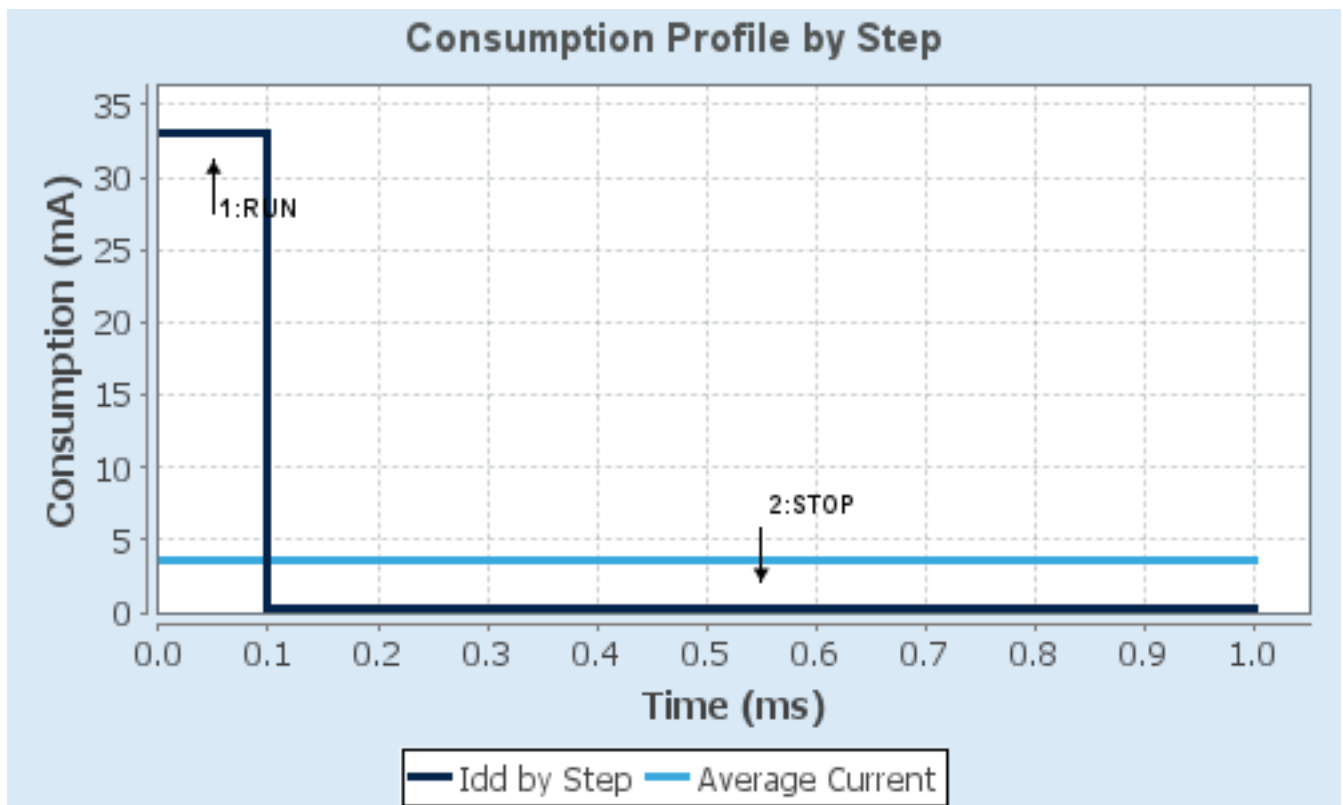
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No-Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	120 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	33 mA	300 μ A
Duration	0.1 ms	0.9 ms
DMIPS	150.0	0.0
Ta Max	100.1	104.96
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	3.57 mA
Battery Life	1 month, 9 days, 5 hours	Average DMIPS	150.0 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	Zadanie1
Project Folder	C:\Users\Dell\STM32CubeIDE\workspace_1.18.0\Zadanie1
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F2 V1.9.5
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_IWDG_Init	IWDG
4	MX_TIM3_Init	TIM3

3. *Peripherals and Middlewares Configuration*

3.1. IWDG

mode: Activated

3.1.1. Parameter Settings:

Clocking:

IWDG counter clock prescaler	4
IWDG down-counter reload value	4095

3.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

3.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

3.3. SYS

Timebase Source: SysTick

3.4. TIM3

Clock Source : Internal Clock

3.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	239 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535

Internal Clock Division (CKD)

No Division

auto-reload preload

Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection

Reset (UG bit from TIMx_EGR)

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
GPIO	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DiodePA5

4.2. DMA configuration

nothing configured in DMA service

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
TIM3 global interrupt	true	0	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM3 global interrupt	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

Middleware

System Core

Analog

Timers

Connectivity

Multimedia

Security

Computing

DMA

TIM3 

GPIO 

IWDG 

NVIC 

RCC 

SYS 

6. Docs & Resources

Type	Link
------	------