Date:
16-04-2020

CS226: Switching Theory Lab

Lab 9

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Ans 1 To design an n-bit synchronous counter, the following steps are to be followed,

(1) Decide number of Flipflops

(2) Draw the excitation table of flipflop

(3) Draw excitation table of circuit

(4) Obtain simplified expressions using K-Map

(5) Draw the logic diagram, every flip flop should be connected in parallel, to the clock.

Implementations of 4-bit counter using,

I) SR flip flop (L9Q1_SR.circ):

Step1: Because we need a 4-bit counter, we use 4 SR flip flops

(P.T.O)

Step 2: Draw the excitation table of SR flip flop

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

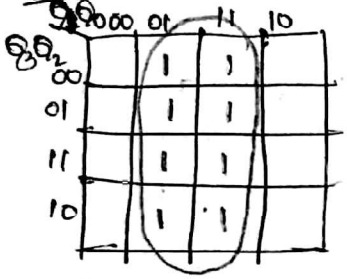
Step 3: Circuit Excitation Table

t-1 ∪ t

Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	S_3	R_3	S_2	R_2	S_1	R_1	S_0	R_0
0	0	0	0	0	0	0	1	0	x	0	x	0	x	1	0
0	0	0	1	0	0	1	0	0	x	0	x	1	0	0	1
0	0	1	0	0	0	1	1	0	x	0	x	x	0	1	0
0	0	1	1	0	1	0	0	0	x	1	0	0	1	0	1
0	1	0	0	0	1	0	1	0	x	x	0	0	x	1	0
0	1	0	1	0	1	1	0	0	x	x	0	1	0	0	1
0	1	1	0	0	1	1	1	0	x	x	0	x	0	1	0
0	1	1	1	1	0	0	0	1	0	0	1	0	1	0	1
1	0	0	0	1	0	0	1	x	0	0	x	0	x	1	0
1	0	0	1	1	0	1	0	x	0	0	x	1	0	0	1
1	0	1	0	1	0	1	1	x	0	0	x	x	0	1	0
1	0	1	1	1	1	0	0	x	0	1	0	0	1	0	1
1	1	0	0	1	1	0	1	x	0	x	0	0	x	1	0
1	1	0	1	1	1	1	0	x	0	x	0	1	0	0	1
1	1	1	0	1	1	1	1	x	0	x	0	x	0	1	0
1	1	1	1	0	0	0	0	0	1	0	1	0	1	0	1

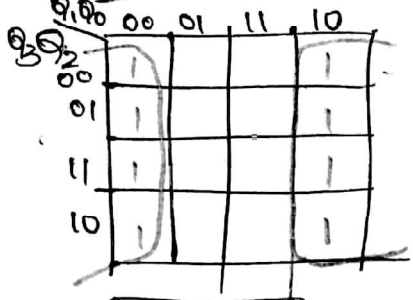
Step4: Expressions for $S3, R3, S2, R2, S1, R1, S0, R0$ by KMaps in terms of $Q3(t-1), Q2(t-1), Q1(t-1), Q0(t-1)$

R_0



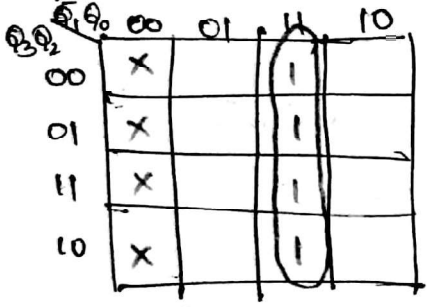
$R_0 = Q_0$

S_0



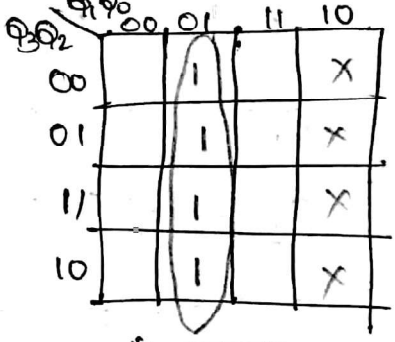
$S_0 = \bar{Q}_0$

R_1



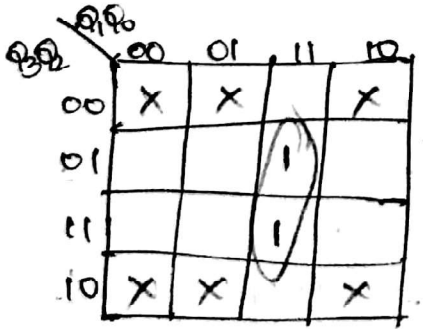
$R_1 = Q_1 Q_0$

S_1



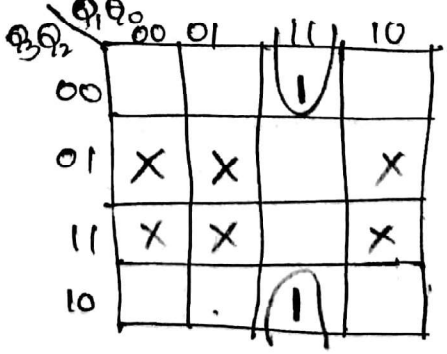
$S_1 = \bar{Q}_1 Q_0$

R_2



$R_2 = Q_2 Q_1 Q_0$

S_2



$S_2 = \bar{Q}_2 Q_1 Q_0$

R_3

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	X	X
01	X	X		X
11			1	
10				

$R3 = Q_3Q_2Q_1Q_0$

S_3

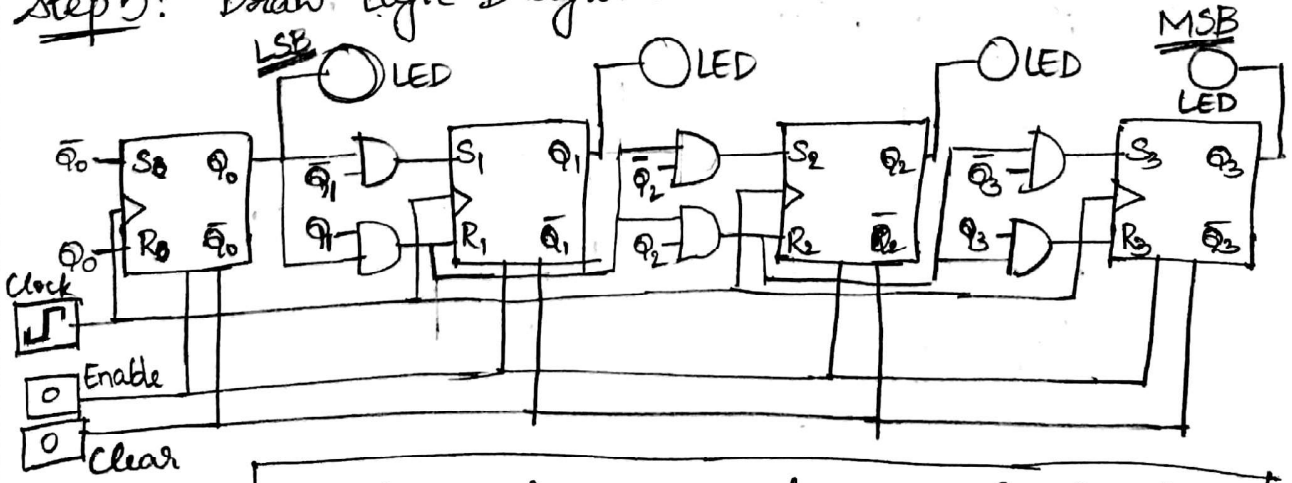
Q_3Q_2 \ Q_1Q_0	00	01	11	10
00				
01			1	
11	X	X		X
10	X	X	X	X

$S3 = \bar{Q}_3 Q_2 Q_1 Q_0$

So the eqn's are:

$S0 = \bar{Q}_0(t+1)$	$S_1 = \bar{Q}_1(t-1)Q_0(t-1)$
$R_0 = Q_0(t+1)$	$R_1 = Q_1(t-1)Q_0(t-1)$
$S_2 = \bar{Q}_2(t-1)Q_1(t-1)Q_0(t-1) = \bar{Q}_2(t-1)R_1$	
$R_2 = Q_2(t-1)Q_1(t-1)Q_0(t-1) = Q_2(t-1)R_1$	
$S_3 = \bar{Q}_3(t-1)Q_2(t-1)Q_1(t-1)Q_0(t-1) = \bar{Q}_3(t-1)R_2$	
$R_3 = Q_3(t-1)Q_2(t-1)Q_1(t-1)Q_0(t-1) = Q_3(t-1)R_2$	

Step 5: Draw Logic Diagram



4-bit synchronous counter using SR flipflops

II) JK flip flop (L9Q1_JK.circ):

Step1: For 4-bit counter we use 4 JK flipflops

Step2: Excitation Table of JK flipflop

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

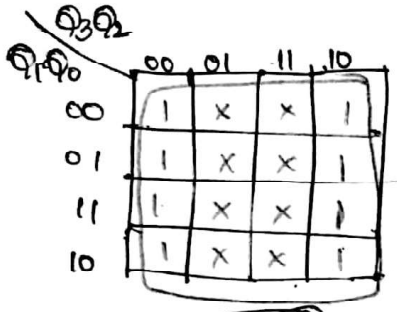
Step3: Excitation Table of Circuit

(t-1)				(t)									
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	J3 K3	J2 K2	J1 K1	J0 K0
0	0	0	0	0	0	0	1	0 x	0 x	0 x	1 x
0	0	0	1	0	0	1	0	0 x	0 x	1 x	x 1
0	0	1	0	0	0	1	1	0 x	0 x	x 0	1 x
0	0	1	1	0	1	0	0	0 x	1 x	x 1	x 1
0	1	0	0	0	1	0	1	0 x	x 0	0 x	1 x
0	1	0	1	0	1	1	0	0 x	x 0	1 x	x 1
0	1	1	0	0	1	1	1	0 x	x 0	1 x	x 1
0	1	1	1	1	0	0	0	1 x	x 1	x 1	x 1
1	0	0	0	1	0	0	1	x 0	0 x	0 x	1 x
1	0	0	1	1	0	1	0	x 0	0 x	1 x	x 1
1	0	1	0	1	0	1	1	x 0	0 x	x 0	1 x
1	0	1	1	1	1	0	0	x 0	x x	x 1	x 1
1	1	0	0	1	1	0	1	x 0	x 0	0 x	1 x
1	1	0	1	1	1	1	0	x 0	x 0	1 x	x 1
1	1	1	0	1	1	1	1	x 0	x 0	x 0	1 x
1	1	1	1	0	0	0	0	x 1	x 1	x 1	x 1

Step4: Expressions for J_3, J_2, J_1, J_0
K_3, K_2, K_1, K_0 in terms of

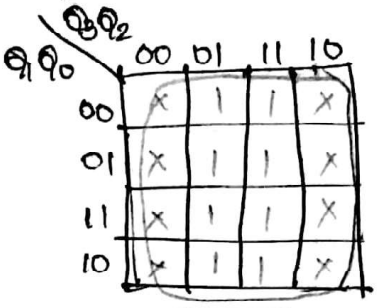
$Q_3(t-1), Q_2(t-1), Q_1(t-1), Q_0(t-1)$ by K-Map

J_0



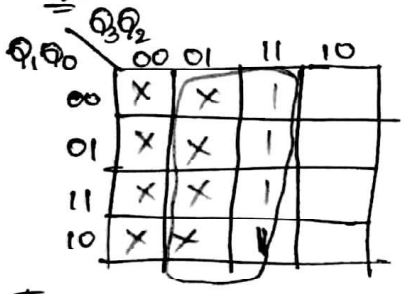
$J_0 = 1$

K_0

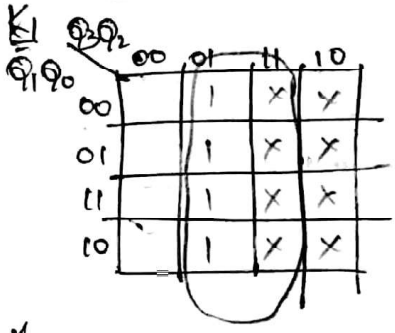


$K_0 = 1$

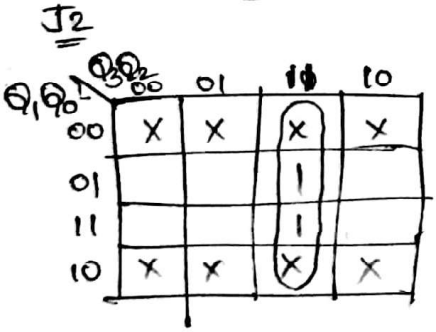
J_1



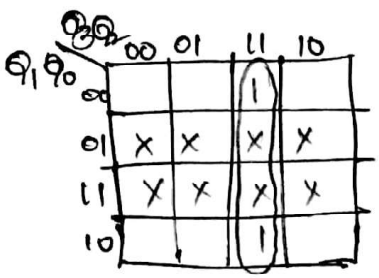
K_1



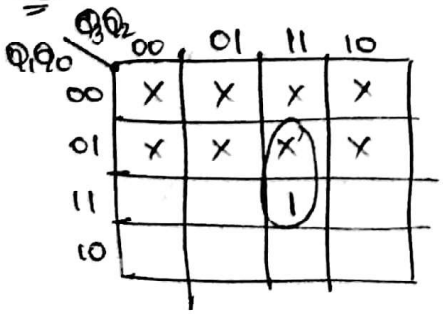
J_2



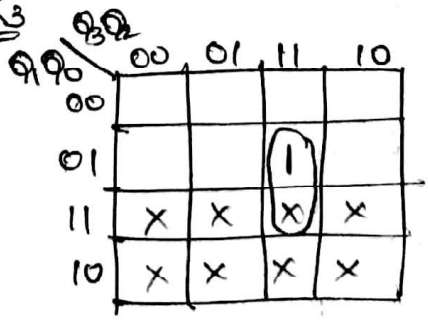
K_2



J_3



K_3



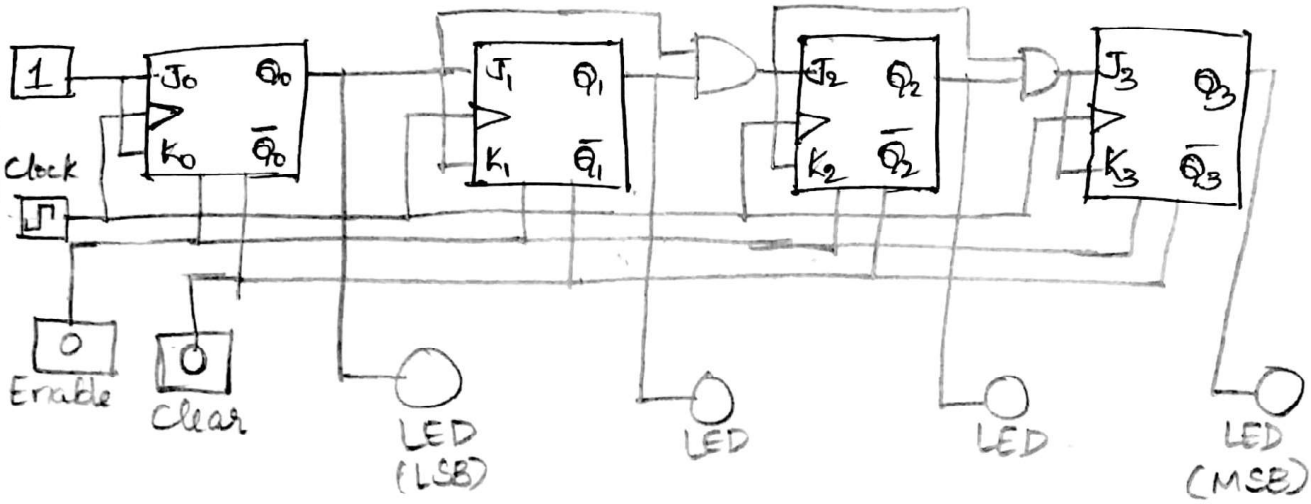
Eqn's are: $J_0 = K_0 = 1$

$J_1 = K_1 = Q_0$

$J_2 = K_2 = Q_1Q_0$

$J_3 = K_3 = Q_2Q_1Q_0 = Q_2J_2$

Step5: Logic Diagram



III) T flip-flop (L9Q1_T.circ):

Step1: No. of T flip flops = 4

Step2: Excitation Table for T flipflop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

(PTO)

Step3: Excitation Table of Circuit

(t-1)				(t)							
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	1	0	1	0	0	0	1	1
1	0	1	0	1	0	1	1	0	0	0	1
1	0	1	1	1	1	0	0	0	1	1	1
1	1	0	0	1	1	0	1	0	0	0	1
1	1	0	1	1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1	0	0	0	1
1	1	1	1	0	0	0	0	1	1	1	1

Step 4: Expressions for T_3, T_2, T_1, T_0

$T_0 = 1$

$T_1 = Q_0(t-1)$

$T_2 = Q_1(t-1)Q_0(t-1)$

$T_3 = Q_2(t-1)Q_1(t-1)Q_0(t-1)$

$T_0 = 1$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$T_1 = Q_0$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00		1	1	
01		1	1	
11		1	1	
10		1	1	

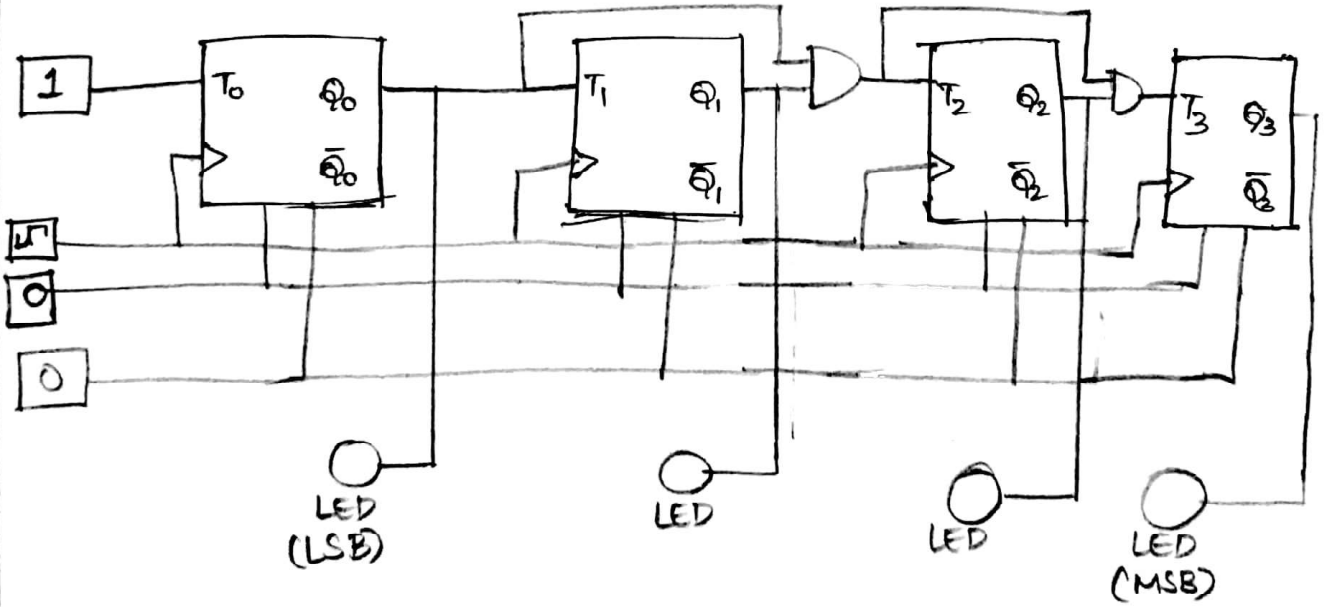
Q_3Q_2 \ Q_1Q_0	00	01	11	10
00			1	
01			1	
11			1	
10			1	

$T_2 = Q_1Q_0$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00				
01			1	
11			1	
10				

$T_3 = Q_2Q_1Q_0$

Step 5: Logic Diagram



(P.T.O)

IV) D-flip flop:

Step1: No. of D-flip flops = 4

Step2: Excitation table of D-flipflop

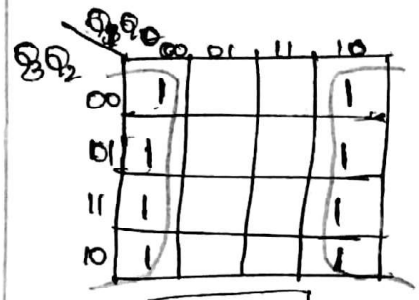
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	1	0
1	0	1

Step3: Circuit Excitation Table

Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	1	1	0	0	1	1	0	0
1	1	0	0	1	1	0	1	1	1	0	1
1	1	0	1	1	1	1	0	1	1	1	0
1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	0	0	0	0	0	0	0	0

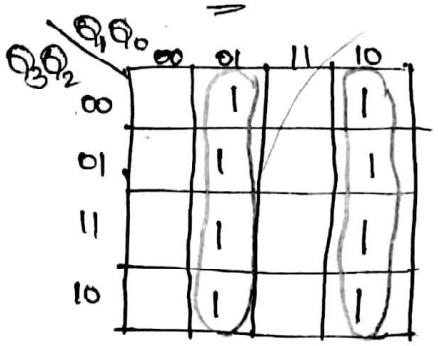
Step 4: Expressions for D_3, D_2, D_1, D_0

D_0



$$D_0 = \bar{Q}_0$$

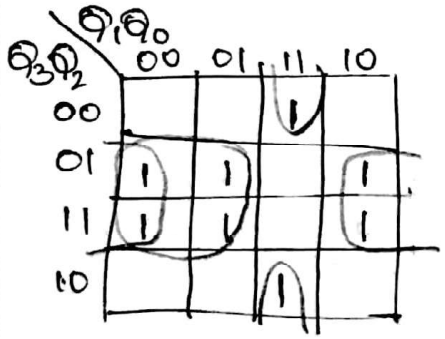
D_1



$$D_1 = \bar{Q}_1 Q_0 + Q_1 \bar{Q}_0$$

$$D_1 = Q_1 \oplus Q_0$$

D_2

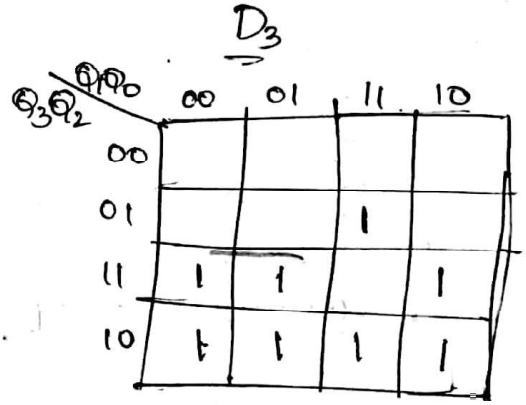


$$D_2 = \bar{Q}_2 Q_1 Q_0 + Q_2 \bar{Q}_1 + Q_2 \bar{Q}_0$$

$$= \bar{Q}_2 (Q_1 Q_0) + Q_2 (\bar{Q}_1 + \bar{Q}_0)$$

$$\Rightarrow D_2 = Q_2 \oplus Q_1 Q_0$$

D_3



$$D_3 = Q_3 \bar{Q}_1 + Q_3 \bar{Q}_2 Q_1 + Q_3 Q_1 \bar{Q}_0 + \bar{Q}_3 Q_2 Q_1 Q_0$$

$$= Q_3 (\bar{Q}_1 + \bar{Q}_2 Q_1 + Q_1 \bar{Q}_0) + \bar{Q}_3 Q_2 Q_1 Q_0$$

$$= Q_3 (\bar{Q}_0 + \bar{Q}_1 + \bar{Q}_2) + \bar{Q}_3 Q_2 Q_1 Q_0$$

$$\Rightarrow D_3 = Q_3 \oplus Q_2 Q_1 Q_0$$

Eqn's are:

$D_0 = \bar{Q}_0$ $\quad D_1 = Q_1 \oplus Q_0$

$D_2 = Q_2 \oplus Q_1 Q_0$

$D_3 = Q_3 \oplus Q_2 Q_1 Q_0$

Step 5: Logic Diagram