Intro to VLSI

Lab Task 4 – Compound gate

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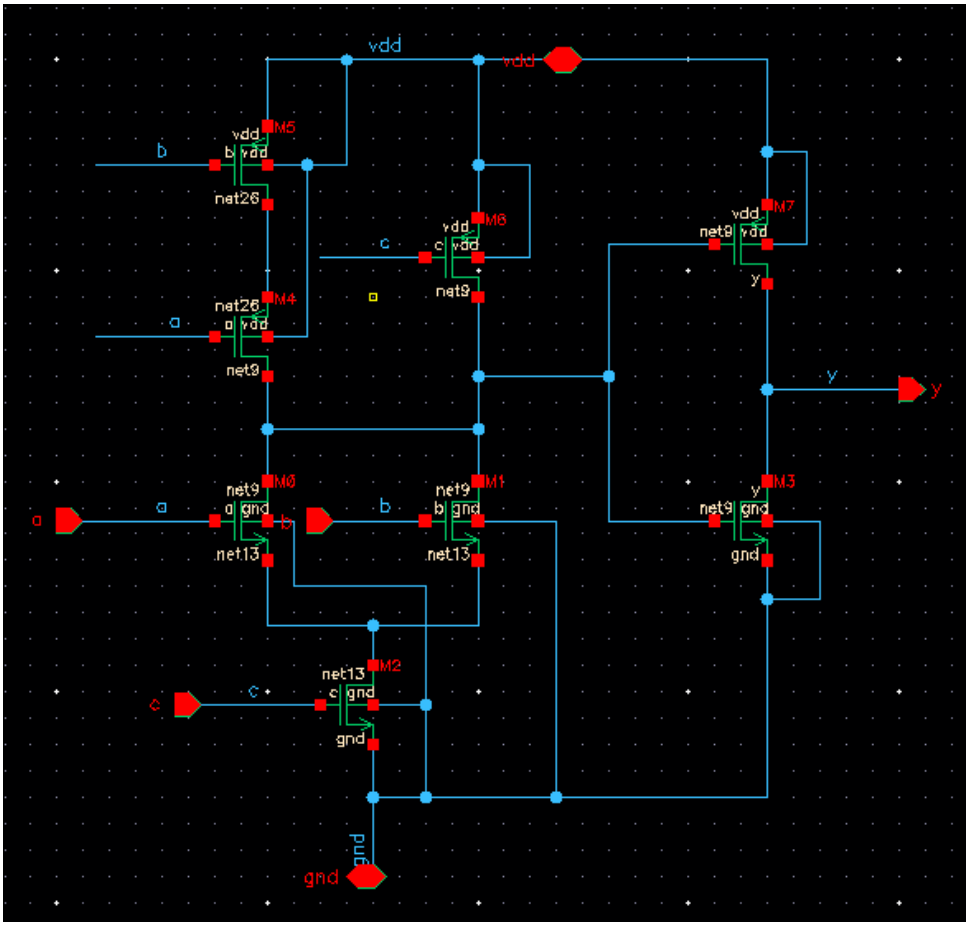
(20171049)

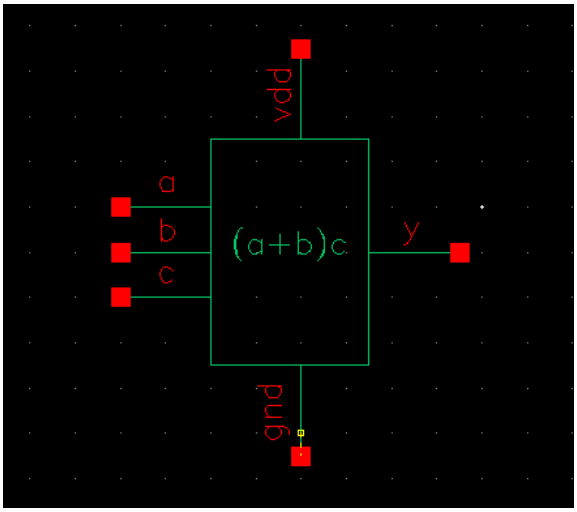
The logic which I have chosen to implement abd design a compound gate is : y=(a+b).c

I have designed the Compound gate schematic which is as shown in figure below:



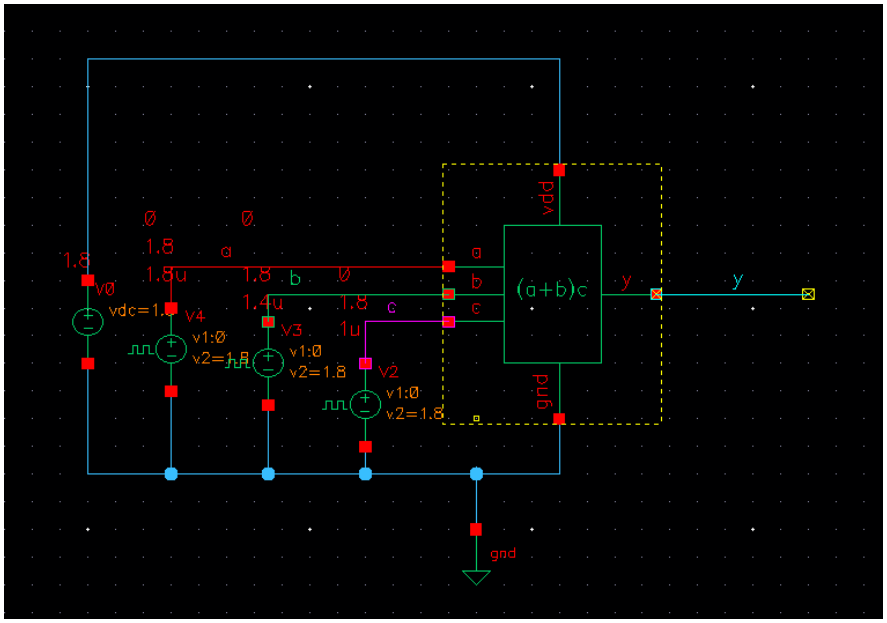
Schematic of Compound gate

Instead of applying power sources, I have attached pins in the schematic to create a symbol for it and then using it to test the working of the COMPOUND gate. So the symbol is created and shown below:



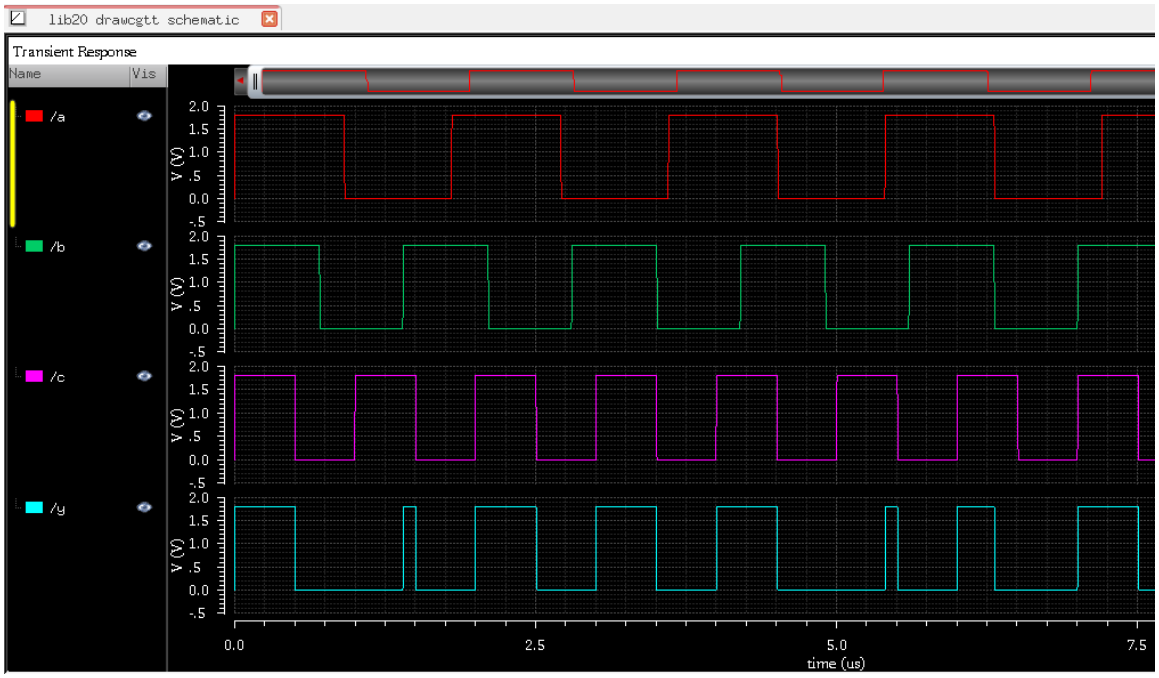
Symbol of Compound gate

Now, we have to test our symbol, so we add it in a new schematic, apply power sources and make the connections properly.



Circuit Diagram of Compound gate with symbol

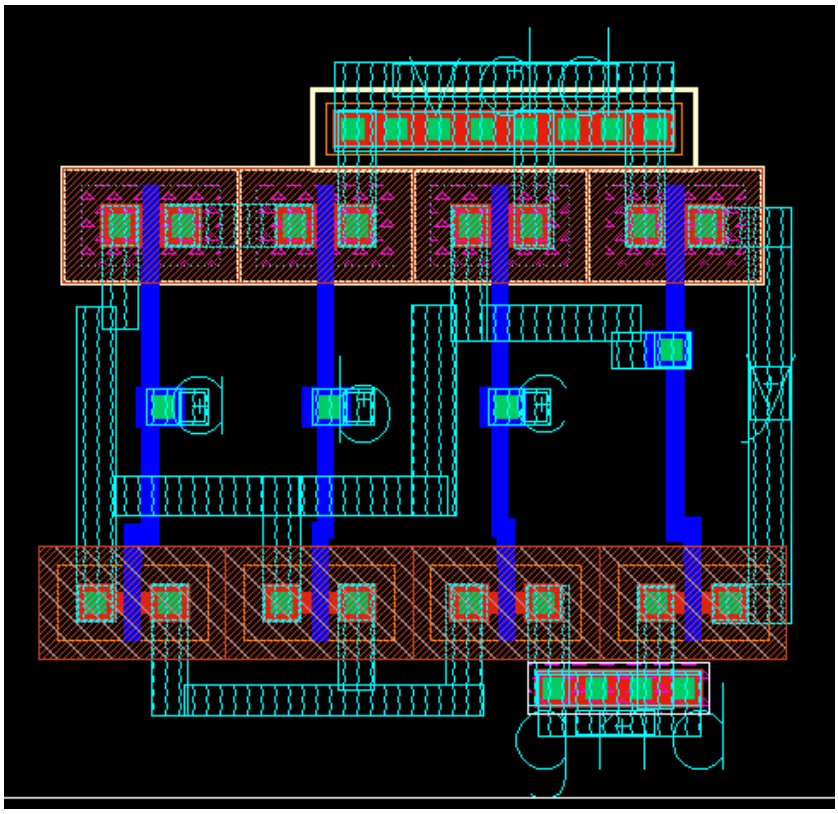
The results obtained from the Compound gate symbol are shown below, and it is verified that our Compound gate is working properly.



Inputs – a (red) , b (green) & c (purple). Output – y (blue)

The above graph shows that only when c is high and when at least one of a and b are high, then only output y, is high.

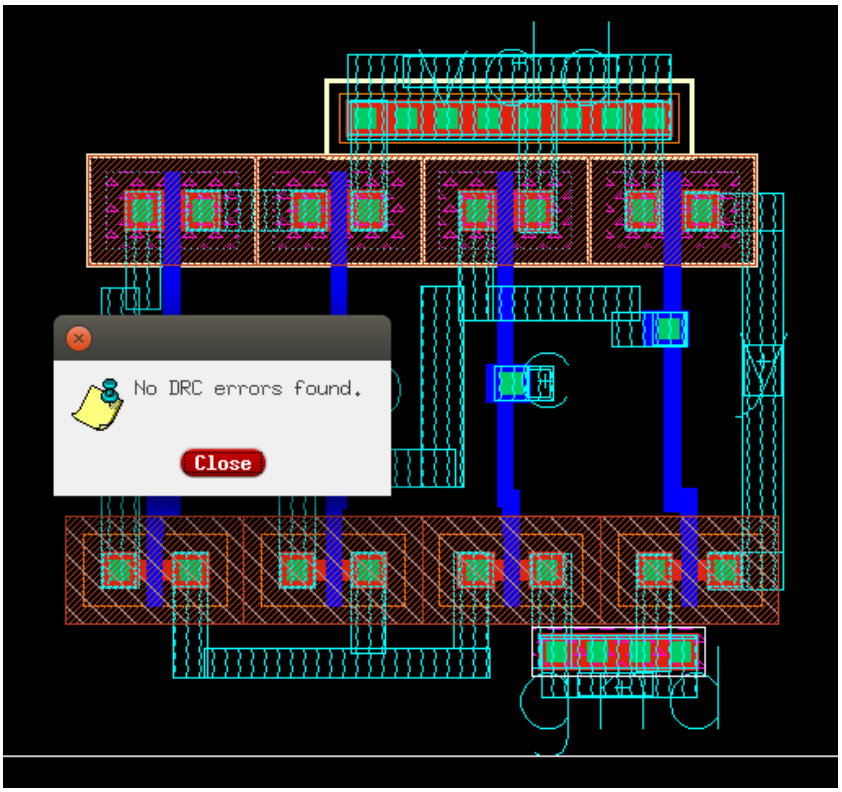
Now we will make the layout for our Compound gate, and draw it in accordance with the lambda rules. The layout formed is shown below:



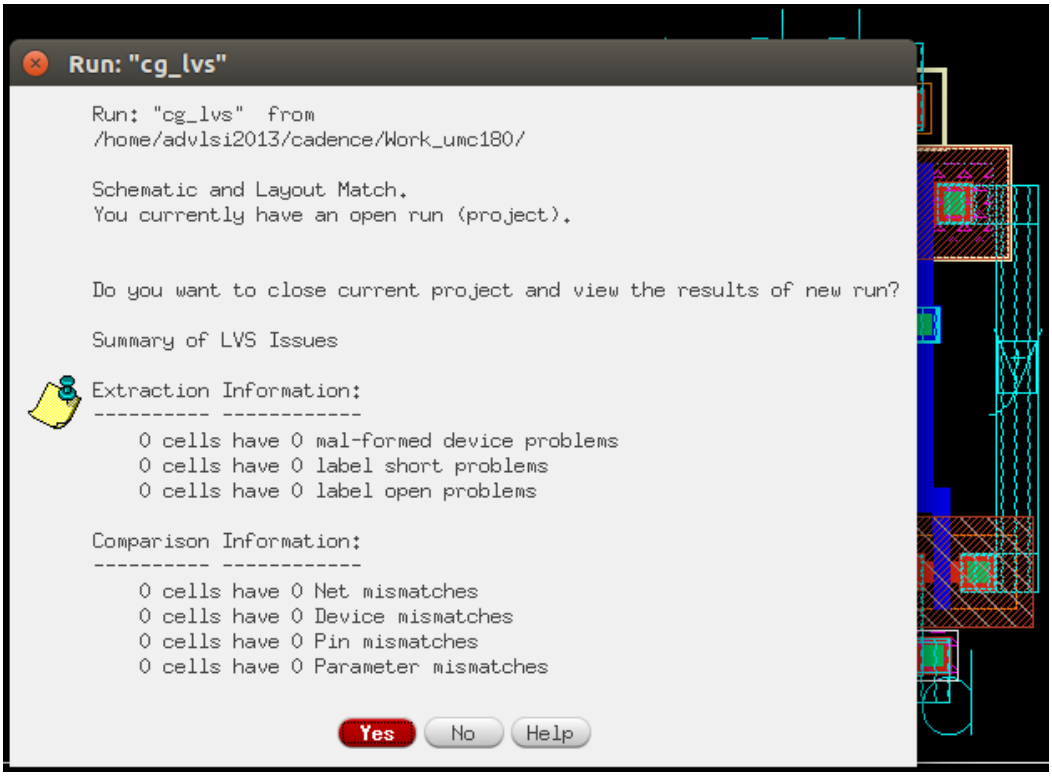
Layout of Compound gate

We have minimized the area and it is found that the minimized area is 7.224um x 8.691um = 62.783 um^2.

The results of the DRC test and LVS test were successful for the layout formed, i.e., there were no errors in the layout and also it is now matched with the schematic which we had drawn earlier.

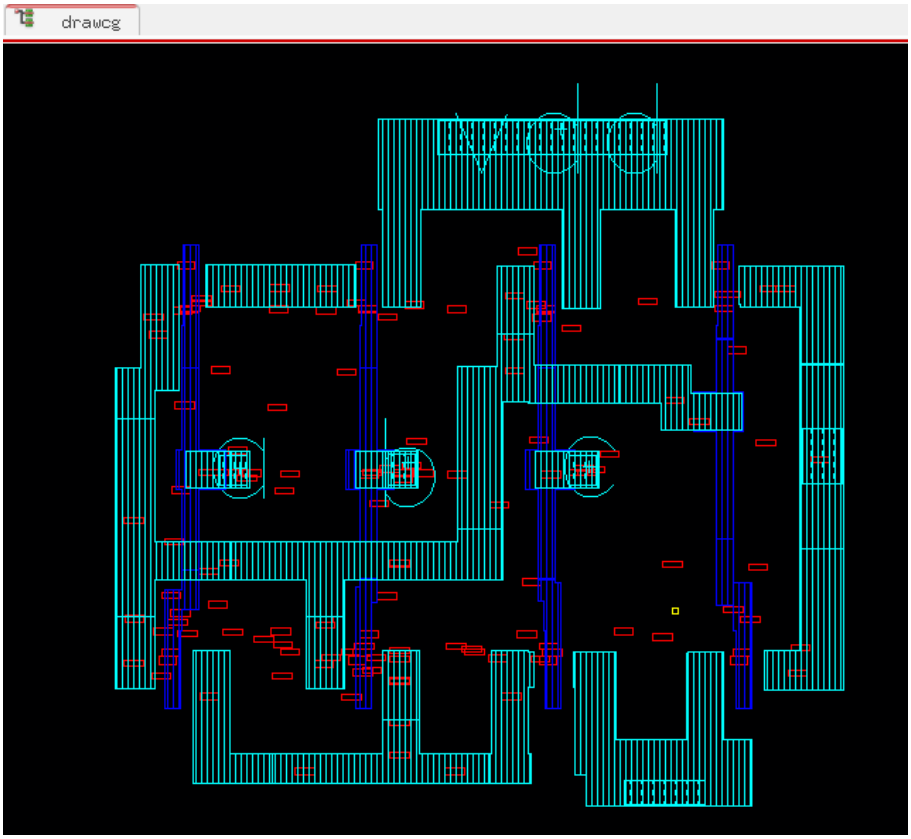


Result of DRC test (successful)



Result of LVS test (successful)

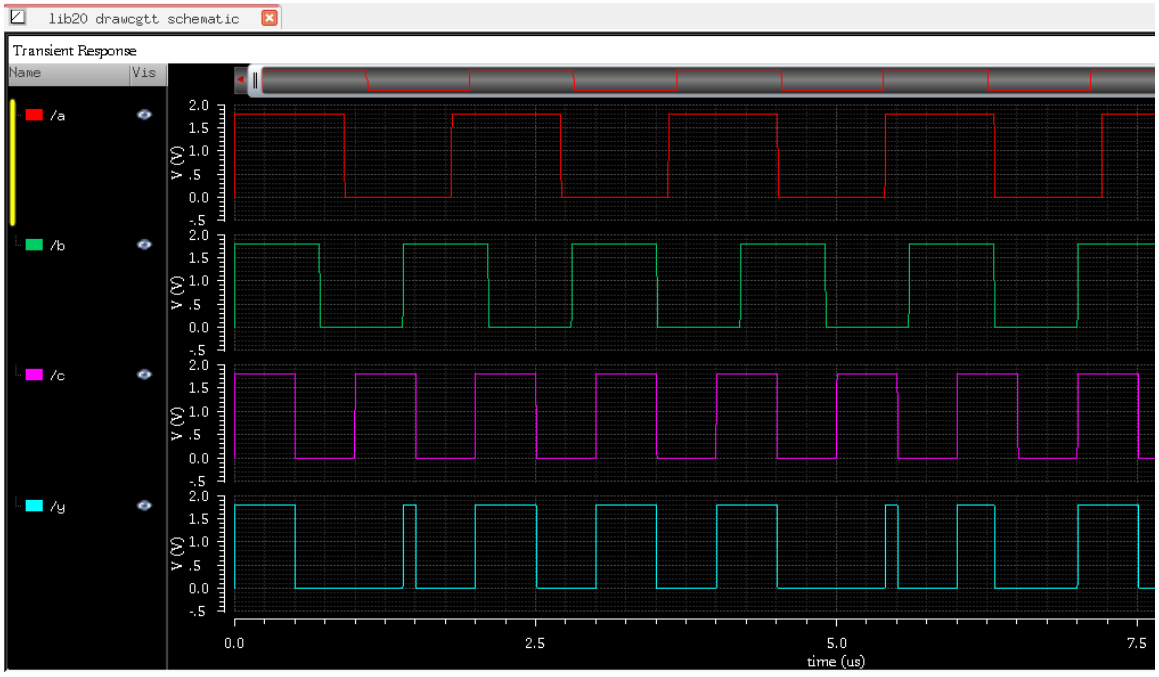
Now, the RCX test is run to generate the extracted view of the layout, which shows the presence of various parasitic capacitances and resistances and it is shown below:



Extracted view of the layout with parasitic capacitances and resistances

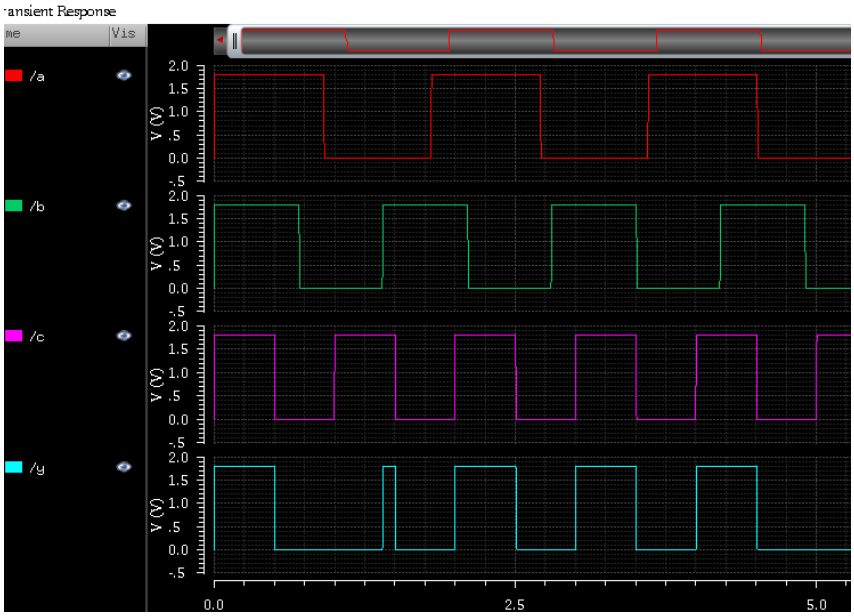
We can now ensure that our layout drawn also gives correct results. So, changing the hierarchy of our symbol from schematic to layout, the following results were obtained and we can see that the output is coming correctly from the transient analysis of the circuit. Also we can see the presence of multiple resistances, capacitances, and nodes in the results, which were not in the schematic.

```
    WARNING (SFE-30): "input.scs" 67: I2.M13: `mf' is not a valid para
    WARNING (SFE-30): "input.scs" 70: I2.M12: `nf' is not a valid para
    WARNING (SFE-30): "input.scs" 70: I2.M12: `mis_flag' is not a valid
        Further occurrences of this warning will be suppressed.


Time for Elaboration: CPU = 23.997 ms, elapsed = 28.6789 ms.
Time accumulated: CPU = 133.979 ms, elapsed = 227.994 ms.
Peak resident memory used = 25 Mbytes.


Time for EDB Visiting: CPU = 999 us, elapsed = 25.661 ms.
Time accumulated: CPU = 134.978 ms, elapsed = 253.838 ms.
Peak resident memory used = 25.3 Mbytes.


Warning from spectre during initial setup.
    WARNING (CMI-2426): I2.M10: `Cdscd' = -28.83e-06 is negative.
    WARNING (CMI-2426): I2.M6: `Pdiblc2' = -37.9166e-03 is negative.
    WARNING (CMI-2426): I2.M6: `Cdscd' = -500e-06 is negative.


Circuit inventory:
              nodes 38
           bsim3v3 8
           resistor 31
            vsource 3


Warning from spectre during initial setup.
    WARNING (CMI-2426): I2.M10: `Cdscd' = -28.83e-06 is negative.
    WARNING (CMI-2426): I2.M6: `Pdiblc2' = -37.9166e-03 is negative.
        Further occurrences of this warning will be suppressed.
Notice from spectre.
    20 warnings suppressed.


Time for parsing: CPU = 2 ms, elapsed = 7.27701 ms.
Time accumulated: CPU = 136.978 ms, elapsed = 261.304 ms.
Peak resident memory used = 26.1 Mbytes.
```

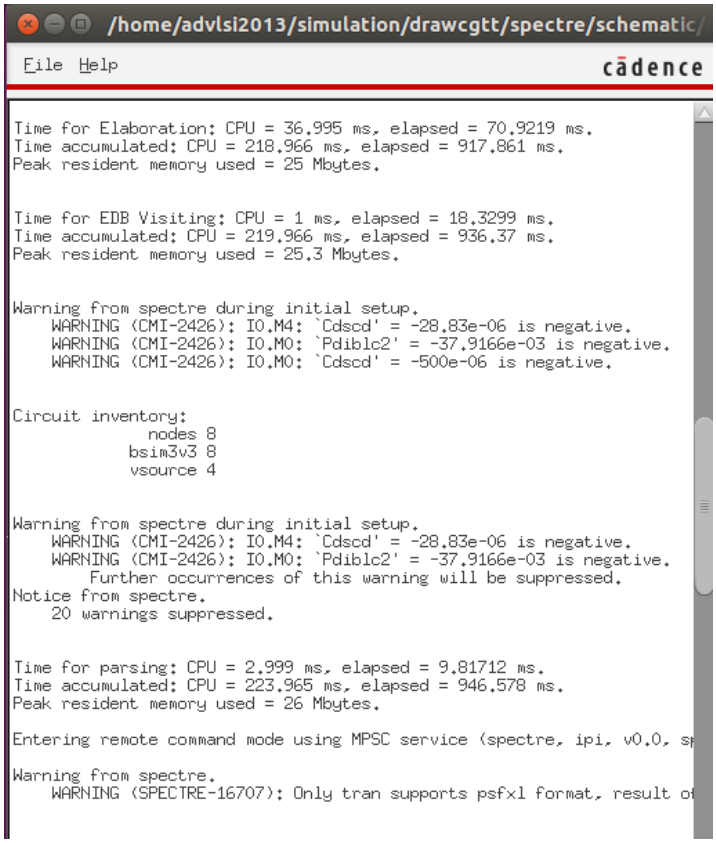


Inputs – a (red) , b (green) & c (purple). Output – y (blue)

Now, we compare the results of the original schematic with that of the results from layout hierarchy. Again transient analysis is done and results are as shown:



Inputs – a (red) , b (green) & c (purple). Output – y (blue)



So, the comparison between the results of the layout and the schematic of the Compound gate are approximately same. There are very little distortions in the output waveforms of the layout which is not in the case of schematic. So, the layout and the schematic are successfully verified theoretically also. Thus our Compound gate design is successfully completed. Also the area of the layout was minimized and was found to be 62.783 um^2.