Intro to VLSI

Lab Task 6 – Adder

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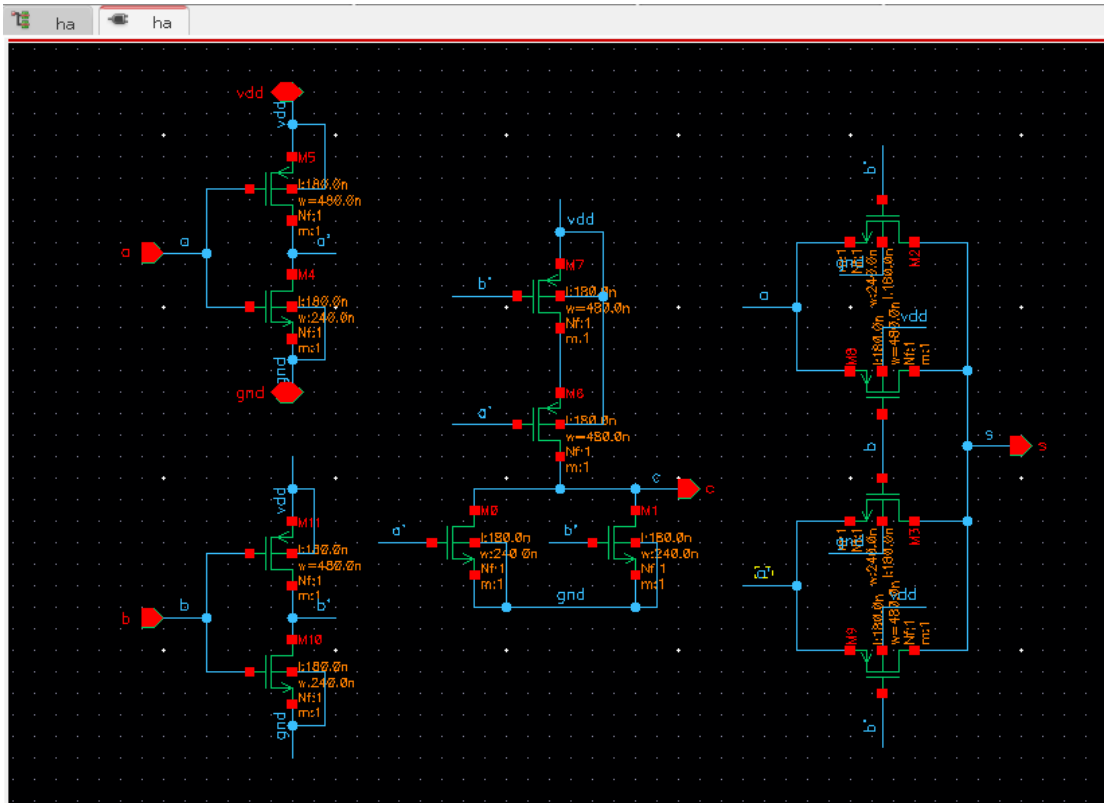
(20171049)

A 2 bit adder can be designed by using one half adder and one full adder. So we will have to first design a half adder (adds 2 bits) and a full adder (adds 3 bits).

Design of Half adder:

I have designed the half adder schematic using the minimum number of transistors, i.e. 6NMOS and 6 PMOS, which is as shown in figure below:

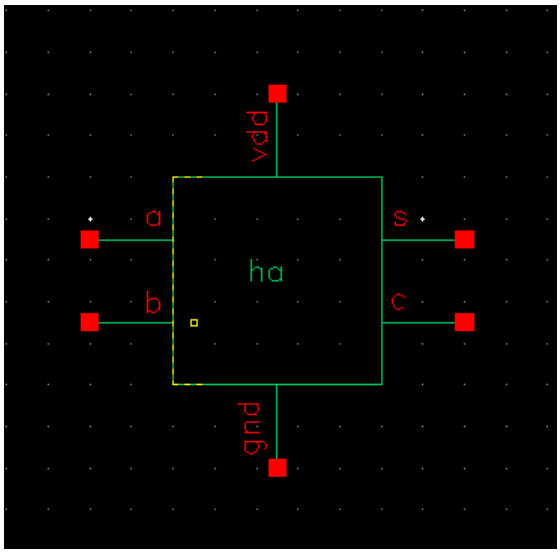


Schematic of Half adder

In the schematic of a half adder, we are adding 2 bits – a and b. I have used 2 inverters for generating a' and b'. To generate the carry, which is equal to c=a.b can be implemented as c=(a'+b')', which is shown above.

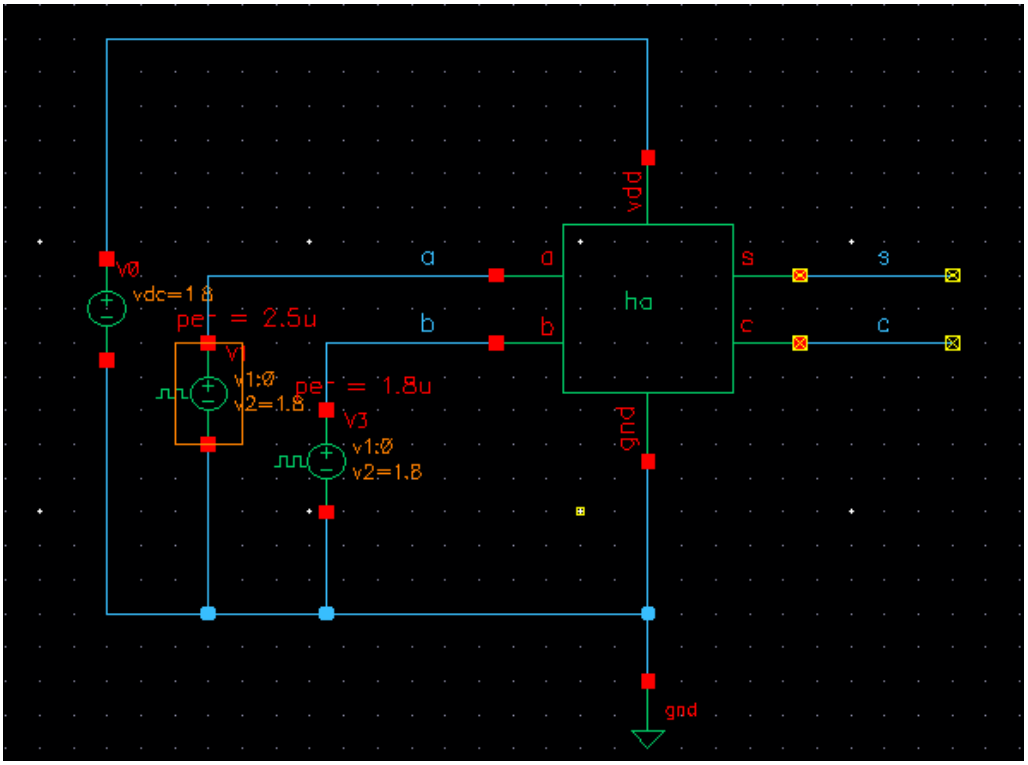
To generate the sum we implement sum=a.b'+a'.b using a xor gate by ptl logic.

Instead of applying power sources, I have attached pins in the schematic to create a symbol for it and then using it to test the working of the half adder. So the symbol is created and shown below:



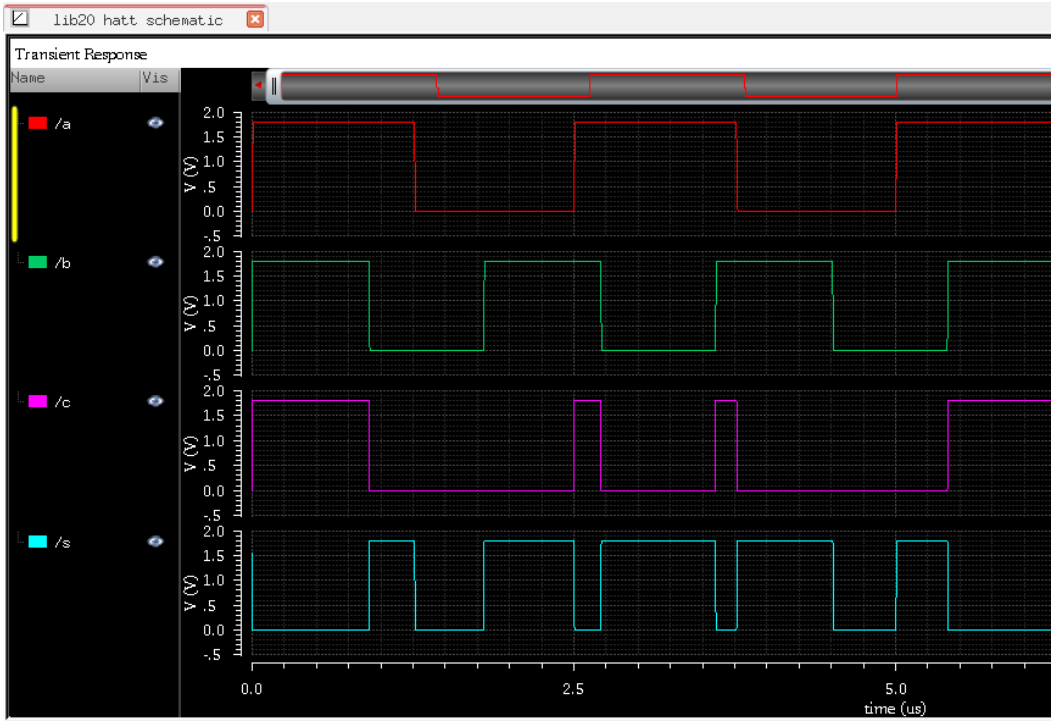
Symbol of a half adder

Now, we have to test our symbol, so we add it in a new schematic, apply power sources and make the connections properly.



Circuit Diagram of a half adder with symbol to test the working

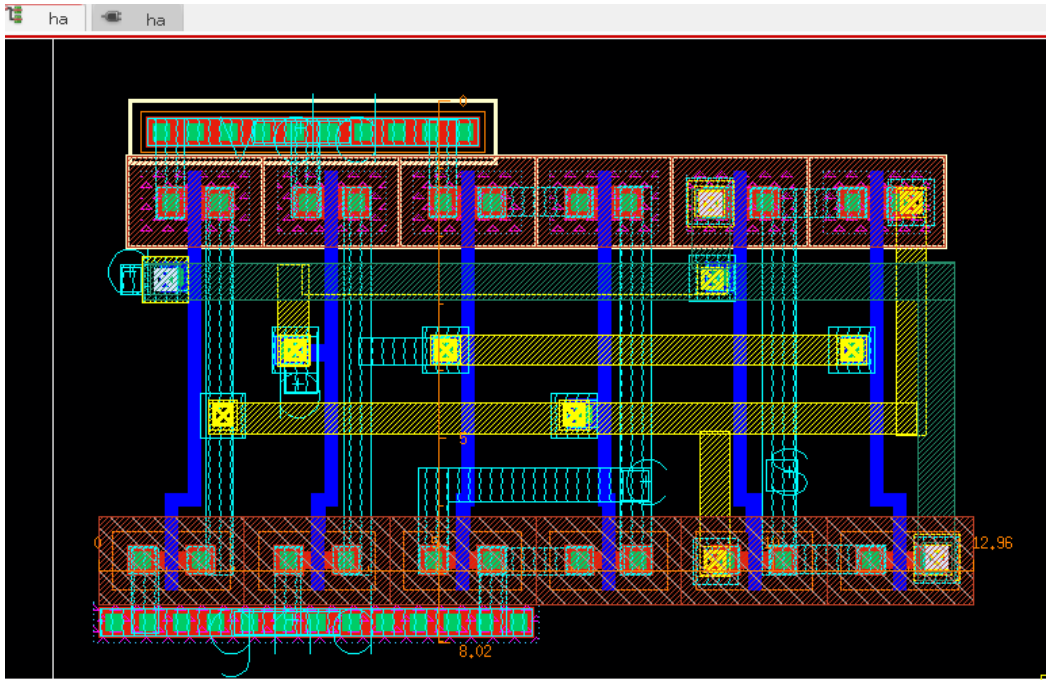
The results obtained from the half adder symbol are shown below, and it is verified that our half adder is working properly.



Inputs – a (red) & b (green). Outputs – c (purple) & s (blue)

From the above graph, we can clearly see that only when a and b are high, carry bit, c is high and also that, when either of a and b is high but not both, sum bit, s is high. So we can say that our half adder is working properly.

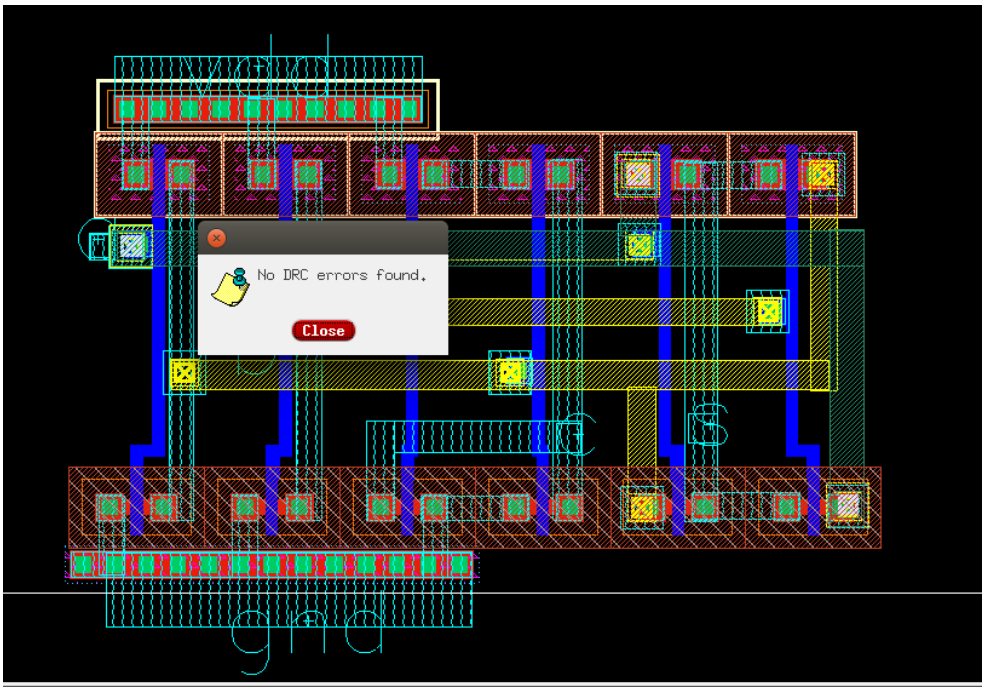
Now we will make the layout for our half adder, and draw it in accordance with the lambda rules. The layout formed is shown below:



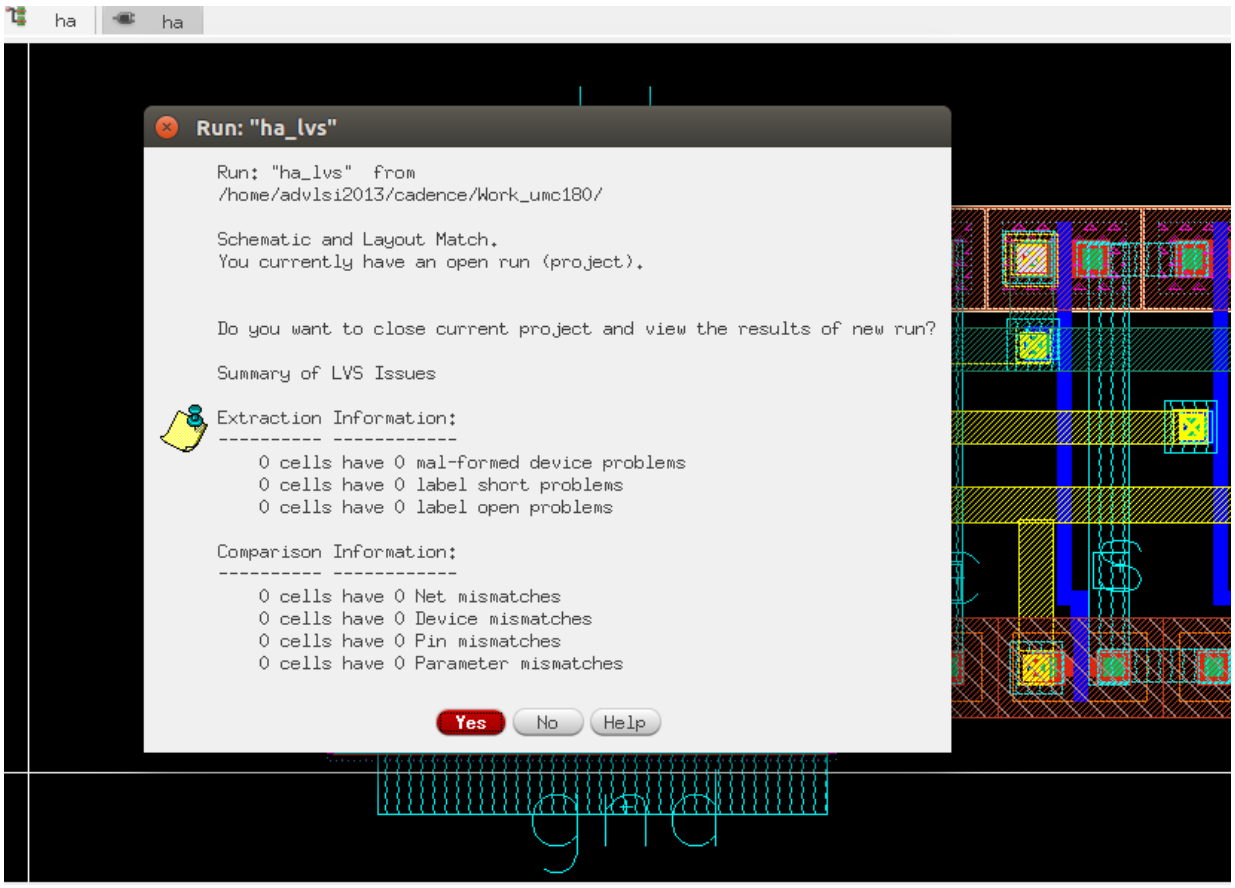
Layout of Half adder

Area of half adder : 12.96um x 8.02um = 103.94um^2.

The results of the DRC test and LVS test were successful for the layout formed, i.e., there were no errors in the layout and also it is now matched with the schematic which we had drawn earlier.

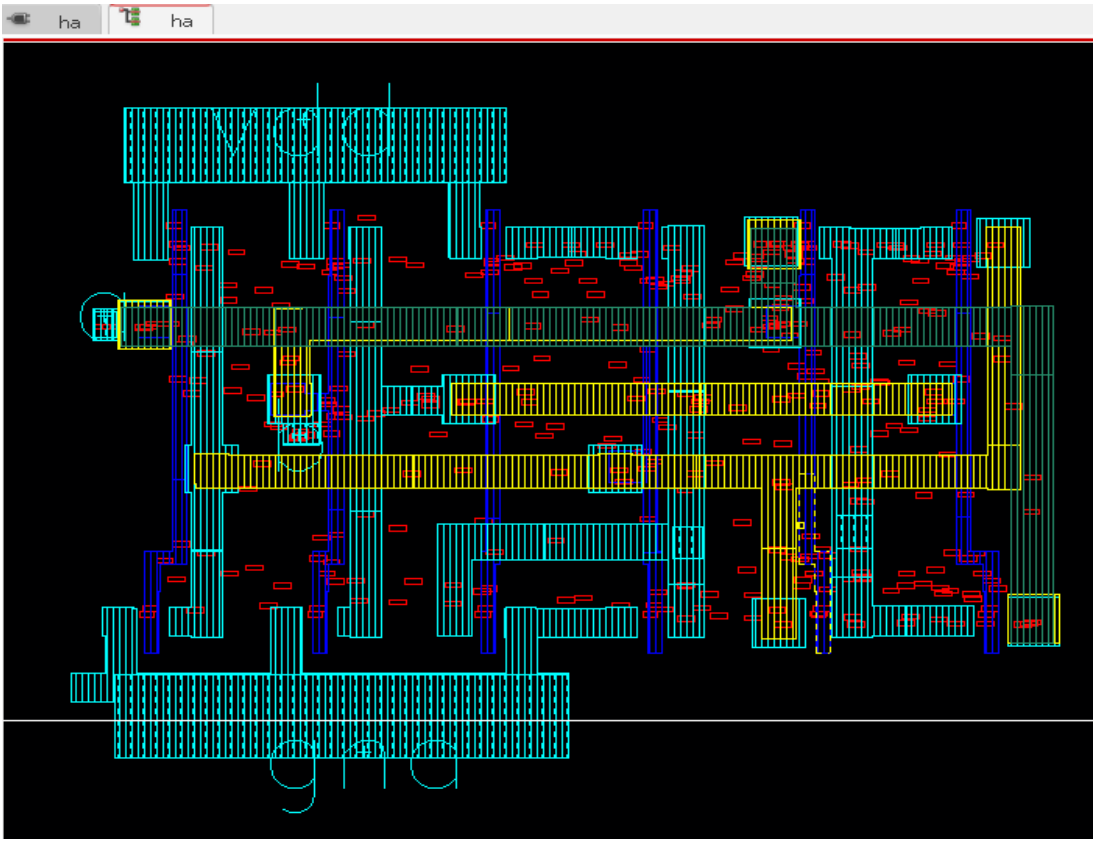


Result of DRC test (successful)



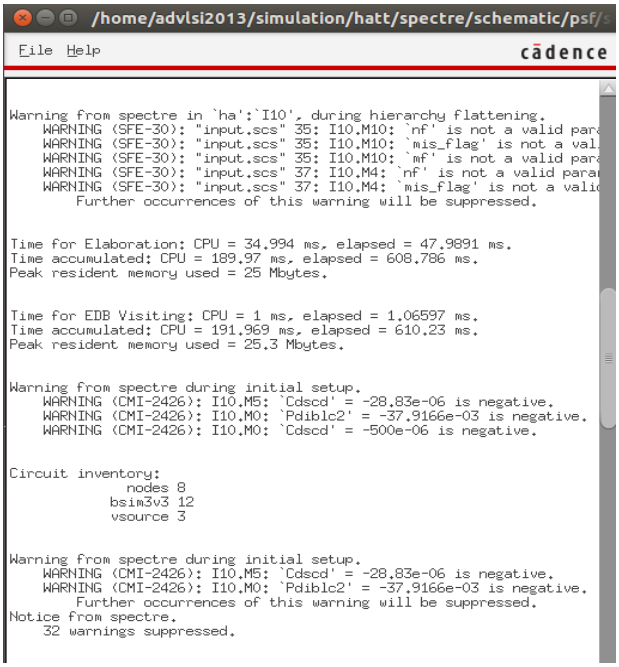
Result of LVS test (successful)

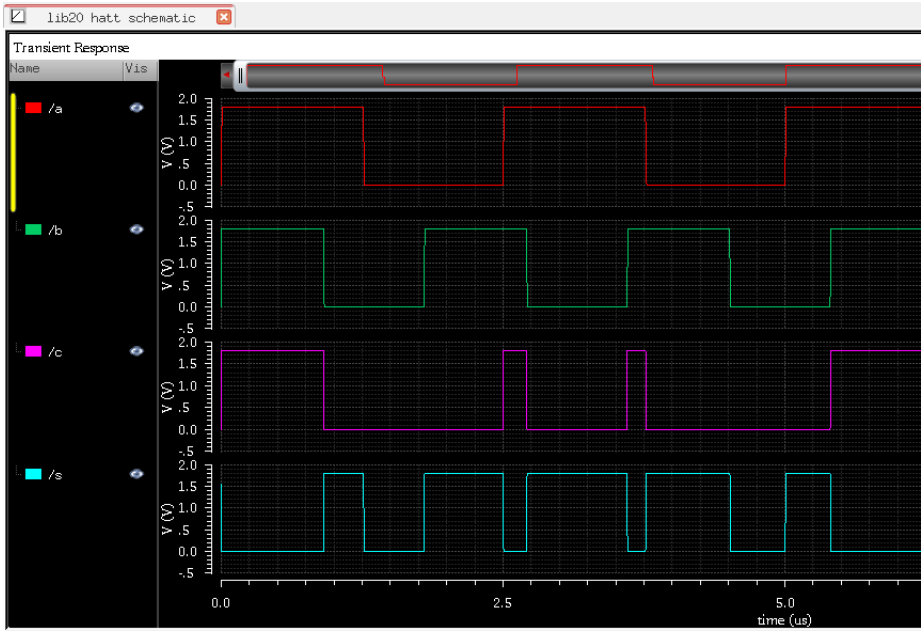
Now, the post layout simulation is done and so the RCX test is run to generate the extracted view of the layout, which shows the presence of various parasitic capacitances and resistances and it is shown below:



Extracted view of the layout with parasitic capacitances and resistances

Now, transient analysis is done and results are as shown below:



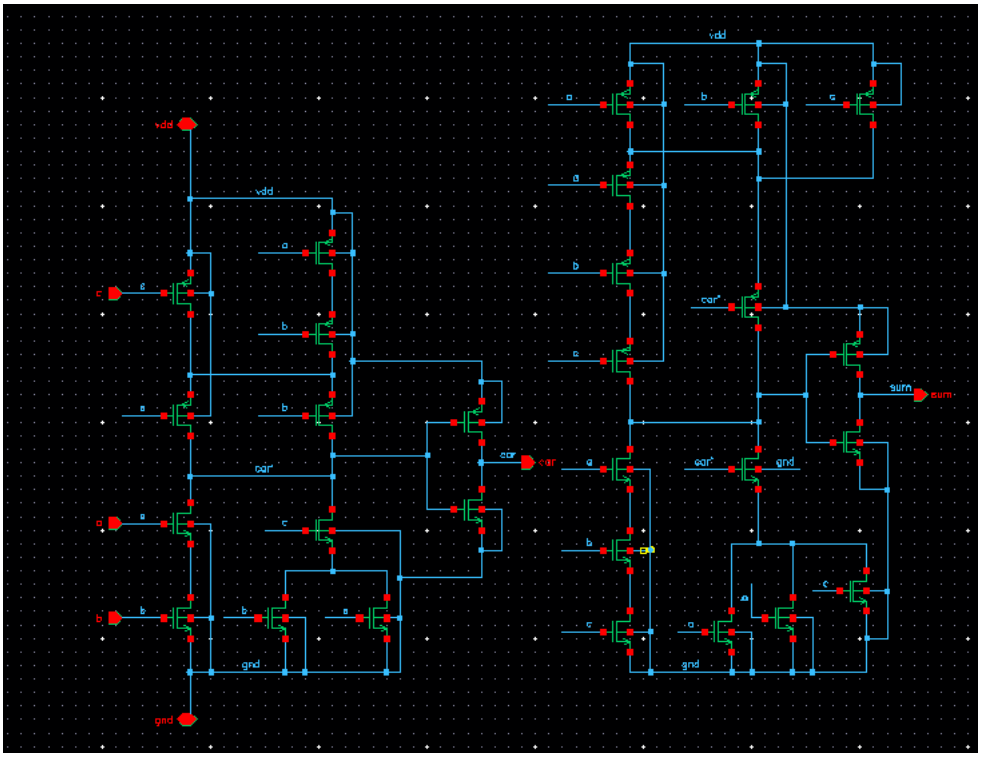


Inputs – a (red) & b (green). Output – c (purple) & s(blue)

So, the layout and the schematic are successfully verified theoretically also and we have also minimized the number of transistors, minimized the area of the layout and the power consumption. Thus our half adder design is successfully completed.

Design of Full adder:

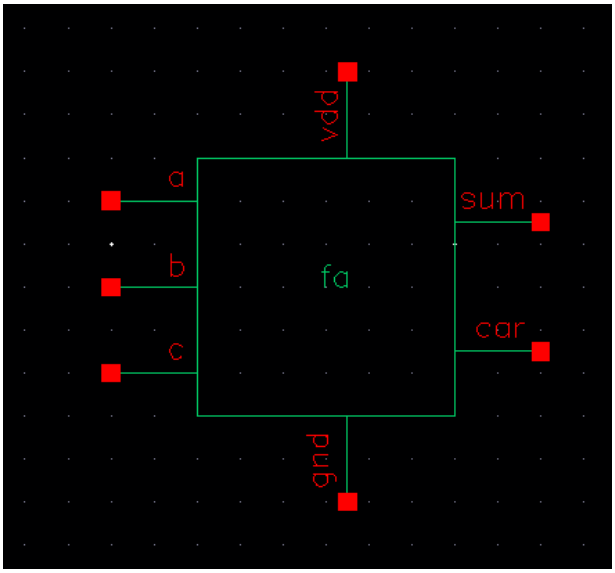
I have designed the full adder schematic, using the minimum number of transistors, i.e. 14NMOS and 14 PMOS, which is as shown in figure below:



Schematic of Full adder

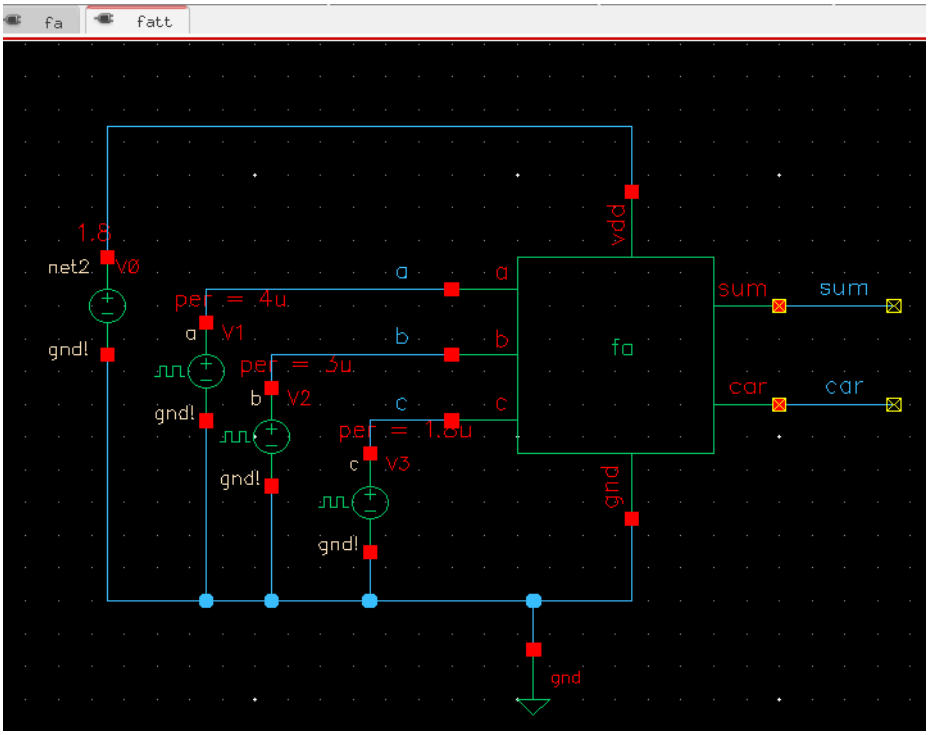
In the schematic of a full adder, we are adding 3 bits – a, b and c. To generate the carry, which is equal to carry=a.b+c.(a+b) and implemented as shown above. To generate the sum we implement sum=(a.b.c)+(carry').(a+b+c).

Instead of applying power sources, I have attached pins in the schematic to create a symbol for it and then using it to test the working of the full adder. So the symbol is created and shown below:



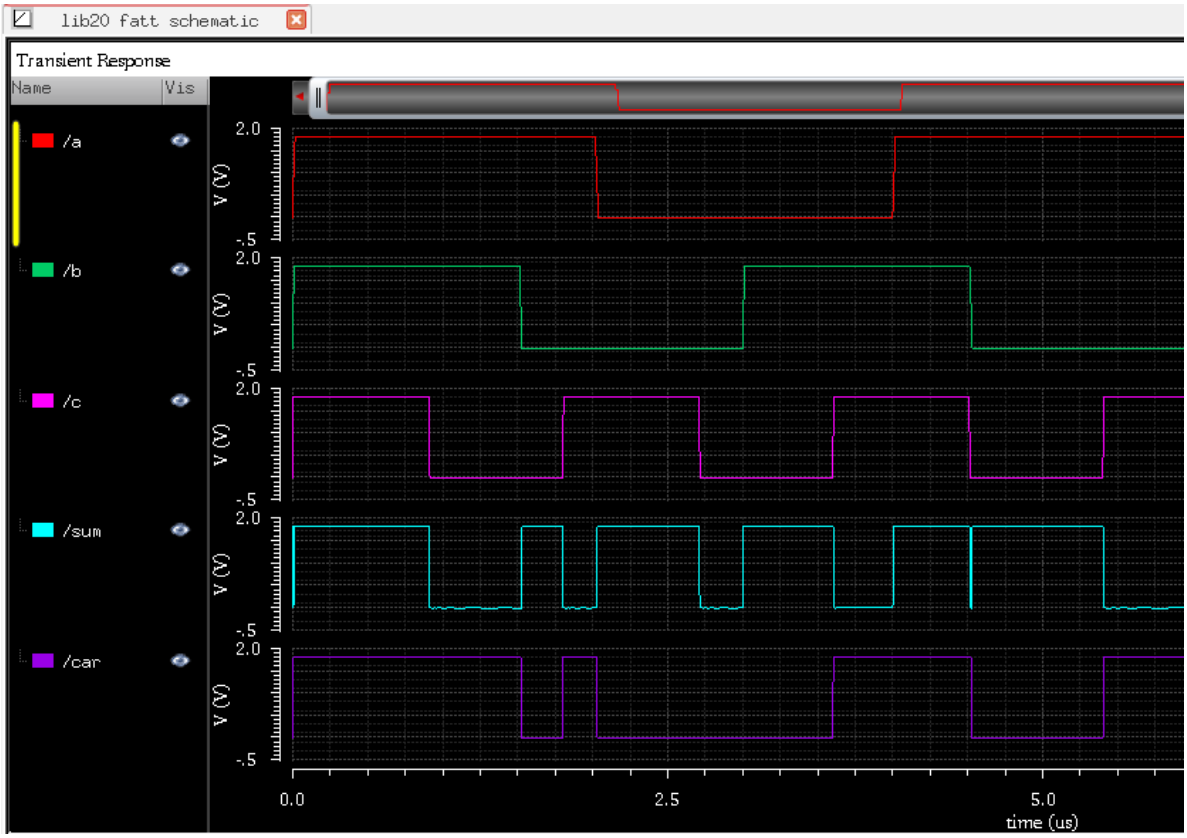
Symbol of a full adder

Now, we have to test our symbol, so we add it in a new schematic, apply power sources and make the connections properly.



Circuit Diagram of a full adder with symbol to test the working

The results obtained from the full adder symbol are shown below, and it is verified that our full adder is working properly.



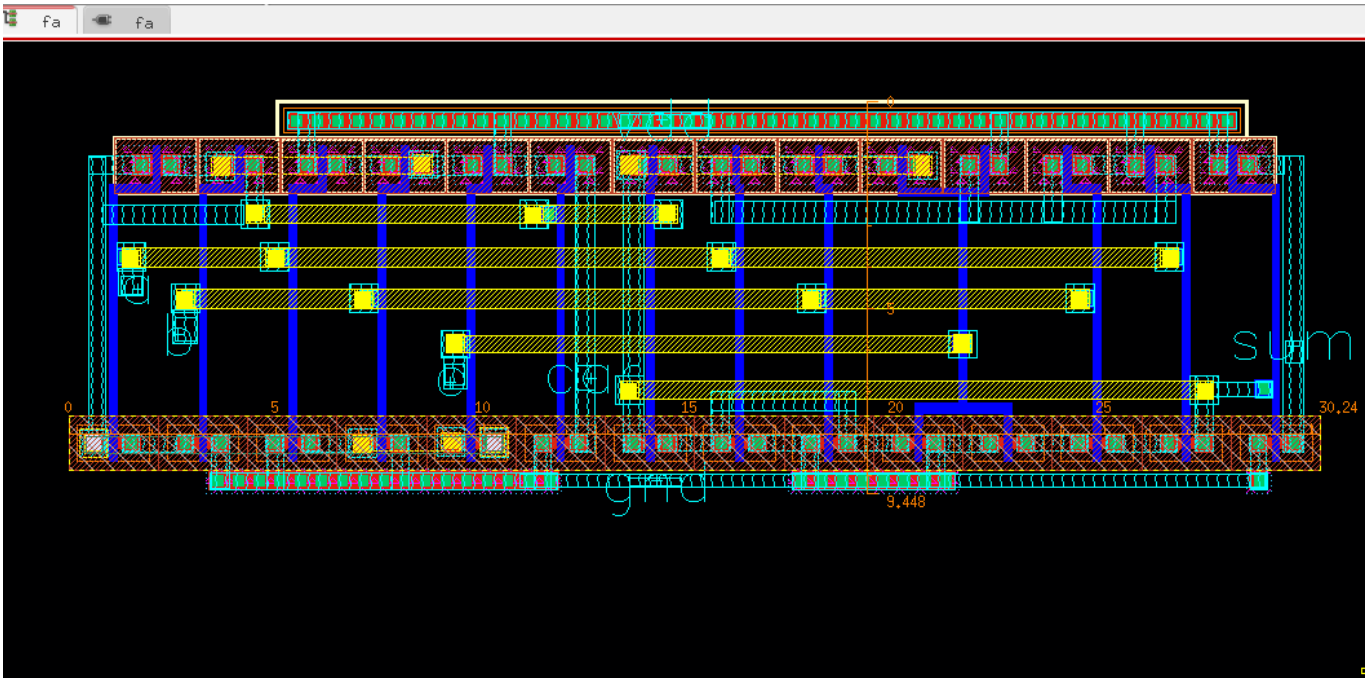
Inputs – a (red), b (green) & c(pink). Outputs – car (purple) & sum (blue)

From the above graph, we can clearly see that our full adder is working properly.

Now we will make the layout for our full adder, and try to minimize the are in accordance with the lambda rules.

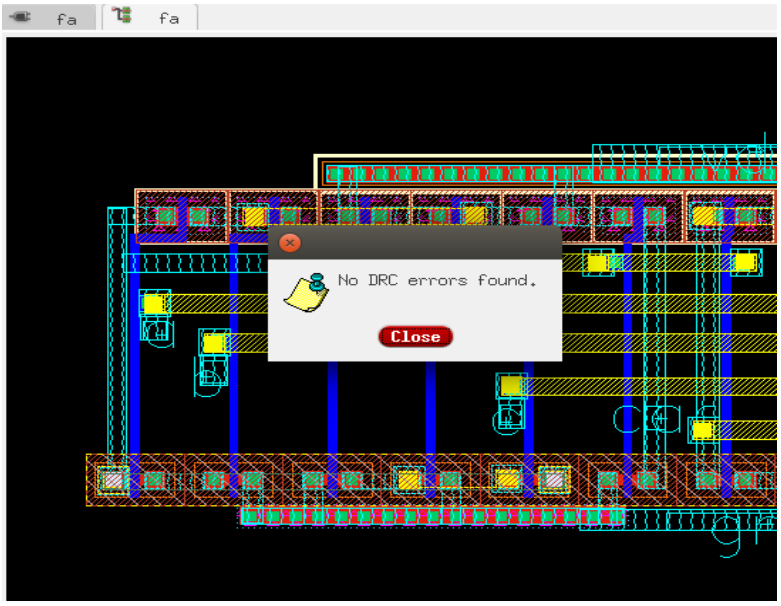
The layout with the minimized area drawn has an area of around 30.24um x 9.448um = 285.7um^2, which is equal to 79363λ^2.

The layout drawn is shown in the below figure:

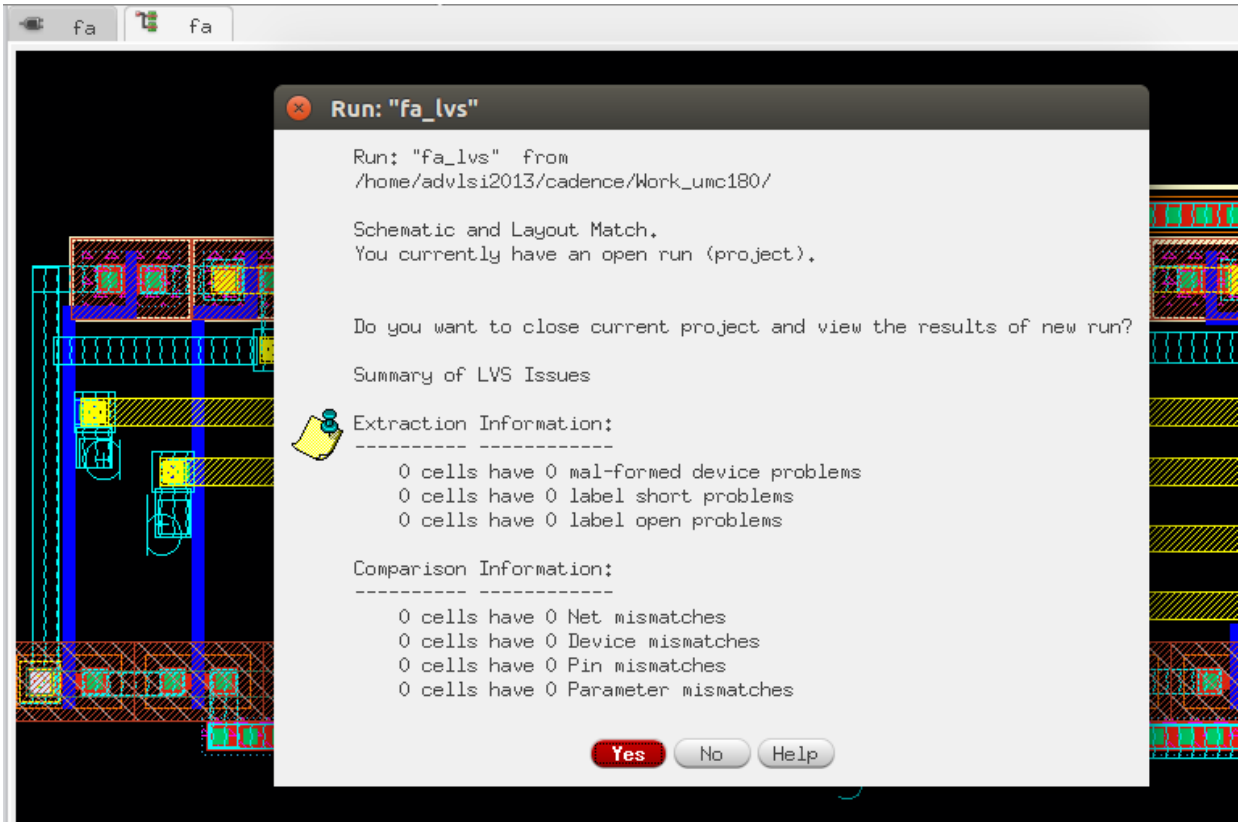


Layout of Full adder

The results of the DRC test and LVS test were successful for the layout formed, i.e., there were no errors in the layout and also it is now matched with the schematic which we had drawn earlier.

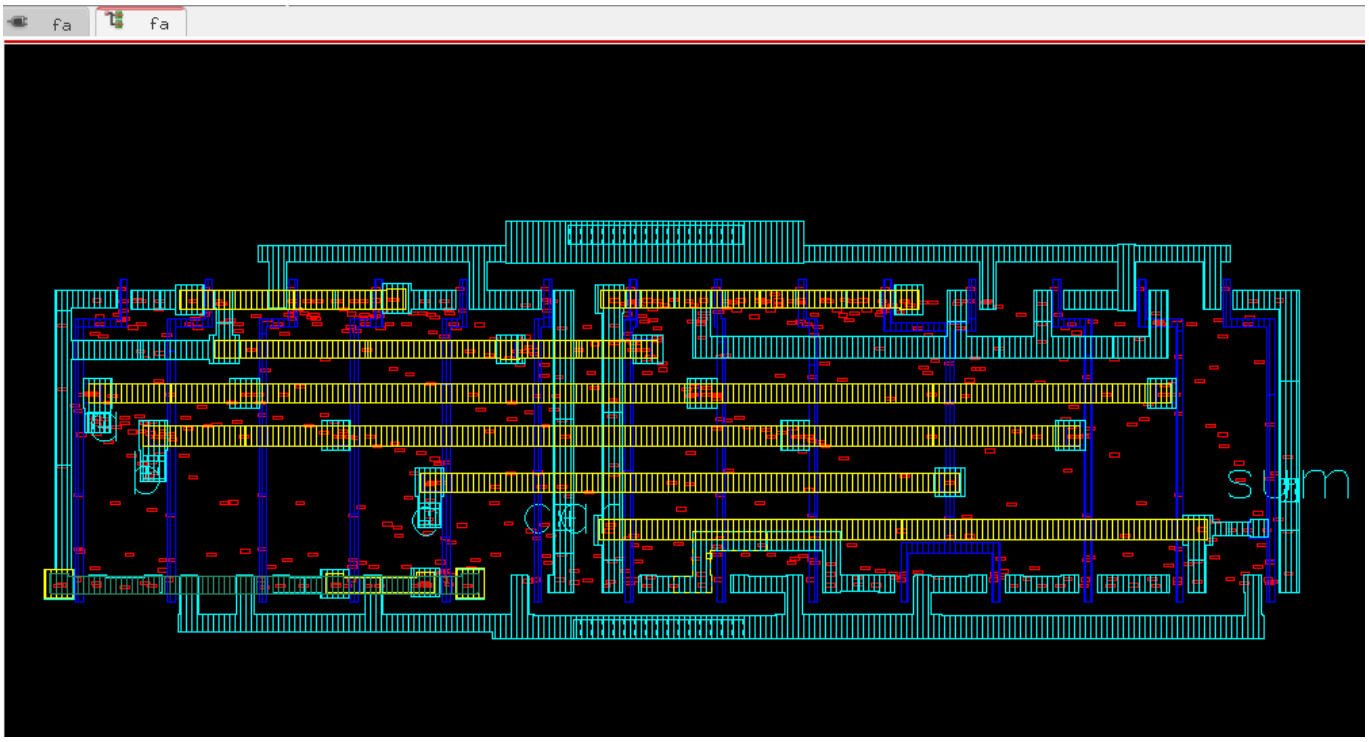


Result of DRC test (successful)



Result of LVS test (successful)

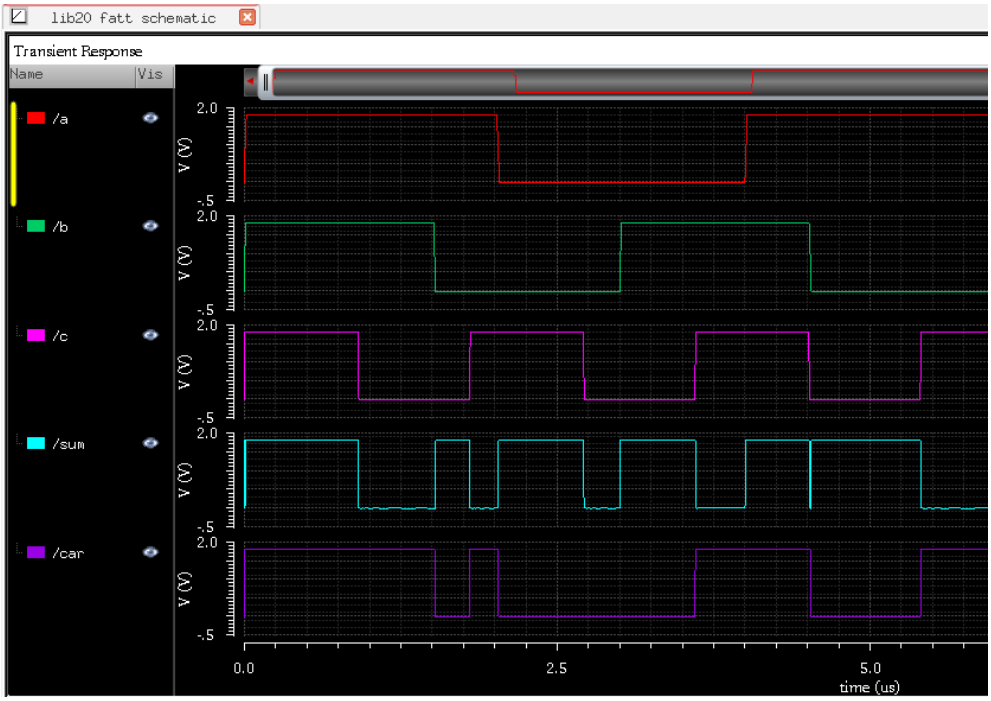
Now, the RCX test is run to generate the extracted view of the layout, which shows the presence of various parasitic capacitances and resistances and it is shown below:



Extracted view of the layout with parasitic capacitances and resistances

When this extracted view is zoomed, we can clearly see in the above figure, the parasitic capacitances and parasitic resistances in metals and poly.

Now, transient analysis is done and results and the outputs are as shown:



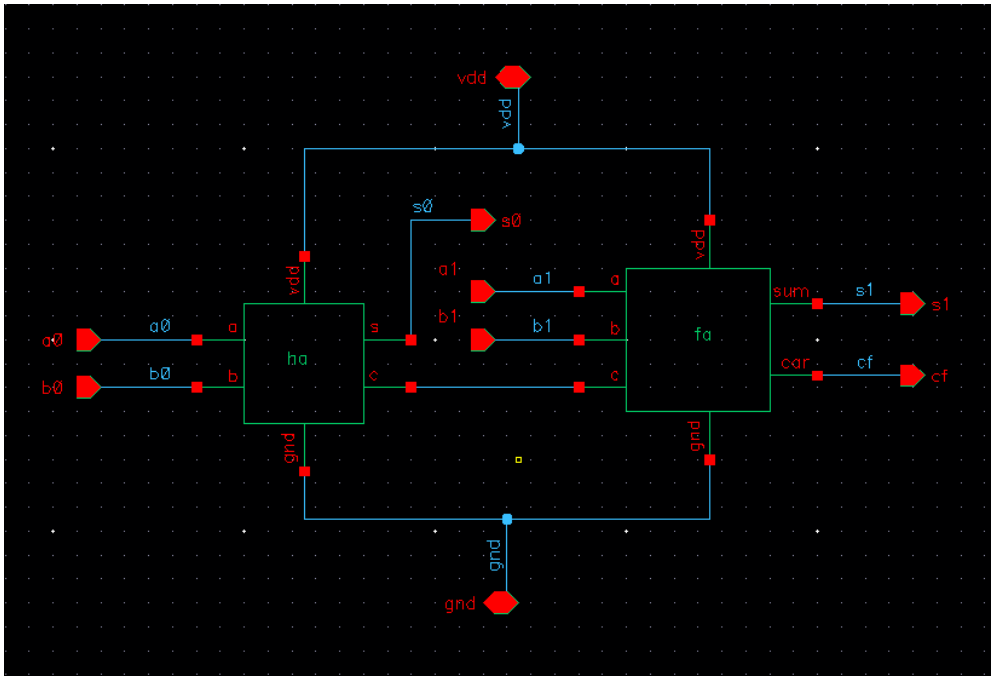
Inputs – a (red), b (green) & c(pink). Output – car (purple) & sum(blue)

So, the comparison between the results of the layout and the schematic of the half adder are approximately same. There are very little distortions in the output waveforms of the layout which is not in the case of schematic. So, the layout and the schematic are successfully verified theoretically also. Thus our full adder design is successfully completed.

Design of a 2 bit adder:

I have designed the 2 bit adder schematic using the symbols made by us for the half adder and full adder, which is as shown in figure below.
It uses the minimum number of transistors and then we have also minimized the area of layout made by us as much as possible. Also the power consumption is minimized.

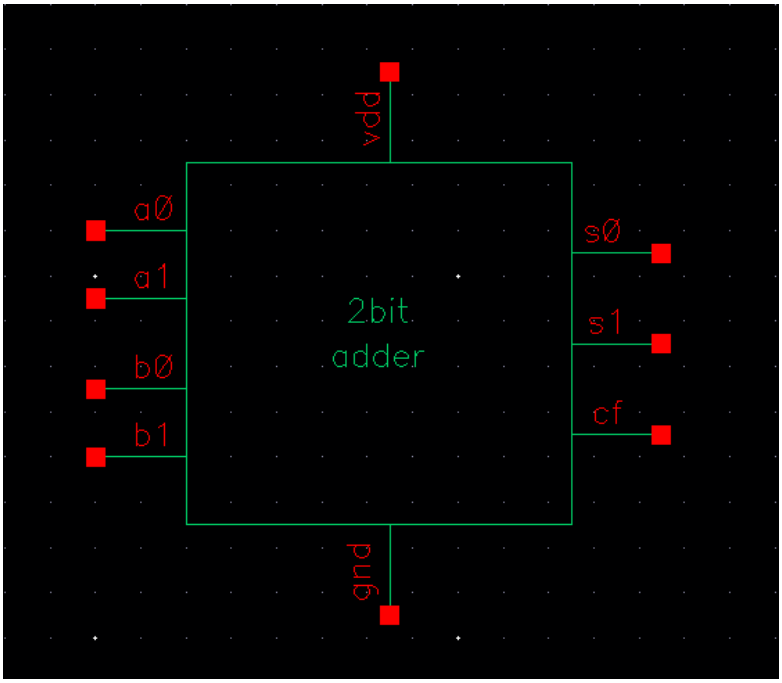
The following is the schematic of the 2 bit adder:



Schematic of 2 bit adder

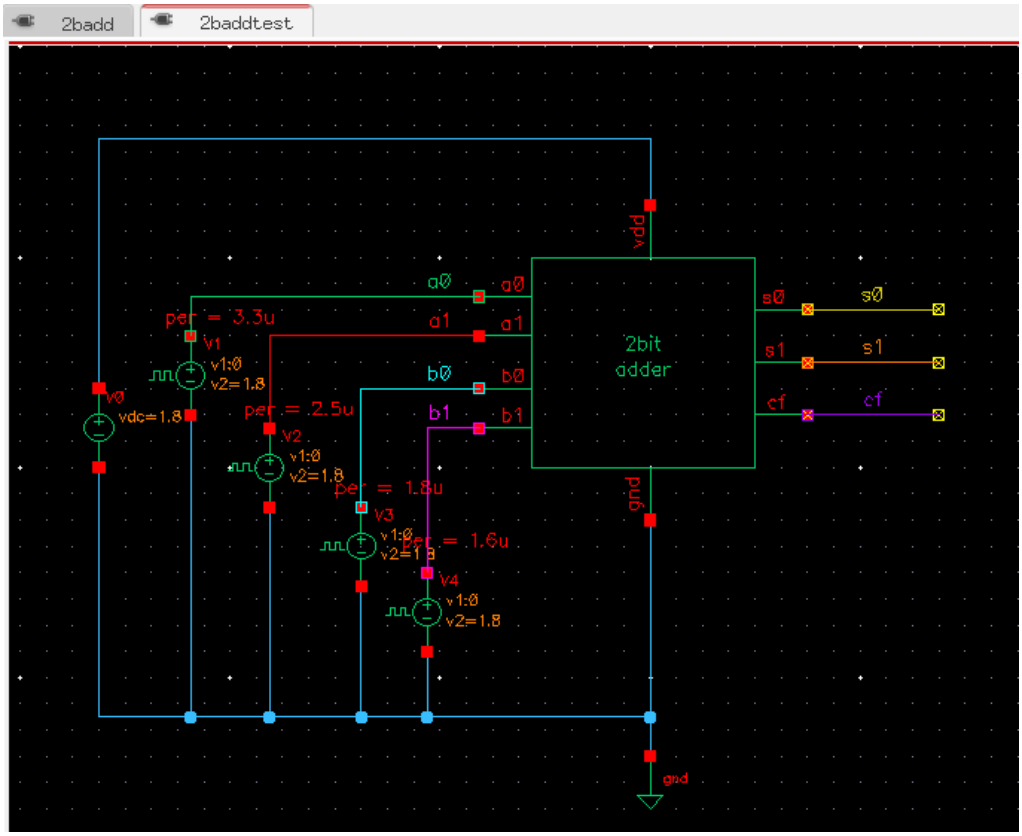
In the schematic of a 2 bit adder, we are adding two 2 bit numbers, i.e., a1 a0 and b1 b0, and the sum is obtained as s1 s0 and the final carry generated is cf.

Instead of applying power sources, I have attached pins in the schematic to create a symbol for it and then using it to test the working of the 2 bit adder. So the symbol is created and shown below:



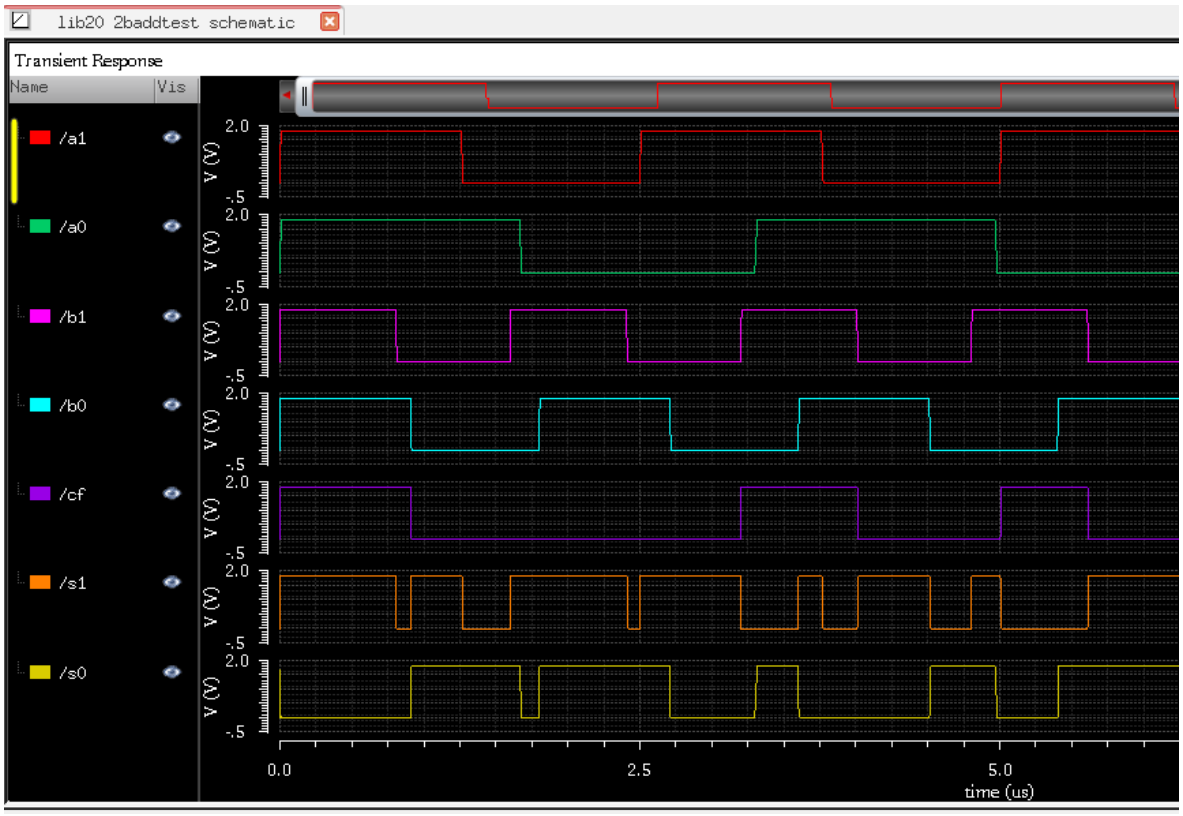
Symbol of a 2 bit adder

Now, we have to test our symbol, so we add it in a new schematic, apply power sources and make the connections properly.



Circuit Diagram of a 2 bit adder with symbol to test the working

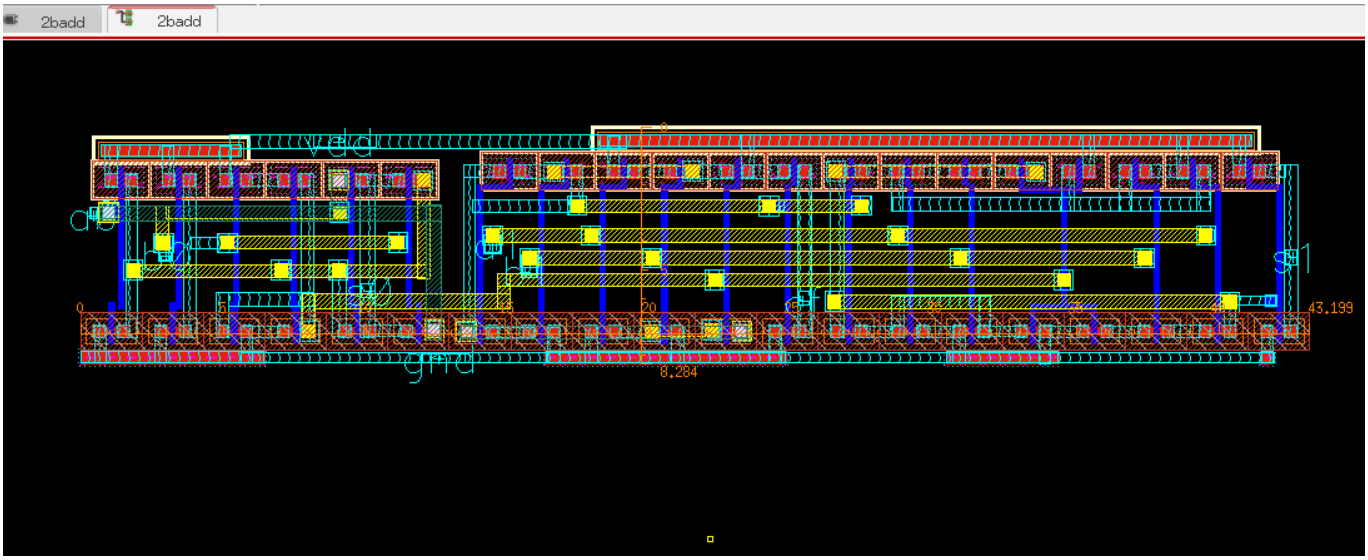
The results obtained from the 2 bit adder symbol are shown below, and it is verified that our 2 bit adder is working properly.



Inputs – a1(red), a0(green), b1pink) & b0(blue). Outputs – cf(purple), s1(orange) & s0(yellow)

From the above graph, we can clearly see that our 2 bit adder is working properly.

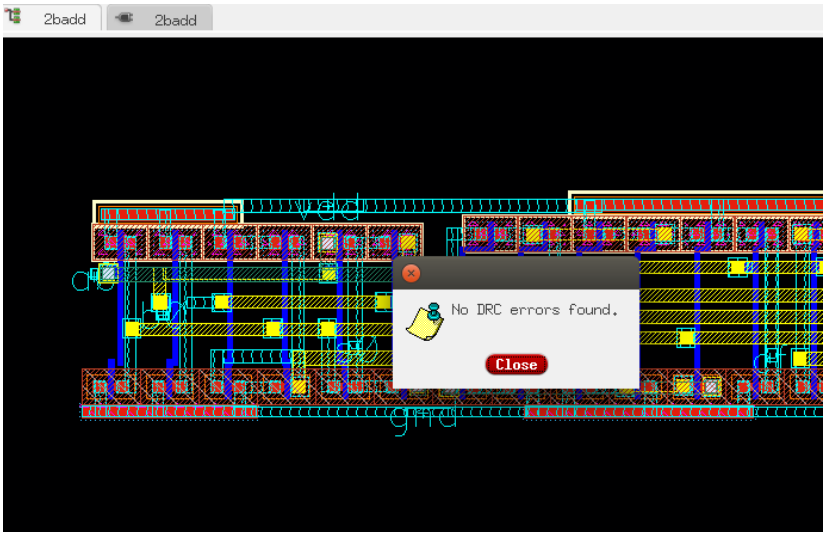
Now we will make the layout for our 2 bit adder, and draw it in accordance with the lambda rules. The layout formed is shown below:



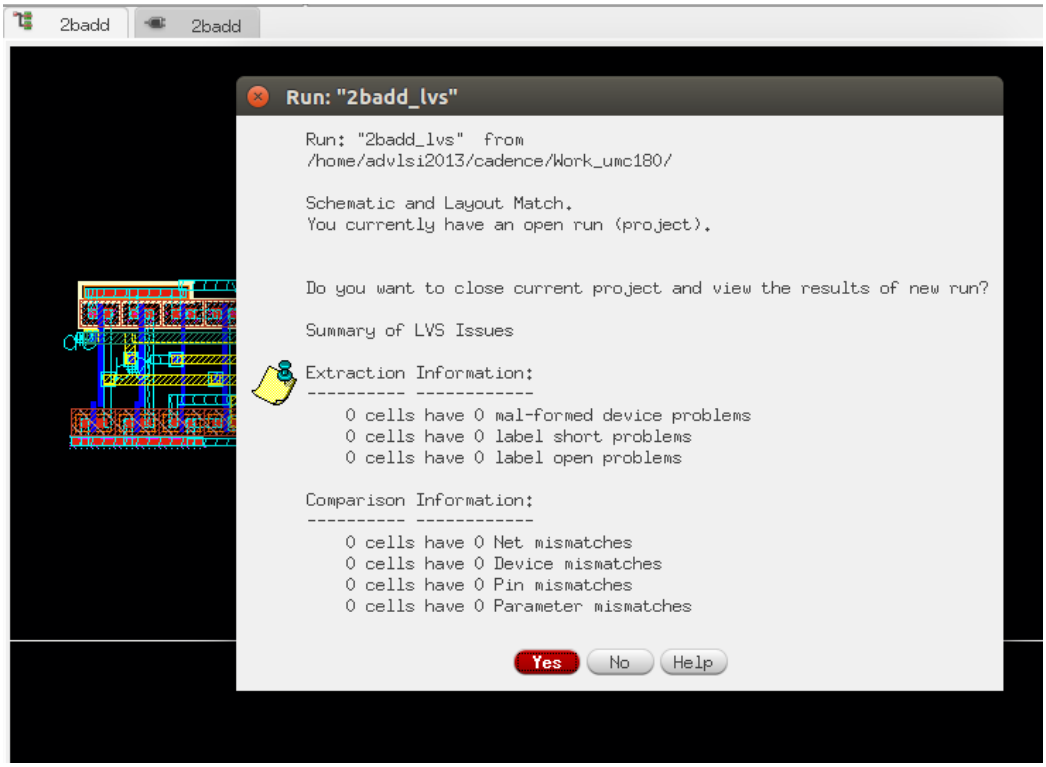
Layout of 2 bit adder

The area is minimized and is equal to 43.199um x 8.284um = 357.86um^2, which is also equal to 99405λ^2. (λ=0.06um and it can be verified in cadence).

The results of the DRC test and LVS test were successful for the layout formed, i.e., there were no errors in the layout and also it is now matched with the schematic which we had drawn earlier.

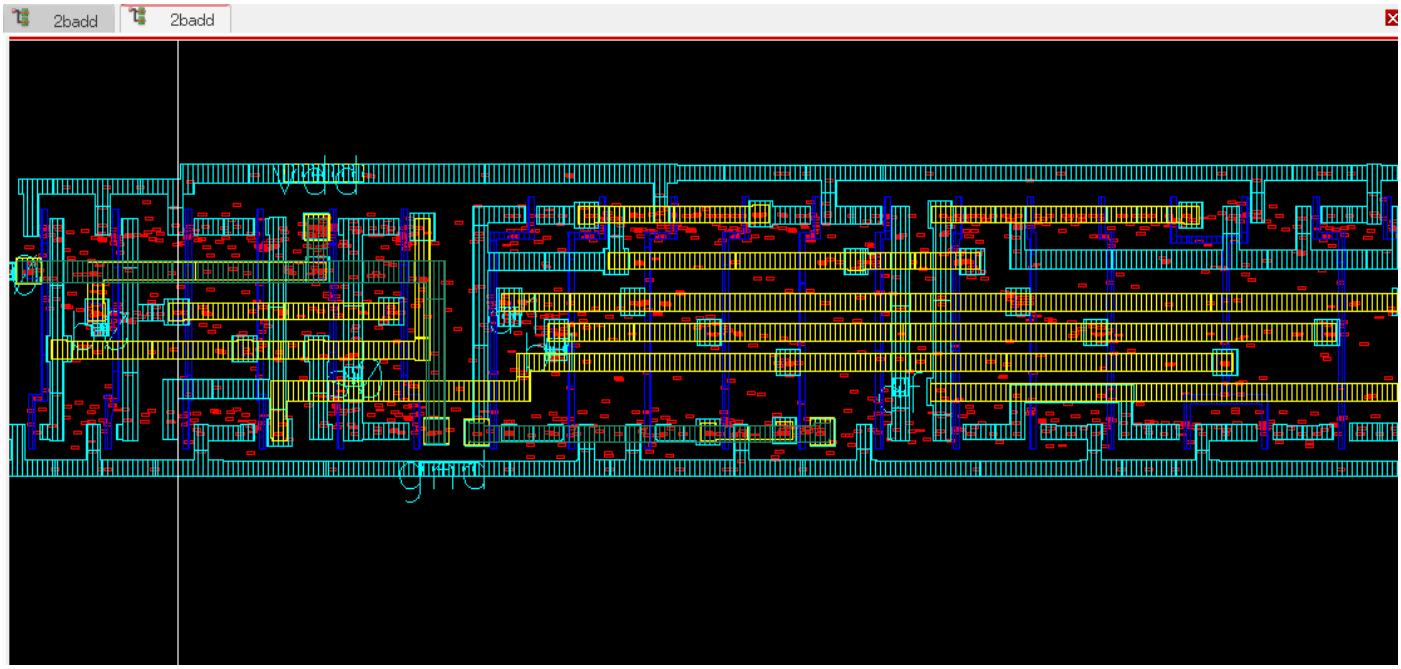


Result of DRC test (successful)

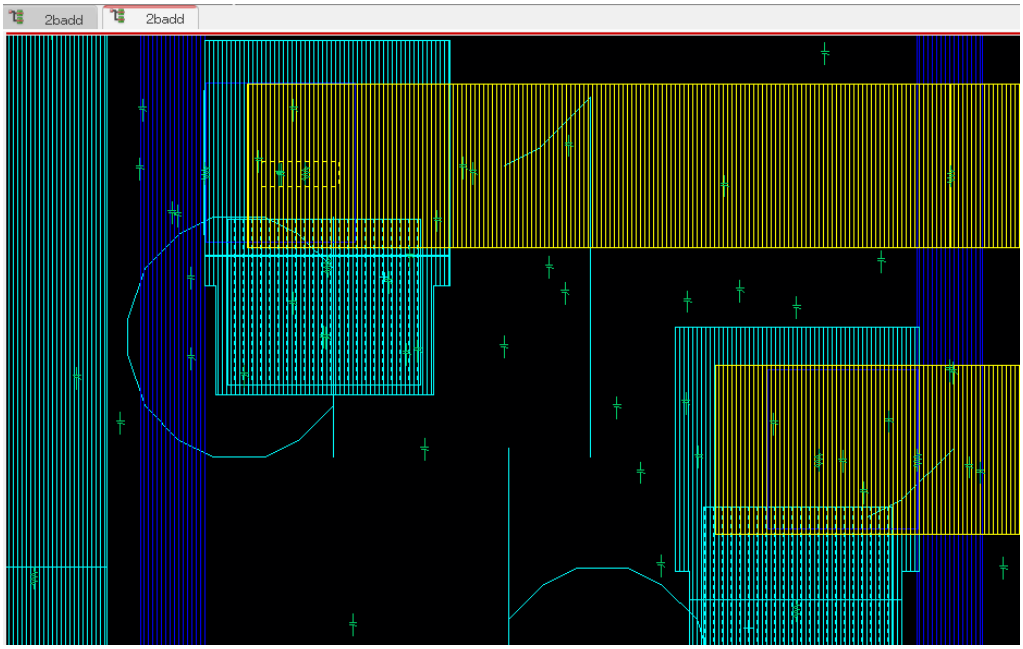


Result of LVS test (successful)

Now, the RCX test is run to generate the extracted view of the layout, which shows the presence of various parasitic capacitances and resistances and it is shown below:

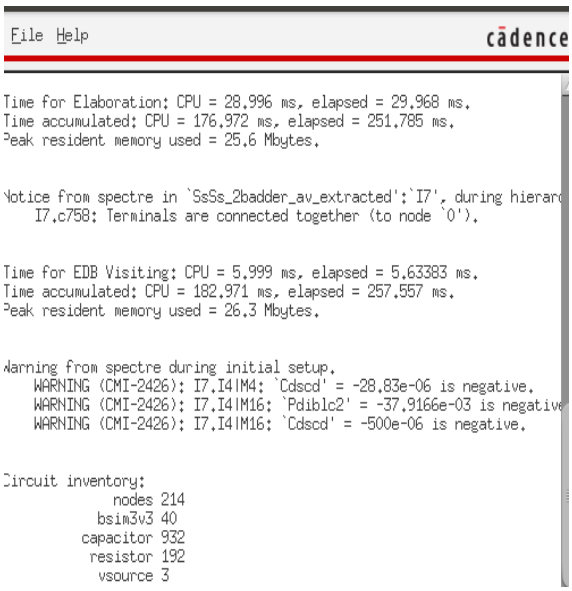


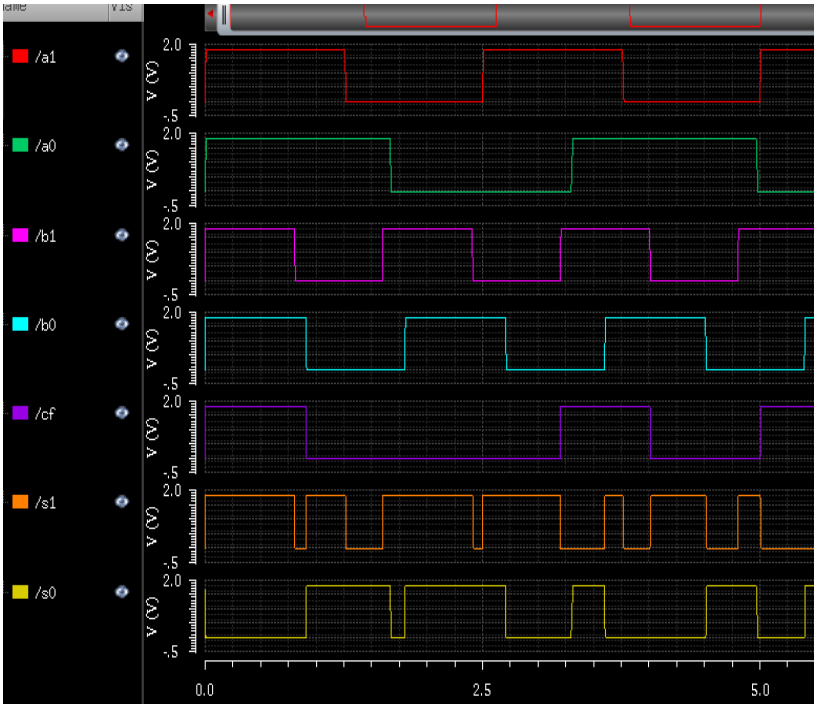
Extracted view of the layout with parasitic capacitances and resistances



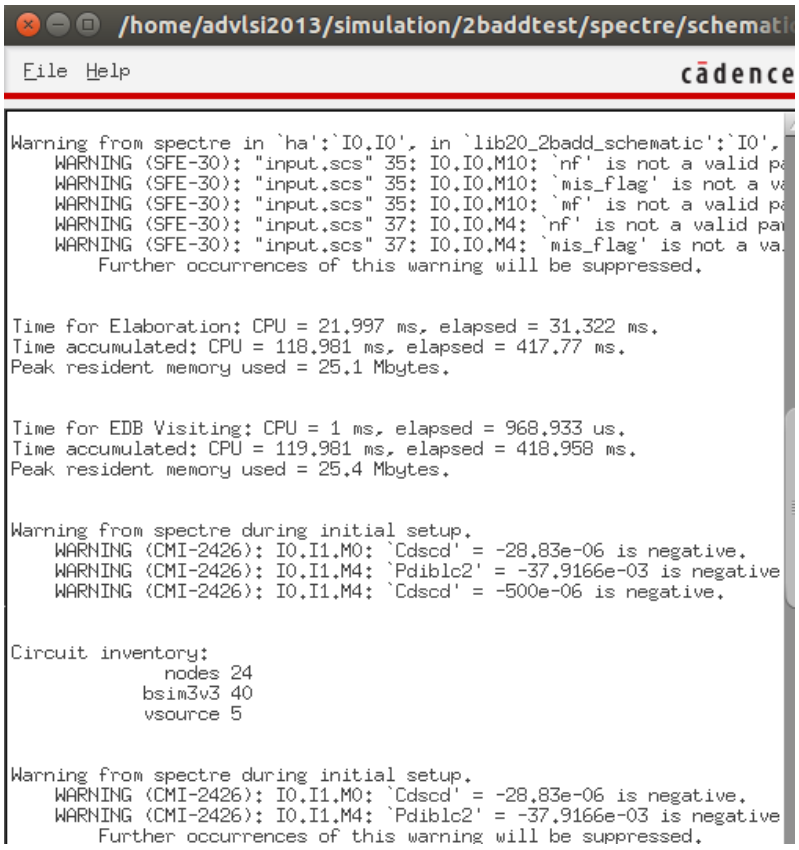
When this extracted view is zoomed, we can clearly see in the above figure, the parasitic capacitances and parasitic resistances in metals and poly.

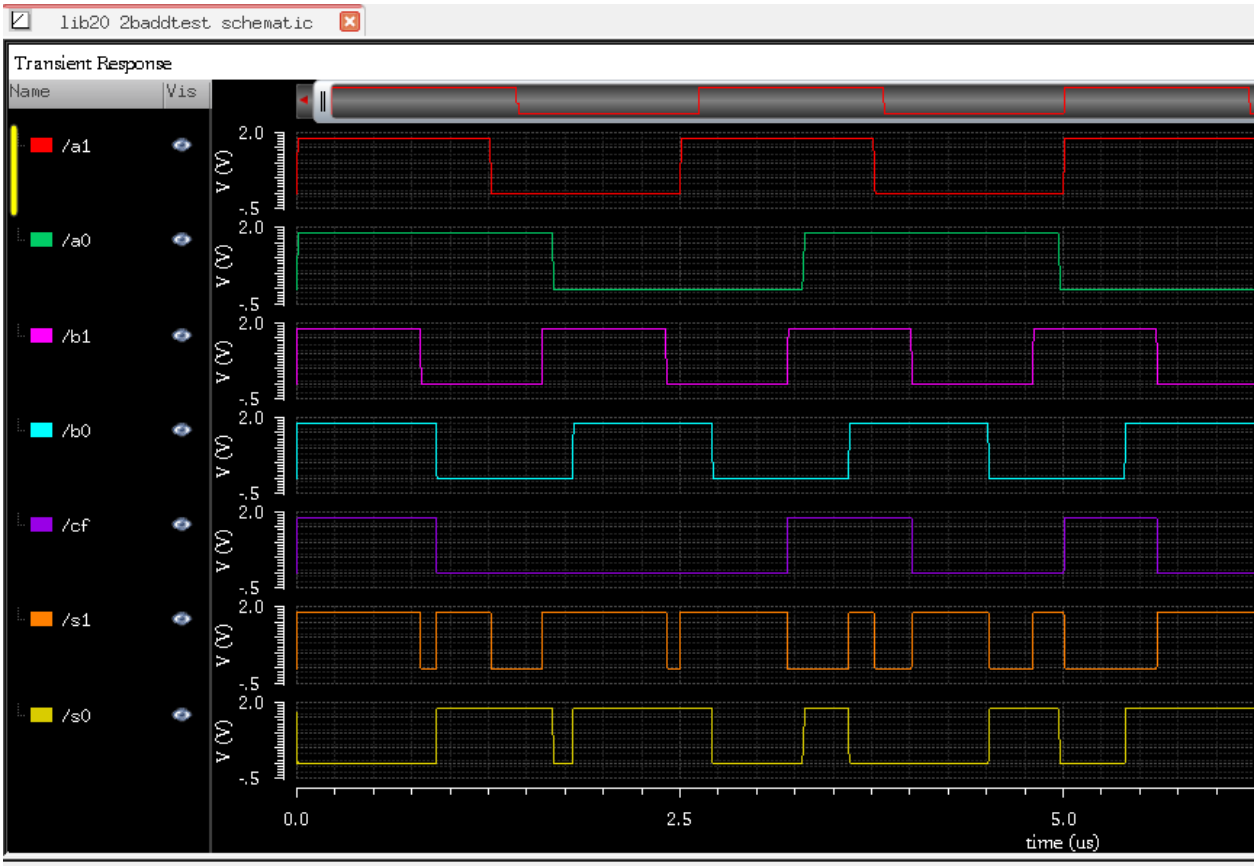
We can now ensure that our layout drawn also gives correct results. So, changing the hierarchy of our symbol from schematic to layout, the following results were obtained and we can see that the output is coming correctly from the transient analysis of the circuit. Also we can see the presence of multiple resistances, capacitances, and nodes in the results, which were not in the schematic.





Now, we compare the results of the original schematic with that of the results from layout hierarchy. Again transient analysis is done and results are as shown:





Inputs – a1(red), a0(green), b1pink) & b0(blue). Outputs – cf(purple), s1(orange) & s0(yellow)

So, the comparison between the results of the layout and the schematic of the half adder are approximately same. There are very little distortions in the output waveforms of the layout which is not in the case of schematic. So, the layout and the schematic are successfully verified theoretically also. Thus our 2 bit adder design is successfully completed and the following conclusions are made.

No. of transistors used: 40 (20NMOS + 20PMOS).
Area consumed by layout: 357.86um^2.
Power consumption: 190.2uW. (calculated by doing DC analysis).
Longest delay path: Longest delay path is to compute the final carry ‘cf’.