Intro to VLSI

Final Project

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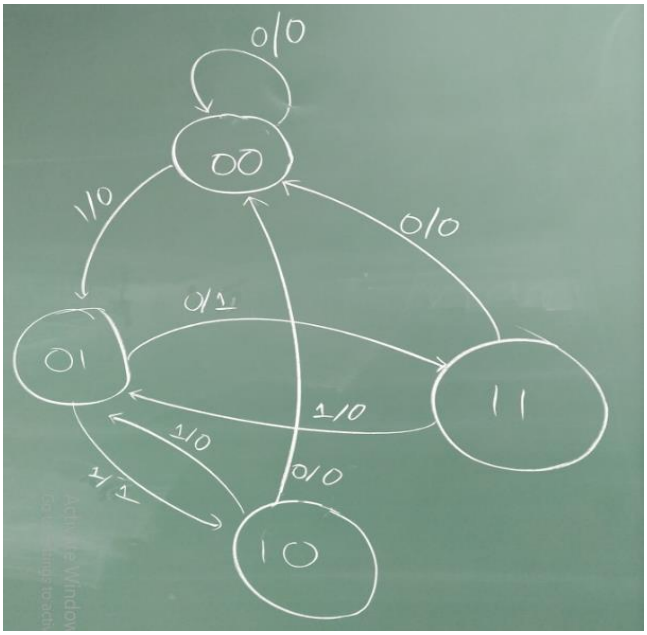
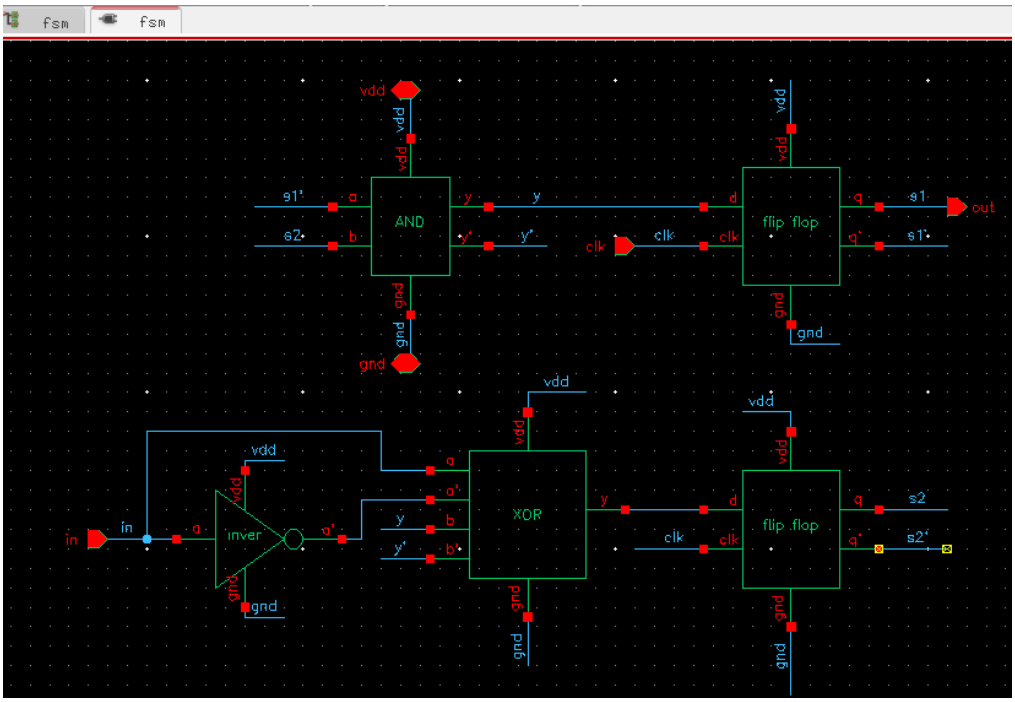
The vending machine can be implemented by using FSM (finite state machine). As the given vending machine has 4 states, we make use of 2 FSM's, as the 4 states can be implemented by using 2 bits and then using 1 FSM for each bit.

The following are the states (s1 s2) used:
00: standby mode
01: money received
10: coffee dispensed
11: tea dispensed
And the output generated is as follows:
1: beverage dispensed
0: beverage not dispensed.
The following is the state diagram of our vending machine (FSM):



We have designed the following vending machine as required with the use of minimum possible number of transistors and minimizing the area and power consumption.

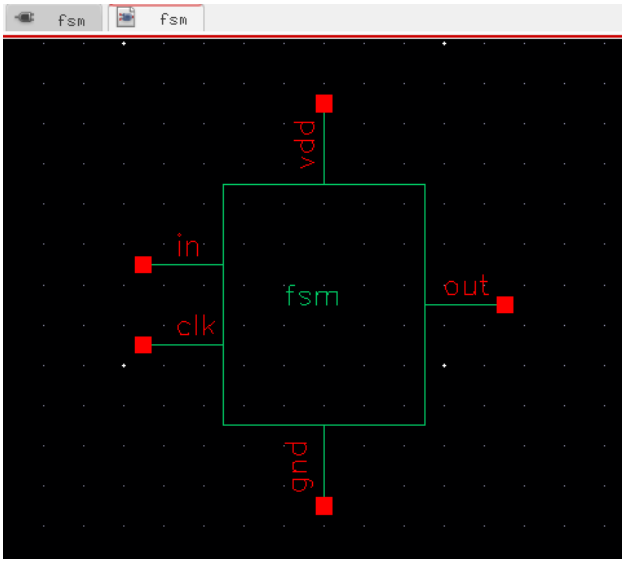
The schematic of the FSM is shown below:



Schematic of FSM

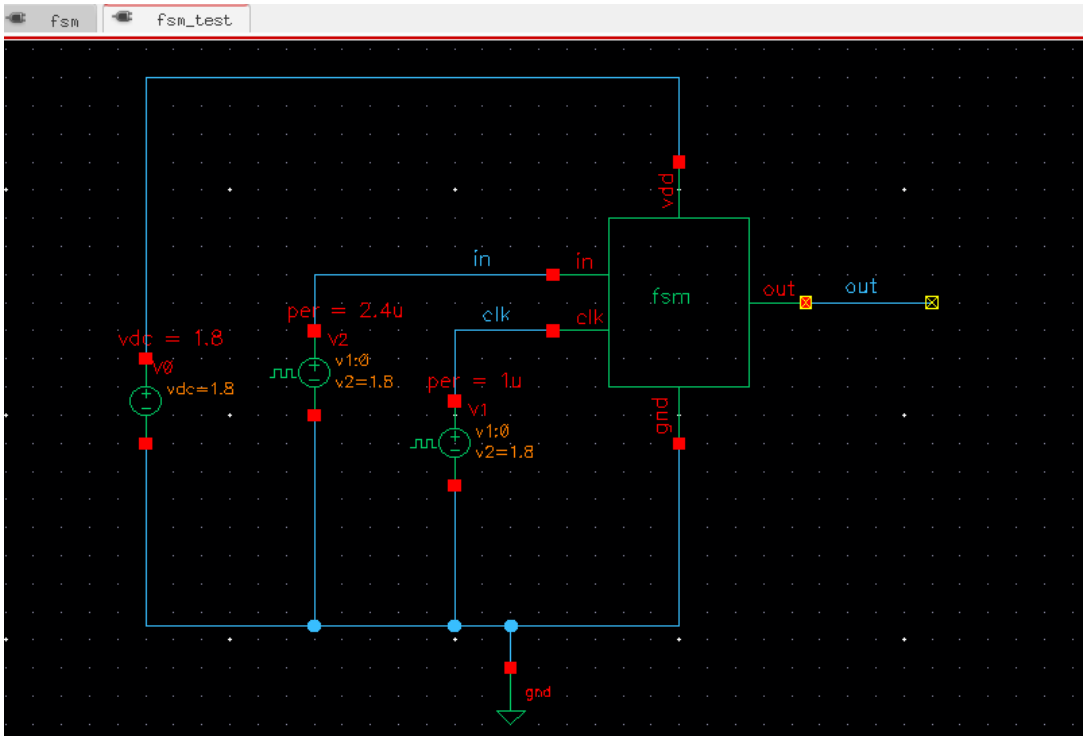
As shown in the above schematic, ‘in’ is the input and out’ is the output and we use 2 flip flops, an inverter, an AND gate, and an XOR gate.

Instead of applying power sources, I have attached pins in the schematic to create a symbol for it and then using it to test the working of the FSM. So the symbol is created and shown below:



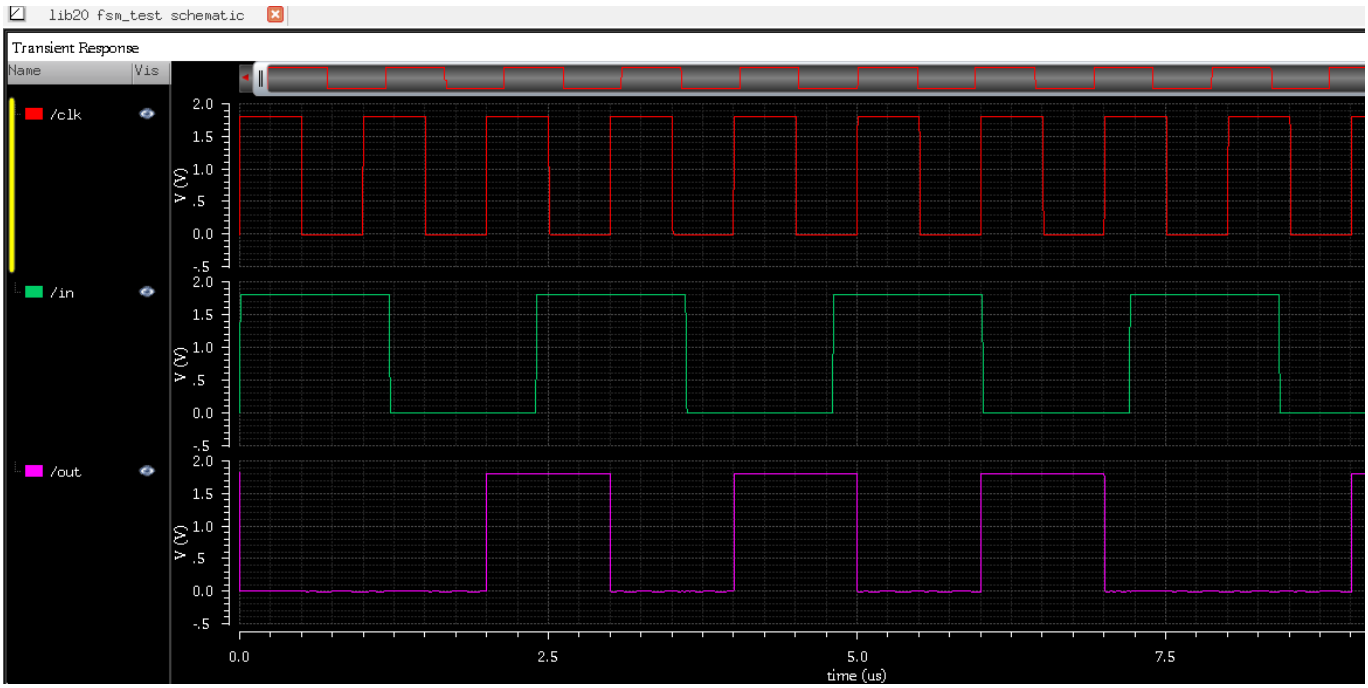
Symbol of FSM

Now, we have to test our symbol, so we add it in a new schematic, apply the power sources and make the connections.



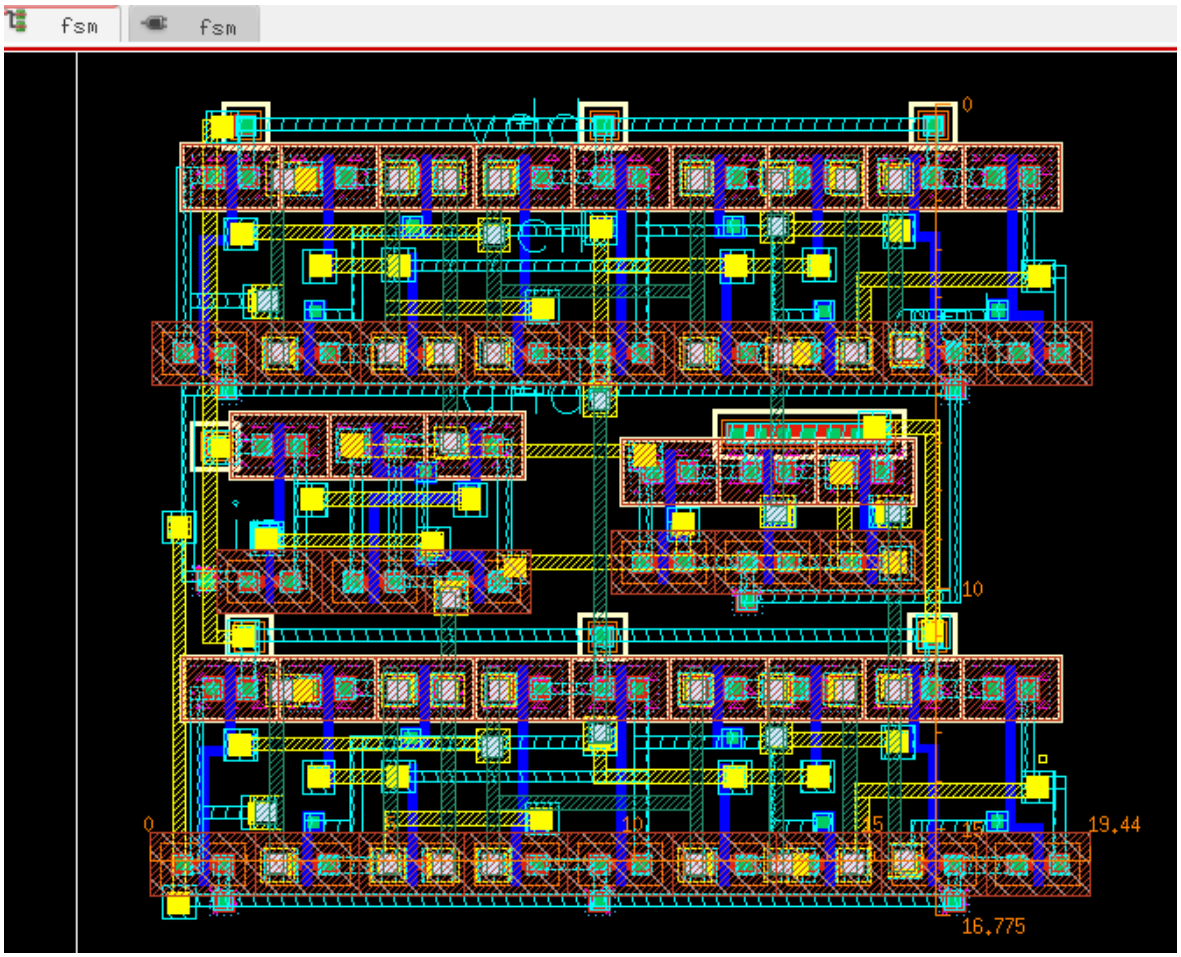
Circuit Diagram of FSM with symbol to test its working

The results obtained from the FSM symbol are shown below, and it is verified that our FSM is working properly and in accordance with the theory.



Inputs – clk (red) & in (green). Output – out (purple)

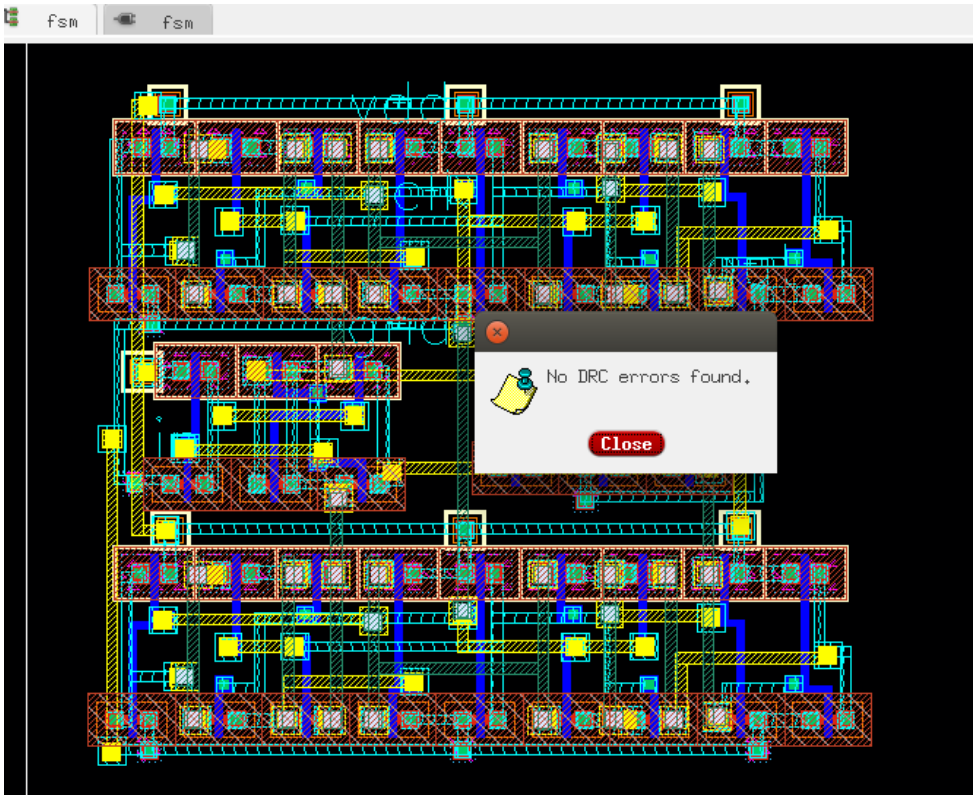
Now we will make the layout for our FSM, and try to minimise the area and draw it in accordance with the lambda rules. The layout formed is shown below:



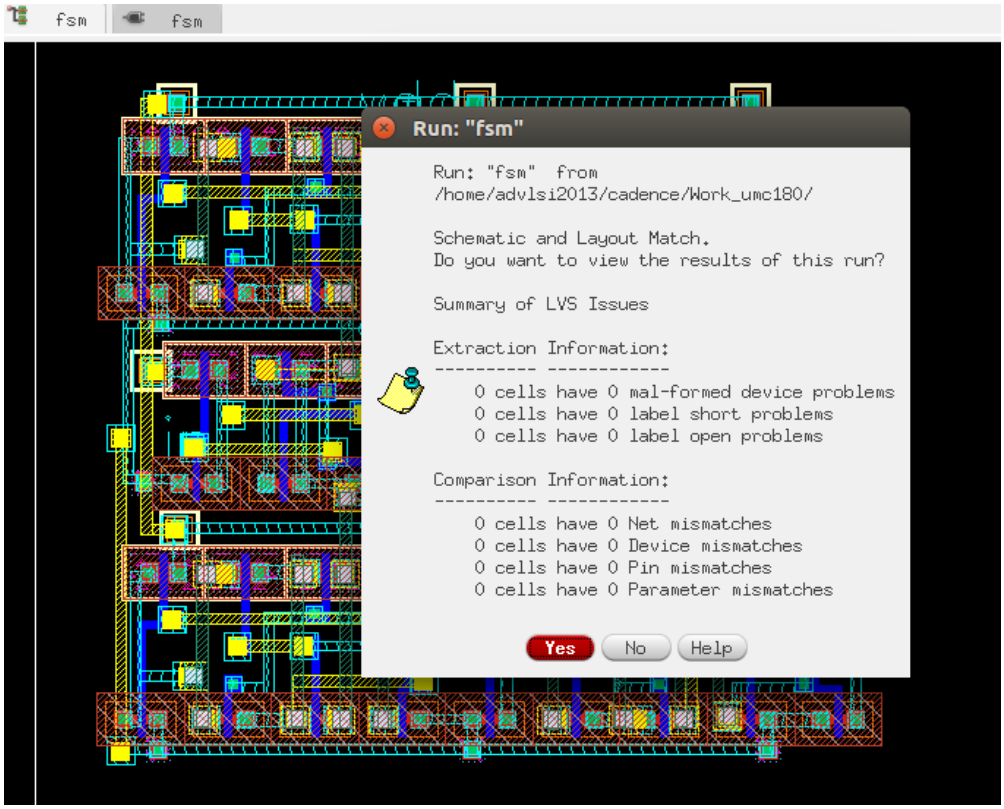
Layout of SRAM

The area consumed by our layout is approximately 19.44um x 16.775um = 326.1 um^2, which is around 90585 λ^2, as the value of λ is 0.06um, which can be verified in cadence.

The results of the DRC test and LVS test for our FSM were successful for the layout formed, i.e., there were no errors in the layout and also it is now matched with the schematic which we had drawn earlier.

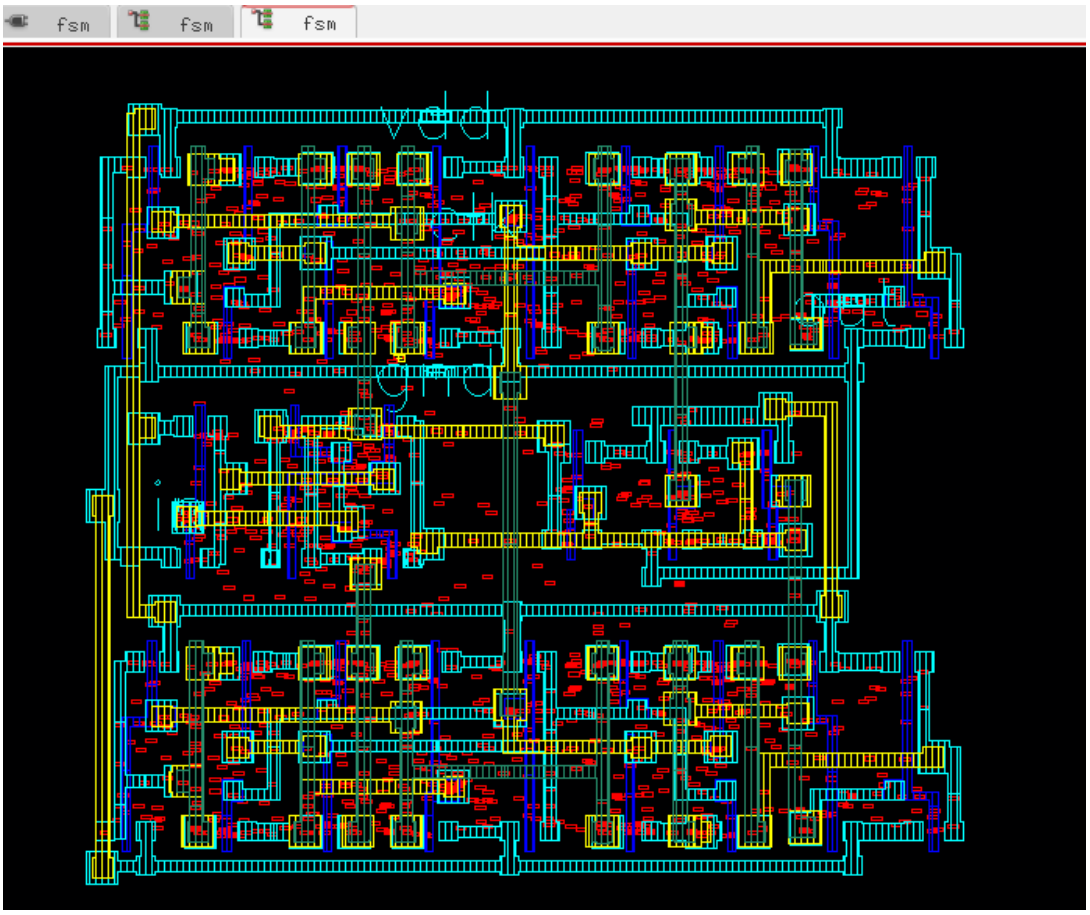


Result of DRC test (successful)



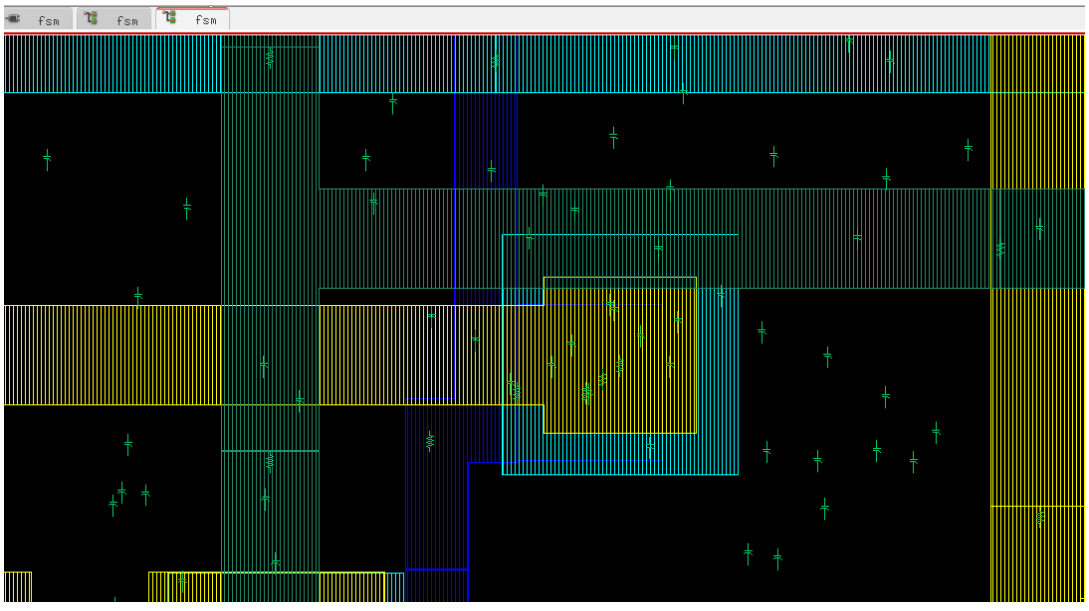
Result of LVS test (successful)

Now, for the post simulation process, the RCX test is run to generate the extracted view of the layout, which shows the presence of various parasitic capacitances and resistances and it is shown below:

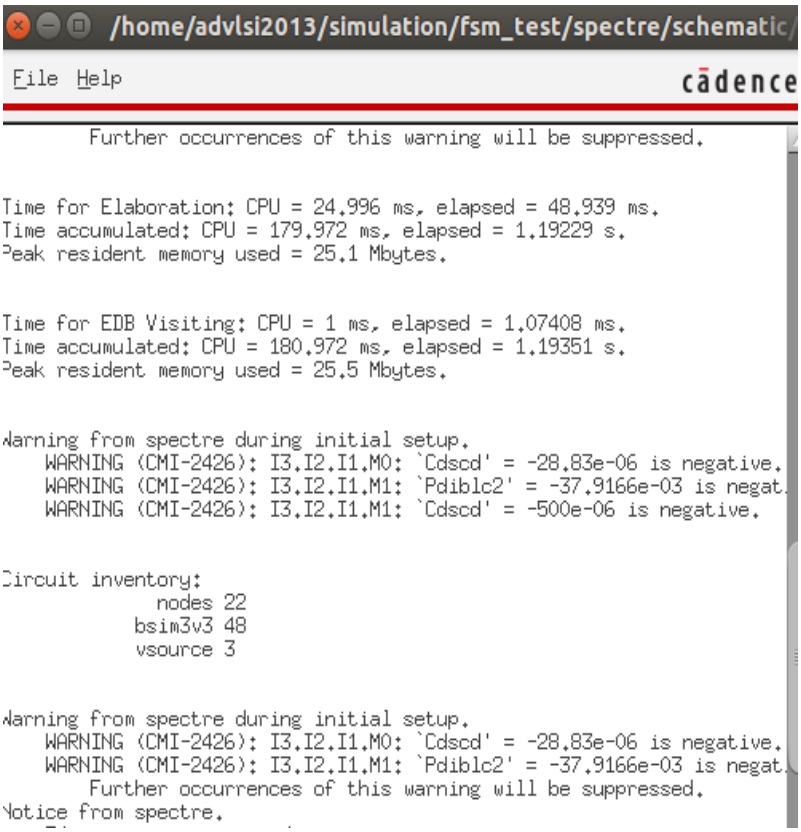


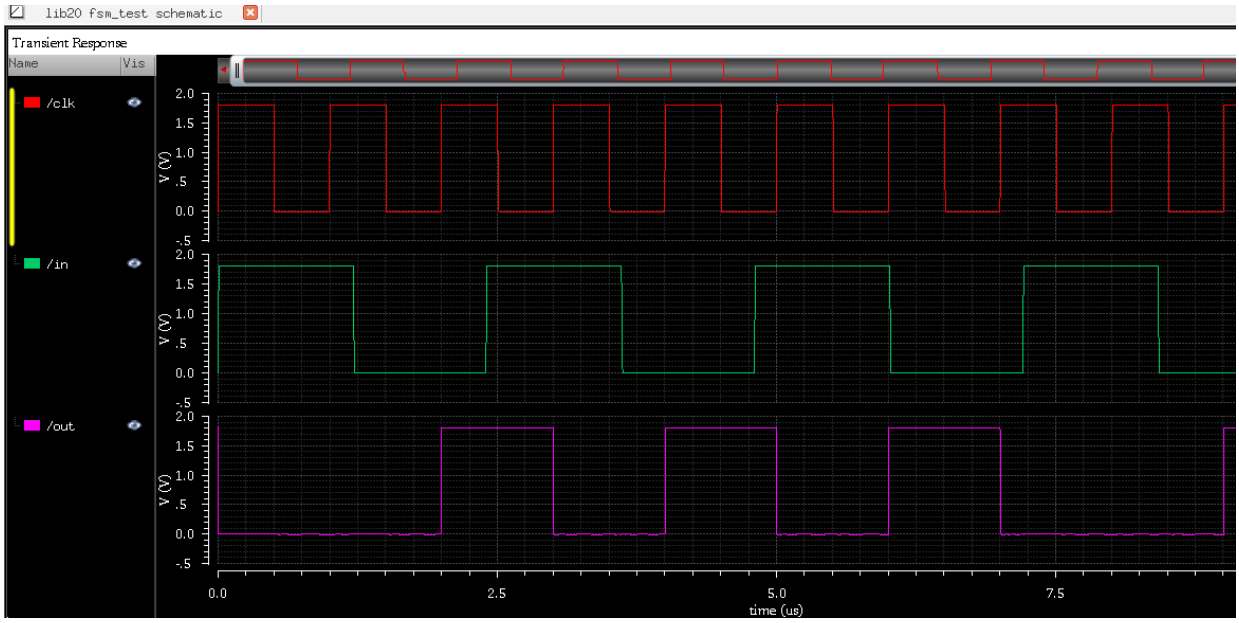
Extracted view of the layout with parasitic capacitances and resistances

When this extracted view is zoomed, we can clearly see the presence of parasitic capacitances and parasitic resistances in metals, vias and poly.



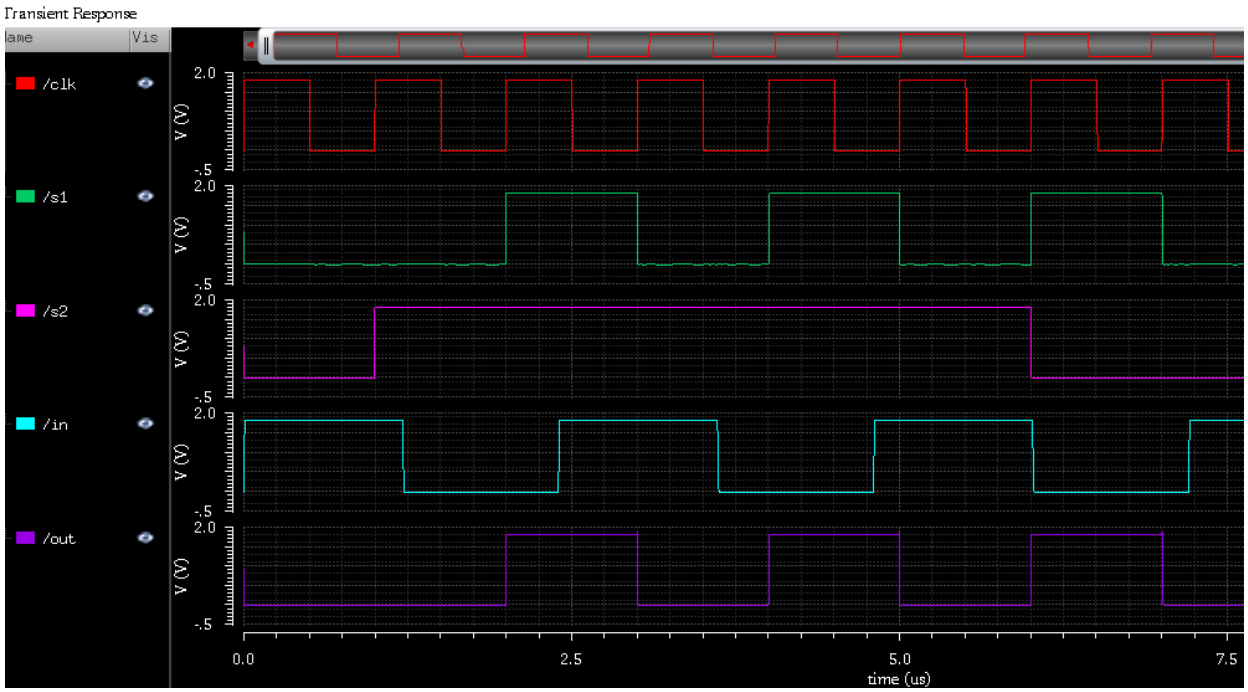
Now transient analysis is done and results are as shown and we can see that there are 22 nodes, 48 transistors and 3 power sources in the circuit:





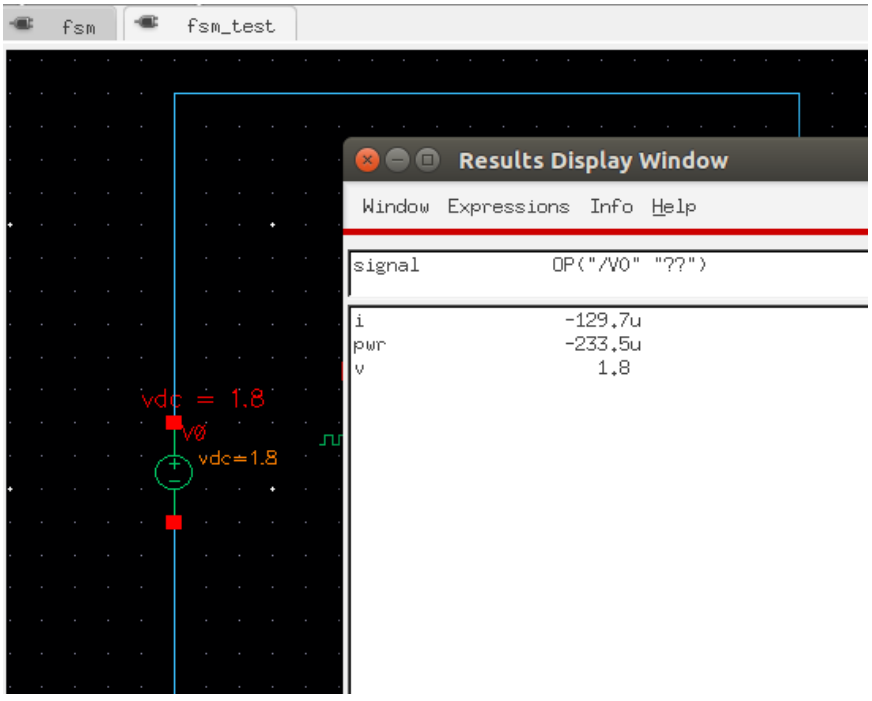
Inputs – clk (red) & in (green). Output – out (purple)

Also we can verify that our states of the FSM are changing properly according to the input and also the output is properly coming as expected from the theoretical equations.



Inputs – clk (red) & in (blue). Output – out (purple). States – s1 (green) & s2 (pink).

Now, for the calculation of the power, we do the DC analysis of the FSM test circuit and it is found that the power consumed by our FSM is 233.5uW.



Hence we have successfully done the designing of the FSM and have properly minimized the number of transistors, minimized the area of the layout according to the lambda rules and also minimized the power.

Thus our FSM design is successfully completed and finally the following conclusions are made.

Transistors used : 48 (24NMOS + 24PMOS).
Area : 330um^2 .
Power consumed : 233.5uW.
Longest delay path : The maximum delay occurs for the output ‘out’ as it takes around 22 transistors for the input ‘in’ to affect the output.