Intro to VLSI

Lab Task 3 – NOT gate (inverter)

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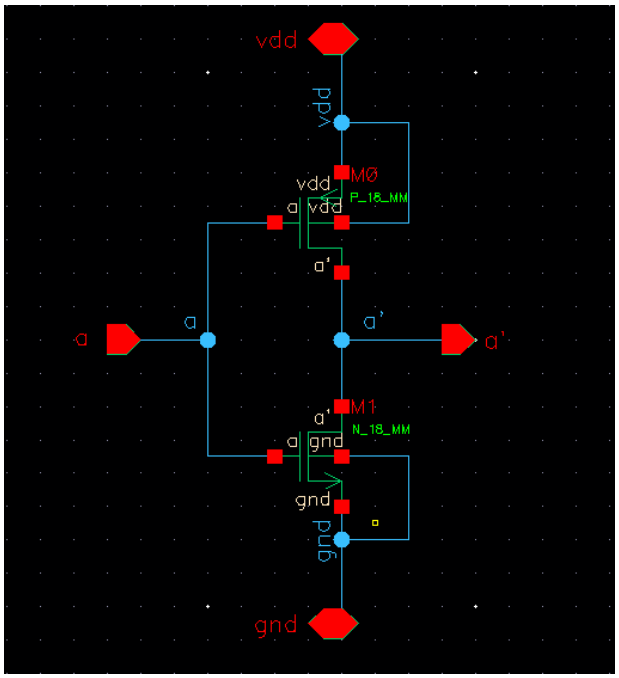
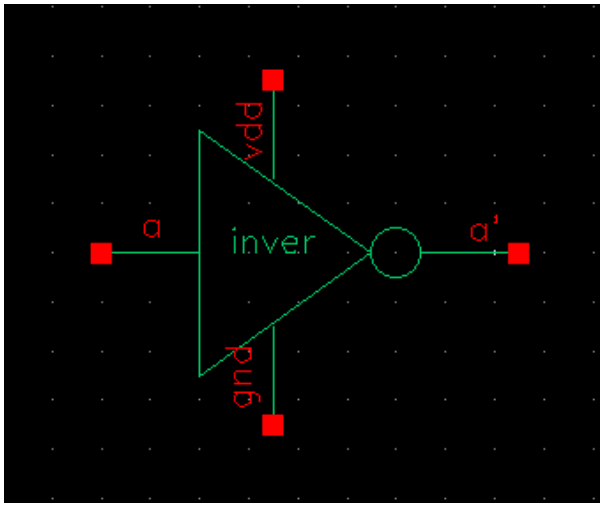
(20171049)

I have designed the NOT gate schematic which is as shown in figure below:



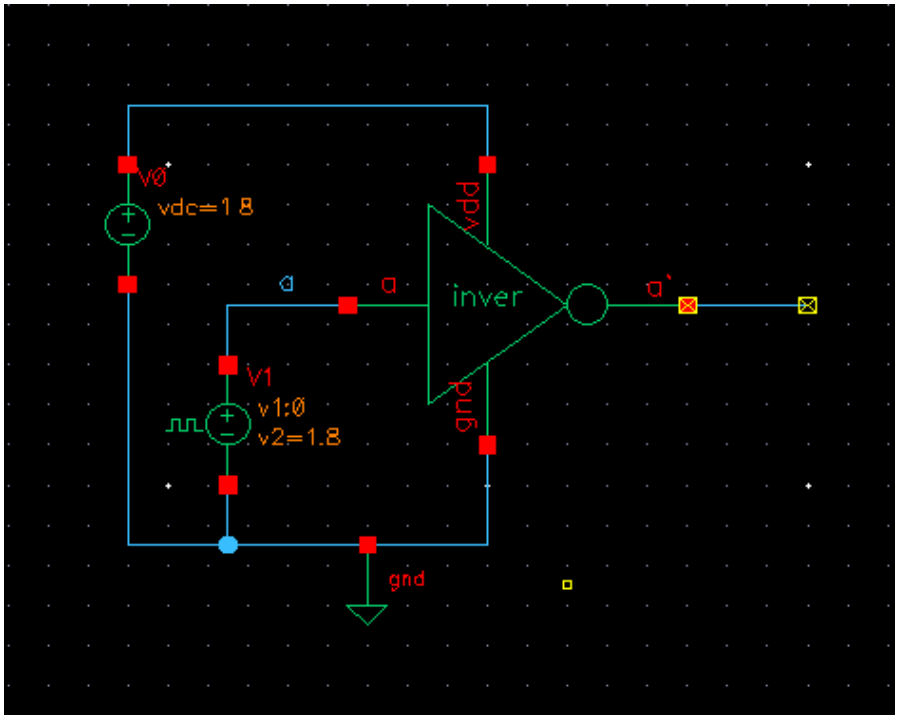
Schematic of NOT gate

Instead of applying power sources, I have attached pins in the schematic to create a symbol for it and then using it to test the working of the NOT gate. So the symbol is created and shown below:



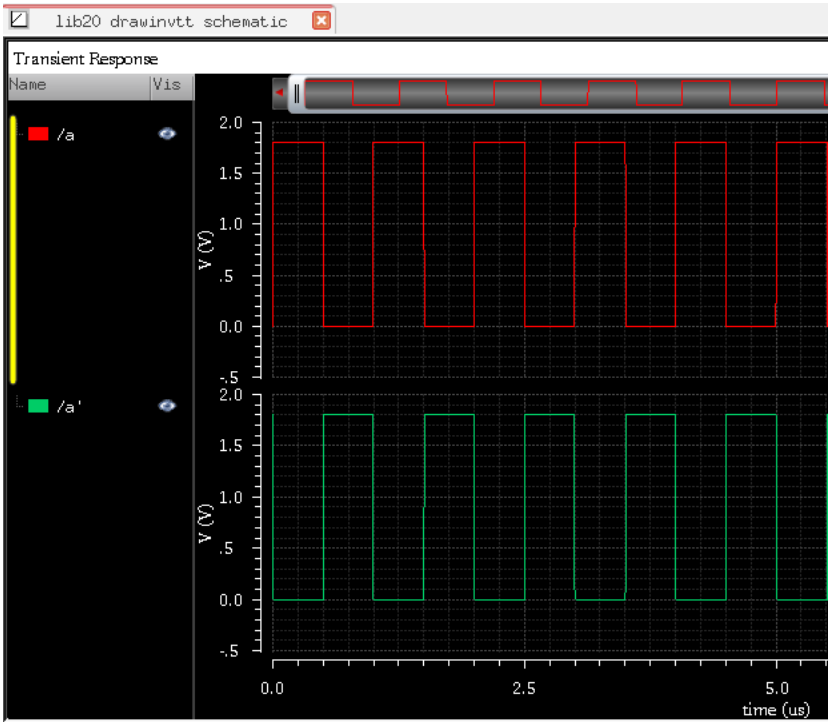
Symbol of NOT gate

Now, we have to test our symbol, so we add it in a new schematic, apply power sources and make the connections properly.



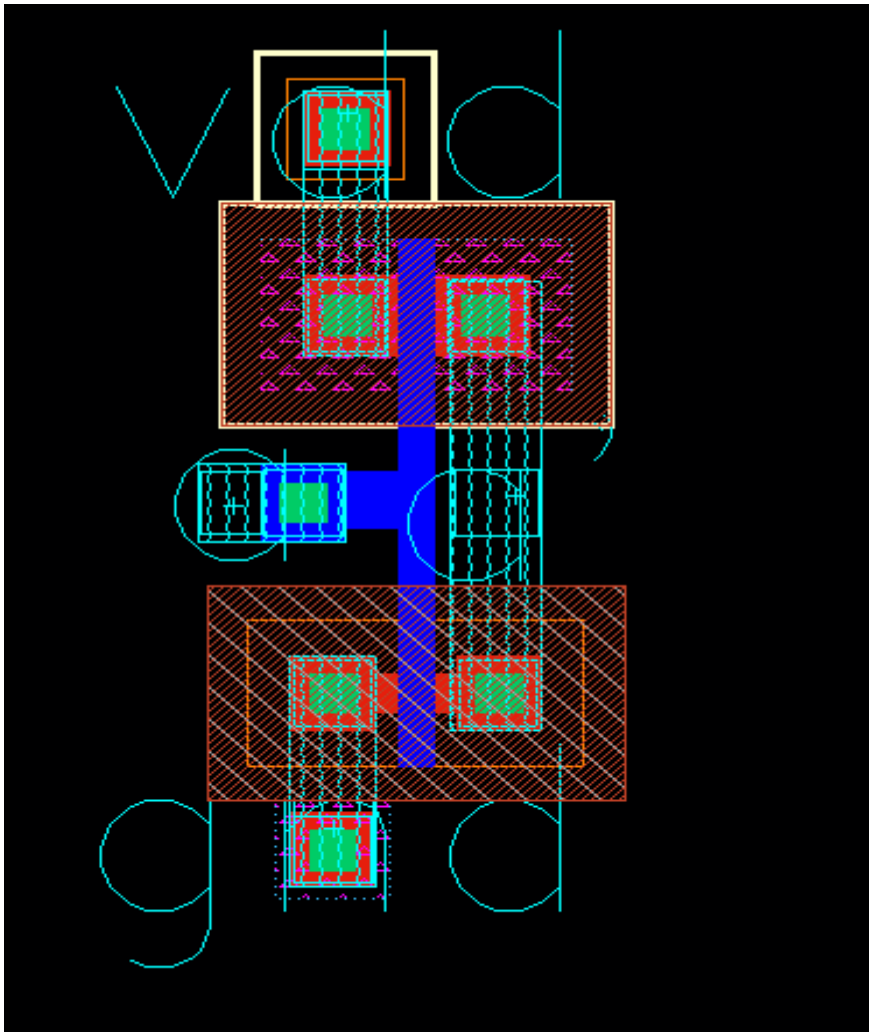
Circuit Diagram of NOT gate with symbol

The results obtained from the NOT gate symbol are shown below, and it is verified that our NOT gate is working properly.



Input – a (red). Output – a’ (green)

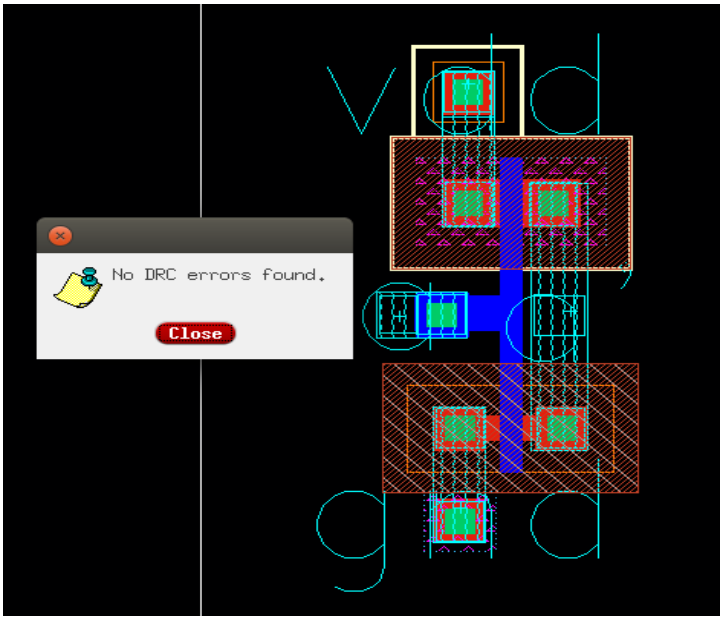
Now we will make the layout for our NOT gate, and draw it in accordance with the lambda rules. The layout formed is shown below:



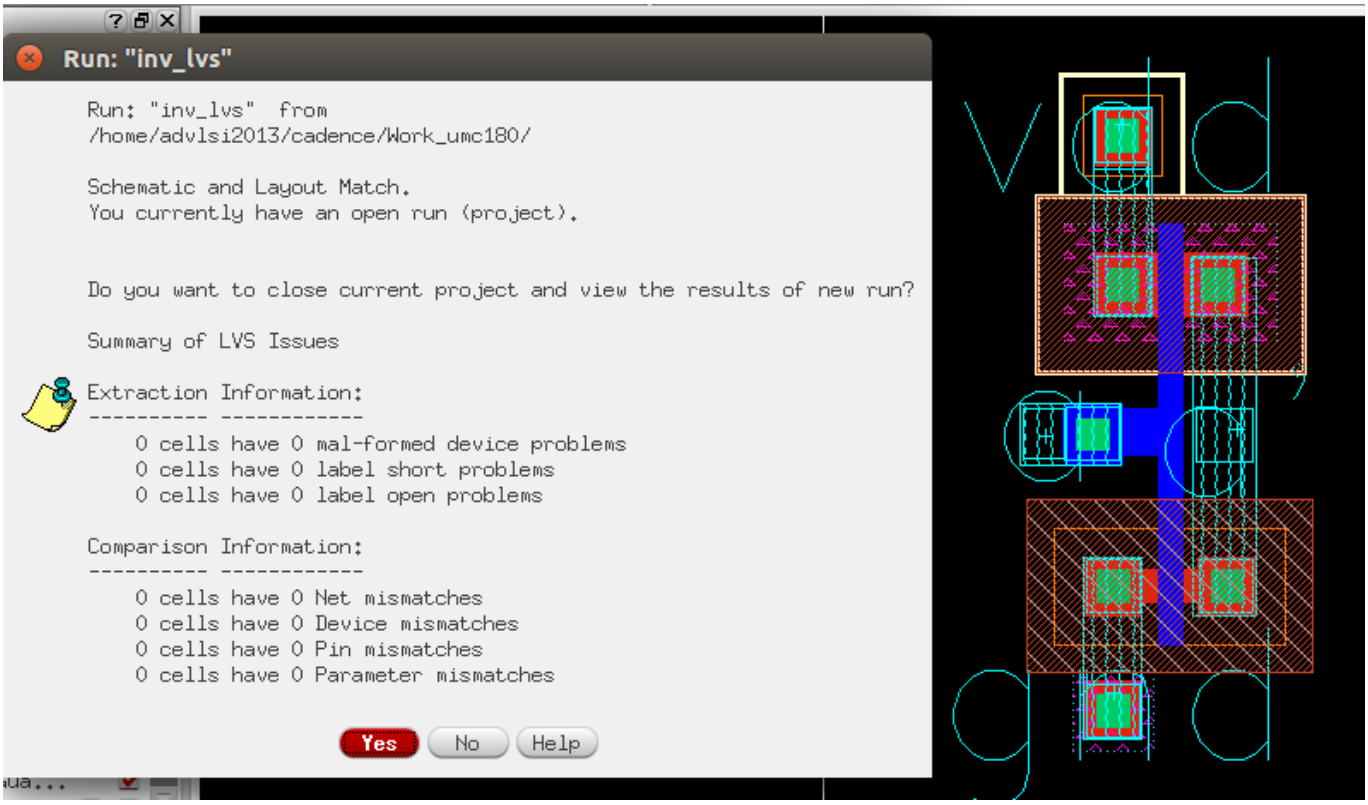
Layout of NOT gate

We have minimized the area and it is found that the minimized area is 4.816um x 2.16um = 10.402 um^2.

The results of the DRC test and LVS test were successful for the layout formed, i.e., there were no errors in the layout and also it is now matched with the schematic which we had drawn earlier.

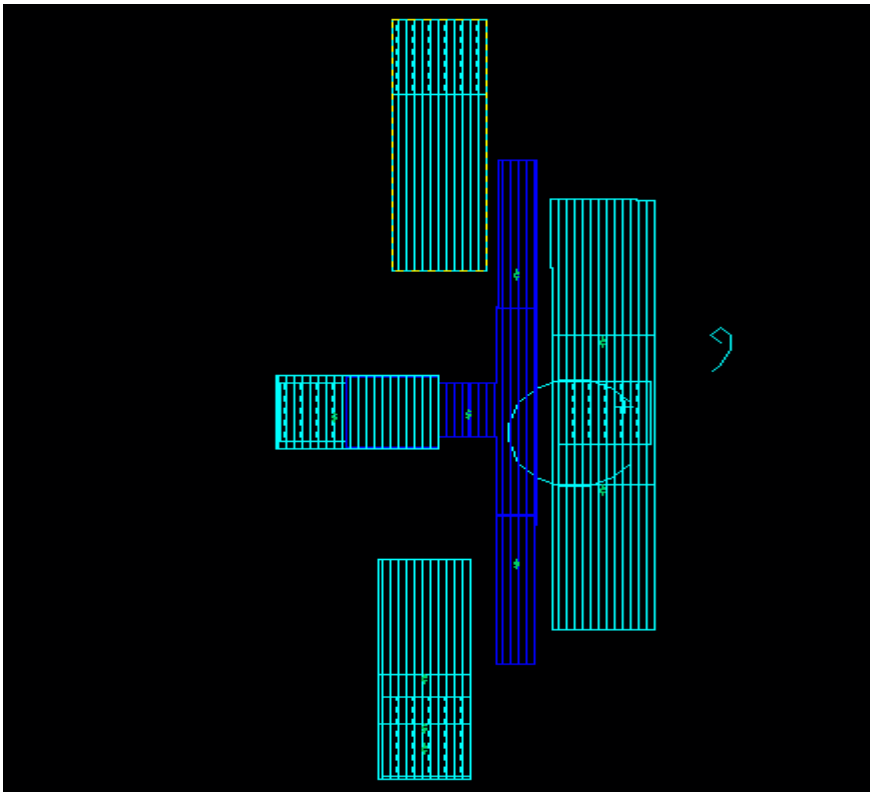


Result of DRC test (successful)



Result of LVS test (successful)

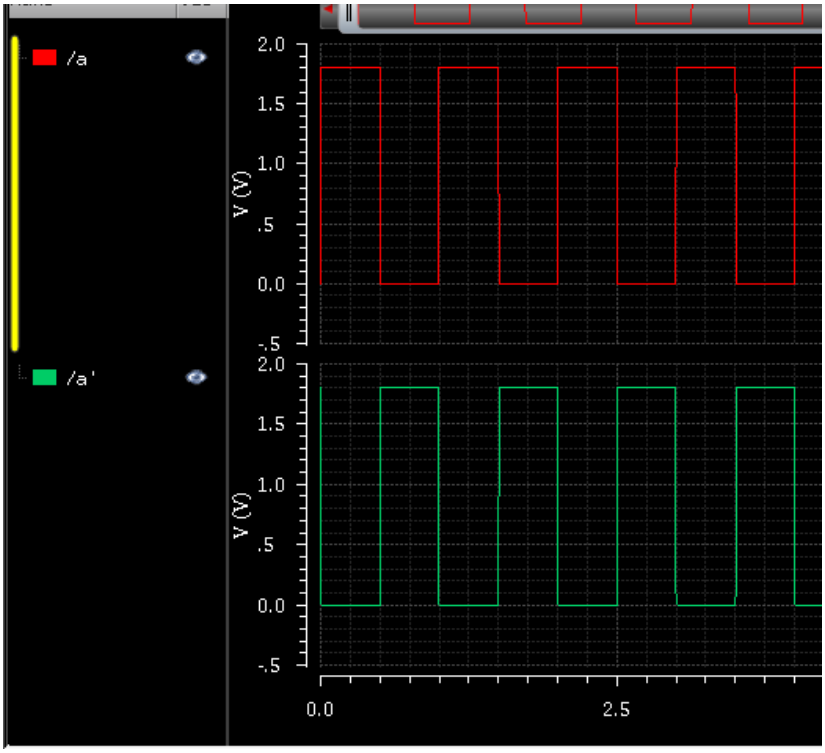
Now, the RCX test is run to generate the extracted view of the layout, which shows the presence of various parasitic capacitances and resistances and it is shown below:



Extracted view of the layout with parasitic capacitances and resistances

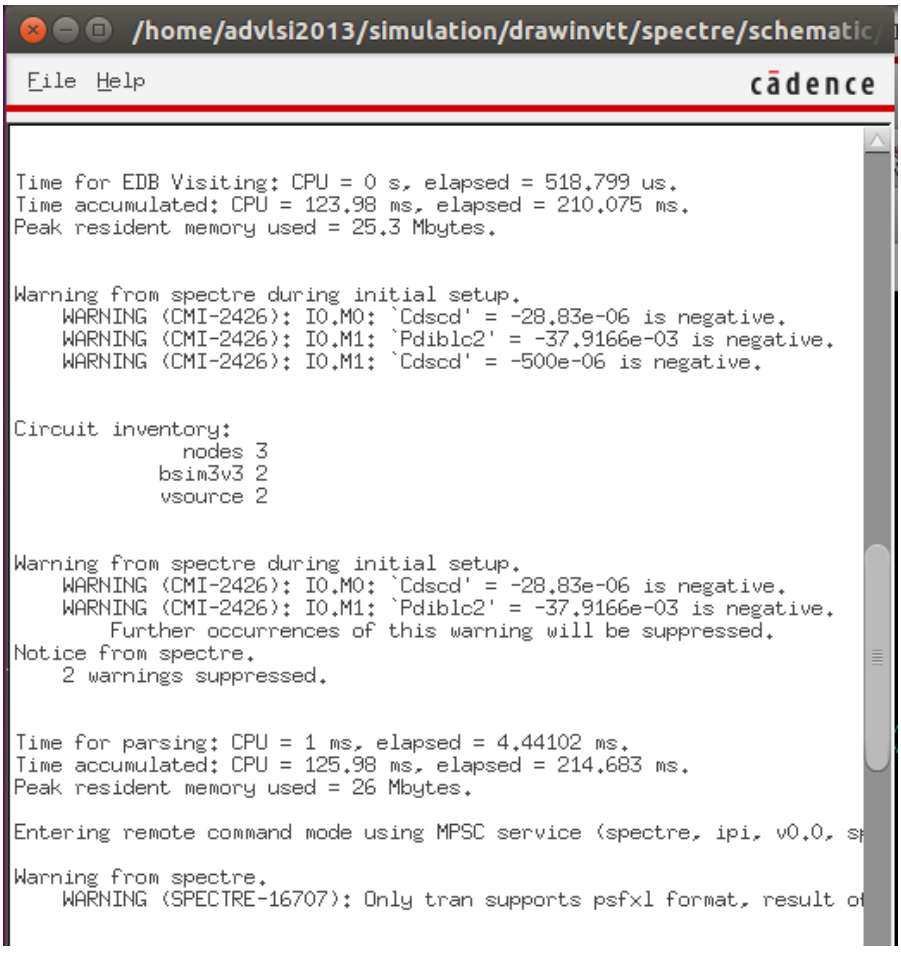
We can now ensure that our layout drawn also gives correct results. So, changing the hierarchy of our symbol from schematic to layout, the following results were obtained and we can see that the output is coming correctly from the transient analysis of the circuit. Also we can see the presence of multiple resistances, capacitances, and nodes in the results, which were not in the schematic.

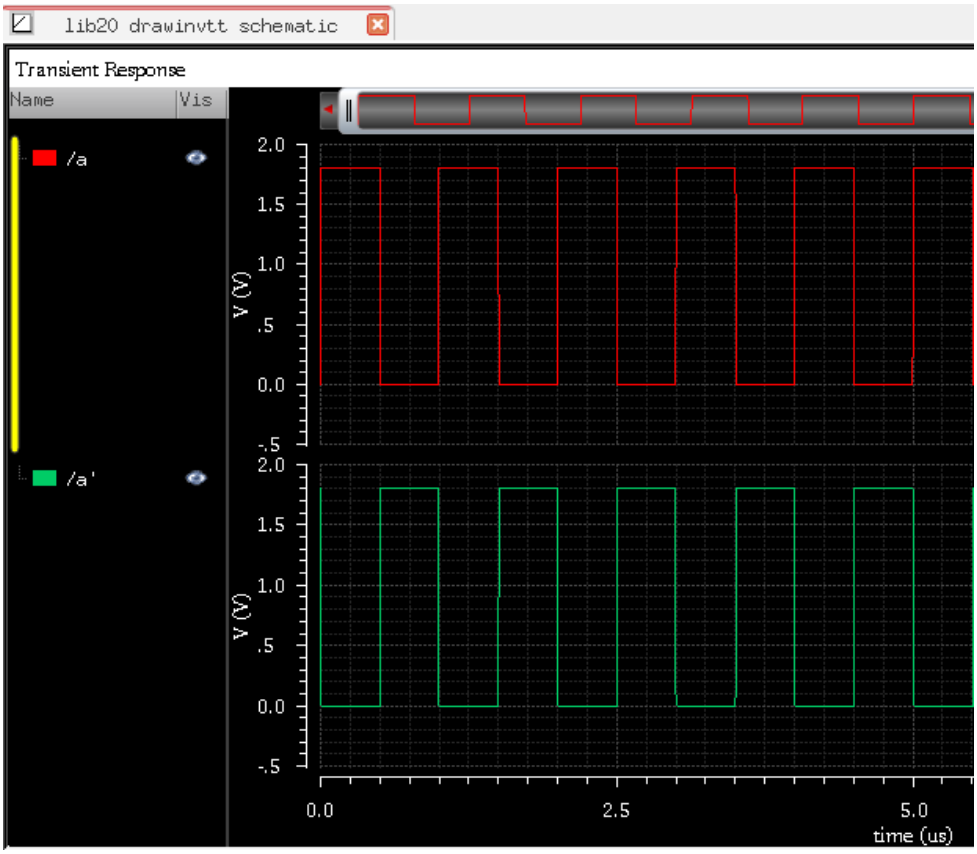
```
Warning from spectre during initial setup.
    WARNING (CMI-2426): I2.M1: `Cdscd' = -28.83e-06 is negative.
    WARNING (CMI-2426): I2.M0: `Pdiblc2' = -37.9166e-03 is negative.
    WARNING (CMI-2426): I2.M0: `Cdscd' = -500e-06 is negative.


Circuit inventory:
             nodes 8
           bsim3v3 2
         capacitor 24
          resistor 5
           vsource 2


Warning from spectre during initial setup.
    WARNING (CMI-2426): I2.M1: `Cdscd' = -28.83e-06 is negative.
    WARNING (CMI-2426): I2.M0: `Pdiblc2' = -37.9166e-03 is negative.
        Further occurrences of this warning will be suppressed.
Notice from spectre.
    2 warnings suppressed.


Time for parsing: CPU = 3 ms, elapsed = 5.28097 ms.
Time accumulated: CPU = 133.979 ms, elapsed = 216.153 ms.
Peak resident memory used = 26.1 Mbytes.

Entering remote command mode using MPSC service (spectre, ipi, v0.0, sp

Warning from spectre.
    WARNING (SPECTRE-16707): Only tran supports psfxl format, result of
```



Inputs – a (red) & b (green). Output – y (purple)

Now, we compare the results of the original schematic with that of the results from layout hierarchy. Again transient analysis is done and results are as shown:





Input – a (red). Output – a' (green)

So, the comparison between the results of the layout and the schematic of the NOT gate are approximately same. There are very little distortions in the output waveforms of the layout which is not in the case of schematic. So, the layout and the schematic are successfully verified theoretically also. Thus our NOT gate design is successfully completed. Also the area of the layout was minimized and was found to be 10.402 um^2.