Intro to VLSI

Lab Task 7 – Multiplier

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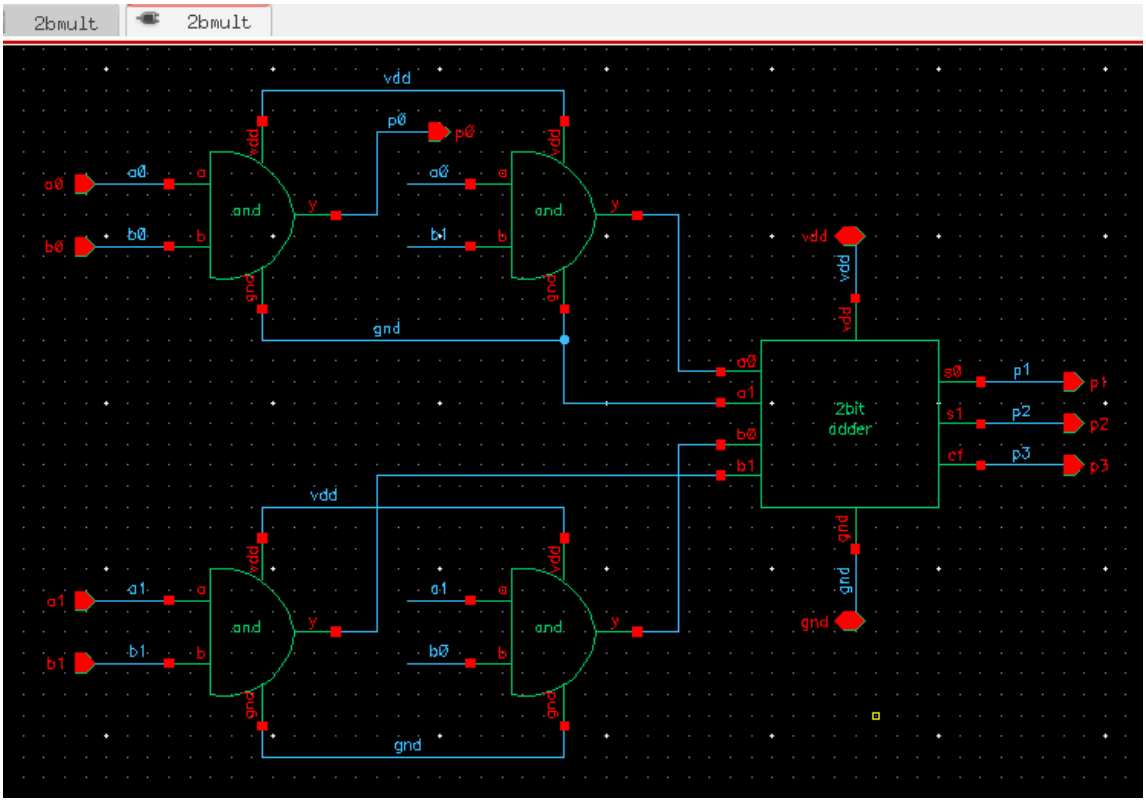
(20171049)

A 2 bit multiplier can be designed by using a 2 bit adder and 4 AND gates. So first we implement an AND gate and check its working. And then we will use the 2 bit adder designed by us in the previous lab and make its connections properly with the AND gates according to the multiplier.

Design of Multiplier:

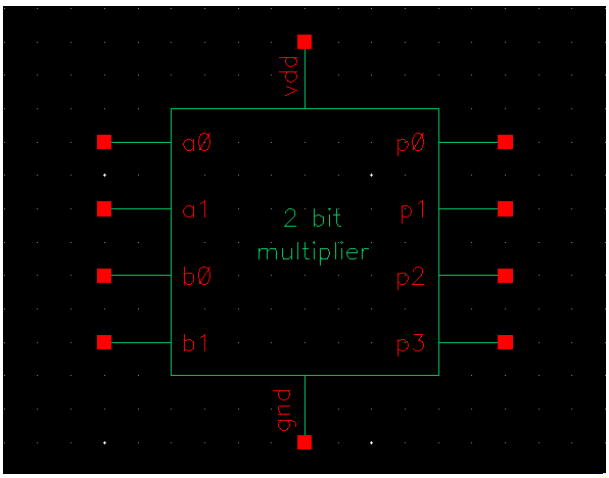
I have designed the multiplier which is as shown in figure below:



Schematic of Multiplier

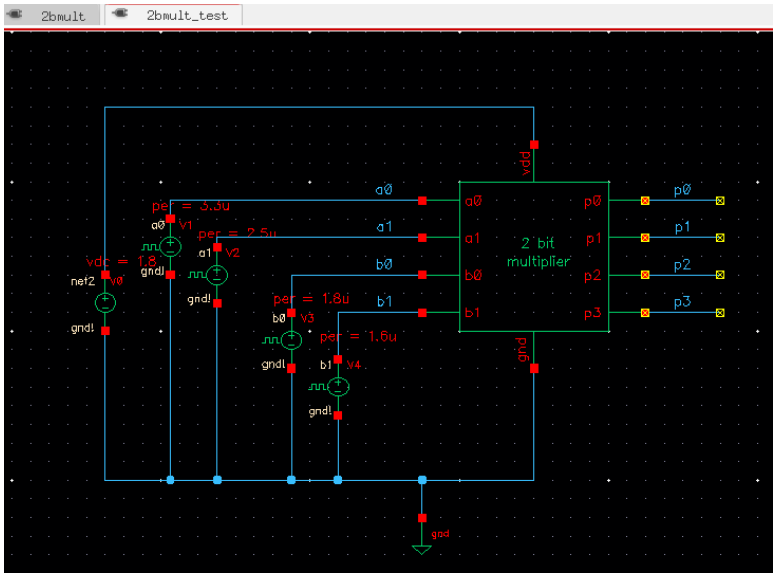
In the schematic of a multiplier, there are 2 inputs of 2 bits each, which we have to multiply. So first we calculate the partial results from the AND gates and then send it properly to the 2 bit adder in order to obtain the product of the inputs.

Instead of applying power sources, I have attached pins in the schematic to create a symbol for it and then using it to test the working of the 2 bit adder. So the symbol is created and shown below:



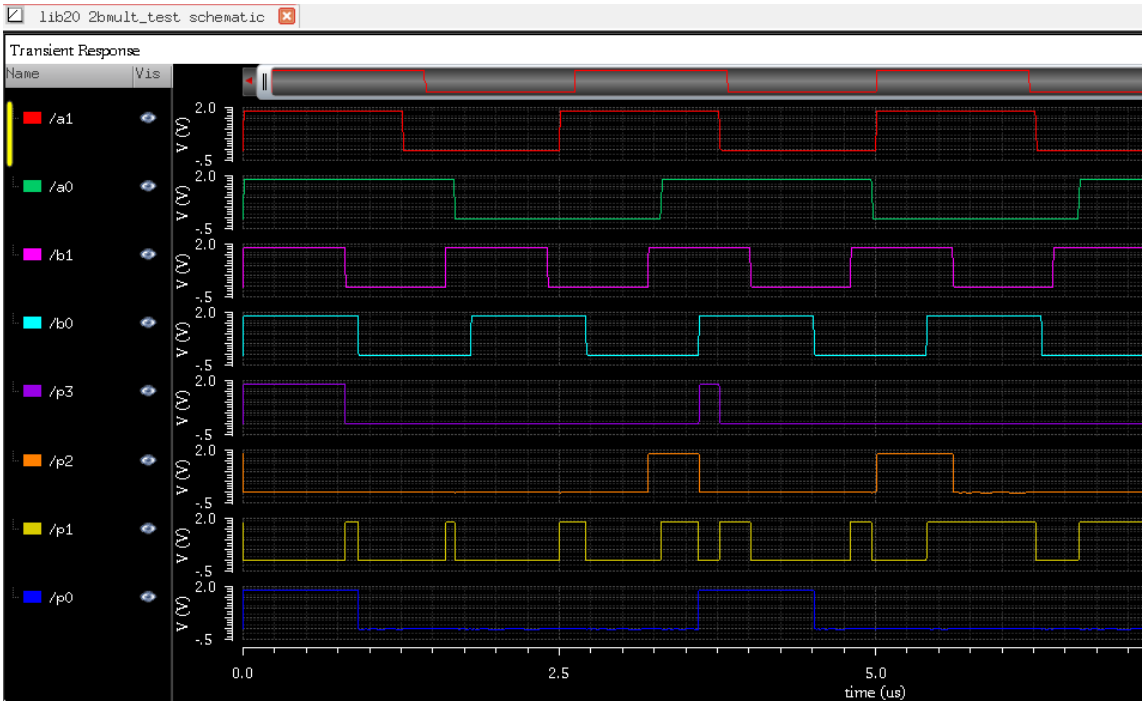
Symbol of a multiplier

Now, we have to test our symbol, so we add it in a new schematic, apply power sources and make the connections properly.



Circuit Diagram of a multiplier with symbol to test the working

The results obtained from the multiplier symbol are shown below, and it is verified that our multiplier is working properly.



Inputs – a1(red), a0(green), b1(pink) & b0(blue).

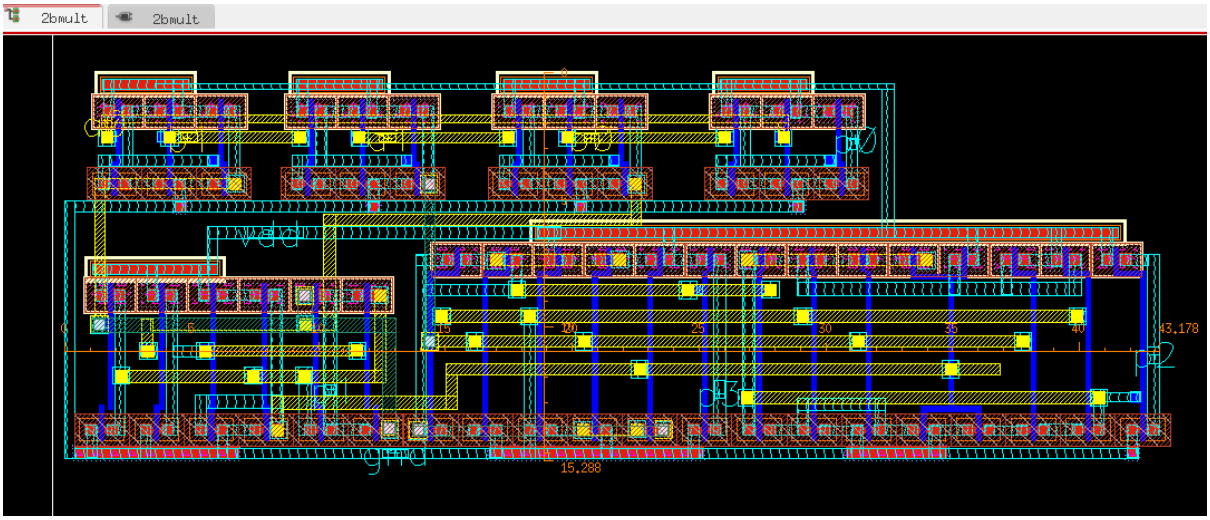
Outputs – p3(purple), p2(orange), p1(yellow), p0(dark blue).

From the above graph, we can clearly see that the results of it are in accordance with that of the theoretical values. So we can say that our multiplier is working properly.

Now we will make the layout for our multiplier, and draw it in accordance with the lambda rules. The layout formed is shown in the below figure.

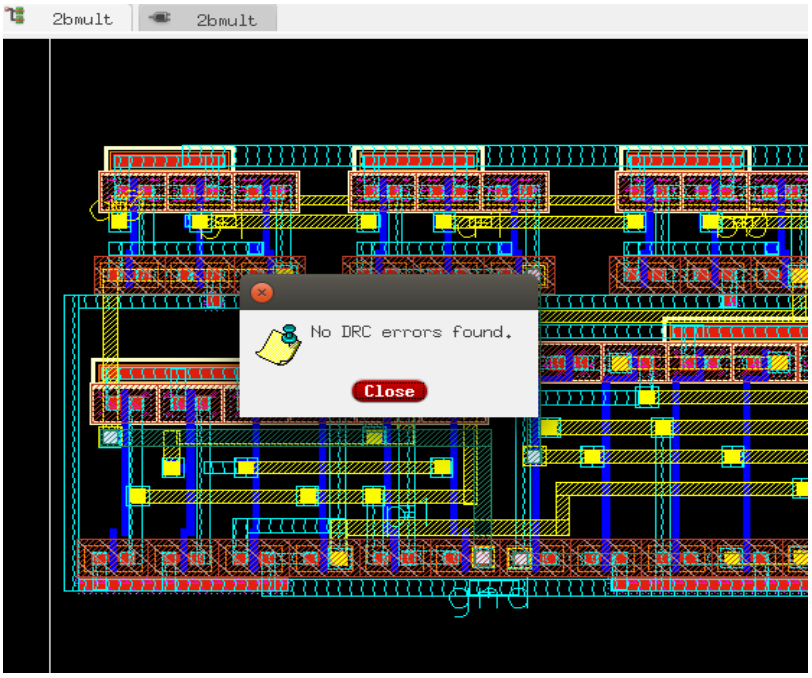
The area of the layout is minimized according to the lambda rules and it is found out that the minimum area required to built a multiplier is 43.178um x 15.288um = 660.1um^2, which is equal to 183361λ^2. (λ=0.06um and can be verified in cadence).

The following is the layout formed:

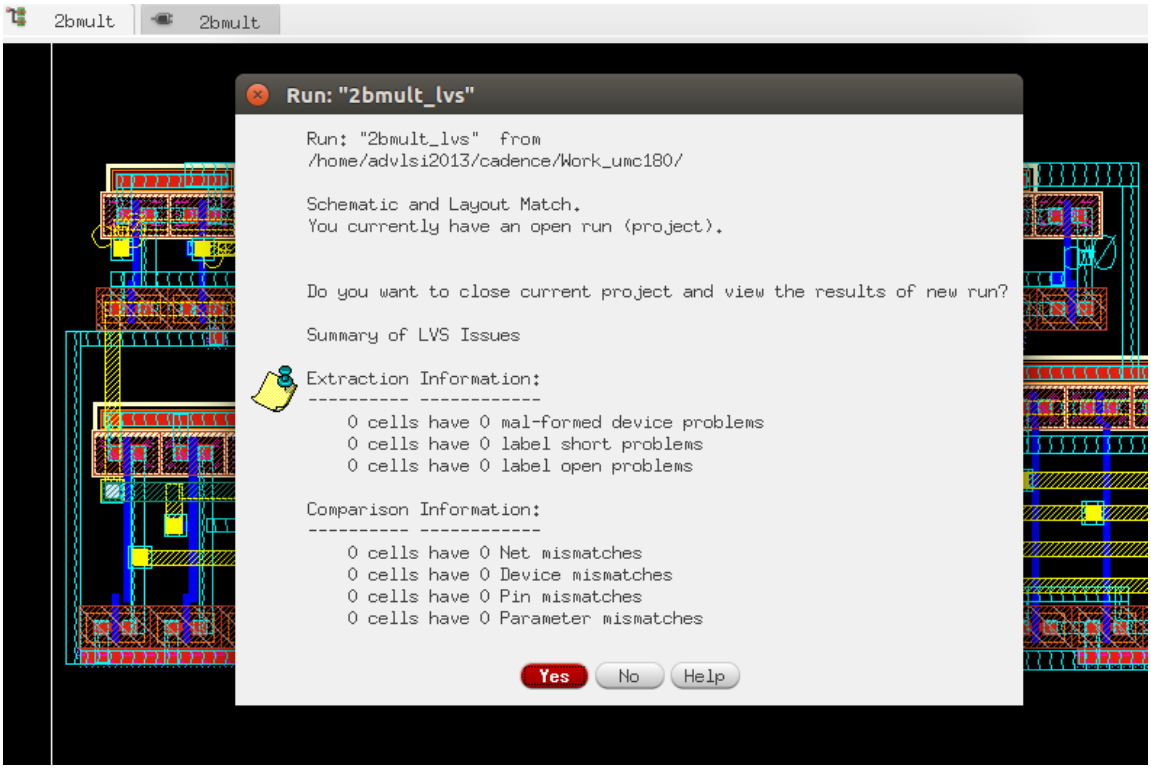


Layout of Multiplier

The results of the DRC test and LVS test were successful for the layout formed, i.e., there were no errors in the layout and also it is now matched with the schematic which we had drawn earlier.

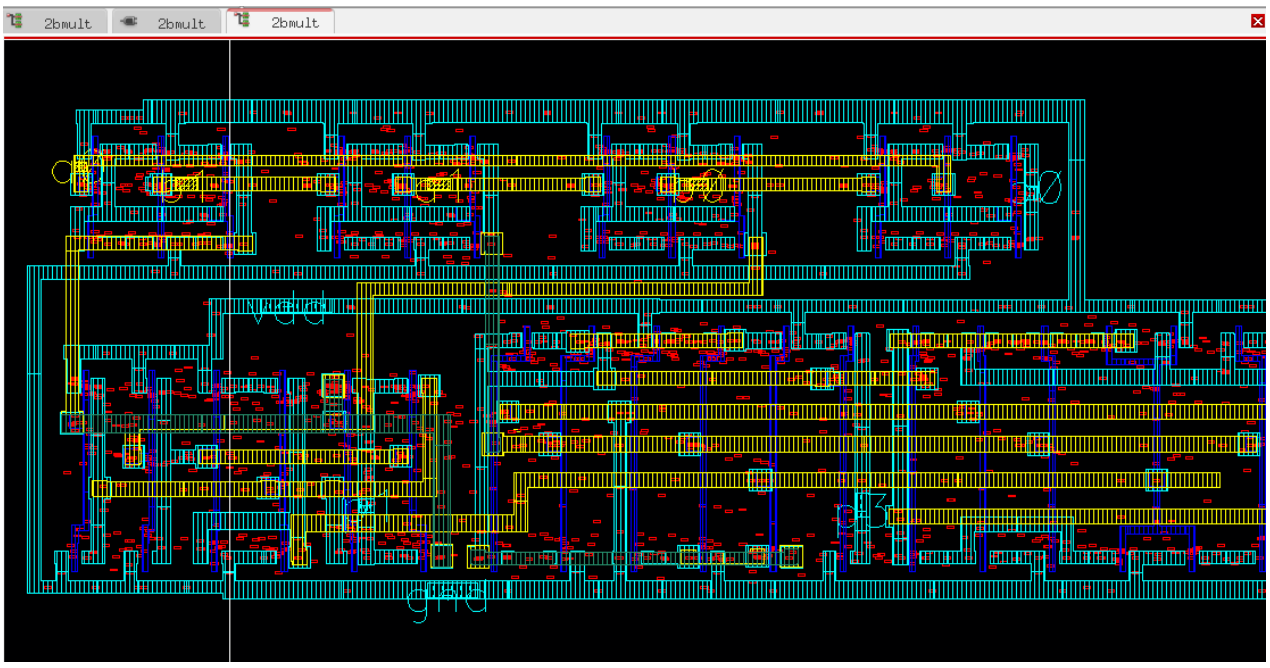


Result of DRC test (successful)



Result of LVS test (successful)

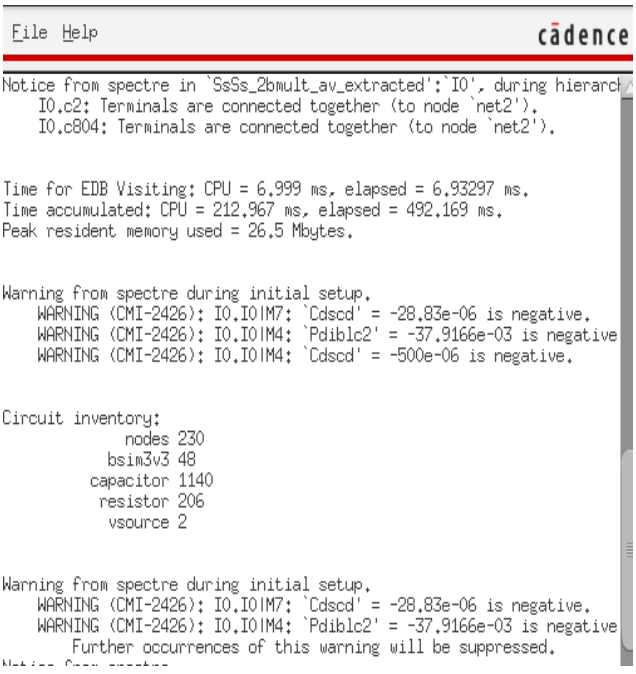
Now, the RCX test is run to generate the extracted view of the layout, which shows the presence of various parasitic capacitances and resistances and it is shown below:

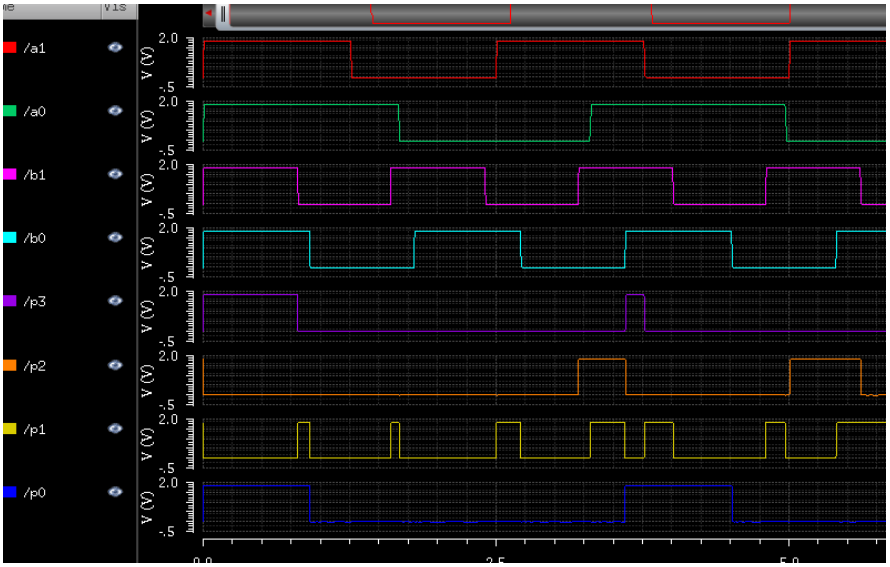


Extracted view of the layout with parasitic capacitances and resistances

When this extracted view is zoomed, we can clearly see in the above figure, the parasitic capacitances and parasitic resistances in metals and poly.

We can now ensure that our layout drawn also gives correct results. So, changing the hierarchy of our symbol from schematic to layout, the following results were obtained and we can see that the output is coming correctly from the transient analysis of the circuit. Also we can see the presence of multiple resistances, capacitances, and nodes in the results, which were not in the schematic.

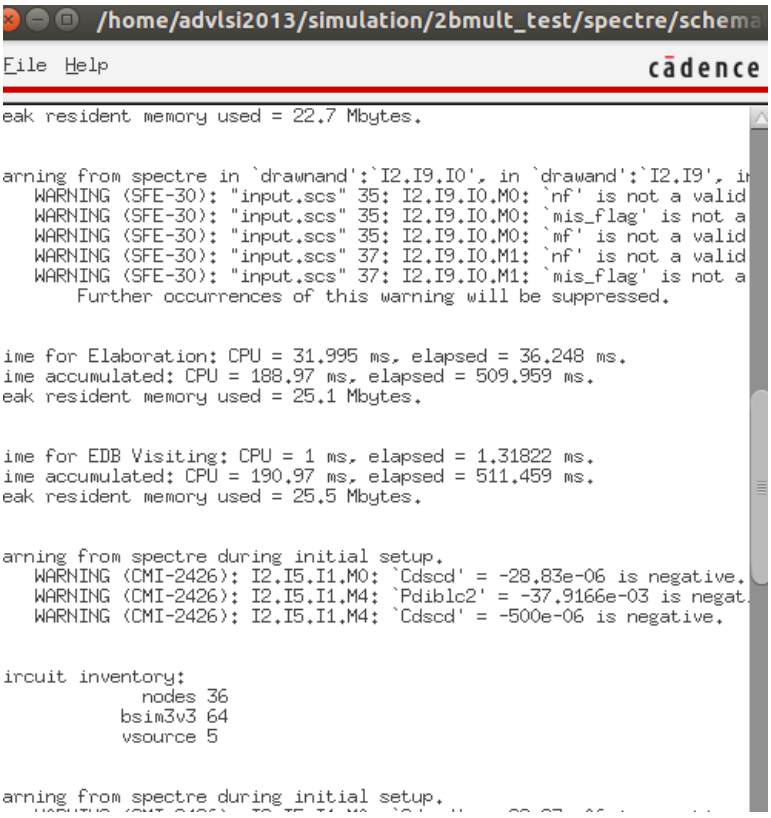


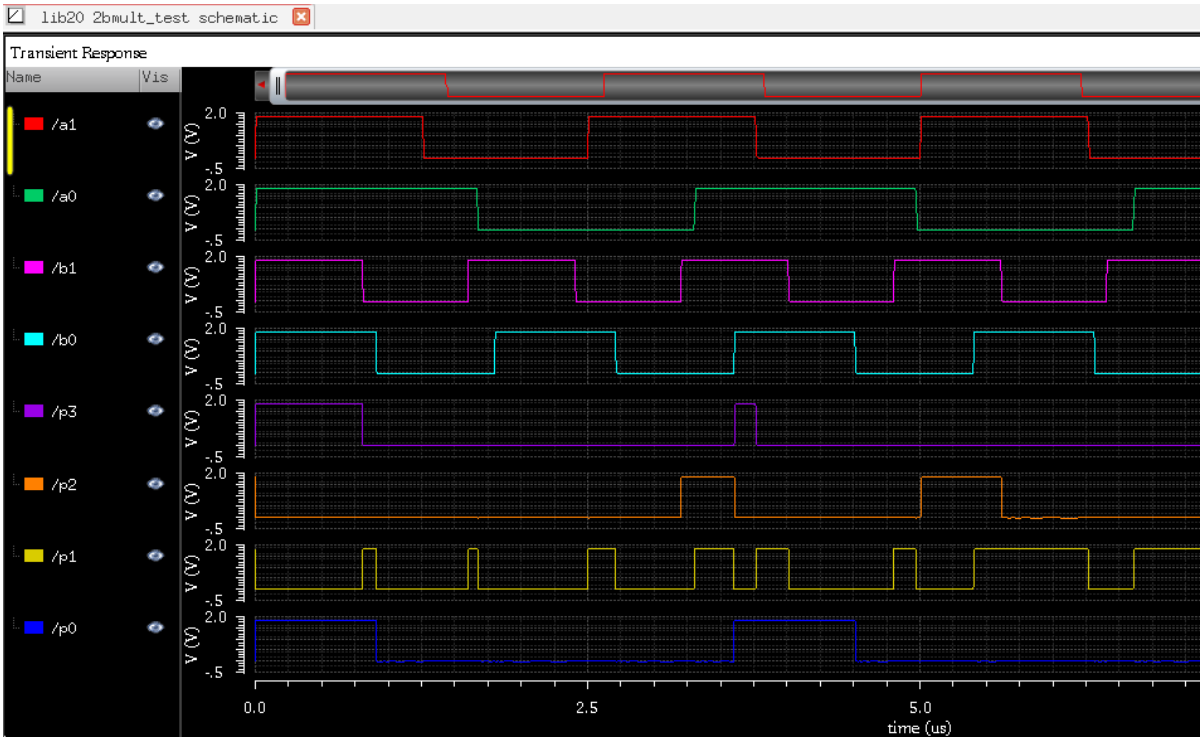


Inputs – a1(red), a0(green), b1(pink) & b0(blue).

Outputs – p3(purple), p2(orange), p1(yellow), p0(dark blue).

Now, we compare the results of the original schematic with that of the results from layout hierarchy. Again transient analysis is done and results are as shown:





Inputs – a1(red), a0(green), b1(pink) & b0(blue).

Outputs – p3(purple), p2(orange), p1(yellow), p0(dark blue).

So, the comparison between the results of the layout and the schematic of the multiplier are approximately same. There are very little distortions in the output waveforms of the layout which is not in the case of schematic. So, the layout's area is minimized and the schematic drawn are successfully verified theoretically also. Thus our multiplier design is successfully completed and the following conclusions are made.

No. of transistors used: 64 (32NMOS + 32PMOS).
Area consumed by layout: 660.1um^2.
Power consumption: 285.7uW. (calculated by doing DC analysis).
Longest delay path: Longest delay path is to compute the fourth bit of the product 'p3'.