Intro to VLSI

Lab Task 8 – Memory

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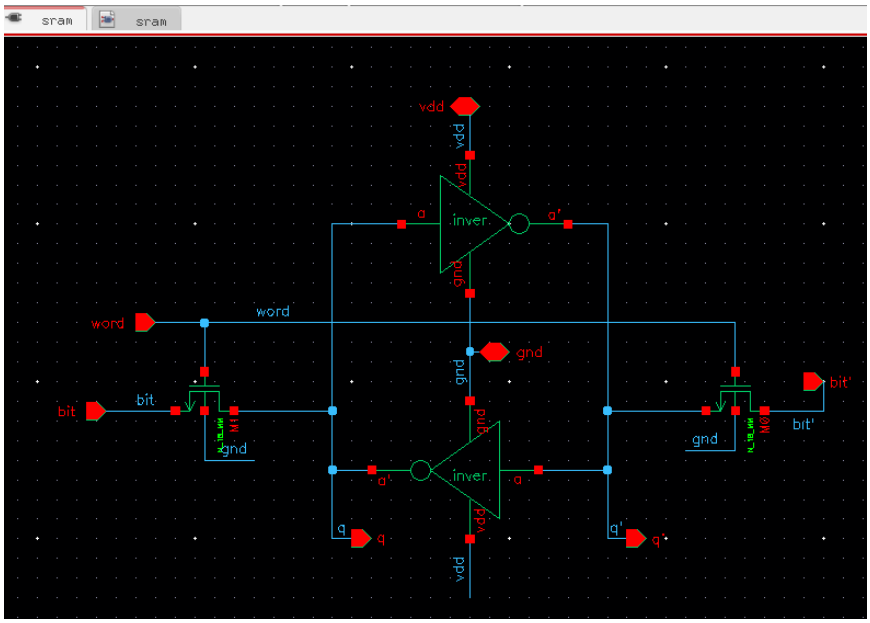
(20171049)

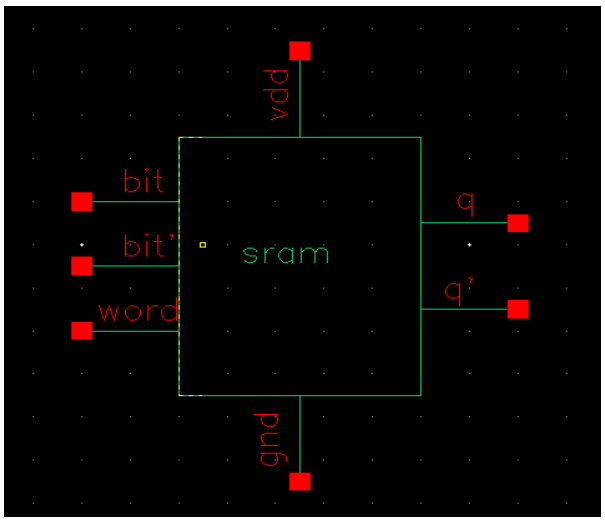
I have designed the volatile memory, i.e., SRAM and its schematic is as shown in figure below:



Schematic of SRAM

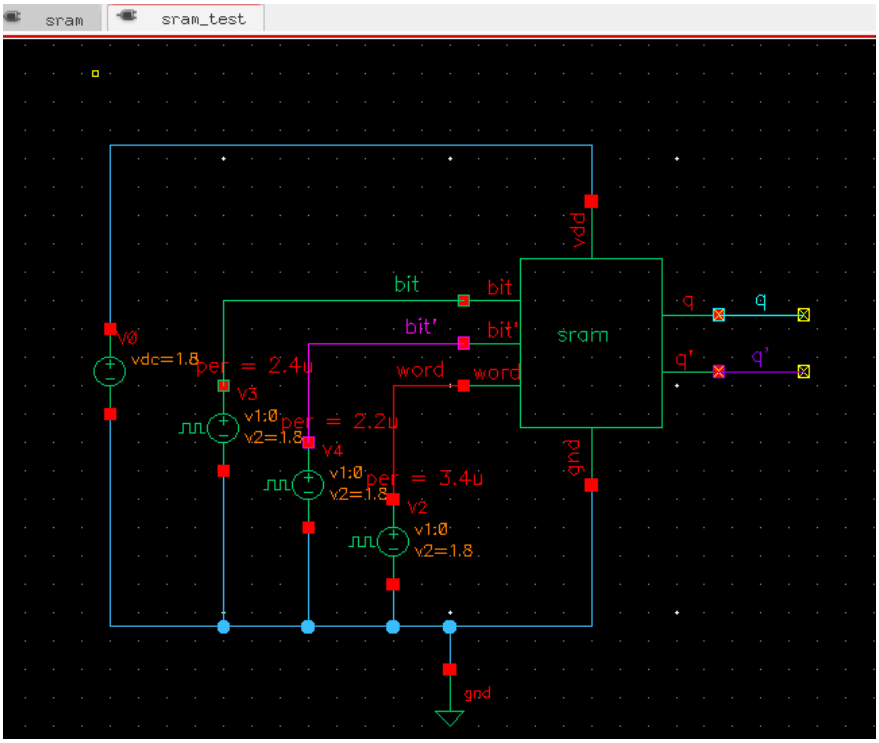
As it contains 6 transistors, it is called 6T-SRAM.

Instead of applying power sources, I have attached pins in the schematic to create a symbol for it and then using it to test the working of the SRAM. So the symbol is created and shown below:



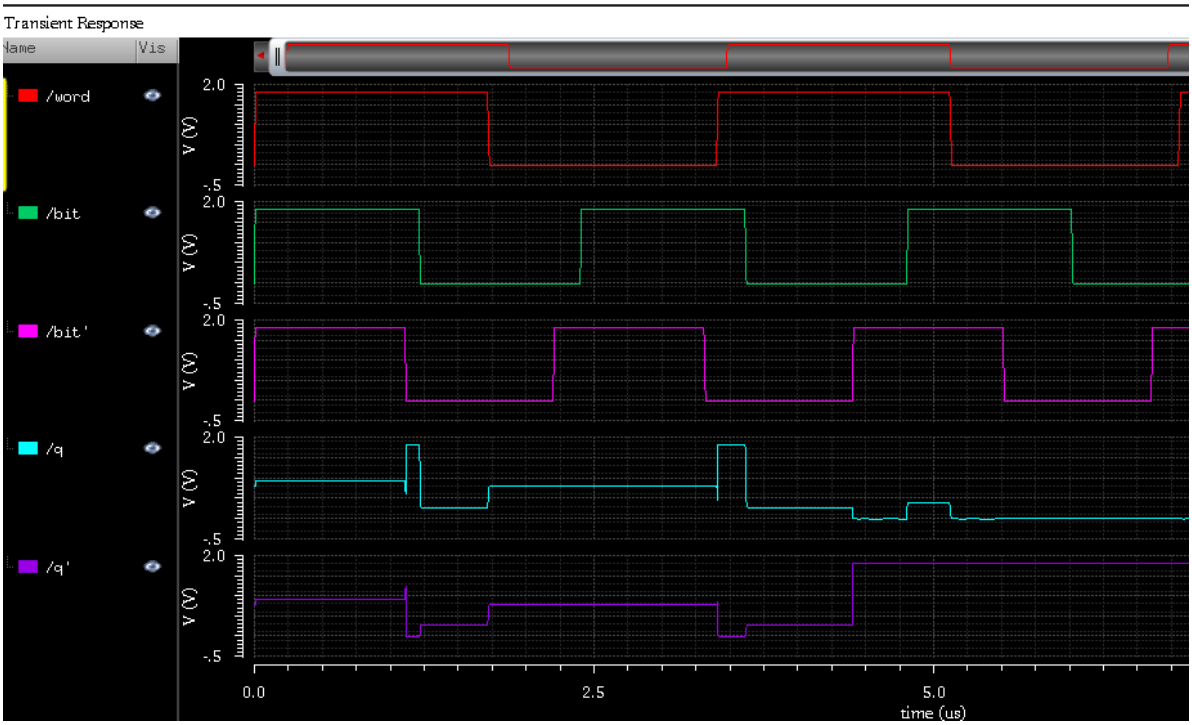
Symbol of SRAM

Now, we have to test our symbol, so we add it in a new schematic, apply power sources and make the connections properly.



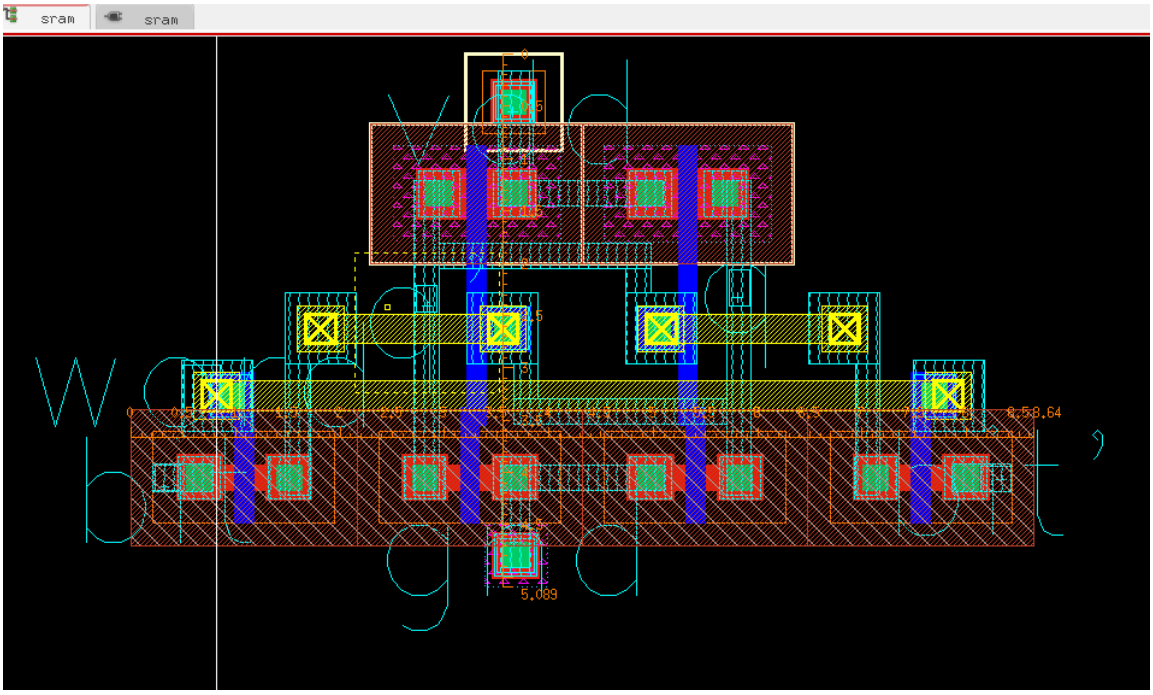
Circuit Diagram of SRAM with symbol

The results obtained from the SRAM symbol are shown below, and it is verified that our SRAM is working properly.



Inputs – word (red), bit (green) & bit' (pink). Outputs – q (blue) & q' (purple)

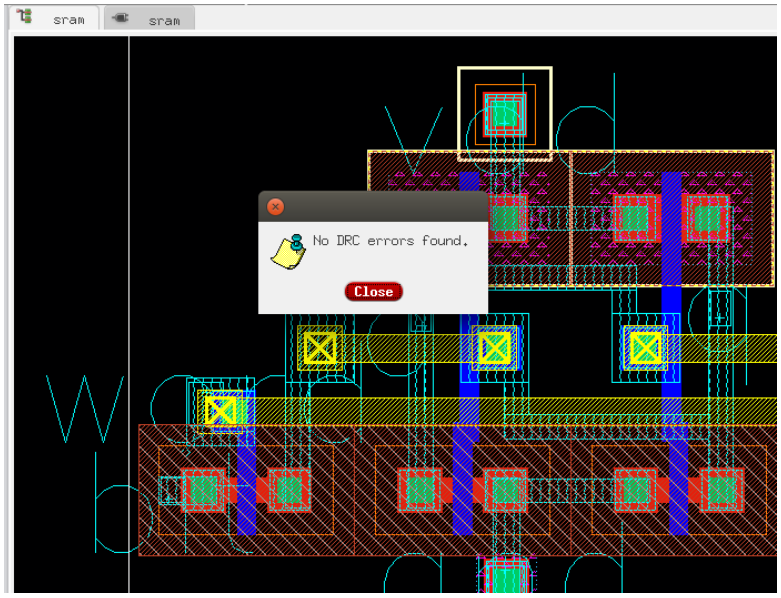
Now we will make the layout for our SRAM, and draw it in accordance with the lambda rules. The layout formed is shown below:



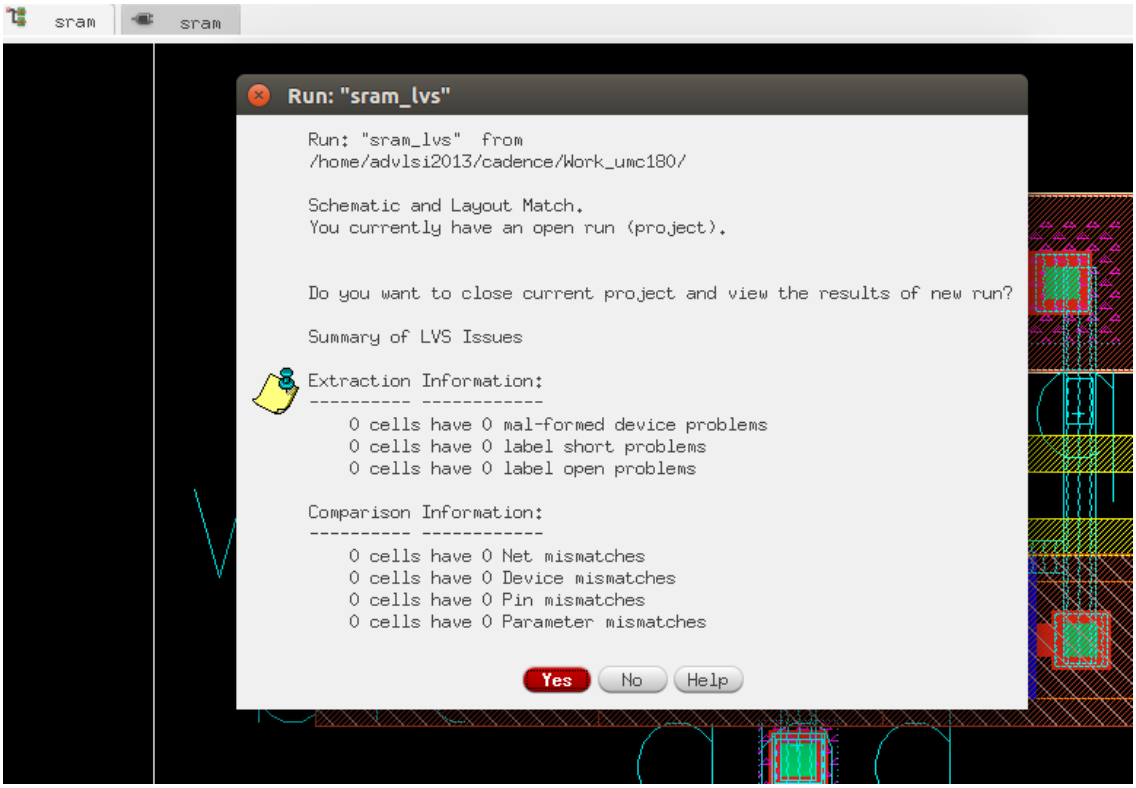
Layout of SRAM

The area of the layout is minimized according to the lambda rules and it is found out that the minimum area required to built a multiplier is 8.64um x 5.089um = 123212um^2, which is equal to 43.97λ^2. (λ=0.06um and can be verified in cadence).

The results of the DRC test and LVS test were successful for the layout formed, i.e., there were no errors in the layout and also it is now matched with the schematic which we had drawn earlier.

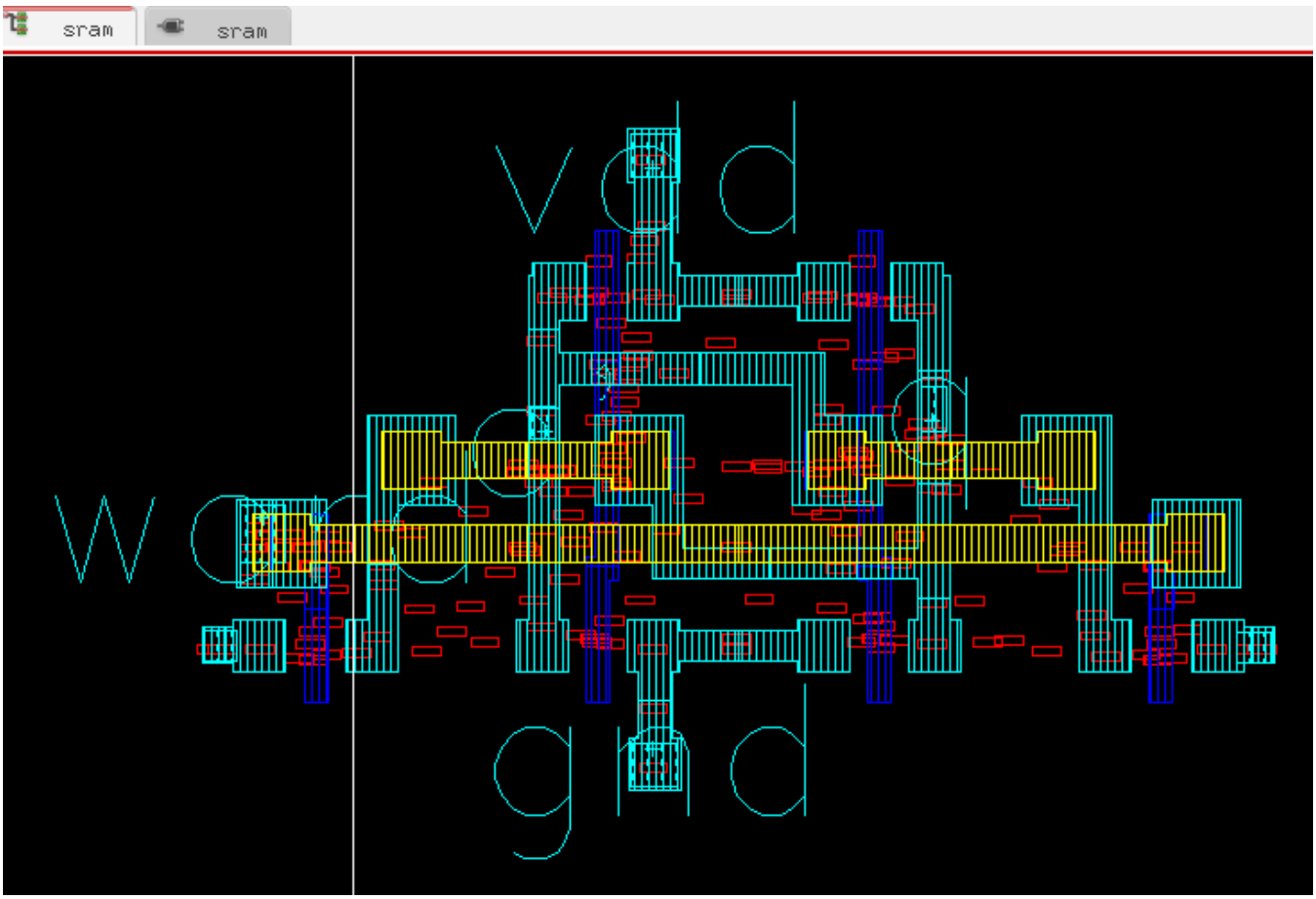


Result of DRC test (successful)

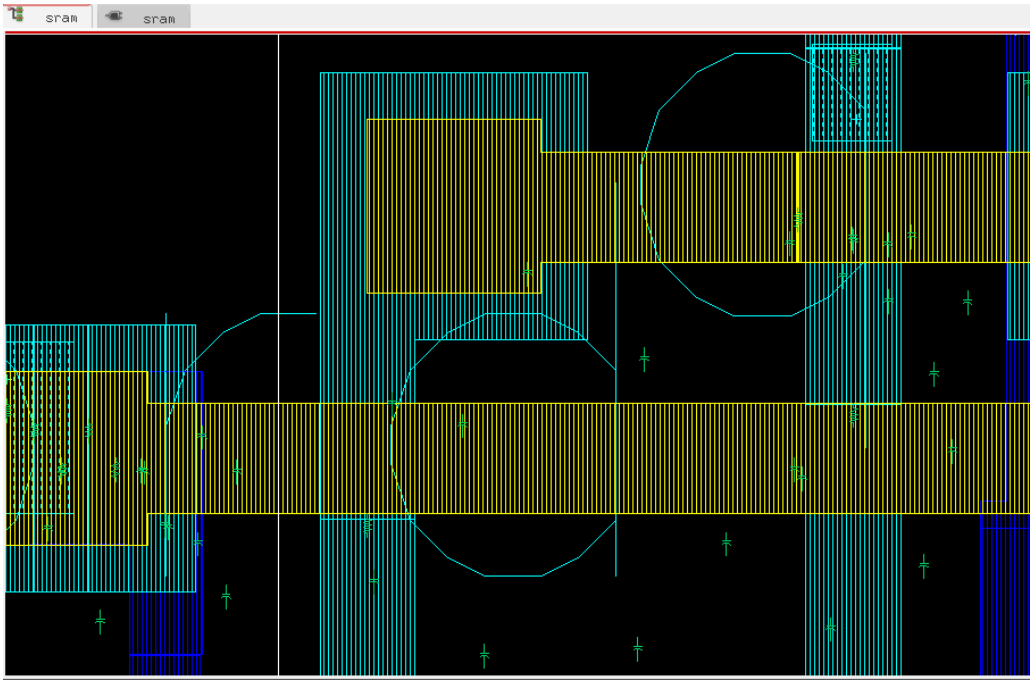


Result of LVS test (successful)

Now, the RCX test is run to generate the extracted view of the layout, which shows the presence of various parasitic capacitances and resistances and it is shown below:

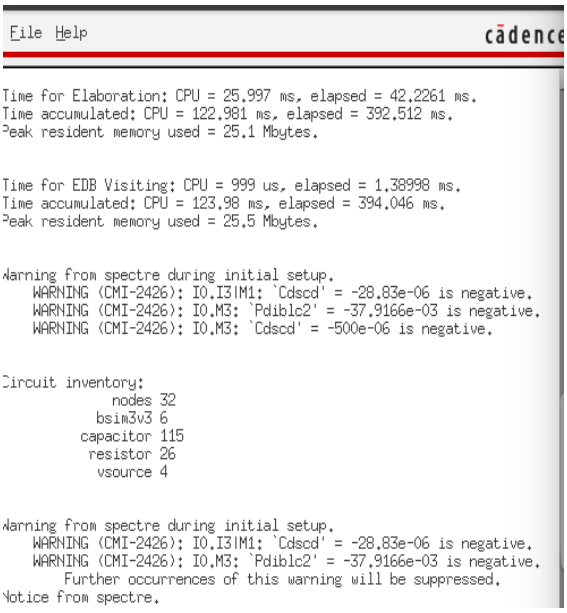


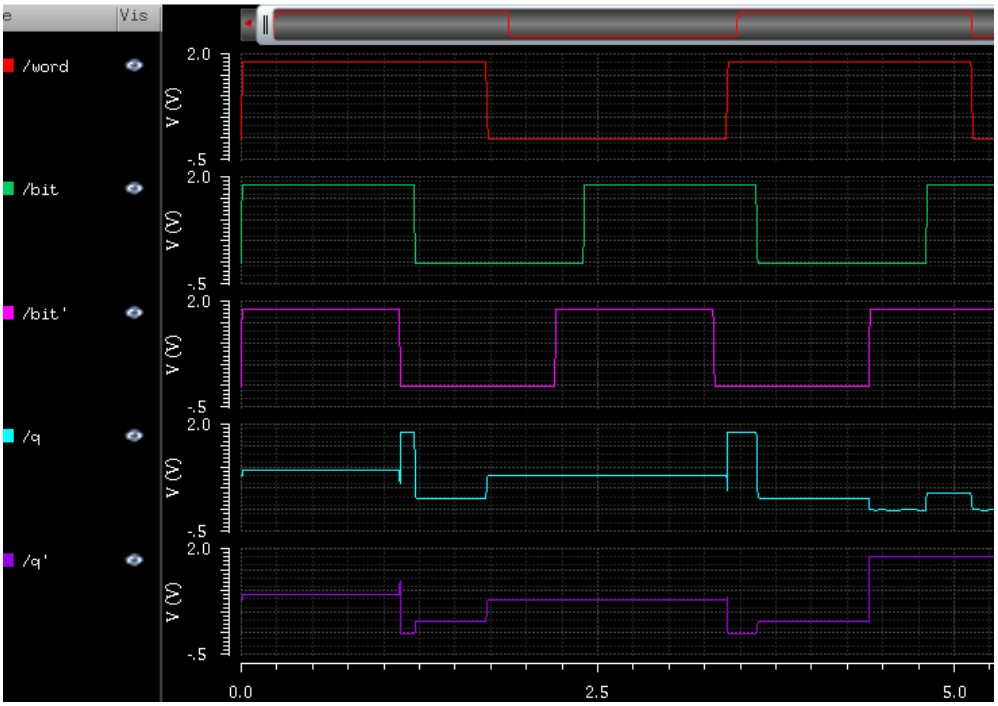
Extracted view of the layout with parasitic capacitances and resistances



When this extracted view is zoomed, we can clearly see in the above figure, the parasitic capacitances and parasitic resistances in metals and poly

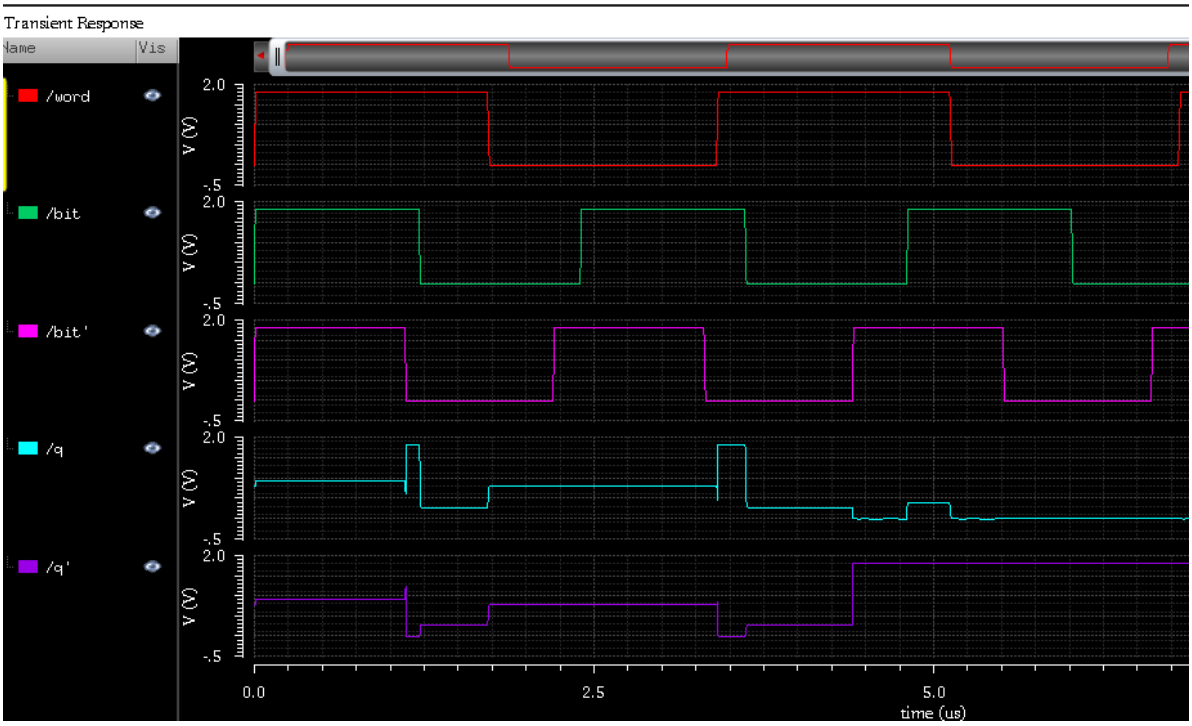
We can now ensure that our layout drawn also gives correct results. So, changing the hierarchy of our symbol from schematic to layout, the following results were obtained and we can see that the output is coming correctly from the transient analysis of the circuit. Also we can see the presence of multiple resistances, capacitances, and nodes in the results, which were not in the schematic.





Inputs – a (red) & b (green). Output – y (purple)

Now, we compare the results of the original schematic with that of the results from layout hierarchy. Again transient analysis is done and results are as shown:



Inputs – word (red), bit (green) & bit' (pink). Outputs – q (blue) & q' (purple)

So, the comparison between the results of the layout and the schematic of the SRAM are approximately same. There are very little distortions in the output waveforms of the layout which is not in the case of schematic. So, the layout and the schematic are successfully verified theoretically also. Thus our SRAM design is successfully completed and the following conclusions are made.

No. of transistors used: 6 (4NMOS + 2PMOS).
Area consumed by layout: 43.97um^2.
Power consumption: 87.8uW. (calculated by doing DC analysis).