Intro to VLSI

Lab Task 2 – 4:1 mux design

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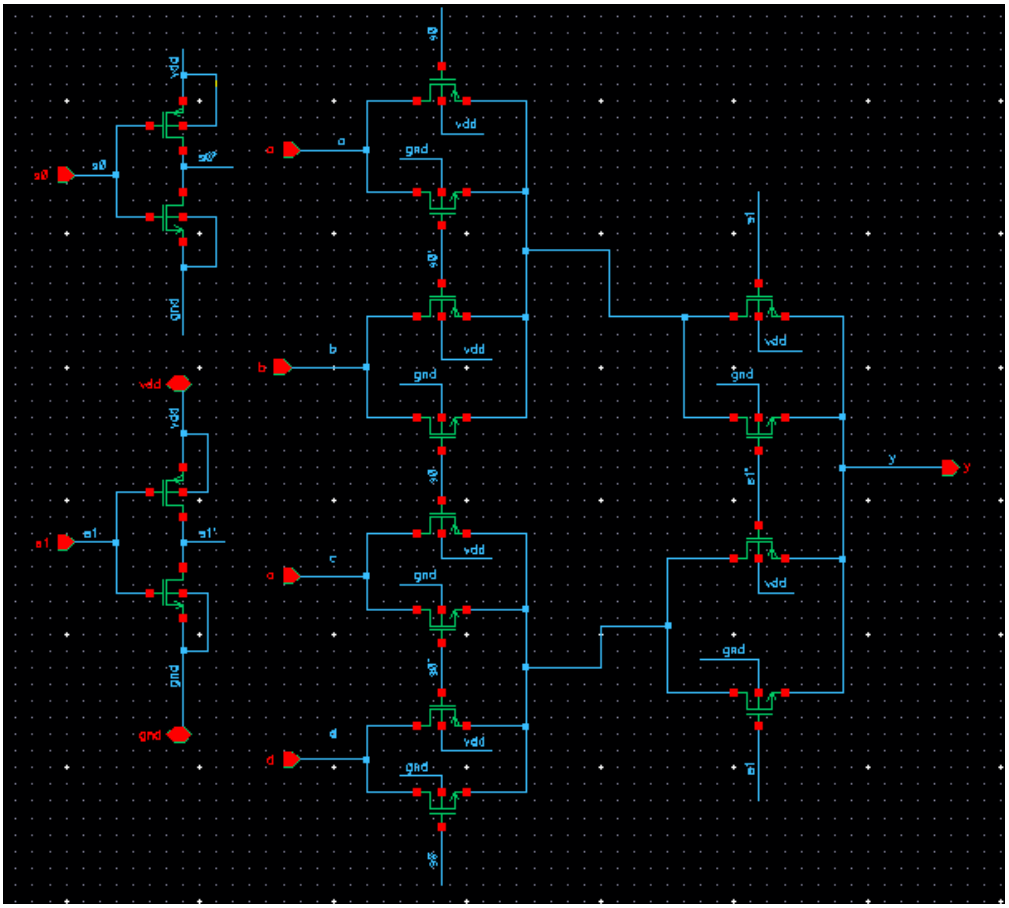
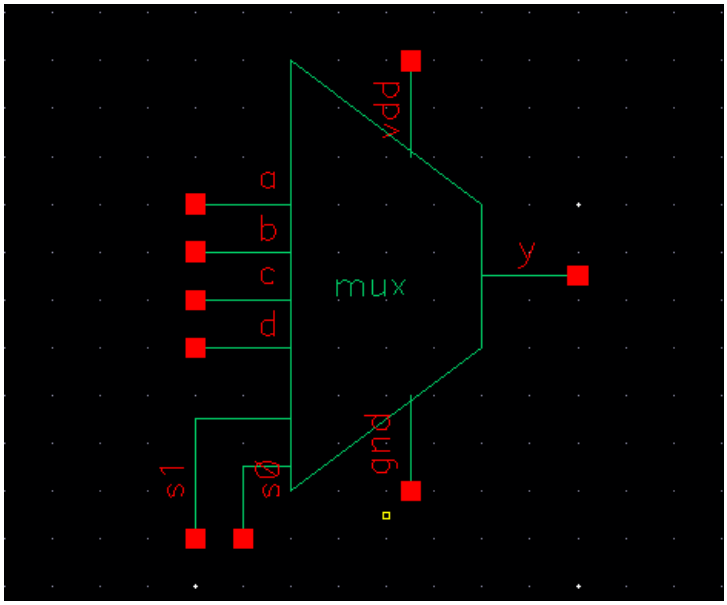
(20171049)

I have designed the 4 input Mux (4:1 mux) schematic using PTL logic which is as shown in figure below:



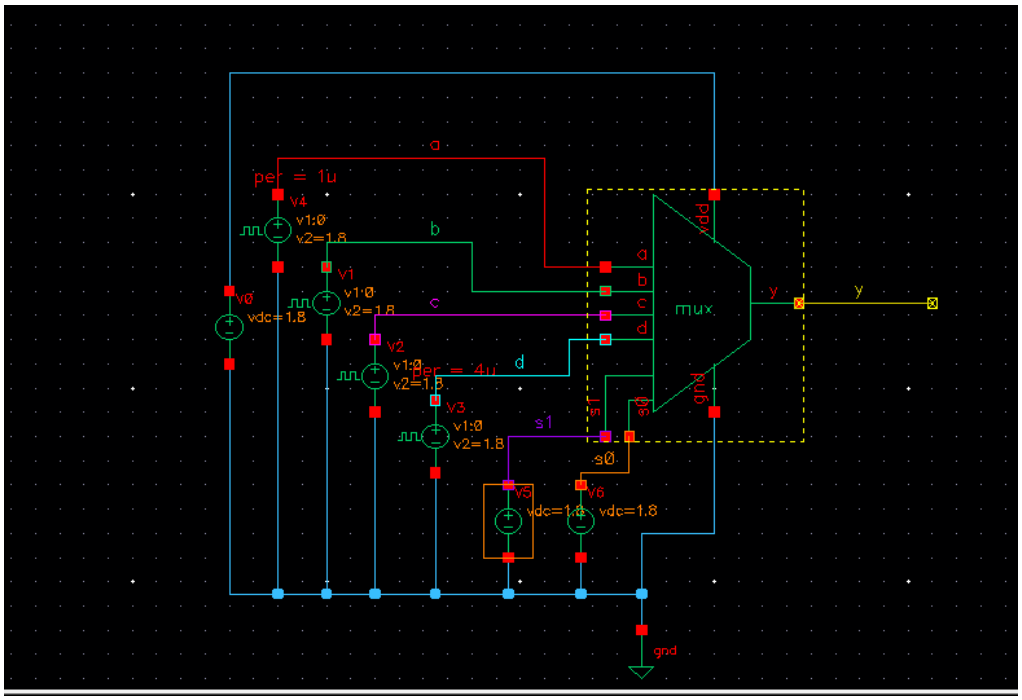
Schematic of Mux

Instead of applying power sources, I have attached pins in the schematic to create a symbol for it and then using it to test the working of the Mux. So the symbol is created and shown below:



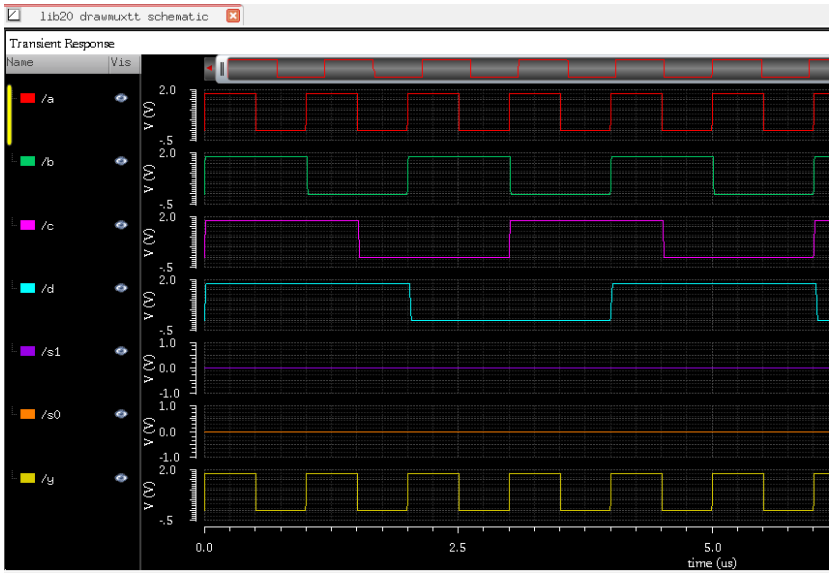
Symbol of Mux

Now, we have to test our symbol, so we add it in a new schematic, apply power sources and make the connections properly.

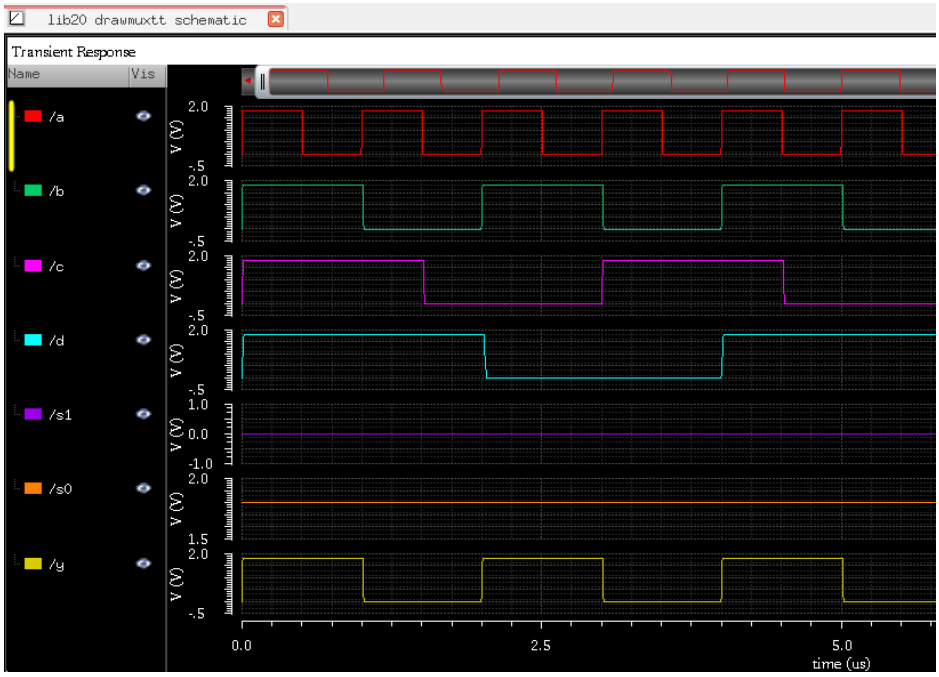


Circuit Diagram of Mux with symbol

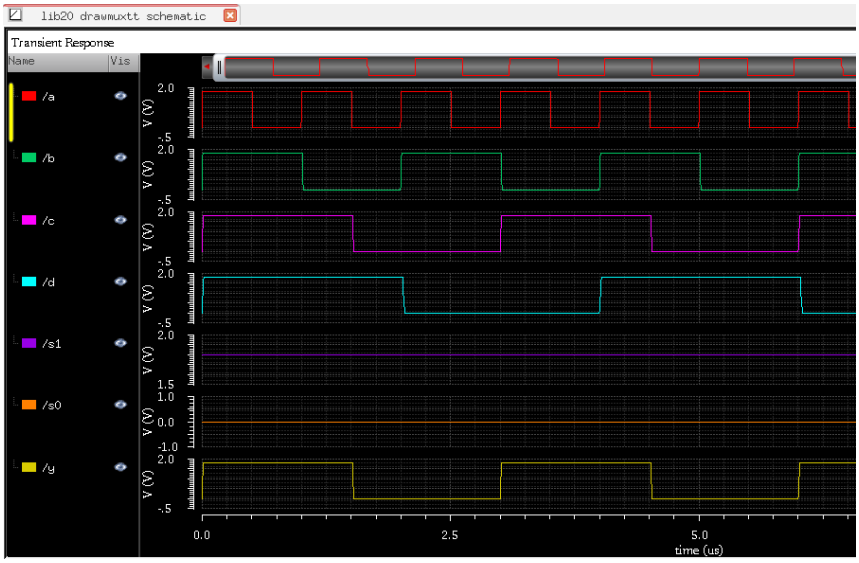
The results obtained from the Mux symbol are shown below, and it is verified that our Mux is working properly. All the possible 4 cases for the select lines are shown below:



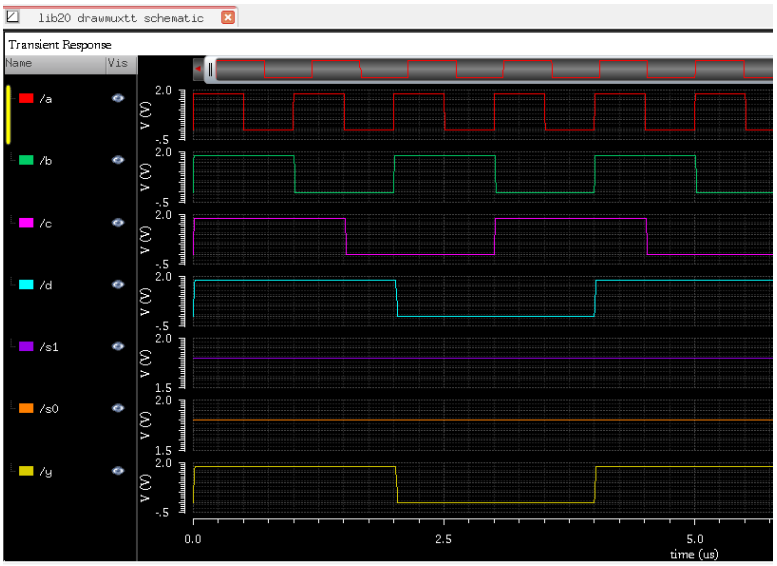
When inputs are s1,s0 = 0,0 , output y=a.



When inputs are s1,s0 = 0,1 , output y=b.



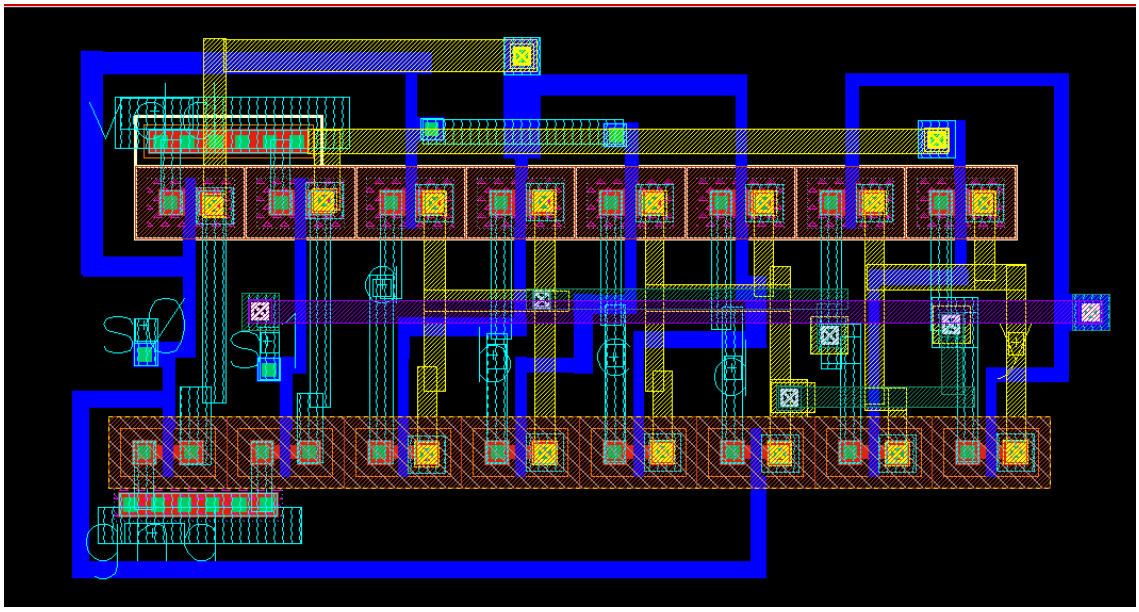
When inputs are s1,s0 = 1,0 , output y=c.



When inputs are s1,s0 = 1,1 , output y=d.

Inputs – a (red) , b (green) , c (pink) , d (blue) , s1 (purple) , s0 (orange). Output – y (yellow)

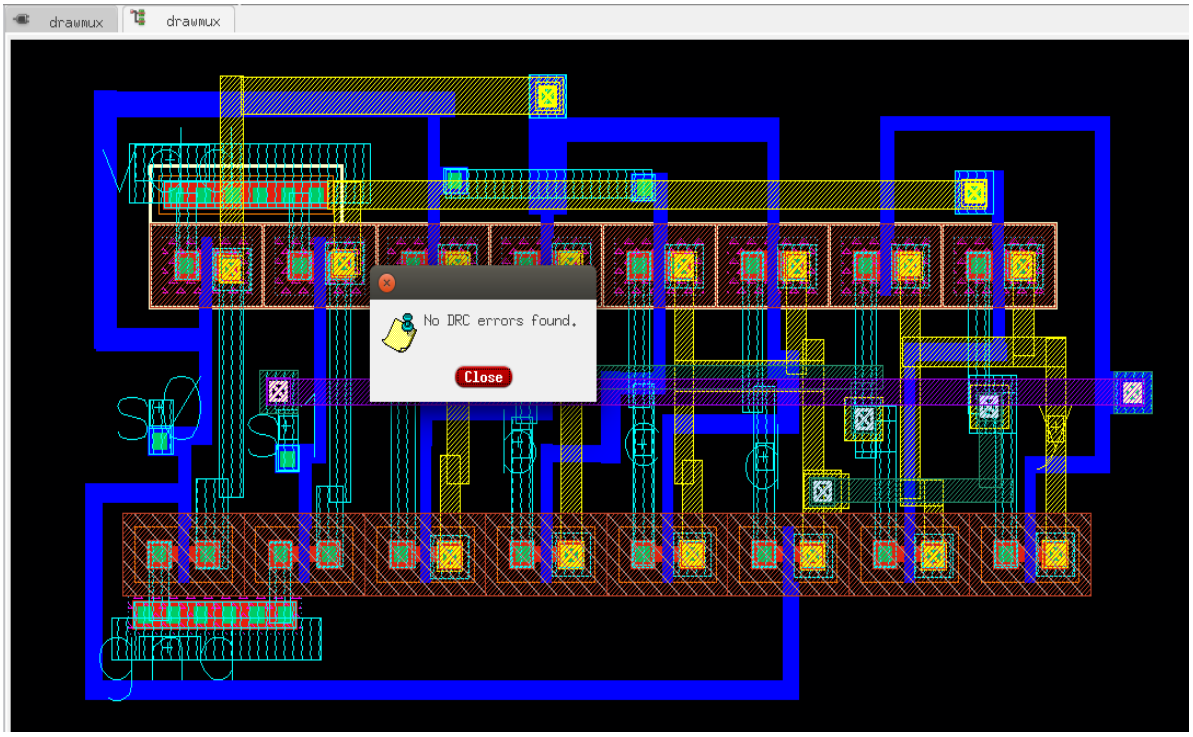
Now we will make the layout for our Mux, and draw it in accordance with the lambda rules. The layout formed is shown below:



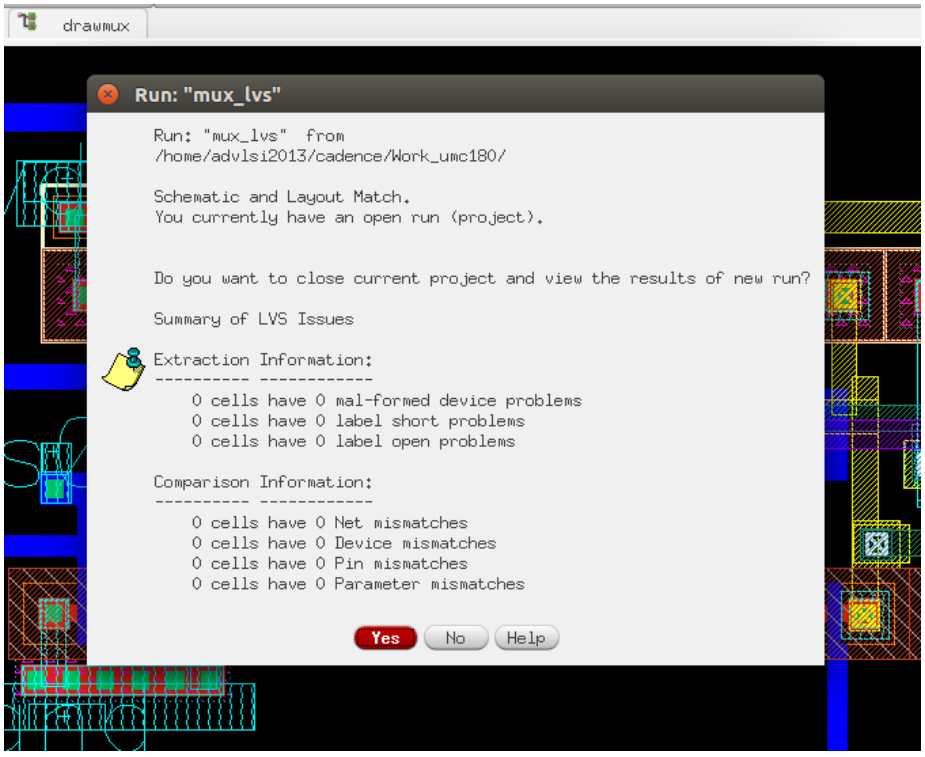
Layout of Mux

We have minimized the area and it is found that the minimized area is 9.883um x 18.879um = 186.581um^2.

The results of the DRC test and LVS test were successful for the layout formed, i.e., there were no errors in the layout and also it is now matched with the schematic which we had drawn earlier.



Result of DRC test (successful)



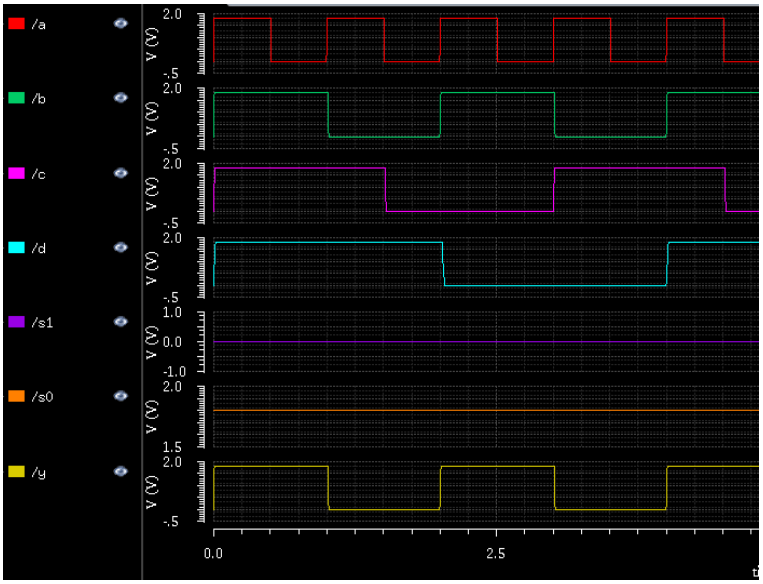
Result of LVS test (successful)

Now, the RCX test is run to generate the extracted view of the layout, which shows the presence of various parasitic capacitances and resistances and it is shown below:

Extracted view of the layout with parasitic capacitances and resistances

We can now ensure that our layout drawn also gives correct results. So, changing the hierarchy of our symbol from schematic to layout, the following results were obtained and we can see that the output is coming correctly from the transient analysis of the circuit. Also we can see the presence of multiple resistances, capacitances, and nodes in the results, which were not in the schematic.

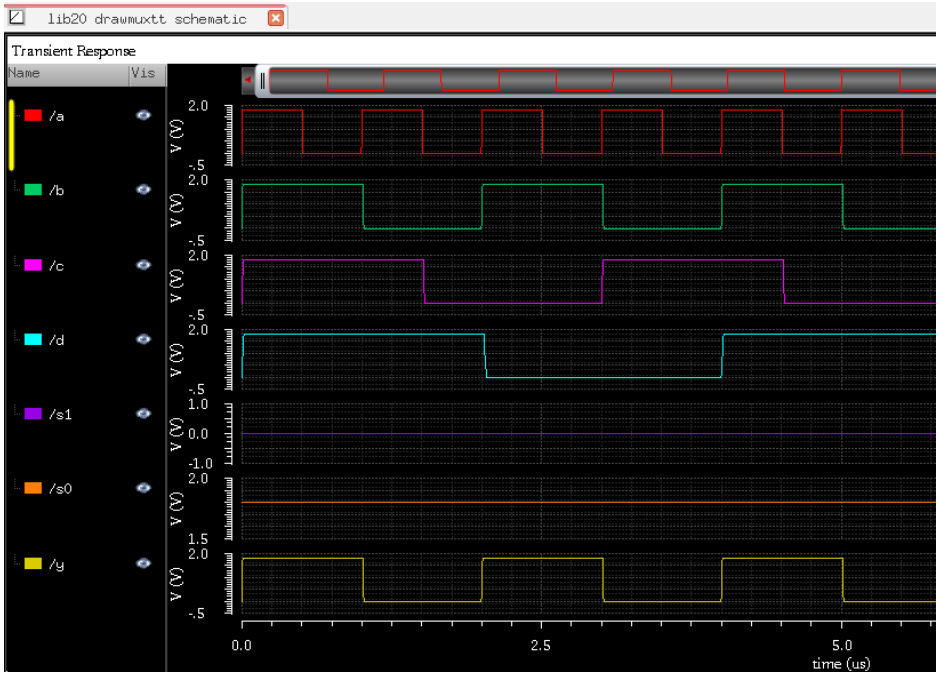
```
Circuit inventory:
              nodes 106
            bsim3v3 16
           resistor 96
            vsource 5


Warning from spectre during initial setup.
    WARNING (CMI-2426): I8.M30: `Cdscd' = -28.83e-06 is negative.
    WARNING (CMI-2426): I8.M22: `Pdiblc2' = -37.9166e-03 is negative.
        Further occurrences of this warning will be suppressed.
Notice from spectre.
    44 warnings suppressed.


Time for parsing: CPU = 1.999 ms, elapsed = 4.85015 ms.
Time accumulated: CPU = 134.978 ms, elapsed = 216.19 ms.
Peak resident memory used = 26.3 Mbytes.

Entering remote command mode using MPSC service (spectre, ipi, v0.0,

Warning from spectre.
    WARNING (SPECTRE-16707): Only tran supports psfxl format, result
```



Inputs – a (red) , b (green) , c (pink) , d (blue) , s1=0 (purple) , s0=1.8V (orange). Output – y (yellow) = b.

Now, we compare the results of the original schematic with that of the results from layout hierarchy. Again transient analysis is done and results are as shown:

```
Time for Elaboration: CPU = 25.996 ms, elapsed = 27.106 ms.
Time accumulated: CPU = 132.979 ms, elapsed = 211.446 ms.
Peak resident memory used = 25.1 Mbytes.


Time for EDB Visiting: CPU = 0 s, elapsed = 627.041 us.
Time accumulated: CPU = 132.979 ms, elapsed = 212.212 ms.
Peak resident memory used = 25.4 Mbytes.


Warning from spectre during initial setup.
    WARNING (CMI-2426): IO.M12: `Cdscd' = -28.83e-06 is negative.
    WARNING (CMI-2426): IO.M6: `Pdiblc2' = -37.9166e-03 is negative.
    WARNING (CMI-2426): IO.M6: `Cdscd' = -500e-06 is negative.


Circuit inventory:
              nodes 12
            bsim3v3 16
            vsource 7


Warning from spectre during initial setup.
    WARNING (CMI-2426): IO.M12: `Cdscd' = -28.83e-06 is negative.
    WARNING (CMI-2426): IO.M6: `Pdiblc2' = -37.9166e-03 is negative.
        Further occurrences of this warning will be suppressed.
Notice from spectre.
    44 warnings suppressed.


Time for parsing: CPU = 2 ms, elapsed = 6.99401 ms.
Time accumulated: CPU = 135.979 ms, elapsed = 219.345 ms.
Peak resident memory used = 26.1 Mbytes.

Entering remote command mode using MPSC service (spectre, ipi, v0.0,

Warning from spectre.
    WARNING (SPECTRE-16707): Only tran supports psfxl format, result
```



Inputs – a (red) , b (green) , c (pink) , d (blue) , s1=0 (purple) , s0=1.8V (orange). Output – y (yellow) = b.

So, the comparison between the results of the layout and the schematic of the Mux are approximately same. There are very little distortions in the output waveforms of the layout which is not in the case of schematic. So, the layout and the schematic are successfully verified theoretically also. Thus our Mux design is successfully completed. Also the area of the layout was minimized and was found to be 186.581 um^2.