Intro to VLSI

Lab Task 5 – D latch

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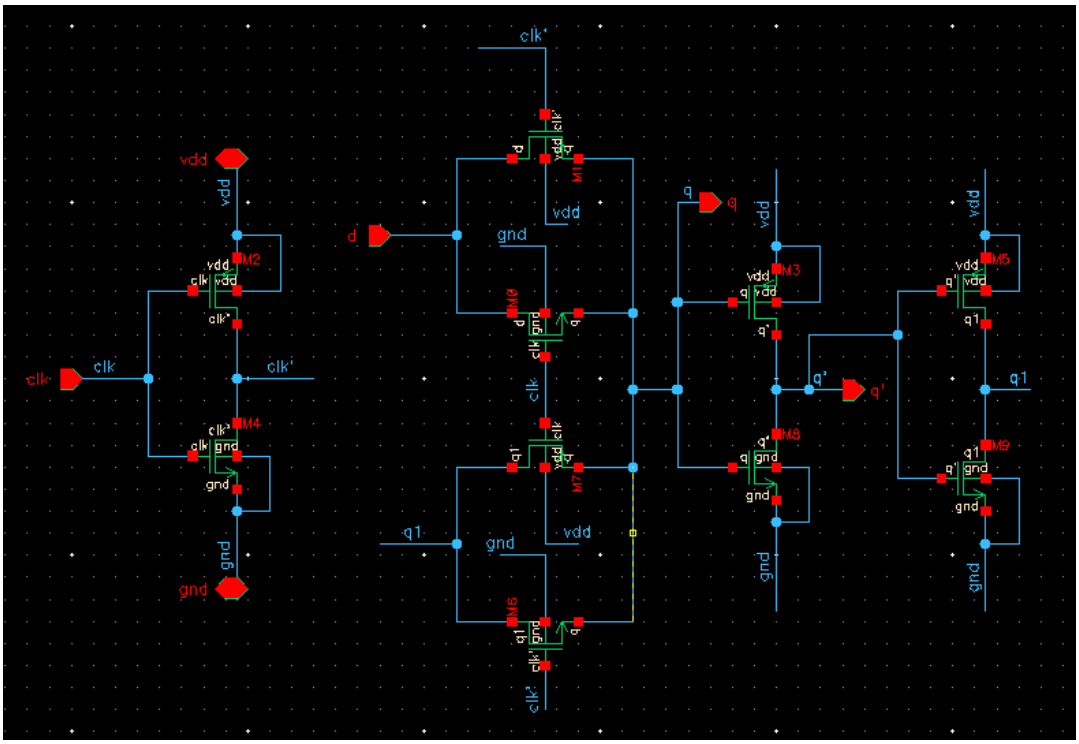
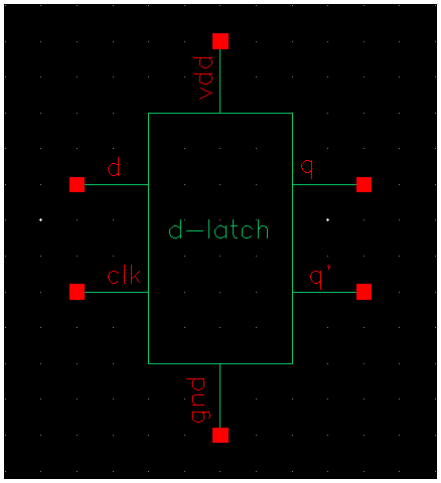
(20171049)

I have designed the D latch schematic which is as shown in figure below:



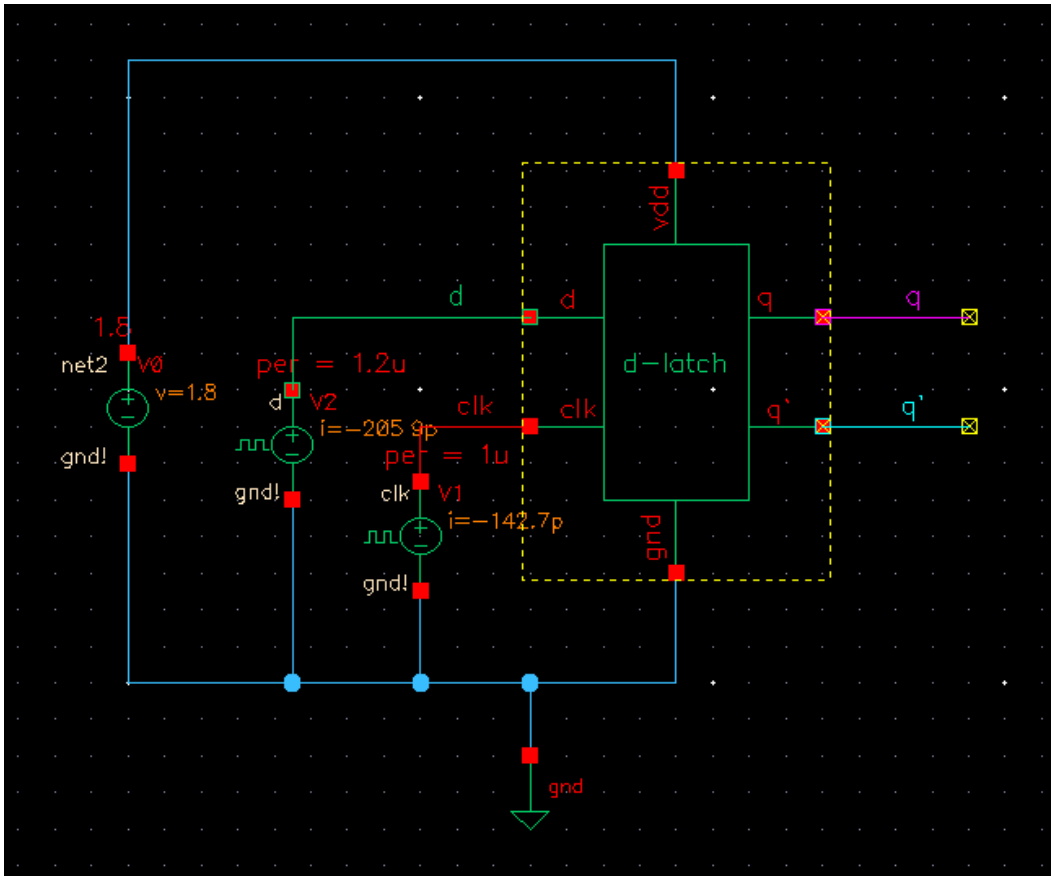
Schematic of D latch

Instead of applying power sources, I have attached pins in the schematic to create a symbol for it and then using it to test the working of the D latch. So the symbol is created and shown below:



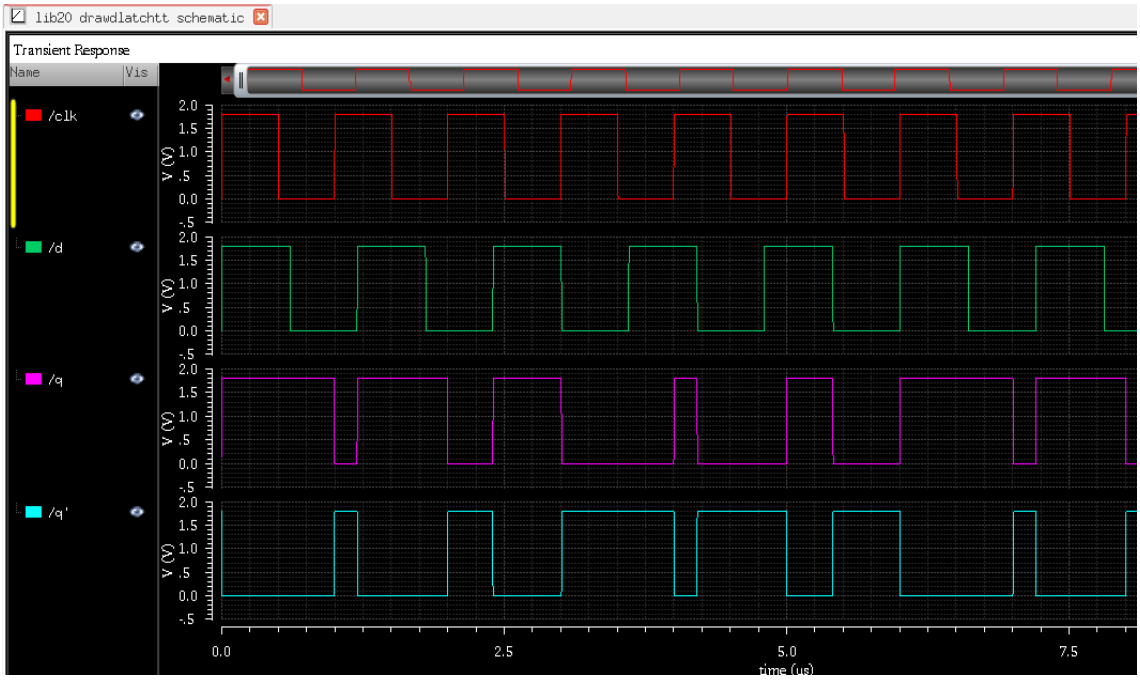
Symbol of D latch

Now, we have to test our symbol, so we add it in a new schematic, apply power sources and make the connections properly.



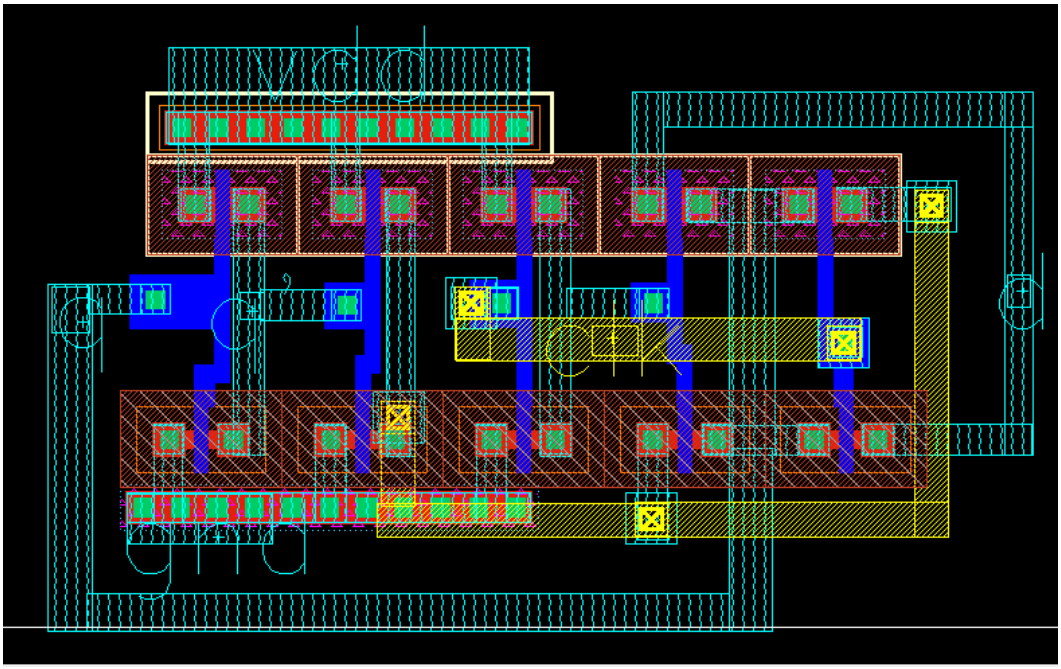
Circuit Diagram of D latch with symbol

The results obtained from the D latch symbol are shown below, and it is verified that our D latch is working properly.



Inputs – clk (red) & d (green). Outputs – q (purple) & q’ (blue)

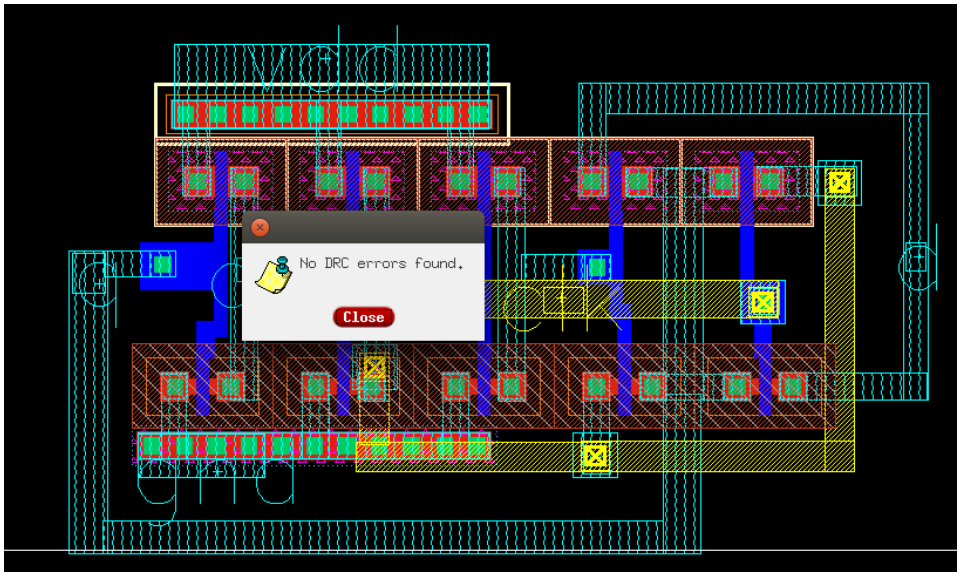
Now we will make the layout for our D latch, and draw it in accordance with the lambda rules. The layout formed is shown below:



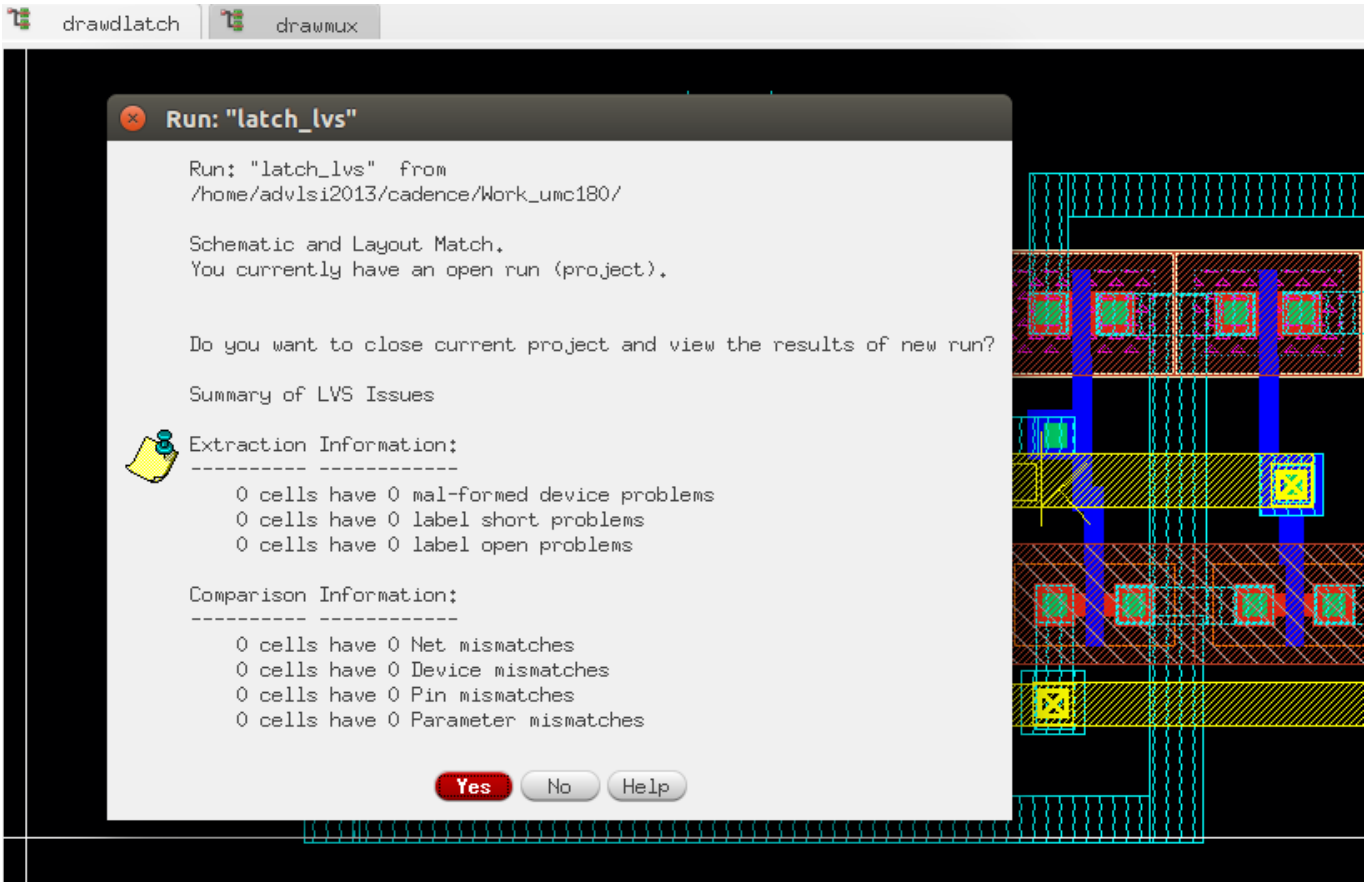
Layout of D latch

We have minimized the area and it is found that the minimized area is 7.816um x 13.206um = 103.206um^2.

The results of the DRC test and LVS test were successful for the layout formed, i.e., there were no errors in the layout and also it is now matched with the schematic which we had drawn earlier.

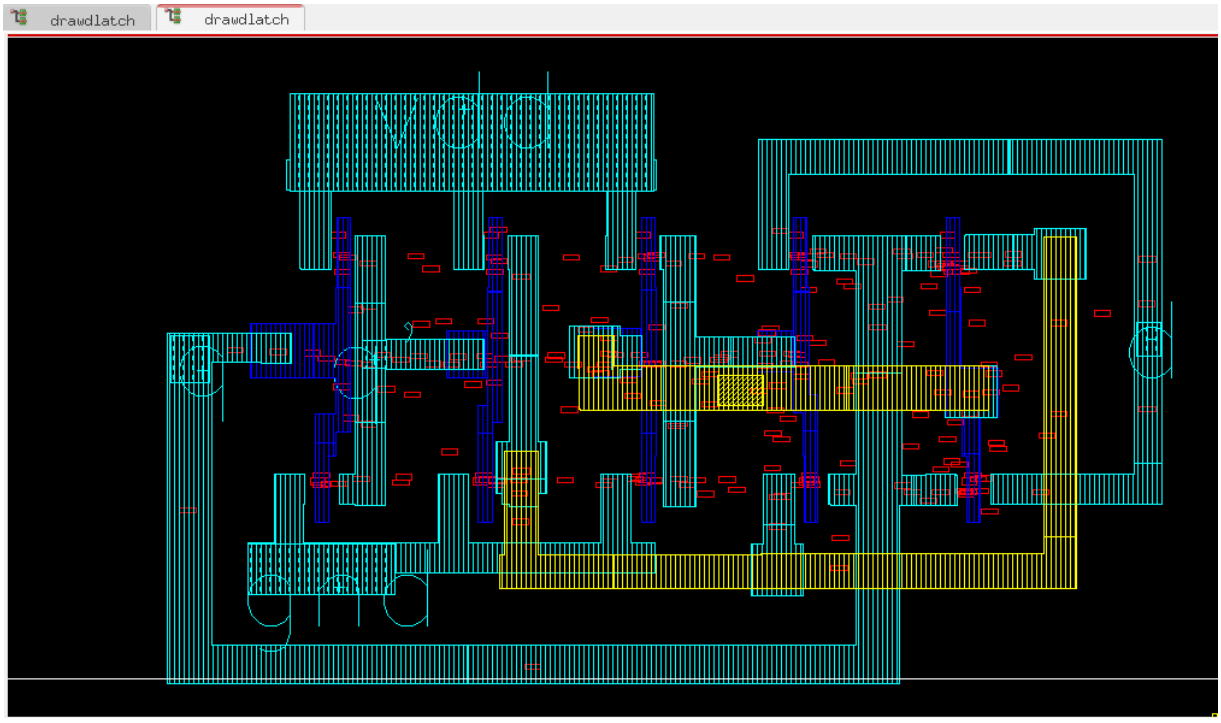


Result of DRC test (successful)



Result of LVS test (successful)

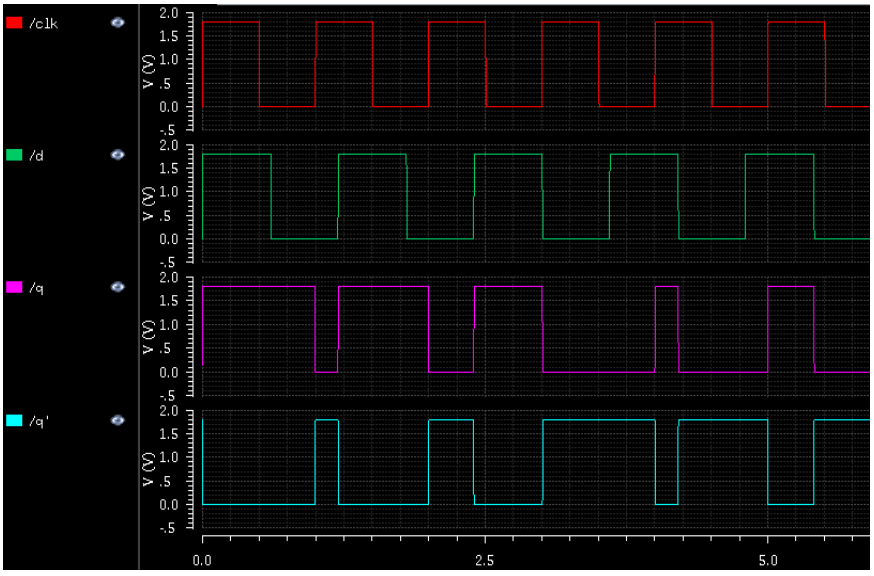
Now, the RCX test is run to generate the extracted view of the layout, which shows the presence of various parasitic capacitances and resistances and it is shown below:



Extracted view of the layout with parasitic capacitances and resistances

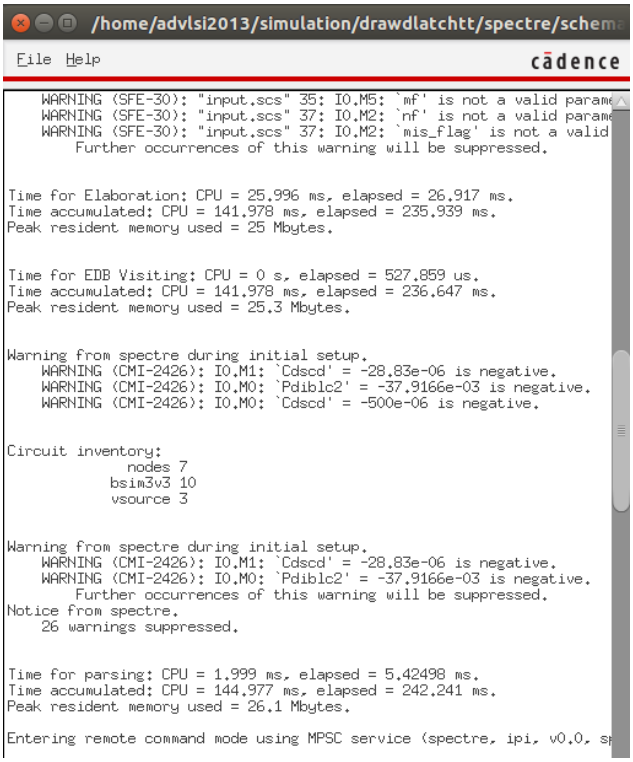
We can now ensure that our layout drawn also gives correct results. So, changing the hierarchy of our symbol from schematic to layout, the following results were obtained and we can see that the output is coming correctly from the transient analysis of the circuit. Also we can see the presence of multiple resistances, capacitances, and nodes in the results, which were not in the schematic.

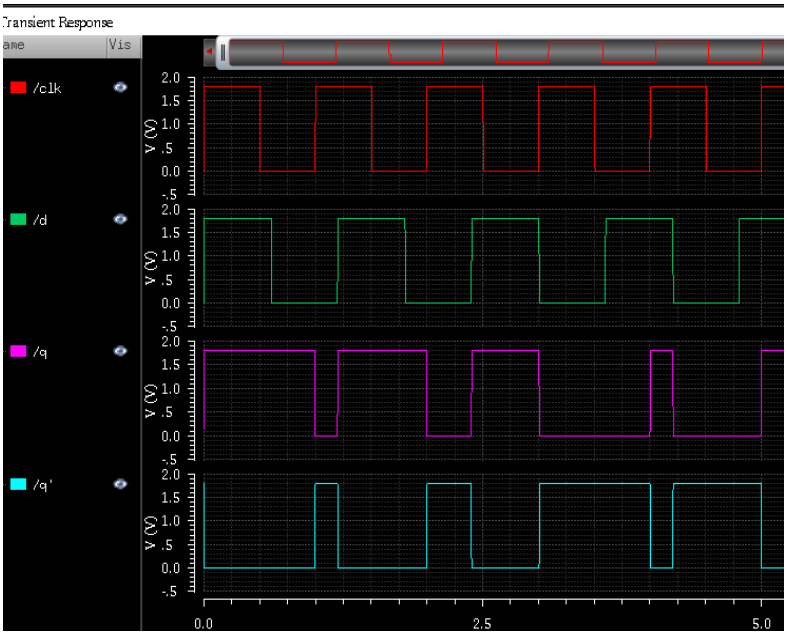
```
Warning from spectre in `latch_av_extracted':`I1', during hierarchy fla
    WARNING (SFE-30): "input.scs" 331: I1.M12: `nf' is not a valid para
    WARNING (SFE-30): "input.scs" 331: I1.M12: `mis_flag' is not a vali
    WARNING (SFE-30): "input.scs" 331: I1.M12: `mf' is not a valid para
    WARNING (SFE-30): "input.scs" 334: I1.M1: `nf' is not a valid paran
    WARNING (SFE-30): "input.scs" 334: I1.M1: `mis_flag' is not a valid
        Further occurrences of this warning will be suppressed.


Time for Elaboration: CPU = 26.996 ms, elapsed = 27.3709 ms.
Time accumulated: CPU = 151.976 ms, elapsed = 214.192 ms.
Peak resident memory used = 25.2 Mbytes.


Time for EDB Visiting: CPU = 2 ms, elapsed = 1.83797 ms.
Time accumulated: CPU = 153.976 ms, elapsed = 216.214 ms.
Peak resident memory used = 25.6 Mbytes.


Warning from spectre during initial setup.
    WARNING (CMI-2426): I1.M9: `Cdscd' = -28.83e-06 is negative.
    WARNING (CMI-2426): I1.M10: `Pdiblc2' = -37.9166e-03 is negative.
    WARNING (CMI-2426): I1.M10: `Cdscd' = -500e-06 is negative.


Circuit inventory:
              nodes 62
          bsim3v3 10
        capacitor 240
         resistor 55
          vsource 3


Warning from spectre during initial setup.
    WARNING (CMI-2426): I1.M9: `Cdscd' = -28.83e-06 is negative.
    WARNING (CMI-2426): I1.M10: `Pdiblc2' = -37.9166e-03 is negative.
        Further occurrences of this warning will be suppressed.
Notice from spectre.
    26 warnings suppressed.
```



Inputs – clk (red) & d (green). Output – q (purple) & q’ (blue)

Now, we compare the results of the original schematic with that of the results from layout hierarchy. Again transient analysis is done and results are as shown:





Inputs – clk (red) & d (green). Output – q (purple) & q' (blue)

So, the comparison between the results of the layout and the schematic of the D latch are approximately same. There are very little distortions in the output waveforms of the layout which is not in the case of schematic. So, the layout and the schematic are successfully verified theoretically also. Thus our D latch design is successfully completed. Also the area of the layout was minimized and was found to be 103.218 um^2.