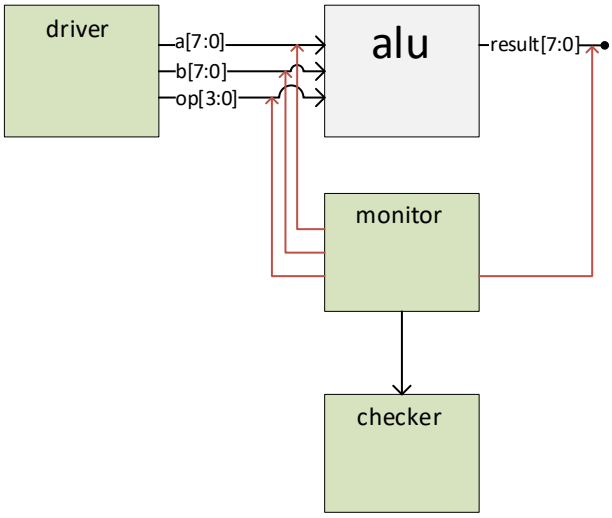
Advanced Logic Design – Lab 2

Question 1 [100 points]

a. [**50 points**] Design an ALU module in System-Verilog (alu.sv) according to the following interface table. Start by drawing the schematic of your design.

Port	Direction	Width	Description
a	In	8	Signed Operand
b	In	8	Signed Operand
op	In	4	ALU Operation 0001 – Bitwise AND 0010 – Bitwise OR 0011 – Logical OR 1001 – Two's complement of **A** 1011 – Logical shift 1-bit right of **A** 1100 – Arithmetic shift 1-bit right of **A** 1101 – Rotate 1-bit left of **B** Others non defined operation – NOP (result=0)
result	Out	8	Signed Operation Result

b. [**50 points**] Write a test-bench (**alu_tb.sv**) that verify the ALU functionality according to the following guidelines:



- Separate the test elements (driver, monitor, checker) functionality in the code.
- For the driver, define the following:
  - Void function that randomizes the 3 inputs.
  - Task that uses the void function above to drive the inputs and give some delay.
- For the checker:
  - Function that calculates the expected *result* value (returns logic [7:0])
  - Try **not** reuse the design code, as much as possible.
  - Use the $error system function for error alert.
- The monitor will detect events on the i/f and will call the checker functions.
- Insert a fault in your ALU, run the test and look for the checker error message. Explain the fault insertion you did and export the waveform image of it. (Don't forget to remove it and submit a working ALU)

Submit:

- SV files: alu.sv, alu_tb.sv
- ALU block diagram
- Waveforms images.