Advanced Logic Design – Lab Number 1

Part I (30 points)

1. Briefly describe:
   a. The term HDL
   b. The main differences between HDL and software languages like C, Python etc.
   c. The main differences between ASIC and FPGA.

Part II (70 points)

2. RTL Simulation
   Open a new ModelSim project, add and compile the Verilog files: tb.sv and safe_box_key.sv , run the simulation for 30ns.

   a. Export the waveform image that shows the *key* and *valid* signals behavior. (Change the format of the *key* signal to hexadecimal.)

3. Gate level simulation
   Replace the safe_box_key.sv with the gate level files: safe_box_key_gl.sv and stdcells_lib.sv, compile and run the simulation until you identify a glitch.

   a. Measure with the cursors how much time it takes to non-glitched *valid* signal to de-assert. Export the waveform image.

   b. Find a glitch on the *valid* signal. Measure the glitch width with the cursors and export the waveform image.

   c. Explain the reason for the glitch.

   d. The U4 module has 2 inputs and 1 output. Load them to the waves and list down its truth table. Which logic gate U4 represents? Export the waveform image.

e. Write a do file that do the following steps:
    - Restart the simulation.
    - Add the *key* and *valid* signals to the wave.
    - Run the simulation for 30ns while after 10ns from the beginning of the simulation the *n3* signal is forced to '1' for 5ns only.