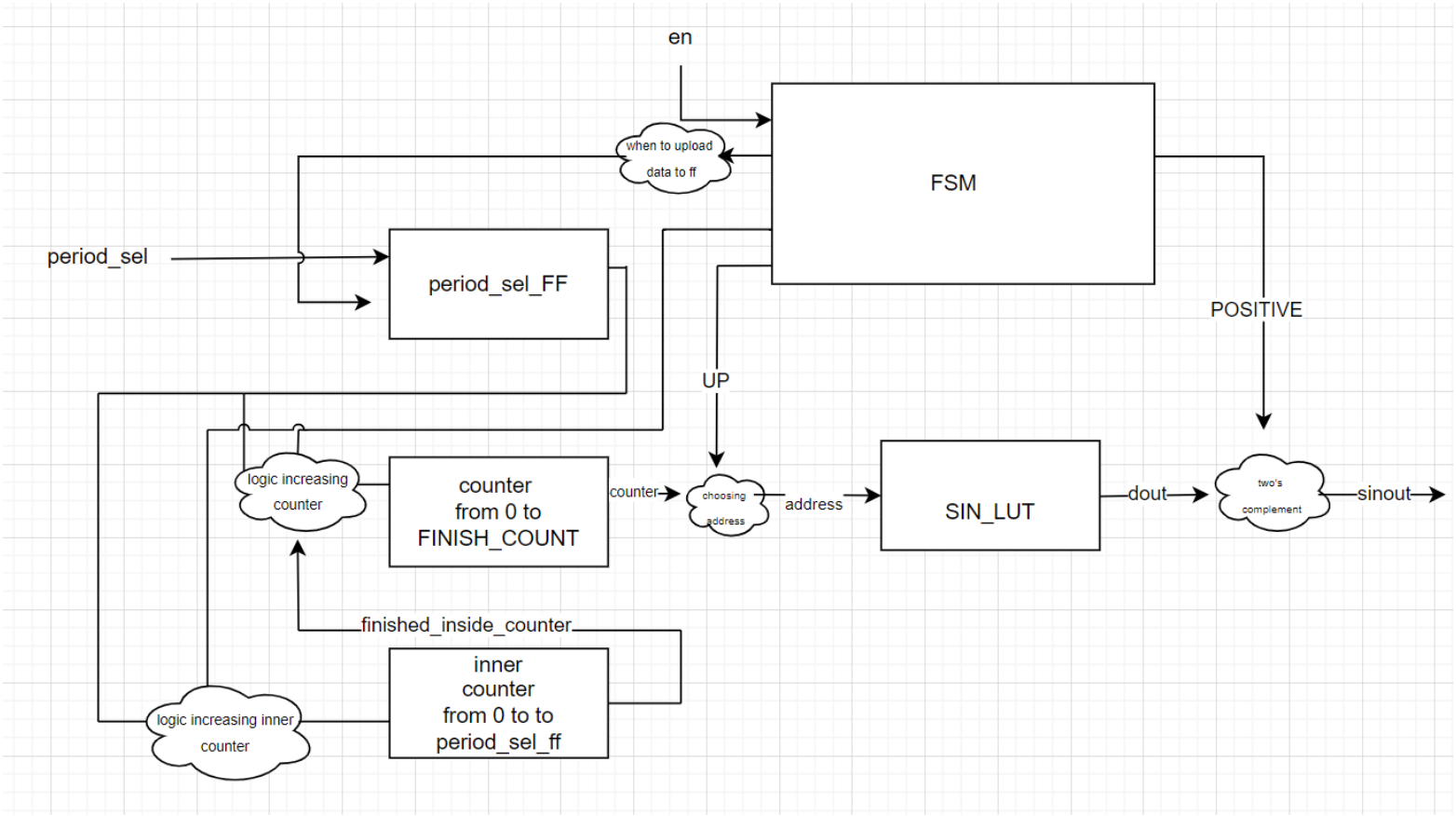
Advanced Logic Design: Lab 4

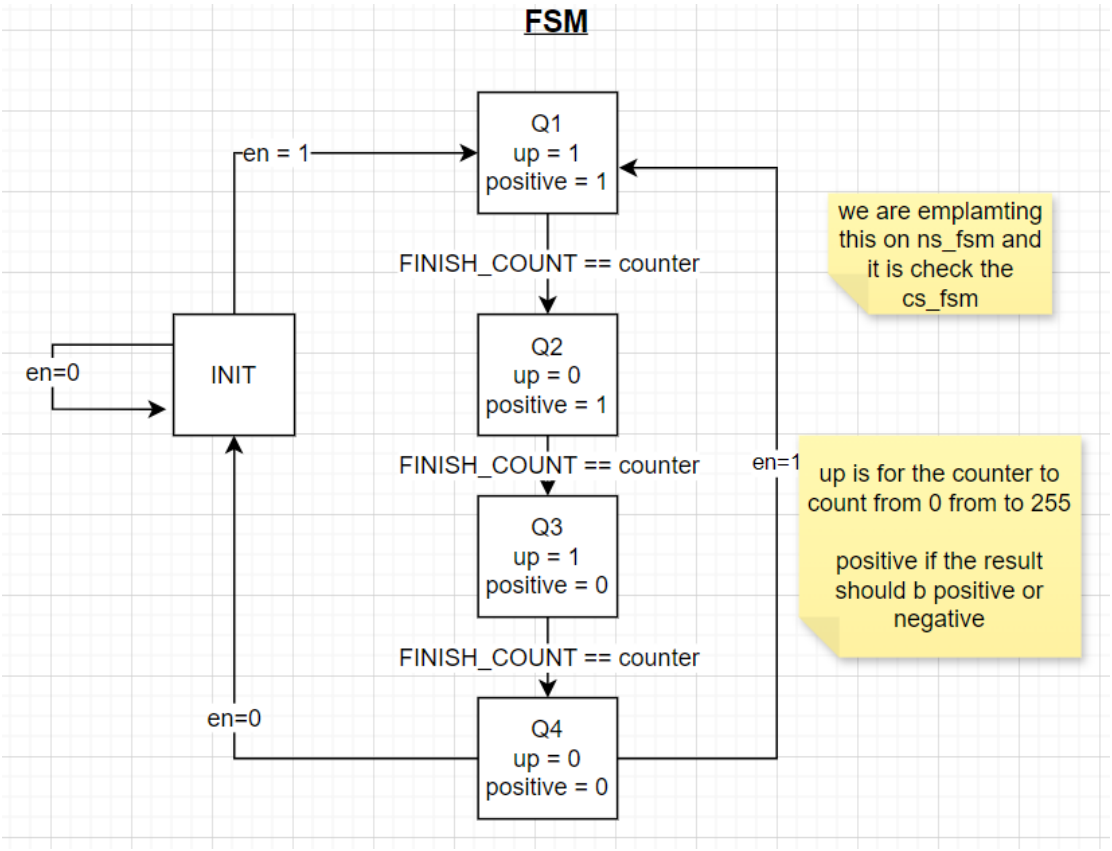
Question 4:

A: Micro Architecture Diagram:

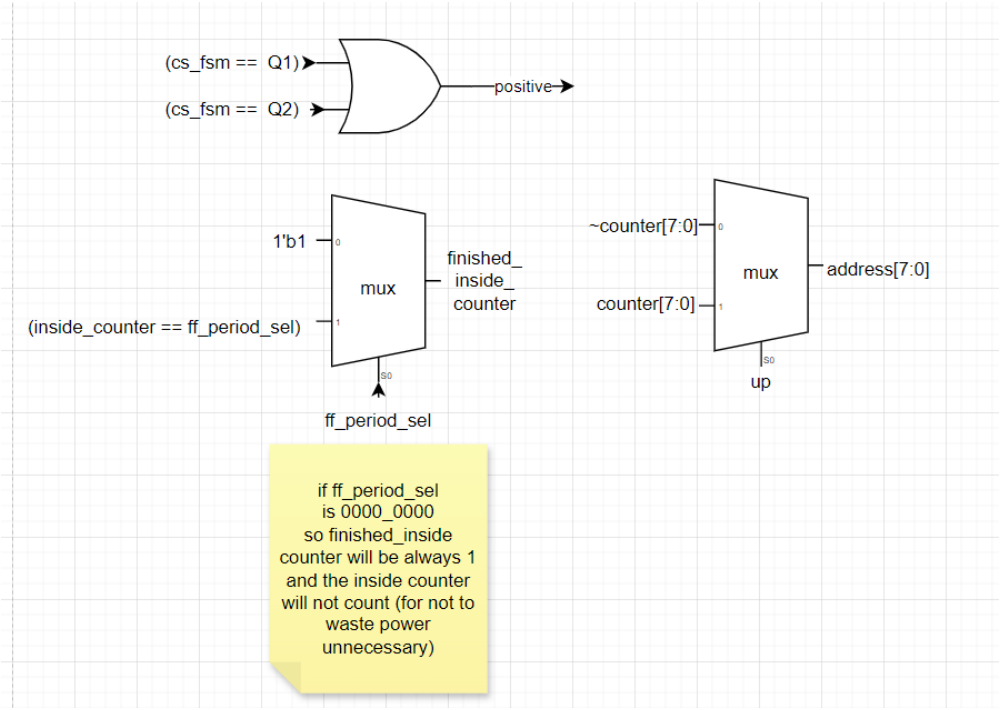


B: FSM Diagram:

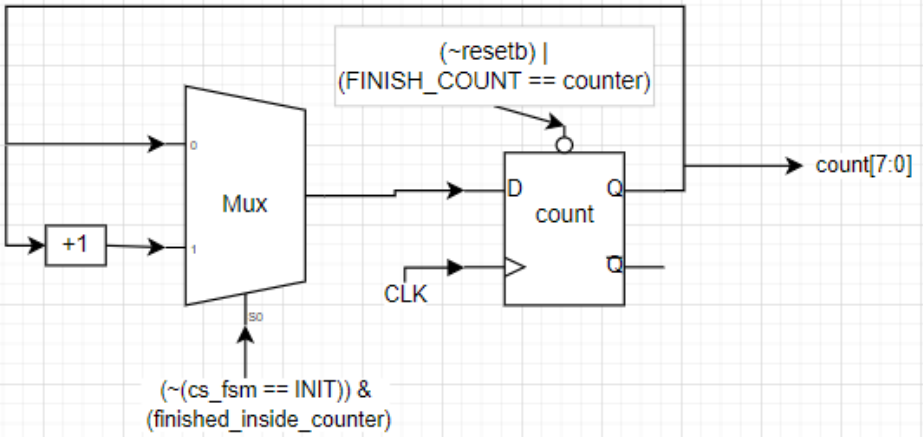
Every “Q” a quarter sinus wave is outputted. In the end of Q4 – a full cycle of sinus wave is outputted



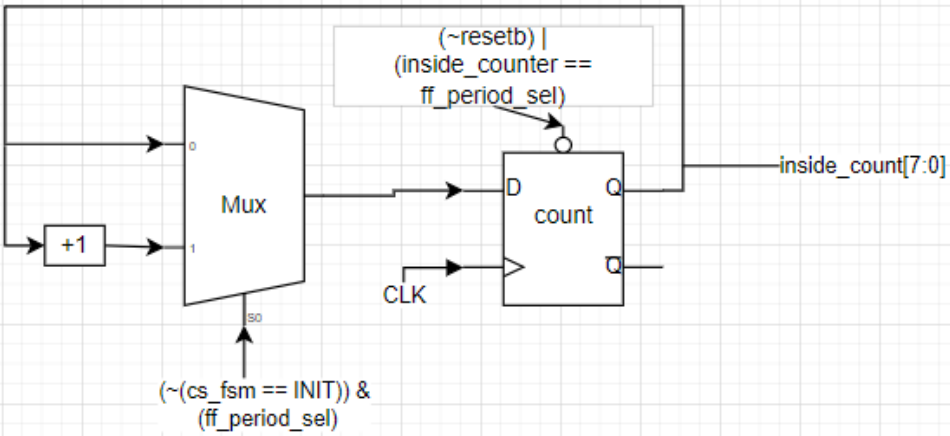
C: Full Design Diagram:



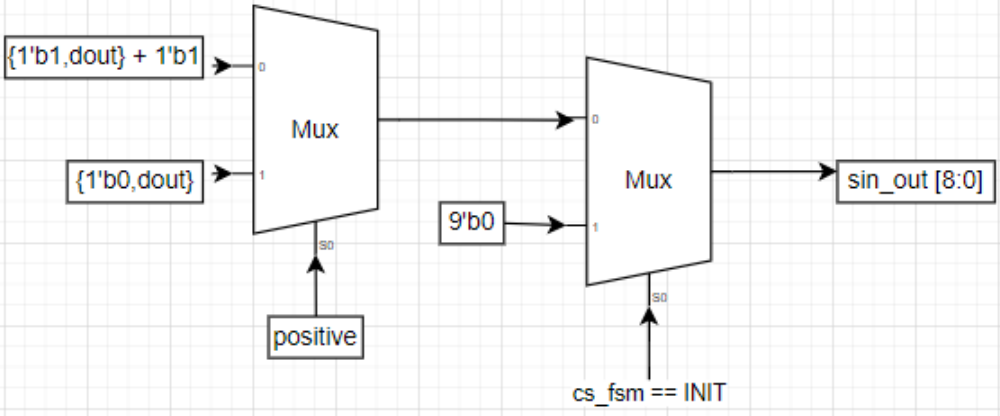
8-bit counter (counter until FINISH_COUNT)

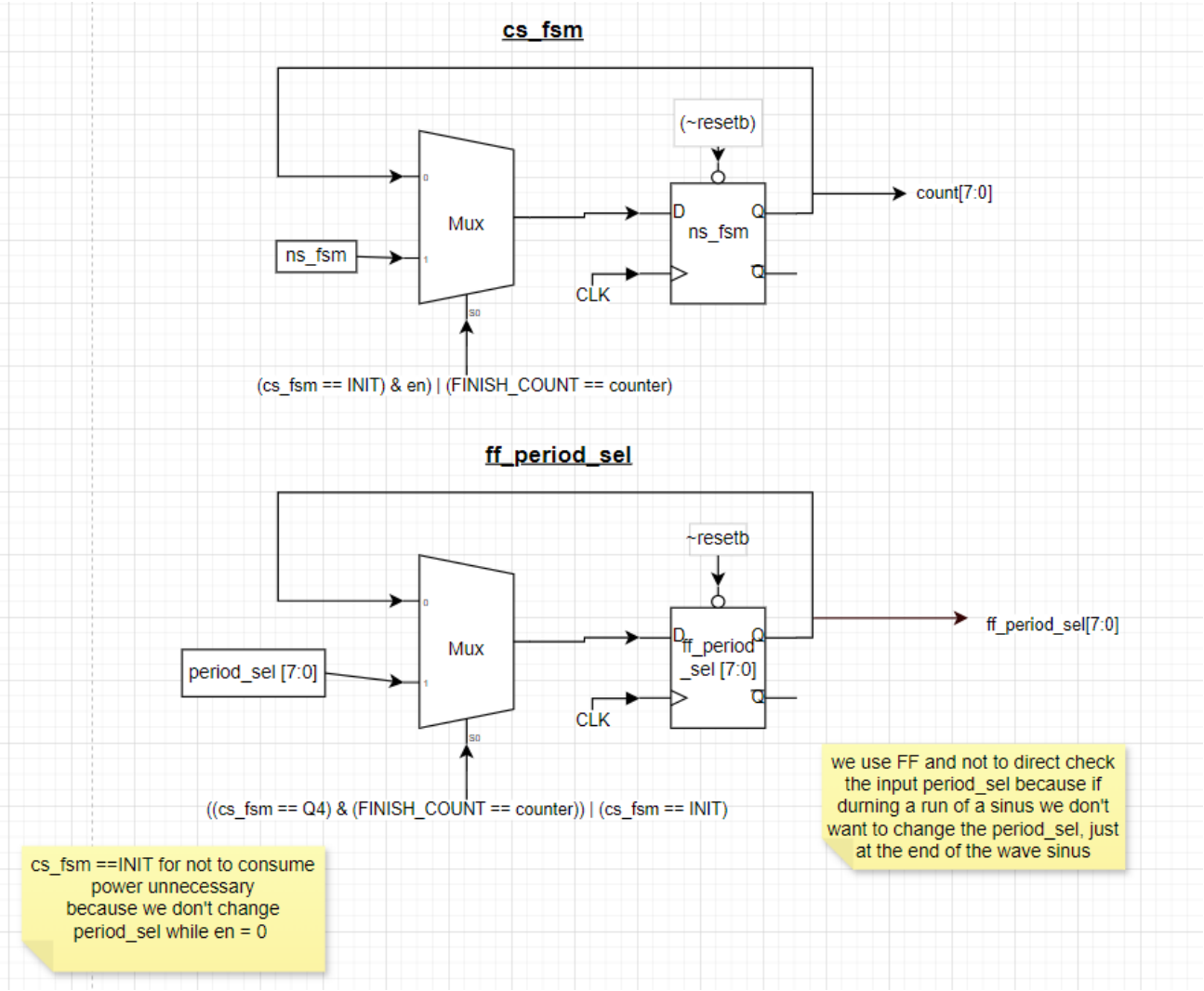


8-bit counter (inside counter)



Sin_ount

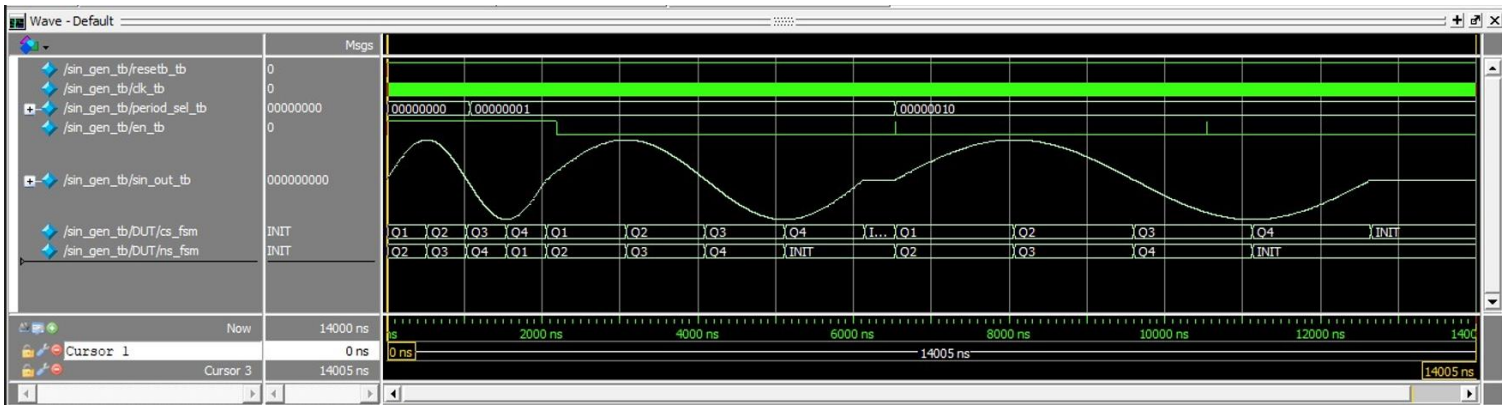



cs_fsm
(~resetb)
Mux
ns_fsm
D
Q
ns_fsm
Q
CLK
count[7:0]
(cs_fsm == INIT) & en) | (FINISH_COUNT == counter)
ff_period_sel
~resetb
Mux
period_sel [7:0]
D
Q
ff_period
_sel [7:0]
Q
CLK
ff_period_sel[7:0]
((cs_fsm == Q4) & (FINISH_COUNT == counter)) | (cs_fsm == INIT)
we use FF and not to direct check the input period_sel because if durning a run of a sinus we don't want to change the period_sel, just at the end of the wave sinus
cs_fsm ==INIT for not to consume power unnecessary because we don't change period_sel while en = 0

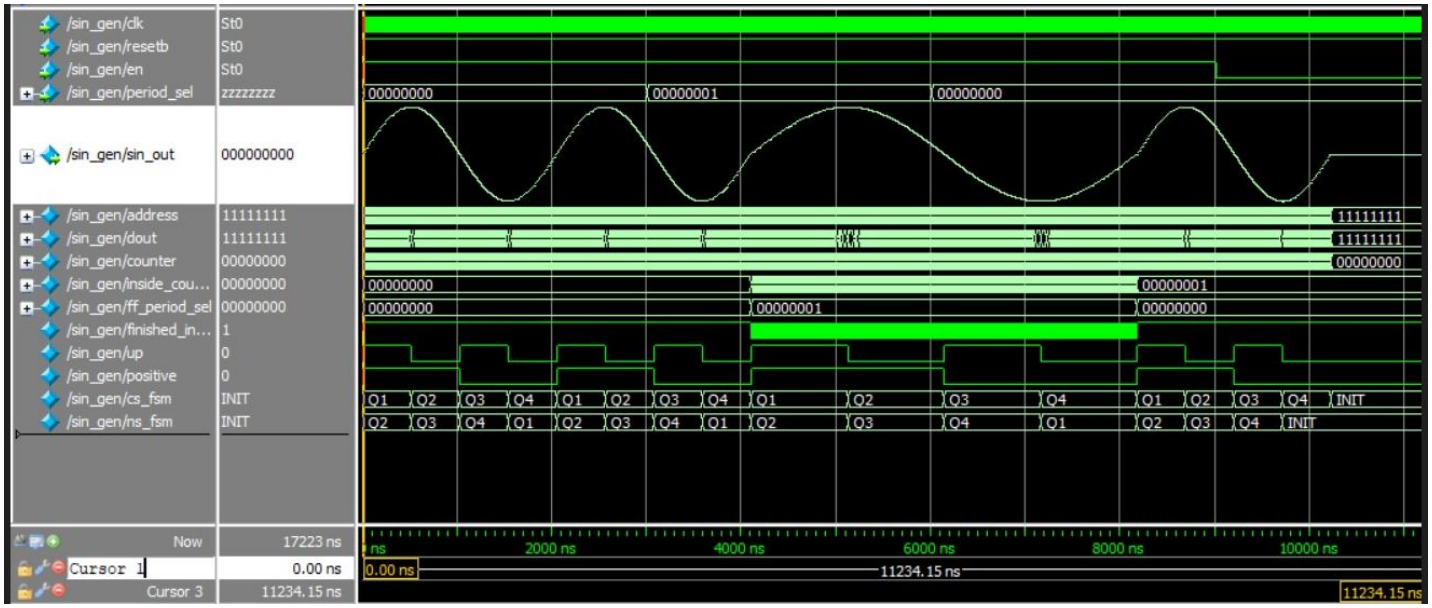
D,E: sin_gen.sv , sin_gen_tb.sv files are attached

F:

Here's scrrenshot to see the module correctness implementation:



Additional screenshot so the movement from different period_sel for en=1 happens smoothly

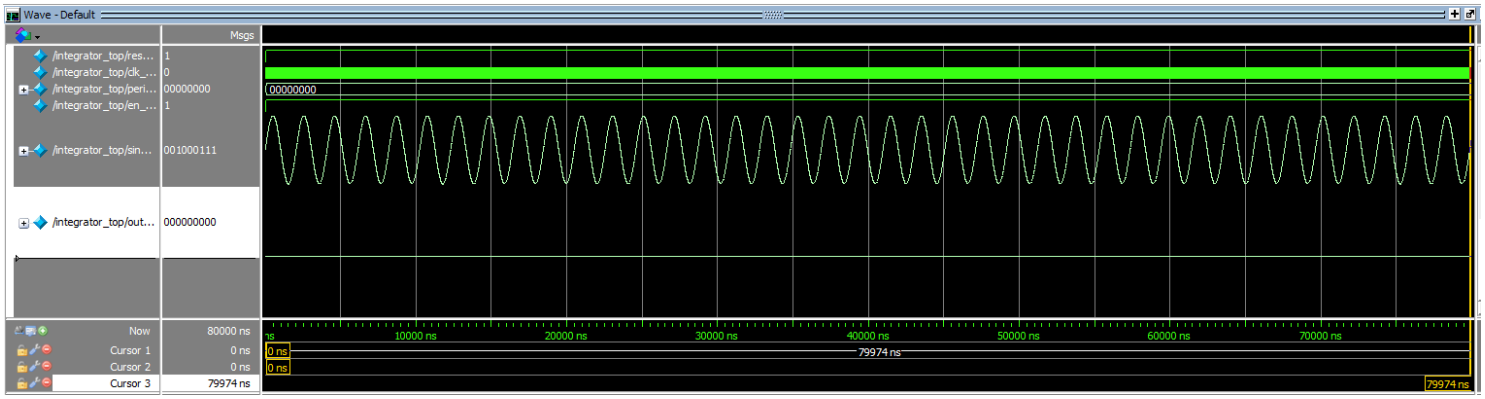


Bonus sections:

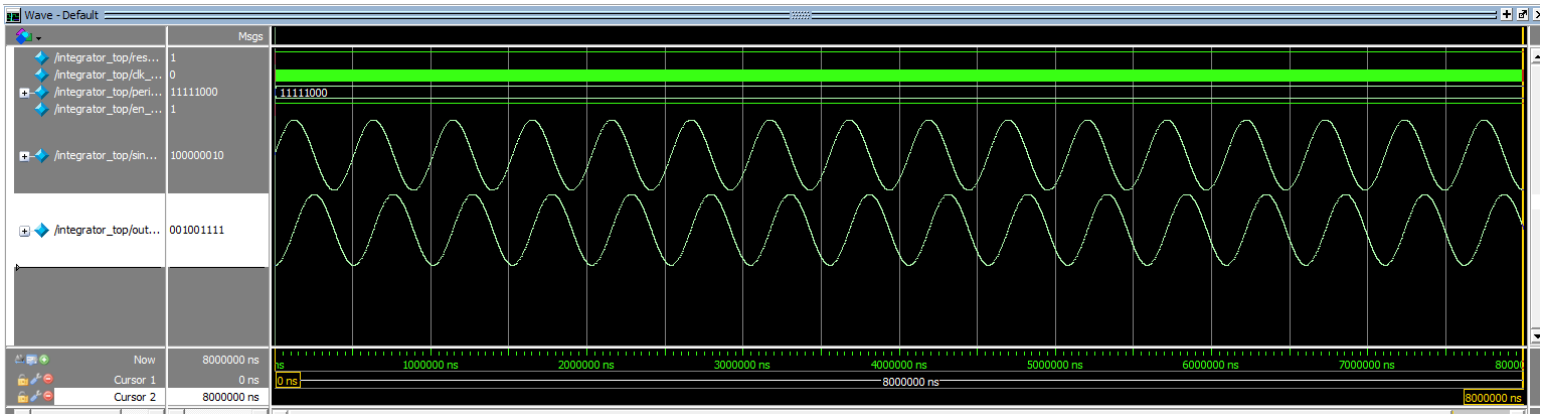
We have declared integrator_top.sv module and did instantiations to sin_gen.sv and integrator.sv (attached)

A: the max frequency is declared for period_sel = 8'b0000_0000

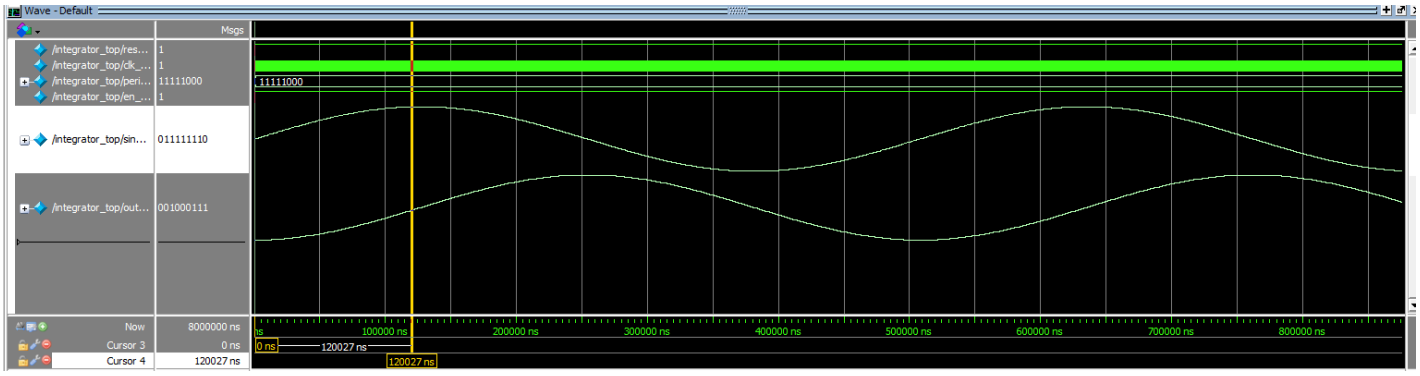
We have made a run and got the 0 function as an output, which means the integrator behaves like "low pass filter"



B: now we run the simulation with frequency of 8'hf8 = 8'b1111_1000 for 800000 ns , we got that the integrator "passes" the data with phase of -90 degrees

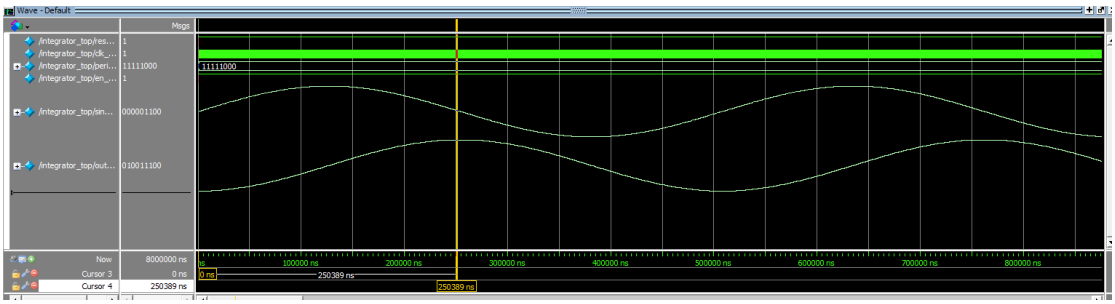


Anlyzing the amplification: We can see that we have negative amplification. For the sinus input:



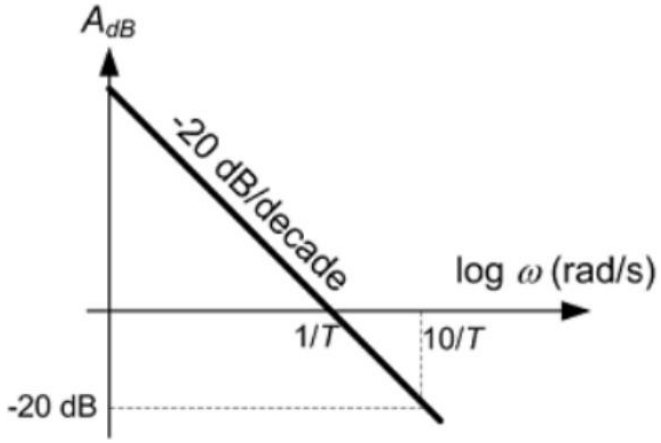
We got in the maximum point 8'b1111_1110 (as an unsigned value), which means 254 in decimal

For the integrator output



We got in the maximum point 8'b1001_1100 (as an unsigned value), which means 156 in decimal

So as we can see we got decreasing of the signal at 40% . this stands with the graph we saw in the Lab question:



(a) Magnitude plot.