

Flipping Bits in Memory: Study of DRAM Disturbance Errors

- Cell density has its advantages with reducing cost-per-bit, but has negative impacts:
 1. Small cell can hold a limited amount of charge
 2. Close proximity causes electromagnetic coupling effects
 3. Higher variation increases the number of outlier cells that corrupt the wanted functional effects of the technology
- High density DRAM is more likely to suffer from:
 - Disturbance: phenomenon in which different cells interfere with other operations
 - Disturbance Error: malfunctions/experiences in cell that is distributed beyond noise margin
- Exposing the disturbance errors in commodity DRAM chip
 - Out of 129 DRAM modules (972 DRAM chips), there are disturbance errors in 110 modules (836 chips)
 - Solution: a user-level program that continuously accesses DRAM by issuing many loads to the same address and ignoring cache-line in between
 - Root cause to disturbance errors are voltage fluctuations on the wordline where each row of cells (to enable wordline you must raise voltage, make it activated)
 - How voltage fluctuations affect are they attack on row's wordline and stirs a cell leakage charge at an accelerated rate. If it loses too much charge before restoration, it will create a disturbance error
- FPGA-based testing platform is environment use to characterize DRAM disturbance errors and understand behavior and symptoms
 - Example: error-correction and frequent refreshes
 - PARA (probabilistic adjacent row activation) prevents disturbance errors
 - Does not require expensive hardware structures or incur large performance penalties
- Accessing DRAM: three steps - (1) opening, (2) accessing desired info, (3) closing
 - Open Row: raise the word line, which connects the row to bitlines, and transfer data to the bank's row-buffer
 - Read/Write Columns: access row-buffer data as necessary
 - Close Row: before opening new row in existing bank, close the row (lower the word line) so that the row-buffer is cleared
- After a rank accepts a command, a delay is required before accepting another command

- The delay is referred to as a DRAM timing constraint.
- DRAM cell charge storage is not persistent, due to various leakage mechanisms by which charge can disperse (i.e. subthreshold leakage and gate-induced drain leakage)
- Cell's charge-level would deviate beyond the noise margin, losing data, which is considered as the cell's retention time
- Before time expires, cell's charge must be refreshed - open the row where the cell belongs
 - Row-buffer not only read the cell's altered charge value but restores the charge completely
 - Refreshing a row and opening a row are identical operations from a circuit's perspective