Board Layout Recommendations

Click on the "Show me" icon to highlight relevant areas on the sample layout.

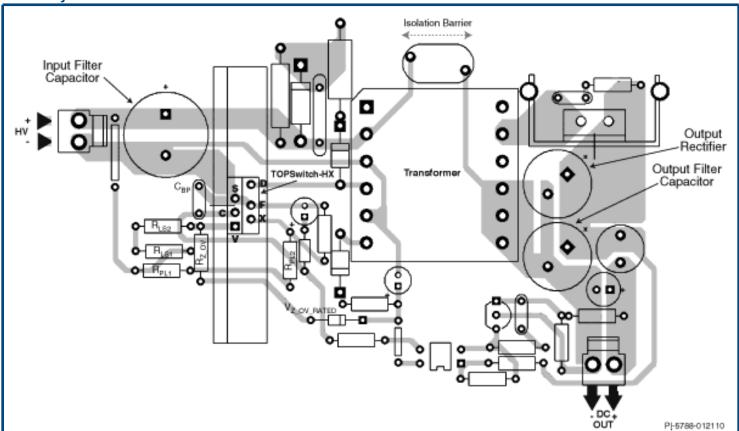
Minimize loop area formed by secondary winding, the output rectifier and the output filter capacitor

B+ connection of RLS or RPL resistor should be on input side of capacitor to prevent switching noise injection

Kelvin connection at SOURCE pins: power and signal currents kept separate

Y capacitor connected between output RTN and B+

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| | Description | Show Me |
|---|---|---------|
| 1 | Minimize loop area formed by drain, clamp and transformer | |
| 2 | Bias winding and bias capacitor are a power connection and therefore returned to Kelvin connection at SOURCE pin | |
| 3 | V and X pin node areas minimized, line sensing (R1 & R2) and power limiting (R3 & R4) close to device. Connections to V and X pin nodes should be away from noisy switching nodes (drain, clamp and bias) | |
| 4 | Place CONTROL pin decoupling capacitor directly across CONTROL and SOURCE pins | |