

# 1. Description

## 1.1. Project

Project Name	MEMSMIC
Board Name	NUCLEO-L476RG
Generated with:	STM32CubeMX 6.9.1
Date	09/16/2023

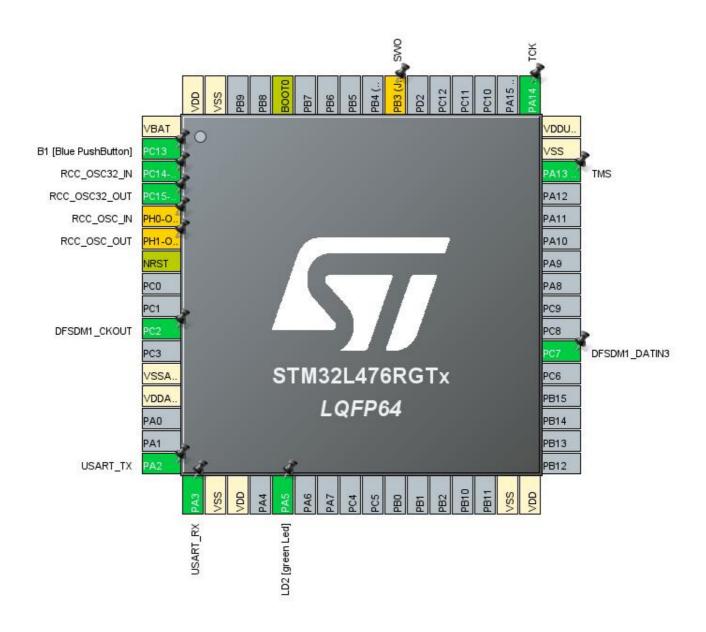
## 1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476RGTx
MCU Package	LQFP64
MCU Pin number	64

## 1.3. Core(s) information

Core(s)	Arm Cortex-M4

# 2. Pinout Configuration



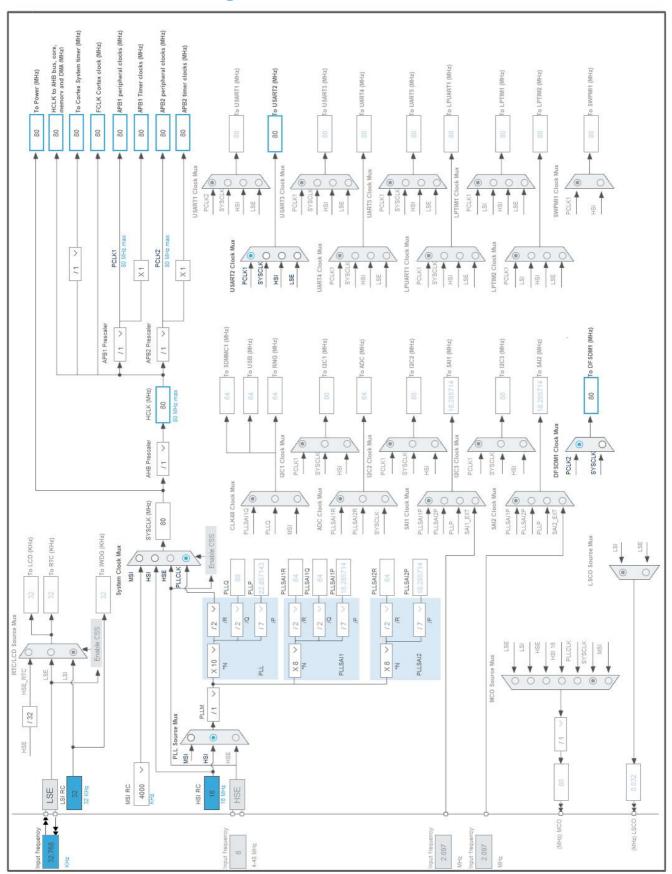
# 3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN (PH0) *	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT (PH1) *	I/O	RCC_OSC_OUT	
7	NRST	Reset		
10	PC2	I/O	DFSDM1_CKOUT	
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
21	PA5 **	I/O	GPIO_Output	LD2 [green Led]
31	VSS	Power		
32	VDD	Power		
38	PC7	I/O	DFSDM1_DATIN3	
46	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDDUSB	Power		
49	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 (JTDO-TRACESWO) *	I/O	SYS_JTDO-SWO	SWO
60	воото	Boot		
63	VSS	Power		
64	VDD	Power		

<sup>\*\*</sup> The pin is affected with an I/O function

<sup>\*</sup> The pin is affected with a peripheral function but no peripheral mode is activated

# 4. Clock Tree Configuration



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# 5. Software Project

## 5.1. Project Settings

Name	Value	
Project Name	MEMSMIC	
Project Folder	C:\Users\shiny\Documents\data-science-study\STM32\MEMSMIC	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_L4 V1.18.0	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

## 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

## 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART2_UART_Init	USART2
5	MX_DFSDM1_Init	DFSDM1

# 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476RGTx
Datasheet	DS10198_Rev4

## 1.2. Parameter Selection

Temperature	25
Vdd	3.0

## 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

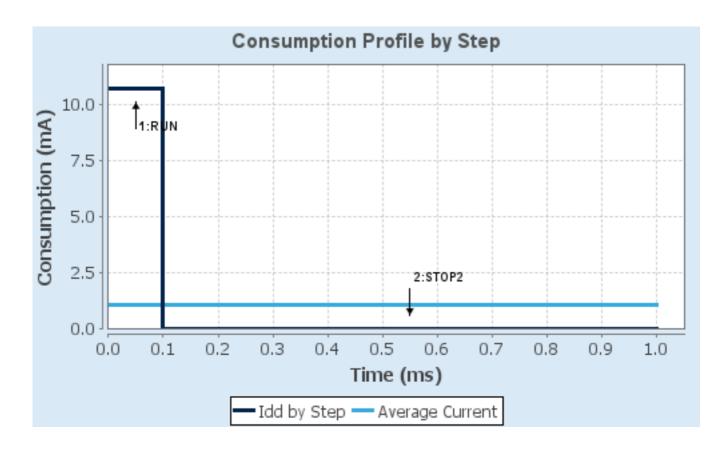
## 1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10.7 mA	1.18 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.56	105
Category	In DS Table	In DS Table

## 1.5. Results

Sequence Time	1 ms	Average Current	1.07 mA
Battery Life	4 months, 10	Average DMIPS	100.0 DMIPS
	days, 3 hours		

## 1.6. Chart



## 2. Peripherals and Middlewares Configuration

#### 2.1. DFSDM1

mode: PDM/SPI input from ch3 and internal clock

#### 2.1.1. Filter 0:

#### regular channel selection:

regular channel selection

Channel 3 \*

Continuous Mode

Continuous Mode

Trigger to start regular conversion

Fast Mode

Enable \*

Enable \*

#### injected channel selection:

Channel0 as injected channel Disable Channel1 as injected channel Disable Channel2 as injected channel Disable Channel3 as injected channel Disable Channel4 as injected channel Disable Channel5 as injected channel Disable Channel6 as injected channel Disable Channel7 as injected channel Disable

#### Filter parameters:

Sinc Order Sinc 3 filter type \*

Fosr 128 \*

#### 2.1.2. Filter 1:

#### regular channel selection:

regular channel selection - None -

#### injected channel selection:

Channel0 as injected channel Disable Disable Channel1 as injected channel Channel2 as injected channel Disable Channel3 as injected channel Disable Channel4 as injected channel Disable Channel5 as injected channel Disable Disable Channel6 as injected channel Channel7 as injected channel Disable

## 2.1.3. Filter 2:

#### regular channel selection:

regular channel selection - None -

injected channel selection:

Channel0 as injected channel Disable Disable Channel1 as injected channel Disable Channel2 as injected channel Disable Channel3 as injected channel Disable Channel4 as injected channel Disable Channel5 as injected channel Disable Channel6 as injected channel Disable Channel7 as injected channel

#### 2.1.4. Filter 3:

#### regular channel selection:

regular channel selection - None -

injected channel selection:

Channel0 as injected channel Disable Channel1 as injected channel Disable Channel2 as injected channel Disable Disable Channel3 as injected channel Channel4 as injected channel Disable Channel5 as injected channel Disable Channel6 as injected channel Disable Channel7 as injected channel Disable

#### 2.1.5. Output Clock:

#### **Output Clock parameters:**

Selection Source for ouput clock is system clock

Divider 32 \*

#### 2.1.6. Channel 3:

#### **Channel 3 parameters:**

Type SPI with rising edge

Spi Clock Internal SPI clock

Offset

Right Bit Shift 0x06 \*

Analog watchdog parameters:

Filter Order FastSinc filter type

Oversampling 1

#### 2.2. RCC

#### Low Speed Clock (LSE): Crystal/Ceramic Resonator

#### 2.2.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled \*
Data Cache Enabled

Flash Latency(WS) 4 WS (5 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 16
MSI Calibration Value 0

MSI Auto Calibration Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

**Power Parameters:** 

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

#### 2.3. SYS

**Debug: Serial Wire** 

Timebase Source: SysTick

#### 2.4. **USART2**

**Mode: Asynchronous** 2.4.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

**Advanced Features:** 

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Disable Data Inversion TX and RX Pins Swapping Disable Enable Overrun DMA on RX Error Enable MSB First Disable

#### \* User modified value

# 3. System Configuration

## 3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DFSDM1	PC2	DFSDM1_CKOU T	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	DFSDM1_DATIN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14- OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T (PC15)	RCC_OSC32_O UT	n/a	n/a	n/a	
SYS	PA13 (JTMS- SWDIO)	SYS_JTMS- SWDIO	n/a	n/a	n/a	TMS
	PA14 (JTCK- SWCLK)	SYS_JTCK- SWCLK	n/a	n/a	n/a	TCK
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USART_RX
Single Mapped Signals	PH0- OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PB3 (JTDO- TRACESWO )	SYS_JTDO- SWO	n/a	n/a	n/a	SWO
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [green Led]

## 3.2. DMA configuration

DMA request	Stream	Direction	Priority
DFSDM1_FLT0	DMA1_Channel4	Peripheral To Memory	Low

### DFSDM1\_FLT0: DMA1\_Channel4 DMA request Settings:

Mode: Circular \*

Peripheral Increment: Disable

Memory Increment: Enable \*

Peripheral Data Width: Word
Memory Data Width: Word

## 3.3. NVIC configuration

## 3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
DMA1 channel4 global interrupt	true	0	0	
USART2 global interrupt	true	0	0	
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
EXTI line[15:10] interrupts	unused			
DFSDM1 filter3 global interrupt	unused			
DFSDM1 filter0 global interrupt	unused			
DFSDM1 filter1 global interrupt	unused			
DFSDM1 filter2 global interrupt	unused			
FPU global interrupt	unused			

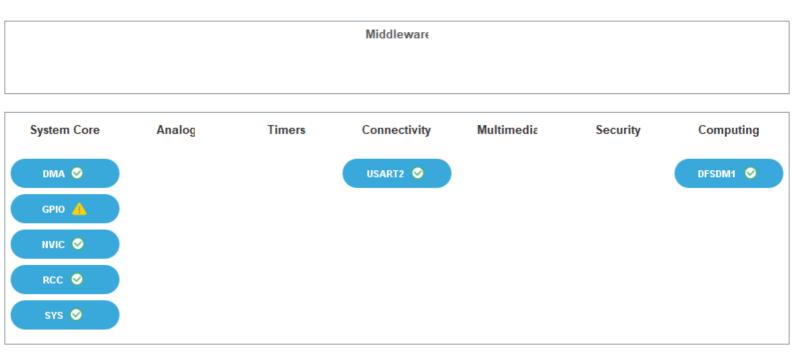
## 3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel4 global interrupt	false	true	true
USART2 global interrupt	false	true	true

\* User modified value

# 4. System Views

- 4.1. Category view
- 4.1.1. Current



## 5. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl\_model/stm32l4\_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis\_model/stm32l4\_ibis.zip

System View https://www.st.com/resource/en/svd/stm32l4\_svd.zip

Description

Presentations https://www.st.com/resource/en/product\_presentation/stm32-

stm8\_embedded\_software\_solutions.pdf

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microcontroller-system-memory-boot-mode-stmicroelectronics.pdf

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recommendations-and-package-information-for-leadfree-ecopack-mcus-

and-mpus-stmicroelectronics.pdf

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best-adc-accuracy-in-stm32-microcontrollers-stmicroelectronics.pdf

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design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application\_note/an3126-audio-and-

waveform-generation-using-the-dac-in-stm32-products-

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used-in-the-stm32-bootloader-stmicroelectronics.pdf

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used-in-the-stm32-bootloader-stmicroelectronics.pdf

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protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

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number-of-touchkeys-for-touch-sensing-applications-on-mcus-

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- used-in-the-stm32-bootloader-stmicroelectronics.pdf
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- Application Notes https://www.st.com/resource/en/application\_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4612-migrating-from-stm32l1-series-to-stm32l4-series-and-stm32l4-series-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4616-migrating-from-stm32f401-and-stm32f411-lines-to-stm32l4-series-and-stm32l4-series-microcontrollers-stmicroelectronics.pdf
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