EE241 Final Project
Fall 2020

due: February 12, Saturday, 23:55

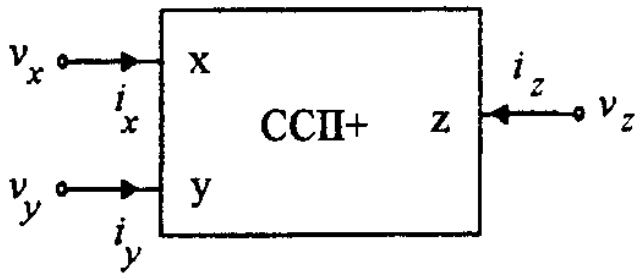
Reminder: By returning this homework assignment you have agreed that you, in person, are fully responsible for the consequences of violating the rules of conduct. As a university student, you are expected to act maturely and responsibly. In short, **do not cheat!** Your submission will be checked automatically (and manually, if needed) for plagiarism.

After doing - before submitting - your homework, you must write the following statement on paper by hand, include your name and the date, sign and scan the paper (into a pdf file, e.g., by using a mobile scanner application), and include the pdf file among the other files to be submitted: **"I have neither given nor received any unauthorized aid on this assignment."**

Please upload all the relevant files as a single zip archive on Moodle until February 12, Saturday, 23:55.
No late homeworks!

SPICE

In the company you are working you are told to design an analog filter for a communication system with the given specifications. You made a literature search and found an RLC passive network which is suitable for your needs (Fig.5 of the paper). Since you will finally design an integrated circuit and since you know that large inductors such as in mH range cannot be integrated, the passive filter cannot be used directly. But you are told that inductors can also be simulated electronically by one or more active elements (like opamp), resistors and capacitors. All of them are integrable (capacitors up to 50pF). Instead of the opamp you decided to use the current conveyor (plus type) which internally consists of a voltage buffer (input y terminal, output x terminal; thus Vx=Vy); and a current buffer where x terminal current is copied to z terminal (Iz=Ix). The governing equation and the symbol is shown below.



$$i_y(t) = 0$$
$$v_x(t) = v_y(t)$$
$$i_z(t) = i_x(t)$$

1. Build the ideal model of the current conveyor with ideal voltage and current buffers in LT Spice.
2. Realize a floating inductor in Fig. 2b with R=R1=R2=20k, C=16pF (as in the simulation section of the paper)
3. Build the Butterworth filter with passive components as shown in Fig.5 of the paper in LT Spice.
4. Make a copy of the Butterworth filter by replacing the inductor by your design in step 2 in the same LT Spice file.
5. Simulate the circuits and plot the frequency response of both ideal passive (step 3) and your ideal design (step 4) on the same graph.
6. Bonus (not required): A current conveyor is commercially available as AD844 CFOA (which has noninverting terminal corresponding to y; inverting terminal corresponding to x, compensation terminal corresponding to z; output terminal of CFOA is not used in CCII+ applications). Replace the ideal model of the current conveyor you created in step 1 with the one you obtain from the manufacturer and repeat step 5.