EPFL

A Network Tour of Data Science | EE-558

Understanding Negotiated-Congestion Routing for FPGAs

Group 49

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What Is an FPGA?

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This holds both for gates and connections

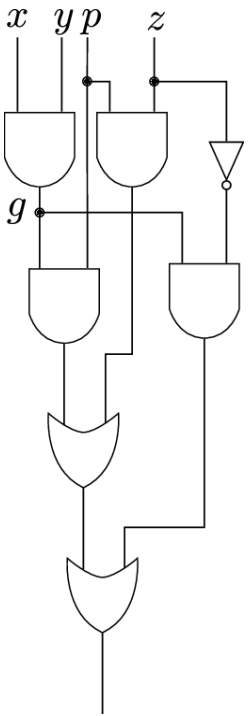
How Is an FPGA Used?

$$f(x, y, z, p) = (xy + z)p + xy\overline{z}$$

1) Specify the desired behavior
   (a circuit graph)

2) Determine location of each gate
   (placement)

3) Determine how their terminals are connected
   (routing)



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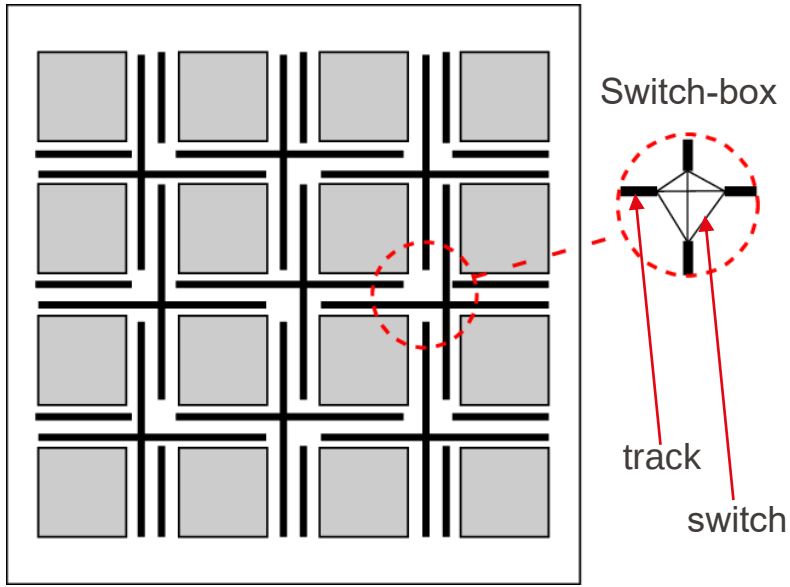
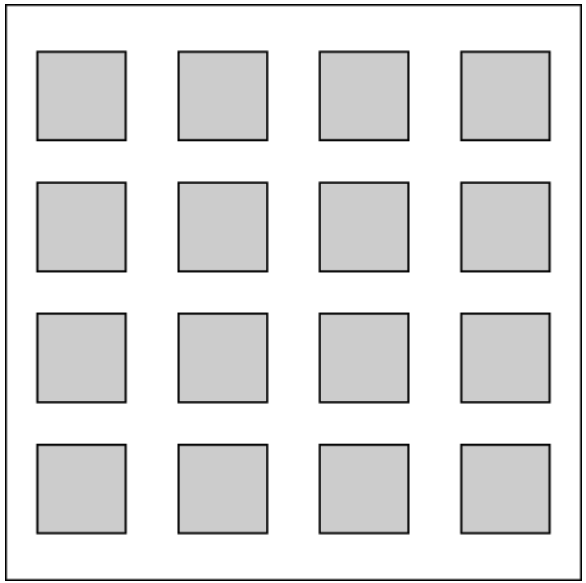


Turn switches "on" or "off"
to connect existing tracks

Placement



Task: Assign each node of the circuit graph a unique location on the FPGA grid s.t:

1) Total wire length is minimized

2) Delay of the slowest (critical) path is minimized

A. Marquardt, V. Betz, and J. Rose, "Timing-driven placement for FPGAs", FPGA'00

Placement: Timing Optimization

We need to know t_d for each connection (u, v)

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Routing after each place modification is not feasible!

Placement: Timing Optimization

Solution: Compute the fastest path delay between each pair of locations (A, B), store the delays in a look-up table, and use this table during placement

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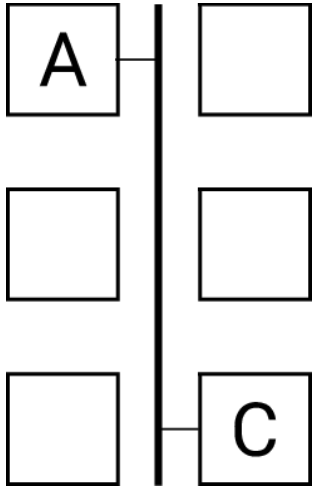
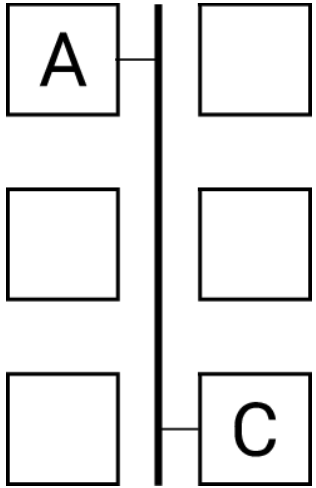
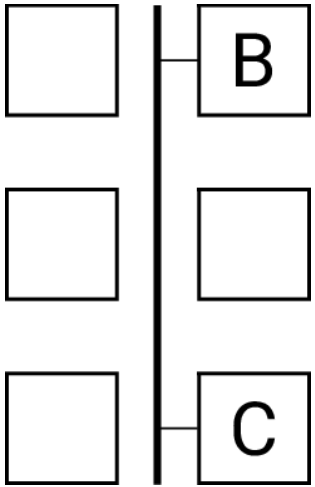


t_d(A, C) = 126 ps

Placement: Timing Optimization

Solution: Compute the fastest path delay between each pair of locations (A, B), store the delays in a look-up table, and use this table during placement



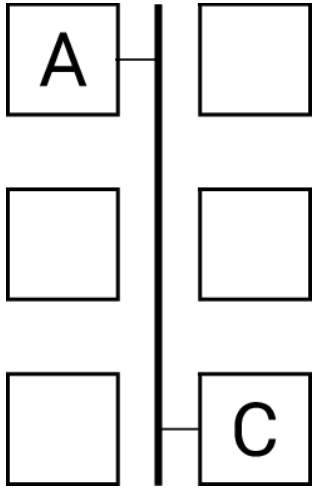


t_d(A, C) = 126 ps

t_d(B, C) = 126 ps

Placement: Timing Optimization

Solution: Compute the fastest path delay between each pair of locations (A, B), store the delays in a look-up table, and use this table during placement



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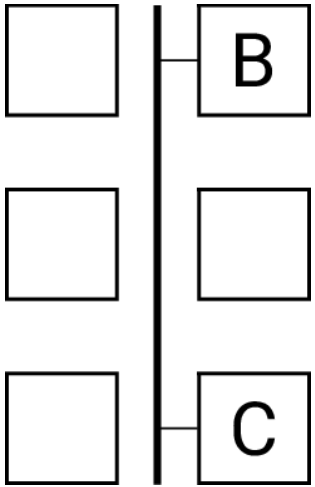
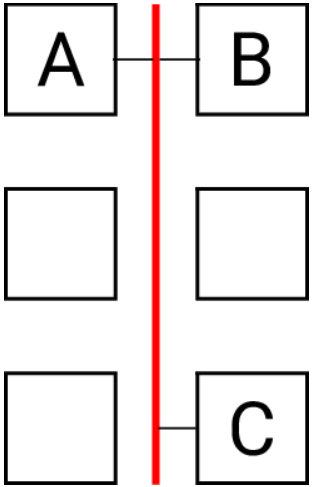


t_d(B, C) = 126 ps



t_d(B, C) = 126 ps
t_d(A, C) = 126 ps

Placement: Timing Optimization

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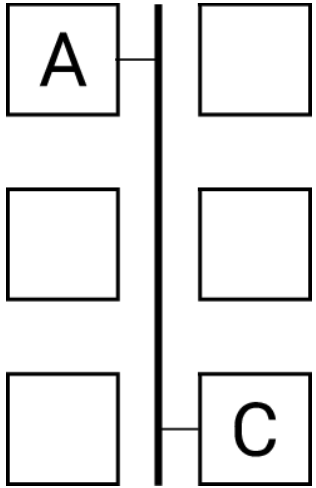

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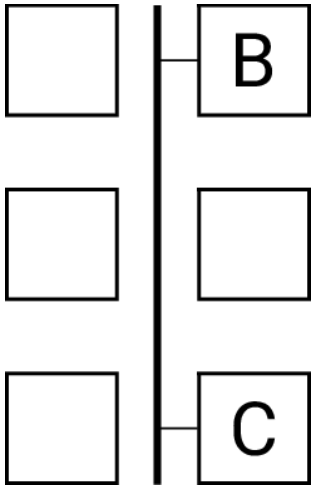

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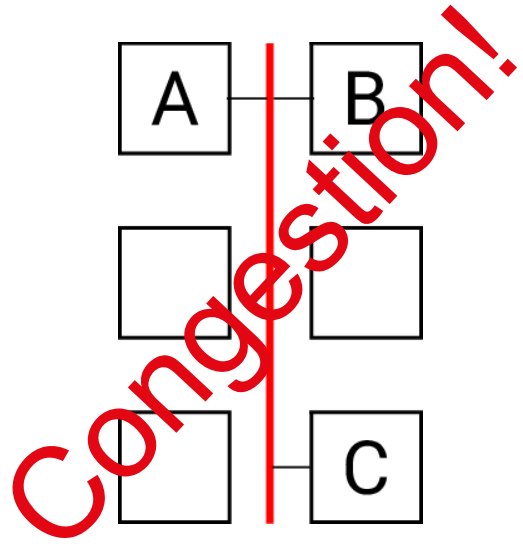

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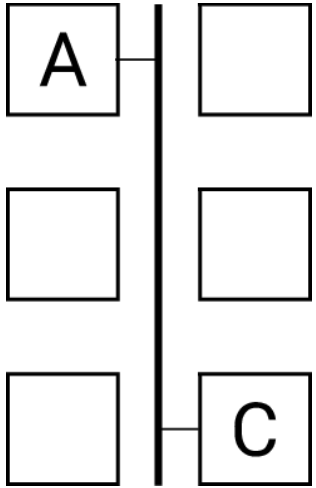

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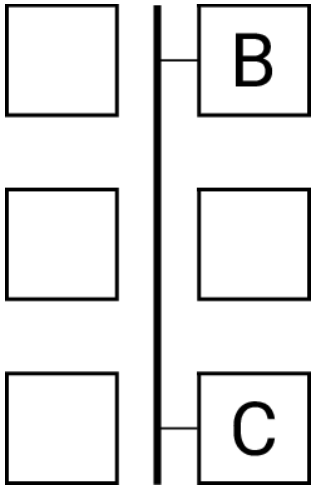

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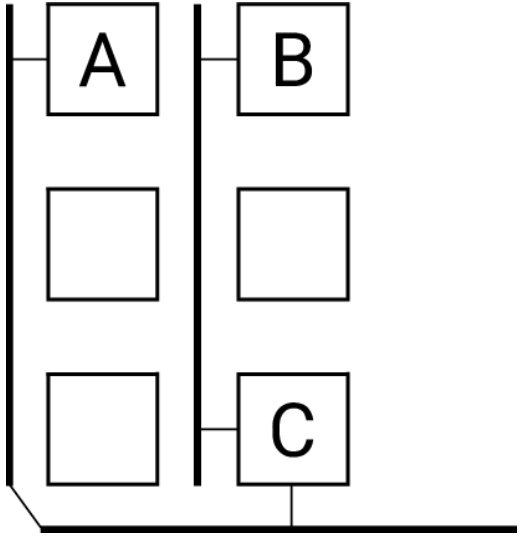


t_d(B, C) = 126 ps
t_d(A, C) = 218 ps

When Does Congestion Influence Delay?

Goals:

- Understand the phenomenon
- Predict it from placement
- Is the placer causing it, or the inherent structure of the circuit?

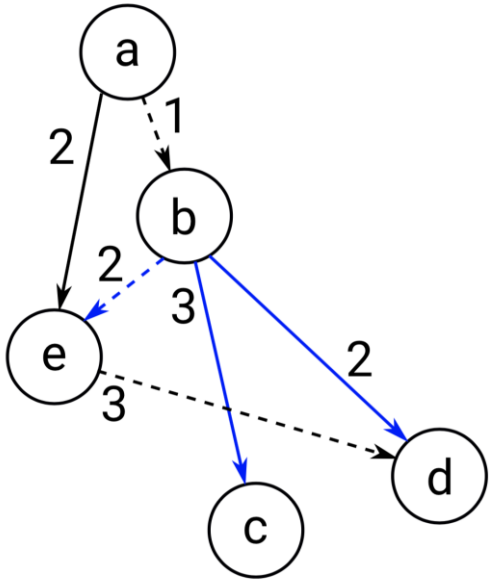
Potential benefits:

- Understand which algorithms need to be improved and get inspiration for doing that
- Get inspiration for FPGA architecture improvement by better appreciating the circuit structure
- Enable wider architectural space exploration by avoiding routing (if we final delay can be more accurately predicted from placement)

The basic model design

Net:

- The set of connections between an output of a particular gate and inputs of all the gates that it drives.
- How can we weight the nets? Criticality!

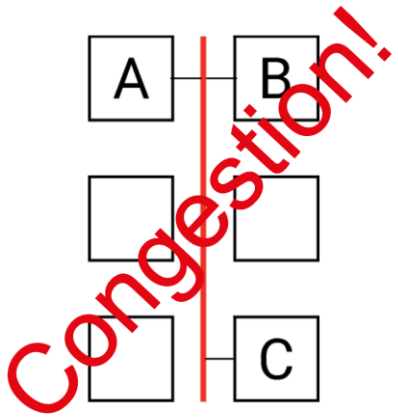


Critical net: Criticality = 1

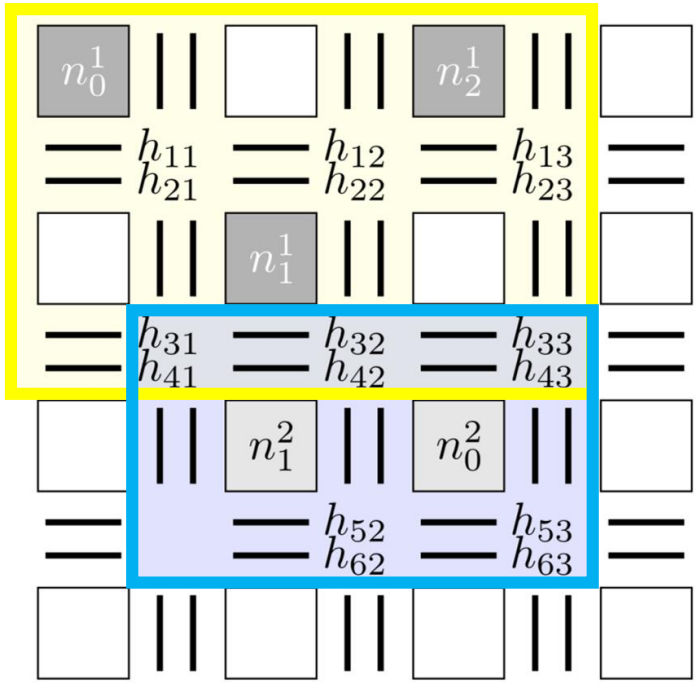
We may run into a problem...

Congestion

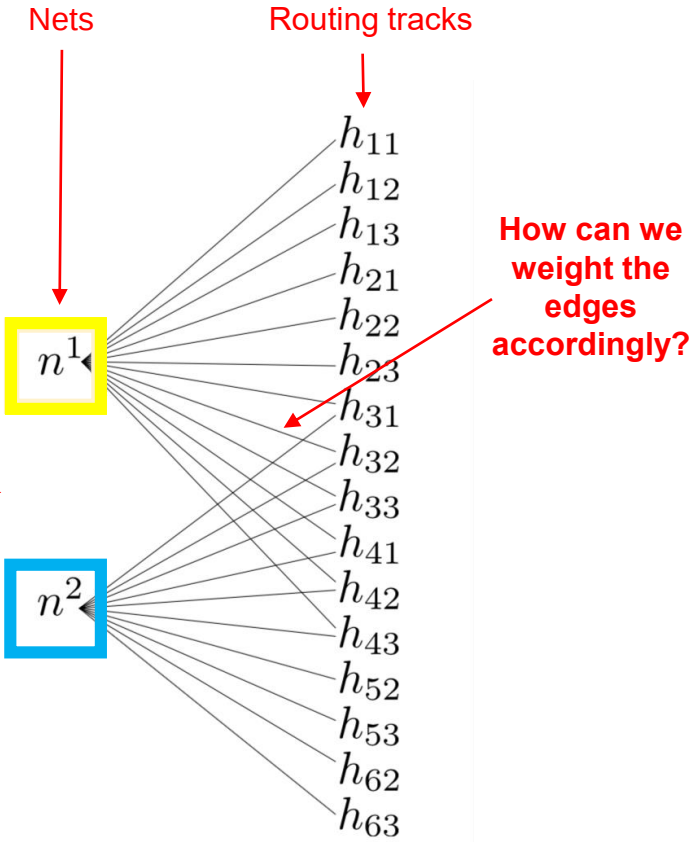
- problematic if, for the given placement of a given circuit, two nets that are (close to) critical must be routed using the same track in order to achieve the shortest route



Design bipartite graph



Bipartite graph



How can we weight the edges accordingly?

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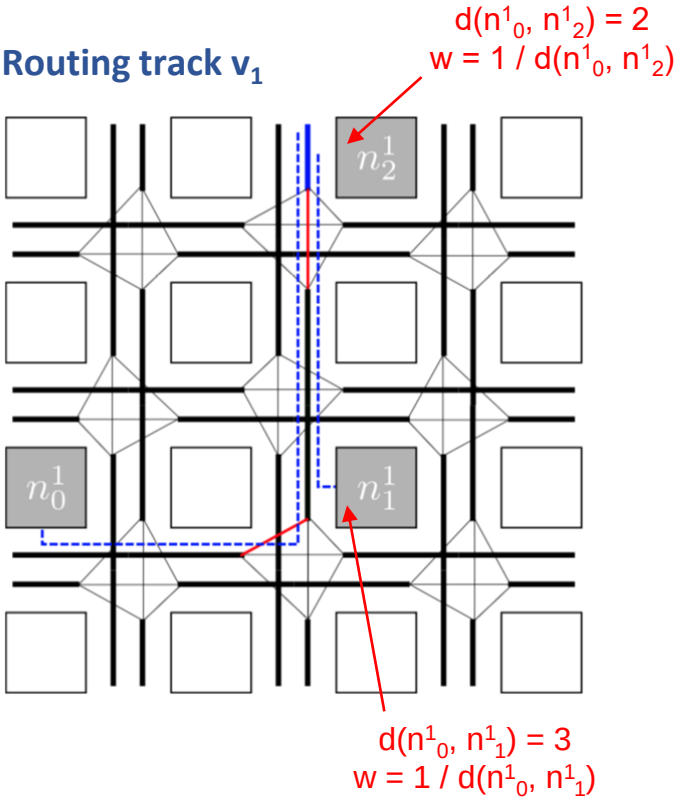
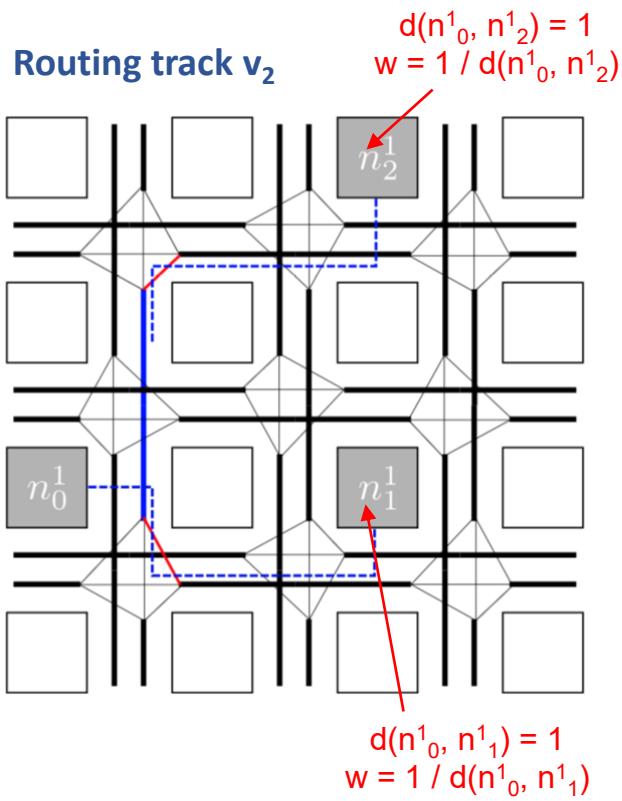
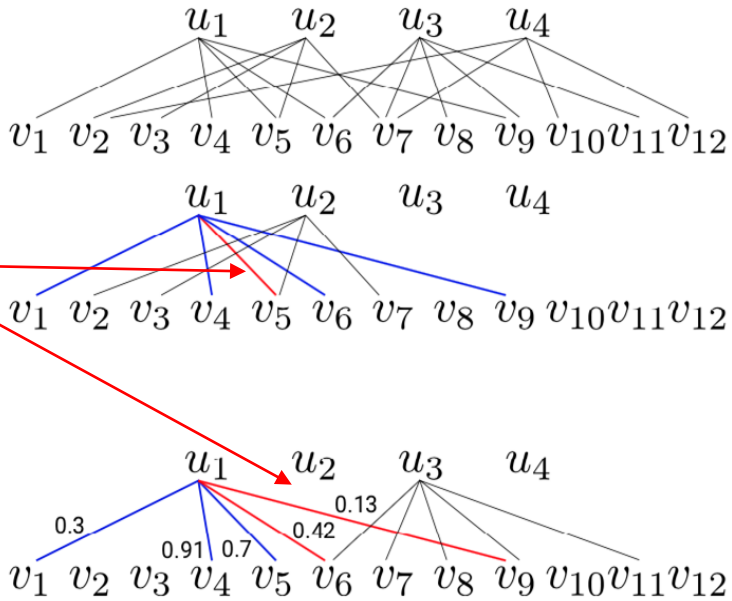
Bipartite graph edge weights



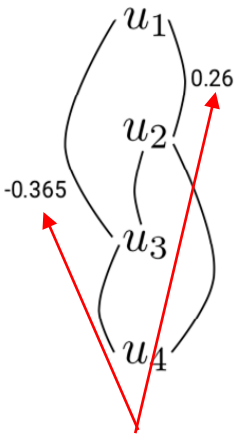


Projection of the bipartite graph



How can we describe these conflicting regions?

Projection



gives an idea about how much a net would lose by giving up its preferred track to its opponent net!

$$\langle w_c(u_1) \rangle = \frac{\sum_{v \in \{N_1 \cap N_2\}} w(u_1, v)}{|N_1 \cap N_2|}$$

$$\langle w_{uc}(u_1) \rangle = \frac{\sum_{v \in \{N_1 \setminus N_2\}} w(u_1, v)}{|N_1 \setminus N_2|}$$

$$w_p(u_1, u_2) = min(\{\langle w_c(u_1) \rangle - \langle w_{uc}(u_1) \rangle, \langle w_c(u_2) \rangle - \langle w_{uc}(u_2) \rangle\})$$

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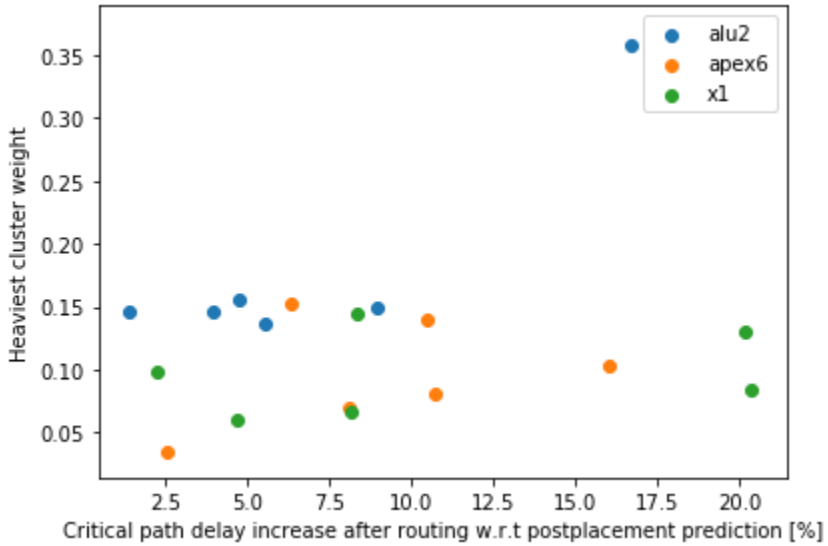
Testing the Main Conjecture

CONJECTURE 1. *The routed delay will be noticeably larger than the post-placement prediction iff there are heavy clusters in the projection of the net-representing partition.*

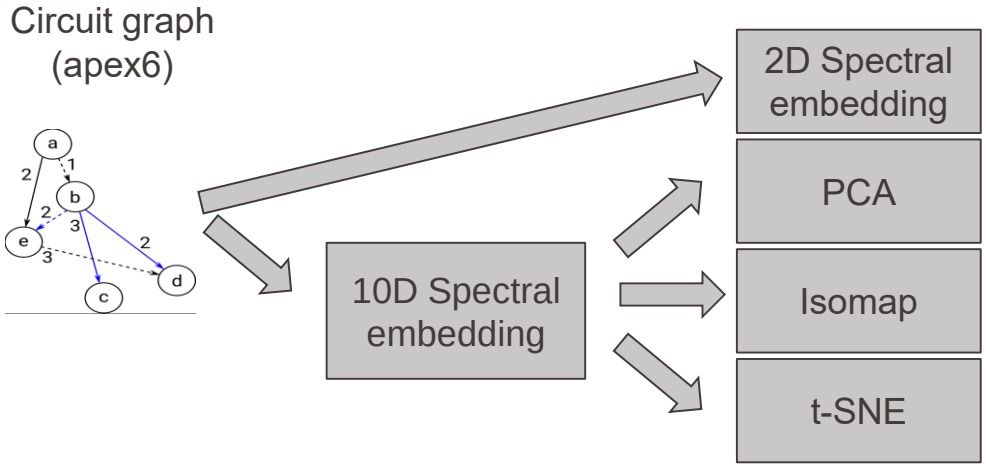
1. Identify 16 clusters using spectral clustering on projection graph
2. Find heaviest clusters
3. Plot heaviest cluster weight vs routed critical path delay increase w.r.t. post-placement prediction

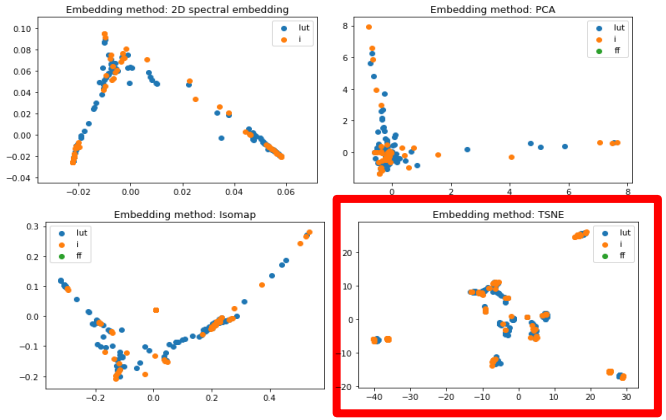


Conjecture rejected

How Good is the Placer?

- Is the structure of the original circuit graph preserved in the 2D embedding produced by the placer?





Most clearly distinguishable clusters

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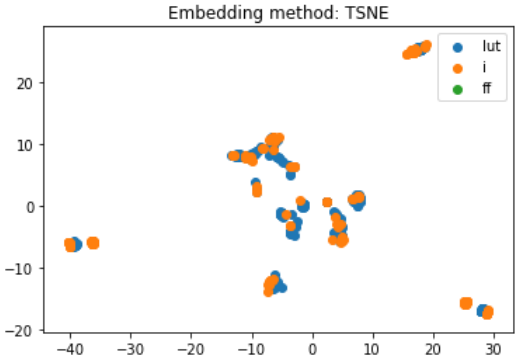
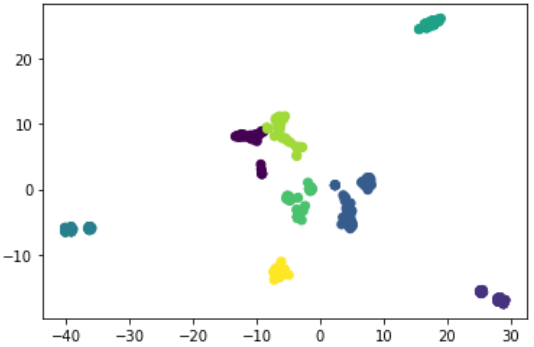
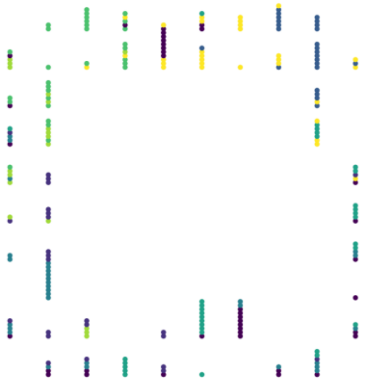
How Good is the Placer?



KMeans



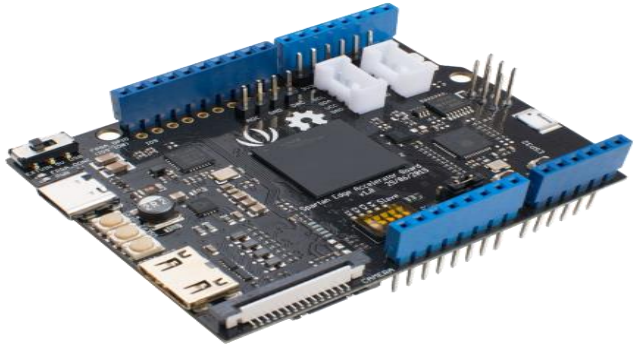
Using the same labels for the placed circuit



Most of the clusters in the original circuit graph seem to have been preserved by the placer

What comes next?

- Industry seem to have optimized the hell out of FPGAs
- It might be very difficult to make significant improvements



What comes next?

2018 International Conference on Field-Programmable Logic and Applications

Machine-Learning Based Congestion Estimation for Modern FPGAs

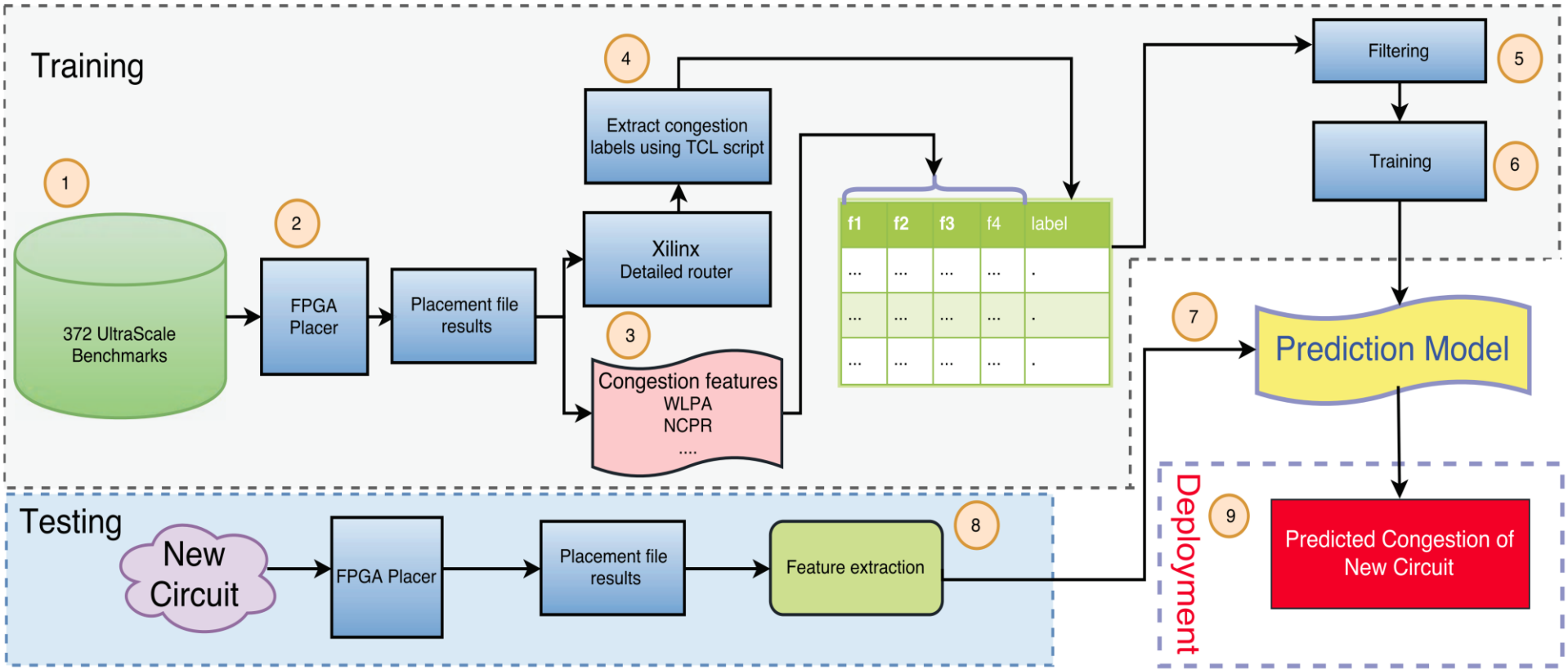
D. Maarouf, A. Alhyari, Z. Abuowaimer, T. Martin, A. Gunter, G. Grewal, S. Areibi, A. Vannelli
School of Engineering/School of Computer Science, University of Guelph
Guelph, Ontario, Canada

- **25% higher prediction accuracy**

  (compared with the state-of-the-art ML congestion-estimation models)

- Same accuracy as congestion estimates using **global router**, but much faster.

What comes next?



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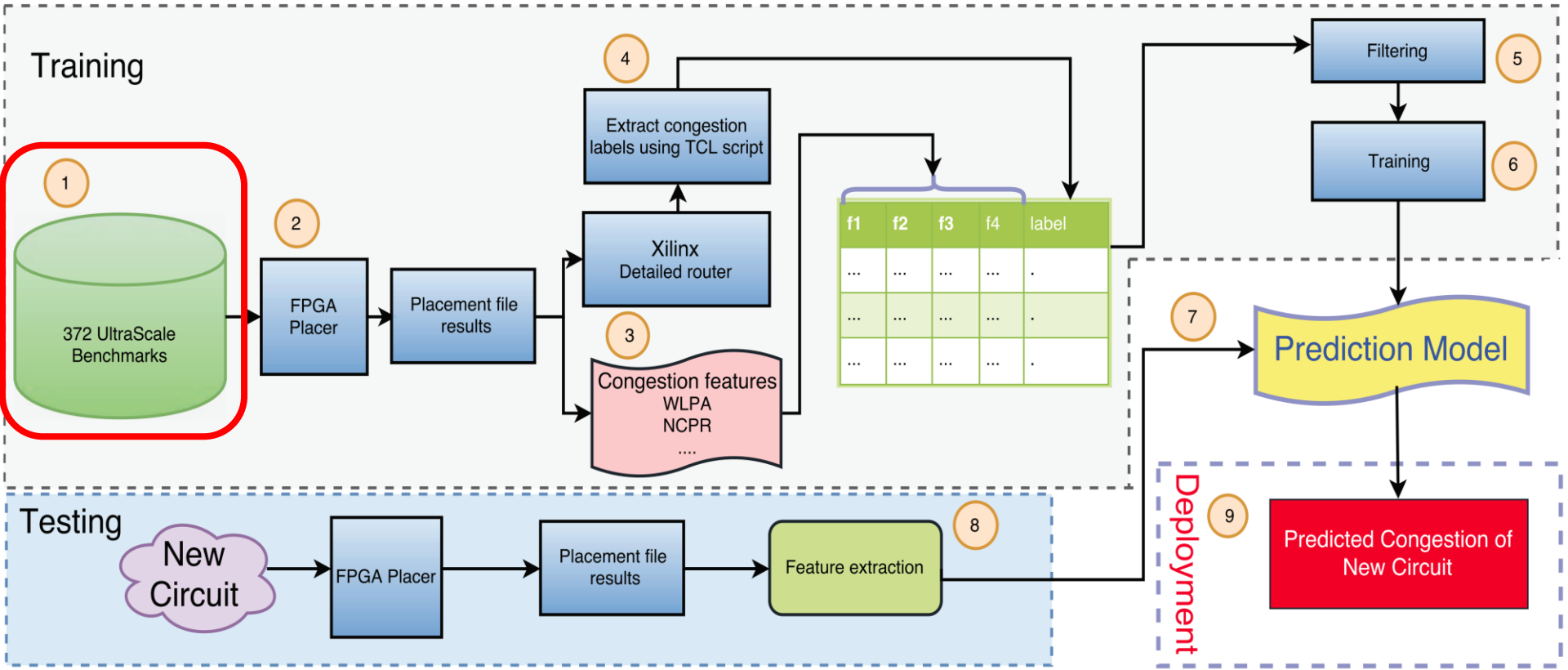

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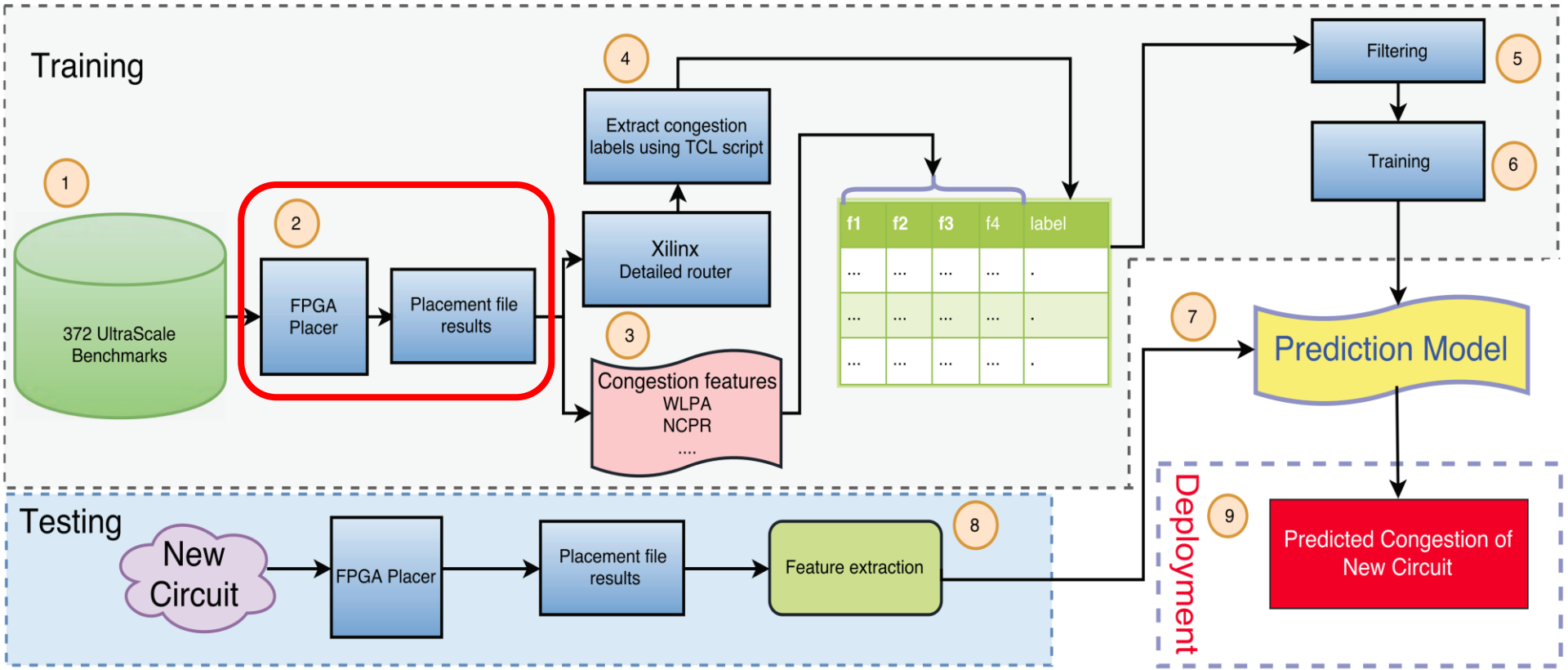

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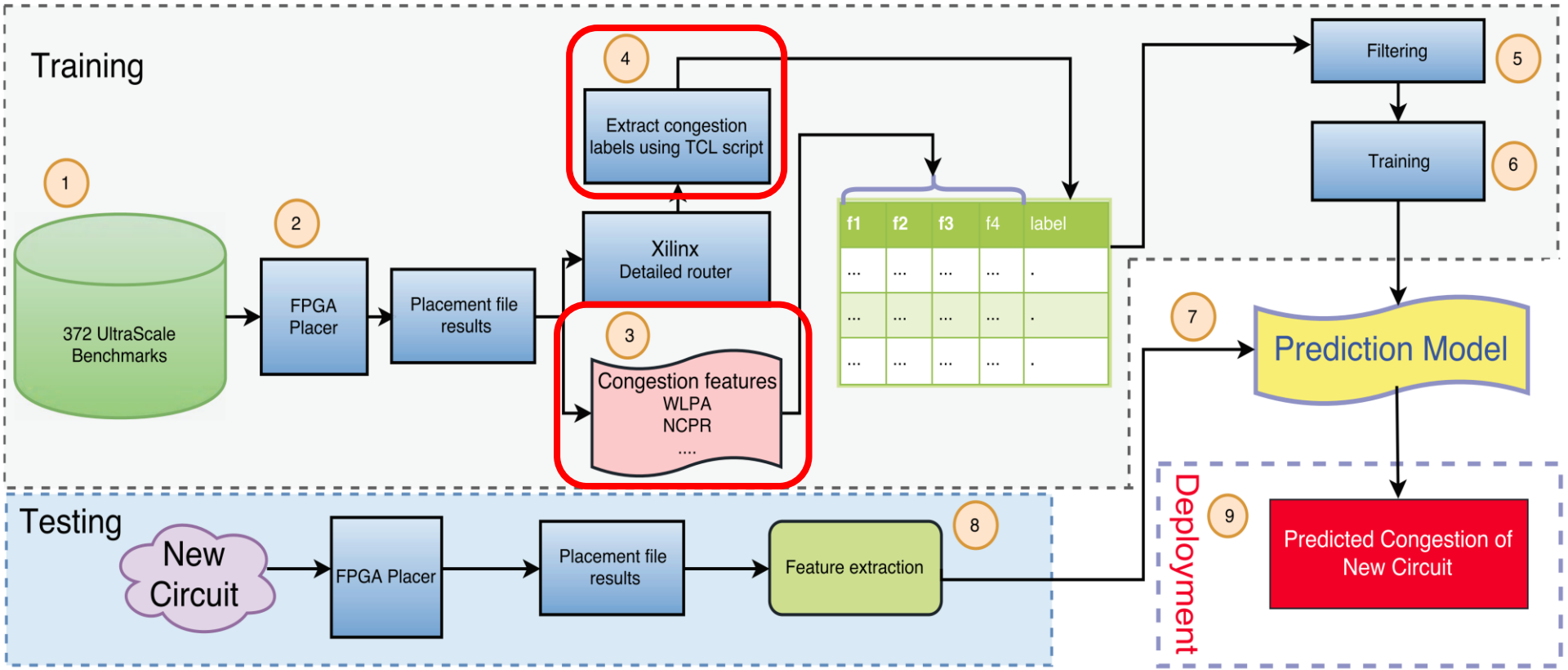

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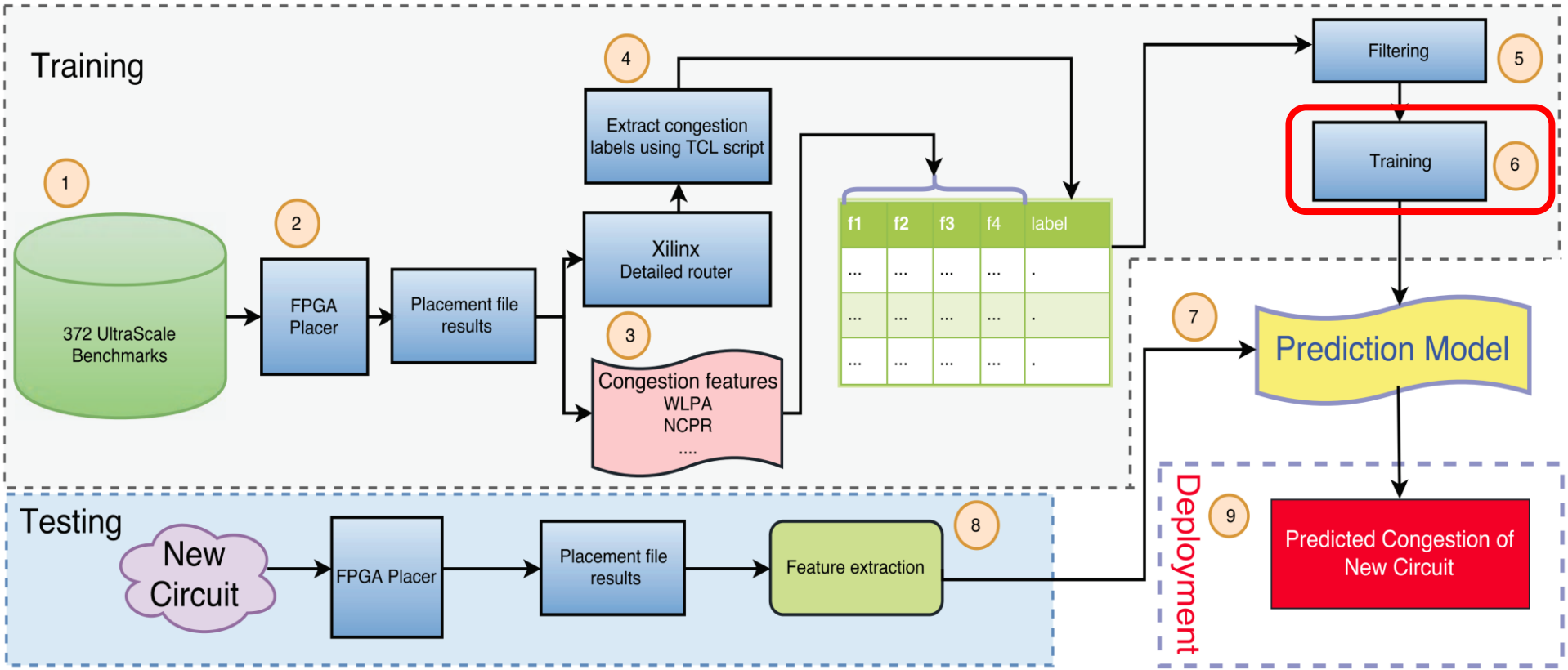

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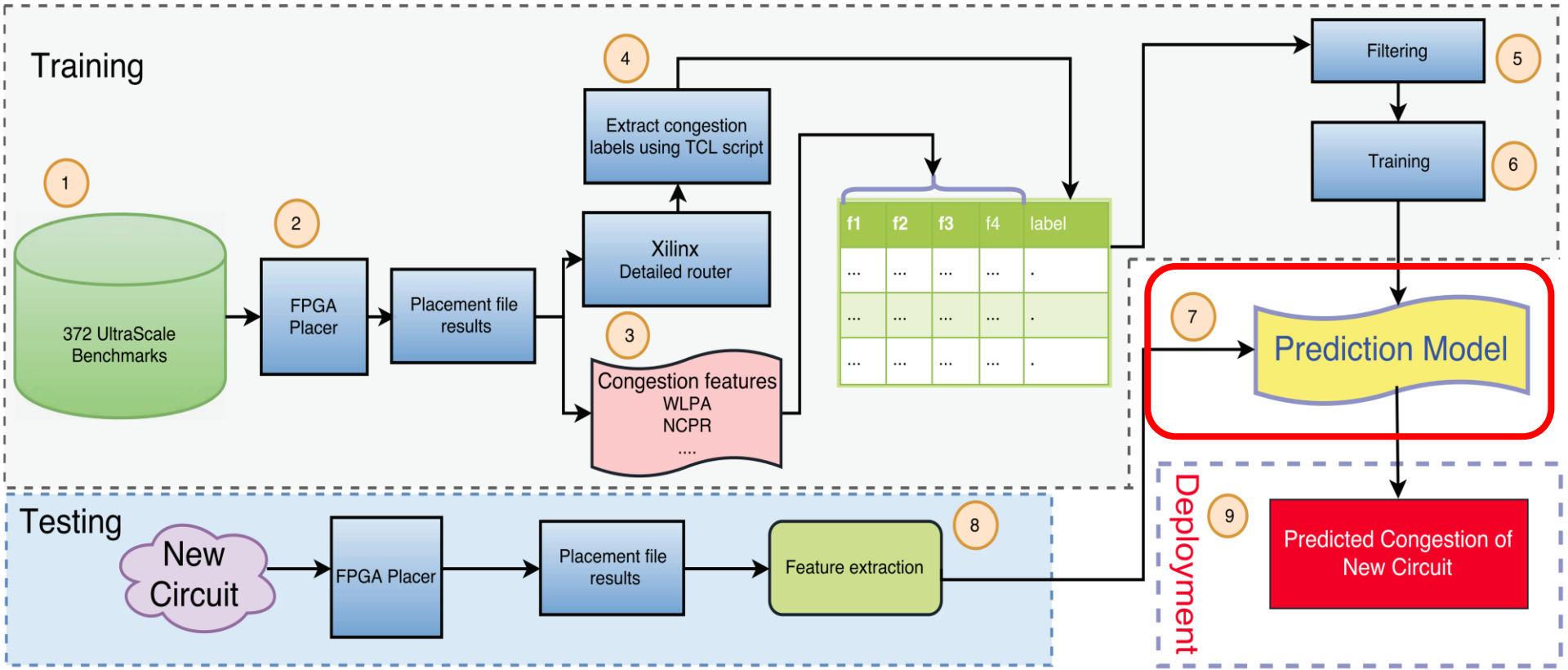

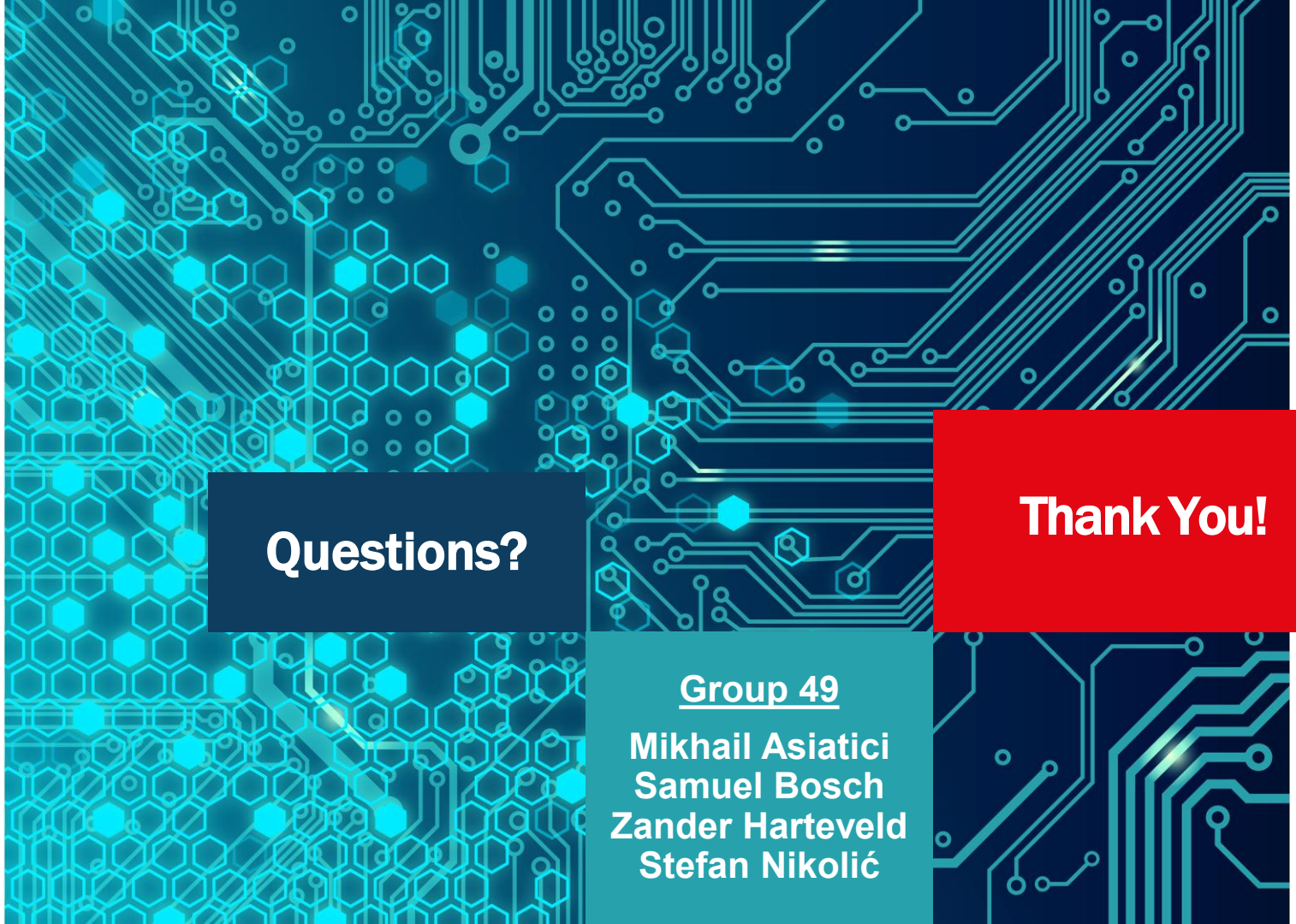

Questions?

Thank You!

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References

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