

Archit Rath

Masters of Engineering Electrical and Computer Engineering

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EDUCATION

M.Eng. Electrical and Computer Engineering,
[University of Ottawa](#)

Jun 2020

GPA: 7.5

Courses: [FPGA Designing](#) [Ethics in AI](#) [Machine Learning Feature Extraction](#) [Software & Product Management](#)

Bachelor of Technology Electronics and Communications Engineering, [G. B. Pant Engineering College, India](#)

Jun 2017

GPA: 77%

Courses: [VLSI & VHDL Design](#) [MRI De-Noiseing](#) [Image Processing](#) [Microelectronics](#)

SKILLS

Programming Languages [C#/C++](#) [Kotlin](#)

Hardware Description Language [Verilog](#) [VHDL](#)

Platforms [Xilinx Vivado](#) [MATLAB](#) [AVR Studio](#) [Unity](#) [Visual Studio](#) [CADENCE](#) [ALTIUM Designer](#) [Adobe Photoshop](#)

EXPERIENCE

Assistant Executive, [iEnergizer Ltd., Noida, India](#)

Dec 2017 → Jul 2018 (8 months)

Focusing on finding solutions for Telecom based grievances for customers for Sprint U.S. Telecom & converting leads/intelligence into sales and signing more customers for our client.

Summer Intern, [Su-Kam Power Systems Ltd.](#)

Jun 2016 → Aug 2016 (3 months)

Manufacturing & PCB testing of solar inverter circuits for 12/ 24 Volt solar panels.

PROJECTS

[Android Game Development](#)

Apr 2020 → now (2 months)

[Gaming](#) [C#](#) [Unity Engine](#) [Visual Studio](#) [Adobe Photoshop](#) [Scripting](#)

Android Game designing using Unity gaming engine creating different sprites and objects. Space exploration game. Adding C# scripting using Visual Studio for functionalities. Object creation and sprite animation using Adobe Photoshop.

[FPGA Verilog Memory Designing](#)

Jan 2020 → Apr 2020 (4 months)

[Verilog](#) [Vivado](#) [Cache Designing](#) [Power system analysis](#) [design optimization](#) [Xilinx](#)

Designed Cache Memory as well as its testbench using Verilog on Xilinx Vivado using Direct Mapping. Power system analysis, clock gating, and pipelining performed for design optimization.

[Research Assistant](#)

Jan 2019 → Dec 2019 (1 year)

[UWB Radar](#) [Data Analysis](#) [Pattern Recognition](#) [Data Classification](#)

Trained system to detect irregular respiration which leads to stroke or heart failure using UWB radar. Performed exploratory data analysis, pattern recognition, and data pipe-lining on time series data to find trends and patterns in respiration variations with the objective to extract relevant features for classification

Final Year Project

Jul 2017 → Jun 2018 (11 months)

MATLAB MRI Image Processing Fuzzy Design Logic Simulink

MATLAB based MRI Image De-Noising filter using Fuzzy Logic Design. Combined Fuzzy Logic with MRI de-noising techniques to better detect brain tumors using MATLAB and Simulink performing better than other methods available for detection.

CERTIFICATIONS

Aerial Robotics, [University of Pennsylvania](#)

Apr 2017

Online course focusing on the mechanics of flight, the design of quadrotor flying robots, and developing dynamic models and synthesizing planners for operating in 3-D environments using programming in MATLAB

Advanced Robotics, [i3Indya Technologies Ltd., India](#)

Jan 2015

Winter training in Embedded System and Robotics focusing on Atmega 16 board projects and its applications. Programming in Embedded C language using AVR Studio 4 and simulations done on Proteus.

Cadence SoC Design in VLSI, [Technical Society of Electronics and Communications Engineering](#)

Sep 2015

Schematic designing and layout of PCB components and performing DRC/LVS checking for design optimization.