Power-Aware Signal Integrity Analysis of DDR4 Data Bus in Onboard Memory Module

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Abstract— **Designing data channels for the DDR4 memory is a challenging due to high data rates of 3.2GB/s per data signal at a low-voltage of 1.2V The coupling of simultaneous switching noise (SSN) in data signals in DDR4 memory modules is a critical signal and power integrity (SI/PI) problem. It is important to catch SI and PI problems at an early stage in design that requires fast and accurate power-aware signal integrity analysis. In this paper, power-aware signal integrity (PI-SI) analysis of data group signals of an onboard DDR4 memory module using power-aware IBIS model is presented. DDR4 power plane and data signals are analyzed using 3D Electromagnetic based PI-SI solver then the transient simulation is performed on combined PI data of power plane and data signals to get simultaneously switching noise (SSN) response of data bus and crosstalk between nearby channels.**

Keywords— ***power integrity; power-aware signal integrity analysis; electromagnetic simulation; channel simulation***

I. INTRODUCTION

Power-Aware signal integrity analysis of DDR4 data bus is necessary for the channel reliability and robustness. In high-speed digital (HSD) boards due to simulation tools limitation, power integrity, and signal integrity analysis are performed separately. The complete data channel performance is the cumulative effect of whole interconnect environment that consists of transceiver ICs, power planes, bond wires, board substrate, data lines and board interconnects that's why it's necessary to consider power plane generated noise effect in data channel signal integrity analysis.

In high-speed digital boards, to reduce the parasitics of the power supply, as well as to increase high-frequency decoupling several power and ground planes are placed in an alternating manner. Data signal lines are routed between these plane pairs. At high-speed it's crucial to characterize both power delivery network and data bus and accurately account the power supply induced jitter to minimize power supply noise in the system. Mainly high-speed design failures are data error rates, cross talk errors, power plane noise coupling to signal causing errors and EMI errors. SI engineers do power-aware SI analysis of channel to ensure proper and reliable operation using Electronic Design Automation tools (EDA) before actual fabrication of board. This reduces board failure chances significantly and also cut production time.

In signal integrity, the main objective is to make sure that transmitted 1s and 0s look like same at the receiver. In power integrity, the main objective is to make sure that the ICs are provided with suitable current to send and receive 1s and 0s. In DDR4 signaling is single ended like DDR3 but data lines have moved closer towards point-to-point interconnect and the interface on the controller side. On the power design front, DDR4 systems use very-low-voltage signaling (1.2V).

II. POWER-AWARE ANALYSIS WORKFLOW

In power-aware SI analysis, the effects of the data signal and non-ideal power and ground planes are considered when analyzing high-speed DDR4 memory interfaces. This paper shows how EDA tool can be used to address power-aware SI challenges associated with DDR4 I/O modeling and interconnect. In power-aware SI analysis, both power plane (PI Analysis) and data signals (SI Analysis) are analyzed. The power-aware SI performance of DDR data bus is evaluated using Keysight's SIPro/PIPro simulation tool.

HSD board presented in this paper is a 12 layer board with 1.2V power distribution networks (PDN) supplying power to DDR4 controller and 5 memory blocks. The main objective of PI-SI analysis is to study the SI/PI effects among DDR4 IO buffers, channel, and DRAM device. The workflow of power-aware signal integrity analysis on HSD layout design is shown in fig. 1. Power plane impedance is optimized within target impedance level using PI analysis of power plane.

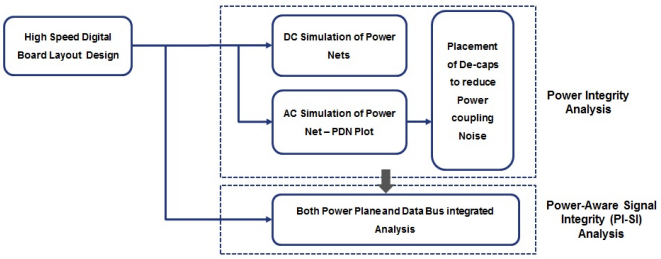

Fig. 1. Power-Aware Analysis workflow

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III. Power Integrity Analysis of DDR4 Power Plane

DDR4 1.2V power plane is used in power integrity analysis. There are 6 I/O devices connected to the 1.2V power plane, controller IC and 5 DDR4 memory blocks as shown in fig. 2.

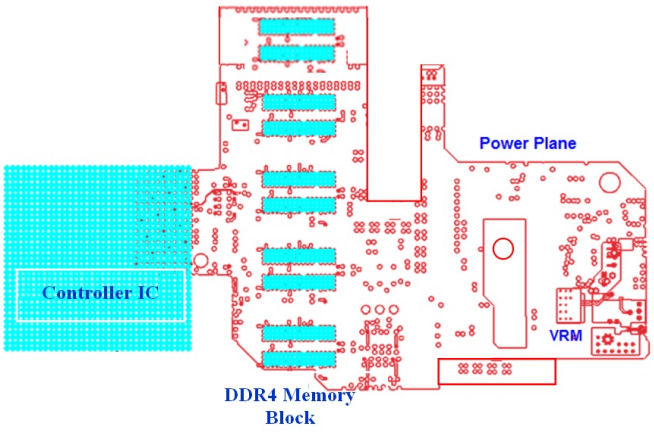


Fig. 2. On Board DDR4 memory blocks and 1.2V power plane

A. DC Simulation

DC-PI guarantees that adequate DC voltage is delivered to all active devices mounted on a PCB. This simulation helps to assure that required criteria for current density in power plane are met. DC-PI is governed by metal resistance and the current pulled from the PDN by each ICs. Voltage distribution of DC PI simulation on power plane is shown in fig. 3.Maximum voltage drop is 36 millivolt that is within 5% allowed tolerance limit.

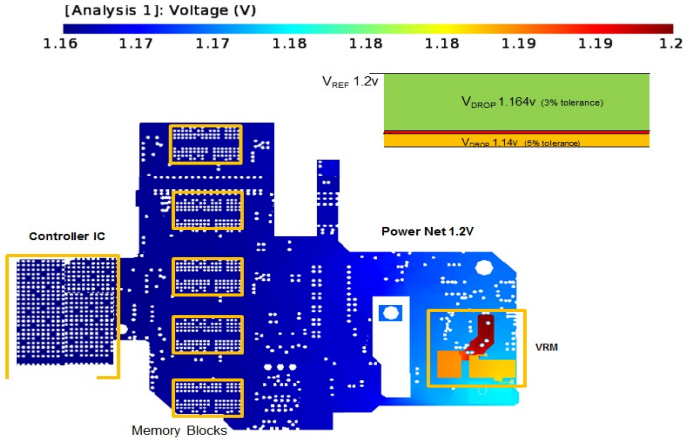


Fig. 3. DC simulation Result of 1.2V Plane showing Voltage distribution on power plane

B. AC Simulation

AC-PI concerns the delivery of AC current to mounted devices to support their switching activity while meeting constraints for transient noise voltage levels within the power delivery network (PDN). The PDN noise margin (variation from nominal voltage) is a sum of both DC IR drop and AC noise. AC analysis is carried out to find out PDN impedance seen from the IC. The voltage regulator module (VRM) provides 1.2V, the IC pulls total 2 Ampere current and a 5% tolerance on the supply voltage is allowed up to around 1GHz. The PDN impedance and target impedance is shown in fig. 4. Target impedance (30 milliohms) is the green dashed line. At higher frequency, the target impedance specification is more relaxed and rises with frequency.

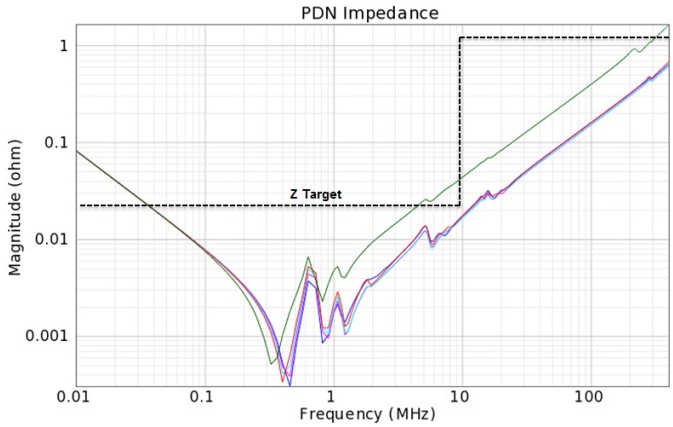


Fig. 4. PND impedance profile of 1.2V power plane

The target impedance is not met above 10 kHz and this will produce voltage ripples. The voltage ripple can be reduced by placing decoupling capacitors. AC simulation gets an effective power solution by iterating capacitor quantity and distribution. After placing 7 decoupling capacitors, the result of target impedance 0.1 Ohms is achieved.

IV. Power-Aware Signal Integrity Analysis

The noise in the power distribution network mainly affects the system jitter performance. This causes degradation in signal quality. The power-Aware signal integrity of DDR4 interfaces, such as inter-symbol interference ISI, reflection, and signal cross talk, needs to be minimized in order to meet an ever shrinking timing budget. SI and PI co-design optimization is driven by both channel performance and overall system cost. For horizontal & vertical transitions, like wire bonds, via array, and solder balls of package and PCB, 3D models were generated for SI/PI simulations combining signal and PDN models together. Combined EM simulated S-parameter result of 16 Data bus lines (DQ lines), 2 differential clock pairs, 2 differential strobe line pairs (DQS) and 1.2 V power plane of DDR4 memory block is shown in fig.5.

EM simulated data is extracted for DDR4 data group signals and combined with power-aware IBIS 5.0 model of controller IC and DDR4 memory in Advance Design System (ADS) for transient simulation. IBIS(Input/output Buffer Information Specification) models are a behavioral model using I-V and V-t look-up tables that make simulations extremely fast. Power-Aware IBIS v5.0 models are used to

represent the non-ideal power effects. There are two BIRDs related to the power awareness of the IBIS v5.0 models.

- BIRD is 95.6: Power Integrity Analysis using IBIS
- BIRD is 98.3: Gate Modulation Effect

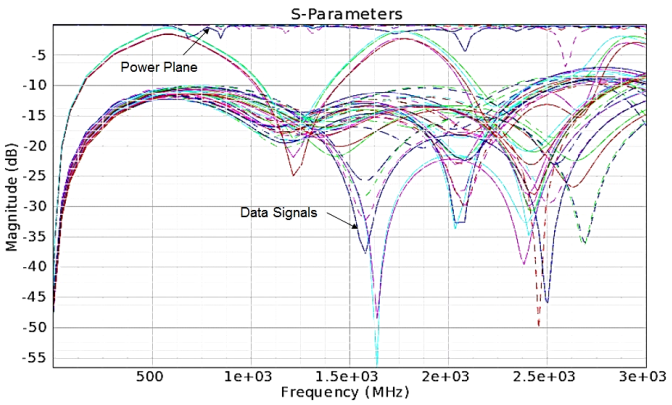


Fig. 5. Extracted DDR4 Data Bus and Power Plane S-parameters from PI-SI

Transient simulation setup for one data signal with IO drivers IBIS model and VRM connected to power plane is shown in fig.6. PI-SI analysis considers the effect of direct interaction between the currents flowing in the PDN and the current flowing through the signal lines.

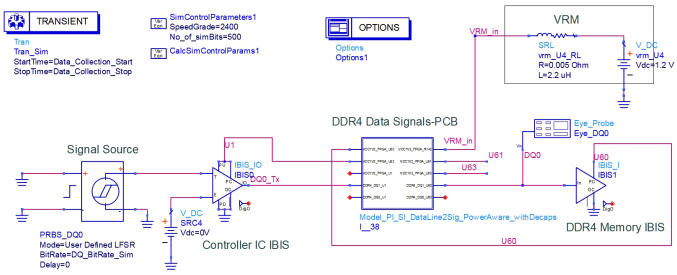


Fig. 6. Transient simulation setup for DQ0 data line using IBIS 5.0 power-aware model

The noise is transferred from one signal line to another as a power-aware IBIS model for the driver is used. The supply current for driving one signal line will cause voltage noise at the power pin of the drivers of the other signal lines what will impact their rise time, this is simultaneous switching noise.

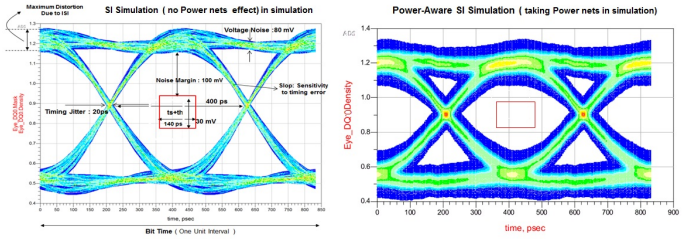


Fig. 7. EYE diagram with and without Power-Aware SI simulation

Eye diagram comparison of DDR4 data bus DQ0 with and without power-aware SI simulation is shown in fig. 7. The eye is more closed in PI-SI analysis because of power plane noise (jitter) that deteriorate signal quality. The bathtub plot is another way to look at jitter and analyze its timing. By plotting BER as a function of sampling position within the bit interval, the bathtub plot represents eye opening versus BER as shown in fig. 8.

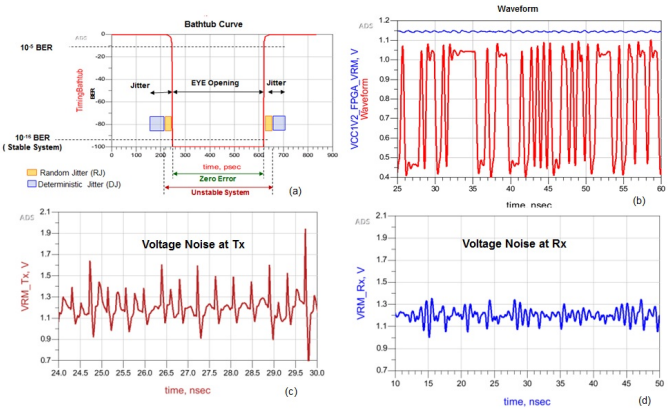


Fig. 8. (a) Bathtub curve plot showing jitters (b) DQ0 data line waveform (c) Voltage noise at controller IC (d) Voltage noise at DDR4 memory

V. SIMULTANEOUS SWITCHING NOISE (SSN) ANALYSIS

Simultaneous switching noise (SSN) is a major component

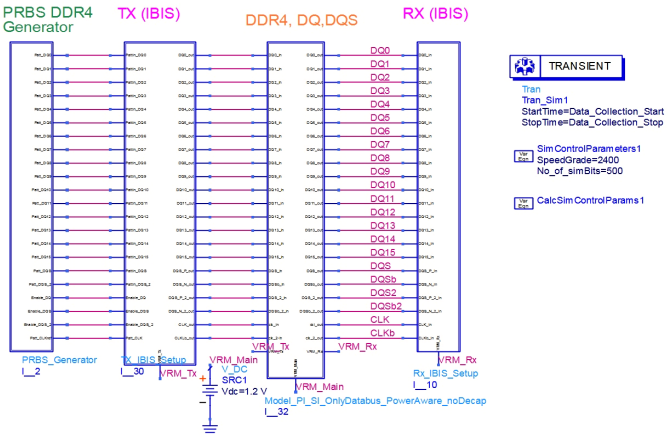


Fig. 9. Transient simulation setup of SSN analysis by exciting all 16 data lines of DDR4 memory

in signal and power integrity analysis. Simultaneous switching noise (SSN) is caused by a number of signals transitioning simultaneously. This causes an instantaneous current demand on the power distribution network as well as the signal's output pad. In SSN analysis, all data signals along with power plane are excited simultaneously. Transient simulation setup of SSN analysis is shown in fig. 9.

Voltage noise on the IO power supply degrades signal timing and operation and SSN is a major cause of power supply noise. Simultaneously Switching increases the ground voltage within the device. This non-zero voltage shift in the ground potential is known as simultaneous switching noise (SSN) or ground bounce. The signal waveform at controller

and memory IC is measured to know timing and voltage degradation as shown in fig.10.

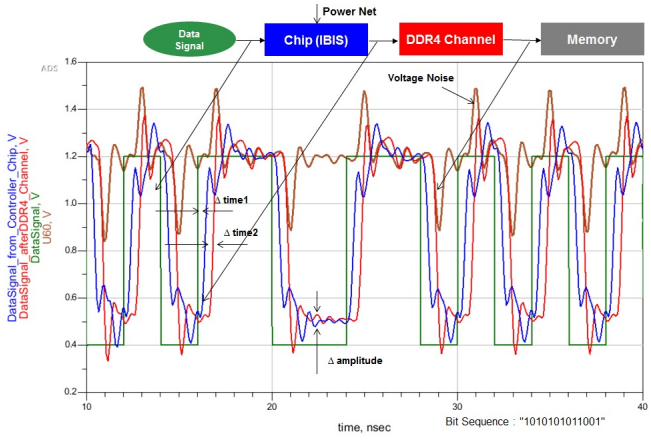


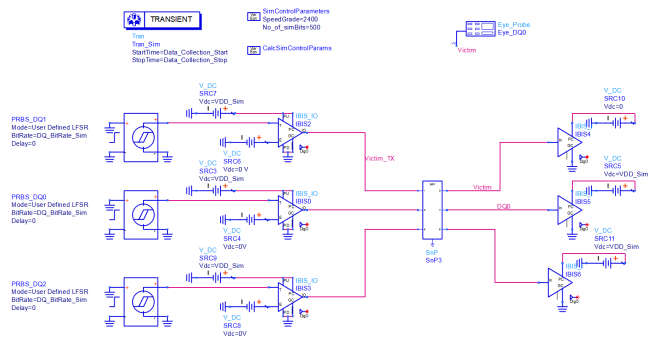
Fig. 10. SSN Analysis Result

VI. DDR4 Data Bus ISI and Crosstalk Analysis

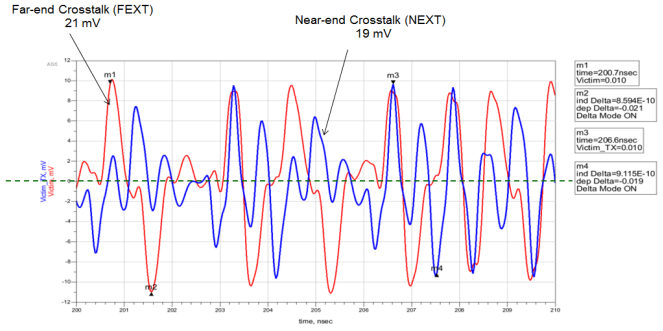
Crosstalk (XT) refers to any condition by which a signal transmitted on one channel creates an undesired effect in another channel. There is two type of crosstalk

a. *Near-end Crosstalk (NEXT)* - is the noise introduced in a channel from a neighboring channel on the same end of transmission lines

b. *Far-end Crosstalk (FEXT)* - is the noise introduced in a channel from a neighboring channel on opposite end of transmission lines



(a)



(b)

Fig. 11. (a) Crosstalk simulation setup (b) Near-end crosstalk (NEXT) and Far-end crosstalk (FEXT) simulation result

In Inter Signal Interference (ISI) simulation, only the victim data signal is transmitting while all other data signals are kept quiet. In crosstalk analysis, all data signals are transmitting but aggressor and victim lines transmit different data patterns. In DDR4 where multiple active lines switch simultaneously, crosstalk can induce power/ground noise. Crosstalk simulation setup on 3 nearby data signals DQ0, DQ10, and DQ11 are shown in fig. 11(a). Here DQ11 is victim signal while DQ0 and DQ10 are aggressors. Fig. 11(b) shows Far-end Crosstalk (FEXT) value 21 mV and Near-end Crosstalk (NEXT) value 19 mV that is within an acceptable limit of DDR4 data signaling.

VII. Conclusion

In this work power-aware signal integrity analysis of a 12 layer, onboard DDR4 Data bus is presented. DC and AC simulation are performed in SIPro/PIPro to know maximum voltage drop and PDN impedance profile. DDR4 1.2V power plane and data signals are analyzed using 3D electromagnetic based PI-SI solver then the transient simulation is performed by using power-aware IBIS 5.0 models to know the actual value of power plane noise introduced in the data signal. The coupling of simultaneous switching noise (SSN) in data signals in DDR4 memory modules analyzed by exciting all the 16 data lines simultaneously. Crosstalk for 3 nearby data signals is analyzed using power-aware IBIS models.

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