Day - 3

Switches → Tristate inverter

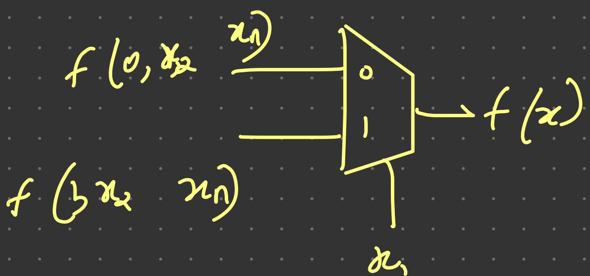
↳ Implement comb, seq circuit

↳ 2x1 MUX

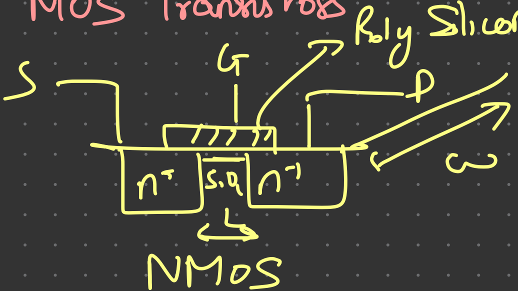
SHANNON'S EXPANSION [Can be done for multiple variable]

$$f(x_1, x_2, \ldots x_n) = \bar{x}_1(0, x_2, x_3 \ldots x_n) + x_1(1, x_2 \ldots x_n)$$

$$S(A,B) = \bar{A}\,S(0,B) + A\,S(1,B)$$



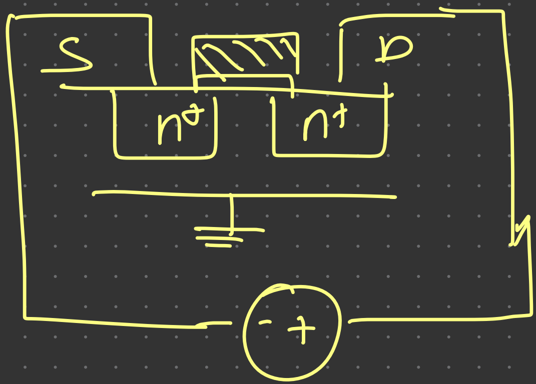
MOS Transistors



Cross-Sectional View

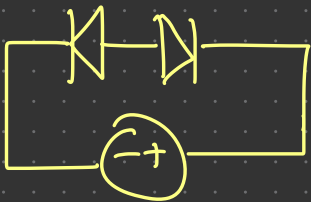
Top View

MOS Operation



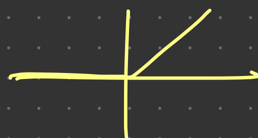
Back to back connected,
No voltage at gate

→ Current governed by reverse diode

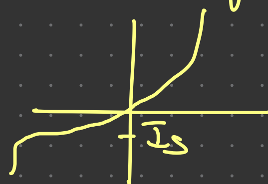


$I_D \cong 0$

Ideally 0



Realistically



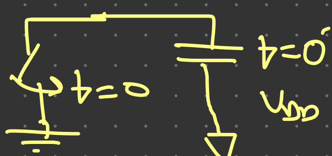
$$I_D = I_s\left(e^{V_D/nV_T} - 1\right)$$

↓

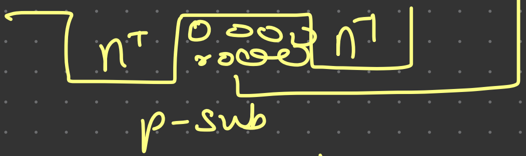
Reverse Saturation Current

↓

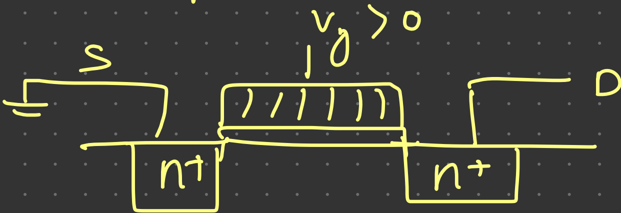
Leakage Current



To have sufficient conduction



→ If, it creates a conductive path, then we can have a meaningfull current flow

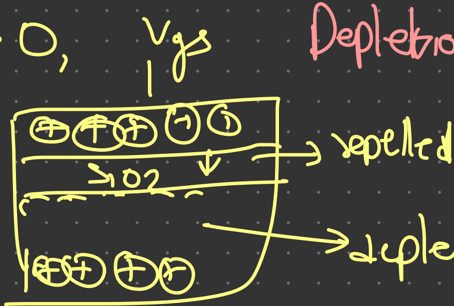


→ If $V_{gs} < 0$, try to induce -ve charge in top holes [+ve] gets accumulated beneath gate called

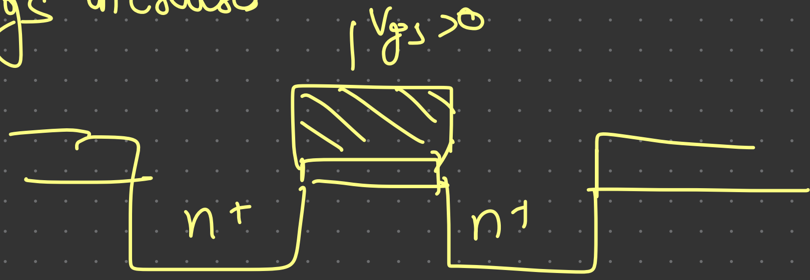
accumulation mode

→ If $V_{gs} > 0$,

Depletion Mode



→ V_{gs} increases



n^+ regions supply electrons and tries to invert behaviour by making inversion layer

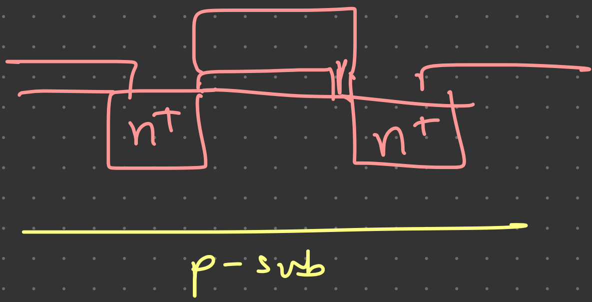
Inversion Mode

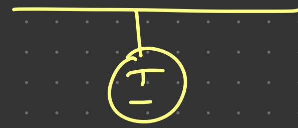
Inversion → Weak Inversion

Inversion → Strong Inversion [Minor carrier conc = Majority carrier conc in channel

p-sub = Electrons are minor

⇒ Threshold Voltage → Channel is complete formed in strong inversion when $V_{gs} > V_{tn}$





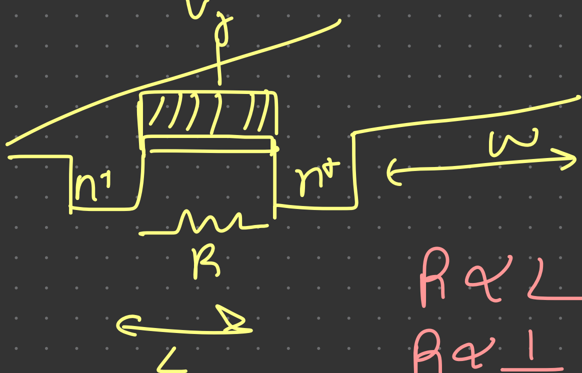
→ Bulk connected to ground

→ Bulk ~~not~~ connected to voltage [oppose as there would be lesser -ve charge]

→ $V_{BS} > 0$

→ $V_{BS} < 0$

V_{th} is a function of V_{SB}

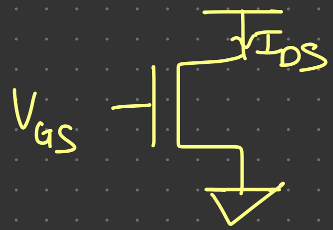


$R \propto L$

$R \propto \frac{1}{W}$ as $R = \frac{\rho L}{A}$

By using wider transistors, we can conduct more current if other constraints are okay

Channel can act as resistor controlled by gate voltage [V_{gs}]



VCCS

$$\begin{cases} V_{gs} < 0, & I_D \cong 0 \\ V_{gs} > 0, & I_{DS} = \text{finite} \end{cases}$$

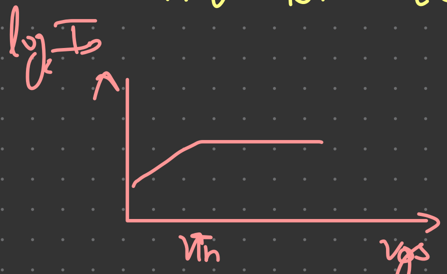
MOSFET: Voltage Controlled Current Source

Accumulation: $V_{GS} < 0$

Depletion: $0 < V_G << V_T$

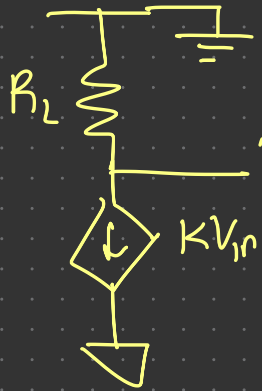
Sub Threshold

Inversion Mode:
- Weak: $0 < V_g < V_T$
- Strong: $V_{GS} > V_T$



$I_D \approx I_0 e^{V_{GS}/\eta V_T}$

Transconductance $= \frac{I}{V}$ for small voltage we can get high current if trans is high



→ NMOS modes of op^n w.r.t V_{DS}

① $V_{GS} < 0$, for any finite V_{DS}, $I_{DS} \approx 0$

Cutoff Region

② $V_{gs} > V_{Th}$ and finite V_{DS} $[V_{DS} > 0]$

There will be electric field

$E = \frac{V_{DS}}{L}$ with

force on charge carrier

On an average they drift from one side to another called <u>drift velocity</u>

$$V_d = \mu E = \mu \frac{V_{DS}}{L}$$

$\mu \downarrow$ ability to move in medium [Mobility]

poly silicon
SiO_2
n channel
} Parallel Plate Capacitor

$dQ =$

C_{ox} = Capacitance per unit area

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_0}{t_{ox}} = fF/\mu m^2$$

$t_{ox} \downarrow$ order of few nm

$\varepsilon \downarrow$ permittivity

$$dQ = C_{ox}(W\,dx)(V_{GS} - V_{th} - V_x)$$

$$I_{DS} = \frac{dQ}{dt} = C_{ox} W (V_{gs} - V_{th} - V_x) \frac{dx}{dt}$$

$$\frac{dx}{dt} = V_d = \mu E(x) = \mu \left(\frac{-dV}{dx} \right)$$

Field

$$\int_0^L I_{DS}\, dx = \mu C_{ox} \frac{W}{L} \left[(V_{gs} - V_{th}) - \frac{V_{DS}}{2} \right] V_{DS}$$

$$I_{DS} = \mu C_{ox} \left[\frac{W}{L} \right] \left[\underbrace{(V_{gs} - V_{th})}_{\text{Overdrive Voltage}} V_{DS} - \frac{V_{DS}^2}{2} \right]$$

If $V_{GS} > V_{tn}$ $\quad V_{DS}$

If $V_{DS} \ll V_{gs} - V_{tn}$, second term $\frac{V_{DS}}{2}$ can be ignored

Linear Mode of Operation

$$I_{DS} \approx \mu C_{ox} \left[\frac{W}{L} \right] (V_{GS} - V_{tn}) V_{DS}$$

R

$$R = \frac{1}{\mu C_{ox} \left(\frac{W}{L} \right) [V_{GS} - V_{tn}]}$$

Cutoff : $V_{GS} < 0$

Linear : $V_{GS} > V_{th}$, $V_{DS} < V_{GS} - V_{tn}$

$$V_{GD} = V_{GS} - V_{DS} = \underbrace{V_G - V_D}_{\text{Common Reference}}$$