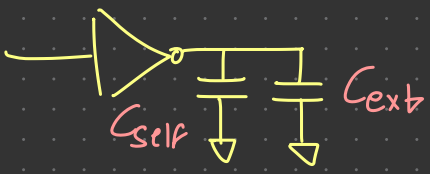
Day-11 18th Feb



Delay of inverter $\propto \left[\frac{C_{ext}+C_{self}}{C_{in}}\right]$ as $\frac{K \cdot \tau}{C}$ or

$$\text{Delay} = \left[g\frac{C_{ext}}{C_{in}} + p\right]\tau_{real}$$

- p → Due to parasitic components
- g → Constant defined as logical effort of gate
- $\frac{C_{ext}}{C_{in}}$ → Constant for given technology
  - ↳ Electrical effort (h)

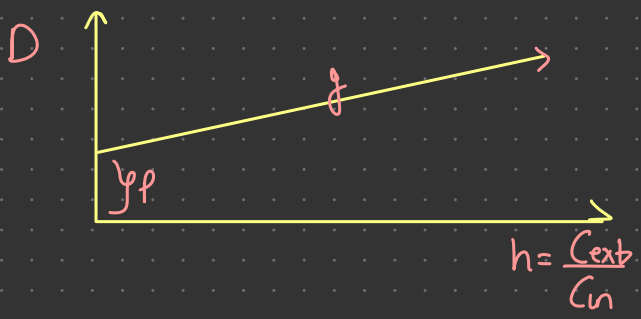
$$\text{Delay} = (gh + p)\tau_{real}$$

↳ Time unit

If we know p, we can find τ_{real}

for simplicity,

$D = gh + p$ in tune units



g = Logical effort parameter

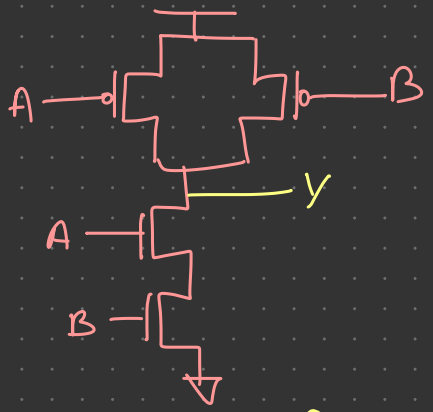
↳ Ratio of input capacitance of gate and input capacitance of inverter

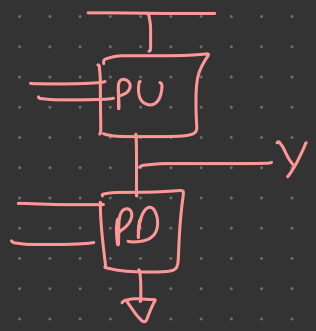
for example:

① Logical effort of inverter = 1 as input cap of inverter w.r.t itself is 1

IMP ② Find logical effort of NAND etc

Example:



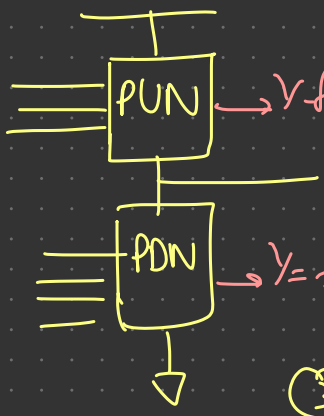


NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$Y = \overline{AB} = \bar{A} + \bar{B}$

Method to design any CMOS Logic:



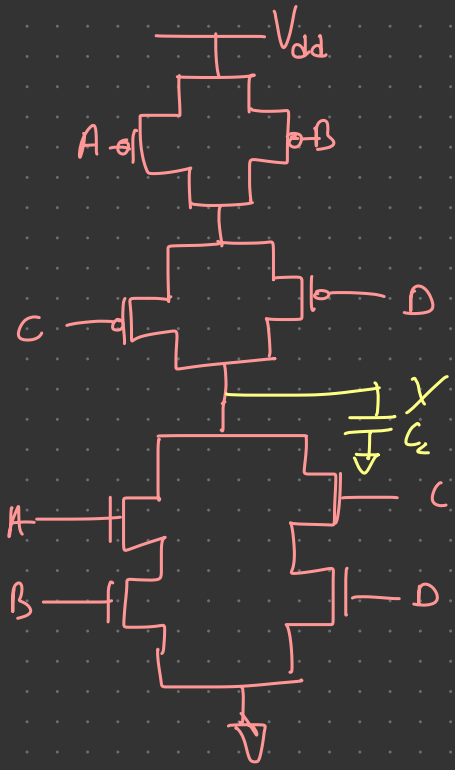
① For designing pull-up network, write Y as a function of complement of input variable

② For pull down, write Y as a function of input variables

③ For AND → Use series
OR → Use parallel

Example:

$$Y = \overline{AB + CD} = \overline{AB} \cdot \overline{CD}$$
$$= (\bar{A} + \bar{B})(\bar{C} + \bar{D})$$



Just structure is not sufficient, we need to decide their sizes of each of the transistors

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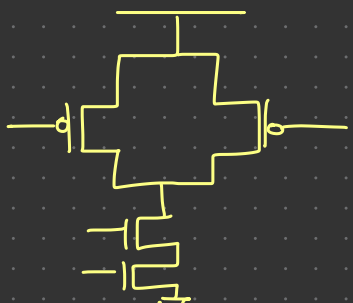
For a NAND Gate,



We can always compare performance of gate with the inverter

We need $\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$

Generally the above ratio is 2, then we will have equal noise margins, all other parameters would be the same too

$C_{in} \propto 3W \rightarrow$ [2W for PMOS, 1W for NMOS]

In pull down, current to discharge will depend on NMOS ie proportional to W

In pull up current to charge will depend on PMOS ie proportional to 2W

In pull down, if these 2 transistors, we still want to mimic inverter i.e W So their respective widths should be 2W → each MOSFET

↳ So the equivalent would be W as it acts like a resistive network in the linear region

$R \propto \frac{1}{W/L}$

For parallel we usually take both worse case scenarios

Best Case
↳ Both can be ON same time

Worse Case:
↳ Only 1 can be ON same time

So, we should have each MOSFT with 2W to account for worse case scenario to maintain the ideal inverter type characteristics

$$LE_{Gate} = \frac{C_{in\,gate}}{C_{in\,inverter}}$$

For 2-input NAND Gate,

$$LE = \frac{4W}{3W} = \frac{4}{3}$$

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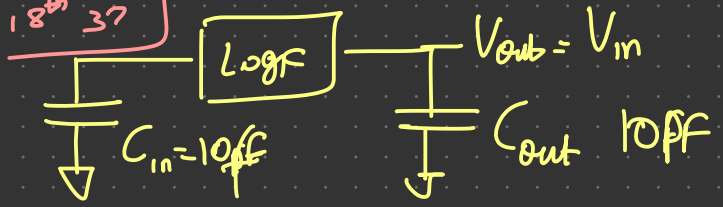
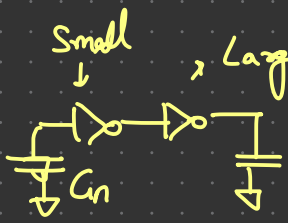


Solutions :

① Small → Large enough



Design for minimum delay

$$D = \sum_{i=0}^{N-1} h_i + N p$$

$$H = \frac{C_{out}}{C_{in}} = \frac{10p}{10f} = 10^3 = h_1 \times h_2 \quad h_{n-1}$$

Q We want to minimise delay by taking algebraic inequality

When $h_1 = h_2 = h_{n-1} = x = H^{1/N}$

Each stage will have same Electrical effort

↳ Also called stage effort

$$N = \frac{\ln H}{\ln x}$$

In the original expression,

$$D = \sum h_i + n\rho$$

$$D = Nx + N\rho$$

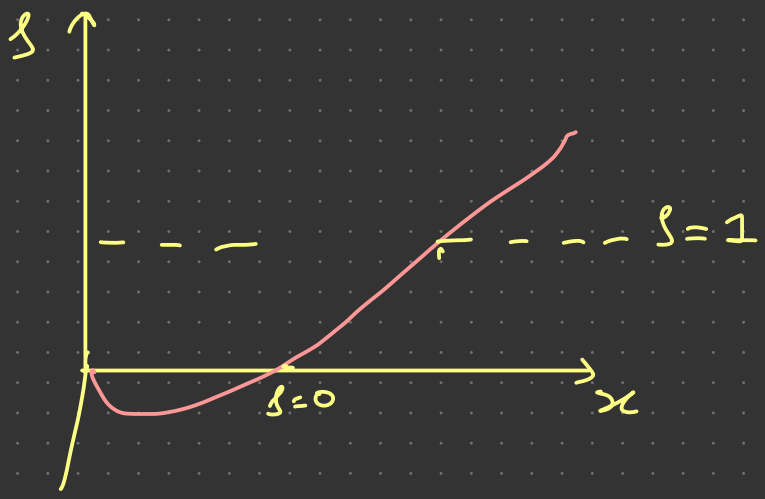
$$\boxed{D = \frac{x \ln H}{\ln x} + \frac{\rho \ln H}{\ln x}}$$

→ Function in terms of x ↳ Stage Effort

$$\frac{\partial D}{\partial x} = \frac{\partial}{\partial x}\left[(x+\rho)\frac{\ln H}{\ln x}\right]$$

$$\frac{\partial D}{dx} = \frac{\ln H}{\ln x}\left[1 - \frac{x+\rho}{x \ln x}\right] = 0$$

$$\boxed{x \ln x - x = \rho}$$



When $S=0$, $x = e = 2.73$

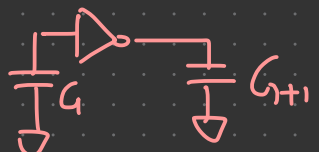
$S = 1$, $x = 3.59$

S = Parasitic delay of inverter that's constant for a given technology

$S = \frac{C_{self}}{C_{in}}$ is known so x value can be found for optimal delay

For $S=1$,

$\text{Stage effort } = \frac{C_{L+1}}{C_i}$



↳ Approximated to 4 So in standard library Fan-out of 4 is used

JMP → Next stage will be scaled up by value of 4

If $H = 10^3$

Delay :

$$N = \frac{\ln H}{\ln x} = \frac{\ln(10^3)}{\ln 4} \approx 5$$

So, To drive we need 5 stages but output will be inverted we use 4 or 6

$$\text{Delay} = NH^{1/N} + Np$$

$$D = 5(10^3)^{1/5} + 5p$$

$$D = 5(1000)^{1/5} + 5p \approx (19.5 + 5p) \text{ units}$$

For $N = 4$,

$$D = 4(1000)^{1/4} + 5p \approx (22.49 + 4p) \text{ units}$$

For $N = 6$,

$$D = 6(1000)^{1/6} + 5p = (18.97 + 6p) \text{ units}$$

On comparison, lower number of stages doesn't always imply lesser delay

① Can this method be used for all cases?

② Brandeburg case can this be used?