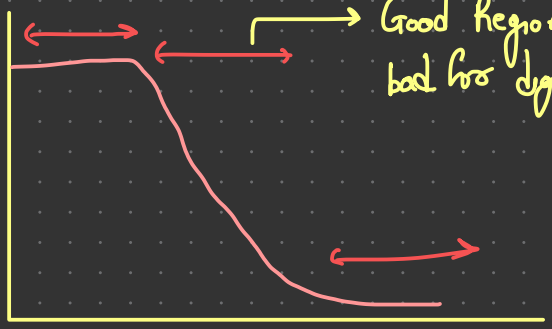
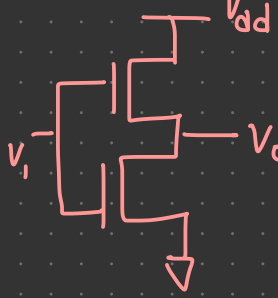
# Day 8- 1st Feb



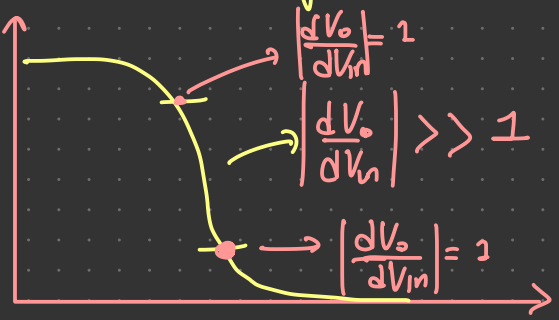
→ Good Region for analog amplifier but bad for digital circuits

Left, Right Most ends are good for digital circuits



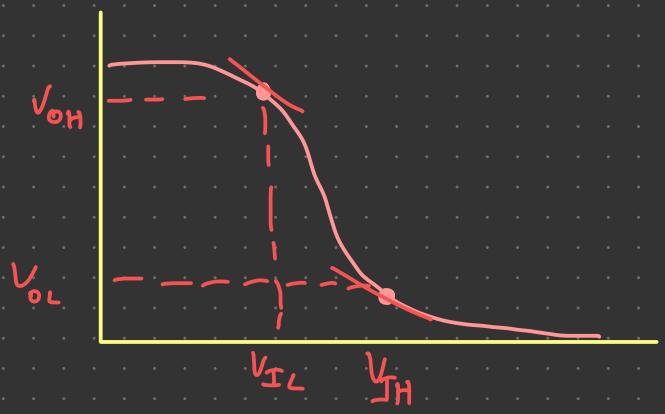

→ Can act as analog inverting amplifier or digital inverter

Parameters defining regions of VTC:




→ Noise Margins gives robustness from the noise appearing

Noises can occur due to metal resistances etc so voltage levels can differ affecting performance of gate




- $V_{IL}$ = Max I/P voltage considered low for which O/P is high
- $V_{IH}$ = Min I/P voltage considered high for which O/P is low
- $V_{OH}$ = Min O/P voltage considered high
- $V_{OL}$ = Max O/P voltage considered low


$V_{IH} \leq V_B \leq V_{OH} \Rightarrow V_C \rightarrow$ Close to 0 logic

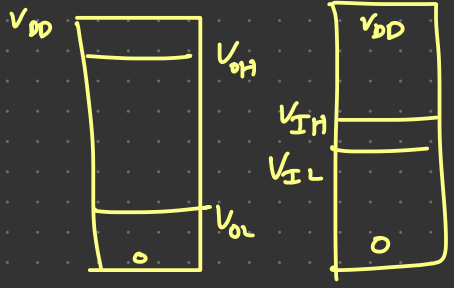
↓ Indicates high value

$NM_H = V_{OH} - V_{IH}$
↳ Noise Margin for high level

$NM_L = V_{IL} - V_{OL}$
↳ Noise Margin for low level

→ If within this range then certainly low output
If not, then can't determine

→ Opposite of $NM_H$'s scenario




Ideally we maximise noise margins

Next & Derivations of noise margin parameters done in Assignment

$$V_{IH} = \frac{5V_{DD} + 3V_{tn} - 5|V_{tp}|}{8} \qquad V_{OH} = \frac{7V_{DD} + |V_{tp}| + V_{tn}}{8}$$

$$V_{OL} = \frac{V_{DD} - V_{tn} - |V_{tp}|}{8} \qquad V_{IL} = \frac{3V_{DD} + 5V_{tn} - 3|V_{tp}|}{8}$$

$$NH_H = V_{OH} - V_{IH} = \frac{V_{DD} + 3|V_{tp}| - V_{tn}}{4}$$

$$NH_L = V_{IL} - V_{OL} = \frac{V_{DD} + 3V_{tn} - |V_{tp}|}{4}$$

If $V_{tn} = |V_{tp}|$,

$NM_H = NM_L = \frac{V_{DD} + 2V_T}{4}$

Ideally we want equal noise margins as output of one inverter is input for next stage

To increase noise margins for a fixed $V_{DD}$,

↳ Change higher $V_T$ transistors → Current drawn will reduce

↓

Speed reduces as it depends on how fast cap charges

## Dynamic characteristics



$$t_{pd} = \frac{t_{pdr} + t_{pdf}}{2}$$

$t_r$ = Rise time → O/P: 0 to $V_{OH}$

$t_f$ = Fall time → O/P: $V_{DD}$ to $V_{OL}$