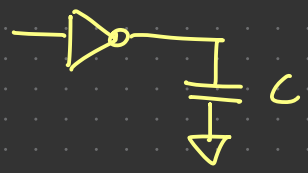
Day10 - 15th Feb

Dynamic Characteristics:

$$\frac{K\varphi}{C} = \text{const} = f$$

$$K = \mu C_{ox}\left[\frac{W}{L}\right]$$



If K is fixed, inverter size is fixed

① Increasing capacitance will increase the delay

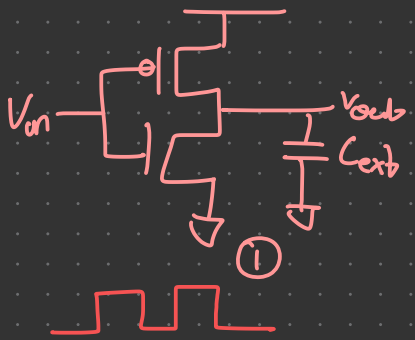
↓

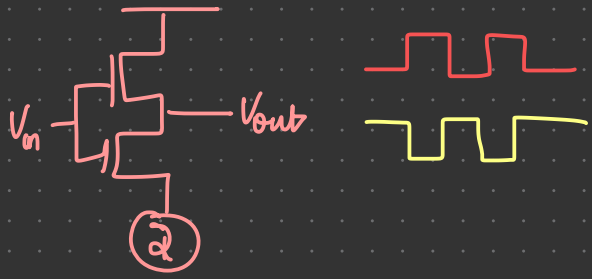
Inverter RC ↑ → Time constant ↑ → Delay ↑

② For increased cap, if we don't want delay to change then we can adjust sizes of capacitor

As $\frac{K\gamma}{C}$ = constant Keeping one term constant we can check the proportionality for any two variables

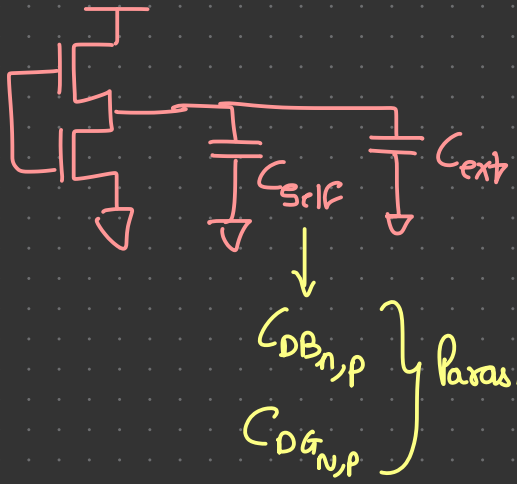
Ideally delay can be made 0 but not practical





In ②, without capacitance C_{DB_N}, C_{DB_N} parasitic cap will be present, so they will store if no external cap

So, self capacitance will always be present → calculated from AS, AD, PS PD



So, even if $C_{ext} = 0$, C_{self} will always be there

$$\zeta \propto \frac{C_{out}}{K} \Rightarrow \zeta \propto \frac{[C_{self} + C_{ext}]}{K}$$

$$K = \mu C_{ox}\left[\frac{W}{L}\right] \Rightarrow K \propto \left[\frac{W}{L}\right]$$

$$C_{in} \propto [W]$$

$$C_{in} = \underbrace{C_{GS_n} + C_{GS_p}}_{C_{GD_n} + C_{GD_p}}$$ → Depends upon MOSFET's operation in saturation

↳ Check in previous lecture

We can infer $\boxed{K \propto C_{in}}$

$$\delta = \frac{C_{ext}}{C_{in}} + \frac{C_{self}}{C_{in}}$$

Will always be a constant

$$\delta \propto \left[\left(C_{ext} + \delta\right)\right]$$

→ Intrinsic delay (or) Parasitic delay

→ Remains constant irrespective of CMOS widths as though sizes are increasing, current carrying capability increases too Hence delay is constant.

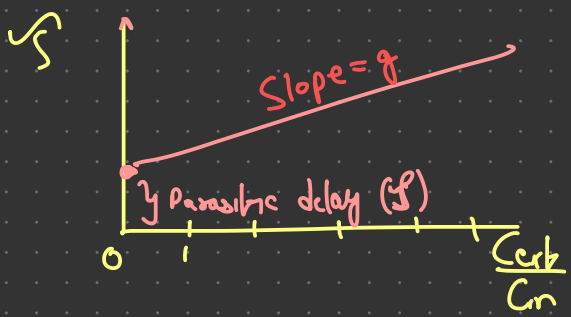
$$\delta = \left[g\frac{C_{ext}}{C_{in}} + \delta\right]$$

$h \rightarrow$ Electrical effort of logical gate

↓

Gives measure of effort gate in doing

$$\delta = gh + \delta$$



g = Logical effort

$$\delta \propto \frac{C_{ext}}{C_{in}\uparrow} + \frac{C_{self}\uparrow}{C_{in}\searrow \text{ Constant}}$$

In extreme case, to minimise delay we may want to increase size → then C_{in} becomes soo large that $C_{self} >> C_{ext}$

↳ $\delta \propto f$ then δ becomes independent of size So it can't be reduced further

Check calc example in 057

IMP →

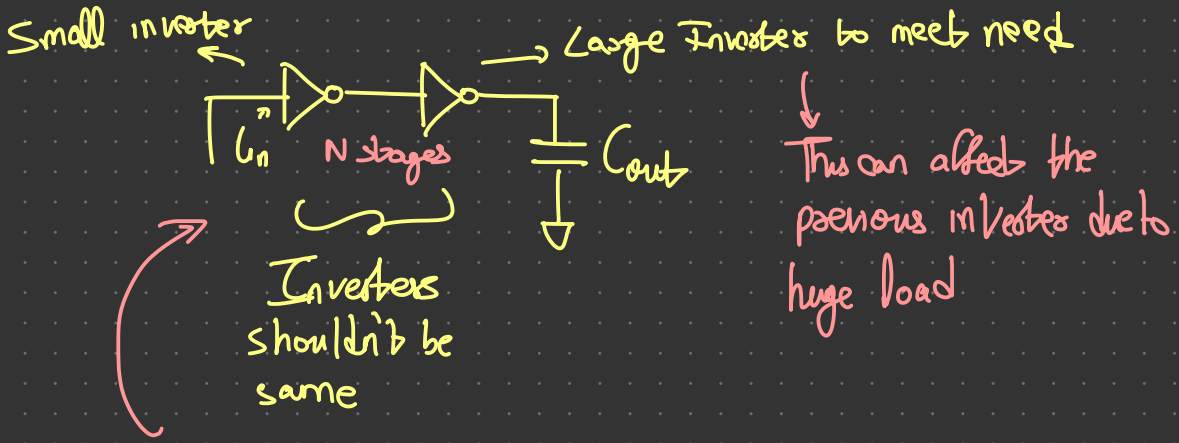
In multiple branches, we can't blindly keep increasing size as it increases C_{in} ⇒ increases load on previous stages

To drive high capacitive load with least delay possible:

$C_L >> C_{in}$ → Size can't the solution

→

Design based question in the end



Tapered Buffer