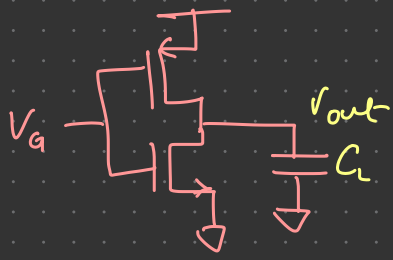
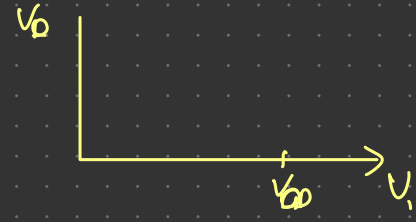
CMOS Inverter:



Transfer:



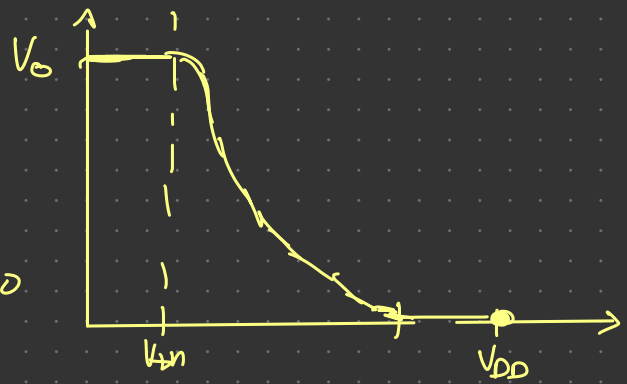
Wire capacitance [0 04]

Self Capacitance:

↳ At Cout node, cap is due to inverter due to which its drain of both NMOS, PMOS

$$C_L + C_{wire} + C_{self-cap}$$

↳ Parasitic



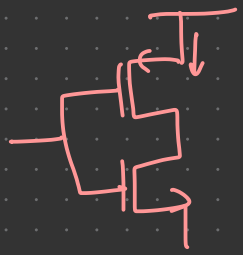
width
0 9 00

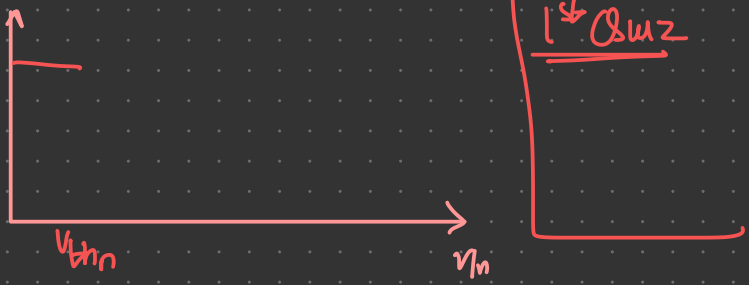
For PMOS to turn ON
$V_{gs_p} < V_{T_p}$

① $0 < V_i < V_T$ NMOS off, PMOS ON $V_o = V_{DD}$

② $V_{DD} - |V_{Tp}| < V_i < V_{DD}$ NMOS ON, PMOS off $V_o = 0$

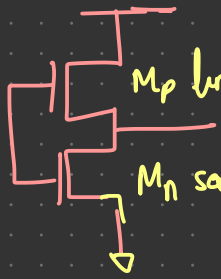
③ $V_i > V_{Tn}$, NMOS ON → Saturation
PMOS ON → Linear Region





$V_i > V_{tn}$:

NMOS: Sat
PMOS: Linear
} There will be a current drawn from supply to ground when $V_i > V_{tn}$



$I_{dn} = |I_{dp}|$

$I_{dsp} = K_p \left[(V_{SG_p} - |V_{tn}|) V_{SD_p} - \frac{1}{2} V_{SD}^2 \right]$

$K_p \rightarrow \mu_p C_{ox} \left[\frac{W}{L}\right]_p$

$I_{dsn} = \frac{K_n}{2} [V_i - V_{tn}]^2$

On simp of I_{dsp},

$$I_{dsp} = K_p\left[(V_{dd} - V_i - |V_{thp}|)(V_{dd} - V_o) - \frac{(V_{DD} - V_o)^2}{2}\right]$$

On solving equality, we get quadratic equation.

$$K_p\left[(V_{DD} - V_i - |V_{tp}|)x - \frac{x^2}{2}\right] = K_n\left[V_i - V_{thn}\right]^2$$

$$\downarrow$$

$$V_{DD} - V_o = x$$

$$\frac{x^2}{2} - x(V_{DD} - V_i + |V_{tp}|) + \frac{1}{2}(V_i - V_{tn})^2 = 0$$

↳ Assumed $K_n = K_p$

$$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

↳ We get +, − but we choose whichever satisfies mode of operation

On simp,

$$V_o = (V_i + |V_{tp}|) + \sqrt{(V_{DD} - V_{thn} - |V_{tp}|)(V_{DD} - 2V_i + V_{thn} - |V_{thp}|)}$$

↳ For $V_i \leq \left[\frac{V_{DD} + V_{tn} - |V_{tp}|}{2}\right]$

Both should be ≥ 0

Negatives don't hold as not possible assumption

Conditions for above:

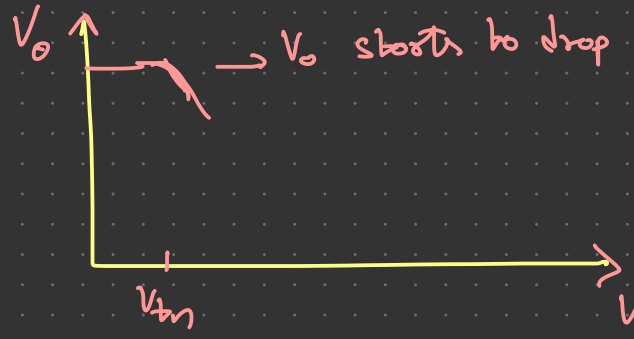
$$V_{DD} - V_{tn} - |V_{tp}| \geq 0$$

$$V_{DD} - 2V_i + V_{tn} - |V_{tp}| \geq 0$$

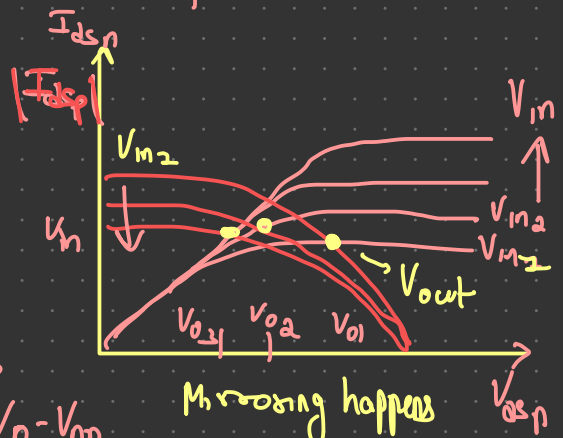
→ Condition on lowest value of V_{DD} that can be used

$$V_{DD_{min}} \geq V_{tn} + |V_{tp}|$$

Now when V_i is increased, we discuss next region



Device's mode of operation:



As $V_{in} \uparrow$, $I_{dsN} \uparrow$, $I_{dsp} \downarrow$ as both are

in series $I_{dsn} = I_{dsp}$ PMOS → Sat
NMOS → Sat

To find point when both are in saturation, we equate

$I_{dn(sat)} = I_{dp(sat)}$ and find the V_1 value satisfying it

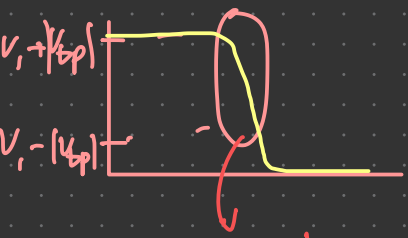
$K_n (V_1 - V_{thn})^2 = K_p (V_{sgp} - |V_{tp}|)^2$ → we ignored channel width modulation

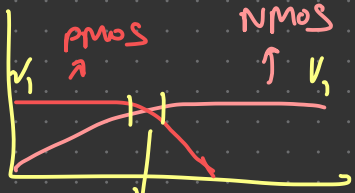
$$V_1 = \frac{V_{DD} + \sqrt{\frac{K_n}{K_p}} V_{tn} - |V_{thp}|}{\sqrt{\frac{K_n}{K_p}} + 1}$$

Now we find V_o for this V_1

$V_{dsn} \geq V_{gsn} - V_{thn}$, $V_{dsp} \leq V_{gsp} - |V_{thp}|$

$V_o \leq V_1 + |V_{tp}|$





$I_{ds_n} = I_{dsp}$ can have this range of values ideally But only 1 value practically

If $K_n = K_p$ and $V_{tn} = |V_{tp}|$

$$\boxed{V_i = \frac{V_{DD}}{2}} \rightarrow \text{Special Case}$$

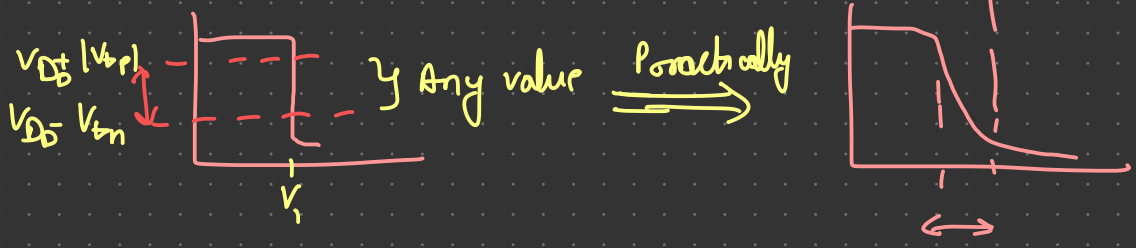
In general,

drain current doesn't depend on drain voltage when its in the constant region.

We find range of V_o with respect to V_i,

$$V_i - V_{tn} < V_o \leq V_i + |V_{tp}|$$

So, when V_i is in that range, V_{out} can be of any value i.e there is no fixed value as its a straight line in ideal situation



Range: $V_{tn_n} + |V_{tn_p}|$

IMP

So, not a good region to operate for static logic as we want well defined outputs

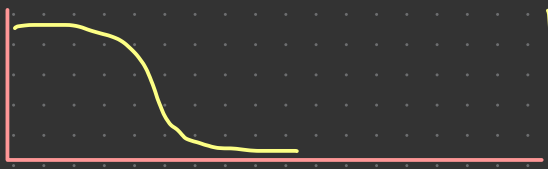
Practically also we have fast transition

When V_{GS} increases beyond 3rd stage,

④ NMOS → Linear mode
PMOS → Saturation mode
} Beyond

V_{DS_p} will become more -ve as output ↓ So remains in saturation

V_{DS_N} decreases so it moves to linear

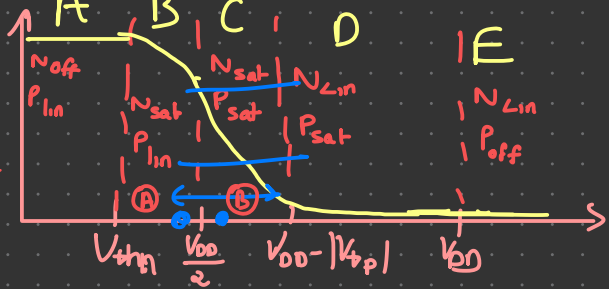


$$V_i \leq V_m \leq V_{DD} - |V_{tp}|$$

We equate $I_{ds_{N(linear)}} = I_{ds_{P(sat)}}$

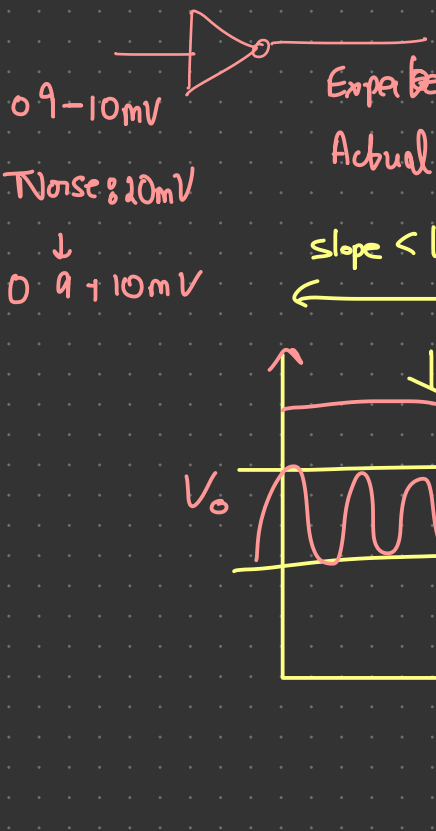
Find V_o from this equation

$$V_o = (V_i - V_{tn}) - \sqrt{(V_{DD} - V_{tn} - |V_{tp}|)(2V_i - V_{DD} - V_{tn} + |V_{tp}|)}$$



Even for a small change in input in that region output can change drastically

Blue Range: won't operate digital signals in that range



$A_v >> 1$

$\frac{dV_o}{dV_{in}}$ = Very Large

⇓

Amplification

Avoid regions with |slopes| > 1 → Also called noise margin parameters