Circuits

CMOS - Static Logic Gate

↑

Complementary MOS

↳ Made up of NMOS, PMOS operated by same set of inputs

↳ Complementary nature of NMOS & PMOS

Static - Well settled response

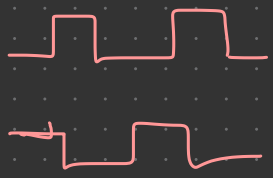
↳ Changing w.r.t. ∞

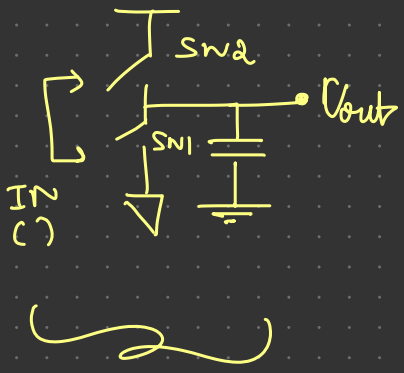
↳ At any point in time, each gate's output is either V_{dd} [Highest] or V_{ss} [or Lowest] are connected through low resistor path

Static Logic:

↳ At all time, output will assume value of boolean function implemented by circuit

→ Should be a fixed value



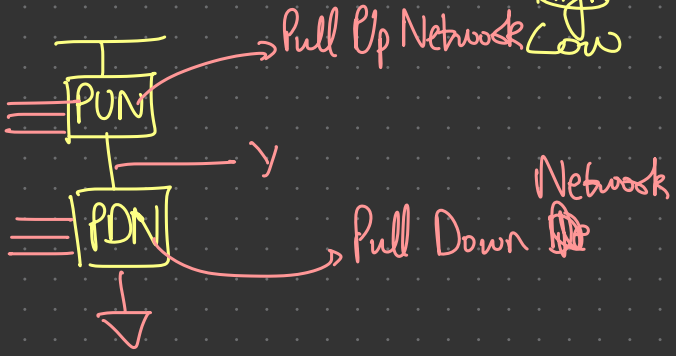


IN → True → SW1 Close
SW2 Open

→ False → SW1 Open
SW2 Close

→ High output

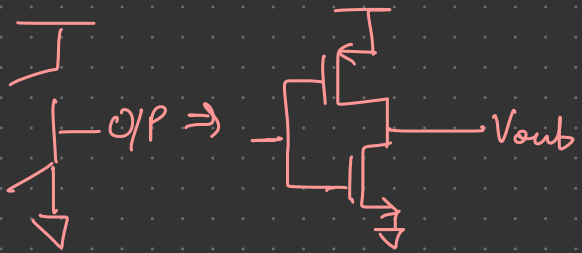
→ Low output

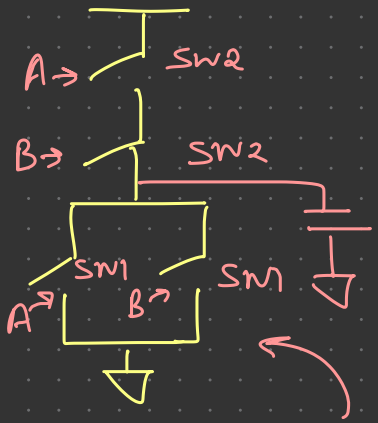


Pull Up Network should have complementary switches to Pull Down Networks

Each logic → PUN, PDN

PMOS & NMOS





A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NOR GATE

IN TERMS OF PMOS

PULL DOWN NETWORK
↳ NMOS

PULL UP NETWORK
↳ PMOS

② Purpose:
↳ Evaluate I/P and drive output to 0 or 1

Ratio-less logic [Final logic is not affected]

If we give sufficient time, irrespective of size, length, etc

↳ Its steady state values

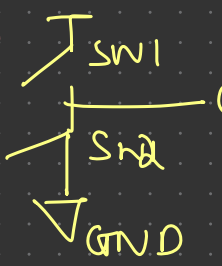
③ If PMOS, it will have low finite resistance when connected to V_{DD}, it is expected as there is no current supply, ∴ Power = 0

Then it means, it static, static power consumption = 0
no power is wasted.

④ If asked to make any gate, different sizes, all give same output what the deciding factor?

→ Efficacy of design
↳ How fast we can charge / discharge output from 0 to V_{dd} or V_{dd} to 0

⑤



There will be moment when both will be ON These will be a slight delay
↳ A lot of current will be drawn from supply

Small Period Power Consuption = $I V_{DD}$ peak

∴ Switching / Dynamic Power ≠ 0

→ Reduce dynamic power consumption
  ↳ Try optimisations

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CMOS INVERTER

→ Most basic & imp
  ↳ Match all design principles to build complex gates

→ Transfer characteristic → Static conditions
                              ↓
                           Settled

Weste & Harris Book / Rabaey

① Static Characteristic [J 11:00] → Remse