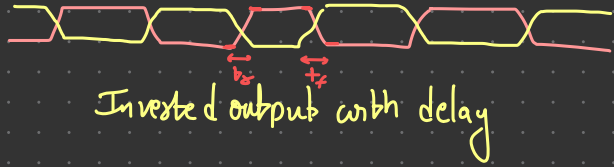




Dynamic Characteristics



Inverted output with delay

t_r - Rise time

t_f - Fall time

t_{pd} - Propagation Delay

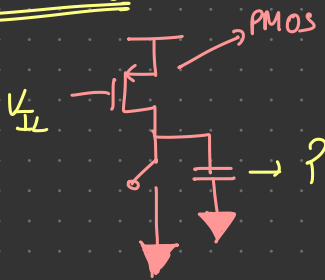
Based on output

$$t_{pd} = \frac{t_r + t_f}{2} \quad [\text{Average of both}]$$

Assumptions:

- ① At a time, only one transistor is ON and other is OFF

Rise-time:



[Assume NMOS is OFF]

We use V_L because one logic gate will ~~and~~ drive one to other

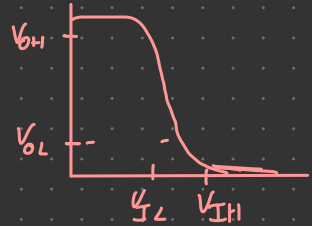
With finite sizes, they will give some gate capacitance which will act as load capacitance to the driver

Essentially corresponds to time taken to charge capacitor

V_{IL} - used as it is considered as max limit till which we can consider as low level

$T_{rise} \rightarrow 0 \text{ to } V_{OH}$

for capacitor



This is the recognised level for logic high

Initially capacitor voltage increases roughly behaving like RC
Ideally we should get

$$V_0 = V_1 [1 - e^{-t/RC}]$$

∞ time to reach $V_0 = V_1$

55% time to reach 98% etc

Due to this ∞ time issue, we find the time taken reach V_{OH}

Derivation:

Drain current = Capacitor current

$$I_{dp} = C \frac{dV_0}{dt} \Rightarrow \int_0^{T_r} \frac{dt}{C} = \int_0^{V_{OH}} \frac{dV_0}{I_{dp}}$$

$$\frac{T_x}{C} = \int_0^{V_{OH}} \frac{dV_o}{I_{dp}}$$

→ Initially when PMOS was ON, it was in saturation

→ After a while due to capacitor charging when

$V_o \leq V_i + |V_{Tp}| \rightarrow$ In saturation initially

$V_o > V_i + |V_{Tp}| \rightarrow$ Goes into linear region

$$\frac{T_x}{C} = \int_0^{V_i + |V_{Tp}|} \frac{dV_o}{I_{dp_{sat}}} + \int_{V_i + |V_{Tp}|}^{V_{OH}} \frac{dV_o}{I_{dp_{lin}}}$$

Do the full derivation for above as it's important for quiz

$$T_{rise} = \frac{2C[V_i + |V_{Tp}|]}{K_p(V_{DD} - V_{IL} - |V_{Tp}|)^2} + \frac{C}{K_p(V_{DD} - V_{IL} - |V_{Tp}|)} \ln \left[\frac{V_{DD} + V_{OH} - 2V_{IL} - |V_{Tp}|}{V_{DD} - V_{OH}} \right]$$

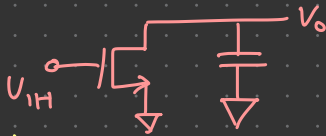
Saturation
Linear

Saturation region - Acts like constant current source

Linear region - Acts like resistor in PMOS

Fall Time:

↳ NMOS - ON
PMOS - OFF



↳ Minimum value of voltage which can be considered logic high

T_f defined by drop from 3

$V_{DD} \rightarrow V_{OL}$

$$I_{dn} = -C \frac{dV_o}{dt}$$

Initially in saturation region
Once it charges, it will eventually go into linear region
Break integral into two parts - saturation, linear

$V_o \geq V_i - V_{th} \rightarrow \text{Saturation}$

$V_o < V_i - V_{th} \rightarrow \text{Linear}$

$$\frac{T_f}{C} = - \int_{V_{DD}}^{V_i - V_{th}} \frac{dV_o}{I_{dsat}} - \int_{V_i - V_{th}}^{V_{OL}} \frac{dV_o}{I_{dlin}}$$

$$T_{fall_{th}} = \underbrace{\frac{2C [V_{DD} - V_{IH} - V_{th}]}{K_n [V_{IH} - V_{th}]^2}}_{\text{Sat}} + \underbrace{\frac{C}{K_n [V_{IH} - V_{th}]} \ln \left[\frac{2(V_{IH} - V_{th}) - V_{OL}}{V_{OL}} \right]}_{\text{Linear}}$$

In general,

$$\frac{K}{C} = f(V_{DD}, V_{IL}, V_{IH}, V_{OL}, V_{IL}, V_{OH}, V_{IO})$$

↳ Function

↳ Function of voltages that are technology dependent.

$$\frac{K}{C} = \text{constant for given technology, supply voltage}$$

IMP

If noise margin parameters are given $\frac{K}{C}$ can be calculated

→ If C is increased, keeping K constant → S will also increase

→ If C is increased, to have same S → Increase K [Adjust $\frac{W}{L}$]

Usually L - const so only W is scaled up/down

↳ $\mu_0 C_{ox} \left[\frac{W}{L} \right]$