Multirate Analog-Digital Systems for Signal Processing and Conversion

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Systems containing both analog and digital functions have been investigated with the purpose of realizing mixed-signal integrated circuits with higher levels of functionality and integration. In most cases, such mixed-signal systems are inherently multirate because of the different sampling rates employed at various stages of the system. The multirate concepts have been used for traditional applications, such as subband coding and narrowband filter design. Some unconventional applications of multirate signal processing are also emerging, both for converting between analog samples and digital words, and for realizing processing functions in an easier and more economical way than would be possible using purely digital or analog techniques. This paper reviews fundamental multirate concepts, discusses some recent developments in this area of integrated multirate analog-digital systems, and outlines some possible future directions for research and application.

I. INTRODUCTION

Multirate signal processing emerged in the 1970's as a specialized branch of digital signal processing (DSP) [1], [2], driven by the need for solving, in the most efficient possible way, a number of problems mainly related to the migration of telephone multiplexing and transmission systems from analog-to-digital solutions [3]. Subsequently, the technique found many more application areas of great relevance today; the decimation and interpolation techniques applied to oversampling data converters are more familiar examples [4]. The emergence of many other signal processing technologies, such as charge transport devices [5] and switched capacitors [6], which are also discrete time, although the signal amplitudes are represented in analog form, led to the development of analog multirate signal processing techniques which have found important application areas in the realization of complex filtering systems with very high Q-factors [7], as well as in high-speed interface and data acquisition systems of which video coders/decoders [8] and magnetic disk read channel coders [9] are some of the most visible examples. Today, new design solutions are emerging, which combine the benefits of both digital and analog multirate signal processing to achieve high efficiency in silicon and power consumption in modern mixed analog-digital integrated circuits [10].

This paper discusses some recent developments in the area of multirate signal processing, including digital, analog, and even mixed-signal analog-digital. We begin in Section II by reviewing fundamentals of multirate theory. In Section III, we review next some basic concepts of multirate analog-digital systems and signals, including the multirate front-end subsystems used to provide the required filtering conditions for converting between continuous-time and discrete-time signals as well as the converters, both single-rate and multirate, that transform analog samples into digital signals and the digital signals back into analog samples. A generalized multirate analog-digital system architecture for digital processing of analog signals is presented leading to the conventional system architectures employed today. Section IV describes specific analog-digital multirate systems for data conversion, including the popular oversampling converters as well as some new architectures based on the quadrature-mirror filter (QMF) banks. Analog-digital multirate systems for signal processing functions are discussed in Section V. First, we discuss some practical issues and multirate design solutions for realizing on a single chip analog front-end filtering subsystems of vital importance for modern very large scale integrated (VLSI) processing systems, specially bearing in mind the state-of-the-art technologies which allow the strategic objective of high quality analog-digital integration. Then we show how a fully analog multirate sampled-data system, based on switched capacitors, can efficiently realize the signal processing functions needed for frequency division multiplexing (FDM). More complex analog-digital

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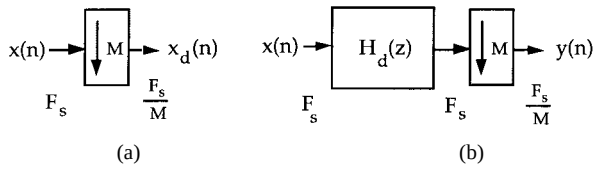

Fig. 1. (a) Down-sampler and (b) decimator.

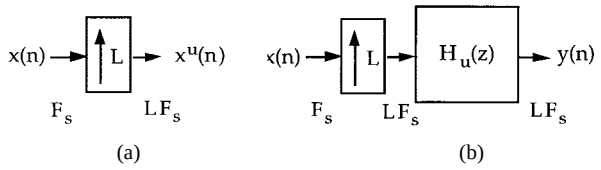

Fig. 2. (a) Up-sampler and (b) interpolator.

multirate systems are also illustrated for transmultiplexing from FDM to time division multiplexing (TDM). This section also shows how very high selectivity filtering, of widespread use in telephony and other communication systems, can also be very efficiently realized using multirate systems. Section VI indicates some potential wide research avenues where the benefits of multirate analog-digital integrated systems can be fully exploited in order to achieve improved performance of many important signal processing and conversion functions, including signal detection, bank filtering, and multidimensional filtering. A brief summary of the paper and its conclusions are finally presented in Section VII.

II. A Review of Multirate Concepts [1], [2]

A. Basic Components

In addition to the three basic components of a linear single-rate discrete-time system, namely, the unit delay, the adder, and the multiplier, a linear multirate discrete-time system employs two other components: the down-sampler and the up-sampler.

The *down-sampler*, shown symbolically in Fig. 1(a), is used to generate from a discrete-time sequence $x(n)$ another discrete-time sequence $y(n)$ with a lower sampling rate. The time-domain input–output (I/O) relation of a down-sampler is given by

$$x_d(n) = x(Mn) \tag{1}$$

where the down-sampling factor M is a positive integer greater than one. Thus if the sampling rate of $x(n)$ is F_s, the sampling rate of $x_d(n)$ is F_s/M. In the frequency-domain, the I/O relation of a down-sampler is given by

$$X_d(e^{j\omega}) = \frac{1}{M}\sum_{k=0}^{M-1} X(e^{j(\omega-2\pi k)/M}) \tag{2}$$

where $X(e^{j\omega})$ and $X_d(e^{j\omega})$ denote the Fourier transforms of $x(n)$ and $x_d(n)$, respectively. As indicated by (2), $X_d(e^{j\omega})$ is the sum of M frequency scaled and shifted images of $X(e^{j\omega})$ with adjacent images of $X_d(e^{j\omega})$ separated by 2π. Thus unless $X(e^{j\omega})$ is band-limited to the region

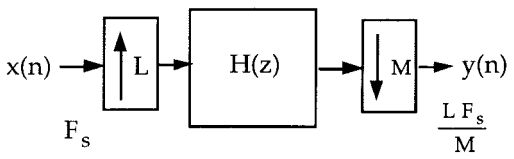

Fig. 3. Sampling rate alteration by a rational factor.

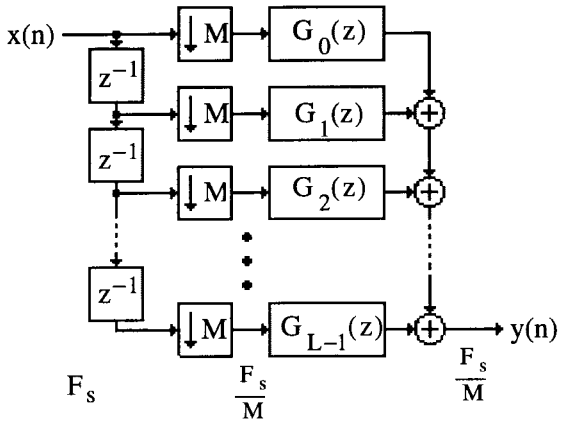

Fig. 4. Computationally efficient implementation of a decimator.

$0 \le \omega \le \pi/M$, there will be overlap of adjacent terms in (2) causing aliasing. As a result, to prevent any aliasing that may be caused by the down-sampling process, $x(n)$ is usually passed through a lowpass filter approximating the ideal frequency response

$$H_d(e^{j\omega}) = \begin{cases} 1, & |\omega| \le \pi/M \\ 0, & \pi/M < |\omega| < \pi \end{cases} \tag{3}$$

before it is down-sampled as indicated in Fig. 1(b). The combination of an anti-aliasing filter and a down-sampler is usually called a *decimator* and the process of lowering the sampling rate by this arrangement is called *decimation.*

The device used to generate a discrete-time sequence $x^u(n)$ with a higher sampling rate from another discrete-time sequence $x(n)$ is called the *up-sampler* shown in Fig. 2(a). The time-domain I/O relation of the up-sampler is given by

$$x^u(n) = \begin{cases} x\left(\frac{n}{L}\right), & n = 0, \pm L, \pm 2L, \cdots \\ 0, & \text{otherwise} \end{cases} \tag{4}$$

where the up-sampling factor L is a positive integer greater than one. Thus if F_s is the sampling rate of $x(n)$, the sampling rate of $x^u(n)$ is LF_s. In the frequency-domain the corresponding relation is given by

$$X^u(e^{j\omega}) = X(e^{j\omega L}) \tag{5}$$

where $X^u(e^{j\omega})$ denotes the Fourier transform of $x^u(n)$. It follows from (5) that the zero-valued samples of $x^u(n)$ can be replaced with their appropriate nonzero values by an interpolation process which in the ideal case is achieved by passing $x^u(n)$ through an ideal lowpass filter with a frequency response [11]

$$H^u(e^{j\omega}) = \begin{cases} L, & |\omega| \le \pi/L \\ 0, & \pi/L < |\omega| < \pi. \end{cases} \tag{6}$$

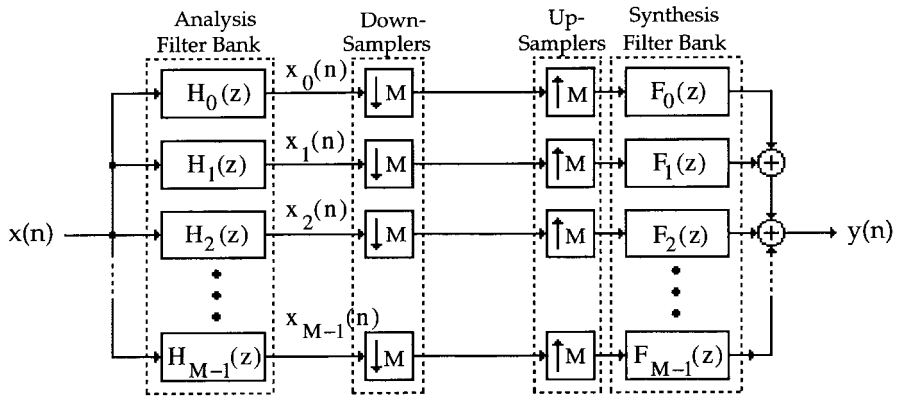

Fig. 5. QMF bank.

The combination of an up-sampler and the lowpass filter, shown in Fig. 2(b), is usually called an *interpolator* and the process of increasing the sampling rate by this arrangement is called *interpolation*.

A cascade of an up-sampler, a lowpass filter, and a down-sampler, as indicated in Fig. 3, can be employed to alter the sampling rate of a discrete-time signal $x(n)$ by any rational factor L/M.

B. Polyphase Implementation [12]

In the implementation of the lowpass filter in the decimator of Fig. 1(b), the arithmetic operations are carried out at the sampling rate F_s of the input rather than at the lower sampling rate F_s/M of the output. A computationally efficient structure for the implementation of the decimator can be obtained by making use of the polyphase representation of the lowpass filter

$$H_d(z) = \sum_{i=0}^{M-1} z^{-i} G_i(z^M) \tag{7}$$

resulting in the structure of Fig. 4 where now the arithmetic operations are carried out at the lower sampling rate F_s/M. In the case of an finite impulse response (FIR) transfer function $H_d(z)$, the polyphase decomposition can be derived by inspection. On the other hand, in the case of an infinte impulse response (IIR) transfer function $H_d(z) = N(z)/D(z)$, the polyphase decomposition is obtained by multiplying the numerator and the denominator with an appropriate factor $Q(z)$, such that the modified transfer function can be expressed as

$$H_d(z) = \frac{N(z)Q(z)}{D(z)Q(z)} = \frac{N'(z)}{D'(z^M)} = \sum_{i=0}^{M-1} z^{-i} \frac{N_i(z^M)}{D'(z^M)}. \tag{8}$$

A special case of the polyphase decomposition of a lowpass decimation (interpolation) filter for a factor-of-M decimation (interpolation) is given by

$$H_d(z) = \alpha + \sum_{i=1}^{M-1} z^{-i} G_i(z^M) \tag{9}$$

where α is a constant which is usually chosen as $1/M$. A lowpass filter with a transfer function of the form of (9) is usually called an M*th band* or *Nyquist filter* [2]. The impulse response $h_d(n)$ of such a filter is given by

$$h_d(nM) = \begin{cases} \alpha, & n = 0 \\ 0, & \text{otherwise.} \end{cases} \tag{10}$$

It follows from the above that an Mth band filter requires fewer computations than an equivalent lowpass decimation (interpolation) filter. For a transfer function $H_d(z)$ satisfying (9), it can be shown that

$$\sum_{k=0}^{M-1} H_d(zW_M^k) = M\alpha = 1 \tag{11}$$

where $W_M = e^{-j2\pi/M}$. An Mth band filter for $M = 2$ is called a *half-band filter*.

Under certain conditions, an Mth band IIR transfer function $H_d(z)$ can be decomposed as a sum of allpass transfer functions in the form

$$H_d(z) = \frac{1}{M} \sum_{i=0}^{M-1} z^{-i} A_i(z^M) \tag{12}$$

where $A_i(z)$ are stable allpass transfer functions for a stable $H_d(z)$. In the case of a two-band $(M = 2)$ decomposition, it has been shown that all Butterworth and elliptic odd-order half-band transfer functions can be analytically decomposed in the form of (12) [13]. For Mth band transfer functions with $M > 2$, a computer-aided design approach to develop the decomposition has been proposed [14].

Similar computationally efficient structures can be derived for the implementation of interpolators based on a polyphase decomposition of the interpolation filter transfer function.

A switched-capacitor filter implementation of a decimator (interpolator) based on the allpass decomposition of the corresponding Mth band lowpass decimation (interpolation) has been recently proposed [15].

C. QMF Bank

A multirate structure developed primarily for efficient data compression is the M-channel QMF *bank* shown in Fig. 5. In this structure, the input discrete-time signal $x(n)$ is passed through an analysis filter bank consisting of a

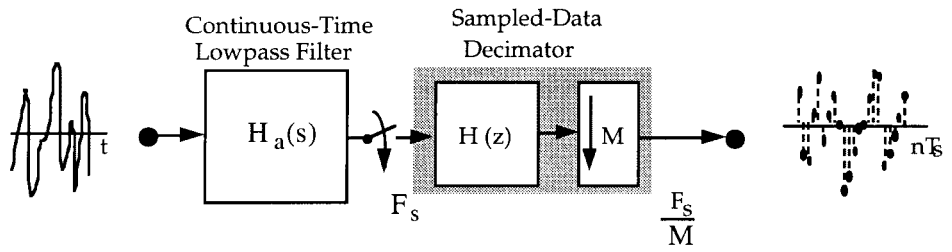

Fig. 6. Multirate architecture for time-discretization of analog signals.

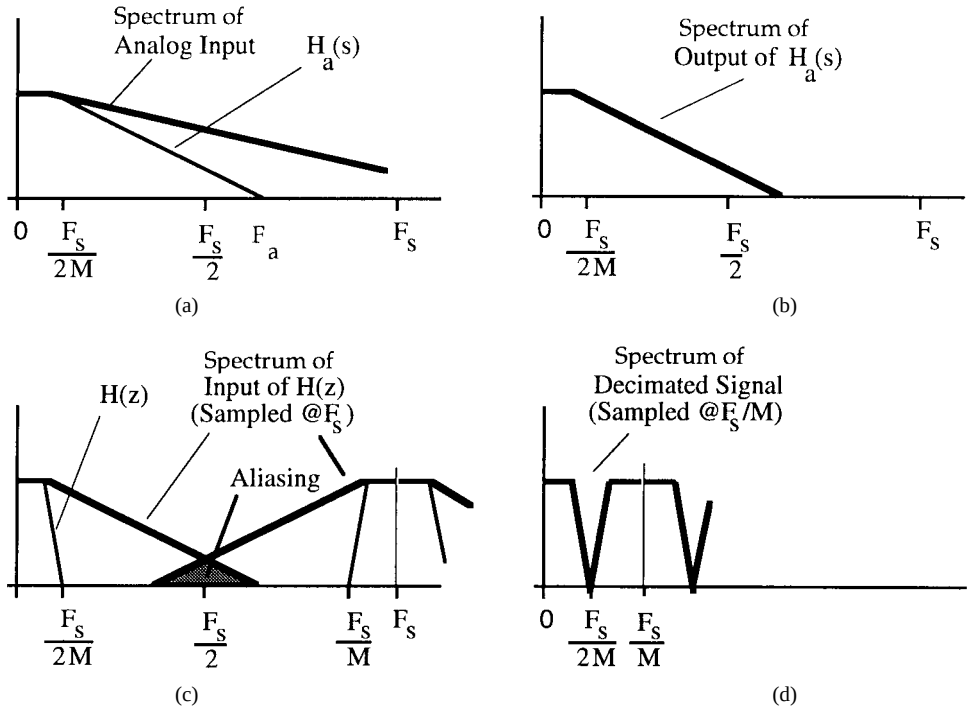

Fig. 7. Frequency domain operation of the continuous-time and sampled-data decimator circuits for anti-aliasing filtering. Observe in (c) that aliasing can be initially allowed, and later removed by the SC filter $H(z)$.

set of M bandpass filters $H_i(z)$ decomposing $x(n)$ into a set of M subband signals $x_i(n)$ occupying contiguous nonoverlapping frequency bands of width $2\pi/M$. The subband signals are then down-sampled by a factor of M. Next, these down-sampled signals are up-sampled by a factor of M, and passed through a synthesis filter bank composed of a set of M bandpass filters $F_i(z)$ to remove the images, resulting in an output signal $y(n)$ whose sampling rate is the same as that of the input $x(n)$. The I/O relation in the z-domain is given by

$$Y(z) = \frac{1}{N}\sum_{k=0}^{N-1} F_k(z)\sum_{i=0}^{N-1} H_k(zW_N^i)X(zW_N^i). \quad (13)$$

The analysis and synthesis filters can be designed to achieve a perfect reconstruction at the output implying that the output is a delayed and scaled replica of the input with complete aliasing cancellation [2]. In this case, (13) reduces to $Y(z) = Kz^{-n_o}X(z)$ where n_o is a positive integer and K is a constant.

III. Multirate Processing of Analog and Digital Signals

A. Converting Between Continuous-Time and Discrete-Time Signals

Time-discretization of continuous-time signals represents the simplest case of multirate processing, whereby a continuous-time signal is transformed into a sequence of analog samples at a frequency F_s. In general, this can be done in two steps using the architecture of Fig. 6. First, a continuous-time filter $H_a(s)$ band limits the input signal as indicated in Fig. 7(a) and (b). Some aliasing effect can even be initially tolerated by the scheme of Fig. 6, with the purpose of alleviating the selectivity requirements on the continuous-time filter. Then, as shown in Fig. 7(c), the resulting sequence of samples is processed through a factor-of-M sampled-data decimator, with a decimation filter of transfer function $H(z)$, that reduces the sampling frequency to a lower value F_s/M [Fig. 7(d)] and removes the aliased components. Usually the output of $H_a(s)$ is initially oversampled at a rate that is a factor of M greater than the

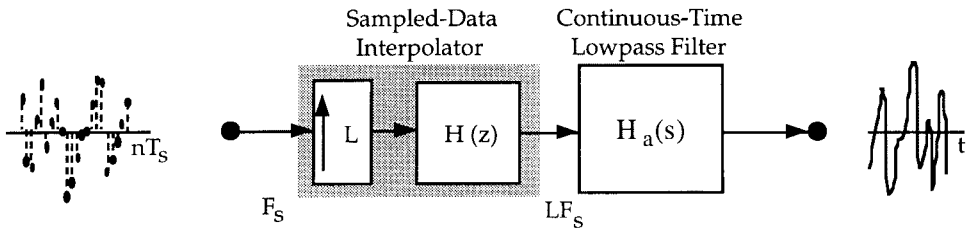

Fig. 8. Multirate architecture for recovering continuous-time signals.

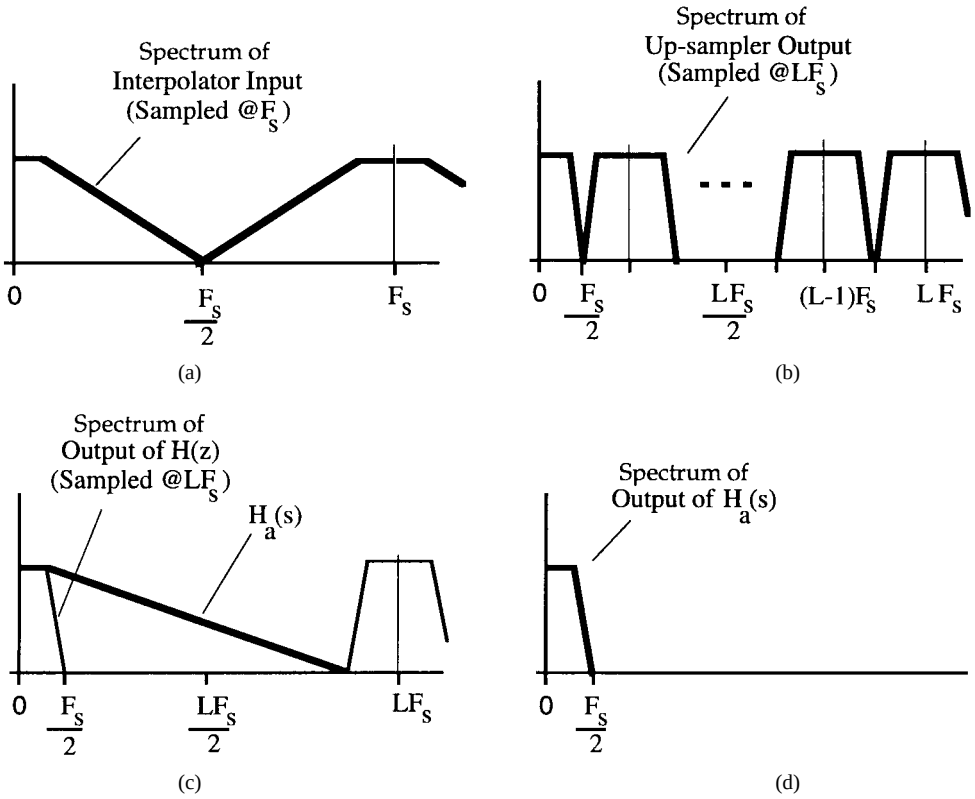

Fig. 9. Frequency domain operation of the continuous-time and sampled-data interpolator circuits for anti-imaging filtering.

desired sampling rate of the discrete-time decimator, so that a low Q continuous-time anti-aliasing filter can be used. In the frequency domain, the characteristic of the decimator is also important because it should attenuate those unwanted alias frequency-translated components associated with the signal at the lower sampling frequency F_s/M which have not been sufficiently attenuated by the continuous-time filter. The combined amplitude characteristics of the continuous-time and sampled-data decimator filters produce the overall anti-aliasing filtering function that is needed to allow a continuous-time signal to be time-discretized into a sequence of analog samples with frequency F_s/M. There is another advantage to this approach. It permits the use of an analog low-Q Bessel filter as the anti-aliasing filter, if needed, followed by a discrete-time decimator with a linear-phase Mth band filter.

The complementary two-step process of recovering a continuous-time signal from a sequence of analog samples is realized by means of the multirate architecture of Fig. 8. Its frequency domain operation is illustrated in Fig. 9. Here, a sampled-data interpolator increases L-fold the frequency of the input sequence of samples and, at the same time, removes the associated $L-1$ frequency-translated image bands. Fig. 9(b) shows only the bands centered at $F_s, 2F_s, \cdots, (L-1)F_s$. Then the frequency-translated image bands centered at $kLF_s, k = 1, 2, \cdots$, associated with the output sequence with the sample rate LF_s, are filtered by the subsequent continuous-time filter, as shown in Fig. 9(c). The combined amplitude characteristics of the sampled-data interpolator and continuous-time filters produce the overall anti-imaging filtering function that is needed to allow a continuous-time signal to be recovered from a sequence of analog samples with frequency F_s.

When designing the above subsystems there are important technology trade-offs that relate the design complexity of the continuous-time and the discrete-time sampled-data

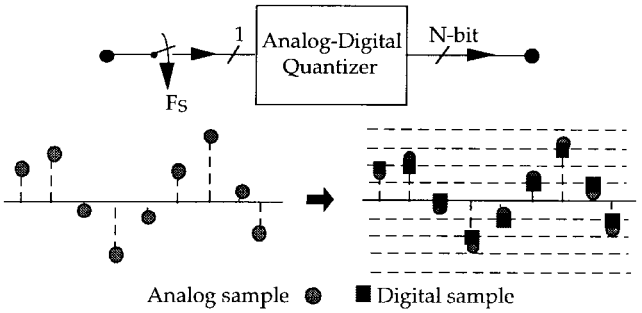

Fig. 10. Quantization of analog samples.

decimation and interpolation filters, which will be discussed in Section V.

B. Converting Between Analog and Digital Samples

Conversion between analog and digital samples is carried out by analog-to-digital (A/D) and digital-to-analog (D/A) converters. In the most conventional type of converters, illustrated in Fig. 10, the input and output sequences are produced at the same frequency, i.e., for each input analog sample (or digital word) there is a corresponding output digital word (or analog sample). Conversion between both sequences is carried-out by means of a quantizer with 2^N levels, as represented in the example of Fig. 11 for the case of a uniform quantizer with equally spaced quantization levels, such that, for N large enough, the resulting power spectral density of the quantization noise is uniformly distributed over the entire Nyquist band from dc to half the conversion frequency $F_s/2$. This is the reason why such converters are also usually known as Nyquist converters. There is a vast body of literature concerned with the design of many different types of Nyquist converters that are currently available to meet a wide range of specifications, whose discussion is out of the scope of this paper [16]–[18].

There is another class of A/D and D/A converters, usually designated as oversampling delta-sigma converters [19], which, unlike the previous Nyquist converters, relate input and output sequences with different frequencies and are, therefore, inherently multirate. Here, the process of signal conversion (SC) corresponds to evaluating a sequence of digital samples, rather than a single sample, produced at a high frequency and then obtain a digital word at a much lower frequency that represents a good estimation of the average of all those samples. In such converters, the resulting conversion resolution does not depend on the quantizer alone but rather on the combined functions of a low-resolution quantizer together with a digital decimation post-filter. This class of converters will be again considered in Section IV.

C. Generalized System Architecture

Based on the various building blocks discussed above, we can represent the generalized architecture of an integrated multirate analog-digital system for the digital processing of an analog signal as indicated in Fig. 12. In the most popular design solutions, only some of the building blocks

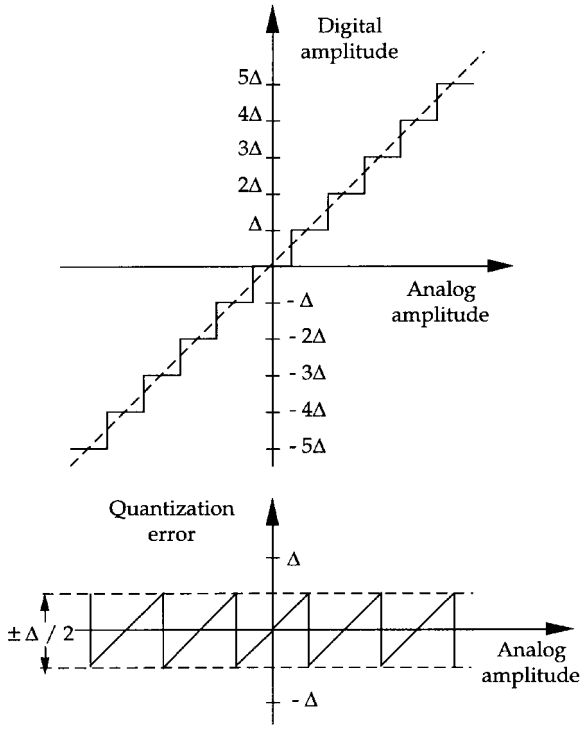

Fig. 11. Ideal conversion characteristic and quantization error produced by an uniform quantizer.

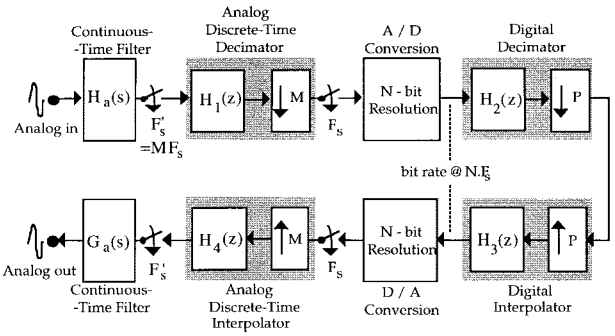

Fig. 12. Generalized multirate architecture for digital processing of analog signals.

are utilized to realize a complete system, as illustrated in the architecture of Fig. 13(a), employing Nyquist-based quantization of the analog samples, or in the architecture of Fig. 13(b), built around an oversampling A/D converter. Many other architectures can be developed by using the complete set of building blocks and trading off their characteristics in order to achieve the highest performance specifications with the most economical design solution.

IV. Analog-Digital Multirate Systems for Signal Conversion

A. Oversampling A/D Converters

As mentioned before, the oversampling A/D converters are inherently multirate because they relate an input sequence of analog samples with a high sampling rate to an

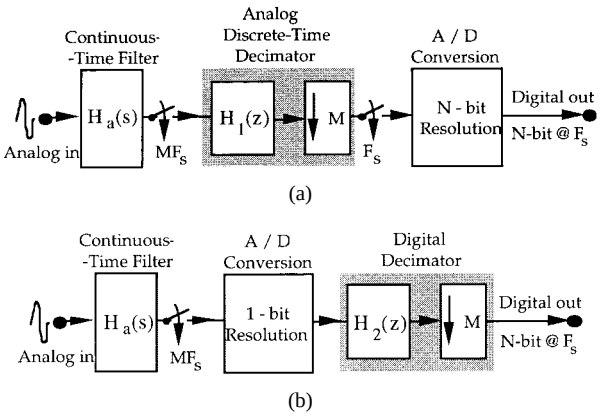

Fig. 13. Multirate architecture for digitization of analog signals employing (a) a Nyquist band converter using a fine N-bit quantizer and (b) an oversampling converter using a coarse 1-bit quantizer.

output sequence of digital words operating at a much lower sampling rate. Such converters achieve high resolution by means of oversampling and noise shaping and have been shown to be a good alternative for the implementation of high-resolution, low-speed A/D converters mainly because they can accommodate the limitations associated with the implementation of its analog processing in digital MOS technology [4]. As illustrated in the schematic diagram of Fig. 14, an analog input signal is sampled at a frequency MF_s significantly higher than $f_{\max}$, the highest frequency present in the input signal. The correspondingly high frequency bit stream produced by a coarse quantizer is then decimated to a much lower frequency digital signal until the required word length is formed. Such decimation is performed by means of a digital decimator consisting of a digital Nyquist lowpass filter together with a down-sampler. The resulting A/D converter is called a delta-sigma A/D converter since it employs a delta-sigma modulator as the basic building block.

A special case of Fig. 14 is when $R = 1$. Here, the digital estimator is a simple voltage comparator and the D/A converter has one-bit resolution. The delta-sigma converter thus quantizes a very high sampling rate (e.g., 2 MHz) analog input sample sequence with very low resolution (e.g., 1 bit). With the aid of down sampling and digital filtering, the sampling rate is reduced (e.g., 8 kHz) and the resolution is increased (e.g., 10 bit). The basic idea for signal-to-noise ratio (SNR) enhancement in a delta-sigma converter is to reduce the quantization noise by a high-pass filter leaving only a small fraction of the noise power inside the frequency band of interest. Further SNR improvement can be obtained by increasing the order of the filter [20]. Although its basic concept has been around for quite a few years, the integrated circuit technology needed to make the delta-sigma converters a viable solution has only recently become available. The delta-sigma A/D converter can be implemented on a single chip using MOS technology [4], with the analog part (delta sigma converter) usually implemented by SC circuits, and the digital part realizing the decimator.

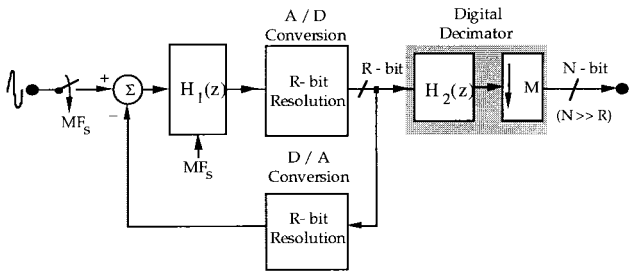

Fig. 14. Typical architecture of a multirate A/D conversion system based on sigma-delta modulation.

B. QMF-Based A/D Converters

In this approach a QMF bank is used to implement a high speed A/D converter, suitable for applications in the video-rate range (up to ≈ 100 MHz) using a number of low-speed, low-cost A/D converters, as indicated in Fig. 15 [21], [22]. Here, the analysis stage is an SC discrete-time network composed of the analysis filter bank and the down-samplers, while the synthesis stage is a digital network composed of the synthesis bank filters and up-samplers. Basically, in this approach the input signal is first decomposed into a number of contiguous frequency bands (subbands) so that a specific A/D converter (subconverter) can be assigned to each subband signal.

Although the structure of Fig. 15 is a natural extension of the time-interleaved A/D converter [23], [24] (in fact, the latter can be seen as a particular case, where the analysis filters $H_k(z) = z^{-k}$, and the synthesis filters $F_k(z) = z^{-(M-1-k)}$), the harmonic distortion due to mismatches among the subconverters is substantially reduced at a little additional cost [25]. The jitter problem due to uneven sample timing, which is another source of error in time-interleaved A/D converters, specially for high-frequency input signals, is reduced by the decimation stage in Fig. 15. A similar idea has been used by Poulton *et al.* [26] and has been called a *two-rank architecture*. The QMF-based converters also incorporate the advantages of subband coding: by appropriately specifying the resolution of the subconverters throughout the respective subbands, the quantization noise can be separately controlled in each band, and the shape of the reconstruction error spectrum can be controlled as a function of the frequency. This strategy has been used in many speech and image coding applications.

This new scheme has been simulated on a computer and tested in the laboratory using discrete components. Both simulation and experimental results have verified its good performance. Some of these results, as well as details about the circuit implementation of the analysis and filter banks, can be found in [21], [22]. Efficient implementation of the SC filters that realize the analysis filter bank has been addressed in [27], where the design of the SC filters for high frequency operations has been discussed. The emphasis has been placed on the use of single-stage operational amplifiers with very high bandwidth and moderate gain.

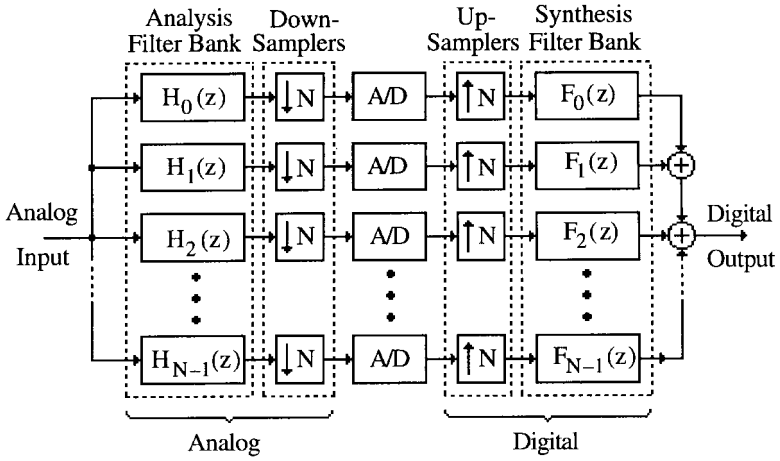

Fig. 15. High-speed A/D conversion system based on the QMF.

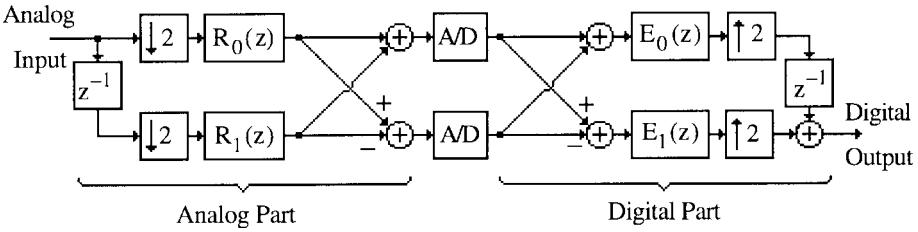

Fig. 16. Example of a more efficient structure for implementation of a high-speed A/D conversion system based on the QMF bank.

Theoretically, the overall resolution depends only on the resolution of the subconverters used. The noise generated by the SC circuits, however, places an upper bound of 11–12 bit [27], which is still well above the usual requirements for video applications. If successive approximation subconverters are used, then substantial savings in die area can be obtained when compared to flash converters.

A more efficient structure for implementation can be obtained by realizing the analysis and the synthesis filters in polyphase form and then moving the down-samplers to the left of the polyphase subfilters in the analysis bank and moving the up-samplers to the right of the polyphase subfilters in the synthesis bank, as indicated in Fig. 16 for a two-band decomposition. Using a tree structure, QMF banks with more than two bands can be developed from the two-band structure of Fig. 16 [28].

V. Analog-Digital Multirate Systems for Signal Processing

A. Front-End Filtering Subsystems

In the context of the front-end subsystems discussed in Section II, continuous-time and analog sampled-data filters are regarded as complementary building blocks. The optimum design of such subsystems consists, therefore, of finding the best possible tradeoffs between the continuous-time and sampled-data decimator and interpolator filters in order to achieve the highest operating performance of the front-end subsystem at the minimum cost in terms of silicon area and power consumption.

Integrated continuous-time filters are known to produce poorly controlled frequency responses, because of the variations suffered by the individual elements defining the filter time constants [29]–[31]. Although on-chip tuning alleviates but does not completely overcome this problem, continuous-time filters for the front-end subsystems should

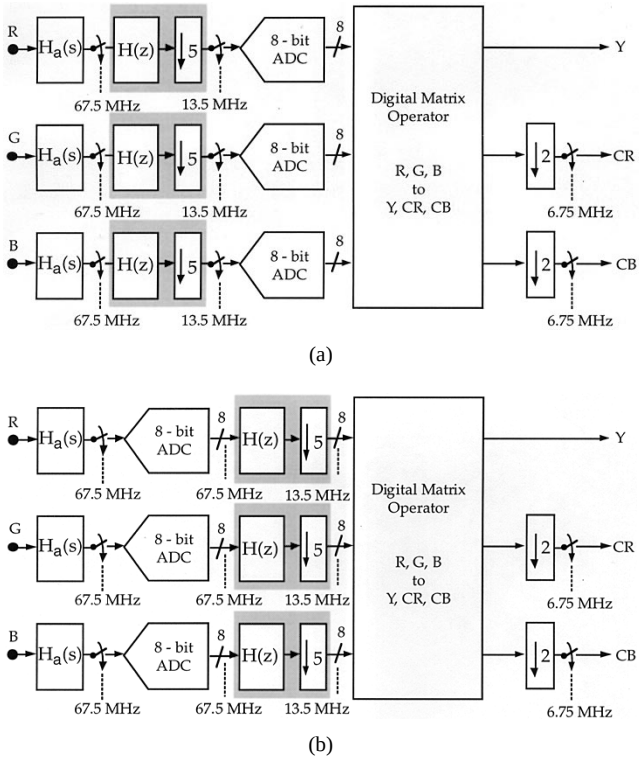

Fig. 17. Multirate architectures for CCIR 601 digitization of video signals. (a) Predominantly analog multirate and (b) predominantly digital multirate.

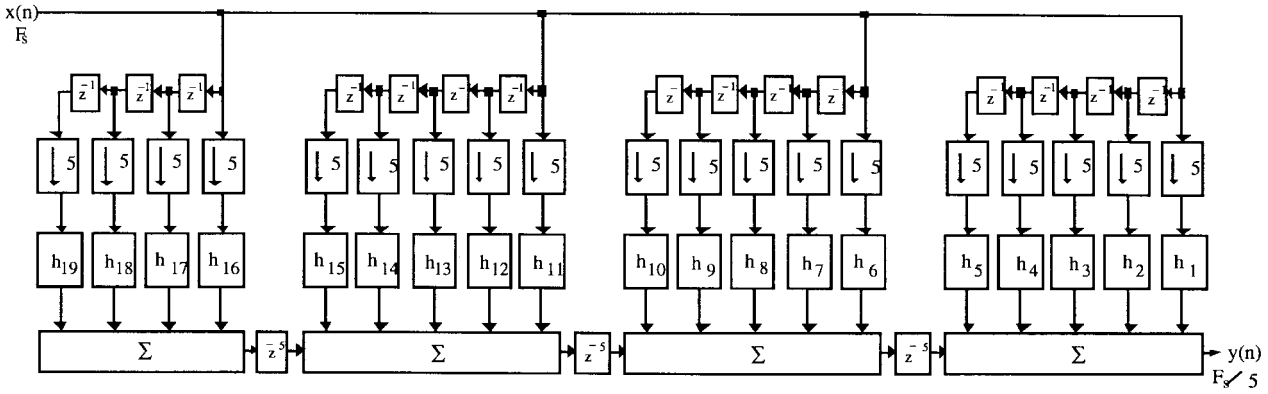

Fig. 18. Active-delayed block polyphase structure for the implementation of a video FIR SC decimator with $M = 5$ allowing relaxed settling requirements for the amplifiers [41].

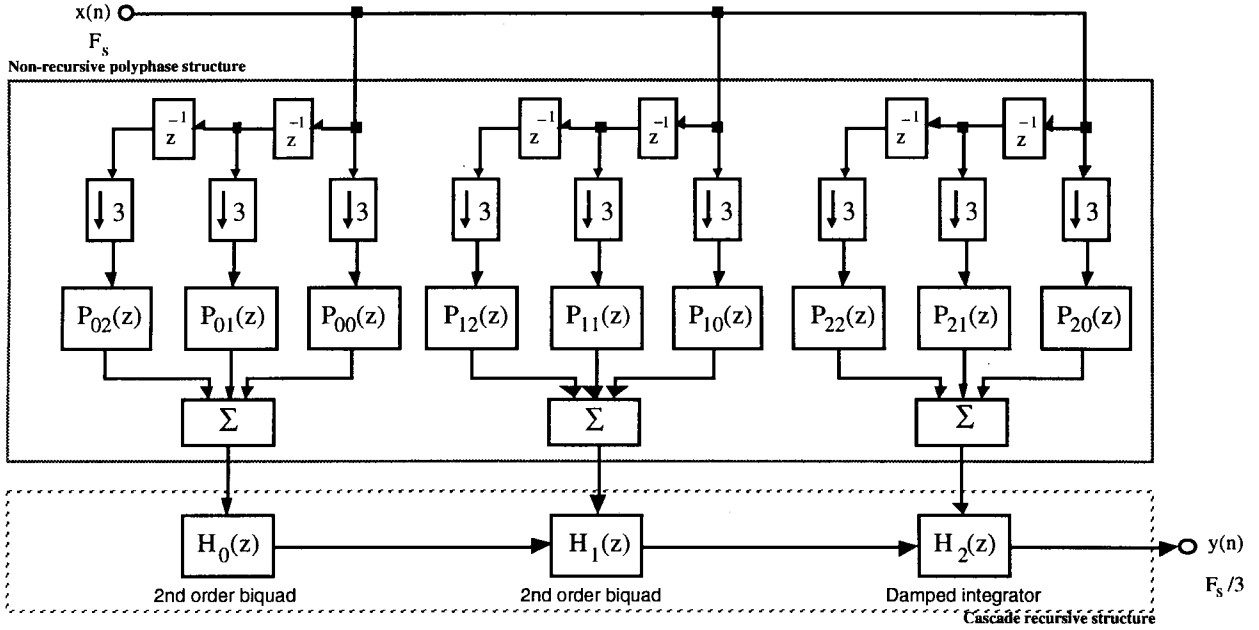

Fig. 19. Internally cascaded multirate structure for the optimum implementation of a video IIR SC decimator with $M = 3$ where the relaxed settling requirements of all the amplifiers are determined by the lower output sampling frequency [44], [45].

be designed in such a way that the predicted variability of the frequency response does not attenuate the signals conveyed through the front-end, nor reduces the minimum rejection of the unwanted aliasing components. Sampled-data filters, on the other hand, are limited in speed by the settling requirements of the amplifiers, and their overall transfer-function precision also requires that the resulting capacitance spread is not too large, either [6].

The above difficulties can be overcome by adopting optimum multirate architectures, whereby the speed requirements of the amplifiers and the capacitance spread are both determined by the lowest operating frequency in the subsystem and which, even for high-speed applications, can be comfortably achieved with state-of-the-art technology. SC circuits are particularly attractive for the implementation of such optimum multirate architectures and their practical feasibility has been demonstrated in a 1.8 μm CMOS prototype chip [32].

The practical advantages to be gained by using multirate SC filter structures in front-end subsystems become even more visible for high-frequency baseband signals, as is the case in video processing applications. This is illustrated with the example given in Fig. 17(a) where a continuous-time filter and a sampled-data decimator are optimally combined to meet the requirements of a single-chip front-end subsystem for digitizing video signals according to the CCIR 601 recommendation [33]. This predominantly multirate analog system solution can lead to significant savings in power and silicon consumption when compared with the functionally equivalent but predominantly multirate digital solution illustrated in Fig. 17(b) [34], [35].

Two solutions have been studied for the SC realization of the above analog decimation and filtering functions, both allowing all amplifiers to settle within a time interval of approximately 25 ns, which can be comfortably achieved using state-of-the-art CMOS amplifiers [36]. One such

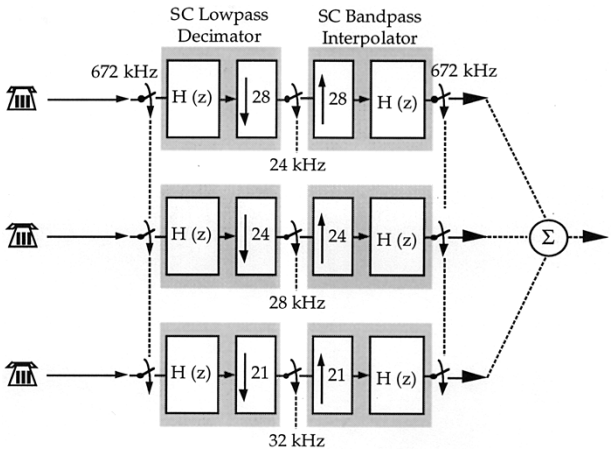

Fig. 20. Multirate analog system for translating a baseband channel into a higher frequency FDM channel.

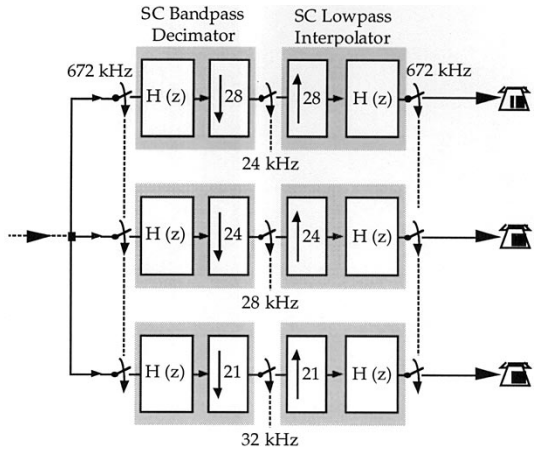

Fig. 21. Multirate analog architecture for baseband channel recovery from an FDM signal.

solution is based on the active-delayed block polyphase structure of Fig. 18, which realizes a FIR transfer function with 19 coefficients and a sampling rate reduction factor of $M = 5$ [37], [38]. The alternative solution is based on the internally cascaded structure illustrated in Fig. 19 [39]–[41], which realizes a fifth order elliptic bilinear z-transfer function with a down-sampling factor of $M = 3$. The practical feasibility and high-frequency operation capability of the latter solution was practically demonstrated in an integrated 2.4 μm CMOS prototype chip [42].

B. Analog FDM System

The generation of an FDM channel typically comprises the operations of frequency-translation of a baseband channel and subsequent high selectivity channel filtering. This can be realized by means of the multirate system of Fig. 20 [43], where each of the three processing channels comprises an SC lowpass decimator followed by an SC bandpass interpolator. The telephone signal sampled at a high frequency MF_s is decimated M-fold to the lower frequency F_s. The amplitude response of the decimator is tailored to allow transmission of the baseband signals from the minimum channel frequency $f_{\min} = 300$ Hz to the maximum channel frequency $f_{\max} = 3400$ Hz while eliminating the unwanted aliasing frequency components associated with the lower sampling frequency, i.e., in those frequency bands such that $kF_s - f_{\max} < f < kF_s + f_{\min}$ $(k = 1, 2, \cdots)$. After decimation, the sampled-data signal in each path is interpolated back to a higher sampling frequency by means of the SC interpolator. Now, the amplitude response of the interpolator, rather than filtering the baseband channel, is defined instead to select one of the frequency-translated image bands around F_s or its integer multiples kF_s up to LF_s, thereby forming the FDM channel. The selection of a particular value of kF_s depends on the required frequency band of the FDM channel. The SC decimator and interpolator circuits employed in such a system can be efficiently designed to achieve low power and reduced silicon area even to meet stringent selectivity and high sampling requirements [37], [38], [40], thus making the overall architecture solution rather cost effective.

Baseband channel recovery of an FDM channel can also be accomplished by a multirate system using complementary SC bandpass decimator and SC lowpass interpolator circuits, as indicated in the illustrative block diagram of Fig. 21 [43].

C. Transmultiplexer

A classical example of a mixed analog-digital multirate system is the transmultiplexer, used for converting a set of voice-band channels from a digital (TDM) format into an analog (FDM) format, and vice versa. In its basic form, the N-band digital transmultiplexer structure is comprised of an N-band synthesis filter bank with upsamplers at its input followed by an N-band analysis filter bank with down-samplers at its output as indicated in Fig. 22(a). For a perfect reconstruction it is desired that the output $\hat{x}_k(n)$ of the kth analysis branch be exactly equal to the input $x_k(n)$ of the kth synthesis branch for $k = 0, 1, \cdots, N-1$. To this end, the two sets of filters should be designed to cancel totally the crosstalk between the channels and eliminate completely the amplitude and phase distortion arising out of the nonideal nature of these filters [44]–[46]. In TDM-FDM conversion applications, the output of the synthesis bank is converted into analog form by means of a D/A converter. The D/A converter output is then converted back into a digital form by means of an A/D converter and applied to the analysis filter bank. A more efficient realization is obtained by making use of a polyphase structure for the set of synthesis filters and for the set of analysis filters, and moving the up-samplers and the down-samplers to the middle as shown in Fig. 22(b).

As in the case of the QMF-based A/D converters, a mixed digital-switched-capacitor realization is feasible for the implementation of the transmultiplexer. The single high-speed D/A converter in the common analog channel can be replaced by a set of N low-speed D/A converters in the synthesis branches and, likewise, the single high-speed A/D converter can be replaced by a set of N low-speed

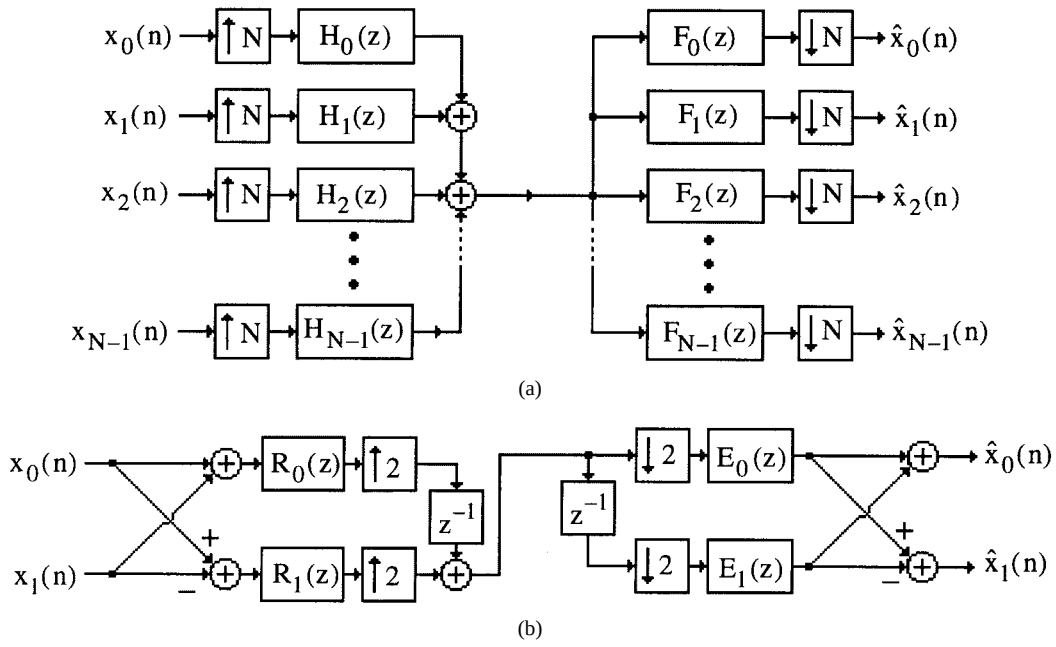

Fig. 22. (a) Basic N-channel transmultiplexer structure and (b) an efficient implementation of a two-channel transmultiplexer structure.

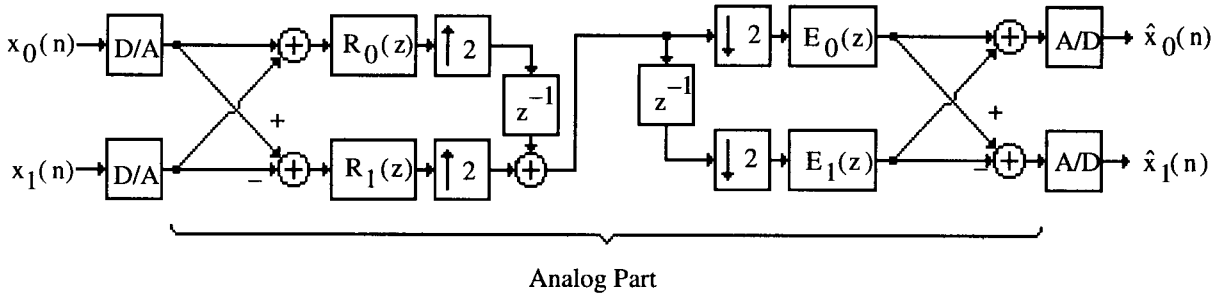

Fig. 23. Architecture for an efficient SC implementation of a two-channel transmultiplexer.

A/D converters in the analysis branches as indicated in Fig. 23, where the analog part can be implemented using SC technology.

D. Narrowband Filtering

Narrowband filtering is another important communication application where frequency-translated signals are processed through a multirate system [7]. In the schematic block diagram of Fig. 24, frequency-translating an input signal with high frequency components to a lower processing frequency and back to an output signal with high frequency components has the property that the absolute bandwidth is preserved and, therefore, the relative bandwidth of the SC bandpass filter at the heart of the system is reduced. In this way, it is practically feasible to realize relative bandwidths well below 1% which cannot be realized using conventional single-rate SC filtering circuits. It has been shown that the conditions for avoiding aliasing distortion and imaging associated with the frequency-translation operations may be met by anti-aliasing and anti-imaging filters which, rather than having the conventional lowpass shape, have instead bandpass responses to select one of the high-frequency bands at the input and the output, as illustrated in Fig. 25. More importantly, the practical realization and experimental characterization of such a system indicated the dynamic range of more than 70 dB that can be achieved with this solution is comparable to that of a more conventional single-rate bandpass filtering system with much larger relative bandwidths [47]. Thus the multirate structure of Fig. 24 offers a superior performance over alternative single-rate solutions for realizing narrowband filters [6].

VI. Future Trends

Having reviewed the fundamentals of discrete-time multirate systems and discussed some application areas where mixed analog-digital multirate systems are used, both for signal processing and for converting between analog and digital signals, we now look at several new possible applications of mixed analog-digital multirate systems.

A. Mixed A/D Implementation of N-Path Filters

Circuits with periodically time-varying parameters are an attractive alternative to circuits with constant parameters.

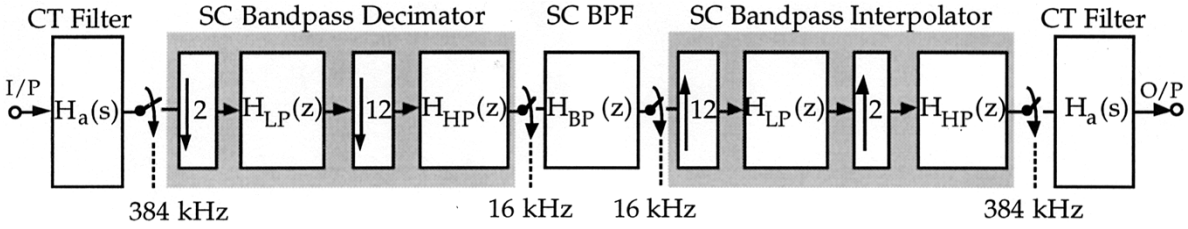

Fig. 24. Example of a multirate analog architecture for narrowband filtering.

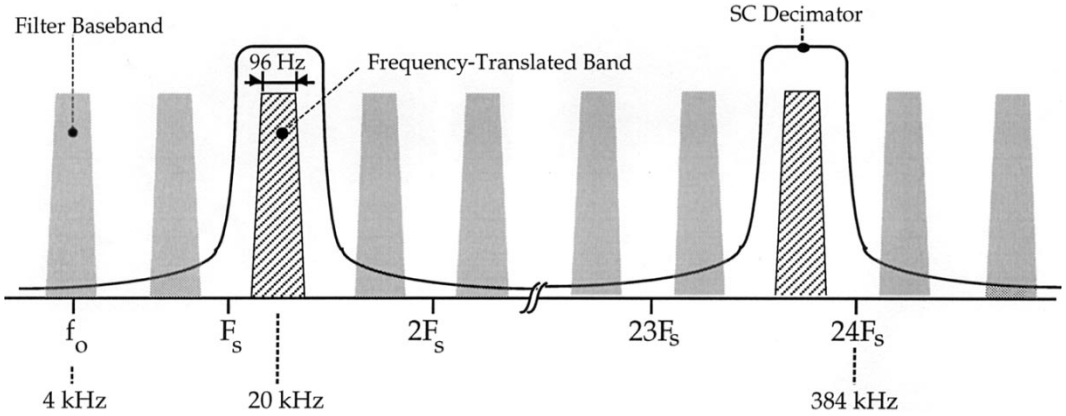

Fig. 25. Frequency-translated band selection in a multirate system for narrowband filtering using bandpass decimators and interpolators.

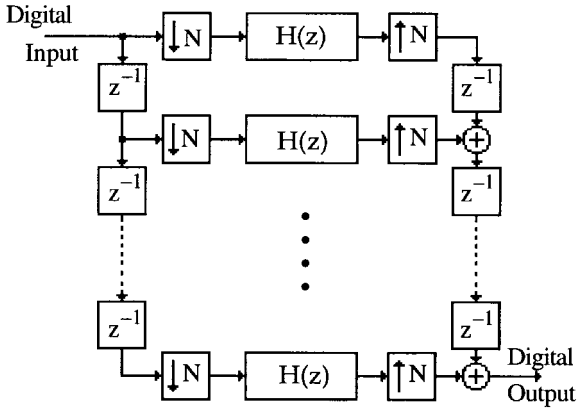

Fig. 26. All-digital N-path filter structure.

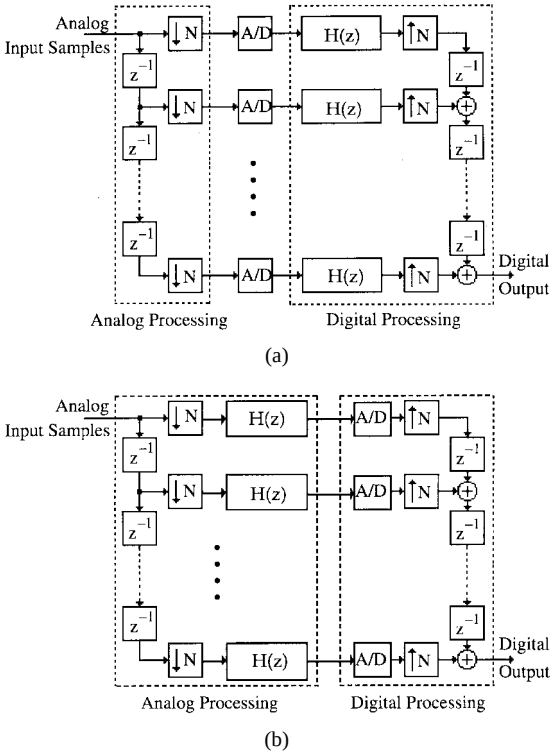

Fig. 27. (a) Predominantly digital and (b) predominantly analog implementations of an A/D N-path architecture for narrow bandpass filtering and high-frequency A/D conversion.

Some of the attractive features of the former are the following.

1) In some cases, they can be designed to match the response of equivalent constant parameter circuits with less computational complexity.
2) They can be designed to exhibit time-invariant components.
3) The filter characteristics can easily be made adjustable by electronic means by controlling the phase, frequency, and harmonic content parameters of the oscillators providing the periodic signals for the time-varying parameters.

The N-path filter, originally introduced for the processing of analog continuous-time signals [48], consists of N identical time-invariant filters, to each of which a common input signal path and a common output signal path are periodically connected synchronously through appropriate modulators. For certain band limited modulating functions, or certain band limited input and output signals, the overall time-varying structure can be made to appear as a time-

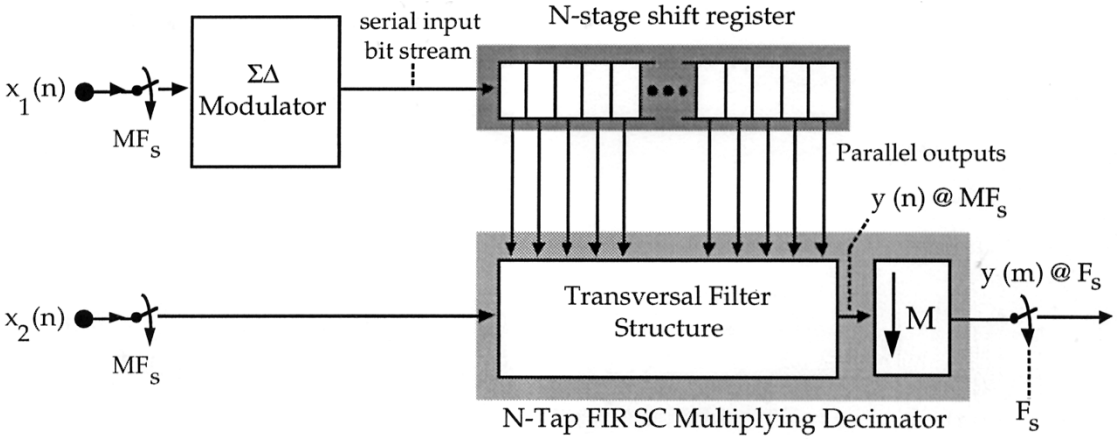

Fig. 28. Architecture of a four-quadrant multiplier employing a multirate A/D system combining digitally modulated sigma-delta and analog sampled-data signals.

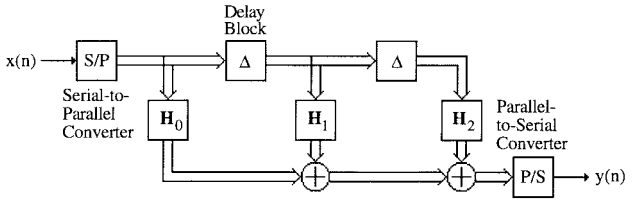

Fig. 29. Illustration of the block implementation of an FIR filter, for $L = 3$.

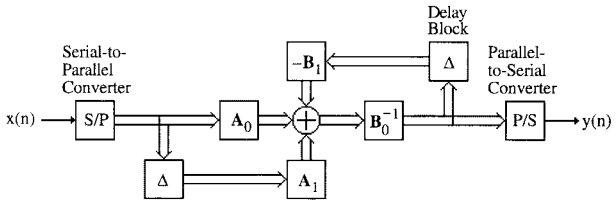

Fig. 30. Illustration of the block implementation of an IIR filter.

invariant network, which leads to its possible practical advantages pointed out earlier. However, the difficulty in ensuring the analog filter paths to be identical has made it difficult to implement the overall structure in a monolithic integrated circuit to reap its benefits. One way to overcome the problem of mismatches between the N paths is by using the pseudo N-path principle [49]. The SC technology has provided a practical method for the fully integrated realization of high-quality narrowband filters based on the N-path concept, as, for instance, in [50] and [51]. The N-path concept has also been extended to all-digital structure by Mitra *et al*. [52]. One particularly attractive form of the all-digital N-path filter is indicated in Fig. 26.

An area of potential interest for the N-path approach is in mobile radio system applications, where low power is a major concern. (An integrated CMOS circuit, which implements a tone receiver/generator using this approach, is described in [53].) For this purpose, the design of a mixed analog-digital N-path architecture is currently being investigated by the authors [54]. A predominantly digital form of implementation of such system is illustrated in Fig. 27(a), consisting of an analog front end serial/parallel converter and an A/D converter followed by a digital filter in each path. It should be noted that all of the attractive features of the all-analog N-path filters are also present in such mixed-signal implementation. For example, relatively simple digital filters in each path can be used to generate an overall filter with a highly selective bandpass filter. Moreover, as in the pseudo-N-path approach, a high-speed digital filter can be time-multiplexed N times to make it look like N separate filters, thus ensuring that each path of the N-path structure is identical. In the alternative, predominantly analog form of implementation shown in Fig. 27(b), an analog sampled-data decimator is placed in front of the channel analog-digital circuits (ADC's) working at a lower sampling frequency and thus allowing for possible savings in power dissipation in the conversion blocks. In this case, however, the analog decimation filter blocks may not be as well as matched as their digital counterparts in Fig. 27(a) and hence yielding a probable increase of inband spurious signals in the overall bandpass filter responses of the system.

B. Multirate Analog-Digital Processing with Delta-Sigma Modulated Signals

Combining analog and delta-sigma modulated sampled-data signals has been shown to be an efficient way of performing signal processing functions that would be much more difficult to realize using purely analog or digital circuitry [55]. Such truly mixed analog-digital multirate processing appears to be particularly attractive for applications involving the multiplication of two signals, as illustrated in the architecture of Fig. 28 [56]. Here, the delta-sigma modulator encodes one continuous-time input signal into a bit stream at high frequency MF_s whose highpass noise shaping is then lowpass filtered by the SC decimator with M-fold sampling reduction.

The above type of mixed analog-digital multirate processing is also being explored for such important communication applications as signal detection in highly degraded noise environments [55]. It is expected that such mixed analog-digital integrated system approach will lead to more

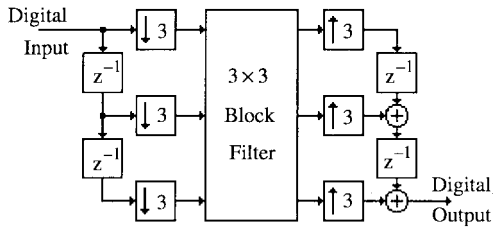

Fig. 31. A schematic multirate interpretation of block processing.

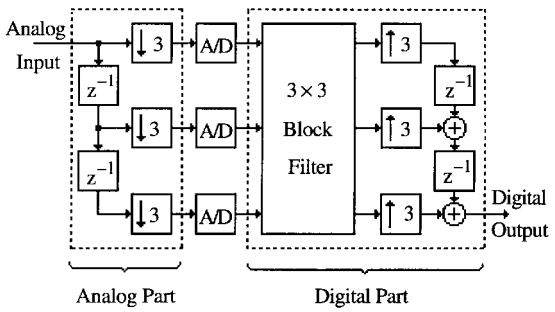

Fig. 32. Illustration of a monolithic signal processor implemented by placing an array of low-speed A/D converters between a serial/parallel register and a block filter.

efficient and economical solutions than would be possible to obtain using merely DSP techniques, which would have to be interfaced with the analog world through very high performance, and thus expensive, interface subsystems.

C. Block Implementation of Digital Filters [57]

Monolithic implementations of digital signal processors with on-chip A/D and D/A converters have become feasible due to the developments of mixed analog-digital CMOS-based technologies, including BiCMOS technology which combines the high integration density and low power consumption of CMOS with the high-speed and driving capability of bipolar transistors. With this technology it is also possible to fabricate other types of analog and digital circuitry on the same chip, in which signal processing can be performed partially in analog form and partially in digital form. On the other hand, as noted by Black [23], [24], the difficulties of implementing single chip processors for high-frequency applications include the large die areas occupied by high-speed A/D converters, and the realization of very fast digital filters. In video applications, the flash conversion approach is still the most popular method for A/D conversion. However, in addition to the large die area associated with this technique, the inevitable input capacitance resulting from paralleling many comparators may seriously limit the achievable conversion speed.

In this section we discuss alternative mixed analog-digital architectures which exploit the savings in the die area achieved with the use of an array of low speed successive approximation A/D converters, and the high-speed implementation of FIR and IIR filters by using block filtering techniques. The potentially high-speed processing achieved with this approach comes from the parallelism of both the A/D conversion and the digital filtering stages, as described next.

Consider a linear, time-invariant causal FIR digital filter characterized by an impulse response $h(n)$ of length N. The input-output relation of this filter is given by the convolution sum

$$y(n) = \sum_{r=0}^{N-1} h(i)x(n-r), \qquad n \geq 0 \tag{14}$$

where $x(n)$ and $y(n)$ are, respectively, the input and output sequences. The above equation permits a sequential computation of the output, one sample at a time, beginning with $y(0)$. The output sequence of an FIR filter can also be computed in blocks of length L with $L \leq N$ by rewriting (14) in a block-convolution form given by

$$\boldsymbol{Y}_k = \sum_{i=0}^{N-1} \boldsymbol{H}_i \boldsymbol{X}_{k-i} \tag{15}$$

where $\boldsymbol{X}_k$ and $\boldsymbol{Y}_k$ are, respectively, the kth input and output blocks of length L:

$$\boldsymbol{X}_k = [x(kL) \quad x(kL+1) \cdots x(kL+L-1)] \tag{16}$$

$$\boldsymbol{Y}_k = [y(kL) \quad y(kL+1) \cdots y(kL+L-1)] \tag{17}$$

and $\boldsymbol{H}_k, k = 0,1,2,\cdots,L-1$, are $L \times L$ matrices composed of the impulse response coefficients. A block implementation of an FIR filter for $L = 3$ is sketched in Fig. 29.

Likewise, in the case of an Mth order IIR filter characterized by a transfer function given by

$$H(z) = \frac{\sum_{i=0}^{M} a_i z^{-i}}{\sum_{i=0}^{M} b_i z^{-i}} \tag{18}$$

one possible block representation is of the form

$$\boldsymbol{Y}_{k+1} = -\boldsymbol{B}_0^{-1}\boldsymbol{B}_1\boldsymbol{Y}_k + \boldsymbol{B}_0^{-1}\boldsymbol{A}_0\boldsymbol{X}_{k+1} + \boldsymbol{B}_0^{-1}\boldsymbol{A}_1\boldsymbol{X}_k \tag{19}$$

where $\boldsymbol{B}_0$, $\boldsymbol{B}_1$, $\boldsymbol{A}_0$, and $\boldsymbol{A}_1$ are $L \times L$ matrices $(M \leq L)$ composed of the transfer function coefficients. A block implementation of an IIR filter based on (19) is sketched in Fig. 30. A multirate interpretation of block processing is indicated in Fig. 31 for $L = 3$.

D. Mixed Analog-Digital Implementation of Block Filtering

The block processing approach lends itself easily for the digital processing of analog signals, as we show next. A monolithic signal processor can be implemented if an array of low-speed A/D converters is placed between the serial/parallel register (which can be implemented by charge coupled devices (CCD) or SC networks) and the block filter as indicated in Fig. 32. Alternatively, the block convolution can be realized using DFT methods which, in turn, can be implemented by CCD or SC networks. In this case the DFT operation can be removed from the block digital filtering stage and placed between the decimators and the A/D array.

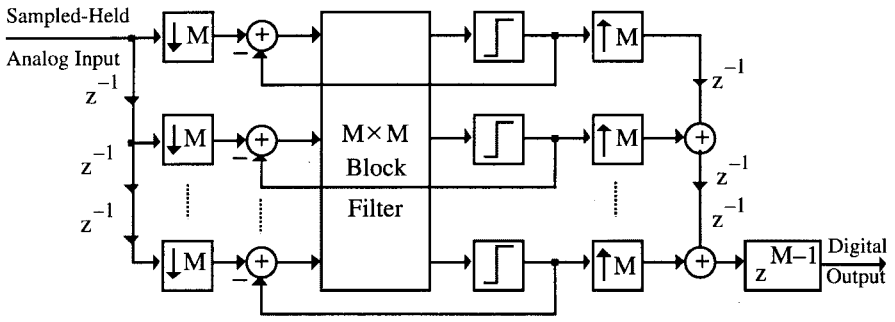

Fig. 33. A time-interleaved oversampling converter with M interconnected modulators increases the effective oversampling ratio, and hence the resolution for conversion, by a factor M [58].

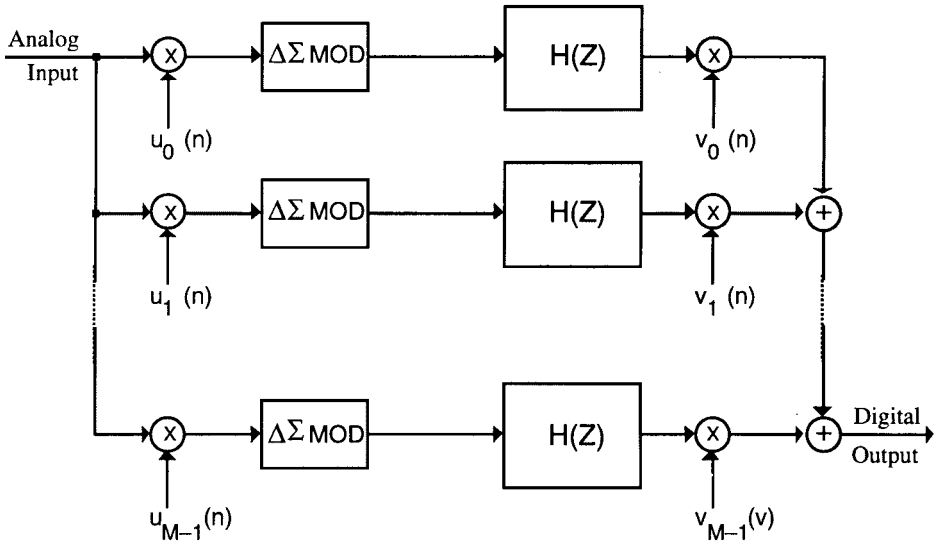

Fig. 34. A parallel delta-sigma architecture for A/D conversion employs Hadamard modulation to achieve (ideally) cancellation of quantization noise and hence increasing the equivalent resolution without increasing the oversampling of the delta-sigma modulators [59], [61].

An architecture has been proposed in [24] where the outputs from separate converters are processed independently by identical digital processors, in much the same way of the so-called N-path technique, which is suited for applications requiring very selective bandpass or band reject filters. A major drawback of such a technique is that any mismatch among the path processors add to the mismatches among the A/D converters in the array, thus increasing the distortion at the output. However, by moving the DFT stage to the front of the system it is possible to reduce the effect of mismatches in the A/D array [21], since the DFT acts as a filter bank.

E. Time-Interleaved and Parallel Oversampling Converters

The emergence of new mixed analog-digital applications with wide-bandwidth requirements, e.g., HDTV, ASDL/HSDL, multichannel transceivers, and high-energy particle detectors, among others, has accelerated the need for the implementation of high-speed high-resolution converters. Two new time-interleaved/parallel architectures employing delta-sigma modulators have been recently proposed for such high-resolution high-speed applications [58]–[62].

The basic architecture of a time-interleaved oversampling converter, schematically illustrated in Fig. 33, is derived

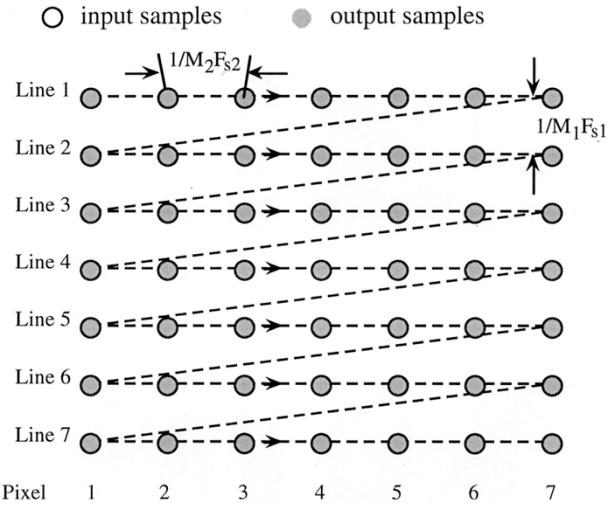

Fig. 35. Raster-type 2-D sampled signal.

by combining the architecture of a block digital filter (e.g., see Fig. 29) together with a conventional delta-sigma structure [58]. It has been shown, both in theory and experimentally, that the effective oversampling ratio of M interconnected delta-sigma modulators is increased by a factor of M without increasing the basic operating speed of the modulators. This, in turn, yields an increase of the

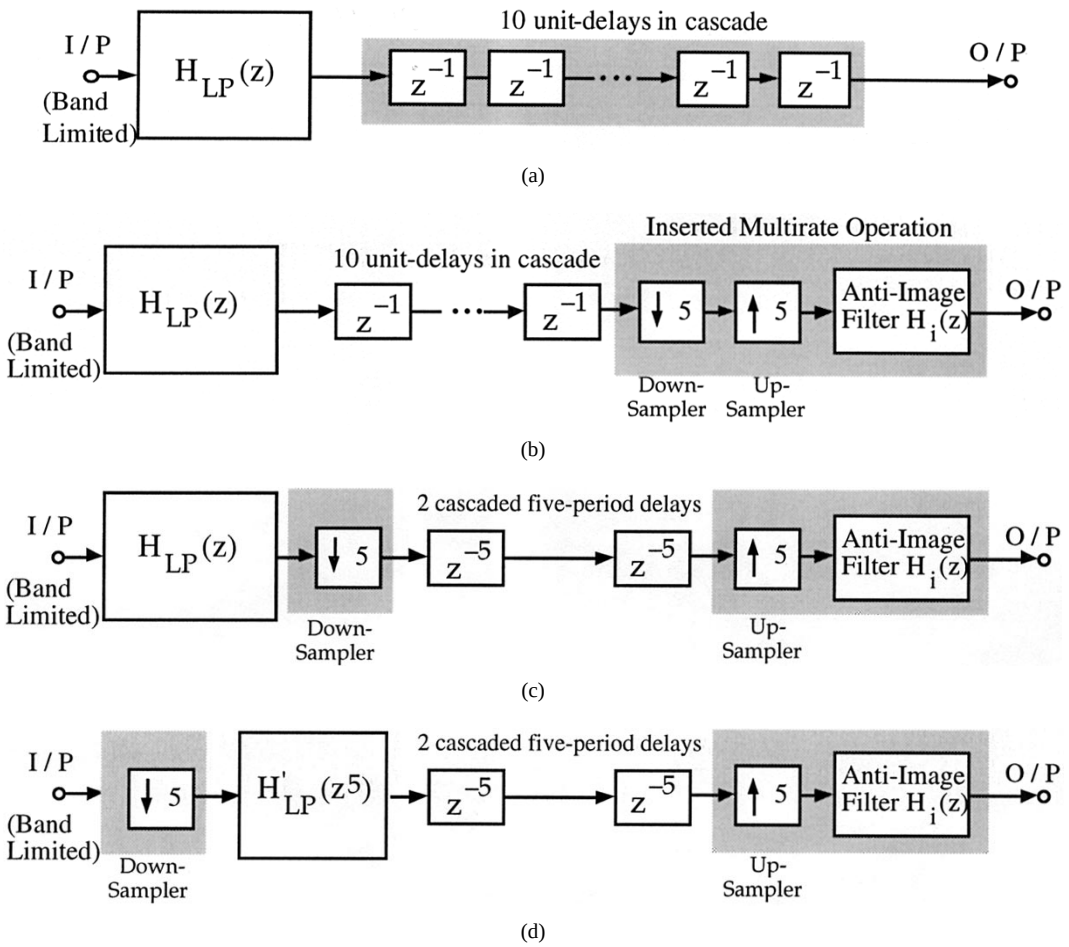

Fig. 36. Relaxing both the circuit size and the operating speed of a filtering system using multirate techniques: (a) traditional 1-D filtering system cascaded with a delay chain of 10 unit delays, (b) inserting an equivalent multirate operation, (c) moving the decimator to the front of the delay chain, and (d) moving the decimator to the front of the filter.

SNR in the baseband and hence the equivalent resolution for conversion also increases. Alternatively, the same resolution can be maintained with wider bandwidth input signals. Because of their intrinsic parallel nature, this type of converters is also subject to the same mismatch effects experienced by the N-path structures discussed above. A method has been proposed that alliviates the resulting performance deterioration by reducing the spectrum energy in the vicinity of the bands of concern that give rise to aliasing [60].

An alternative parallel oversampling architecture that achieves a similar increase of accuracy by interconnecting M delta-sigma modulators is shown in Fig. 34 [59], [61], [62]. By contrast with the previous architecture, the combination of the multiple modulators in this architecture is performed using simple Hadamard modulators. The effect of such modulators is to achieve an additional filtering effect of the quantization noise generated by each delta-sigma modulator without interfering with the main signal path. This increases the SNR in the passband and hence increases the equivalent resolution for conversion, in a similar way as in the previous structure. The filtering of the quantization noise produced by the Hadamard modulators is based on the ideal cancellation of signals. In practice, the level of such cancellation is limited by mismatch effects in the parallel structure but which can be minimized by appropriate calibration and compensation techniques [62].

F. Two-Dimensional Analog Filtering

Two-dimensional (2-D) filtering is another area where multirate analog structures can play an interesting role by providing improved low cost integrated implementations for future applications requiring high-speed processing but with moderate accuracy (e.g., machine vision and robotics [63]).

The 2-D analog signals processed by 2-D SC filters are usually scanned line by line, from left to right and from top to bottom, as depicted in the illustration of Fig. 35 where the horizontal sampling frequency is (M_2F_{s2}) and the vertical sampling frequency is (M_1F_{s1}). For filtering, the current output pixel is obtained from previous pixels in the current and previous lines. Pixels from previous lines are stored using delay-line memories whose size is (M_2F_{s2}/M_1F_{s1}). Both sampling frequencies are usually much higher than the signal bandwidth to maintain a good picture quality, but for ease of signal processing and practical hardware implementation it is highly desirable to reduce the sampling ratio between the input and the output of the filtering system [64]–[66].

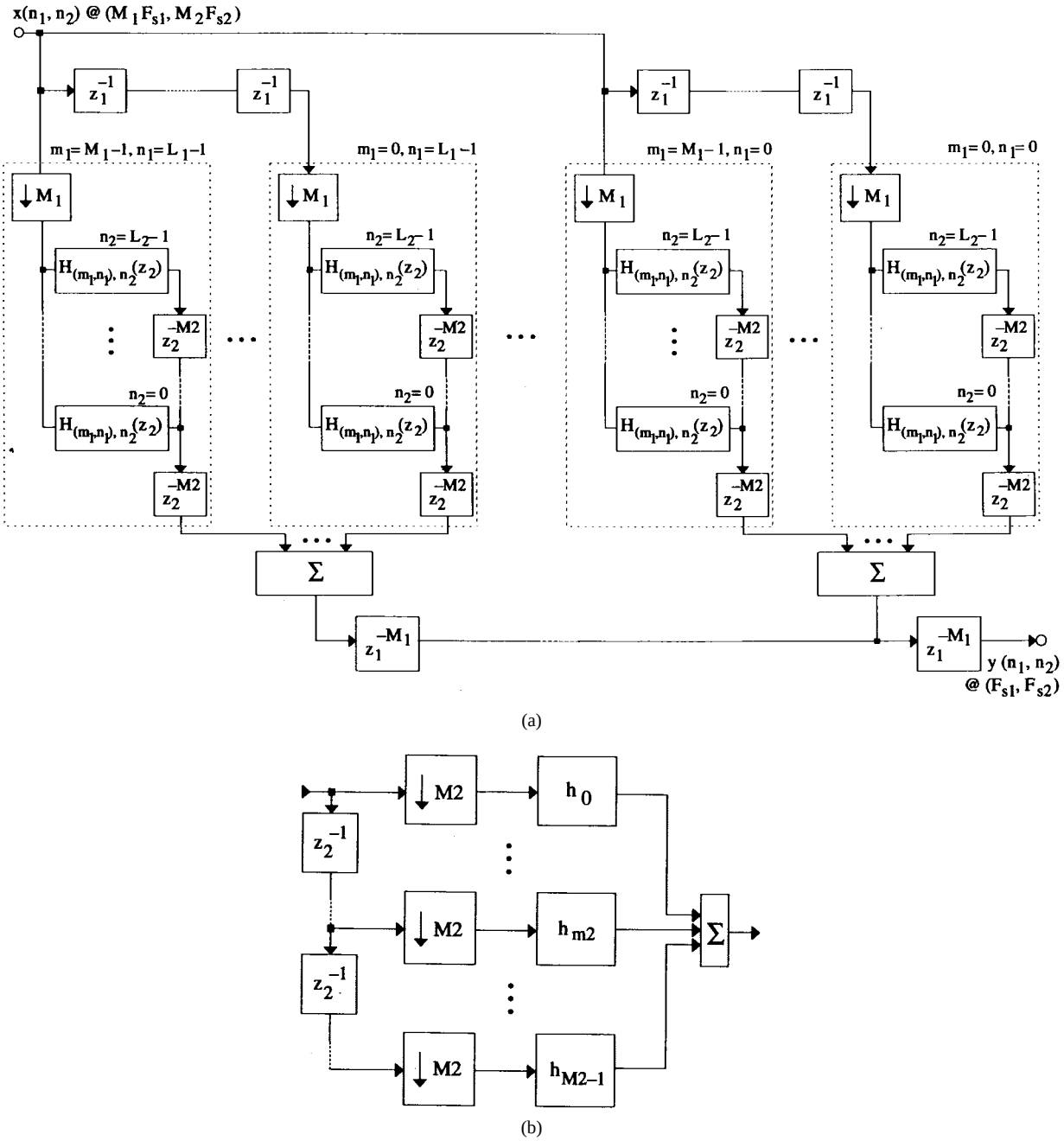

Fig. 37. Direct form nonrecursive polyphase structure for 2-D filtering. (a) Schematic diagram of the inner processing block corresponding to, and (b) complete structure.

To illustrate the above, consider first the block diagram of Fig. 36(a) where the one-dimensional (1-D) lowpass filtering system $H(z)$, with bandlimited input signal, is followed by a delay chain of ten unit delays. In Fig. 36(b) a multirate operation consisting of a five-fold decimation followed by a five-fold interpolation and an ideal anti-image filter is inserted between those delays and the output terminal. According to the multirate filtering concepts discussed earlier, such modified multirate system is equivalent to the one of Fig. 36(a). The decimator in Fig. 36(b) can be placed in front of the delay chain yielding only two five-unit delays following the filter $H(z)$, as illustrated in Fig. 36(c). By moving the decimator further to the front of filter, as shown in Fig. 36(d), $H(z)$ becomes $H'(z^5)$ and hence the operating speed of the system is also reduced five-fold since the new unit delay is now equivalent to a delay of five sample periods in the previous time frame. Now, consider the system of Fig. 36(a) as a simple 2-D filter where $H(z)$ is the horizontal filter and the delay chain represents a simple vertical filter with delay-line size of ten memory cells. From the multirate system of Fig. 36(d) we see that the delay line size is reduced by five-fold. The decimator with filtering function $H'(z^5)$ is defined as the decimating filter in the horizontal dimension and which,

besides the required baseband filtering, should also provide the necessary anti-aliasing filtering.

Traditional 2-D SC filters require very large line-memories mainly because of the oversampled characteristic of the signal, both at the input and at the output. By bringing the output sampling rate closer to the Nyquist signal bandwidth it is possible to reduce considerably the line-memory requirements and thus saving silicon area and power dissipation for cheaper integrated circuit implementation. Besides, lower output sampling rates also contribute for ease of signal digitization and processing and economy of signal transmission. Such operation of reducing the sampling rate from the input to the output can be achieved using appropriate 2-D decimating filters which, besides the required baseband filtering, should also provide the necessary antialiasing filtering.

Let the general z-transfer function of a 2-D linear, causal, shift-invariant FIR filter be expressed as

$$H(z_1, z_2) = \sum_{n_2=0}^{N_2-1} \sum_{n_1=0}^{N_1-1} h(n_1, n_2) z_1^{-n_1} z_2^{-n_2} \tag{20}$$

where N_1 and N_2, respectively, represent the prototype filter length in the z_1 and the z_2 dimensions. The z_1^{-1} delay term refers to the input sampling frequency of $M_1 F_{s1}$ along the vertical axis whereas the z_2^{-1} delay term refers to the input sampling frequency of $M_2 F_{s2}$ along the horizontal axis.

In the general case when decimation occurs in both dimensions the prototype expression given by (20) can be rewritten as

$$H(z_1, z_2) = \sum_{n_1=0}^{L_1-1} \left[\sum_{m_1=0}^{M_1-1} h_{1,m_1+n_1M_1}(z_2) z_1^{-m_1} \right] (z_1^{M_1})^{-n_1} \tag{21}$$

where

$$h_{1,m_1+n_1M_1}(z_2) = \sum_{n_2=0}^{L_2-1} \left[\sum_{m_2=0}^{M_2-1} h(m_1 + n_1M_1, m_2 + n_2M_2) z_2^{-m_2} \right] (z_2^{M_2})^{-n_2}. \tag{22}$$

In the above equations, M_1 and M_2 are the decimation factors whereas L_1 and L_2 represent, respectively, the number of subfilters in both dimensions. By defining 2-D polyphase coefficients as

$$\overline{h}_{i,j}(z_1, z_2) = \sum_{m_1=0}^{M_1-1} \sum_{m_2=0}^{M_2-1} h(m_1 + n_1M_1, m_2 + n_2M_2) z_2^{-m_2} z_1^{-m_1} \tag{23}$$

we obtain the more compact expression

$$H(z_1, z_2) = \sum_{n_1=0}^{L_1-1} \sum_{n_2=0}^{L_2-1} \overline{h}_{i,j}(z_1, z_2) (z_2^{M_2})^{-n_2} (z_1^{M_1})^{-n_1} \tag{24}$$

which can be implemented using the 2-D direct-form decimating polyphase structure of Fig. 37 [67] comprising $z_1^{-M_1}$ and $z_2^{-M_2}$ delayed blocks [38]. The subscripts (m_1, n_1) denote the m_1th impulse response coefficient in the n_1th subfilter in the vertical dimension, whereas subscripts (m_2, n_2) represent the m_2th impulse response coefficient in the n_2th subfilter in the horizontal dimension. Therefore, one 2-D impulse response coefficient in such structure must be expressed by four parameters: for example, the coefficient $h(m_1 + n_1M_1, m_2 + n_2M_2)$ corresponds to a coefficient between the (m_1, n_1)th subfilter in z_1 and the (m_2, n_2)th subfilter in z_2.

Alternative architectures for 2-D multirate filtering can be derived for linear, causal, shift-invariant IIR 2-D filters with separable denominator polynomials and which can be expressed as

$$H(z_1, z_2) = \frac{\sum_{n_1=0}^{N_1-1} \sum_{n_2=0}^{N_2-1} a_{n_1,n_2} z_2^{-n_2} z_1^{-n_1}}{\left(1 + \sum_{n_1=1}^{N_1-1} b_{n_1} z_1^{-n_1}\right)\left(1 + \sum_{n_2=1}^{N_2-1} b_{n_2} z_2^{-n_2}\right)} \tag{25}$$

where, as before, z_2^{-1} and z_1^{-1} are, respectively, the unit delay periods referring to the input sampling frequencies $M_2 F_{s2}$ and $M_1 F_{s1}$.

Considering again the general case of multirate processing in both dimensions we arrive at the 2-D IIR decimating transfer function (see (26) at the bottom of the page) where the coefficients p_{k_1} and q_{k_2} are determined in a similar way as for the simpler IIR 1-D case. After defining the 2-D

$$H(z_1, z_2) = \frac{\left(\sum_{n_1=0}^{N_1-1} \sum_{n_2=0}^{N_2-1} a_{n_1,n_2} z_2^{-n_2} z_1^{-n_1}\right)\left(\sum_{k_1=0}^{(M_1-1)(N_1-1)} p_{k_1} z_1^{-k_1}\right)\left(\sum_{k_2=0}^{(M_2-1)(N_2-1)} q_{k_2} z_2^{-k_2}\right)}{\left(1 + \sum_{n_1=1}^{N_1-1} b_{n_1} z_1^{-n_1}\right)\left(1 + \sum_{n_2=1}^{N_2-1} b_{n_2} z_2^{-n_2}\right)\left(\sum_{k_1=0}^{(M_1-1)(N_1-1)} p_{k_1} z_1^{-k_1}\right)\left(\sum_{k_2=0}^{(M_2-1)(N_2-1)} q_{k_2} z_2^{-k_2}\right)} \tag{26}$$

polyphase coefficient as

$$\overline{A}_{n_1,n_2}(z_1,z_2)=\sum_{m_1=0}^{M_1-1}\sum_{m_2=0}^{M_2-1}\cdot A(m_1+n_1M_1,m_2+n_2M_2)z_2^{-m_2}z_1^{-m_1} \tag{27}$$

and carrying out simple algebraic manipulations we arrive at the more compact expression

$$H(z_1,z_2)=\frac{\sum_{n_1=0}^{N_1-1}\sum_{n_2=0}^{N_2-1}\overline{A}_{n_1,n_2}(z_1,z_2)(z_2^{M_2})^{-n_2}(z_1^{M_1})^{-n_1}}{\left[1+\sum_{n_1=1}^{N_1-1}B_{n_1}(z_1^{M_1})^{-n_1}\right]\left[1+\sum_{n_2=1}^{N_2-1}B_{n_2}(z_2^{M_2})^{-n_2}\right]} \tag{28}$$

to describe the digital transfer function of the 2-D IIR decimation filter. From this, we can readily obtain the corresponding decimating architecture combining the type of ADB structure represented in Fig. 37 together with 2-D recursive network realizing the denominator function [69].

SC discrete-time networks have been proposed for the analog implementation of the above 2-D multirate structures [70], both with FIR and IIR digital transfer functions, and their practical feasibility for integrated circuit fabrication has also been demonstrated in a 1.0 μm CMOS prototype chip [71].

VII. Concluding Remarks

This paper has presented an overview of the most recent developments in the area of multirate signal processing, including digital, analog, and mixed-signal analog-digital. After reviewing some basic aspects of multirate analog-digital systems and signals, a generalized multirate analog–digital system architecture for digital processing of analog signals has been presented leading to the conventional system architectures employed today. Bearing in mind the state-of-the-art technologies which allow the strategic objective of high quality analog-digital integration, we then described various multirate systems for SC, including the popular oversampling converters as well some new architectures based on the QMF banks, and for signal processing, including an analog front-end filtering subsystem for video processing, analog-digital multirate systems for FDM and FDM/TDM transmultiplexing, and also a multirate system for very narrowband bandpass filtering. Finally, the paper addressed some recent research topics in the areas of signal detection, multidimensional filtering and bank filtering, which show potential for future expansions, and where the benefits of multirate analog-digital integrated systems can be fully exploited for integrated circuit implementation using modern technologies.

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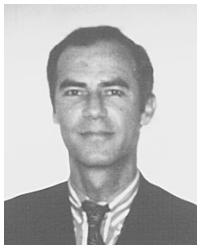

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