# Time Interleaved Converter Arrays

WILLIAM C. BLACK, JR., MEMBER, IEEE, AND DAVID A. HODGES, FELLOW, IEEE

*Abstract*—High-speed monolithic converters normally use a variation of the flash technique, which uses $2^n$ comparators in parallel to obtain a fast $n$-bit conversion. Although this method allows for high converter bandwidth, it is not very area efficient, and results in large die sizes for even modest resolution converters. In the technique presented here, a number of small but area efficient converters are operated in a time-interleaved fashion to achieve the bandwidth of a flash circuit, but in a substantially smaller area. This technique is analyzed with respect to noise and distortion resulting from nonideal array characteristics, and is demonstrated by way of a four-way array test-chip. This chip consists of four time-interleaved 7-bit weighted-capacitor A/D converters, fabricated in a 10 $\mu$m metal-gate CMOS process. Full 7-bit linearity is maintained up to a 2.5 MHz conversion rate, with operation at reduced linearity continuing to approximately 4 MHz. The design of this chip, and anticipated characteristics if fabricated in a modern 4–5 $\mu$m process are described.

## I. Introduction

THE advantages of digital signal processing and storage techniques could be brought to many new application areas, such as commercial television receivers, if high-speed monolithic analog-to-digital (A/D) converters were available at a sufficiently low cost. As present-day monolithic converters use techniques which require large die sizes and/or fairly exotic fabrication processes, these circuits have remained too expensive for many applications. Furthermore, these A/D techniques will be exceedingly difficult to integrate along with a VLSI digital signal processor because of the large A/D die-size and/or process bandwidth requirements.

In the method presented here, the die-size and/or process requirements of a high-speed converter are considerably reduced, by employing the converter-array technique shown in Fig. 1. In this approach, a number of small converters with interleaved sampling times are used as if they are effectively a single converter operating at a much higher sampling rate. Analysis has shown that this technique may be used to achieve a considerable reduction in die-size and power dissipation over other circuits, without sacrificing bandwidth or signal to noise ratio. This method is easily implemented in an MOS technology, allowing on-chip compatibility with dense digital signal processors. Furthermore, this technique may be used to achieve faster sampling rates than are possible with any single converter.

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The authors are with the Department of Electrical Engineering and the Electronics Research Laboratory, University of California, Berkeley, CA 94720.

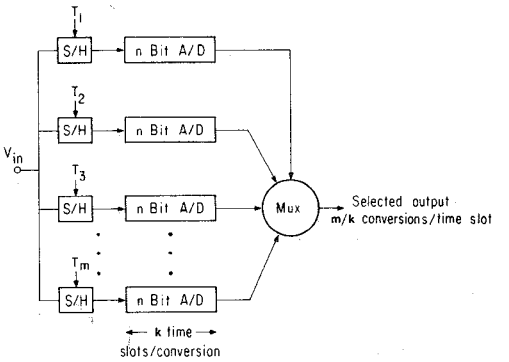


Fig. 1. Converter array technique uses a number of converters with interleaved sampling times to achieve a fast effective conversion rate. An $n$-bit, $m$-way array is shown.

## II. Comparison of High-Speed Converter Methods

Most high-speed monolithic converters can be grouped into one of three basic types: the one-step flash, two-step flash, and successive approximation techniques. In the first method [1], [2], $2^n$ comparators are used in parallel to obtain a fast $n$-bit conversion. Although this technique allows for large converter bandwidth, it results in large die sizes for $n > 6$, and has not been practical for $n > 8$. In the second approach, two sets of smaller flash arrays (typically of $n/2$ bits each) are used in sequence to obtain a fairly fast conversion rate ($\sim\frac{1}{2}$ of straight flash), yet in a modest die area. This technique has been used to realize a 7-bit video converter in a double-level metal bipolar process [3], although very fast MOS converters of this type would be difficult to implement due to the reduced converter throughput. In the last approach, a simple successive approximation technique is used, but in a very fast process [4]. This technique is perhaps the smallest in area per converter, but is also the slowest in a given process. It is doubtful whether this method by itself will soon be used in any MOS converter circuit which achieves video bandwidths.

A summary of the relevant characteristics of these techniques is presented in Table I. In this table, it has been assumed that each method has been implemented in a similar MOS process, and where relative values may vary by perhaps 30 percent depending upon specific assumptions. It has been assumed for the successive approximation converters, that binary-weighted capacitors [5], or their equivalent, are used in the respective designs.

A figure of merit which is rarely cited in converter literature, is the relative throughput per unit chip area. This is listed for each of the converter types in the last column of Table I. As is evident, the converters which display the best area efficiency

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TABLE I
SUMMARY OF HIGH-SPEED MOS A/D CONVERSION TECHNIQUES ($n$-BIT)

| Method | Relative Die Size D | Time Slots per Conversion T (n=7) | Throughput per Area $1/(D \cdot T)_{n=7} \times 10^3$ |
|---|---|---|---|
| • 1-Step Parallel (Flash) | $2^n$ | 2 | 4 |
| • 2-Step Parallel (1/2-Flash) | $3 \cdot 2^{n/2}$ | 3-4 | 7-9 |
| • n-Step Sequential (Succ. Approx.) | 1.5n | n+1,(8) | 12 |
| • 4-Way Successive Approx. Array | 4(1.5n) | (n+1)/4,(2) | 12 |

are in fact those with the lowest throughput. Thus, although the successive approximation technique is slower than either of the flash circuits, it usually will use its area more efficiently. It would be desirable if a technique could be developed which would allow the throughput of flash circuits to be obtained, yet with the area efficiency of the successive approximation method. As is indicated in the last row of Table I, an array of interleaved successive approximation converters may be used to achieve this desired end. Note that for the 7-bit case, 4 parallel converters are needed to achieve a throughput equal to that of the flash approach, but with only a third of the required die-size. This area savings becomes even more pronounced at higher resolution levels [6].

## III. Error Analysis

### A. Total Quantizing Error

This array technique may be used with nearly any type of A/D converter. As will be shown, however, a variation of converter quantizing characteristics within an array may introduce additional noise or distortion. This will tend to make some converter types more suitable for use in arrays than others, and may result in a slightly increased component matching requirement for a specified performance level.

A commonly used measure of an A/D converter's dynamic performance is the single-frequency signal-to-noise ($S/N$) ratio. In this test, a typically full-scale sinusoidal signal is fed into the A/D to be measured, as shown in Fig. 2. The output of the A/D is then reconstructed with a high-quality digital-to-analog (D/A) converter, and bandlimited to the Nyquist rate of the sampler or below. The ratio of the measured power at the original signal frequency to all other measured power is the single frequency signal to noise ratio.[1] The power at nonfundamental frequencies, or the "error power," is due to the A/D converter displaying both finite resolution and limited linearity. This situation is depicted in Fig. 3, where a small section of an A/D converter's transfer characteristic is shown. From the figure the converter quantizing error is seen to be

$$\epsilon(x) = \delta(x) \tag{1}$$

where

$$\delta(x) = \hat{x} - (ax + b) \tag{2}$$

[1] This test, as indicated, will not detect delay distortion terms at the fundamental frequency. For these to be included, the notch filter of Fig. 2 must be made phase as well as frequency selective.

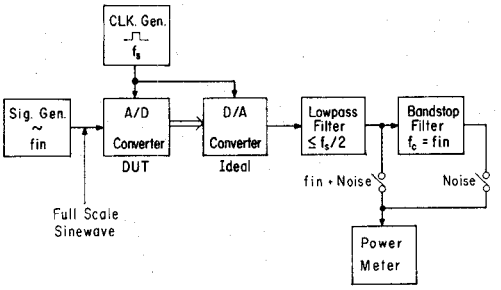



Fig. 2. Single-frequency signal-to-noise ratio test.

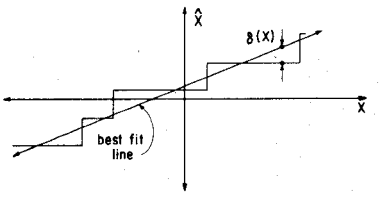



Fig. 3. Quantization and nonlinearity error in a single A/D converter.

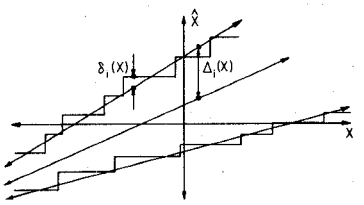



Fig. 4. Quantization and nonlinearity error in a converter array.

in which $\hat{x}$ is the quantized level of $x$, and $a$ and $b$ are error minimization terms corresponding to the best fit converter gain and offset. This results in an average error power (referred to 1 Ω) of simply

$$E_p = \langle \delta^2 \rangle \tag{3}$$

where $\langle \delta^2 \rangle$ indicates the mean or expectation value of $\delta^2$, and where $a$ and $b$ in (2) have been chosen to minimize $E_p$ for a specified input distribution.[2]

If instead of a single converter, an array of interleaved converters is employed, the error analysis becomes more involved. This situation is depicted in Fig. 4, where the transfer functions of two converters in an array are shown, each of which exhibits different gain, offset, and nonlinearity. For this case, the error in the $i$th converter is given by

$$\epsilon_i(x) = \delta_i(x) + \Delta_i(x) \tag{4}$$

where

$$\delta_i(x) = \hat{x}_i - (a_i x + b_i) \tag{5}$$

and

$$\Delta_i(x) = (a_i - a_{\min})x + b_i - b_{\min}. \tag{6}$$

[2] The best fit parameters $a$ and $b$ are usually near the converter gain and offset values as they are normally defined, however as shown in the Appendix, $a$ and $b$ are also dependent upon converter nonlinearities and the probability distribution of the input signal.

In these equations, $\delta_i(x)$ indicates the error that would exist if the $i$th converter were used alone, while $\Delta_i(x)$ indicates an additional error which exists when the $i$th converter is used as part of an array. The best fit gain and offset of the $i$th converter is represented by $a_i$ and $b_i$, while the best fit gain and offset of the array as a whole is given by $a_{min}$ and $b_{min}$.[3] This results in an average error power for an $m$-way array, of

$$E_p = \frac{1}{m}\sum_{i=1}^{m} \langle(\delta_i + \Delta_i)^2\rangle \tag{7}$$

which, for an input signal that is asynchronous with the sampling clock becomes

$$E_p \simeq \frac{1}{m}\sum_{i=1}^{m} [\langle\delta_i^2\rangle + \langle\Delta_i^2\rangle]. \tag{8}$$

This equation implies that converter gain and offset variations within an array will result in increased error power. These variations may be due to mismatches in gain or offset establishing components, or from differences in converter nonlinearities, which may result in a slightly different best fit gain and offset for each converter. In converters where these variations are well controlled, however, the array error power will be approximately the average of the individual error powers due to quantization and nonlinearity.

In both single and multiple converter applications, there is one additional source of error power: phase skew or jitter of converter sampling. Specifically, if the aperture timing of a converters sample and hold (S/H) circuit exhibits any variance in period, the overall error power will increase. Phase skew is particularly troublesome in converter arrays, as it may result from even a slight difference in timing line layout or loading between converters.

The amount of error power resulting from gain mismatch, offset mismatch, and sampling skew in a converter array is analyzed in the Appendix and summarized in Table II. To determine the overall signal to noise ratio of a converter array, the error powers listed in the second column need only be added together, along with the average error power due to individual nonlinearities, and compared with the original signal power ($V_{p\text{-}p}^2/8$). The relative sensitivies of the error power to different nonidealities are shown in the third column. In this comparison, the indicated variance of each of the three parameters, is that which produces a degradation of $S/N$ ratio to 40 dB when all other noise sources are zero. Note that the overall error power is least sensitive to gain variance and most sensitive to phase skew and jitter. As a point of reference, however, the gain matching requirement is actually twice as severe as the most significant bit component matching requirement of a single converter, for a nonlinearity limited $S/N$ ratio of 40 dB. This implies that arrays of converters which have a specific gain determining element, such as R-2R ladders, will have a more severe component matching requirement when used in an array then when used individually, for a specified $S/N$ ratio. Similarly, multiple flash circuits [2] may suffer from a reduced $S/N$ ratio, as "bow" errors will modify the effective converter gains and offsets. In converters employing binary-weighted capacitors (or the equivalent), this increase in the component matching requirement is usually small, although different nonlinearities will still result in slightly mismatched best-fit converter parameters. This weighted-capacitor technique is particularly attractive for use in converter arrays, in that, not only are there no specific gain setting components (which could potentially mismatch), but intrinsic comparator offsets (which could also mismatch) are easily cancelled [5].

[3] As shown in the Appendix, the minimizing values of the array parameters are simply $a_{min} = \bar{a}_i$ and $b_{min} = \bar{b}_i$.

TABLE II
MAGNITUDE AND SENSITIVITY OF ERROR POWER TO MISMATCH IN A CONVERTER ARRAY FOR AN INPUT SINUSOID CENTERED ABOUT ZERO

| Noise Source | Sinusoid Error Power | Requirement for Sinusoid S/N = 40 dB |
|---|---|---|
| Gain (a) Mismatch | $\frac{V_{p\text{-}p}^2}{8}\sigma_a^2$ | $\frac{\sigma_a}{\bar{a}} = 1\%$ |
| Offset (b) Mismatch | $\sigma_b^2$ | $\frac{\sigma_b}{V_{p\text{-}p}} = .71\%$ |
| Phase (t) Skew | $\frac{V_{p\text{-}p}^2}{8}\omega^2\sigma_t^2$ | $\frac{\omega\sigma_t}{2\pi} = .16\%$ |

$$\sigma_X^2 = \overline{X^2} - \overline{X}^2$$

### B. Spectral Distribution of Noise and Distortion

Of equal importance to the error power magnitude is the noise and distortion spectral distribution. Analysis of the power spectrum resulting from a gain mismatched array, is similar to that performed by Messerschmitt for the case of induced gain errors by "bit robbing" in digital channel banks [7]. For an $m$-way array with gain mismatch, an input signal of power spectrum $S_x(\omega)$ will result in a reconstructed output power spectrum (assuming impulse sampling) given by

$$S_{\hat{x}}(\omega) = |H(\omega) f_s|^2 \sum_{k=-\infty}^{\infty} |G_k|^2 S_x(\omega - kf_s/m) \tag{9}$$

where $H(\omega)$ is the transfer function of the reconstruction filter, $f_s$ is the sampling frequency, and $G_k$ is the discrete Fourier transform of gain in the array.

$$G_k = \frac{1}{m}\sum_{i=1}^{m} a_i\, e^{-j2\pi k(i-1)/m}. \tag{10}$$

The $k = 0$ case in (9) corresponds to the original signal component, while the remaining terms are a form of aliasing distortion. This distortion is demonstrated for the case of a sinusoidal input signal and a four-way array in Fig. 5(b), as compared with the ideal case in Fig. 5(a). As is evident from the figure, sidebands develop about fractions of the sampling rate, which are identical in spectral content to the original input signal. The relative magnitude of each sideband, which except for the $k = m/2$ case exist in pairs, is determined by the appropriate order of discrete transform as defined above. Note that for nonzero dc levels, gain errors will produce noise at exact multiples of $f_s/m$.

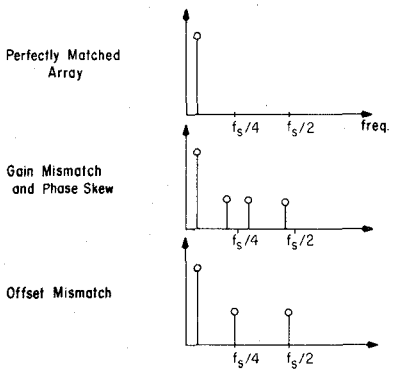



Fig. 5. Spectrum of a reconstructed sinusoid for a four-way converter array and bandlimited to $f_s/2$).

Unlike the gain variations discussed above, a mismatch of converter offsets will produce a constant noise, which is independent of the input frequency spectrum. More specifically [8]

$$N_{\dot{x}}(\omega) = |H(\omega) f_s|^2 \sum_{k=-\infty}^{\infty} |B_k|^2 \, \delta(\omega - k f_s/m) \tag{11}$$

where $B_k$ is the discrete Fourier transform of best fit offsets in the array. This noise spectrum is illustrated in Fig. 5(c) for a four-way array, along with the original signal spectrum. As is evident from the figure, the offset related noise appears at multiples of $f_s/m$, just as gain errors do for nonzero dc input levels.

The noise due to phase skew in a converter array is similar in spectral content to that of gain error. The noise resulting from an input sinewave of amplitude $A$ and frequency $\xi$ may be shown to be [8]

$$N_{\dot{x}}(\omega) \sim |AH(\omega) f_s|^2 \sum_{k=-\infty}^{\infty} |\Phi_k|^2 \, \Pi \, \frac{\omega - k f_s/m}{2\xi} \tag{12}$$

where $\Phi_k$ is the discrete Fourier transform of phase skew in the array, and $\Pi$ may be defined in terms of the impulse function $\delta$ by

$$\Pi(x) = \tfrac{1}{2}\delta(x + \tfrac{1}{2}) + \tfrac{1}{2}\delta(x - \tfrac{1}{2}). \tag{13}$$

The noise term corresponding to $k = 0$ in the above is a delayed signal component at the fundamental frequency, which is zero if the average phase skew is defined to be zero. Note that the phase skew ($\phi$) of a converter at a given frequency may be expressed in terms of its sampling time skew ($\delta t$) by simply $\phi = \omega \delta t$.

The previous spectral analysis has not specifically included the effects of quantization and nonlinearity. In converters with asynchronous sources, these effects usually appear as broad-band noise and simple or aliased harmonic distortion. This is also the situation with converter arrays if the converter nonlinearities are similar. If the nonlinearities are different, however, a given input level may be encoded differently by different converters, resulting in a "dithered" output signal. This is ultimately equivalent to a gain and offset mismatch, as the different nonlinearities will result in different best fit converter parameters. In real converter arrays, which do not otherwise exhibit a gain or offset mismatch, this may result in an overall $S/N$ degradation of perhaps a few decibels in the reconstruction of a full scale input signal (see experimental results). This noise may be objectionable in some systems, particularly during low-level or idle input conditions. In video systems it is often desirable, however, as it reduces the appearance of sharp quantization boundaries in picture areas where the luminance changes slowly [9]. If necessary, the dithering at a given voltage may be eliminated by altering the effective converter offsets (by either analog or digital means) so as to place a given voltage within a common quantization level.

Of final note in the overall error analysis is the effect of the previously considered noise and distortion sources on the $S/N$ ratio of a band-limited input signal. As significant portions of the noise and distortion products are clustered at, or near the Nyquist rate, the actual in-band $S/N$ ratio of an array, may be larger than what the power figures of Table II may indicate. More specifically, for a system whose signal bandwidth is limited to $f_s/k$ ($k \geq 2$), up to $k/2$ badly matched converters can be used in an array with no degradation of in-band $S/N$ ratio.

## IV. Implementation

To demonstrate the characteristics of this array technique, a four-channel CMOS test-chip has been fabricated in a 10 $\mu$m metal-gate CMOS process. This chip consists of four time-interleaved 7-bit weighted-capacitor A/D converters, associated timing and control logic and an implanted MOS voltage reference. Also included on this chip, is a four-way input multiplexor, which allows some, or all, of the individual A/D converters to be connected with a specific input line. This enables each of the converters to be operated as part of an array (common inputs), or independently. A block diagram of this test-chip is shown in Fig. 6. In this figure, the converters are seen to exist as a matrix of bit cells, where each row corresponds to a separate A/D converter, and where each column represents the bit-cells which are active in a given time-state. For example, during the first time-state, the first A/D converter is sampling, the second A/D converter is determining bit 6 of its conversion sequence, and so on. A total of eight time-states are required for a complete 7-bit conversion, which, because there are four converters per chip, results in an effective throughput of one conversion every two clock cycles. Note that this throughput may be doubled by interleaving two chips for a total of an eight-way converter array.

This entire chip is defined in terms of general purpose cells, which were placed and interconnected via an automated layout program. Although this approach resulted in a considerable increase in die size, it greatly simplified the required layout effort and provided a library cell-base from which other converter configurations can be designed. In theory, other converters may be realized by simply modifying the cell interconnect list, and rerunning the layout program. A layout of the complete chip, in cellular form, is shown in Fig. 7(a). A metal-gate CMOS process was chosen for this circuit, for reasons of simplicity and ease of fabrication at Sandia Laboratories. A more advanced process would have been desirable from the standpoint of performance, but was unnecessary for the demonstration of the concept, and not immediately avail-

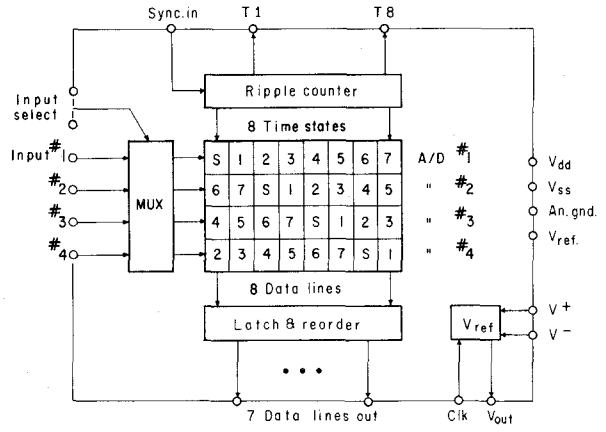
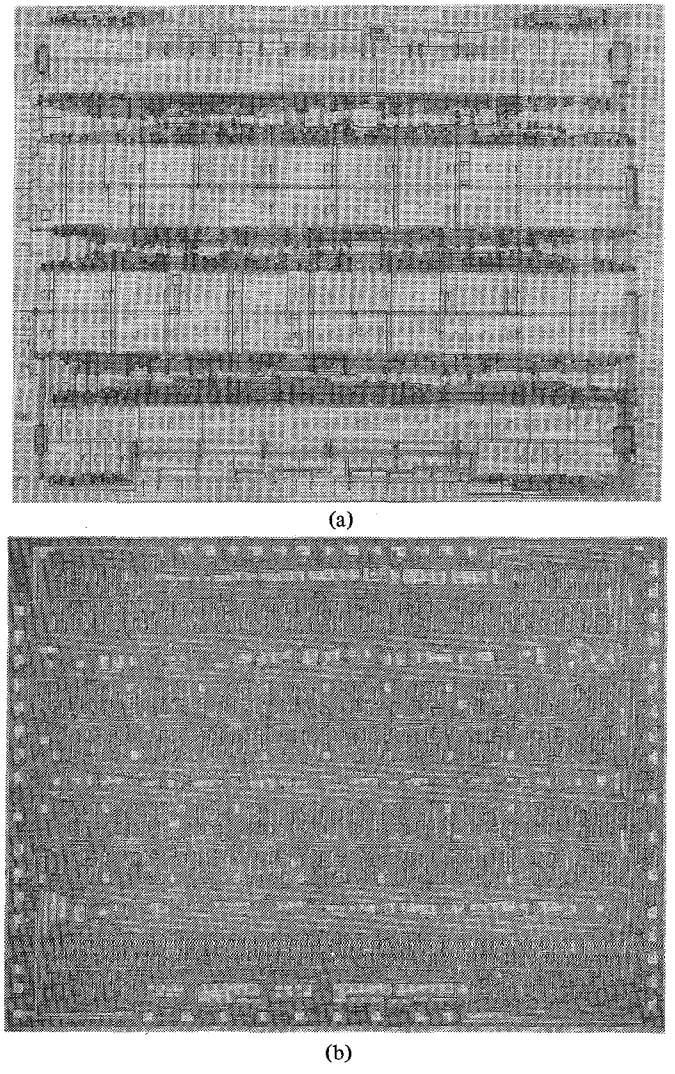



Fig. 6. Converter array chip block diagram.



(a)

(b)

Fig. 7. (a) Computer plot of array chip showing cellular layout technique. Each of the four cell rows along the middle of the chip is a separate 7-bit A/D converter. (b) Die photograph.

able. The fairly large die-size of this chip (208 X 278 mils) is principally a result of the cellular automated layout technique and the fully guard-banded CMOS process, which required that diffused $n^+$ or $p^+$ guard-bands (which were not self-aligned) be placed around each transistor. As only 1250

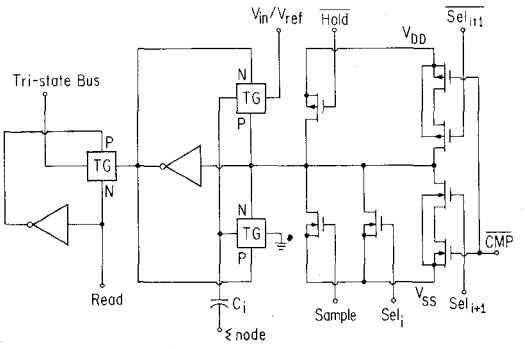



Fig. 8. Schematic of SAR bit cell. Die size in cell form is about 400 mil$^2$. TG indicates CMOS transmission gate.

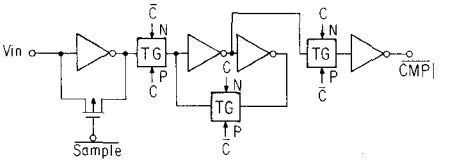


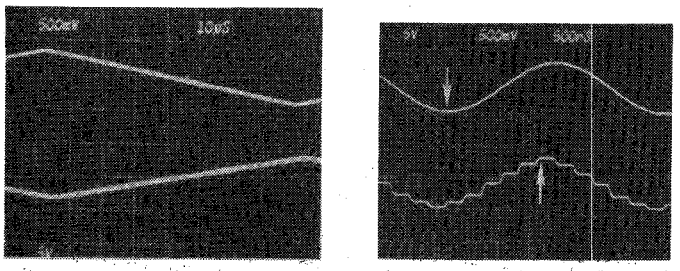

Fig. 9. Voltage comparator schematic.

mostly minimum sized devices are employed in this circuit, extensions of this design using more area efficient techniques would indeed have a small total area. A die photograph of the complete chip is shown in Fig. 7(b).

An example of one of the cells used in this chip, a dynamic bit slice of a successive approximation register is shown schematically in Fig. 8. This cell, or one quite similar to it, is used in each of the 28 bit cells present in the converter array. The state of this cell is established by the voltage present upon the floating node "$\bar{Q}$." This node is either pulled high or low at the appropriate bit time by the complementary devices shown on the right of the cell. In turn, this node allows the associated precision capacitor to be charged to the appropriate value by way of a pair of CMOS transmission gates. The state of the cell is read during the associated converters final bit time, by passing its value onto a tri-state data line which is common to all of the cells in a given time-state.

Another commonly used cell, the voltage comparator, is shown in Fig. 9. This circuit is single-ended and is used with its input node tied directly to the top plate of a capacitor array. During a given converter's "sample" interval, the associated comparator cell is offset cancelled, by shorting the input inverter's output and input together. During subsequent bit times, the input inverter is used as a linear amplifier, where the output reflects the value of the input voltage with respect to its offset point. The output of this inverter is then regenerated and buffered, by the flip-flop which follows it. Note that, although this comparator is small and fairly fast, a much more sophisticated comparator could be used, without substantially impacting the overall die size. Modifications of the design to improve resolution or power-supply rejection, for instance, would be much easier to incorporate in this array method than with a flash technique, as the number of required comparators is so much smaller.

The precision capacitors used in this chip are defined by thin-oxide cuts over $n^+$ diffusion regions and consist of about



(a) (b)

Fig. 10. Original (top) and reconstructed (bottom) waveforms after sampling with converter array chip (5 V/div. on vertical scale, bottom traces are inverted). (a) Single converter within an array at a 625 kHz conversion rate. (b) Four-way array at 3.5 MHz conversion rate (points shown correspond).

10 pF of total capacitance for each of the four converters. Although the converters in this chip employ binary-weighted capacitors, higher resolution converters could be realized with little or no increase in array capacitance, by using a "split array" [10] technique. The on-chip voltage reference circuit uses a closed-loop CMOS amplifier which has an implant-induced offset voltage [11] of approximately 0.8 V. To improve transient settling response, and to allow an increase in reference voltage, this circuit is used with an external 10 nF capacitor and trimpot.

## V. Experimental Results

Reconstructed ramp and sinewave input signals, which were digitized by this array chip, are shown in Fig. 10. Low frequency linearity is maintained to approximately a 2.5 MHz conversion rate, with operation at reduced linearity (5–6 bits) continuing to 4 MHz. The low-frequency linearity is dictated by binary-weighted capacitor matching, which in this case appears to have been limited by consistent pattern-generator and mask run-out errors. These effects are usually pronounced in high-speed circuits, which by necessity, must employ small capacitors. The capacitor errors are quite consistent from wafer to wafer, however, implying that a simple mask adjustment (or *e*-beam generated masks) should allow consistently good linearity in even higher resolution applications. High-frequency conversion linearity appears to be dominated by signal-related power line noise affecting the single-ended comparator operation. This effect could be substantially reduced by using differential comparators, which as mentioned previously, could be more easily employed in this technique than with the flash method, as only a few comparators are used.

A spectrograph of a reconstructed 100 kHz sinewave after sampling at a 2 MHz rate is shown in Fig. 11. Although the D/A used to reconstruct the converters output is not deglitched, power readings from this test indicate an A/D $S/N$ ratio of at least 39 dB. This contrasts to a 40.5–41 dB $S/N$ ratio when the converters within an array are measured individually. This difference is principally due to independent nonlinearities affecting the best fit converter gains and offsets, and a slight variance in feedthrough from the comparator reset switch. Channel isolation between converters is sufficiently high that no component of a full scale 100 kHz input signal to one converter is observable on the reconstructed quiet channel

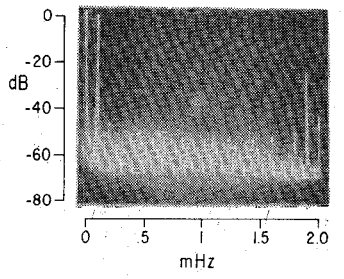



Fig. 11. Spectrum of reconstructed 100 kHz sinewave after sampling at 2 MHz with array chip.

TABLE III
Summary of Converter Array Chip Characteristics

| | |
|---|---|
| NUMBER OF MOS DEVICES | 1250 |
| TOTAL POWER CONSUMPTION | 250 mW |
| MAXIMUM SAMPLING RATE PER CHIP | 4 MHz |
| DIE SIZE | 208×278 MILS |
| RESOLUTION (2.5 MHz SAMPLE RATE) | 7 BITS |
| LINEARITY " | 1/2 LSB |
| S/N RATIO, FULL SCALE INPUT " | 39 db |
| PHASE SKEW AND JITTER | < 4 nsec |
| REFERENCE VOLTAGE DRIFT, 0-70° C | < 1 % |

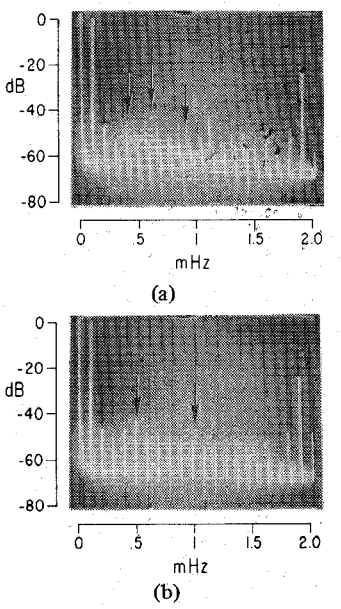



Fig. 12. Noise and distortion due to induced converter mismatch. Spikes shown are caused by mismatch indicated. (a) Gain variation ($\sigma_a/\bar{a}$) of approximately 1 percent. (b) Offset variation ($\sigma_b$) of approximately 0.5 percent of full scale range.

output of any other. A summary of the characteristics of this test converter-array chip is given in Table III.

Spectral plots of reconstructed sinewaves after artificially inducing gain and offset variance within an array, are shown in Fig. 12. Note that the noise spikes are at the frequencies indicated in Fig. 5, while the magnitude of the error (after compensating for nonlinearity effects) is approximately that indicated by Table II.

## VI. Extrapolation of Results

If this basic design, which used a 10 $\mu$m fully guard-banded CMOS process and program interconnected cells, were to be implemented in a modern 4-5 $\mu$m silicon-gate process using more area efficient techniques, a substantial improvement in die-size and performance would result. The die size would be reduced by a factor of four by simply scaling the major lithographic dimensions to half of their present size (shrinking 10 $\mu$m gates to 5 $\mu$m for instance). Further reductions in die size would occur if the field isolation regions were implanted or self-aligned, rather than consisting of diffused guard bands, and the computer generated cell-based layout was replaced with one drawn by hand. In fact, an overall reduction in die size by a factor of 6 appears to be conservative if the above improvements were incorporated into a new design.

As the maximum conversion rate is directly related to the capacitance which must be driven by internal nodes, the reductions in die size considered above, would all result in higher speed. Further improvements in conversion rate could be obtained by using optimized device sizes in all of the internal logic, rather than a standard cell approach, and by incorporating a lower resistivity interconnect than the P+ diffusions which were available here. These various improvements would allow an improvement in conversion rate by at least a factor of four. This would imply that an 8-bit video bandwidth (10-15 MHz) converter could be fabricated in a die size of less than 10 000 mil$^2$.

## VII. Conclusion

This array method has been shown to offer a number of advantages over more conventional A/D techniques in high-speed applications, and to be realizable in a monolithic form. Although this method will, in some cases, result in increased noise or distortion, these effects are both predictable and consistent, and may be minimized in the design of an array. This technique should be useful in reducing the cost of both high-speed monolithic converter circuits and single- or few-chip digital signal processors which must operate on high-frequency analog input signals.

## Appendix

### Error Power Due to Gain and Offset Mismatch

The quantized output value of the $i$th converter within a converter array, may be represented by

$$\hat{x}_i(x) = a_i x + b_i + \delta_i(x) \tag{A1}$$

where $a_i$ and $b_i$ are the best fit gain and offset and $\delta_i(x)$ is the quantizing and nonlinearity error. The error minimizing parameters $a_i$ and $b_i$ are given by

$$a_i = \frac{\langle \hat{x}_i x\rangle - \langle \hat{x}_i\rangle\langle x\rangle}{\langle x^2\rangle - \langle x\rangle^2} \tag{A2}$$

and

$$b_i = \langle \hat{x}_i\rangle - a_i\langle x\rangle \tag{A3}$$

in which

$$\langle f(x)\rangle \triangleq \int_{-\infty}^{\infty} f(x)\,P(x)\,dx \tag{A4}$$

for an input probability function $P(x)$.

As previously shown, the error power which results when this converter is used alone, is

$$E_p = \langle \delta_i^2\rangle. \tag{A5}$$

If a number of such converters are used as an array, the error power becomes

$$E_p = \frac{1}{m}\sum_{i=1}^{m} \langle (\hat{x}_i - (a_{\min}x + b_{\min}))^2\rangle \tag{A6}$$

where $a_{\min}$ and $b_{\min}$ are best fit parameters for the array as a whole, and $m$ is the number of converters in the array. Substituting (A1) into the above results in

$$E_p = \frac{1}{m}\sum_{i=1}^{m} \langle ((a_i - a_{\min})x + b_i - b_{\min} + \delta_i(x))^2\rangle \tag{A7}$$

or

$$E_p = \frac{1}{m}\sum_{i=1}^{m} \langle (\Delta_i(x) + \delta_i(x))^2\rangle \tag{A8}$$

as referred to in the text. The above may be expanded to give

$$\begin{aligned} E_p = \frac{1}{m}\sum_{i=1}^{m} [&(a_i - a_{\min})^2\langle x^2\rangle + (b_i - b_{\min})^2 \\ &+ \langle \delta_i^2\rangle + 2(a_i - a_{\min})(b_i - b_{\min})\langle x\rangle \\ &+ 2(a_i - a_{\min})\langle \delta_i x\rangle + 2(b_i - b_{\min})\langle \delta_i\rangle]. \end{aligned} \tag{A9}$$

For input signals which are asynchronous with the sampling clock, the last two terms are near zero, even for badly matched arrays. This results in the approximation given by (8), or

$$E_p = \frac{1}{m}\sum_{i=1}^{m} [\langle \delta_i^2\rangle + \langle \Delta_i^2\rangle]. \tag{A10}$$

The minimizing values of $a_{\min}$ and $b_{\min}$ are obtained by differentiating (A9) with respect to both variables and solving for the zero of each derivative. This occurs at simply $a_{\min} = \bar{a}_i$ and $b_{\min} = \bar{b}_i$, resulting in an error power of

$$E_p = \sigma_a^2\langle x^2\rangle + \sigma_b^2 + \overline{\langle \delta_i^2\rangle} \tag{A11}$$

in signals for which $\langle x\rangle \simeq 0$, where

$$\sigma_x^2 = \overline{(x^2)} - (\bar{x})^2. \tag{A12}$$

### Error Power Due to Sampling Time Skew for a Sinusoidal Input Signal

The average error power for an $m$-way array of interleaved samplers may be given by

$$E_p = \frac{1}{m}\sum_{i=1}^{m} \langle (\hat{x}_i - x)^2\rangle \tag{A13}$$

where $\hat{x}_i$ is the sampled value of $x$. For a sinusoidal input waveform, and for distortionless samplers which exhibit a timing skew,

$$x = A \sin(\omega t) \tag{A14}$$

and

$$\hat{x}_i = A \sin(\omega(t + t_i - t_{\min})) \tag{A15}$$

where $\hat{x}_i$ is the value sampled near time $t$, $t_i$ is the absolute delay in the $i$th sampler, and $t_{\min}$ is a minimizing sampling delay of the array as a whole. For these values of $x$ and $\hat{x}_i$, the error power may be shown to be

$$E_p = \frac{A^2}{m} \sum_{i=1}^{m} (1 - \cos(\omega(t_i - t_{\min}))) \tag{A16}$$

in which $t_{\min}$ is defined to be the value which minimizes $E_p$. The value of $t_{\min}$ may be obtained by differentiating the above and equating to zero, giving an error minimizing delay of simply $t_{\min} = \bar{t}_i$. The expression for $E_p$ may now be expanded, resulting in

$$E_p = \frac{A^2}{m} \sum_{i=1}^{m} \left[ \frac{\omega^2 (t_i - \bar{t}_i)^2}{2!} - \frac{\omega^4 (t_i - \bar{t}_i)^4}{4!} + \cdots \right] \tag{A17}$$

which for small values of time skew may be approximated by

$$E_p \simeq \frac{A^2 \omega^2 \sigma_t^2}{2}. \tag{A18}$$

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**W. C. Black, Jr.** (S'76–M'80), for a photograph and biography, see this issue, p. 938.

**David A. Hodges** (S'59–M'65–SM'72–F'77) received the B.E.E. degree from Cornell University, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley.

From 1966 to 1970 he was at Bell Laboratories, first in the components area at Murray Hill, then as Head of the System Elements Research Department at Holmdel, NJ. Now he is Professor of Electrical Engineering and Computer Sciences at the University of California, Berkeley, where he has been a member of the faculty since 1970. He has served as a consultant in the integrated circuits and communications equipment industries. His research interests are in the area of integrated circuits and large-scale integration.

Dr. Hodges is a former Editor of the IEEE Journal of Solid-State Circuits (1971–1974), and has served as Program Chairman (1977) and Conference Chairman (1978) for the International Solid-State Circuits Conference.