

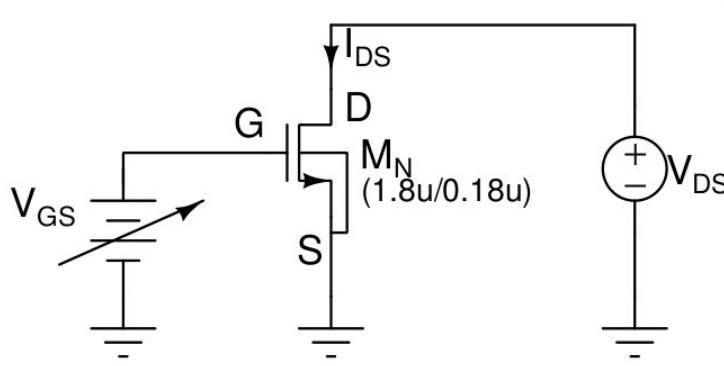
VLSI ASSIGNMENT - 1 REPORT

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2019102014

Question 2:

Circuit Diagram:

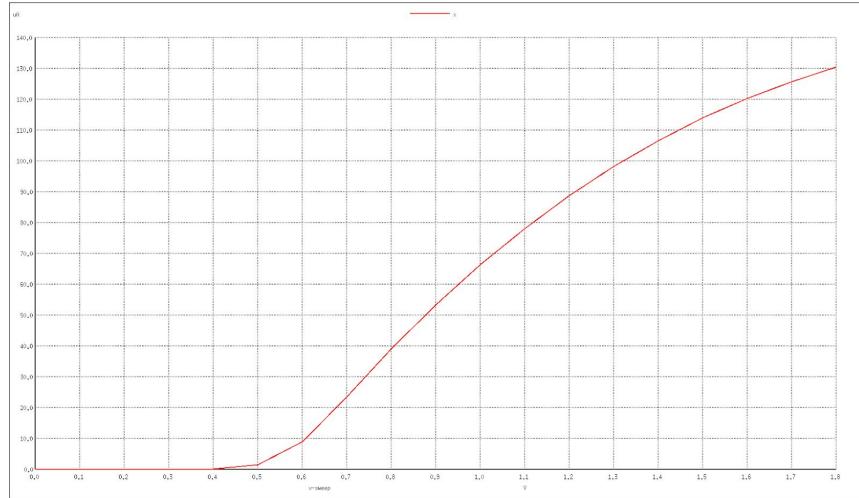


A)Code:

```
VLSI Assignment-1 > Question2 > Q2a.cir
 1  VLSI Assignment Question 2a
 2  * Answers to question 2a
 3  .include TSMC_180nm.txt
 4  .param SUPPLY=1.8
 5  .param LAMBDA=0.09u
 6  .param width_N={20*LAMBDA}
 7  .global gnd vdd
 8
 9  VGS G gnd 0
10  VDS D gnd 50m
11
12  *MOSFET Initialisation
13  M1 D G gnd gnd CMOSN W={width_N} L={2*LAMBDA}
14  + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
15  + AD={5*width_N*LAMBDA}
16
17  *DC Sweep
18  .dc VGS 0 1.8 0.1
19
20  * Plots
21  .control
22  set hcopyright = 1 *White background for saving plots
23  set color0=white ** color0 is used to set the background of the plot (manual sec:17.7))
24  set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7))
25
26  run
27  let x = (-VDS#branch)
28  set curplottitle="Id vs Vgs Characteristics"
29  plot x
30
31  hardcopy fig_Q2a.eps (-VDS#branch)
32  .endc
33
```

Plots:

Id vs Vgs Characteristics:



First and Second Derivatives:

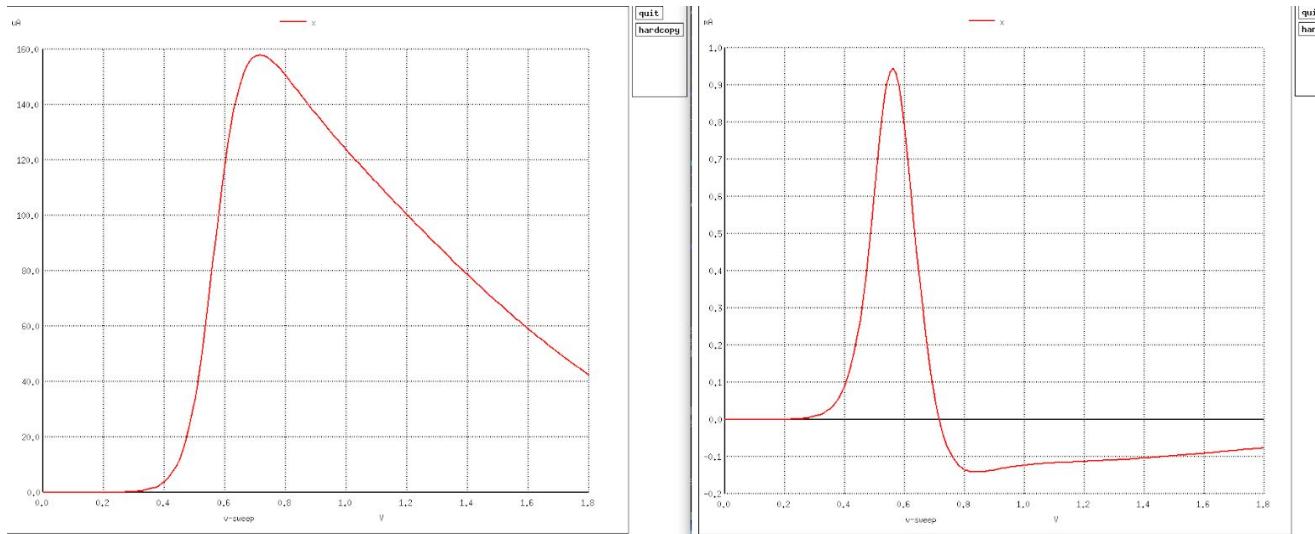


Fig.Plot 1: First derivative of I_d vs V_{gs} Plot 2: Second Derivative of I_d vs V_{gs}

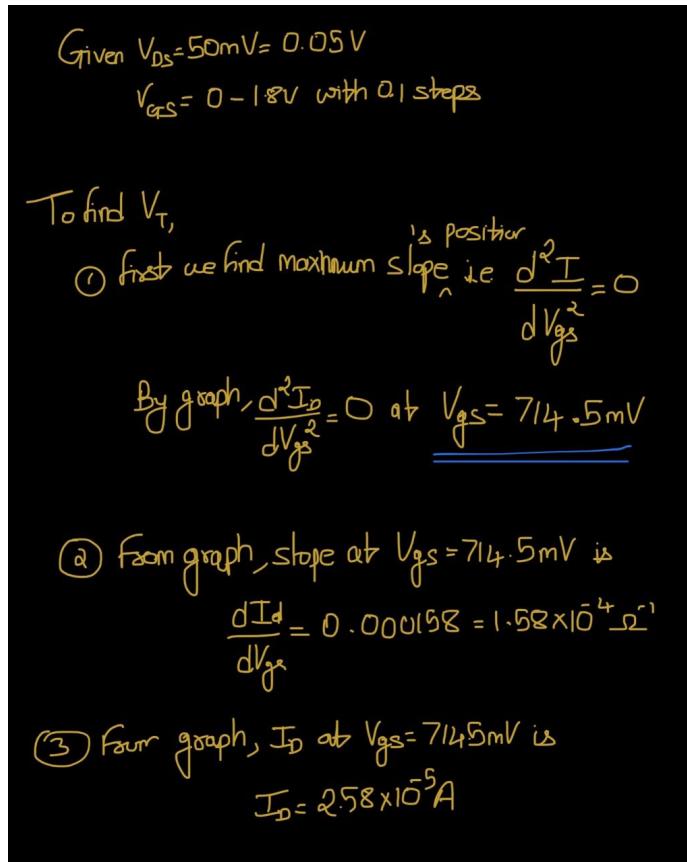
State of MOSFET:

We see that the MOSFET is in linear region, but it will not follow exact linear state as V_{ds} is very small and

$$V_{ds} < V_{gs} - V_{th}$$

We see that the deviations and aberrations of second order effect will affect.

Threshold Calculation:



④

$$y - y_0 = m(x - x_0)$$

$$y - 2.58 \times 10^{-5} = 1.58 \times 10^{-4}(x - 0.7145)$$

To find V_T , $y = 0$

$$\frac{-2.58 \times 10^{-5}}{1.58 \times 10^{-4}} = x - 0.7145$$

$$-1.63 \times 10^{-1} = x - 0.7145$$

$$0.7145 - 0.163 = x$$

$$x = 0.5515 \text{ V}$$

$\boxed{A \text{ n.s } V_T = 0.5515 \text{ V}}$

B)

VDS = 1.8 V and V GS is swept from 0 to 1.8 V in a step of 0.1 V

Theory:

- In this case for most parts of the simulation, the NMOS is in saturation region as $V_{ds} \geq V_{gs} - V_{th}$ and unlike the part a, this condition is definitely of larger value .
- The current in saturation region is a 2nd order term with respect to V_{gs} and V_t , therefore we cannot directly compute the V_{th} due to proportionality.
- But to account for this we take the square root of I_d then do the same method as done in Part A.

In saturation region,

$$I_{D,sat} = \frac{UC_x}{2} \left[\frac{W}{L} \right] [V_{gs} - V_{th}]^2$$

So, $I_{D,sat} \propto [V_{gs} - V_{th}]^2$

To get a linear relationship,

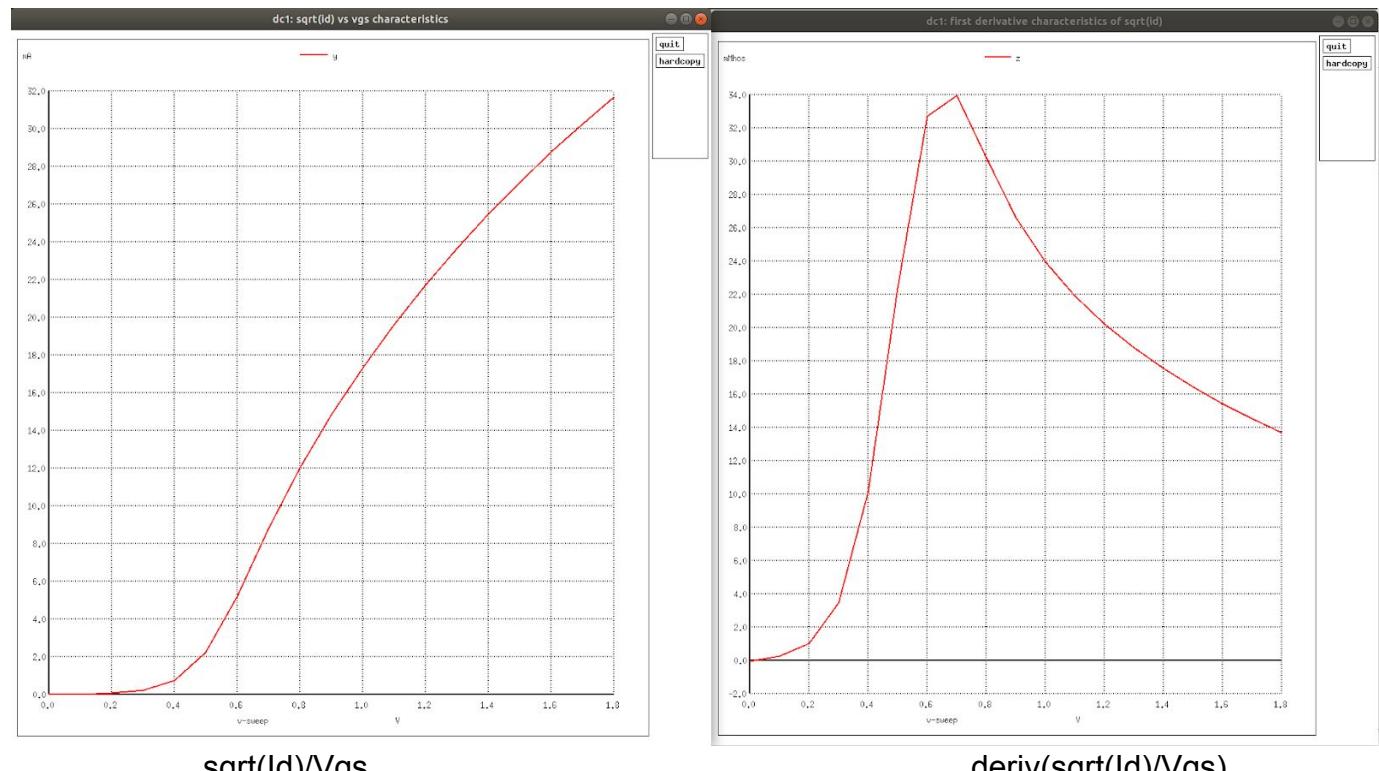
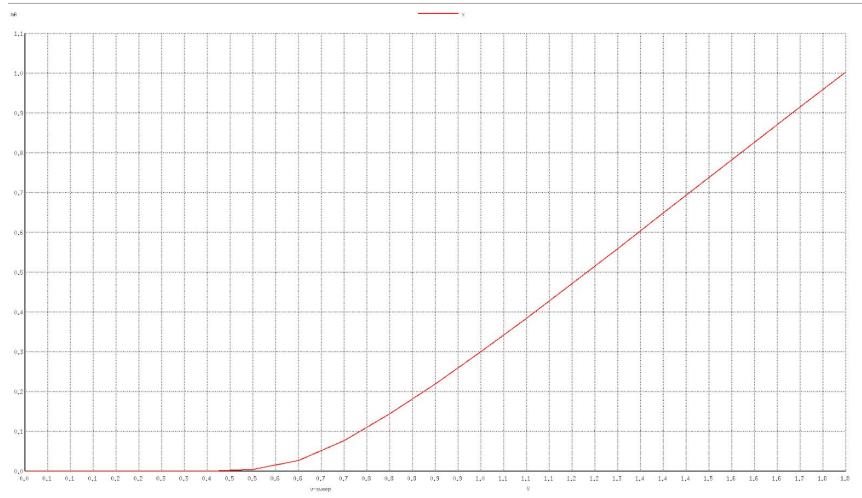
$$\sqrt{I_{D,sat}} \propto [V_{gs} - V_{th}]$$

Code:

```
VLSI Assignment-1 > Question2 > Q2b.cir
 1  VLSI Assignment Question 2b
 2  * Answers to question 2b
 3  .include TSMC_180nm.txt
 4  .param SUPPLY=1.8
 5  .param LAMBDA=0.09u
 6  .param width_N={20*LAMBDA}
 7  .global gnd vdd
 8
 9  VGS G gnd 0
10  VDS D gnd 1.8
11
12 M1 D G gnd gnd CMOSN W={width_N} L={2*LAMBDA}
13 + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
14 + AD={5*width_N*LAMBDA}
15
16 .dc VGS 0 1.8 0.1
17
18 .control
19 set hcopypscolor = 1 *White background for saving plots
20 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
21 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
22
23
24 run
25 let x = sqrt(-VDS#branch)
26 set curplottitle="Id vs Vgs Characteristics"
27 plot x
28
29 let y = deriv(sqrt(-VDS#branch))/deriv(V(G))
30 set curplottitle="First Derivative Characteristics"
31 plot y
32
33
34 hardcopy fig_Q2b.eps sqrt(-VDS#branch) deriv(sqrt(-VDS#branch))/deriv(V(G))
35 .endc
```

Plots:

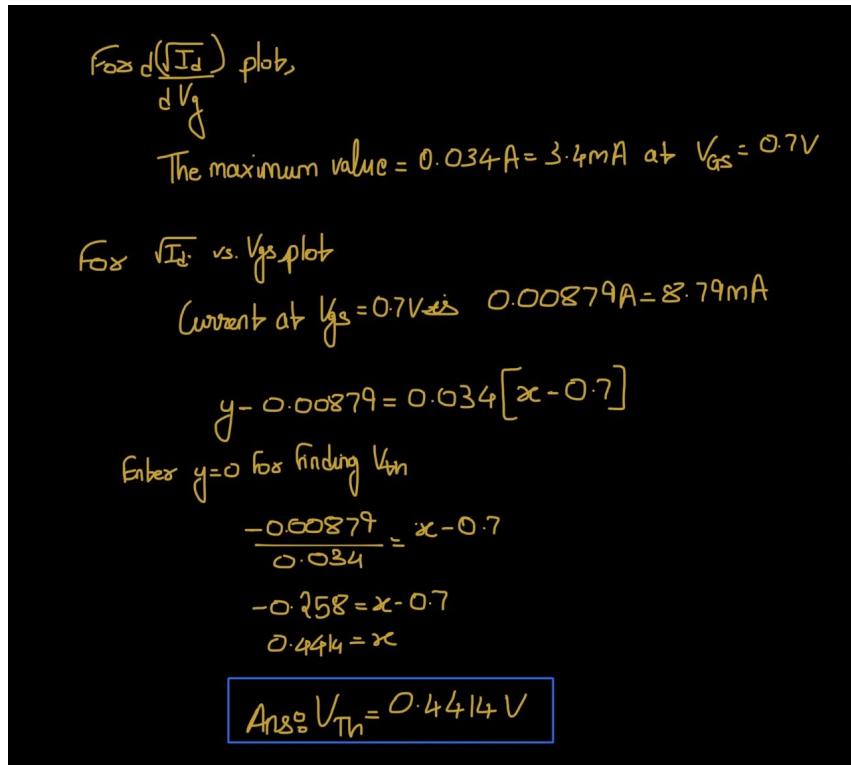
Id vs Vgs:



$\text{sqrt}(Id)/Vgs$

$\text{deriv}(\text{sqrt}(Id))/Vgs$

Calculation:



C) Observation:

We see that the threshold voltage for $V_{ds} = 50 \text{ mV}$ is more than that of $V_{ds} = 1.8 \text{ V}$ as in the first case the MOSFET is in linear region and in the second case, due to operation in saturation region.

The MOSFET experiences **Drain Induced Barrier Lowering(DIBL)** which is the inversion at lower V_{gs} where the threshold voltage decreases due to the drain voltage.

$$V_t = V_{t0} - \eta V_{ds} \quad \text{where } \eta = \text{DIBL Coefficient}$$

Question 3:

A) NMOS:

Theory:

In this question, main objective is to compute μC_{ox} and V_t for various bodies to source voltage.

So for convenience, we take $V_{ds} = 1.8V$ (same as previous question) so that the MOSFET stays in saturation region always

To calculate threshold voltage,

Find maximum slope of $\frac{d(\sqrt{I_d})}{dV_g}$ either by estimation or taking $\frac{d^2(\sqrt{I_d})}{dV_g^2} = 0$

$$I_D = \frac{1}{2} \mu C_{ox} \left[\frac{W}{L} \right] [V_{GS} - V_{th}]^2$$

$$\sqrt{I_D} = \underbrace{\left[\frac{1}{2} \mu C_{ox} \left[\frac{W}{L} \right] \right]}_{\text{Slope or linear equation}} [V_{GS} - V_{th}]$$

For max slope of $\frac{d(\sqrt{I_d})}{dV_g} = m_o$,

If we draw a tangent across any point from the point of max slope,

$$y - y_0 = m_o (x - x_0)$$

(Units: \sqrt{A}) (Units: Volt)

To find V_t , taken x-intercept,

$$-y_0 = m_o (x - x_0)$$

$$x = x_0 - \frac{y_0}{m_o}$$

$x = x_0 - \frac{y_0}{m_o}$

$\rightarrow x = V_{th}$
 $\rightarrow x_0 = x - \text{coord. of max slope}$
 $y_0 = y - \text{coord. of max slope}$
 $m_o = \text{Max slope}$

To calculate μ_{Cox} ,

$$\text{To find } \mu_{Cox},$$

$$m_o^2 = \frac{1}{2} \mu_n C_{ox} \left[\frac{W}{L} \right]$$

$$\frac{W}{L} = \frac{10}{1} \text{ as } W=1.8\mu, L=0.18\mu$$

$$m_o^2 = \frac{1}{2} [\mu_n C_{ox}]^2 \left[\frac{W}{L} \right]^5$$

$$\mu_n C_{ox} = \frac{m_o^2}{5}$$

Code:

```
VLSI Assignment-1 > Question3 > Q3i_NMOS.cir
1 VLSI Assignment Question 3i
2 * Answers to question 3i
3 .include TSMC_180nm.txt
4 .param SUPPLY=1.8
5 .param LAMBDA=0.09u
6 .param width_N={20*LAMBDA}
7 .global gnd vdd
8
9 VGS G gnd 0V
10 VDS D gnd 1.8V
11 VBS B gnd 0V
12
13 M1 D G gnd B CMOSN W={width_N} L={2*LAMBDA}
14 + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
15 + AD={5*width_N*LAMBDA}
16
17 .dc VGS 0 1.8 0.01
18
19 .control
20 set hcopypscolor = 1 *White background for saving plots
21 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
22 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
23
24 run
25 let x = (-VDS#branch)
26 let y = sqrt(-VDS#branch)
27 let z = deriv(sqrt(-VDS#branch))/deriv(V(G))
28
29 set curplottitle="Id vs Vgs Characteristics"
30 plot x
31
32 set curplottitle="sqrt(Id) vs Vgs Characteristics"
33 plot y
34
35 set curplottitle="First derivative Characteristics"
36 plot z
37
38 hardcopy fig_Q3iNMOS.eps (-VDS#branch) sqrt(-VDS#branch) deriv(sqrt(-VDS#branch))/deriv(V(G))
39 .endc
```

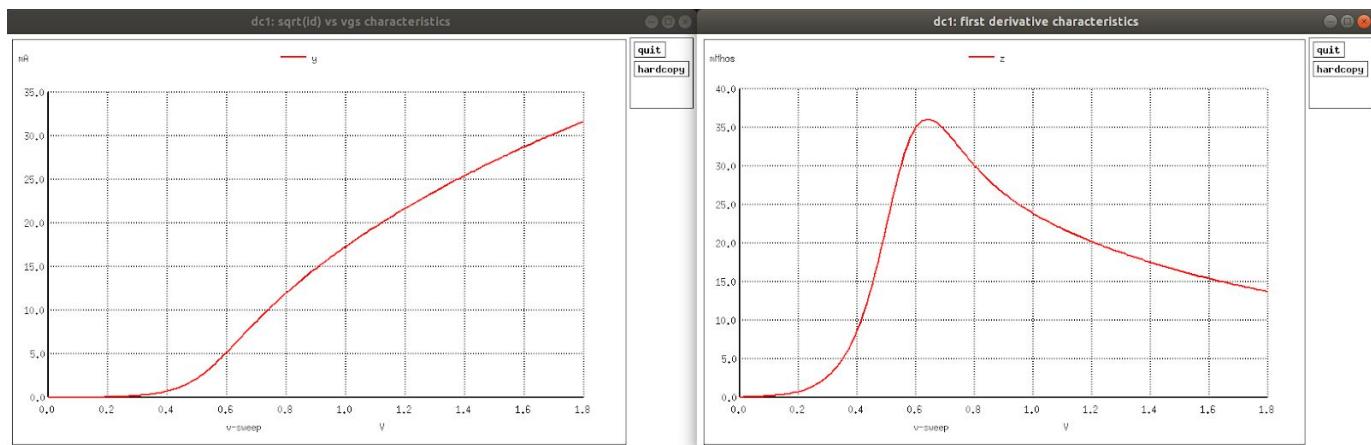
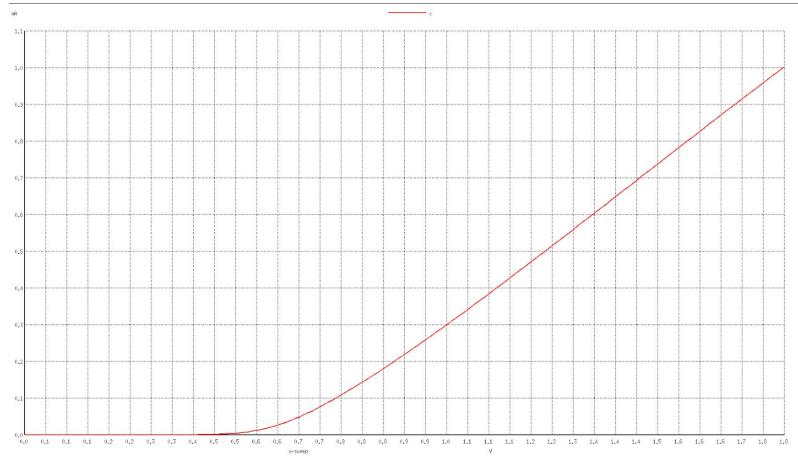
NOTE: This code is a template used for case 1. For other cases, "VBS B gnd 0V is modified.

Plots:

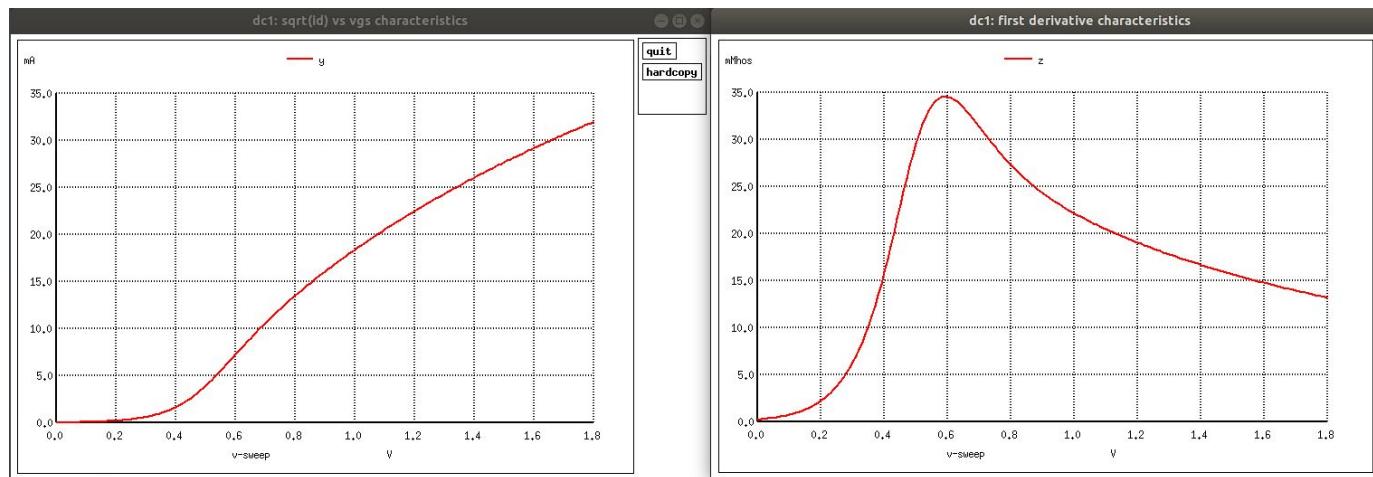
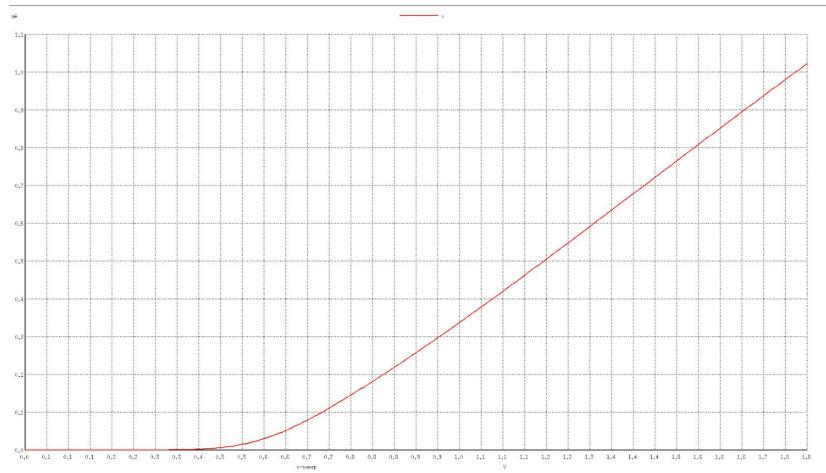
All the three cases have 3 plots each:

- 1) I_d vs V_{gs}
- 2) $\sqrt{I_d}$ vs V_{gs}
- 3) First derivative of 2nd plot

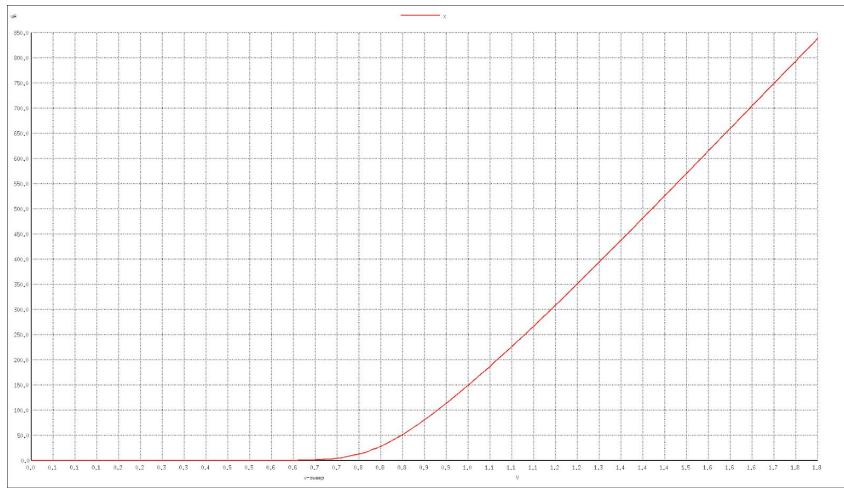
(I) $V_{bs} = 0V$

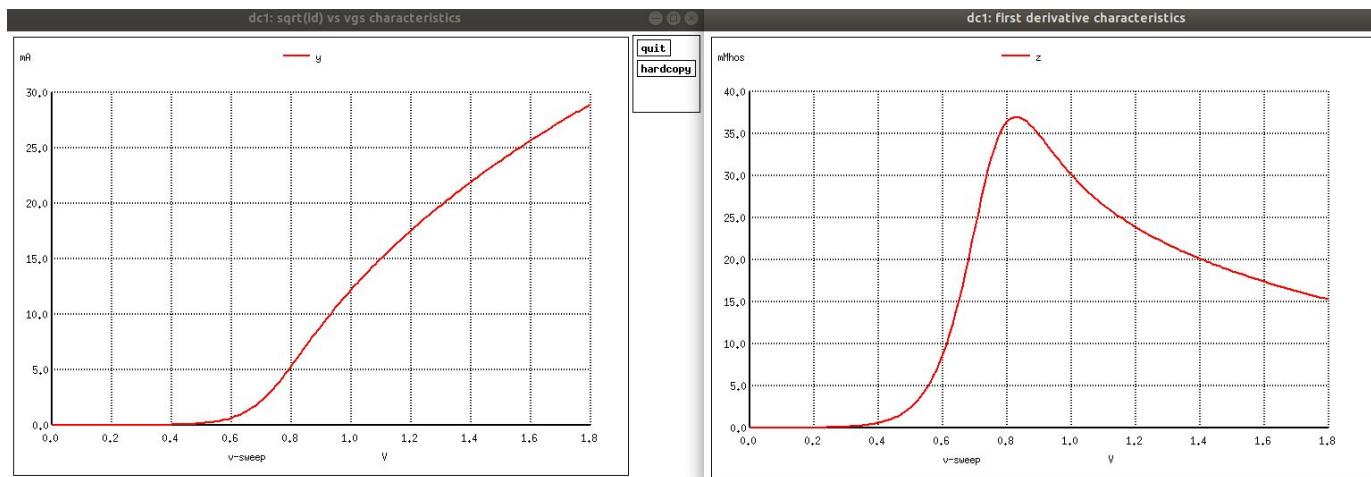


(II) $V_{bs} = 900\text{mV}$



(III) $V_{bs} = -900\text{mV}$





CALCULATIONS:

The steps mentioned in the theory is executed and the following table is obtained:

Body-Source Voltage(mV)	Threshold Voltage (V)	$\mu \text{Cox} (\mu \text{A}/V^2)$
0	0.473	246.7
900	0.395	236.3
-900	0.66	271.4

OBSERVATIONS:

- We see that the threshold value decreases with increase in body-source voltage due to it's **body-effect** while it increases for a negative body-source voltage.
- The μCox also follows a similar trend as the threshold voltage

B) PMOS:

Theory:

The PMOS is kept in saturation region during its calculation for convenience i.e $V_{SG} > V_t$ to calculate the μC_{ox} and V_t . Similar to the previous case, Source-Drain voltage is taken as 1.8V then plot the drain current with respect to the gate-source voltage.

Method to calculate both the parameters:

① Find maximum slope of $\frac{d(\sqrt{I_D})}{dV_g}$ either by estimation or taking $\frac{d^2(\sqrt{I_D})}{dV_g^2} = 0$

Here, $V_{SG} = V_S - V_G$
 \uparrow
 1.8

$I_D = \frac{1}{2} \mu C_{ox} \left[\frac{W}{L} \right] [V_{SG} - V_{th}]^2$ So the slopes are calculated accordingly

$\sqrt{I_D} = \underbrace{\sqrt{\frac{1}{2} \mu C_{ox} \left[\frac{W}{L} \right]}}_{\text{Slope of linear equation}} [V_{SG} - V_{th}]$

To find max slope of $\frac{d\sqrt{I_D}}{dV_g} = m_o$,

If we draw a tangent across any point from the point of max slope,

$y - y_0 = m_o (x - x_0)$

(Units: \sqrt{A}) (Units: Volt)

To find V_t , taken x -intercept,

$-y_0 = m_o (x - x_0)$

$x = x_0 - \frac{y_0}{m_o}$

$\rightarrow x = |V_{th}|$

$\rightarrow x_0 = x$ -coord. of max slope

$y_0 = y$ -coord. of max slope

$m_o = \text{Max slope}$

To find $\mu_n C_{ox}$,

$$m_o^2 = \frac{1}{2} \mu_p C_{ox} \left[\frac{W}{L} \right]$$

$$\frac{W}{L} = \frac{10}{1} \text{ as } W=1.8\mu, L=0.18\mu$$

$$m_o^2 = \frac{1}{2} [\mu_n C_{ox}] \left[\frac{W}{L} \right]^5$$

$$\mu_n C_{ox} = \frac{m_o^2}{5}$$

CODE:

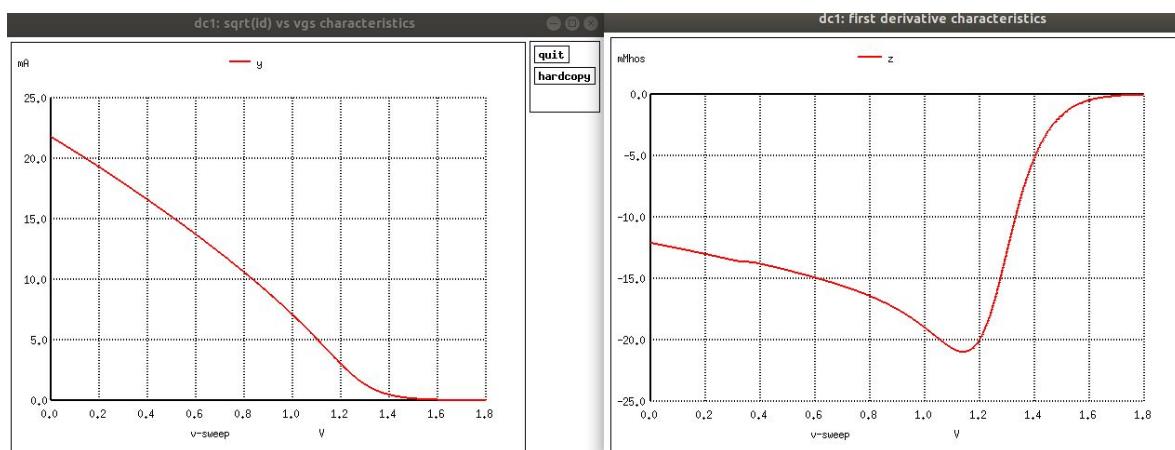
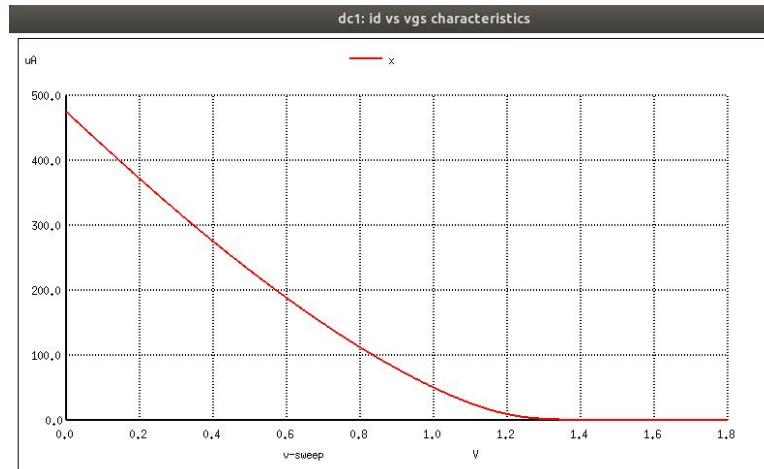
```
VLSI Assignment-1 > Question3 > Q3iii_PMOS.cir
1 VLSI Assignment Question 3iii
2 * Answers to question 3iii
3 .include TSMC_180nm.txt
4 .param SUPPLY=1.8
5 .param LAMBDA=0.09u
6 .param width_P={20*LAMBDA}
7 .global gnd vdd
8
9 VGS G gnd 0
10 VDS D gnd 1.8V
11 VBS B D -900mV
12
13 M1 D G gnd B CMOS P W={width_P} L={2*LAMBDA}
14 + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
15 + AD={5*width_P*LAMBDA}
16
17 .dc VGS 0 1.8 0.001
18
19
20 .control
21 set hcopypscolor = 1 *White background for saving plots
22 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7))
23 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7))
24
25 run
26 let x = (-VDS#branch)
27 set curplottitle="Id vs Vgs Characteristics"
28 plot x
29
30 let y = sqrt(-VDS#branch)
31 set curplottitle="sqrt(Id) vs Vgs Characteristics"
32 plot y
33
34 let z = deriv(sqrt(-VDS#branch))/deriv(V(G))
35 set curplottitle="First derivative Characteristics"
36 plot z
37
38 hardcopy fig_Q3iiiPMOS.eps (-VDS#branch) sqrt(-VDS#branch) deriv(sqrt(-VDS#branch))/deriv(V(G))
39 .endc
```

PLOTS:

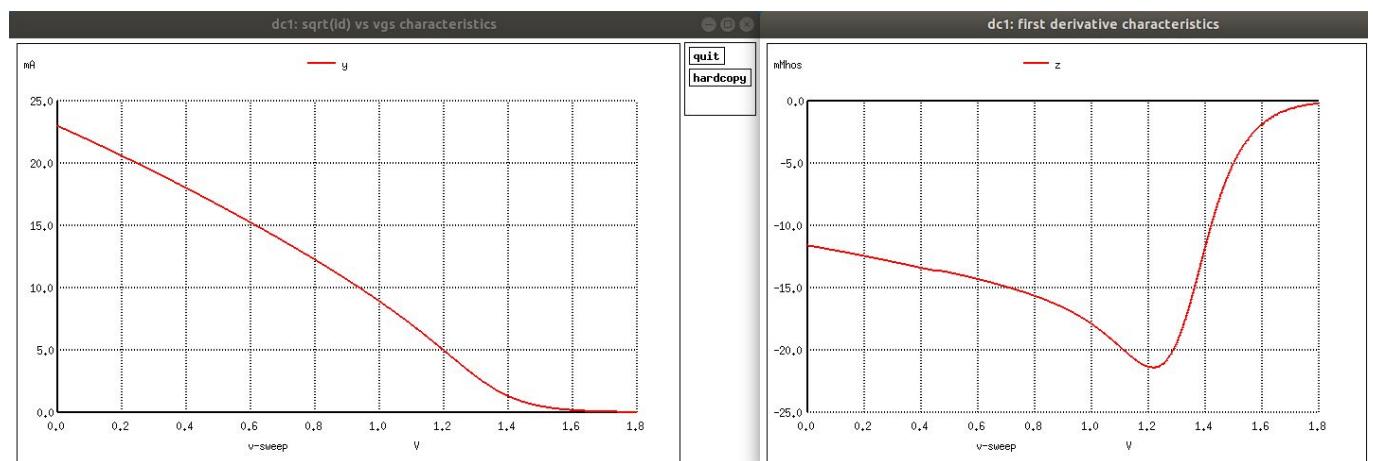
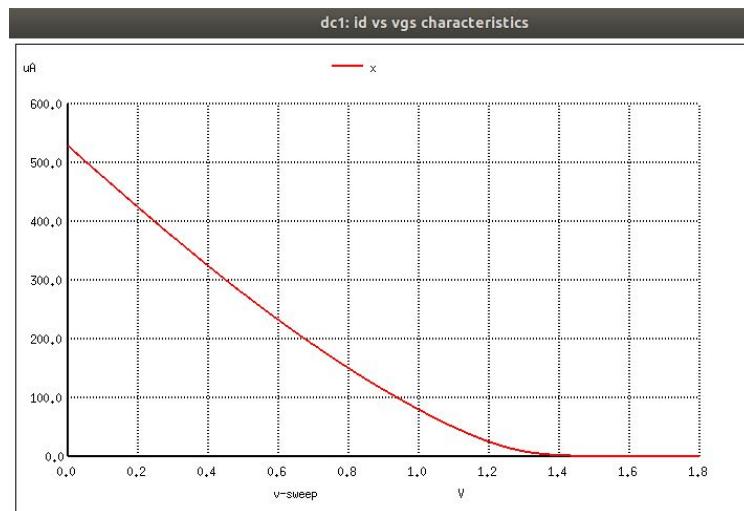
All the three cases have 3 plots each:

- 4) I_d vs V_{gs}
- 5) $\sqrt{I_d}$ vs V_{gs}
- 6) First derivative of 2nd plot

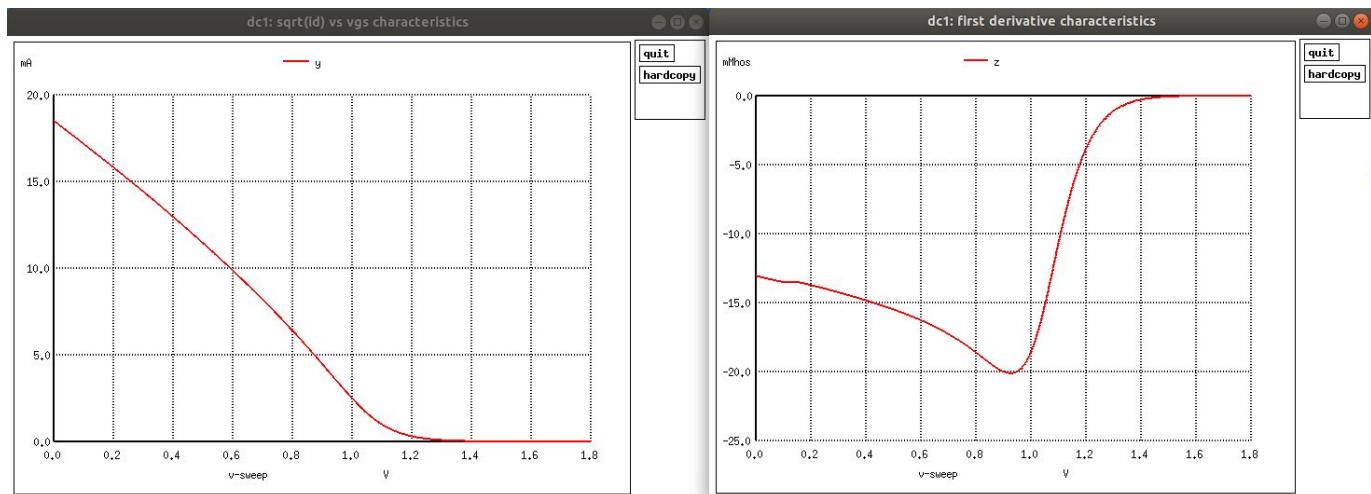
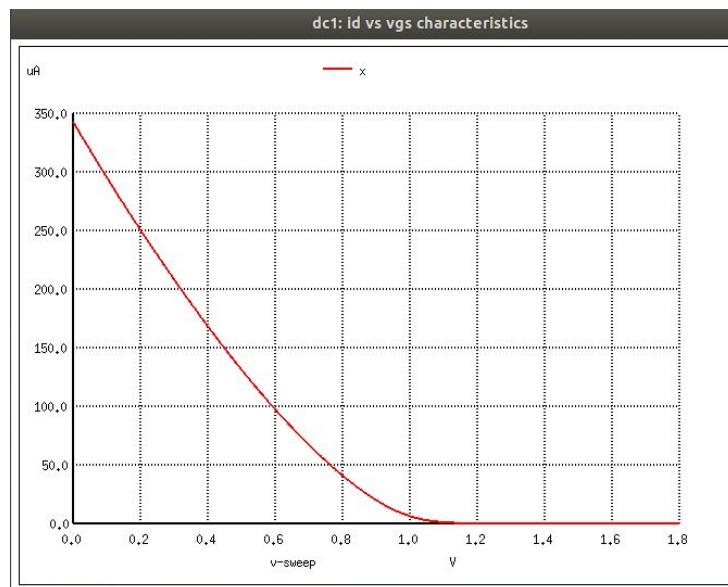
(I) $V_{bs} = 0V$



(II) $V_{bs} = -900\text{mV}$



(III) $V_{bs} = +900\text{mV}$



CALCULATIONS:

The steps mentioned in the theory is executed and the following table is obtained:

Body-Source Voltage(mV)	Threshold Voltage (V)(Absolute Value)	$\mu \text{Cox} (\mu \text{A}/\text{V}^2)$
0	0.48	93.2
900	0.72	85.57
-900	0.38	92.6

OBSERVATIONS:

- We see that the threshold value increases with increase in body-source voltage due to it's **body-effect** while it increases for a negative body-source voltage.
- The μCox also changes with the change in body-source voltage.

γ : Body effect coefficient

- Positive for NMOS
- Negative for PMOS

Φ_F : Fermi potential

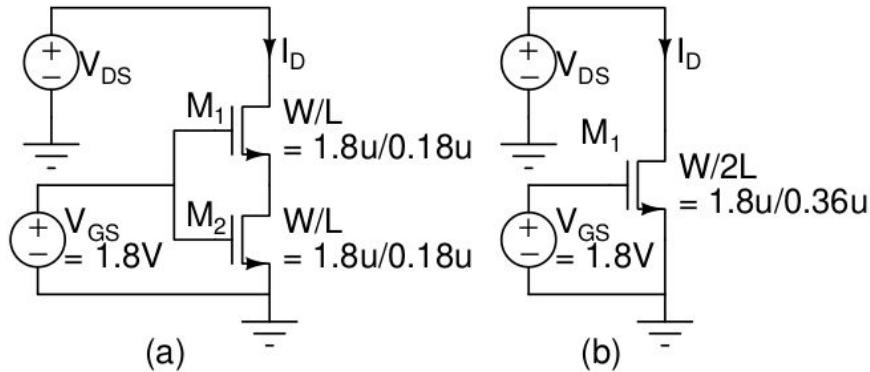
- Negative for NMOS
- Positive for PMOS

V_{T0} : Zero body bias ($V_{SB} = 0$) threshold voltage

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|})$$

Question 4:

Circuit Diagrams:



Codes:

```
VLSI Assignment1 > Question4 > Q4a.cir
1 Series combination of two transistors
2 .include TSMC_180nm.txt
3 .param SUPPLY=1.8
4 .param LAMBDA=0.09u
5 .param width_N=20*LAMBDA
6 .global gnd vdd
7
8 VDS D1 gnd 0
9 VGS G gnd 1.8V
10 * MOSFET DECLARATION
11 M1 D1 G D2 gnd CMOSN W={width_N} L={2*LAMBDA}
12 + AS={(5*width_N*LAMBDA)} PS={(10*LAMBDA+2*width_N)}
13 + AD={(5*width_N*LAMBDA)}
14
15 M2 D2 G gnd gnd CMOSN W={width_N} L={2*LAMBDA}
16 + AS={(5*width_N*LAMBDA)} PS={(10*LAMBDA+2*width_N)}
17 + AD={(5*width_N*LAMBDA)}
18
19 * Performing DC Sweep
20 .dc VDS 0 3 0.1
21
22 * Control for plots
23 .control
24 set hcopypscolor = 1 *White background for saving plots
25 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
26 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
27
28 run
29 let x = (-VDS#branch)
30 set curplottitle="Q4a Id vs Vds Characteristics"
31 plot x
32
33 hardcopy fig_Q4a.eps (-VDS#branch)
34 .endc

VLSI Assignment1 > Question4 > Q4b.cir
1 Series combination of two transistors
2 .include TSMC_180nm.txt
3 .param SUPPLY=1.8
4 .param LAMBDA=0.09u
5 .param width_N=20*LAMBDA
6 .global gnd vdd
7
8 VDS D gnd 1.8V
9 VGS G gnd 1.8V
10 * MOSFET DECLARATION
11 M1 D gnd gnd CMOSN W={width_N} L={4*LAMBDA}
12 + AS={(5*width_N*LAMBDA)} PS={(10*LAMBDA+2*width_N)}
13 + AD={(5*width_N*LAMBDA)}
14
15 * Performing DC Sweep
16 .dc VDS 0 3 0.01
17
18 * Control for plots
19 .control
20 set hcopypscolor = 1 *White background for saving plots
21 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
22 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
23
24 run
25 let x = (-VDS#branch)
26 set curplottitle="Q4b Id vs Vds Characteristics"
27 plot x
28
29 hardcopy fig_Q4b.eps (-VDS#branch)
30 .endc
```

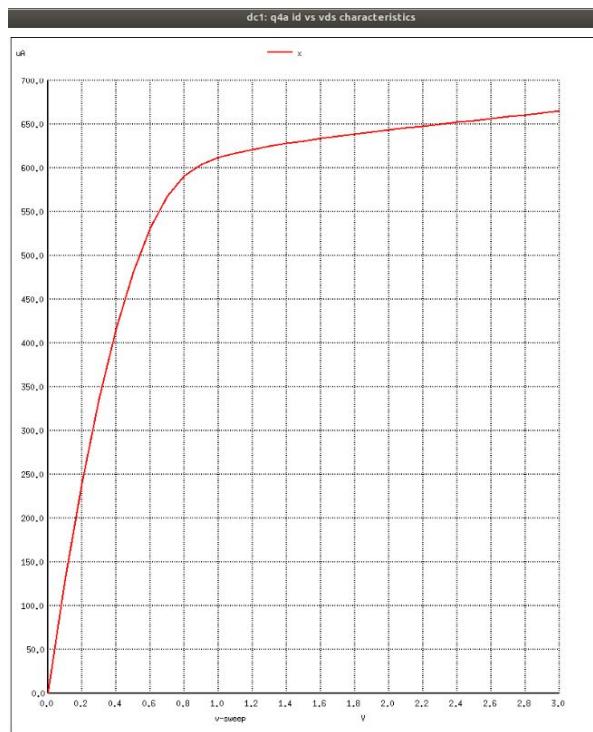
State of MOSFET Operation:

When the V_{DS} goes from 0 to 3V, initially the MOSFET is in linear region till V_{DS}<= V_{GS}-V_{TH} due to which we observe a linear current increase with respect to V_{DS}.

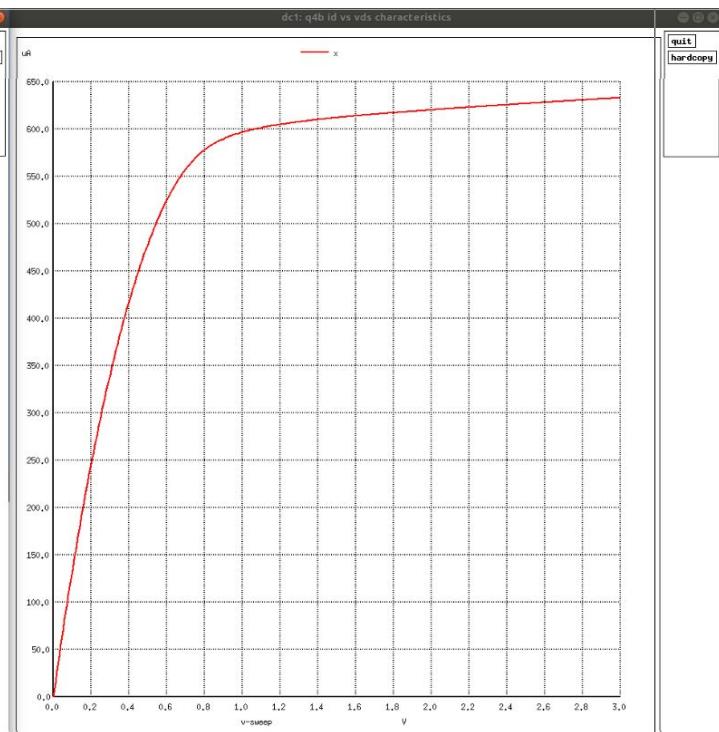
Then $I_{D,lin} = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T)V_{DS} - V_{DS}^2]$ $\begin{cases} V_{GS} \leq V_T \\ V_{DS} > V_{GS} - V_T \end{cases}$ when $V_{ds} > V_{th}$, the MOSFET moves to the saturation region.

$$I_{D,sat} = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \begin{cases} V_{GS} \leq V_T \\ V_{DS} \leq V_{GS} - V_T \end{cases}$$

PLOTS:



Id vs Vds for A.



Id vs Vds for B.

OBSERVATIONS:

- Theoretically we must see that a combination of two W/L NMOS devices should give equal drain current flow across them.
- But practically we can see that in (B) the drain current is lower than in (A) by a difference of 3.4 micro-Ampere(uA).**

Reasons for discrepancy in (A) and (B):

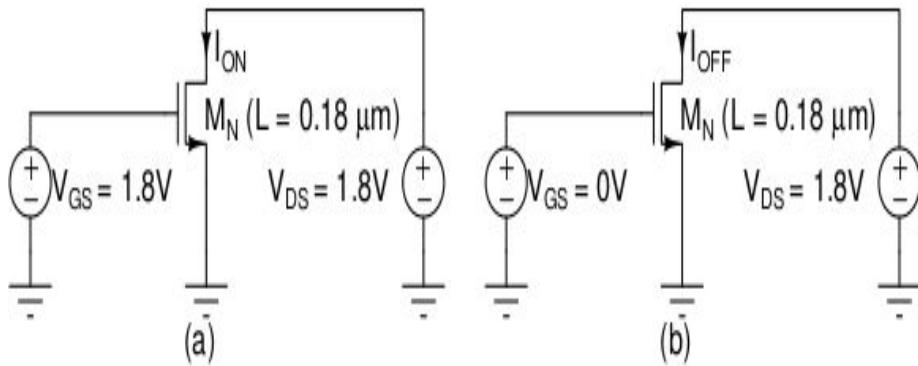
When we take a combination of two W/L NMOS, we notice that there is a role of drain capacitance of the lower NMOS and the source capacitance of the upper NMOS as these two capacitance are present in between the two MOS's channels.

Due to these two parasitic capacitance in parallel there is a new capacitance of $C_d + C_s$ which affects the way the transistors charge or discharge, which in turn is the reason why we see more current in (A).

In (B) we only have a single MOSFET due to which we don't see such extra parasitic capacitance playing a role in affecting the I_d .

Question 5:

Circuit:



Codes:

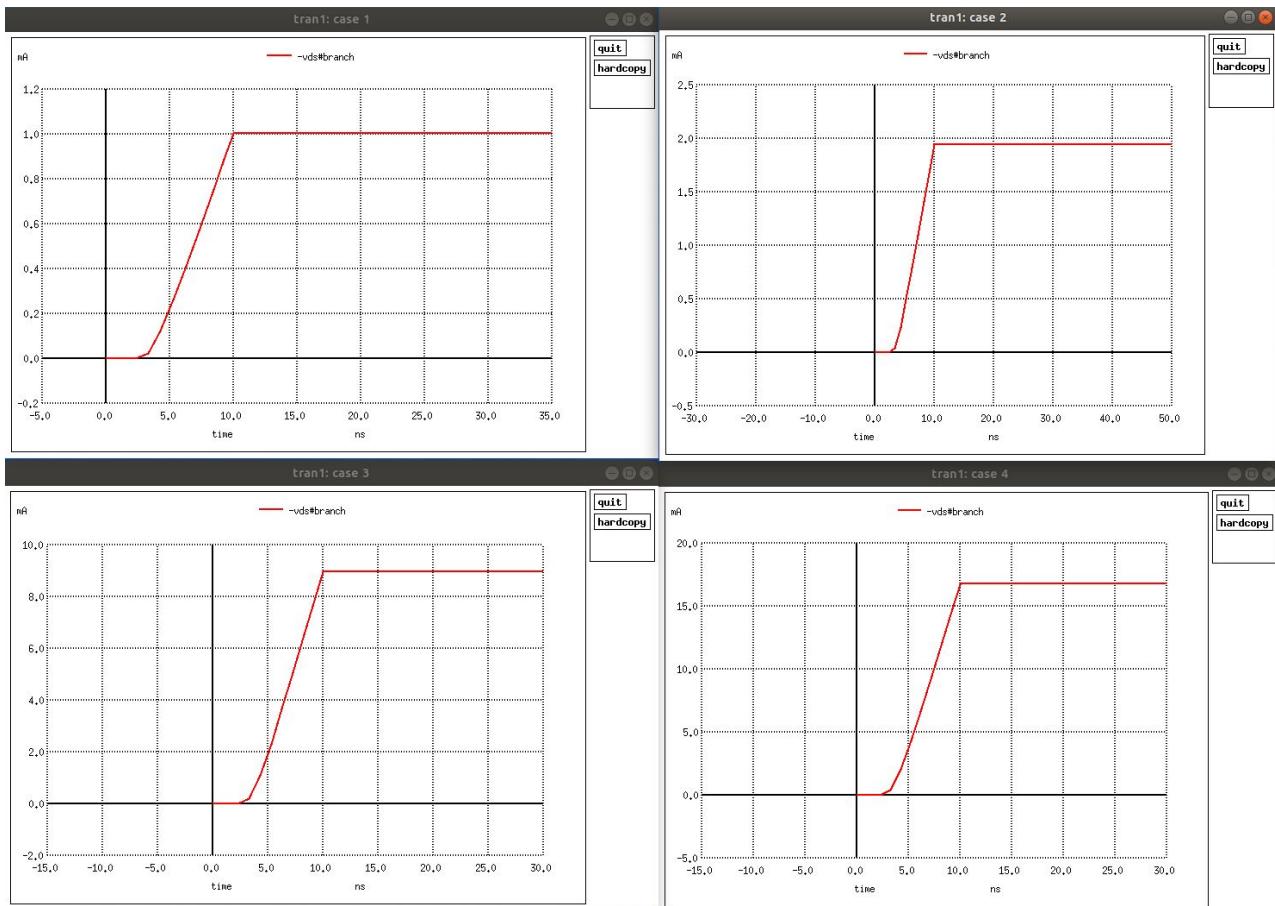
```
VLSI Assignment-1 > Question5 > Q5_I_Case_1.cir
1  VLSI Assignment Question 5 for I_On
2  * Answers to question 5 I_On Calculation
3  .include TSMC_180nm.txt
4  .param SUPPLY=1.8
5  .param LAMBDA=0.09u
6  .param width_N={20*LAMBDA}
7  .global gnd vdd
8
9  VGS G gnd 0
10 VDS D gnd 'SUPPLY'
11
12 M1 D G gnd gnd CMOSN W={width_N} L={2*LAMBDA}
13 + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
14 + AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
15
16 VGS G 0 pulse 0 1.8 0ns 10ns 10ns 1000ns 2000ns
17 .tran 1ns 2000ns
18
19 .control
20 set hcopypscolor = 1 *White background for saving plots
21 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7))
22 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7))
23
24 run
25 | set curplottitle="Case 1"
26 plot -VDS#branch
27 set hcopypscolor = 1 *White background
28 hardcopy fig_Q5_I.eps -VDS#branch
29 .endc
```

NOTE: For other cases, only the parameters need to be tweaked. For consistency, only one example has been provided in the report

Simulation Method:

- Take a pulse which goes from 1.8V to 0V after a certain time and do a transient analysis.
- By doing this, we can observe both Ion and Ioff in the same plot.
- When the voltage $V_g = 1.8V$, we will get the peak Ion for each width case.
- When the voltage $V_g = 0V$, after some time we will have some oscillations in the I_{off} very close to 0A in the pA/nA region.

Plots for Ion:



LEGEND for Ion and Ioff plots:

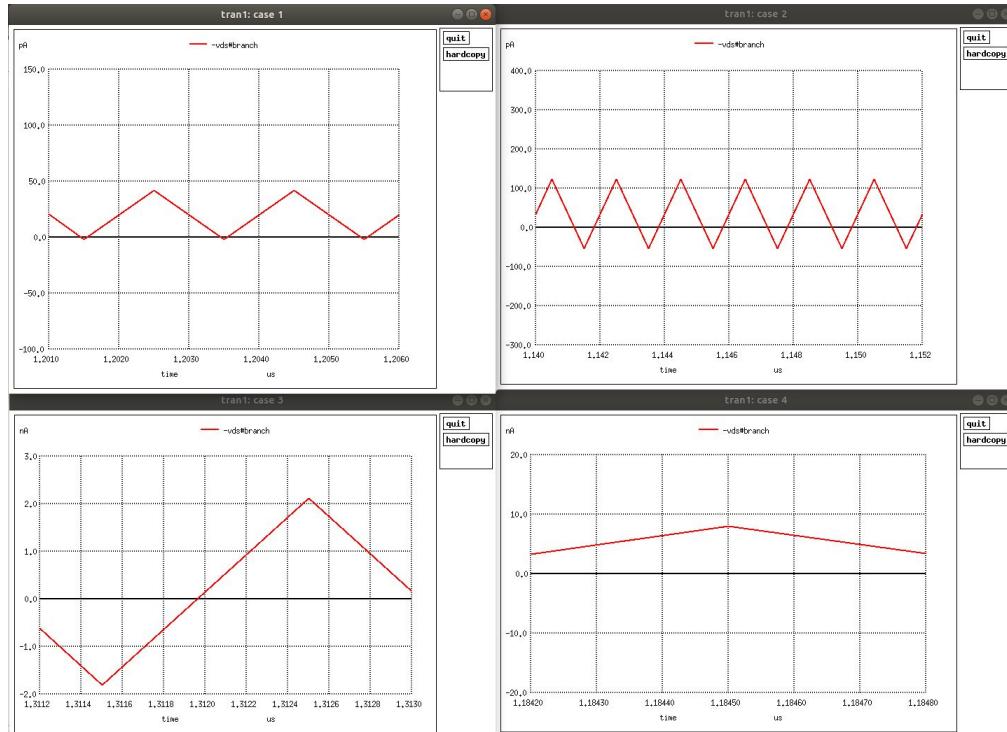
TOP -LEFT : $W = 1.8\mu m$

TOP-RIGHT: $W = 3.6\mu m$

BOTTOM-LEFT: $W = 18\mu m$

BOTTOM-RIGHT: $W = 36\mu m$

Plots for Ioff:



Observation Table:

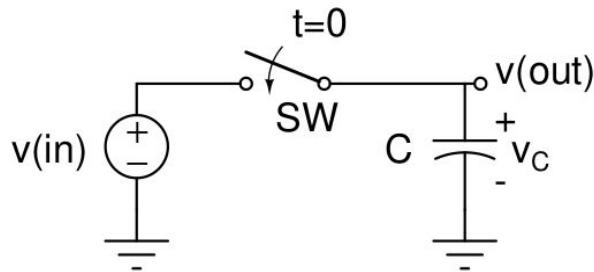
Serial Number	Width	Peak I _{on}	Average I _{off}
1	1.8um	1.00368mA	20pA
2	3.6um	1.94116mA	33.5pA
3	18um	8.97936mA	1.44nA
4	36um	16.7483mA	9.8nA

- We see that the **peak I_{on} and average I_{off} increases with respect to the increase in the Width of the MOSFET.**
- Although there is a steady increase, we only observe a linear increase in the peak I_{on}.
- The peak I_{on} approximately linear as we see that for 1.8 ,18um and 3.6, 36um pairs differ by approximately a factor of 10 and it is similar due to **channel width modulation**.
- Theoretically we expect that as the Gate Voltage is 0, the drain current must drop to 0 as well because the MOS is not activated.
- But practically we see a current in the pico/nano ampere region. This is mainly due to the incorrect assumption we have made that current is zero when $V_{gs} < V_t$. There is some inversion charge at the surface, which gives rise to sub-threshold current flowing between the drain and the source of the MOSFET.

- We also see a slight linearity for average loff which is also mainly due to the channel width modulation.

Question 6:

Circuit:

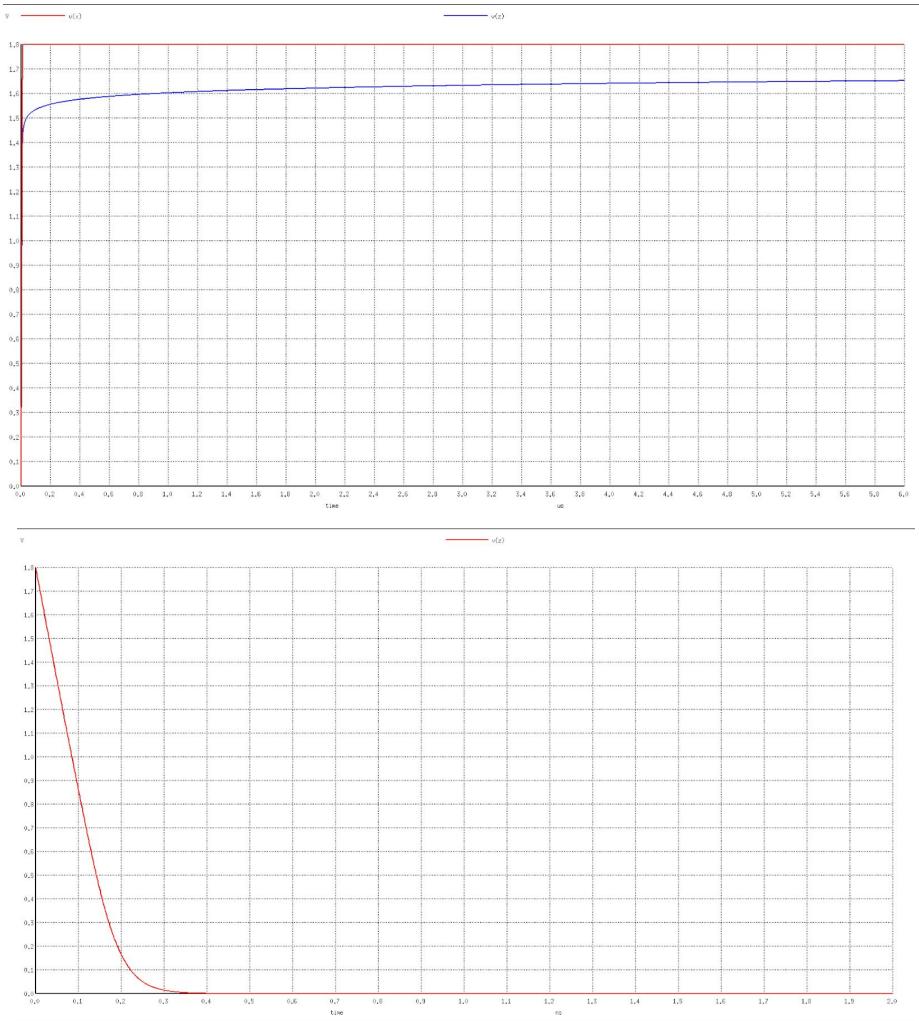


A) NMOS:

Code:

<pre> Q6a_i.cir x VLSI Assignment-1 > Question6 > Q6a_i.cir 1 VLSI Assignment Question 6ai 2 * Answers to question 6ai 3 .include TSMC_180nm.txt 4 .param SUPPLY=2.2 5 .param LAMBDA=0.18u 6 .param width_N=10*LAMBDA 7 .global gnd vdd 8 9 Vdd vdd gnd 'SUPPLY' 10 vin x pulse 0 1.8 0ns 10ns 10ns 6000ns 6000ns 11 12 M1 x vdd z gnd CMOSN W=(width_N) L={LAMBDA} 13 + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} 14 + PD={10*LAMBDA+2*width_N} 15 16 Cout z gnd 100f 17 18 .ic v(z)= 0 19 .tran 0.1n 6000n 20 21 .control 22 set hcopypscolor = 1 *White background for saving plots 23 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7) 24 set color1=black ** color1 is used to set the grid color of the plot [manual sec:17.7] 25 26 27 run 28 plot v(x) v(z) 29 hardcopy fig_06_i.eps v(x)v(z) 30 .endc </pre>	<pre> Q6a_ii.cir x VLSI Assignment-1 > Question6 > Q6a_ii.cir 1 VLSI Assignment Question 6ai 2 * Answers to question 6a (ii) 3 .include TSMC_180nm.txt 4 .param SUPPLY=1.8 5 .param LAMBDA=0.18u 6 .param width_N=10*LAMBDA 7 .global gnd vdd 8 9 Vdd vdd gnd 'SUPPLY' 10 vin x gnd 0 11 12 M1 x vdd z gnd CMOSN W=(width_N) L={LAMBDA} 13 + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} 14 + PD={10*LAMBDA+2*width_N} 15 16 Cout z gnd 100f 17 18 .ic v(z)= 1.8 19 .tran 0.001n 2n 20 21 .control 22 set hcopypscolor = 1 *White background for saving plots 23 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7) 24 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7) 25 26 27 run 28 plot v(z) 29 hardcopy fig_06a_ii.eps v(z) 30 .endc </pre>
--	--

Capacitor Charge & Discharge Cases for NMOS:



Observation:

Case 1: Capacitor Charges for V(in) = 1.8V

- We see that in NMOS, the capacitor undergoes charging but does not reach the input value of 1.8V.
- This is due to the fact that capacitor charges only till $V_{gs} \geq V_{th}$. After that, NMOS turns off ($V_{gs} < V_{th}$) due to which the capacitor does not reach the input value.

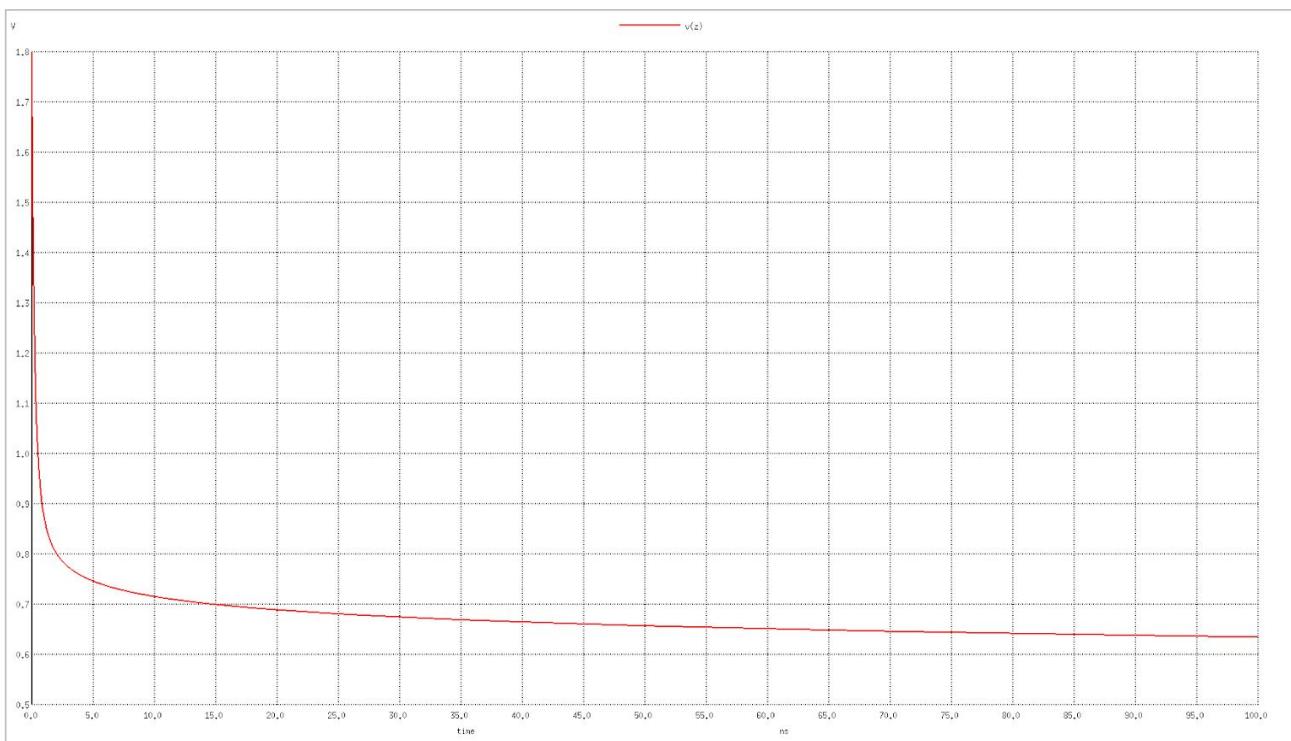
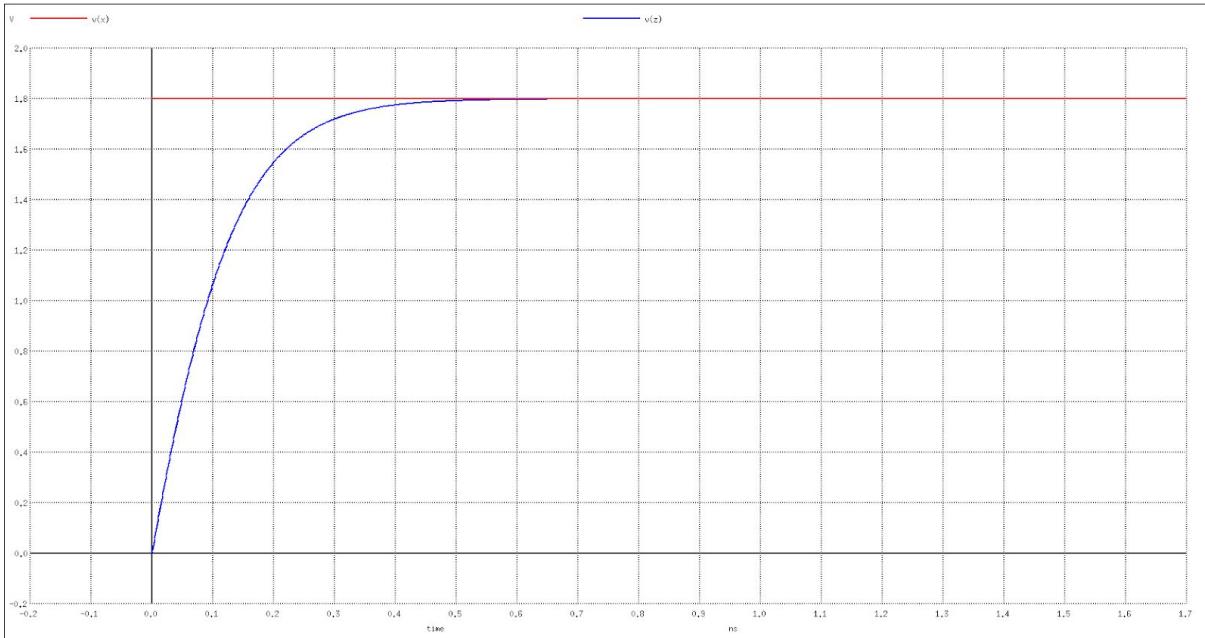
Case 2: Capacitor Discharges for V(in) = 0V

The gate-source voltage does not change in this case when the capacitor is discharging. Therefore, the capacitor gets fully discharged to 0V

B) PMOS:

Code:

Capacitor Charge & Discharge for PMOS:



Observation:

In general, as NMOS and PMOS are complementary in nature with respect to each other, we observe the following:

Case 1: Capacitor Charges for $V(\text{in}) = 1.8V$

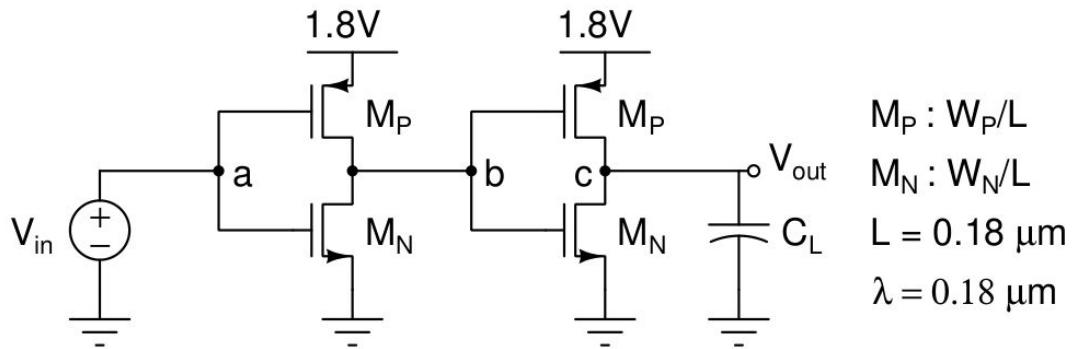
- The capacitor fully charges to the input voltage of 1.8V as the V_{sg} is always the same so the PMOS does not switch off.

Case 2: Capacitor Discharges for $V(\text{in}) = 0V$

- Here, the capacitor does not fully discharge to 0V. Instead, we see that it stops at approximately 0.58V.
- This is due to the fact that when $V_{\text{sg}} < V_t$ occurs after a point when the capacitive voltage equals threshold voltage.
- Due to this condition, the PMOS is switched off and doesn't discharge further.

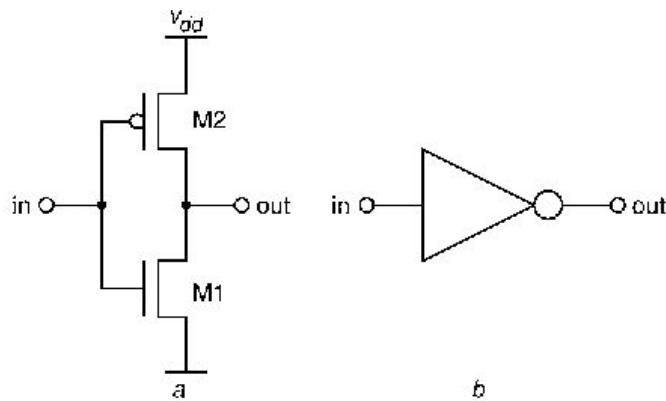
Question 7:

Circuit:

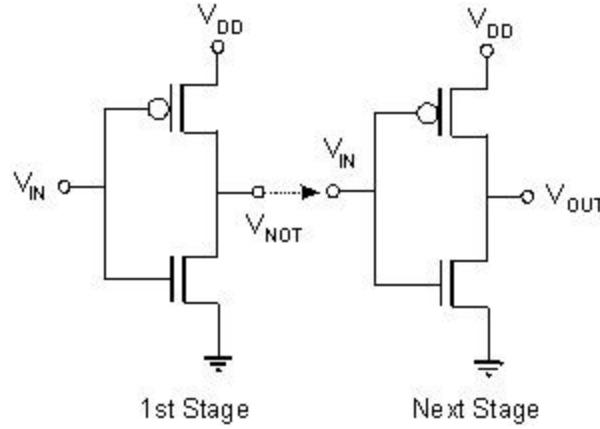


Theoretical Expectation:

Simple CMOS Inverter's first stage:



Combination of two CMOS inverters acts like a double inverter to give a output in the same shape as the input pulse but with some delay acting like a buffer. The delay is dependent



Code:

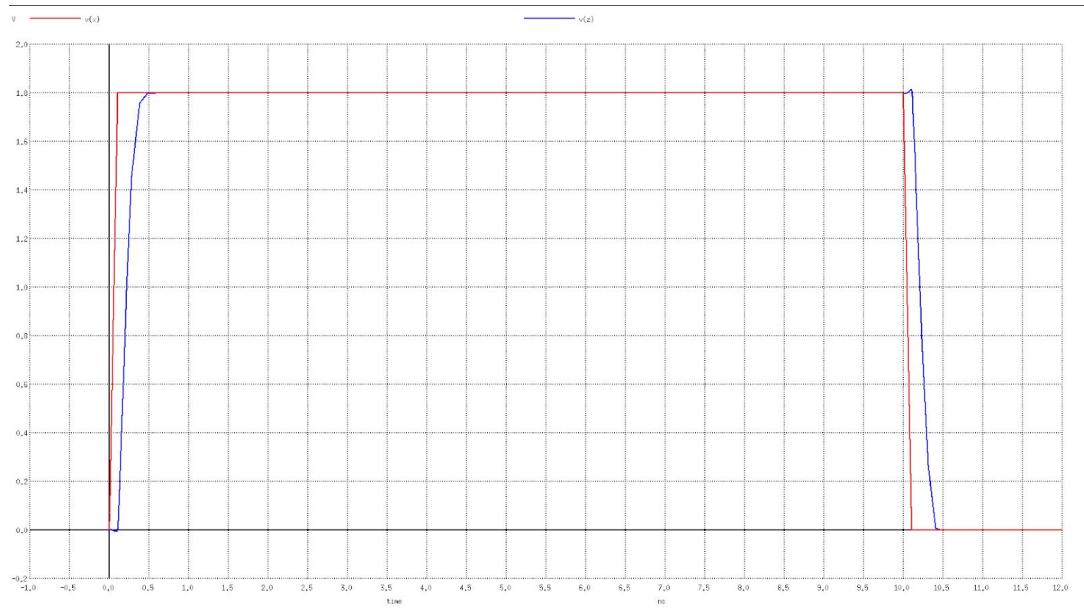
```

VLSI Assignment-1 > Question7 > Q7a.cir
1  VLSI Assignment Question 7a
2  * Answers to question 7a
3  .include TSMC_180nm.txt
4  .param SUPPLY=1.8
5  .param LAMBDA=0.18u
6  .param width_N=10*LAMBDA
7  .param width_P=2.5*width_N
8  .global gnd vdd
9
10 Vdd vdd gnd 'SUPPLY'
11 vin x 0 pulse 0 1.8 0ns 100ps 100ps 9.9ns 20ns
12
13 M1      y      x      gnd      gnd   CMOSN  W={width_N}  L={LAMBDA}
14 + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
15
16 M2      y      x      vdd      vdd   CMOSP  W={width_P}  L={LAMBDA}
17 + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
18
19 M3      z      y      gnd      gnd   CMOSN  W={width_N}  L={LAMBDA}
20 + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
21
22 M4      z      y      vdd      vdd   CMOSP  W={width_P}  L={LAMBDA}
23 + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
24
25 Cout z gnd 100f
26
27 .tran 0.1n 60n
28
29 ** MEASURING DELAYS (Refer manual section 15.4.5)
30 .measure tran tperiod
31 + TRIG v(y) VAL='SUPPLY/2' RISE=1
32 + TARG v(y) VAL='SUPPLY/2' RISE=2
33 .measure tran tpd
34 + TRIG v(y) VAL='SUPPLY/2' FALL=1
35 + TARG v(z) VAL='SUPPLY/2' RISE=1
36
37 .measure tran tpdf
38 + TRIG v(y) VAL='SUPPLY/2' RISE=1
39 + TARG v(z) VAL='SUPPLY/2' FALL=1
40
41 .measure tran tpd param='(tpdr+tpdf)/2' goal=0
42 .measure tran diff param='tpdr-tpdf' goal=0
43
44
45 .control
46 set hcopyright= 1 *White background for saving plots
47 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7))
48 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7))
49
50
51 run
52 *plot v(a)
53 *plot v(b)
54 plot v(x) v(z)
55
56 hardcopy fig_07a.eps v(x)v(z)
57 .endc

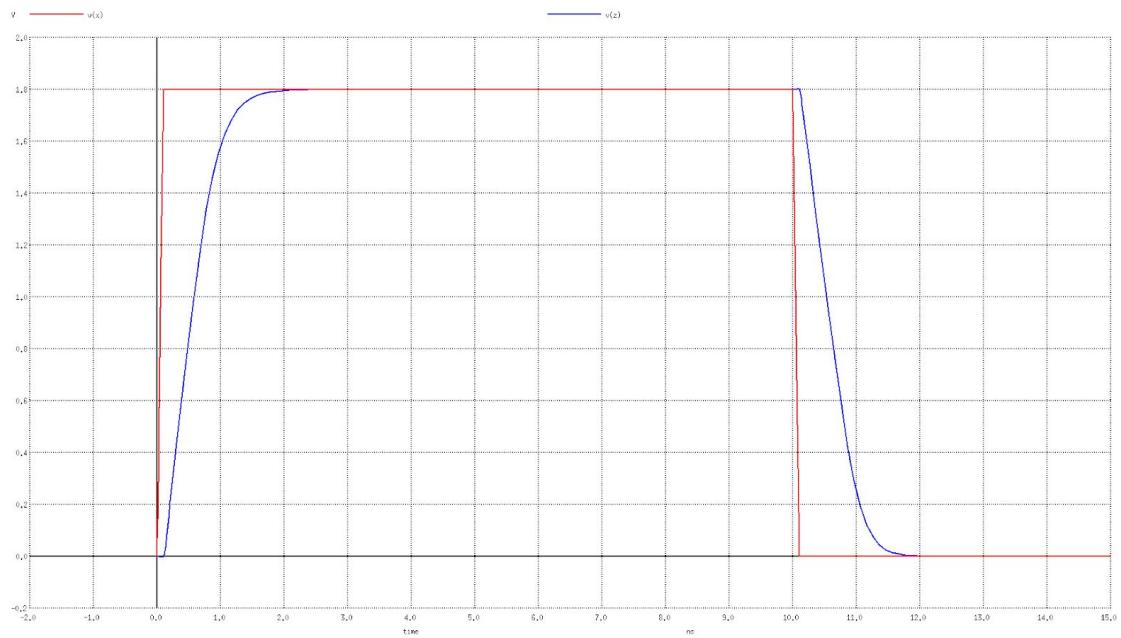
```

Plots:

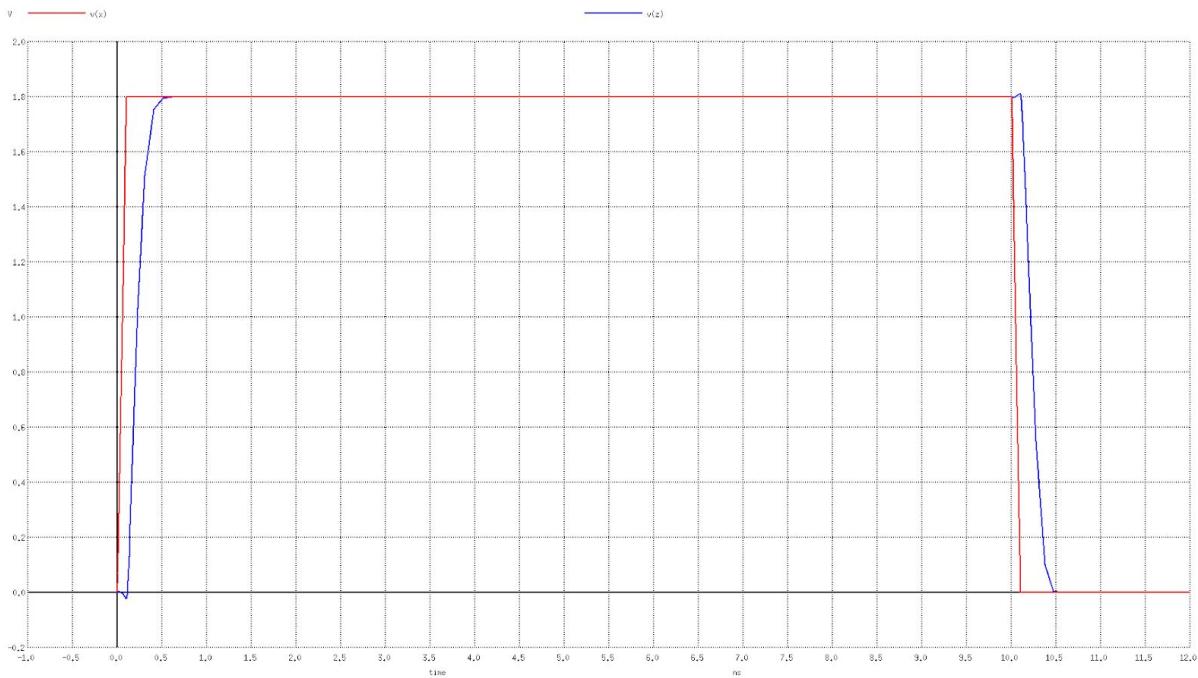
(a) CL = 100 fF, Wn = 1.8 μ m Wp = 2.5 \times Wn



(b) CL = 500 fF, Wn = 1.8 μ m Wp = 2.5 \times Wn



(c) CL = 500 fF, Wn = 9μm Wp = 2.5 × W n



Observation Table:

NMOS Width	PMOS Width	Capacitance	Rise-Time	Fall-Time	Delay
1.8um	4.5um	100fF	10.9425ns	12.1116ns	11.527ns
1.8um	4.5um	500fF	43.3369ns	49.1465ns	46.2415ns
9um	22.5um	500fF	11.73026ns	13.1203ns	12.4253ns

- In the above table delay = (rise + fall)/2 as it is the average propagation delay of both rise and fall.
- We notice that the delay increases as the capacitance increases. This is due to the increase in time taken for the charge and discharge of the 500fF capacitor over 100fF.
- Thus to achieve high speed circuits one has to minimize the load capacitance seen by a gate.
- By **increasing the width of the MOS, we see that the delay decreases**. This can be correlated to a decrease in the area of the MOSFET as a capacitor which is in series with the load capacitance thereby, reducing the total capacitance and decreasing the delay.
- This delay vs width proportionality can also be derived from the substituting the current equation in the capacitor voltage calculation.