

VLSI DESIGN

Assignment-2

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Roll Number: 2019102014

Question 3

(A)

Circuit:

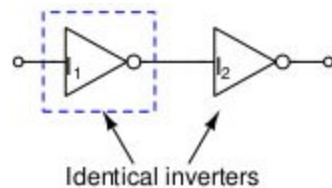


Figure 1

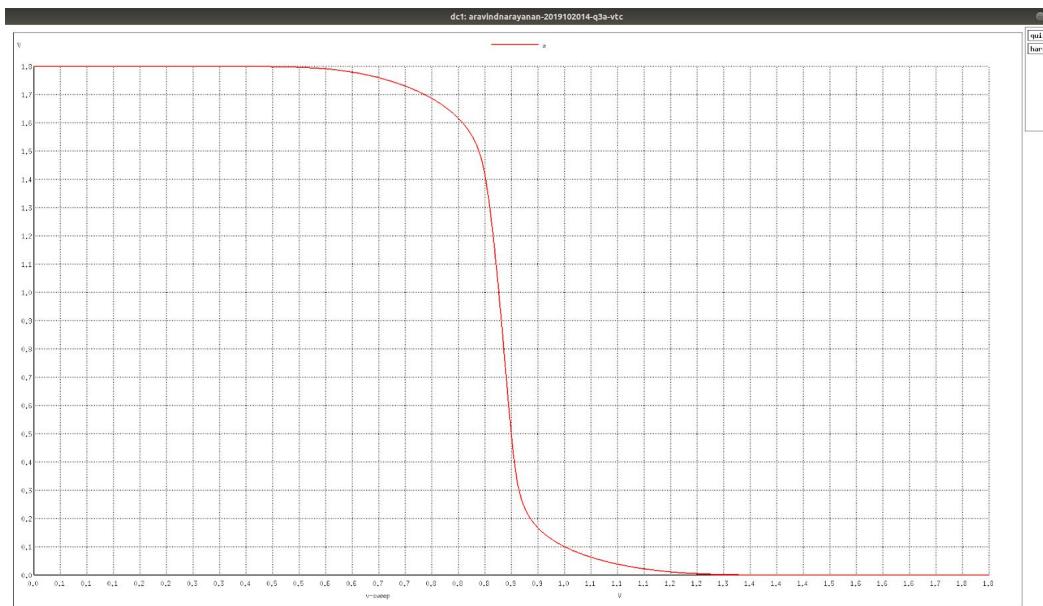
Theoretically this circuit acts like a buffer as it is a combination of two CMOS inverters.

Netlist:

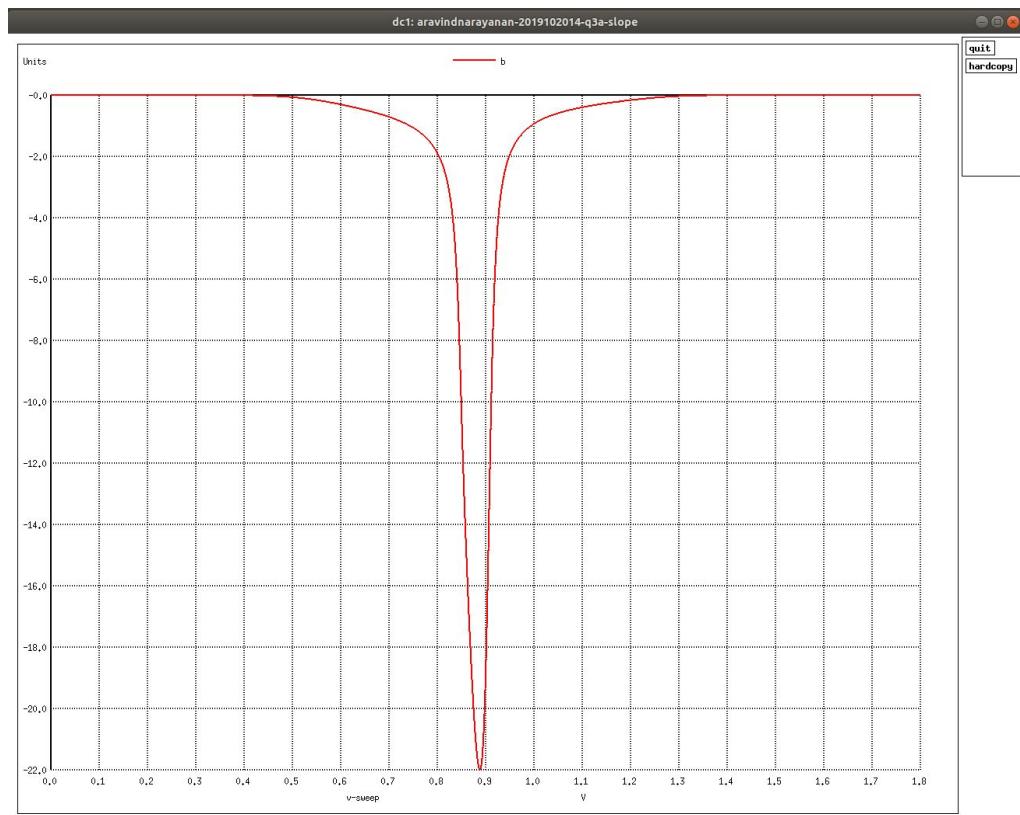
```
Question 3 > Pre_Layout.cir
 1 VLSI Assignment Question 3S=a
 2 * Answers to question 3a
 3 .include TSMC_180nm.txt
 4 .param SUPPLY=1.8
 5 .param LAMBDA=0.09u
 6 .param width_N=20*LAMBDA
 7 .param width_P=2.5*width_N
 8 .global gnd vdd
 9
10 Vdd vdd gnd 1.8V
11 vin x 0 0V
12
13 M1 y x gnd gnd CMOSN W={width_N} L={2*LAMBDA}
14 + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
15
16 M2 y x vdd vdd CMOSP W={width_P} L={2*LAMBDA}
17 + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
18
19 M3 z y gnd gnd CMOSN W={width_N} L={2*LAMBDA}
20 + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
21
22 M4 z y vdd vdd CMOSP W={width_P} L={2*LAMBDA}
23 + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
24
25 Cout z gnd 100f
26
27 .dc vin 0 1.8 0.0001
28
29
30
31 .control
32 set hcopypscolor = 1 *White background for saving plots
33 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7))
34 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7))
35
36
37 run
38 let a = v(y)
39 let b = deriv(v(y))/deriv(v(x))
40 set curplottitle="AravindNarayanan-2019102014-Q3a-VTC"
41 plot a
42 set curplottitle="AravindNarayanan-2019102014-Q3a-SLOPE"
43 plot b
44
45 hardcopy fig_Q3a.eps v(z) deriv(v(y))/deriv(v(x))
46 .endc
```

Figure:

(I) Voltage Transfer Characteristics:

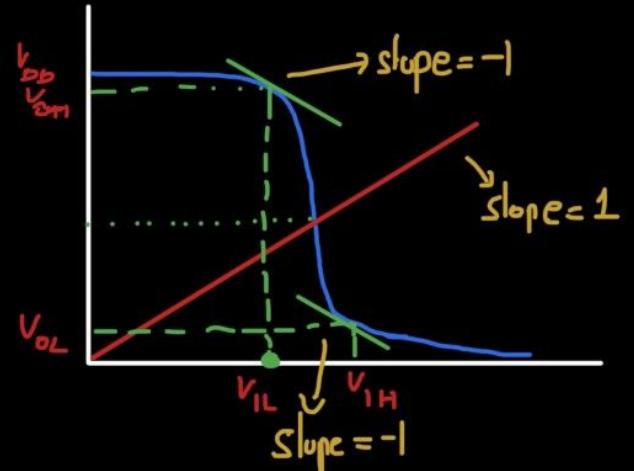
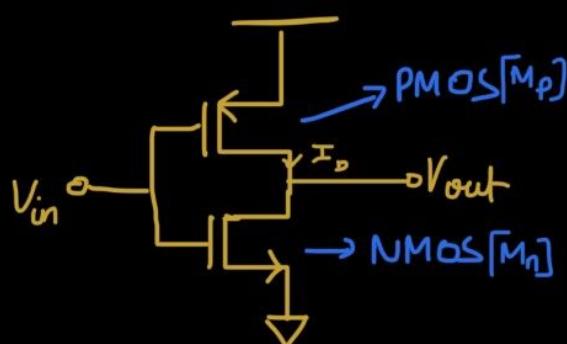


(II) Slope of VTC (deriv(Vout)/deriv(Vin))



(B)

CMOS Inverters:



V_{IH} = Minimum input voltage considered high state

V_{IL} = Maximum input voltage considered low state

V_{OH} = Minimum output voltage which can be considered as 'high'

V_{OL} = Maximum output voltage which can be considered as 'low'

$$\left. \begin{array}{l} \text{Voltage Noise Margins } (NM_H) = V_{OH} - V_{IH} \\ \text{Voltage Noise Margins } (NM_L) = V_{IL} - V_{OL} \end{array} \right\} \text{ Ideally } NM_H = NM_L = \frac{V_{DD}}{2}$$

NMOS ≈

$$V_{GS} = V_{in}$$

$$V_{DS} = V_{out}$$

PMOS ≈

$$V_{GS} = V_{in} - V_{DD}$$

$$V_{DS} = V_{out} - V_{DD}$$

$$V_{GS} = -V_{SG}$$

$$V_{DS} = V_{SD}$$

① Calculating V_i :

$$\text{When } V_I = V_L, \frac{dV_{out}}{dV_{in}} = 1$$

NMOS is in saturation
PMOS is in linear

$$\text{As } I_{Dn} = I_{Dr},$$

$$\frac{R_n}{\alpha^2} [V_i - V_{thn}]^2 = \frac{k_p}{2} [V_{SD} - |V_{thp}|] k_{SO} - V_{SD}^2$$

$$\frac{R_n}{R_p} [V_i - V_{thn}]^2 = [V_{DD} - V_i - |V_{thp}|] [V_{Dn} - V_{out}] - [V_{Dn} - V_{out}]^2$$

Take $R_n = R_p$ and express V_{out} in terms of V_{out}

$$V_{out} - V_{DD} = [V_{DD} - V_i - |V_{thp}| \pm \sqrt{[V_{DD} - V_i - |V_{thp}|]^2 - [V_i - V_{thn}]^2}]$$

$$V_{out} = V_{DD} - V_{DD} + V_i + |V_{thp}| \mp \sqrt{[V_{DD} - V_i - |V_{thp}|]^2 - [V_i - V_{thn}]^2}$$

①

Differentiate w.r.t V_{in}

(1)

$$\frac{dV_{out}}{dV_m} = 1 \mp \sqrt{\frac{V_{DD} - |V_{thp}| - V_{thn}}{V_{DD} - 2V_i - |V_{thp}| + V_{thn}}}$$

$$\downarrow \\ -1 \text{ for } V_i = V_{I_L}$$

$$Q = \sqrt{\frac{V_{DD} - |V_{thp}| - V_{thn}}{V_{DD} - 2V_{I_L} - |V_{thp}| + V_{thn}}}$$

Negative isn't possible

Above equation is simplified to get V_{I_L} in terms of other terms

$$V_{I_L} = \frac{3V_{DD} + 5V_{thn} - 3|V_{thp}|}{8}$$

As when $V_{in} = V_{I_L}$, $V_{out} = V_{OH}$ we substitute in (1) to find V_{OH}

$$V_o = V_I + |V_{thp}| + \sqrt{[V_{DD} - V_I - |V_{thp}|]^2 - [V_I - V_{thn}]^2}$$

$$V_{OH} = \frac{7V_{DD} + |V_{thp}| + V_{thn}}{8}$$

Calculating V_{IL} ,

When $V_I = V_L$, $\frac{dV_{out}}{dV_I} = -1$, $V_{out} = V_{UL}$

NMOS \rightarrow Saturation

PMOS = Linear

As $I_{Dn} = I_{Dp}$,

$$\frac{k_n}{2} \left[2(V_{GSn} - V_{th})V_{DSn} - |V_{DSn}|^2 \right] = \frac{k_p}{2} \left[V_{SG} - |V_{thp}| \right]^2$$

Taking $k_n = k_p$

$$2 \left[V_I - |V_{thn}| \right] V_{out} - |V_{out}|^2 = \left[V_{DD} - V_I - |V_{thp}| \right]^2$$

Express V_{out} in terms of ~~and~~ and,

$$V_{out} = V_I - V_{thn} \pm \sqrt{\left[2V_I - V_{DD} - |V_{thp}| - |V_{thn}| \right] \left[V_{DD} - V_I - |V_{thp}| \right]} \quad (3)$$

Differenzial WRT V_{in} and $\frac{V_{out}}{V_{in}} = -1$ when $V_I = V_{I+}$

$$-1 = 1 \pm \sqrt{\frac{V_{DD} - |V_{thp}| - V_{th}}{\alpha V_{I+} - V_{th} - |V_{thp}| - V_{DD}}}$$

$$\alpha = \sqrt{\frac{V_{DD} - |V_{thp}| - V_{th}}{\alpha V_{I+} - V_{th} - |V_{thp}| - V_{DD}}}$$

$$V_{I+} = \frac{5V_{DD} + 3V_{th} - 5|V_{thp}|}{\alpha}$$

Substitute V_{I+} for V_I in ②

$$V_{OL} = \frac{V_{DD} - |V_{thp}| - V_{th}}{\alpha}$$

Now we calculate the final noise margins:

$$N_{MH} = V_{OH} - V_{IH} = \frac{V_{DD} - V_{Thn} + 3|V_{Thp}|}{4}$$

$$N_{ML} = V_{IL} - V_{OL} = \frac{V_{DD} - |V_{Thp}| + 3V_{Thn}}{4}$$

From previous assignment, we know that

$$V_{Thn} = 0.473V$$

$$|V_{Thp}| = 0.48V$$

In this question we take $V_{DD} = 1.8V$

So,

$$NM_H = \frac{1.8 - 0.473 + 3(0.48)}{4} = 0.69175V$$

$$NM_L = \frac{1.8 - 0.48 + 3(0.473)}{4} = 0.68475V$$

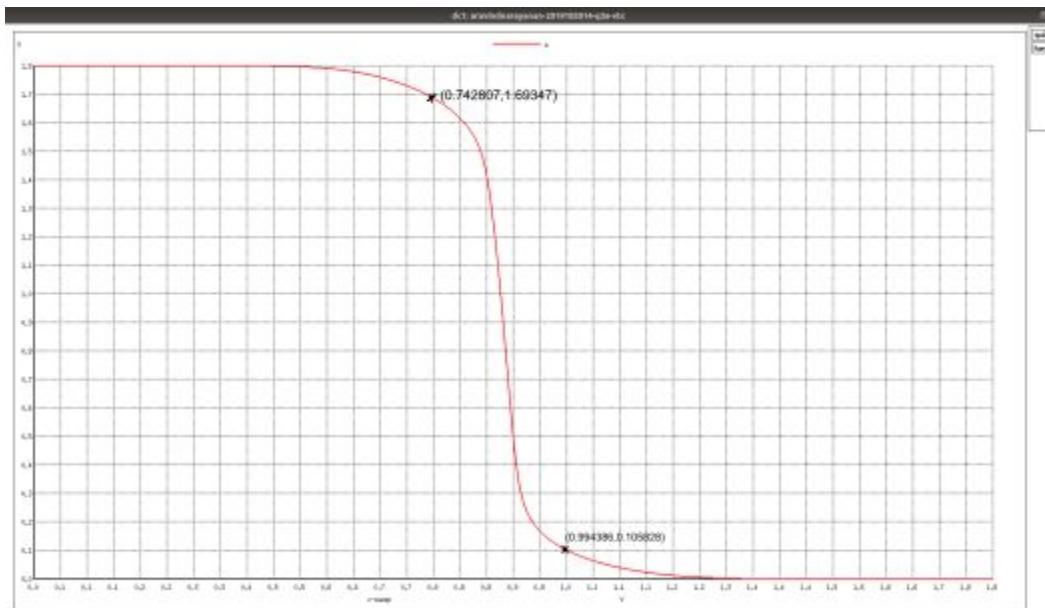
(C)

NETLIST:

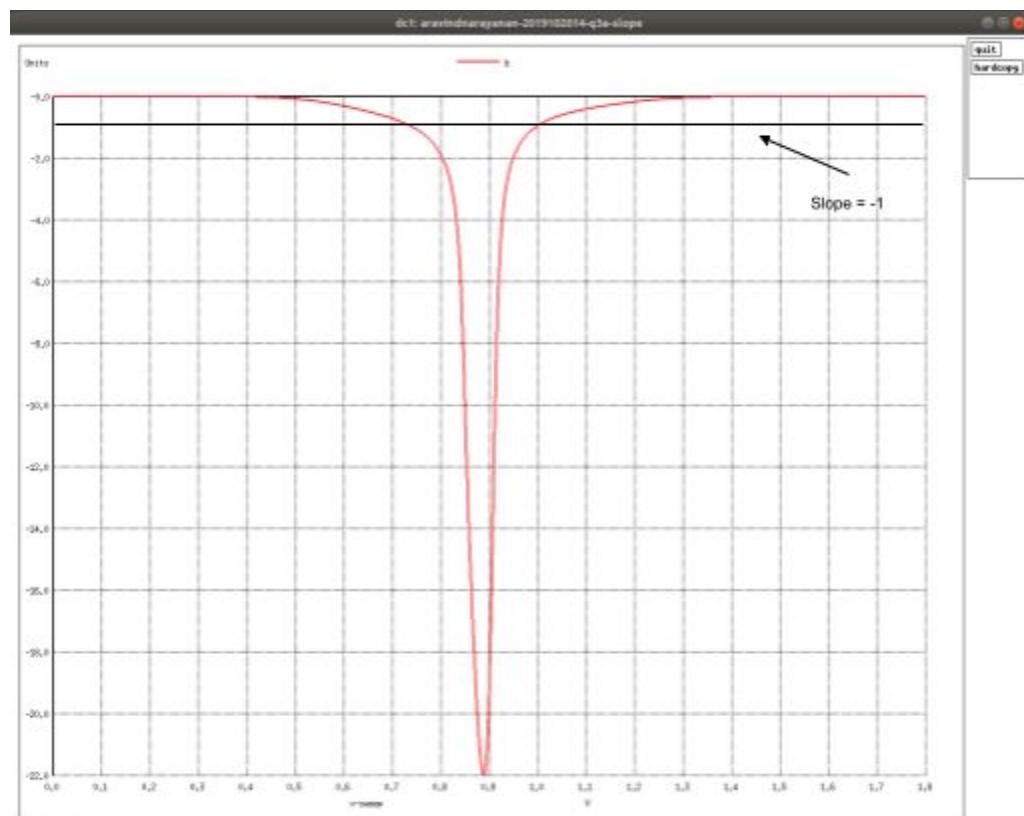
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7  .param width_P=2.5*width_N
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9
10 Vdd vdd gnd 1.8V
11 vin x 0 0V
12
13 M1      y      x      gnd      gnd  CMOSN  W={width_N}  L={2*LAMBDA}
14 + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
15
16 M2      y      x      vdd      vdd  CMOSP  W={width_P}  L={2*LAMBDA}
17 + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
18
19 M3      z      y      gnd      gnd  CMOSN  W={width_N}  L={2*LAMBDA}
20 + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
21
22 M4      z      y      vdd      vdd  CMOSP  W={width_P}  L={2*LAMBDA}
23 + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
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40 set curplottitle="AravindNarayanan-2019102014-Q3a-VTC"
41 plot a
42 set curplottitle="AravindNarayanan-2019102014-Q3a-SLOPE"
43 plot b
44
45 hardcopy fig_Q3a.eps v(z) deriv(v(y))/deriv(v(x))
46 .endc
```

Figure:

(I) Voltage Transfer Characteristics:



(II) Slope of VTC ($\text{deriv(Vout)}/\text{deriv(Vin)}$)



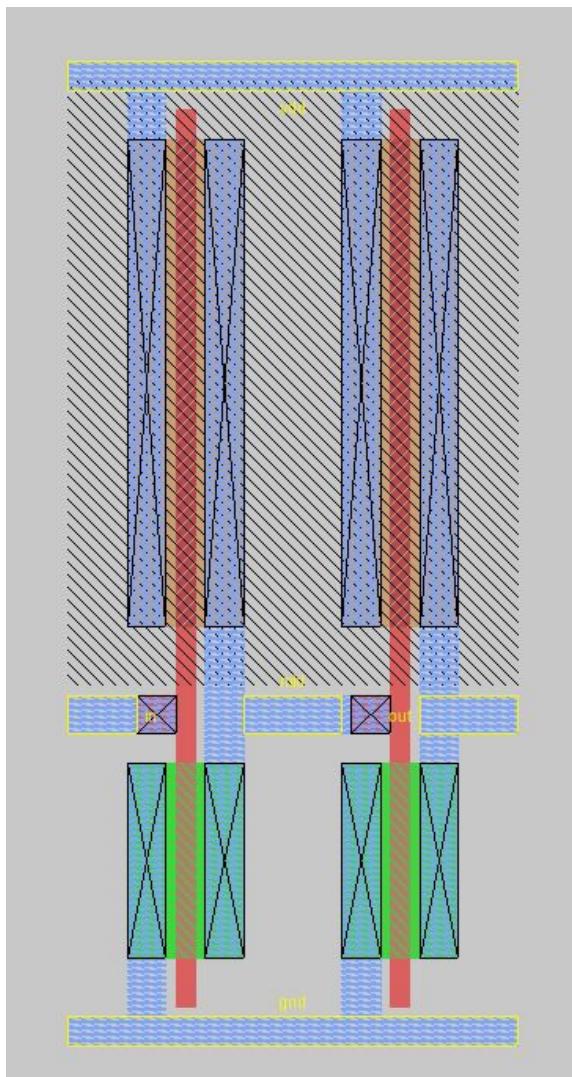
Observations:

Noise Margin Parameters	Practical Values	Theoretical Values
V_{IH}	0.994386V	1.002375VV
V_{IL}	0.742807V	0.790625V
V_{OL}	0.105828V	0.105875V
V_{OH}	1.69347V	1.694125V
NM_H	0.699084V	0.69175V
NM_L	0.636979V	0.68475V

We observe minor differences between the theoretical and NGSpice obtained values which are due to small approximation differences in the calculations.

(D)

Magic Layout:

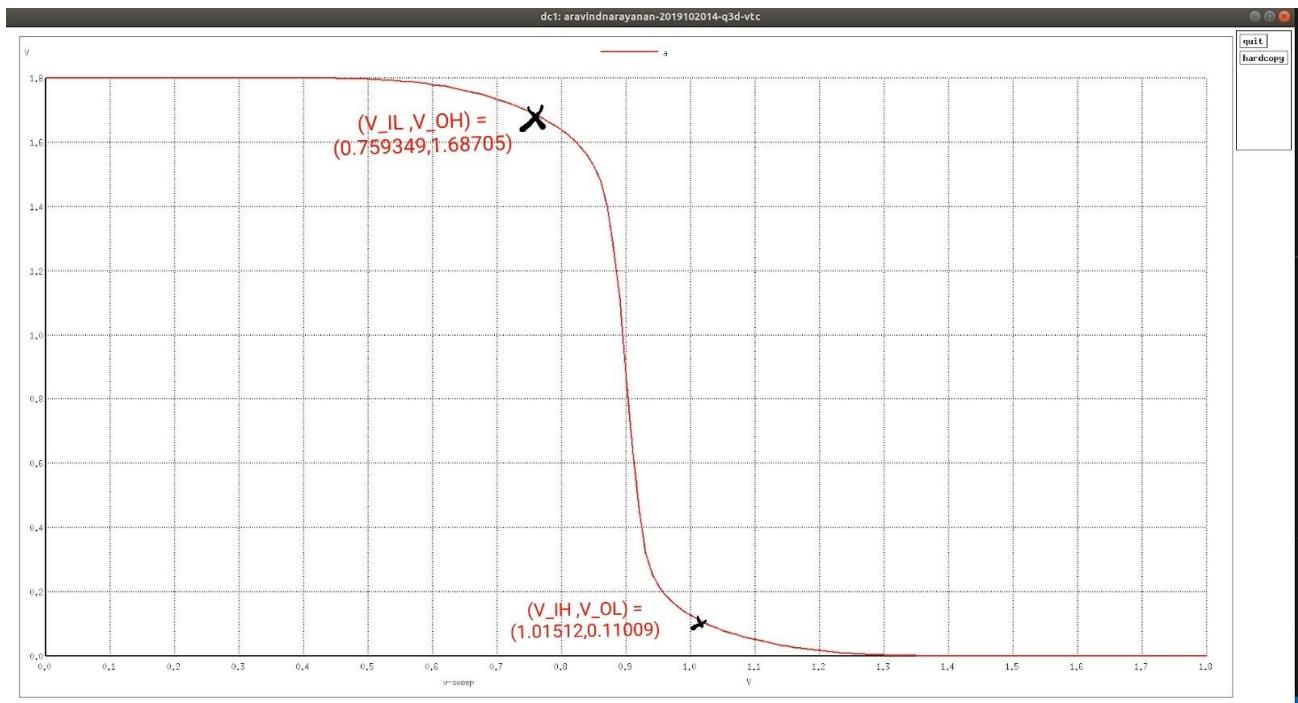


Converted NGSpice Netlist:

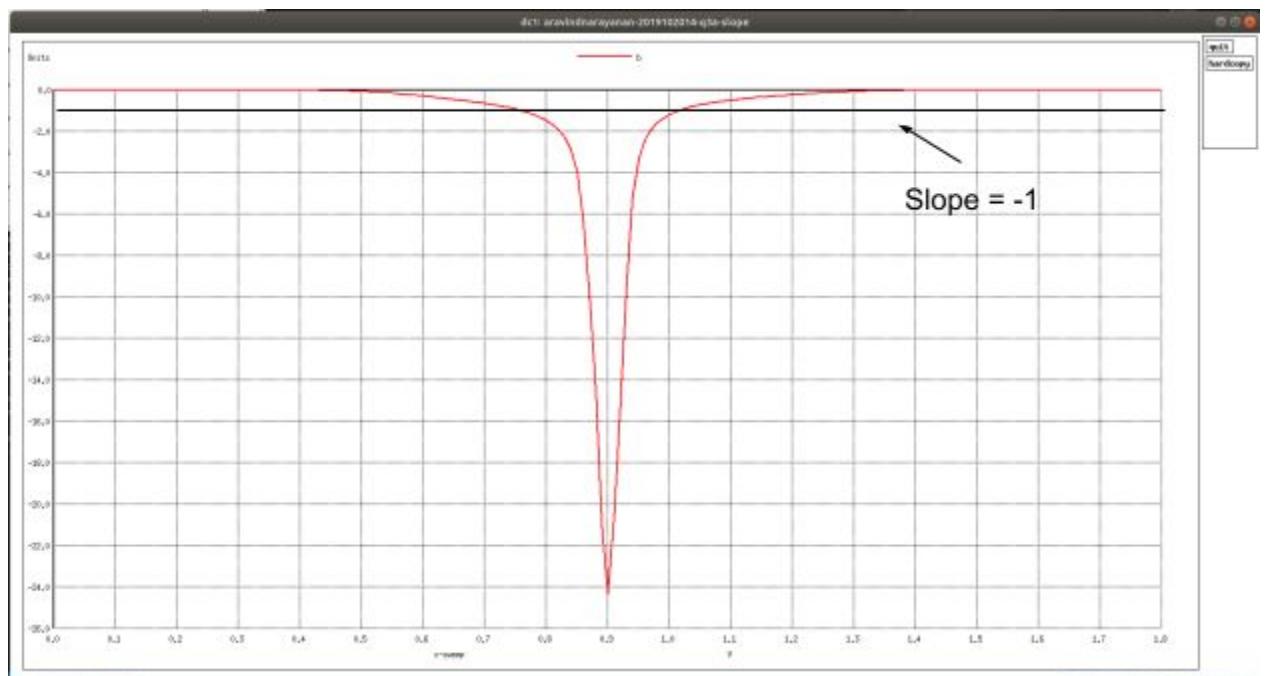
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Question 3 > Post_double_inverter.cir
 1 * SPICE3 file created from double_inverter.ext - technology: scmos
 2 * Answers to question 3
 3 .include TSMC_180nm.txt
 4 .param SUPPLY=1.8
 5 .param LAMBDA=0.09u
 6 .option scale=0.09u
 7 .global gnd vdd
 8
 9 Vdd vdd gnd 1.8V
10 vin in 0 0V
11
12 M1000 mid in vdd w_0_0# CMOSP w=50 l=2
13 + ad=250 pd=110 as=500 ps=220
14
15 M1001 out mid vdd w_0_0# CMOSP w=50 l=2
16 + ad=250 pd=110 as=0 ps=0
17
18 M1002 mid in gnd gnd CMOSN w=20 l=2
19 + ad=100 pd=50 as=200 ps=100
20
21 M1003 out mid gnd gnd CMOSN w=20 l=2
22 + ad=100 pd=50 as=0 ps=0
23
24 C0 w_0_0# gnd 2.9fF
25
26 .dc vin 0 1.8 0.01
27
28 .control
29 set hcopypscolor = 1 *White background for saving plots
30 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
31 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
32
33 run
34 let a = v(mid)
35 let b = deriv(v(mid))/deriv(v(in))
36 set curplottitle="AravindNarayanan-2019102014-Q3d-VTC"
37 plot a
38 set curplottitle="AravindNarayanan-2019102014-Q3d-SLOPE"
39 plot b
40
41 hardcopy fig_Q3d.eps v(mid) deriv(v(mid))/deriv(v(in))
42 .endc
```

FIGURE:

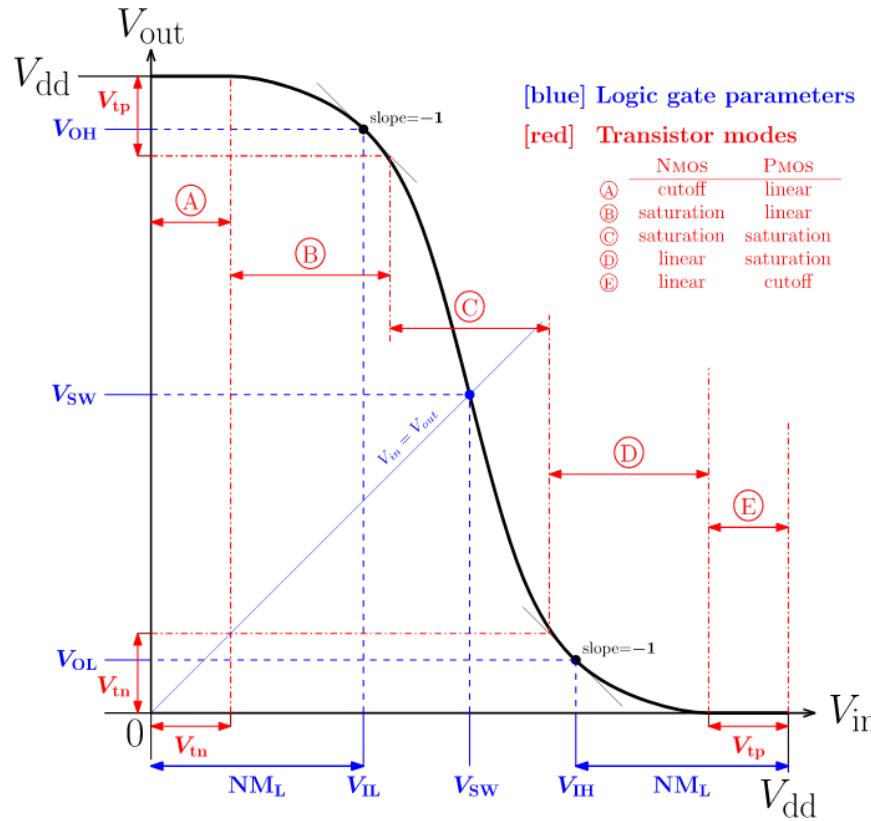
(I) Voltage Transfer Characteristics of I1(Post Layout)



(II) Slope of VTC ($\text{deriv}(V_{mid})/\text{deriv}(V_{in})$)



Procedure:



As shown in this figure, in the switching region the slope at the two points are -1. So we plot the derivative of the VTC with respect to V_{in} and identify where the slopes at -1. Then accordingly we obtain V_{il} and V_{ih} in the derivative graph. Then we observe the y-coordinate for these values in the VTC graph and find V_{ol} and V_{oh} .

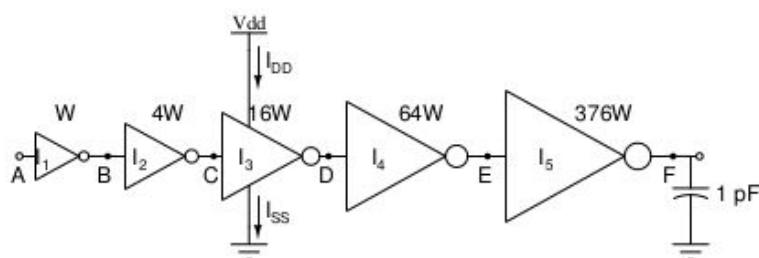
Observations:

Noise Margin Parameters	Pre Layout Values	Post Layout Values
V_{IH}	0.994386V	1.01512V
V_{IL}	0.742807V	0.759349V
V_{OL}	0.105828V	0.11009V
V_{OH}	1.69347V	1.68705V
NM_H	0.699084V	0.67193V
NM_L	0.636979V	0.649259V

We notice that the post-layout and pre-layout values are not the same. In post-layout, we have parasitic capacitances present which aren't present in pre-layout. We also know that in the formula of noise margin calculations are dependent on the threshold voltages. Threshold voltages of the NMOS and PMOS will change depending on the parasitic capacitances present.

Question 4

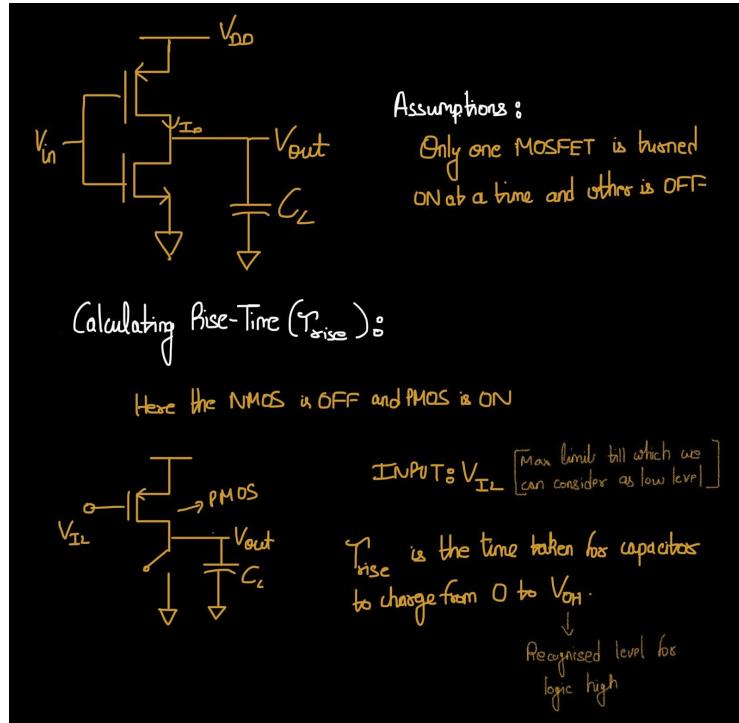
Circuit:



The above figure is a fan-out of 4 inverters which is used to calculate the delay of characterise the delay.

(A)

Rise Time:



Derivation:

$$I_{dp} = \frac{C \cdot dV_o}{dt}$$

$$\int_{V_o=0}^{V_o=V_{OH}} \frac{dV_o}{C} = \int_0^{V_{OH}} \frac{dV_o}{\frac{C \cdot dV_o}{dt}}$$

$$\int_0^{V_{IL} + |V_{thp}|} \frac{dV_o}{\frac{C \cdot dV_o}{dt}} + \int_{V_{IL} + |V_{thp}|}^{V_{IL} + |V_{thp}| + V_{thp}} \frac{dV_o}{\frac{C \cdot dV_o}{dt}}$$

$\overset{V_o \leq V_{IL} + |V_{thp}|}{\text{Saturation Region}}$ $\overset{V_o > V_{IL} + |V_{thp}|}{\text{Intrinsic Region}}$

$$I_{dp_{sat}} = \frac{V_{IL} + |V_{thp}|}{\frac{C \cdot dV_o}{dt_{sat}}} + \frac{V_{IL} + |V_{thp}| + V_{thp}}{\frac{C \cdot dV_o}{dt_{in}}}$$

$$I_{dp_{sat}} = \frac{1}{C} k_p \left[V_{SG} - |V_{thp}| \right]^2$$

$$I_{dp_{in}} = \frac{1}{C} k_p \left[2[V_{SG} - |V_{thp}|] V_{SD} - V_{SD}^2 \right]$$

We know

$$V_{SG} = V_{DD} - V_{IL}$$

$$V_{SD} = V_{DD} - V_{out}$$

Solving ①,

$$\text{def } \chi = \int_0^{V_{IL} + |V_{thp}|} \frac{dV_o}{I_{load}} = \int \frac{\frac{V_{IL} + |V_{thp}|}{K_p}}{\frac{1}{2} \left[V_{DD} - V_{IL} - |V_{thp}| \right]^2}$$

$$\chi = \int \frac{\frac{dV_{out}}{I_{load}}}{\frac{K_p}{2} \left[V_{DD} - V_{IL} - |V_{thp}| \right]^2}$$

$$\chi = \frac{1}{K_p} \left[\frac{V_{out}}{\left[V_{DD} - V_{IL} - |V_{thp}| \right]^2} \right]^{V_{IL} + |V_{thp}|}$$

$$\chi = \frac{1}{K_p} \left[\frac{V_{out}}{\left[V_{DD} - V_{IL} - |V_{thp}| \right]^2} \right]$$

Solving ②

$$Y = \int \frac{dV_{out}}{I_{load} \cdot R_{series}}$$

$$Y = \int \frac{dV_{out}}{\frac{K_p}{2} \left[\left(V_{DD} - V_{IL} - |V_{thp}| \right) V_{DD} - V_{DD}^2 \right]}$$

$$Y = \frac{1}{K_p} \int \frac{dV_{out}}{\frac{1}{2} \left[\left(V_{DD} - V_{IL} - |V_{thp}| \right) \left(V_{DD} - V_{out} \right) - \left(V_{DD} - V_{out} \right)^2 \right]}$$

$$Y = \frac{1}{K_p} \left[- \frac{\ln \left[\frac{V_{out} - V_{DD} + \sqrt{V_{DD} - V_{IL} - |V_{thp}|}}{V_{out} - V_{DD}} \right]}{\left[V_{DD} - V_{IL} - |V_{thp}| \right]} \right]^{V_{DD}}$$

$$Y = \left[\frac{\ln \left[\frac{V_{DD} + V_{out} - 2V_{IL} - 2|V_{thp}|}{V_{out} - V_{DD}} \right]}{K_p [V_{DD} - V_{IL} - |V_{thp}|]} \right]^{V_{OH}}$$

$$Y = \frac{\ln \left[\frac{V_{DD} + V_{OH} - 2V_{IL} - 2|V_{thp}|}{V_{OH} - V_{DD}} \right]}{K_p [V_{DD} - V_{IL} - |V_{thp}|]} - \ln \left[\frac{V_{DD} - [V_{IL} + |V_{thp}|]}{V_{IL} + |V_{thp}| - V_{in}} \right]^{V_{OL}=0}$$

$$Y = \frac{\ln \left[\frac{V_{in} + V_{OH} - 2V_{IL} - 2|V_{thp}|}{V_{OH} - V_{in}} \right]}{K_p [V_{in} - V_{IL} - |V_{thp}|]}$$

Combining ① & ④,

$$S_{rise} = CX + CY$$

$$S_{rise} = \frac{\alpha C [V_{IL} + |V_{thp}|]}{K_p [V_{DD} - V_{IL} - |V_{thp}|]^2} + \frac{C}{K_p [V_{DD} - V_{IL} - |V_{thp}|]} \ln \left[\frac{V_{DD} + V_{OH} - 2V_{IL} - 2|V_{thp}|}{V_{DD} - V_{OH}} \right]$$

Saturation Linear

Fall Time:

Calculating Fall-Time (τ_{fall}):

Here PMOS is OFF while NMOS is ON

\Rightarrow Minimum value of voltage to be considered high

$$\tau_{fall} = -C \cdot \frac{dV_{out}}{dt}$$

$$\Rightarrow \int_{V_{DS}}^{V_{I_H} - V_{thn}} \frac{dt}{C} = - \int_{I_{D_{sat}}}^{\frac{dV_{out}}{I_{D_{sat}}}} \frac{dV_{out}}{I_{D_{sat}}}$$

Here for NMOS,

- (1) $V_o \geq V_{I_H} - V_{thn} \rightarrow$ Saturation Region
- (2) $V_o < V_{I_H} - V_{thn} \rightarrow$ Linear Region

$$V_{GS} = V_{I_H}, \quad V_{DS} = V_{out}$$

$$\frac{\tau_{fall}}{C} = - \int_{V_{DS}}^{V_{I_H} - V_{thn}} \frac{dV_o}{I_{D_{sat}}} - \int_{V_{DS}}^{V_{I_H} - V_{thn}} \frac{dV_o}{I_{D_{linear}}}$$

$$\downarrow \quad \quad \quad \downarrow$$

$$I_{D_{sat}} = \frac{K_n}{2} \left[V_{GS} - V_{thn} \right]^2 = \frac{K_n}{2} \left[V_{I_H} - V_{thn} \right]^2$$

$$I_{D_{linear}} = \frac{K_n}{2} \left[2(V_{GS} - V_{thn})(V_{DS}) - (V_{DS})^2 \right]$$

$$= \frac{K_n}{2} \left[2(V_{I_H} - V_{thn})(V_{out}) - (V_{out})^2 \right]$$

Solving ①,

$$\text{Let } \chi = \int_{V_{DD}}^{V_I + V_{th}} \frac{dV_{out}}{\frac{k_n}{2} [V_{IH} - V_{th}]^2}$$

$$\chi = \frac{2}{k_n [V_{IH} - V_{th}]^2} \left[\frac{V_{out}}{V_{DD}} \right]^{V_I + V_{th}}$$

$$\chi = \frac{2[V_{IH} + V_{th} - V_{DD}]}{k_n [V_{IH} - V_{th}]^2}$$

Solving ②,

$$Y = \int_{V_I - V_{th}}^{V_{OL}} \frac{dV_{out}}{\frac{k_n}{2} [2(V_{IH} - V_{th}) (V_{out}) - (V_{out})^2]}$$

$$Y = \frac{2}{k_n} \left[\frac{\ln \left[\frac{V_{out}}{V_{OL} - 2(V_{IH} - V_{th})} \right]}{2(V_{IH} - V_{th})} \right]^{V_{OL}}$$

$$Y = \frac{1}{k_n (V_{IH} - V_{th})} \left[\ln \left[\frac{V_{OL}}{V_{OL} - 2(V_{IH} - V_{th})} \right] - \ln \left[\frac{V_{IH} - V_{th}}{V_{IH} - V_{th}} \right] \right]$$

$$Y = \frac{1}{k_n (V_{IH} - V_{th})} \ln \left[\frac{V_{OL}}{V_{OL} - 2(V_{IH} - V_{th})} \right]$$

Combining both,

$$\frac{S_{full}}{C} = -\chi - Y$$

$$T_{full} = \frac{2C [V_{DD} - V_{IH} - V_{th}]}{k_n [V_{IH} - V_{th}]^2} + \frac{C}{k_n [V_{IH} - V_{th}]} \ln \left[\frac{V_{th} - 2(V_{IH} - V_{th})}{V_{OL}} \right]$$

Calculation of $K_p \tau_{rise}/C_l$ and $K_n \tau_{fall}/C_l$:

Calculating $\frac{K_p S_{rise}}{C}$,

$$\frac{K_p S_{rise}}{C} = \frac{2[V_{IL} + |V_{thp}|]}{[V_{DD} - V_{IL} - |V_{thp}|]^2} + \frac{1}{[V_{DD} - V_{IL} - |V_{thp}|]} \ln \left[\frac{\frac{V_{DD} + V_{on} - 2|V_{thp}|}{V_{DD} - V_{on}}}{\frac{V_{DD} + V_{on} - 2|V_{thp}|}{V_{DD} - V_{on}}} \right]$$

$$RHS = \frac{2[0.759 + 0.48]}{[1.8 - 0.759 - 0.48]^2} + \frac{1}{[1.8 - 0.759 - 0.48]} \ln \left[\frac{1.8 + \frac{1.68}{0.561} - 2[0.749 + 0.48]}{1.8 - 1.687} \right]$$

$$RHS = \frac{2 \cdot 478}{(0.561)^2} + \frac{1}{(0.561)} \ln \left[\frac{8.429}{1} \right]$$

$$RHS = 7.874 + \frac{2.189}{0.561} = 7.874 + 3.902 = 11.775$$

$$\boxed{\frac{K_p S_{rise}}{C} = 11.775}$$

Calculating $\frac{K_n S_{fall}}{C}$

$$\frac{K_n S_{fall}}{C} = \frac{2[V_{DD} - V_{IH} - V_{thn}]}{[V_{IH} - V_{thn}]^2} + \frac{1}{[V_{IH} - V_{thn}]} \ln \left[\frac{V_{th} + 2V_{th} - 2V_{IH}}{V_{DL}} \right]$$

$$RHS = \frac{2[1.8 - 1.015 - 0.473]}{[1.015 - 0.473]^2} + \frac{1}{[1.015 - 0.473]} \ln \left[\frac{-0.147}{0.11} \right]$$

$$RHS = \frac{2[0.312]}{[0.542]^2} + \frac{1}{[0.542]} \ln \left[\frac{0.403}{0.11} \right]$$

$$RHS = \frac{2[0.312]}{[0.542]^2} + \frac{1.7014}{0.542} = 5.2633$$

$$Ans = \frac{K_n S_{fall}}{C} = 5.2633$$

(B)

Code:

Question 4 > 4b.cir

```

1 VLSI Assignment Question 4b
2 * Answers to question 4b
3 .include TSMC_180nm.txt
4 .param SUPPLY=1.8
5 .param LAMBDA=0.09u
6 .param width_N1=20*LAMBDA
7 .param width_P1=2.5*width_N1
8
9 .param width_N2=4*width_N1
10 .param width_P2=2.5*width_N2
11
12 .param width_N3=16*width_N1
13 .param width_P3=2.5*width_N3
14
15 .param width_N4=64*width_N1
16 .param width_P4=2.5*width_N4
17
18 .param width_N5=376*width_N1
19 .param width_P5=2.5*width_N5
20 .global gnd vdd
21
22 Vdd vdd gnd 1.8V
23 vin a pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)
24
25 * First Inverter
26 M1 b a gnd gnd CMOSN W=(width_N1) L=(2*LAMBDA)
27 + AS=(5*width_N1*LAMBDA) PS=(10*LAMBDA+2*width_N1) AD=(5*width_N1*LAMBDA) PD=(10*LAMBDA+2*width_N1)
28
29 M2 b a vdd vdd CMOSP W=(width_P1) L=(2*LAMBDA)
30 + AS=(5*width_P1*LAMBDA) PS=(10*LAMBDA+2*width_P1) AD=(5*width_P1*LAMBDA) PD=(10*LAMBDA+2*width_P1)
31 * Second Inverter
32 M3 c b gnd gnd CMOSN W=(width_N2) L=(2*LAMBDA)
33 + AS=(5*width_N2*LAMBDA) PS=(10*LAMBDA+2*width_N2) AD=(5*width_N2*LAMBDA) PD=(10*LAMBDA+2*width_N2)
34
35 M4 c b vdd vdd CMOSP W=(width_P2) L=(2*LAMBDA)
36 + AS=(5*width_P2*LAMBDA) PS=(10*LAMBDA+2*width_P2) AD=(5*width_P2*LAMBDA) PD=(10*LAMBDA+2*width_P2)
37
38 * Third Inverter
39 M5 d c gnd gnd CMOSN W=(width_N3) L=(2*LAMBDA)
40 + AS=(5*width_N3*LAMBDA) PS=(10*LAMBDA+2*width_N3) AD=(5*width_N3*LAMBDA) PD=(10*LAMBDA+2*width_N3)
41
42 M6 d c vdd vdd CMOSP W=(width_P3) L=(2*LAMBDA)
43 + AS=(5*width_P3*LAMBDA) PS=(10*LAMBDA+2*width_P3) AD=(5*width_P3*LAMBDA) PD=(10*LAMBDA+2*width_P3)
44
45 * Fourth Inverter
46 M7 e d gnd gnd CMOSN W=(width_N4) L=(2*LAMBDA)
47 + AS=(5*width_N4*LAMBDA) PS=(10*LAMBDA+2*width_N4) AD=(5*width_N4*LAMBDA) PD=(10*LAMBDA+2*width_N4)
48
49 M8 e d vdd vdd CMOSP W=(width_P4) L=(2*LAMBDA)
50 + AS=(5*width_P4*LAMBDA) PS=(10*LAMBDA+2*width_P4) AD=(5*width_P4*LAMBDA) PD=(10*LAMBDA+2*width_P4)
51

```

Question 4 > 4b.cir

```

51 * Fifth Inverter
52 M9 f e gnd gnd CMOSN W=(width_N5) L=(2*LAMBDA)
53 + AS=(5*width_N5*LAMBDA) PS=(10*LAMBDA+2*width_N5) AD=(5*width_N5*LAMBDA) PD=(10*LAMBDA+2*width_N5)
54
55 M10 f e vdd vdd CMOSP W=(width_P5) L=(2*LAMBDA)
56 + AS=(5*width_P5*LAMBDA) PS=(10*LAMBDA+2*width_P5) AD=(5*width_P5*LAMBDA) PD=(10*LAMBDA+2*width_P5)
57
58
59
60 Cout f gnd lpf
61 .tran 10p 5n
62
63
64 ** MEASURING DELAYS (Refer manual section 15.4.5)
65 *'13
66 .measure tran tpdrC
67 + TRIG v(d) VAL=0.18 RISE=1
68 + TARG v(d) VAL=1.62 RISE=1
69
70 .measure tran tpdfC
71 + TRIG v(d) VAL=1.62 FALL=1
72 + TARG v(d) VAL=0.18 FALL=1
73
74 * .measure tran tpdrC param='(tpdrC+tpdfC)/2' goal=0
75 * .measure tran diffC param='tpdrC-tpdfC' goal=0
76
77 *'14
78 .measure tran tpdrD
79 + TRIG v(e) VAL=0.18 RISE=1
80 + TARG v(e) VAL=1.62 RISE=1
81
82 .measure tran tpdfD
83 + TRIG v(e) VAL=1.62 FALL=1
84 + TARG v(e) VAL=0.18 FALL=1
85
86 * .measure tran tpd param='(tpdrD+tpdfD)/2' goal=0
87 * .measure tran diff param='tpdrD-tpdfD' goal=0
88
89
90
91 .control
92 set hcopiescolor = 1 "White background for saving plots
93 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7))
94 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7))
95
96 run
97 set curplottitle="AravindNarayanan-2019102814-04-b"
98 plot v(c) v(d)
99 hardcopy fig_4b.eps v(c) v(d)
100 .endc
101

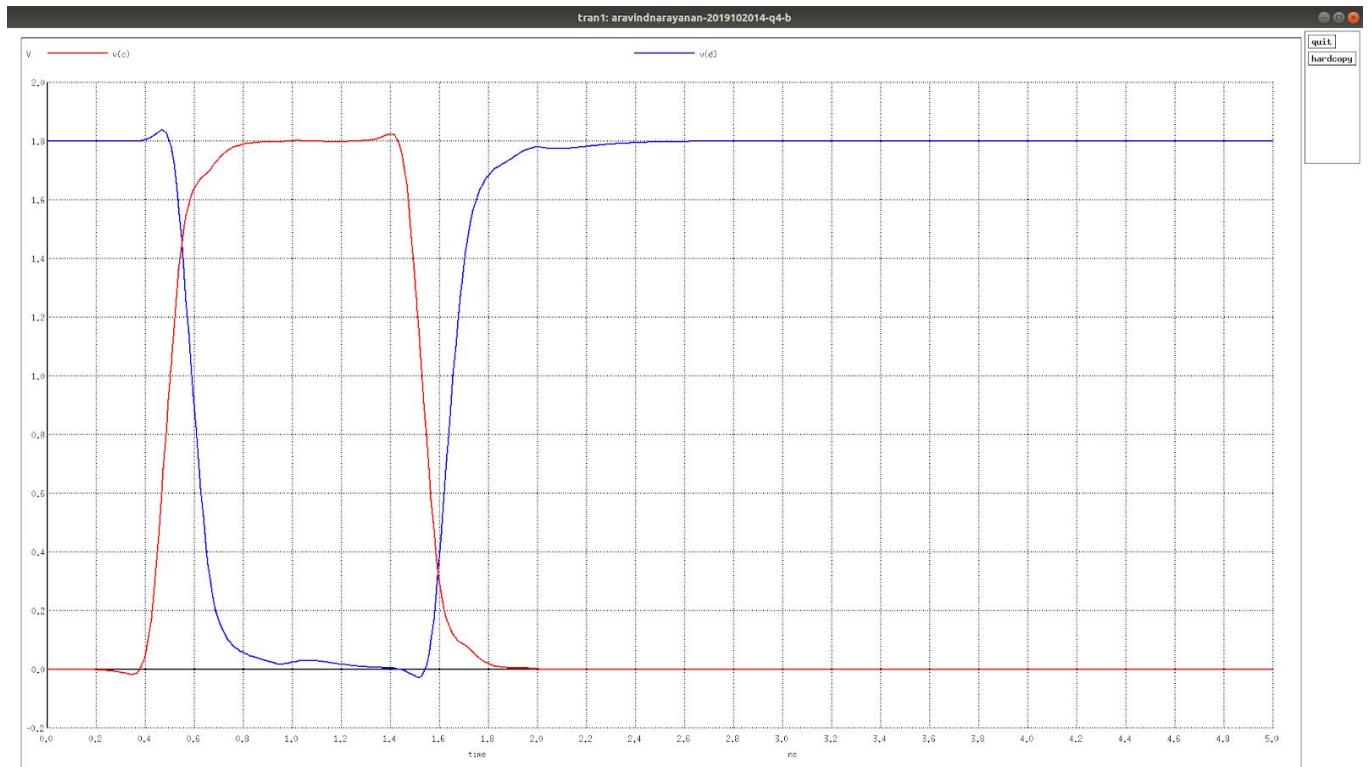
```

Code for 4b

| | |

Continuation

Figure:



Pre Layout Values:

NODE	$\tau_{rise\ 10\%}$	$\tau_{rise\ 90\%}$	$\tau_{rise} = \tau_{rise\ 90\%} - \tau_{rise\ 10\%}$
C	0.4235ns	0.5886ns	0.1651ns
D	1.5761ns	1.75645ns	0.1803ns
	$\tau_{fall\ 90\%}$	$\tau_{fall\ 10\%}$	$\tau_{fall} = \tau_{fall\ 90\%} - \tau_{fall\ 10\%}$
C	1.46891ns	1.62516ns	0.15625ns
D	0.5295ns	0.693521ns	0.1640ns

Observations:

- We see that the Rise time for both node C and D, Fall time for both C and D are **not equal** to each other. In fact we see that both the rise and fall time is **more for node D than node C**.
- An inverter can be thought of as an RC equivalent if the output of a CMOS inverter is another CMOS inverter. So for the case of node C, the output load is significantly lower than the output capacitive load for node D as output of node C drives an inverter load of 64W while node D drives the inverter of load 376W.
- Hence this delay can be attributed to the increase in width in turn increasing out output load leading to higher rise and fall times for node D than node C.

(C)

Code:

```
Question 4 > 4ccir
1 | VLSI Assignment Question 4c
2 | * Answers to question 4c
3 | .include TSMC 180nm.txt
4 | .param SUPPLY=1.8
5 | .param LAMBDA=0.09u
6 | * First Inverter
7 | .param width_N1=20*LAMBDA
8 | .param width_P1=2.5*width_N1
9 | * Second Inverter
10 | .param width_N2=4*width_N1
11 | .param width_P2=2.5*width_N2
12 | * Third Inverter
13 | .param width_N3=16*width_N1
14 | .param width_P3=2.5*width_N3
15 | * Fourth Inverter
16 | .param width_N4=64*width_N1
17 | .param width_P4=2.5*width_N4
18 | * Fifth Inverter
19 | .param width_N5=376*width_N1
20 | .param width_P5=2.5*width_N5
21 | global gnd vdd
22 |
23 | Vdd vdd gnd 1.8V
24 | Vin a 0 pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)
25 |
26 | * First Inverter
27 | M1 b a gnd gnd CMOSN W=(width_N1) L=(2*LAMBDA)
28 | + AS=(5*width_N1*LAMBDA) PS=(10*LAMBDA+2*width_N1) AD=(5*width_N1*LAMBDA) PD=(10*LAMBDA+2*width_N1)
29 |
30 | M2 b a vdd vdd CMOSP W=(width_P1) L=(2*LAMBDA)
31 | + AS=(5*width_P1*LAMBDA) PS=(10*LAMBDA+2*width_P1) AD=(5*width_P1*LAMBDA) PD=(10*LAMBDA+2*width_P1)
32 | * Second Inverter
33 | M3 c b gnd gnd CMOSN W=(width_N2) L=(2*LAMBDA)
34 | + AS=(5*width_N2*LAMBDA) PS=(10*LAMBDA+2*width_N2) AD=(5*width_N2*LAMBDA) PD=(10*LAMBDA+2*width_N2)
35 |
36 | M4 c b vdd vdd CMOSP W=(width_P2) L=(2*LAMBDA)
37 | + AS=(5*width_P2*LAMBDA) PS=(10*LAMBDA+2*width_P2) AD=(5*width_P2*LAMBDA) PD=(10*LAMBDA+2*width_P2)
38 |
39 | * Third Inverter
40 | M5 d c gnd gnd CMOSN W=(width_N3) L=(2*LAMBDA)
41 | + AS=(5*width_N3*LAMBDA) PS=(10*LAMBDA+2*width_N3) AD=(5*width_N3*LAMBDA) PD=(10*LAMBDA+2*width_N3)
42 |
43 | M6 d c vdd vdd CMOSP W=(width_P3) L=(2*LAMBDA)
44 | + AS=(5*width_P3*LAMBDA) PS=(10*LAMBDA+2*width_P3) AD=(5*width_P3*LAMBDA) PD=(10*LAMBDA+2*width_P3)
45 |
46 | * Fourth Inverter
47 | M7 e d gnd gnd CMOSN W=(width_N4) L=(2*LAMBDA)
48 | + AS=(5*width_N4*LAMBDA) PS=(10*LAMBDA+2*width_N4) AD=(5*width_N4*LAMBDA) PD=(10*LAMBDA+2*width_N4)
49 |
50 | M8 e d vdd vdd CMOSP W=(width_P4) L=(2*LAMBDA)
51 | + AS=(5*width_P4*LAMBDA) PS=(10*LAMBDA+2*width_P4) AD=(5*width_P4*LAMBDA) PD=(10*LAMBDA+2*width_P4)

Question 4 > 4ccir
52 | * Fifth Inverter
53 | M9 f e gnd gnd CMOSN W=(width_N5) L=(2*LAMBDA)
54 | + AS=(5*width_N5*LAMBDA) PS=(10*LAMBDA+2*width_N5) AD=(5*width_N5*LAMBDA) PD=(10*LAMBDA+2*width_N5)
55 |
56 | M10 f e vdd vdd CMOSP W=(width_P5) L=(2*LAMBDA)
57 | + AS=(5*width_P5*LAMBDA) PS=(10*LAMBDA+2*width_P5) AD=(5*width_P5*LAMBDA) PD=(10*LAMBDA+2*width_P5)
58 |
59 |
60 |
61 | Cout f gnd lpf
62 | .tran 10p 5n
63 |
64 |
65 | ** MEASURING DELAYS
66 | * Node C
67 | .measure tran tpdrC
68 | + TRIG v(c) VAL='SUPPLY/2' RISE=1
69 | + TARG v(d) VAL='SUPPLY/2' FALL=1
70 |
71 | .measure tran tpdfC
72 | + TRIG v(c) VAL='SUPPLY/2' RISE=1
73 | + TARG v(d) VAL='SUPPLY/2' FALL=1
74 |
75 | .measure tran tpdfD param='(tpdrC+tpdfC)/2' goal=0
76 |
77 | * Node D
78 | .measure tran tpdrD
79 | + TRIG v(d) VAL='SUPPLY/2' RISE=1
80 | + TARG v(e) VAL='SUPPLY/2' FALL=1
81 |
82 | .measure tran tpdfD
83 | + TRIG v(d) VAL='SUPPLY/2' RISE=1
84 | + TARG v(e) VAL='SUPPLY/2' FALL=1
85 |
86 | .measure tran tpdrD param='(tpdrD+tpdfD)/2' goal=0
87 |
88 | .control
89 | set hcopyright = 1 /*White background for saving plots
90 | set color0=white ** color0 is used to set the background of the plot ([manual sec:17.7])
91 | set color1=black ** color1 is used to set the grid color of the plot ([manual sec:17.7])
92 | run
93 | plot v(c) v(d) v(e)
94 | hardcopy fig_Q4c.eps v(c) v(d) v(e)
95 | .endc
96 |
97 |
98 |
99 |
```

Propagation Delay Table:

NODE	τ_{rise}	τ_{fall}	$\tau_{pgd} = (\tau_{fall} + \tau_{rise})/2$
C	0.1092809ns	0.1068939ns	0.108087ns
D	0.1845302ns	0.1649294ns	0.174730ns

Observation:

- We observe that both the delays are not the same. The delay in node D is more than the delay of node C. This can be attributed to the increase in the fan-out in the circuit between node C,D and node D,E. The fanout-width of I4 is 64W while I3 is only 16W.
- So we can say that an increase in fanout is directly affecting propagation delay proportionately i.e degrades the transient response. This proportionality comes as the output of I3 is connected to a load(I4) which has a significantly less load than output of I4.
- As load is more in case of node D, the response is also slower resulting in more delay.
- This is also why we should avoid using large fanout structures if we want to improve the performance of a circuit.

(D)

Netlist:

Combined Netlist for (D) and (E):

```
VLSI Assignment Question 4d
* Answers to question 4d
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
* First Inverter
.param width_N1=20*LAMBDA
.param width_P1=2.5*width_N1
* Second Inverter
.param width_N2=4*width_N1
.param width_P2=2.5*width_N2
* Third Inverter
.param width_N3=16*width_N1
.param width_P3=2.5*width_N3
* Fourth Inverter
.param width_N4=64*width_N1
.param width_P4=2.5*width_N4
* Fifth Inverter
.param width_N5=376*width_N1
.param width_P5=2.5*width_N5
.global gnd vdd

Vdd vdd gnd 1.8V
vin a 0 pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)
VDSP sP gnd 1.8V
VDSN sN gnd 0V
* First Inverter
M1 b a gnd gnd CMOSN W={width_N1} L={2*LAMBDA}
+ AS={5*width_N1*LAMBDA} PS={10*LAMBDA+2*width_N1} AD={5*width_N1*LAMBDA} PD={10*LAMBDA+2*width_N1}

M2 b a vdd vdd CMOSP W={width_P1} L={2*LAMBDA}
+ AS={5*width_P1*LAMBDA} PS={10*LAMBDA+2*width_P1} AD={5*width_P1*LAMBDA} PD={10*LAMBDA+2*width_P1}
* Second Inverter
M3 c b gnd gnd CMOSN W={width_N2} L={2*LAMBDA}
+ AS={5*width_N2*LAMBDA} PS={10*LAMBDA+2*width_N2} AD={5*width_N2*LAMBDA} PD={10*LAMBDA+2*width_N2}

M4 c b vdd vdd CMOSP W={width_P2} L={2*LAMBDA}
+ AS={5*width_P2*LAMBDA} PS={10*LAMBDA+2*width_P2} AD={5*width_P2*LAMBDA} PD={10*LAMBDA+2*width_P2}

* Third Inverter
M5 d c sN sN CMOSN W={width_N3} L={2*LAMBDA}
+ AS={5*width_N3*LAMBDA} PS={10*LAMBDA+2*width_N3} AD={5*width_N3*LAMBDA} PD={10*LAMBDA+2*width_N3}

M6 d c sP sP CMOSP W={width_P3} L={2*LAMBDA}
+ AS={5*width_P3*LAMBDA} PS={10*LAMBDA+2*width_P3} AD={5*width_P3*LAMBDA} PD={10*LAMBDA+2*width_P3}

* Fourth Inverter
M7 e d gnd gnd CMOSN W={width_N4} L={2*LAMBDA}
+ AS={5*width_N4*LAMBDA} PS={10*LAMBDA+2*width_N4} AD={5*width_N4*LAMBDA} PD={10*LAMBDA+2*width_N4}

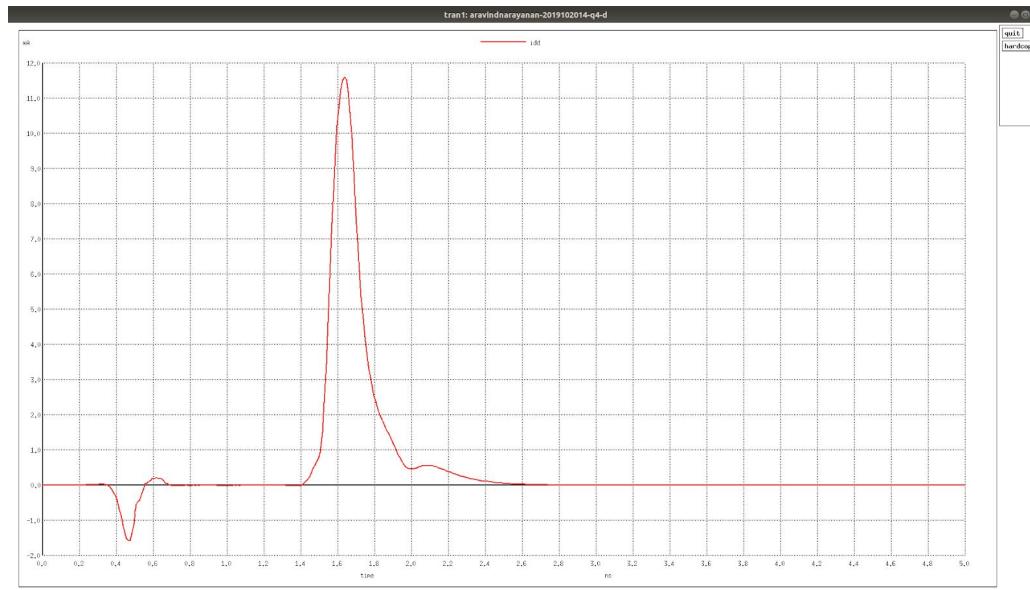
M8 e d vdd vdd CMOSP W={width_P4} L={2*LAMBDA}
+ AS={5*width_P4*LAMBDA} PS={10*LAMBDA+2*width_P4} AD={5*width_P4*LAMBDA} PD={10*LAMBDA+2*width_P4}

* Fifth Inverter
M9 f e gnd gnd CMOSN W={width_N5} L={2*LAMBDA}
+ AS={5*width_N5*LAMBDA} PS={10*LAMBDA+2*width_N5} AD={5*width_N5*LAMBDA} PD={10*LAMBDA+2*width_N5}

M10 f e vdd vdd CMOSP W={width_P5} L={2*LAMBDA}
+ AS={5*width_P5*LAMBDA} PS={10*LAMBDA+2*width_P5} AD={5*width_P5*LAMBDA} PD={10*LAMBDA+2*width_P5}
```

```
62 Cout f gnd 1pf
63 .tran 10p 5n
64
65
66
67 .control
68 set hcopypscolor = 1 *White background for saving plots
69 set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
70 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
71 run
72 set curplottitle="AravindNarayanan-2019102014-Q4-d&e"
73 let IDD = (-VDSP#branch)
74 let ISS = (VDSN#branch)
75 plot IDD
76 plot ISS
77 plot v(c) v(d)
78 hardcopy fig_Q4c.eps IDD ISS v(c) v(d)
79 .endc
```

Figure:



Explanation:

We see that when we compare the $v(C)$, $v(D)$'s graph with this IDD graph, we notice that the current becomes maximum when the node D's voltage goes from 0 to 1.8V while node C's voltage simultaneously goes from 1.8V to 0V. This is because the **current mainly flows only when the switching action** takes place. This means that the current flow for IDD is when both the NMOS and PMOS are in saturation region,

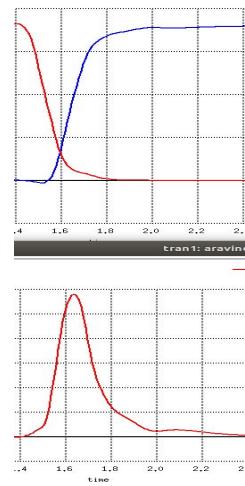


Fig. A zoomed in version of $V(c), V(d)$ on the top and i_{DD} on the bottom to show the effect of switching

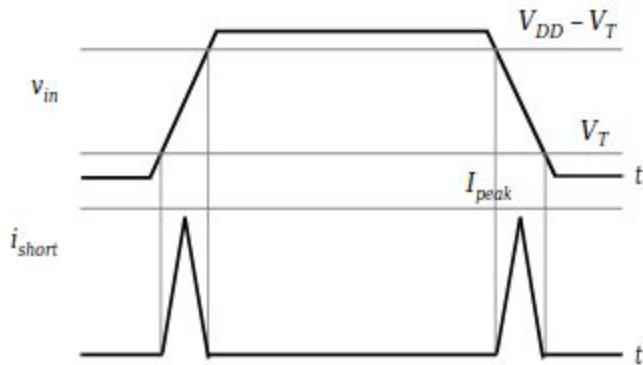
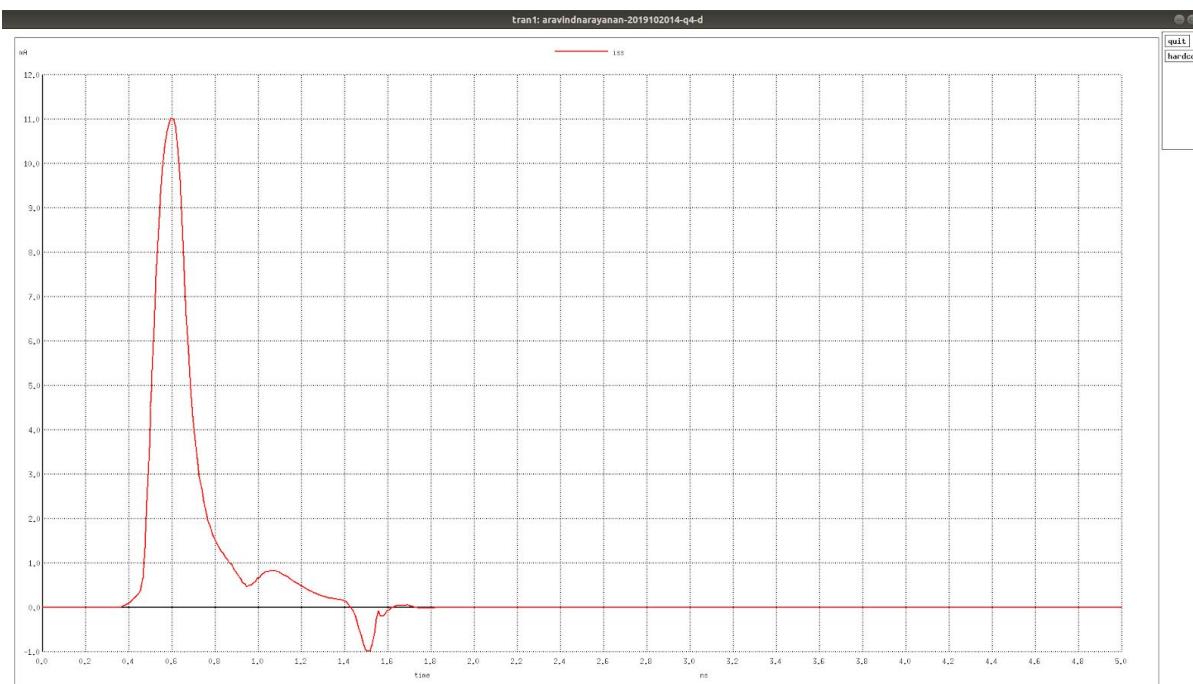


Fig. Sample of effect of current with input voltage(the left side spike is for ISS while write side for ISS)

Initially, the IDD goes negative which is possible when the drain voltage of PMOS > VDD(1.8V). Then the decrease in current is due to the shifting of the PMOS outside the saturation region. At this point we also notice V(D) goes towards the maximum due to which the currents goes down to zero.

(E)

Figure:



Explanation:

- The graph for ISS can be explained the similar way as done in the case of IDD. It is complementary to the IDD current graph. But the method remains the same.
- Both the PMOS and NMOS are in saturation region during the switching action which is also when the ISS increases to a maximum till the NMOS goes to linear stage (and) PMOS goes to the cutoff region.
- The current tends to zero after that until there's a small negative drop in the current which is due to the leakage currents and gate capacitances.

Why do IDD and ISS look complementary (by complementary, it refers to the opposite behaviour of the currents at two different time intervals) ?

- When we calculated the rise and fall time, we made a general assumption that only one of the mosfets are ON at a time theoretically.
- Following this assumption, when node C voltage rises from 0 to Vdd only the PMOS is ON which is why we observe a spike in the ISS while IDD is slightly negative due to the

leakage current in the opposite direction.

- Similarly, when node C voltage falls to 0 from Vdd only the NMOS is ON which is why we observe a spike in the IDD while ISS is slightly negative due to the leakage current in the opposite direction.

So, we can say that the theoretical assumption used to calculate rise and fall time also holds here.

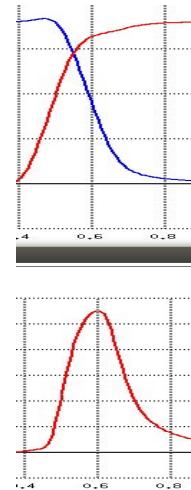


Fig. A zoomed in version of $V(c), V(d)$ on the top and ISS on the bottom to show the effect of switching

Question 5

(A)

Circuit:

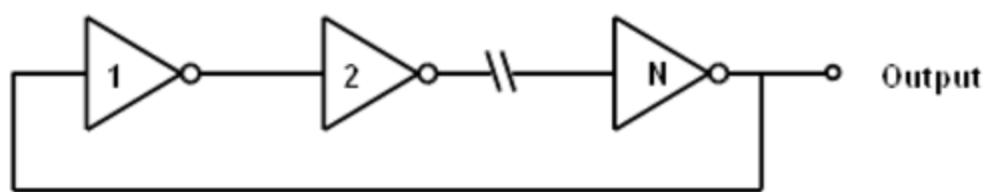


Fig: n-Stage Ring Oscillator

A n-stage ring oscillator is a device composed of an odd number of CMOS Inverters in a ring,

whose output oscillates between two voltage levels, representing SUPPLY(1.8V) and GND(0V). The inverters are attached in a chain and the output of the last inverter is fed back into the first.

The delay for the n-stage oscillator is given by:

$$f = \frac{1}{2n\tau_d}$$

where f = frequency of n-stage oscillator, n = number of stages, τ_d = delay of single CMOS inverter.

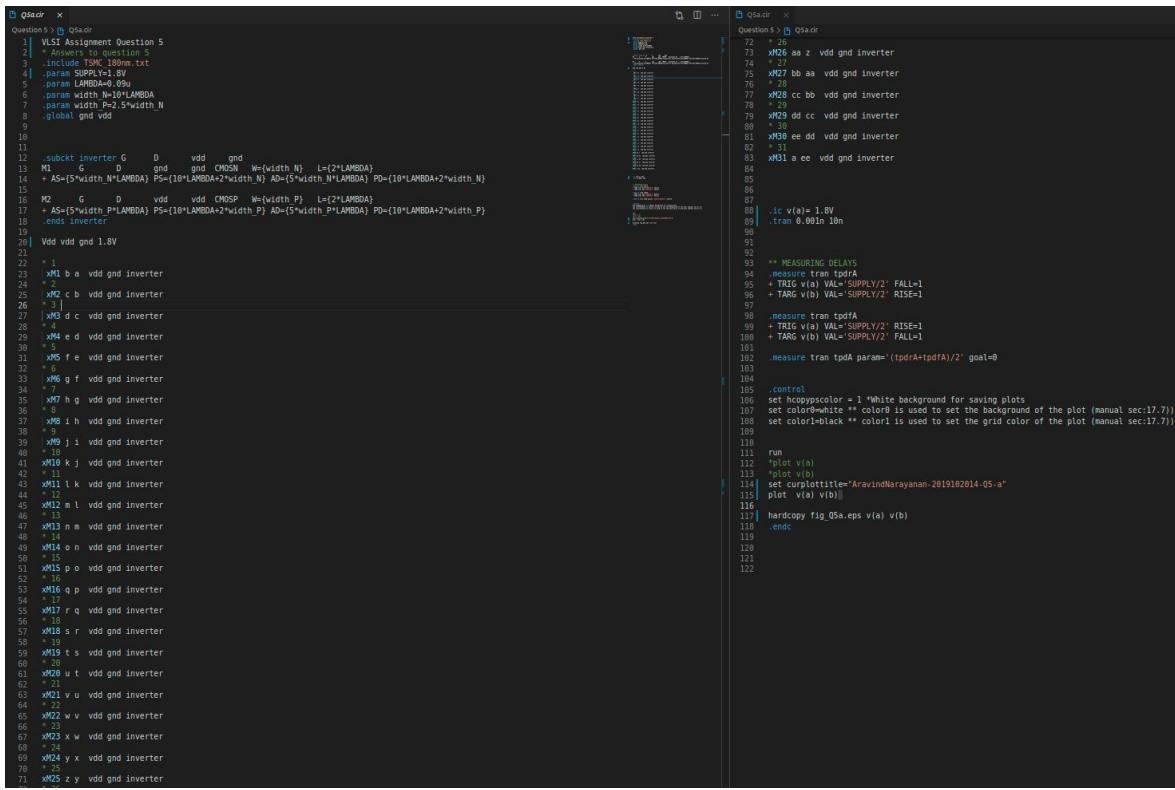
In this question $n = 31$, so the frequency of the inverter is:

$$f = \frac{1}{62\tau_d}$$

Parameters:

- $\lambda = 0.09 \mu m$
- Length of PMOS = Length of NMOS = 2λ
- Width of NMOS = $W_n = 10\lambda$
- Width of PMOS = $W_n = 25\lambda$

Netlist:

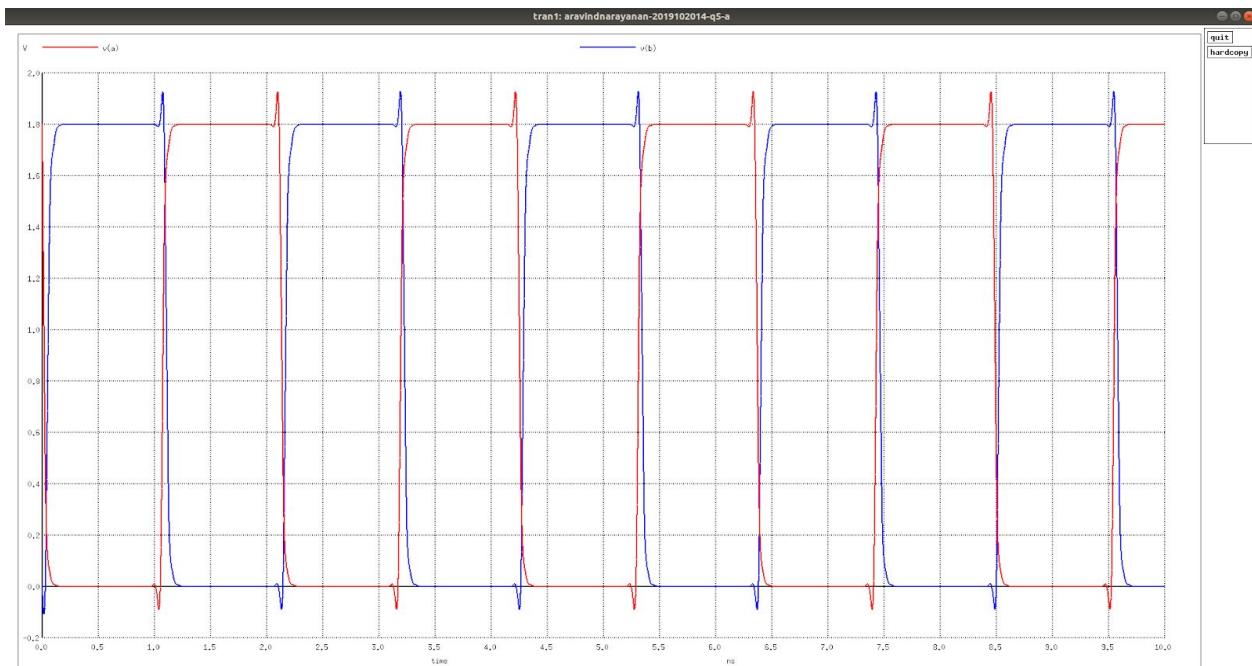


```

QSim > QSim
Question 5 > QSim
1 VLSI Assignment Question 5
2 * Answers to question 5
3 * File name: q5a.v
4 .param SUPPLY=1.8V
5 .param LAMBDA=0.09u
6 .param width_N=10*LAMBDA
7 .param width_P=2.5*width_N
8 .global gnd vdd
9
10
11
12 .subckt inverter G D vdd gnd
13 M1 G D gnd gnd CMOSN W=(width_N) L=(2*LAMBDA)
14 + AS=(5*width_N*LAMBDA) PS=(10*LAMBDA+2*width_N) AD=(5*width_N*LAMBDA) PD=(10*LAMBDA+2*width_N)
15
16 M2 G D vdd vdd CMOSP W=(width_P) L=(2*LAMBDA)
17 + AS=(5*width_P*LAMBDA) PS=(10*LAMBDA+2*width_P) AD=(5*width_P*LAMBDA) PD=(10*LAMBDA+2*width_P)
18 .ends inverter
19
20 Vdd vdd gnd 1.8V
21
22 * 1
23 xM1 b a vdd gnd inverter
24 * 2
25 xM2 c b vdd gnd inverter
26 | M3 | vdd gnd inverter
27 | M4 d c vdd gnd inverter
28 * 4
29 xM4 e d vdd gnd inverter
30
31 xM5 f e vdd gnd inverter
32 * 6
33 xM6 g f vdd gnd inverter
34
35 xM7 h g vdd gnd inverter
36 * 8
37 xM8 i h vdd gnd inverter
38
39 xM9 j i vdd gnd inverter
40 * 10
41 xM10 k j vdd gnd inverter
42
43 xM11 l k vdd gnd inverter
44 * 12
45 xM12 m l vdd gnd inverter
46
47 xM13 n m vdd gnd inverter
48 * 14
49 xM14 o n vdd gnd inverter
50
51 xM15 p o vdd gnd inverter
52 * 16
53 xM16 q p vdd gnd inverter
54
55 xM17 r q vdd gnd inverter
56 * 18
57 xM18 s r vdd gnd inverter
58
59 xM19 t s vdd gnd inverter
60 * 20
61 xM20 u t vdd gnd inverter
62
63 xM21 v u vdd gnd inverter
64 * 22
65 xM22 w v vdd gnd inverter
66
67 xM23 x w vdd gnd inverter
68 * 24
69 xM24 y x vdd gnd inverter
70
71 xM25 z y vdd gnd inverter

```

Figure:



Observations Table:

Sno.	Cases	Rise Time(τ_{rise})	Fall Time(τ_{fall})	$\tau_{pd} = (\tau_{rise} + \tau_{fall})/2$	Frequency($1/(\tau_{rise} + \tau_{fall})$)
1	1-stage	13.08543ps	14.66467ps	13.8750ps	36.036GHz
2	31-stage	33.36732ps	34.68365ps	34.0255ps	0.47GHz

Now that we have found the frequency of oscillation, delay of single inverter and 31 stage ring oscillator, we verify if the formula is in agreement with the simulated values.

VERIFICATION:

$$f_{RO_1} = \frac{1}{2\tau_{d_1}}$$

$$f_{RO_2} = \frac{1}{62\tau_{d_2}}$$

From the table taking ratios of both,

$$\text{LHS} = \frac{f_{ro_2}}{f_{ro_1}} = 0.013$$

$$\text{RHS} = \frac{2\tau_{d_1}}{62\tau_{d_2}} = 0.013$$

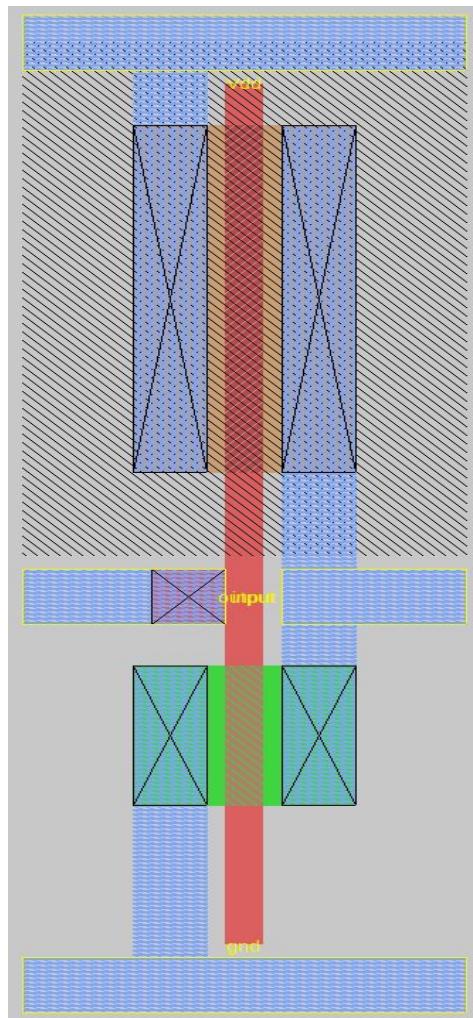
CONCLUSION:

The formula to find the frequency of oscillations holds true for a n-stage oscillator as the ratios above are equal. This shows that if we have the delay for a single inverter. We can directly estimate the frequency of oscillation of a n-stage ring oscillator.

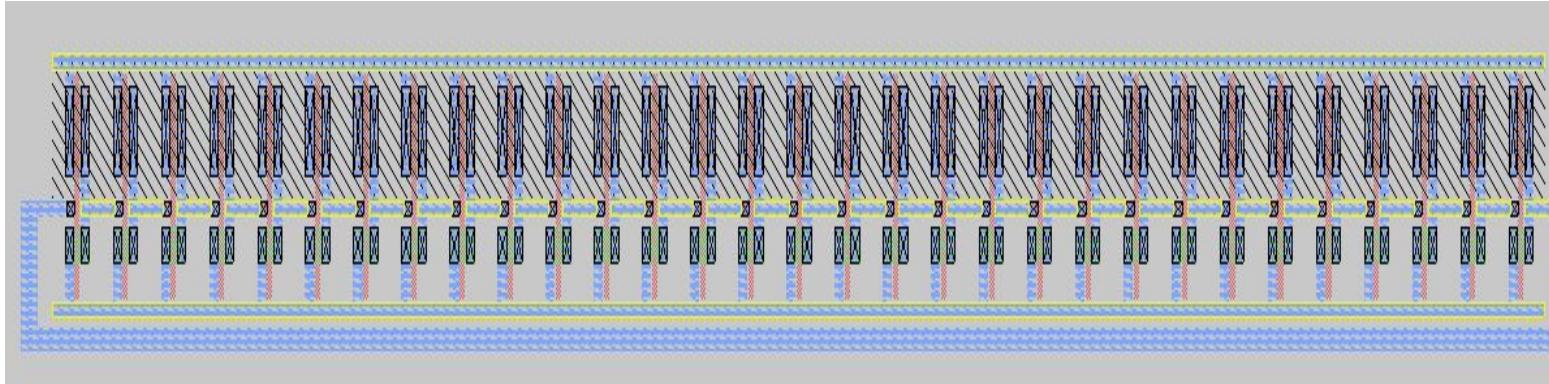
(B)

Layout:

(I) Single Inverter



(II) Unoptimised 31-stage inverter



(III) Optimised 31-stage inverter

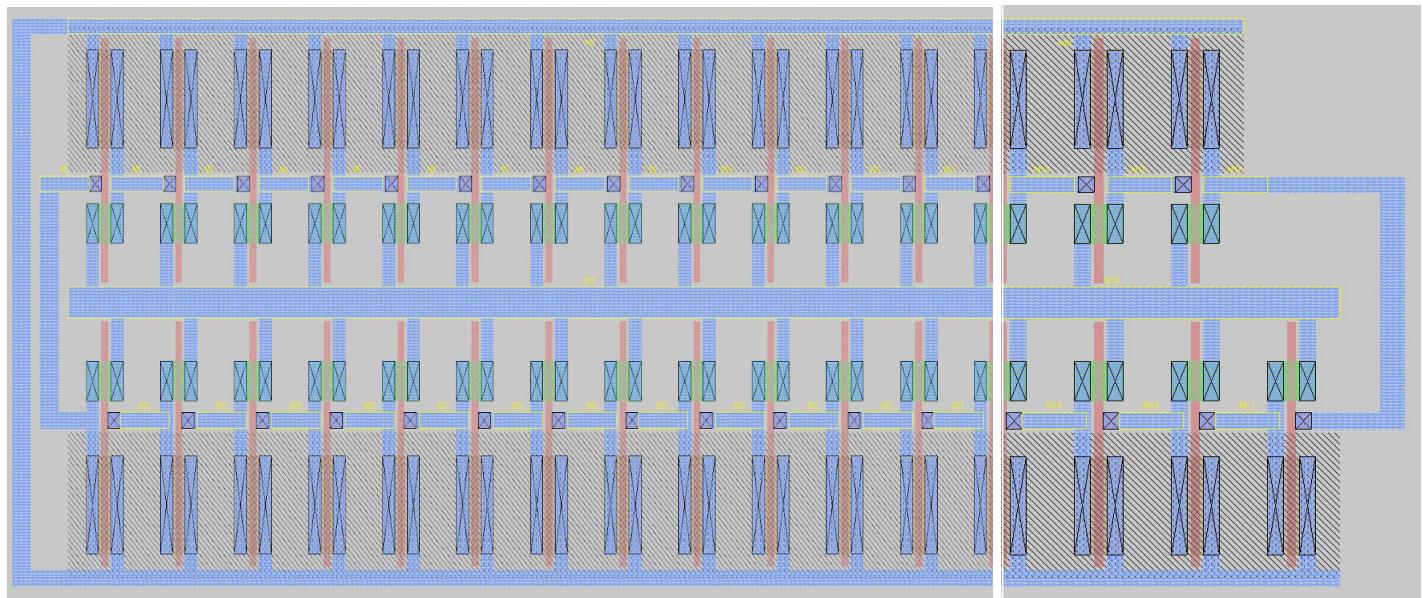


Fig: Optimised 31-stage ring oscillator

(C)

Netlist:



```

Magic Answers > Ring Oscillator > POST_new1_optimized_ring_oscillator.cir
1 * SPICE3 created from new1_optimized_ring_oscillator.net - technology: scmos
2 .include TSMC_180nm.txt
3 .param SUPPLY=1.8
4 .param LAMBDA=0.09u
5 .global gnd vdd
6 .option scale=0.00u
7 .Vdd vdd gnd SUPPLY
8 .option scale=0.09u
9
10 M0000 M1 M31 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
11 + ad=125 pd=60 as=3875 ps=1860
12 M0001 M1 M31 gnd gnd CMOSN w=10 l=2
13 + ad=50 pd=60 as=1590 ps=93
14 M0002 M2 M28 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
15 + ad=125 pd=60 as=3875 ps=1860
16 M0003 M31 M30 vdd gnd CMOSN w=10 l=2
17 + ad=50 pd=60 as=9 ps=0
18 M0004 M30 M29 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
19 + ad=125 pd=60 as=9 ps=0
20 M0005 M29 M28 gnd gnd CMOSN w=10 l=2
21 + ad=50 pd=60 as=9 ps=0
22 M0006 M28 M29 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
23 + ad=125 pd=60 as=9 ps=0
24 M0007 M29 M28 gnd gnd CMOSN w=10 l=2
25 + ad=50 pd=60 as=9 ps=0
26 M0008 M28 M27 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
27 + ad=125 pd=60 as=9 ps=0
28 M0009 M27 M28 gnd gnd CMOSN w=10 l=2
29 + ad=50 pd=60 as=9 ps=0
30 M0010 M27 M26 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
31 + ad=125 pd=60 as=9 ps=0
32 M0011 M27 M26 gnd gnd CMOSN w=10 l=2
33 + ad=50 pd=60 as=9 ps=0
34 M0012 M26 M25 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
35 + ad=125 pd=60 as=9 ps=0
36 M0013 M25 M26 gnd gnd CMOSN w=10 l=2
37 + ad=50 pd=60 as=9 ps=0
38 M0014 M25 M24 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
39 + ad=125 pd=60 as=9 ps=0
40 M0015 M24 M24 gnd gnd CMOSN w=10 l=2
41 + ad=50 pd=60 as=9 ps=0
42 M0016 M24 M23 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
43 + ad=125 pd=60 as=9 ps=0
44 M0017 M23 M24 gnd gnd CMOSN w=10 l=2
45 + ad=50 pd=60 as=9 ps=0
46 M0018 M23 M22 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
47 + ad=125 pd=60 as=9 ps=0
48 M0019 M22 M22 gnd gnd CMOSN w=10 l=2
49 + ad=50 pd=60 as=9 ps=0
50 M0020 M22 M21 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
51 + ad=125 pd=60 as=9 ps=0
52 M0021 M22 M21 gnd gnd CMOSN w=10 l=2
53 + ad=50 pd=60 as=9 ps=0
54 M0022 M21 M20 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
55 + ad=125 pd=60 as=9 ps=0
56 M0023 M21 M20 gnd gnd CMOSN w=10 l=2
57 + ad=50 pd=60 as=9 ps=0
58 M0024 M20 M19 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
59 + ad=125 pd=60 as=9 ps=0
60 M0025 M20 M19 gnd gnd CMOSN w=10 l=2
61 + ad=50 pd=60 as=9 ps=0
62 M0026 M19 M19 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
63 + ad=125 pd=60 as=9 ps=0
64 M0027 M19 M18 gnd gnd CMOSN w=10 l=2
65 + ad=50 pd=60 as=9 ps=0
66 M0028 M18 M17 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
67 + ad=125 pd=60 as=9 ps=0
68 M0029 M17 M17 gnd gnd CMOSN w=10 l=2
69 + ad=50 pd=60 as=9 ps=0
70 M0030 M17 M16 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
71 + ad=125 pd=60 as=9 ps=0
72 M0031 M16 M16 gnd gnd CMOSN w=10 l=2
73 + ad=50 pd=60 as=9 ps=0
74 M0032 M16 M15 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
75 + ad=125 pd=60 as=9 ps=0
76 M0033 M2 M1 gnd gnd CMOSN w=10 l=2
77 + ad=50 pd=60 as=9 ps=0
78 M0034 M3 M2 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
79 + ad=125 pd=60 as=9 ps=0
80 M0035 M3 M2 gnd gnd CMOSN w=10 l=2
81 + ad=50 pd=60 as=9 ps=0
82 M0036 M3 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
83 + ad=125 pd=60 as=9 ps=0
84 M0037 M4 M3 gnd gnd CMOSN w=10 l=2
85 + ad=50 pd=60 as=9 ps=0
86 M0038 M5 M4 vdd inverter_wo_label_05_1[0]/v_0_0# CMOSP w=25 l=2
87 + ad=125 pd=60 as=9 ps=0

```

```

Magic Answers > Ring Oscillator > POST_new1_optimized_ring_oscillator.cir
98 M1040 M6 M5 vdd inverter_wo_label_05_0[0]/v_0_0# CMOSP w=25 l=2
99 + ad=125 pd=60 as=9 ps=0
100 M1041 M6 M5 gnd gnd CMOSN w=10 l=2
101 + ad=50 pd=30 as=9 ps=0
102 M1042 M7 M6 vdd inverter_wo_label_05_0[0]/v_0_0# CMOSP w=25 l=2
103 + ad=125 pd=60 as=9 ps=0
104 M1043 M7 M6 gnd gnd CMOSN w=10 l=2
105 + ad=50 pd=30 as=9 ps=0
106 M1044 M8 M7 vdd inverter_wo_label_05_0[0]/v_0_0# CMOSP w=25 l=2
107 + ad=125 pd=60 as=9 ps=0
108 M1045 M8 M7 gnd gnd CMOSN w=10 l=2
109 + ad=50 pd=30 as=9 ps=0
110 M1050 M11 M10 vdd inverter_wo_label_05_0[0]/v_0_0# CMOSP w=25 l=2
111 + ad=125 pd=60 as=9 ps=0
112 M1051 M11 M10 gnd gnd CMOSN w=10 l=2
113 + ad=50 pd=30 as=9 ps=0
114 M1052 M12 M11 vdd inverter_wo_label_05_0[0]/v_0_0# CMOSP w=25 l=2
115 + ad=125 pd=60 as=9 ps=0
116 M1053 M12 M11 gnd gnd CMOSN w=10 l=2
117 + ad=50 pd=30 as=9 ps=0
118 M1054 M13 M12 vdd inverter_wo_label_05_0[0]/v_0_0# CMOSP w=25 l=2
119 + ad=125 pd=60 as=9 ps=0
120 M1055 M13 M12 gnd gnd CMOSN w=10 l=2
121 + ad=50 pd=30 as=9 ps=0
122 M1056 M14 M13 vdd inverter_wo_label_05_0[0]/v_0_0# CMOSP w=25 l=2
123 + ad=125 pd=60 as=9 ps=0
124 M1057 M14 M13 gnd gnd CMOSN w=10 l=2
125 + ad=50 pd=30 as=9 ps=0
126 M1058 M15 M14 vdd inverter_wo_label_05_0[0]/v_0_0# CMOSP w=25 l=2
127 + ad=125 pd=60 as=9 ps=0
128 M1059 M15 M14 gnd gnd CMOSN w=10 l=2
129 + ad=50 pd=30 as=9 ps=0
130 M1060 M16 M15 vdd inverter_wo_label_05_0[0]/v_0_0# CMOSP w=25 l=2
131 + ad=125 pd=60 as=9 ps=0
132 M1061 M16 M15 gnd gnd CMOSN w=10 l=2
133 + ad=50 pd=30 as=9 ps=0
134 C1 inverter wo_label_05_1[0]/v_0_0# vdd 1.2FF
135 C1 vdd 1.2FF
136 C2 inverter wo_label_05_0[0]/v_0_0# vdd 1.2FF
137 C3 vdd 1.9FF
138 C4 inverter wo_label_05_0[0]/v_0_0# gnd 13.4FF
139 C5 gnd 3.2FF
140 C6 M16 gnd 1.3FF
141 C7 inverter wo_label_05_1[0]/v_0_0# gnd 14.3FF
142 C8 M30 gnd 1.1FF
143 C9 M31 gnd 1.2FF
144 C10 M31 gnd 2.3FF
145
146
147
148 .ic v(M1) = 'SUPPLY'
149 .tran 1n 20m
150
151 ** MEASURING DELAYS
152 .measure tran tpd
153 + TRIG v(M1) VAL='SUPPLY/2' FALL=1
154 + TARG v(M2) VAL='SUPPLY/2' RISE=1
155
156 .measure tran tpd
157 + TRIG v(M1) VAL='SUPPLY/2' RISE=1
158 + TARG v(M2) VAL='SUPPLY/2' FALL=1
159
160 .measure tran tpd param='(tpdr+tpdf)/2' goal=0
161
162
163
164 .control
165 set curplottitle="Aravind Narayanan-2019102014-(S-b1)-Optimized"
166 set color=white ** color1 is used to set the background of the plot (manual sec:17.7)
167 set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
168
169 run
170 set curplottitle="Aravind Narayanan-2019102014-(S-b1)-Optimized"
171 plot v(M1) v(M2)
172 hardcopy Optimized_Ring_Oscillator.eps v(M1) v(M2)
173 .endc
174
175 .end
176

```

Figure:

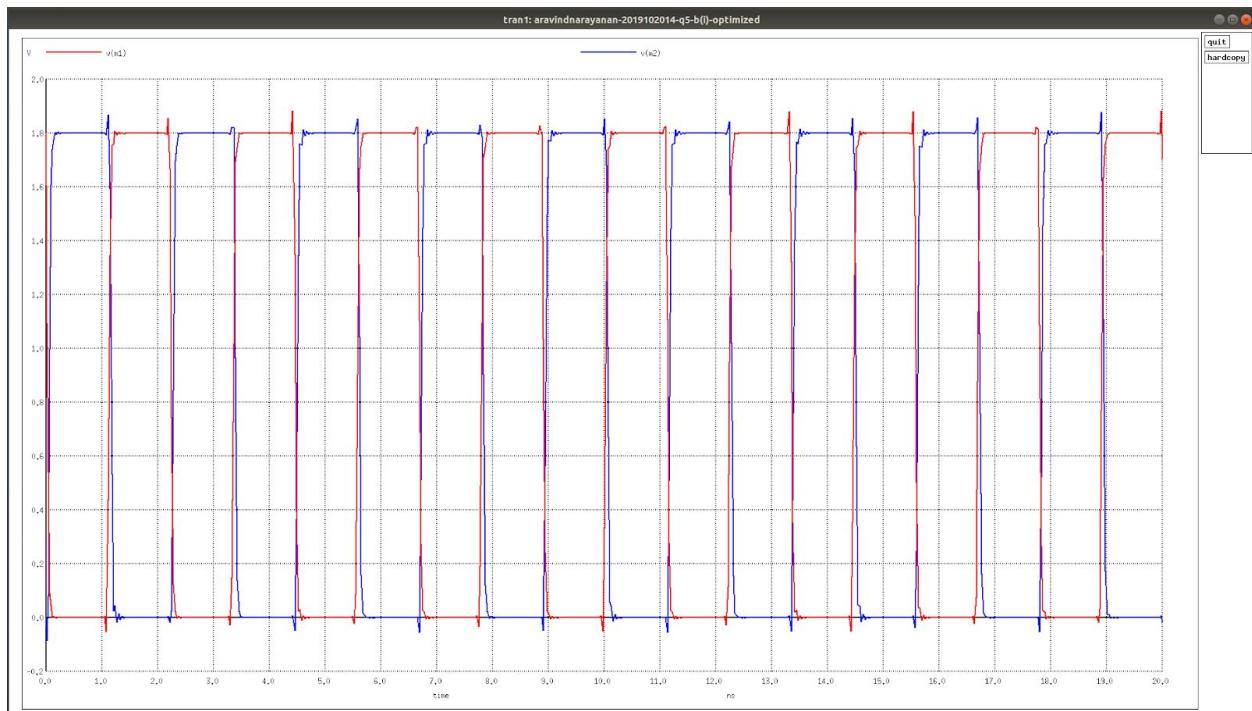


Fig: Output waveform of M1 and M2 to show inverter characteristics

(D)

SNo	Rise Time	Fall Time	Time Delay	Frequency of Oscillation
NGSPICE	33.36732ps	34.68365ps	34.0255ps	474MHz
Unoptimised	57.44622ps	50.97764ps	54.1569ps	297.8MHz
Optimised	34.45674ps	36.42392ps	35.4403ps	455.1MHz

Effect of Parasitic Capacitors on a CMOS Inverter:

We try to show how parasitic capacitors influence delay in a single inverter then extend the same logic for a 31-stage ring oscillator.

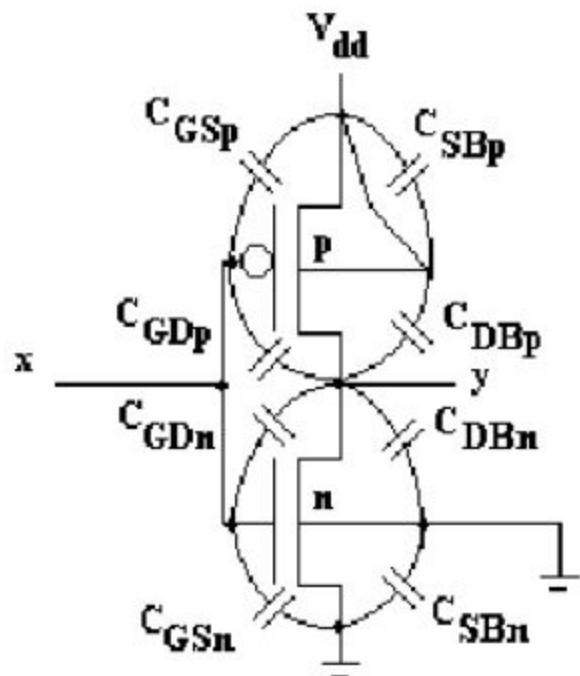


Fig: CMOS INVERTER WITH PARASITIC CAPACITANCES

In this figure,

- The Gates of transistors are the inputs to the inverter, any capacitor touching the gate should be considered input capacitance.
- The Drains of the transistors are connected to the inverter output, any capacitor touching the Drains should be considered output capacitance

These output capacitances will increase the load on the inverter it is connected to, thereby increasing delay.

So the **main goal of making an optimised layout is to reduce the presence of parasitics** as much as possible.

Observations:

- It's clearly visible that when we optimise the layout diagram, we get a frequency that's

relatively much close to the ngspice time delay. We see this effect due to the parasitics in effect.

- In the unoptimised layout, the metal between the 31st inverter and the 1st inverter is long(large length) due to which the capacitances will increase and the propagation delay is obviously more.
- In the optimised layout as we built a **circular structure** for the mosfet, the metals used are significantly less. We also have a common ground which reduces the redundancy significantly reducing the requirement of extra metal.