Indian Institute of Technology Bombay
Department of Electrical Engineering
EE-224: Digital Design

Project- Part A

Submission Deadline: December 4, 2020 (Friday) 11:29 pm

Group size: Maximum four

Description of design:

Design a signed 16-bit Arithmetic and Logical Unit (ALU) which computes the following functions. Use Structural VHDL for the design. You are also required to write testbench to verify your design.

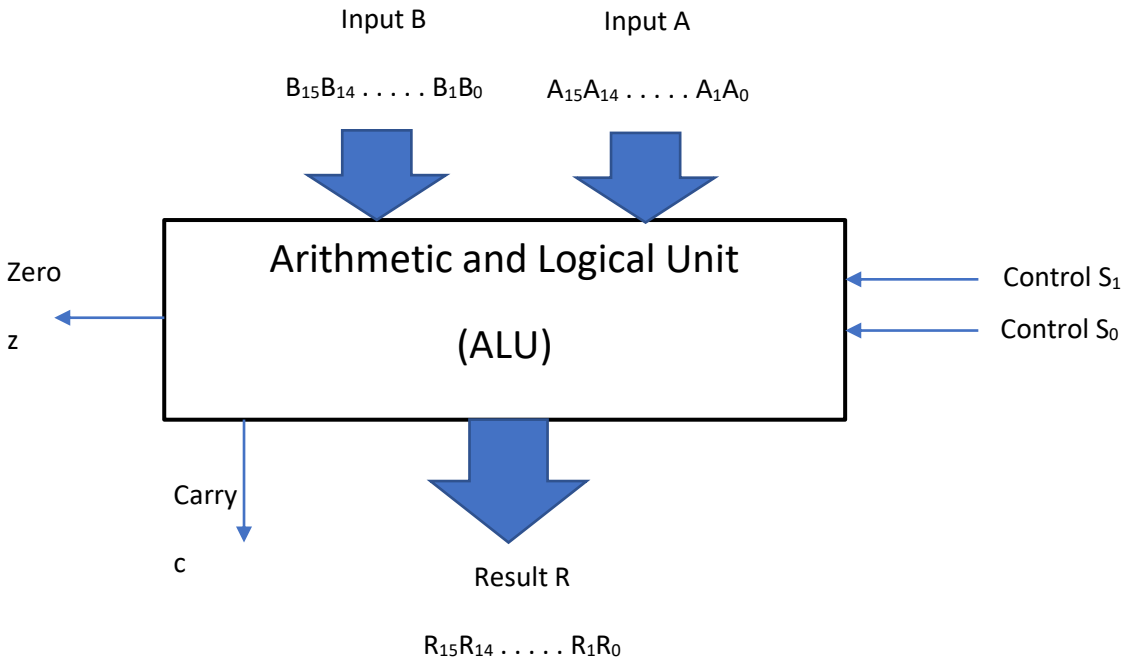
1. Signed Addition (control input $S_1S_0 = 00$)
2. Subtraction (Control input $S_1S_0 = 01$)
3. NAND operation (Control input $S_1S_0 = 10$)
4. XOR operation (control input $S_1S_0 = 11$)

The output should be the 16 bit result of the computation and carry (in case of arithmetic operation) and zero bit. If the result of computation is zero then it should set the zero output (i.e, z = 1). Assume that the inputs are in 2's complement form.

Design a fast adder (Brent Kung/ Kogge Stone) to compute addition operation.

Submission output:

1. VHDL Code
2. Testbench
3. Output waveform


Input B
$B_{15}B_{14}$ . . . . . B_1B_0
Input A
$A_{15}A_{14}$ . . . . . A_1A_0
Arithmetic and Logical Unit
(ALU)
Zero
z
Control S_1
Control S_0
Carry
c
Result R
$R_{15}R_{14}$ . . . . . R_1R_0