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Edveon Technologies - Written Test Admit Card

raksha@edveon.com <raksha@edveon.com>   1 August 2025 at 14:50
To: aravindaravindhan243@gmail.com

Edveon Technologies - Written Test Admit Card

Candidate Name: Aravindhan
Position Applied For: Chip Design Verification Engineer
Date of Test: 07 August 2025 (Thursday)
Exam Centre: Jerusalem College of Engineering, Chennai - 600100

Reporting Time: 9.00 am

Important Instructions:

1. Please print this email – it will serve as your admit card for the written test. Entry will not be allowed without a printed copy.

2. Carry a valid photo ID proof for verification (Aadhar Card, PAN Card, or Driving License).

3. Bring a printed copy of your updated resume.

4. Ensure you report at least **30 minutes early**. Late arrivals will not be permitted.

5. Electronic devices (e.g., mobile phones, smartwatches) are **strictly prohibited** inside the exam hall.

6. Bring your own stationery: A4 sheets, pens, pencils, writing pad, etc.

7. The test will cover the following areas:

- **Logical Aptitude –** To test your reasoning and problem-solving skills
- **Digital Electronics –** Basic concepts and fundamental principles
- **Programming –** To evaluate logic and solving problems using any programming language. (Avoid using built-in methods)

Note: This is a written test and **not MCQ-based**.

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