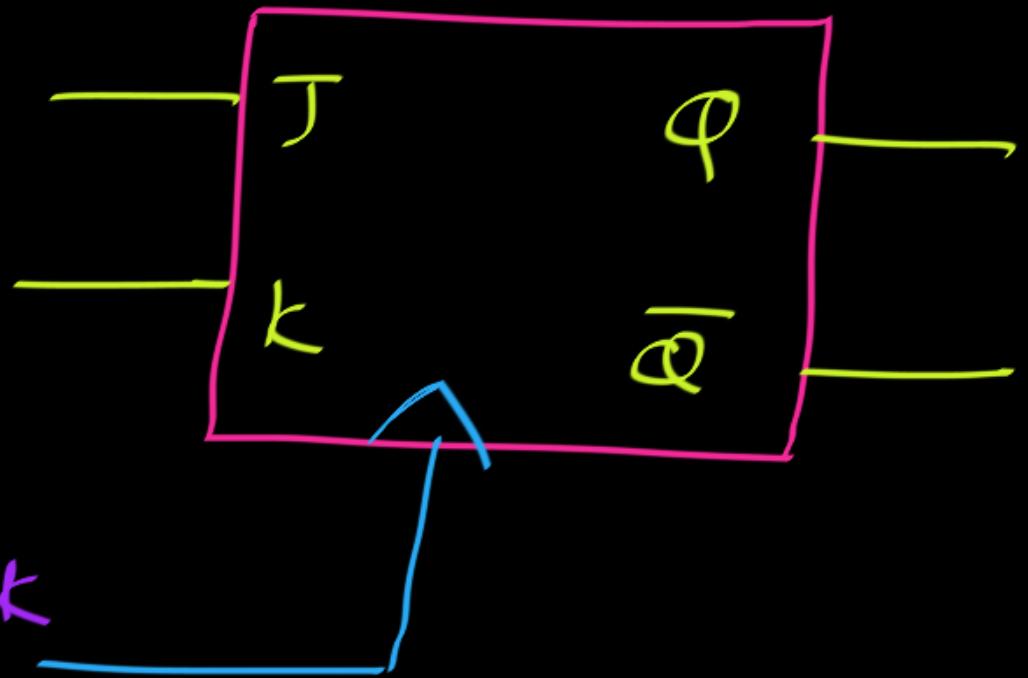




Next Topic :

Special Inputs in flipflops

Preset, Clear inputs



+ve Edge Triggered
JK - FF.



Direct Inputs

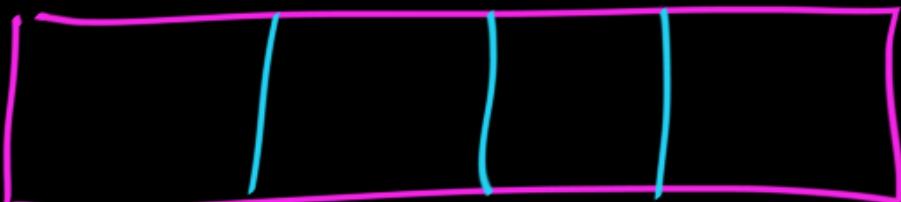
Some flip-flops have asynchronous inputs that are used to force the flip-flop to a particular state independently of the clock. The input that sets the flip-flop to 1 is called *preset* or *direct set*. The input that clears the flip-flop to 0 is called *clear* or *direct reset*. When power is turned on in a digital system, the state of the flip-flops is unknown. The direct inputs are useful for bringing all flip-flops in the system to a known starting state prior to the clocked operation.



CLASSES



CPU →

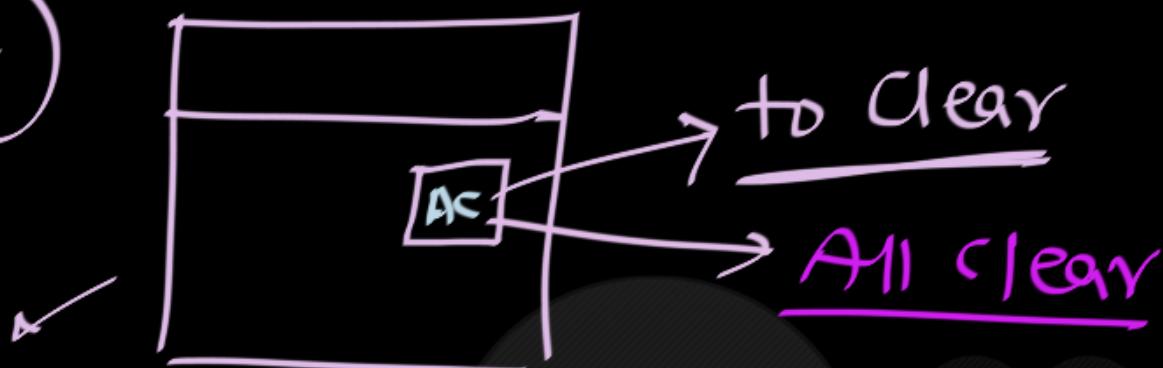


4-flipflops

Registers
↓
Collection
of
flipflops



(2)



Calculator

Digital ckt's :

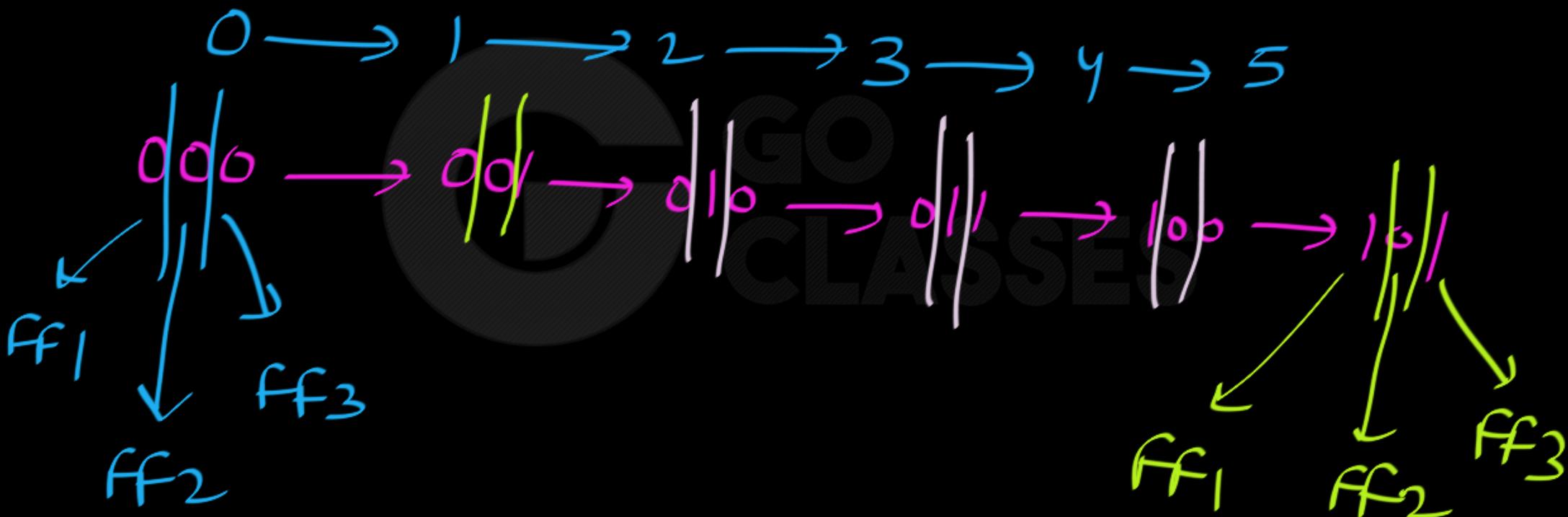
Desirable
Buttons/
signals

Clear \Rightarrow make
state 0

Preset \Rightarrow make
state 1

- ③ most of time Counting is Done
in increasing or Decreasing order.
- ✓ Clear is beneficial
- ✓ Preset is beneficial.
- ↓
Rocket launch

④ in Counter we will study :





Using 3-flipflop:

Counting:
(naturally)



But I want to count
0 → 1 → 2 → 3 → 4 → 5 → Clear → 0



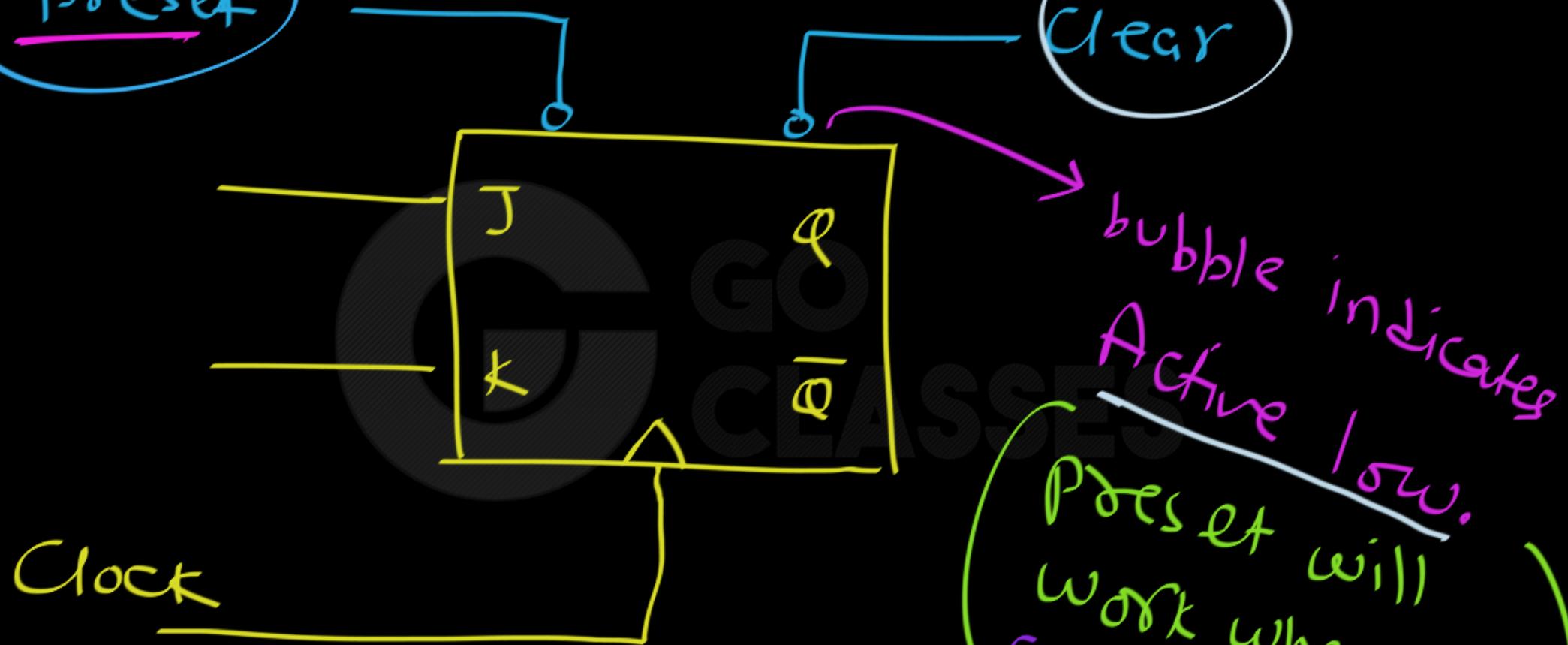
Preset input : make state 1.

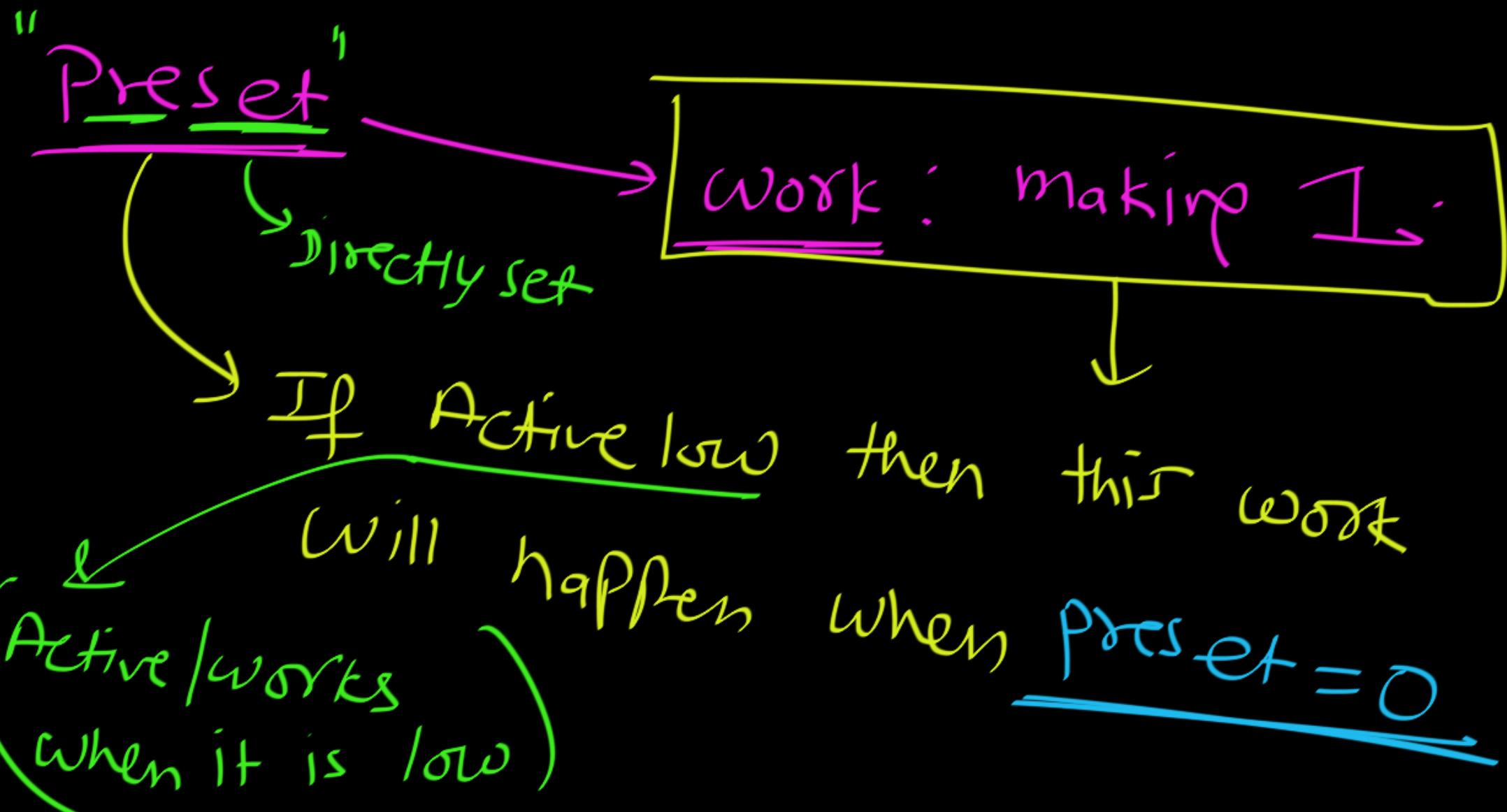
Direct inputs

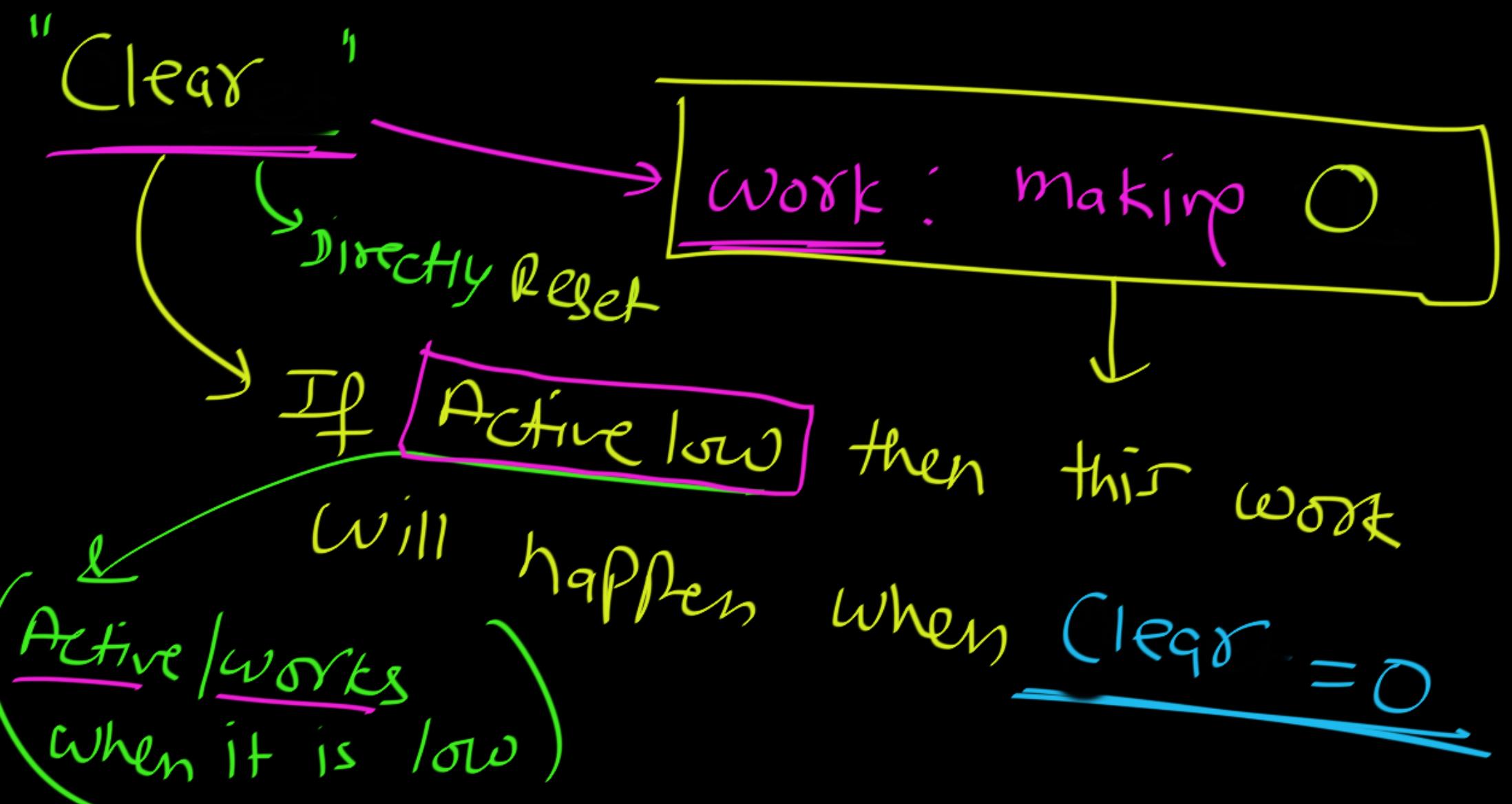
Clear input : make state 0.

Preset

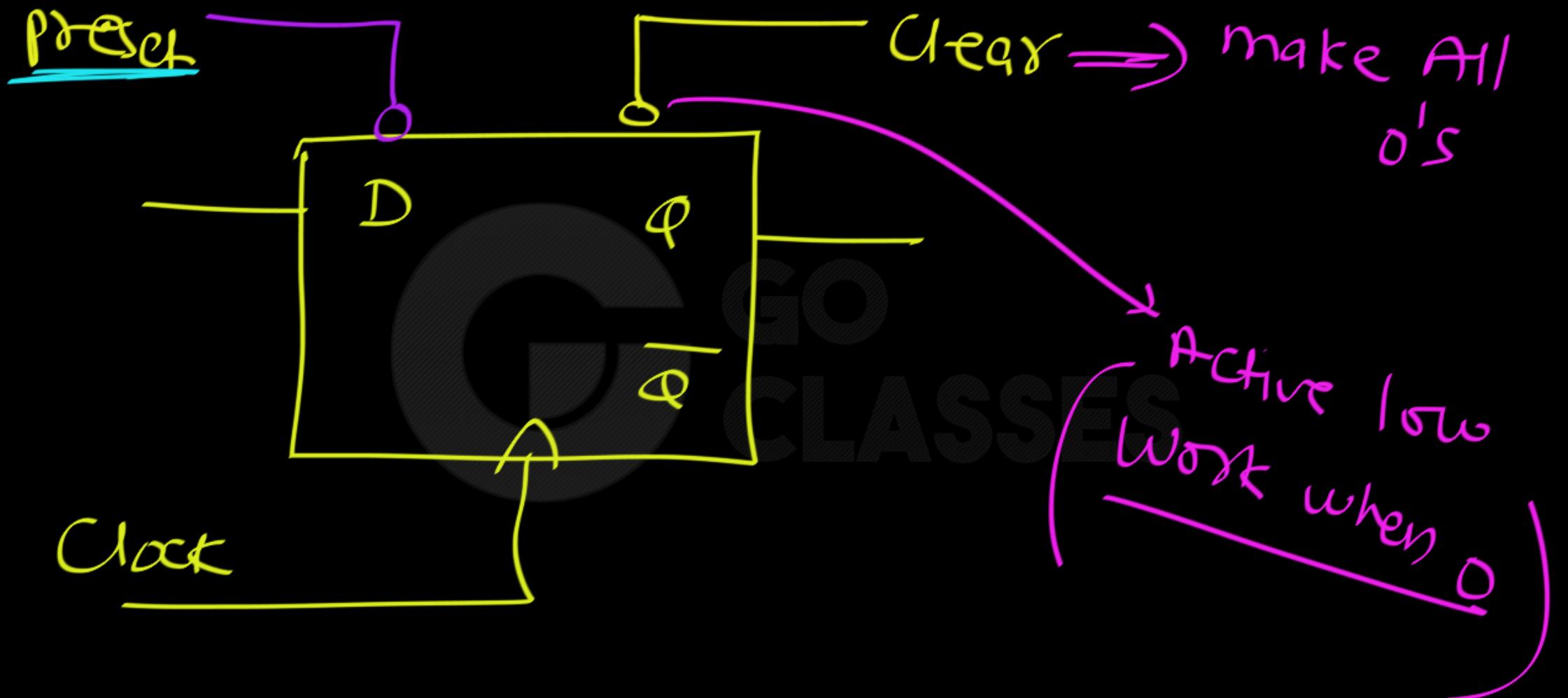
Clear







Preset	Clear	Clock	J	K	Q_n
✓ 0 =	1	X	X	X	1 set
1	0	X	X	X	0 clear
1	1				Normal JK behaviour
Never occur	0				Uncertain (forbidden)

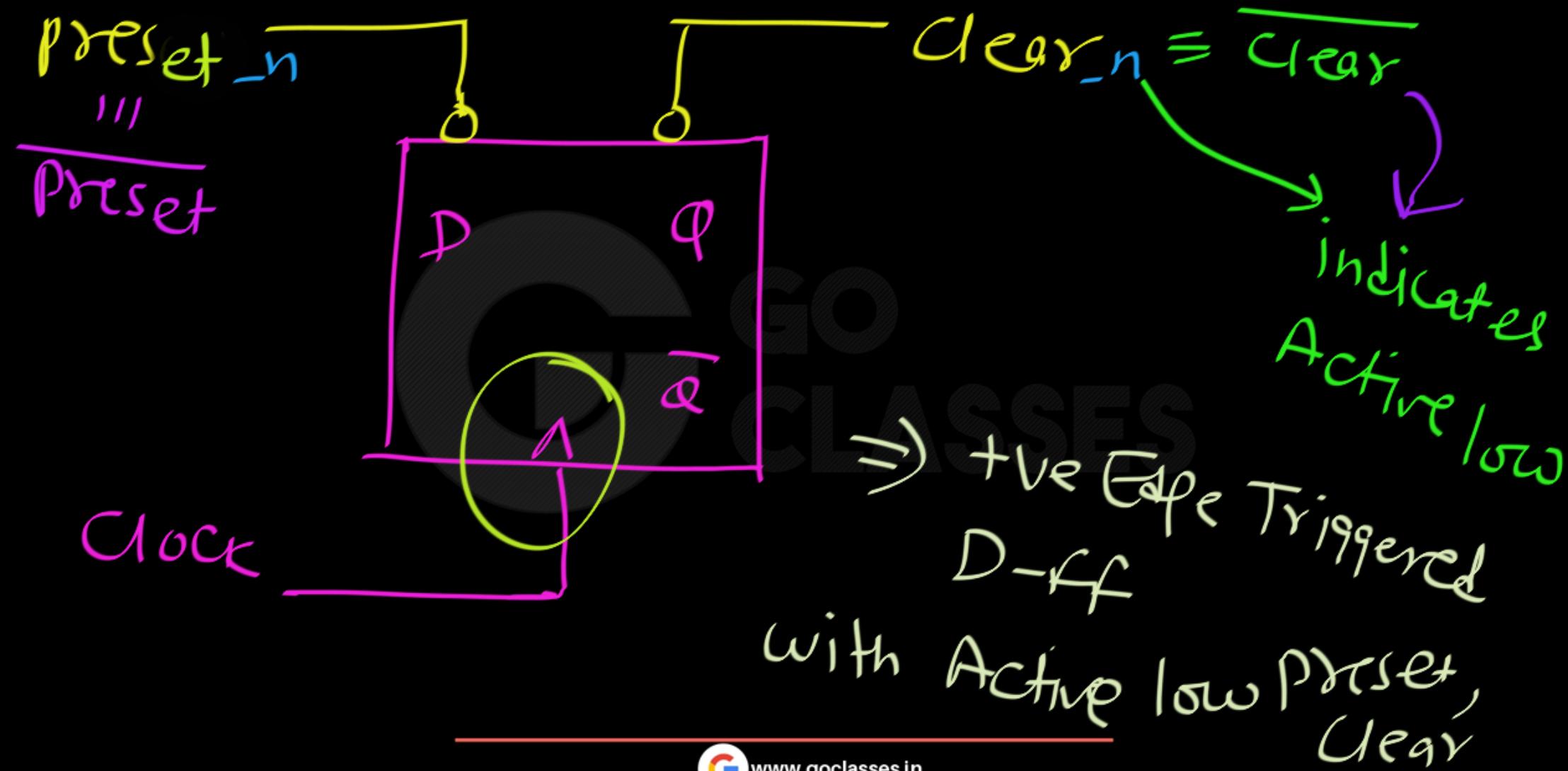


Preset, Clear : \Rightarrow



Direct inputs

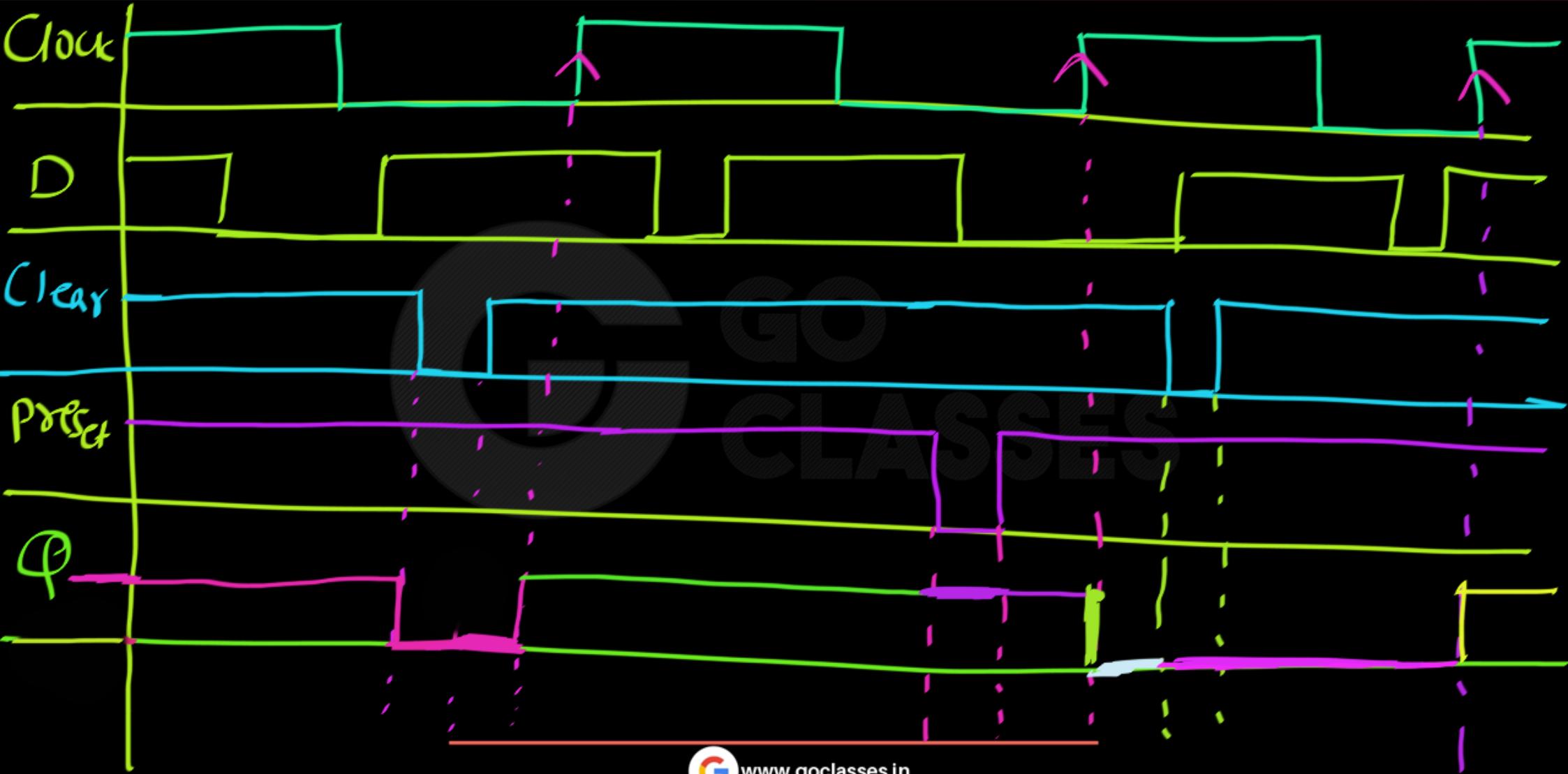
Work immediately (like E_{n0})





Digital Logic







Clear | Preset \Rightarrow Don't Care About

Clock, inputs



Asynchronous (not in sync with clock)



In Seq. Ckt:

- ① Synchronous : in sync with Clock
- ② Asynchronous : Not in Sync with Clock

- Preset
- Clear
- ① Asynchronous (Not in sync with clock)
They don't wait for clock.
 - ② Immediately work
 - ③ Active low
 - ④ Both 0 Not Allowed
 - ⑤ Both 1 \Rightarrow Normal FF behaviour



So far:

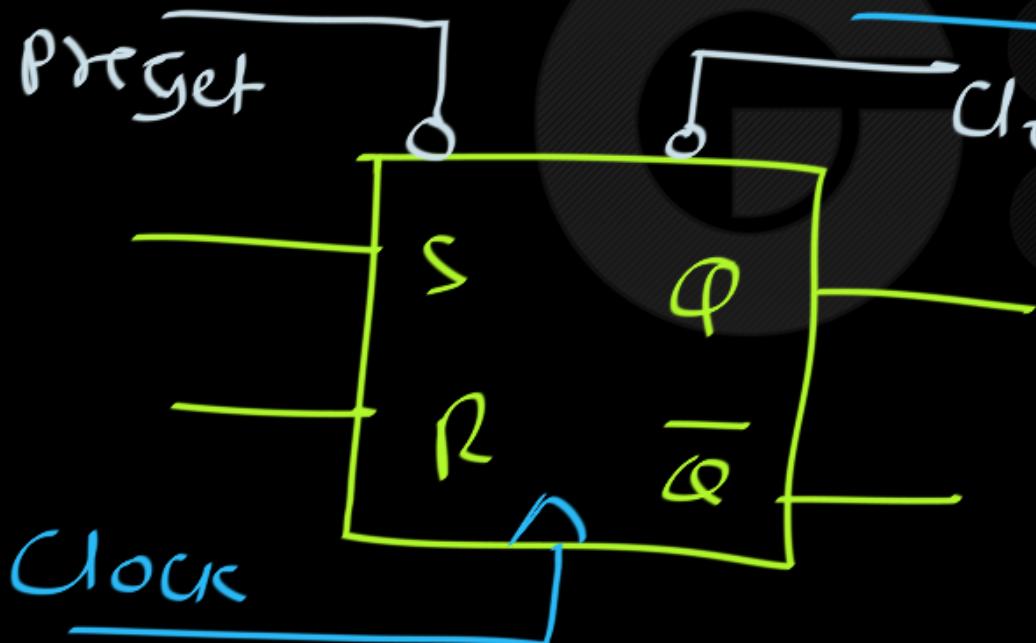
Preset, clear behaviour ✓

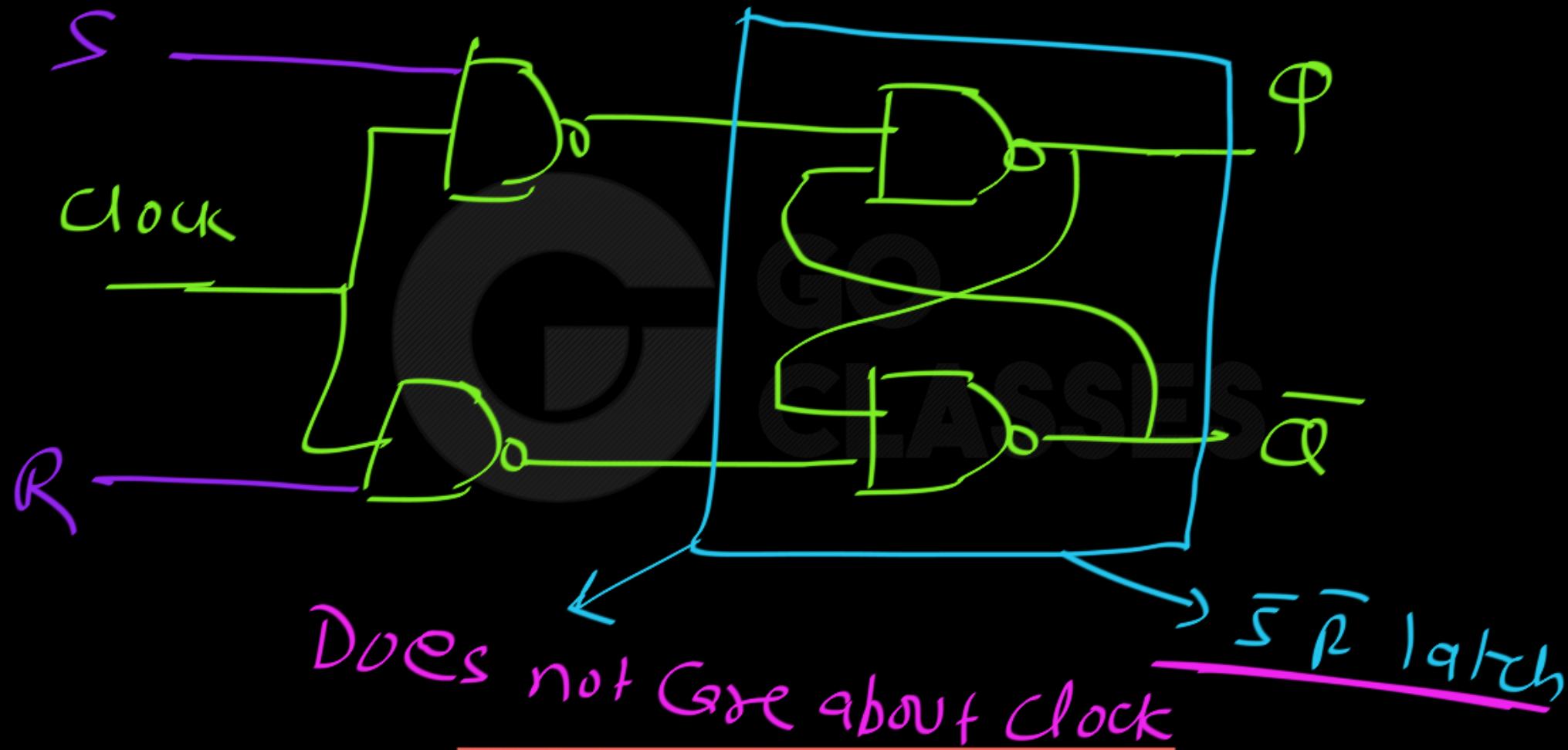
How to implement them?

6

φ : In SR - FF (of NAND implementation)

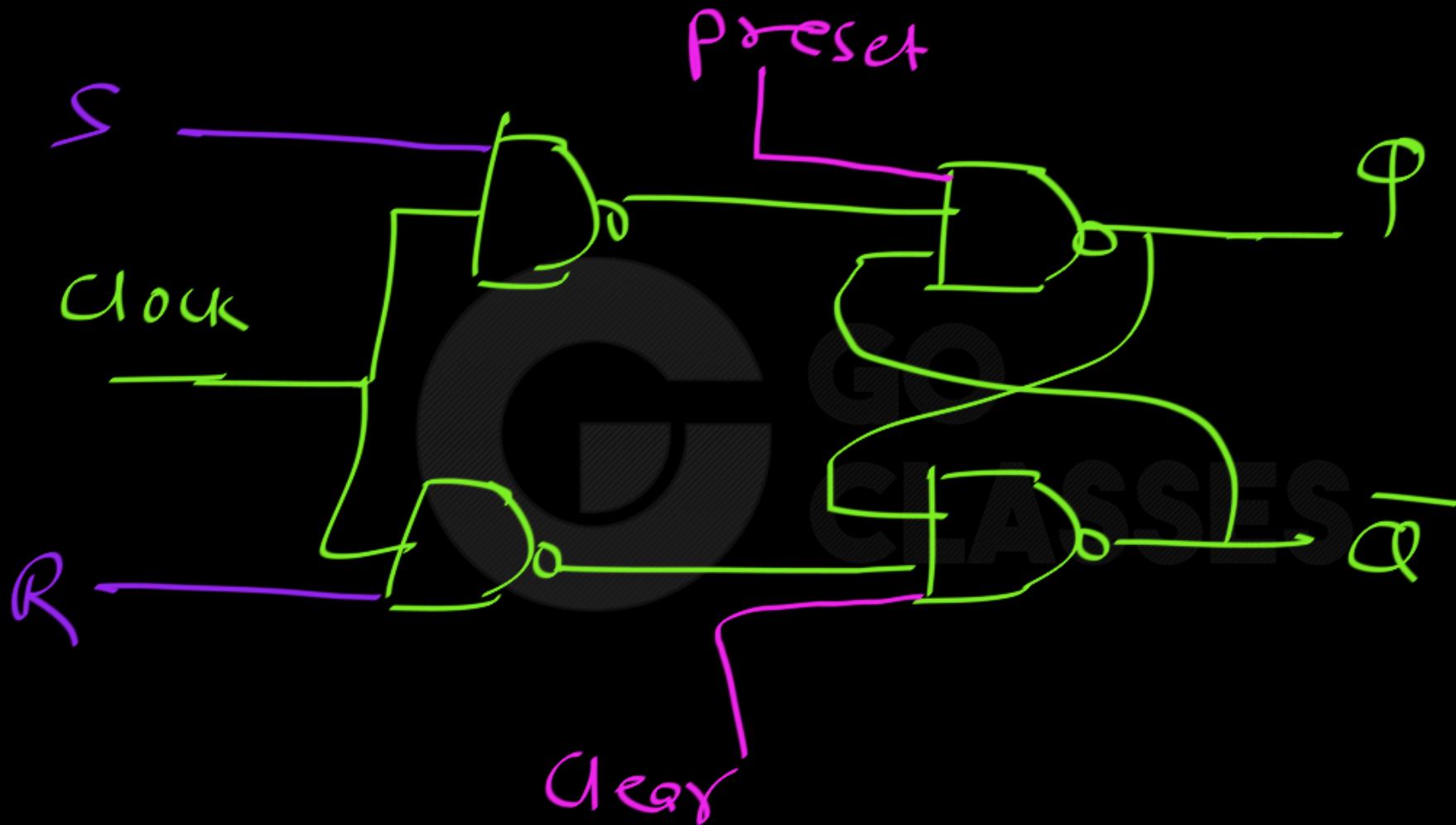
How to add Preset, Clear input





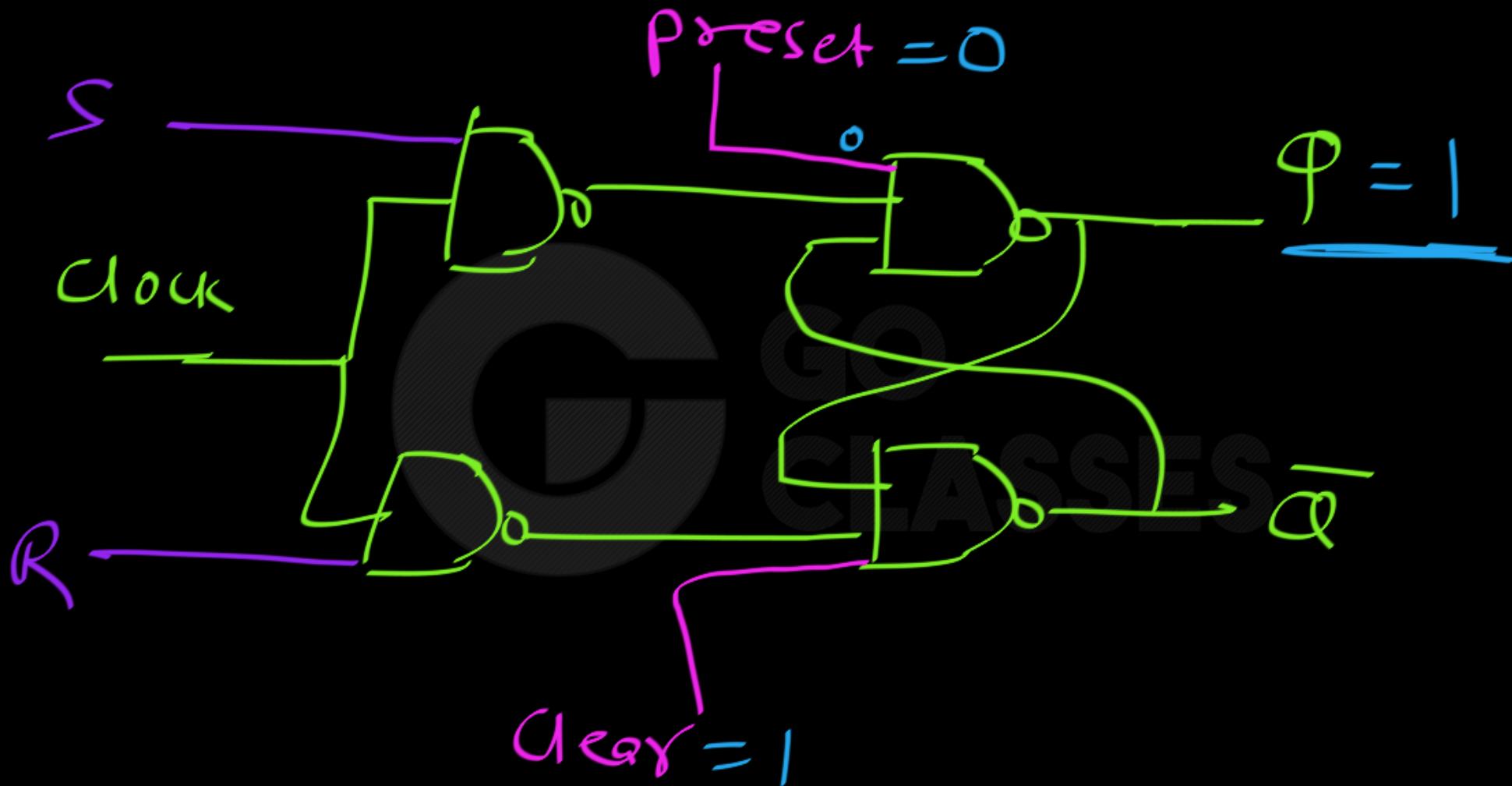


Digital Logic



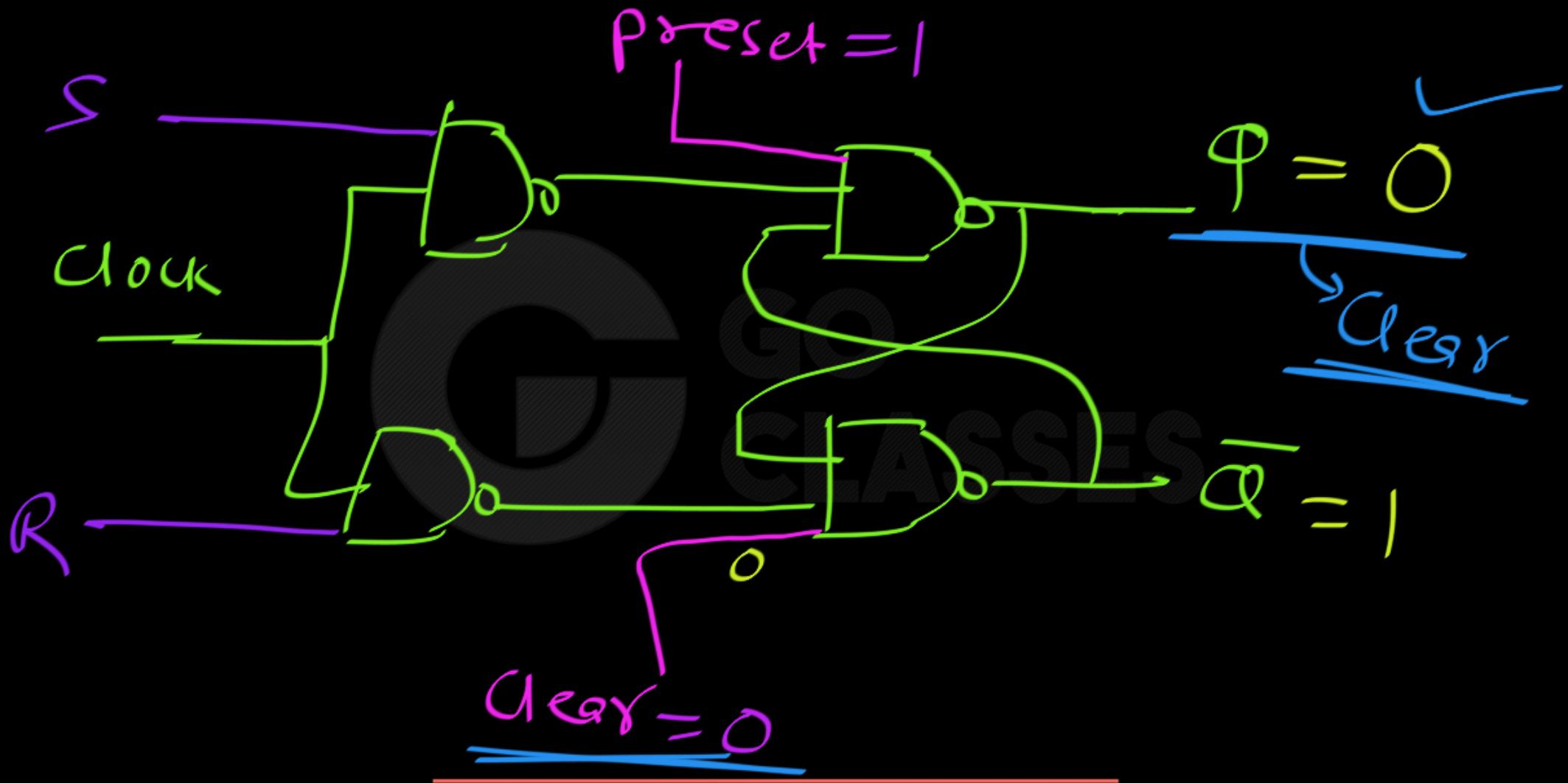


Digital Logic





Digital Logic

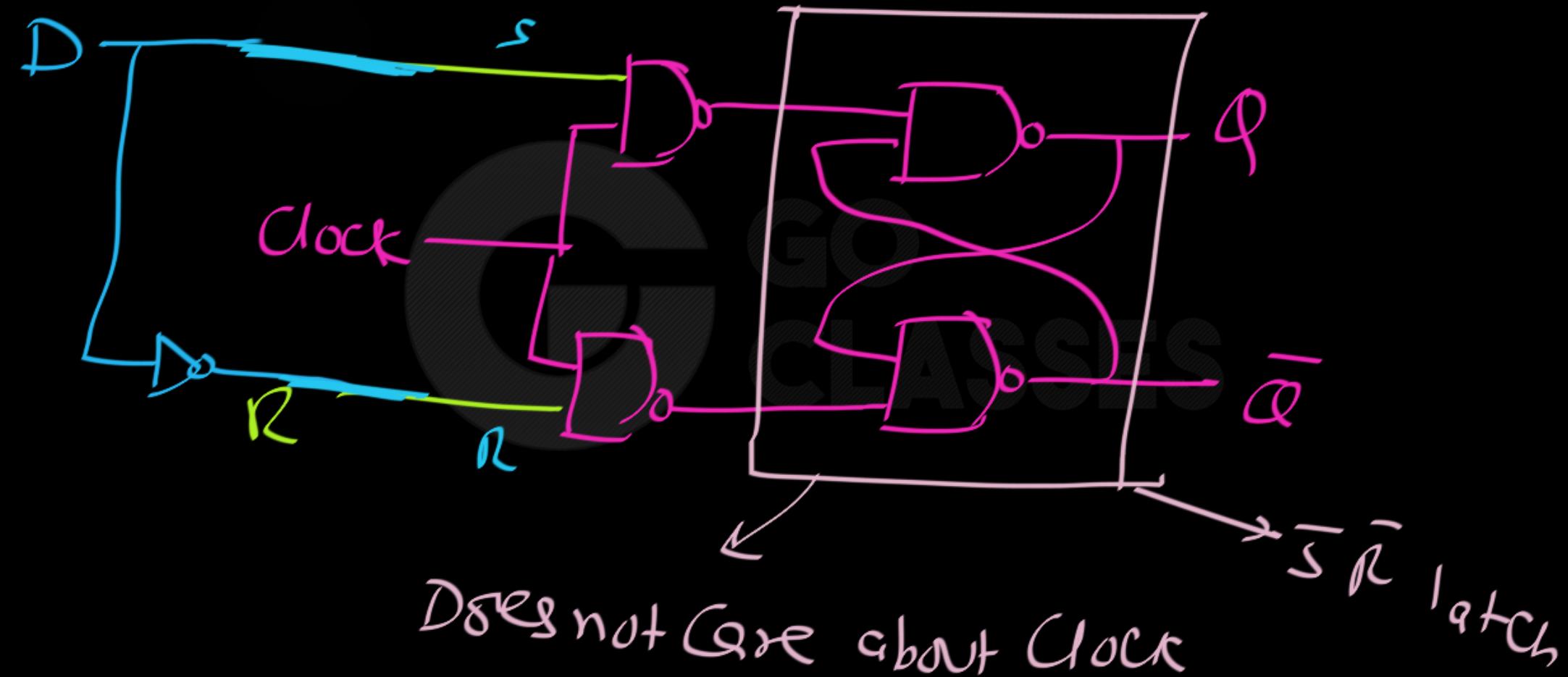


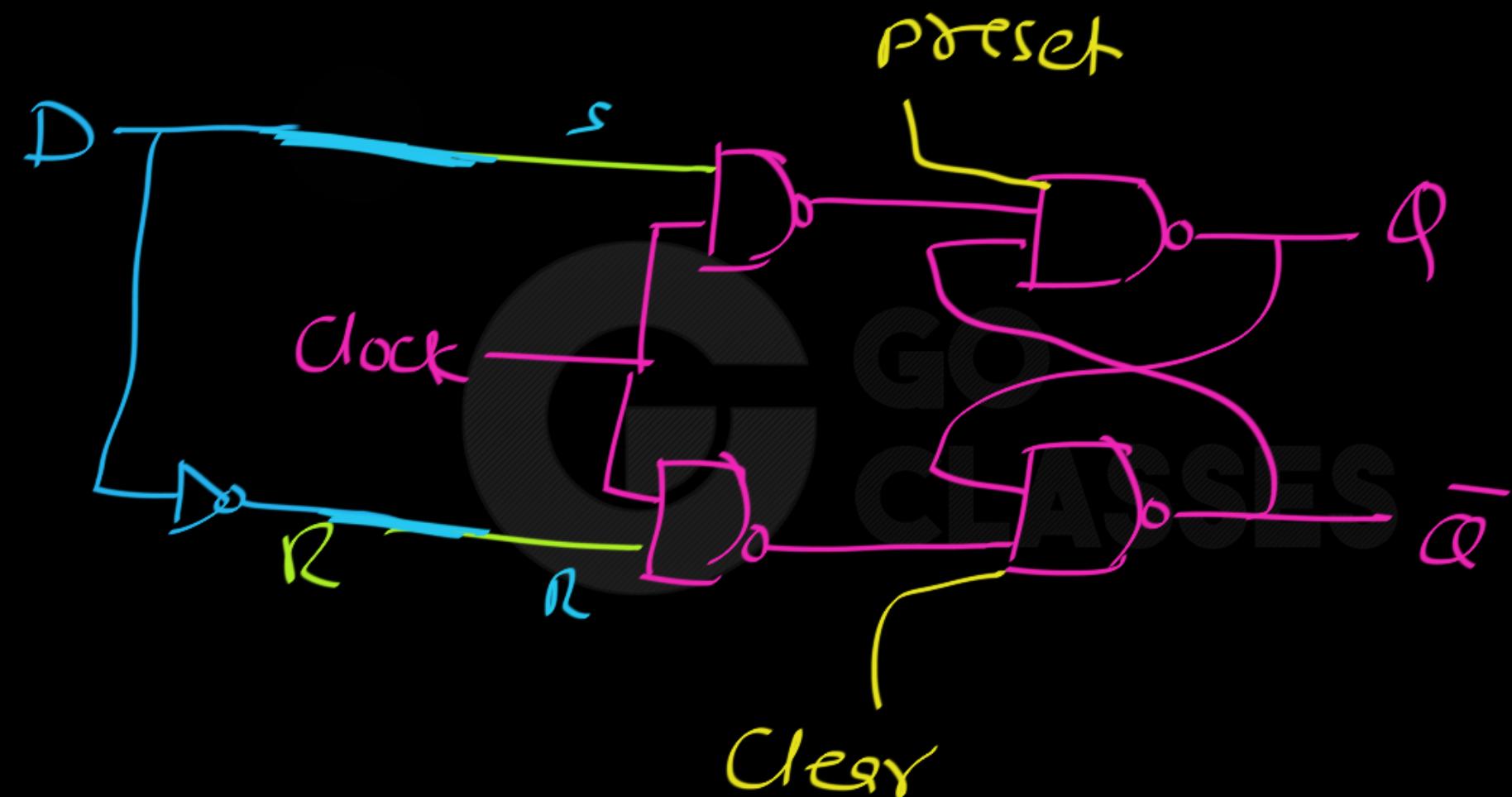
Q: In D-FF (NAND implementation)

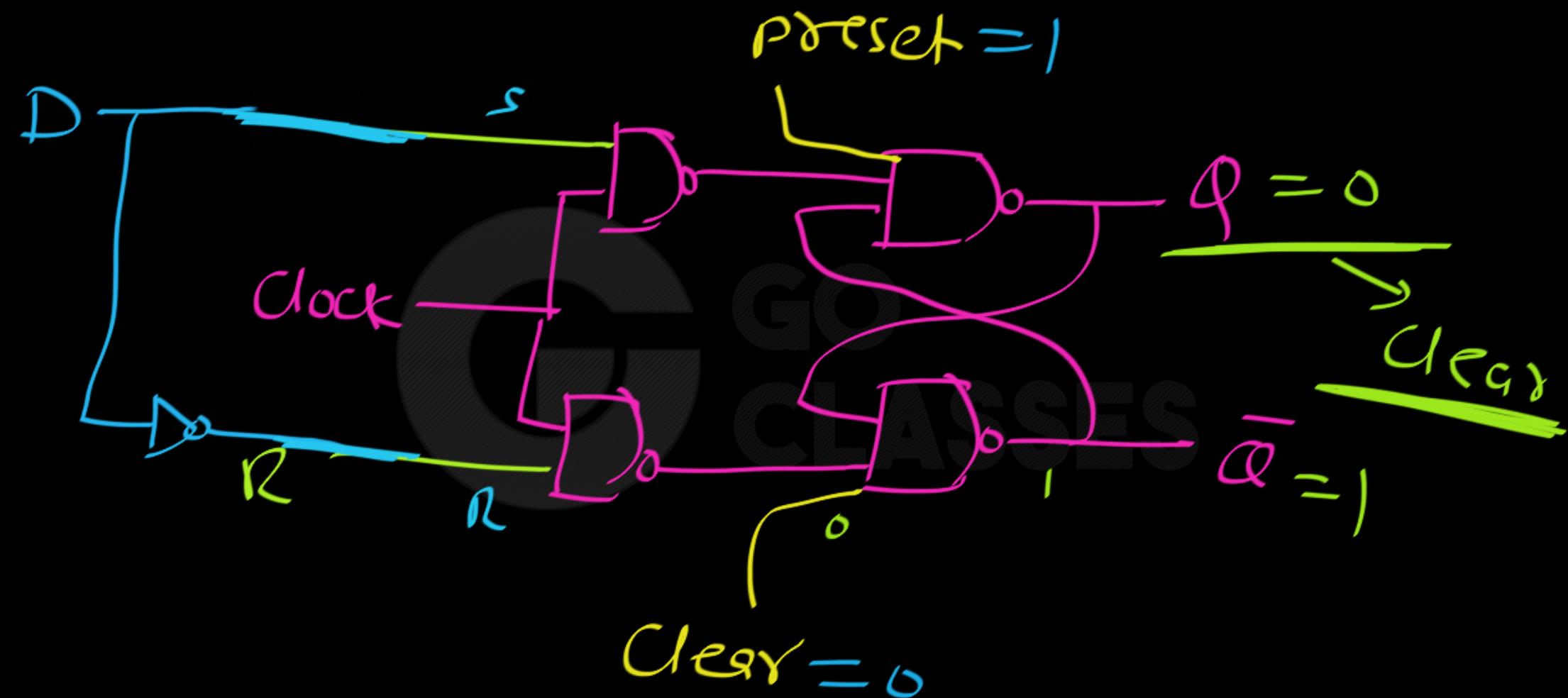
How to Preset & Clear
?

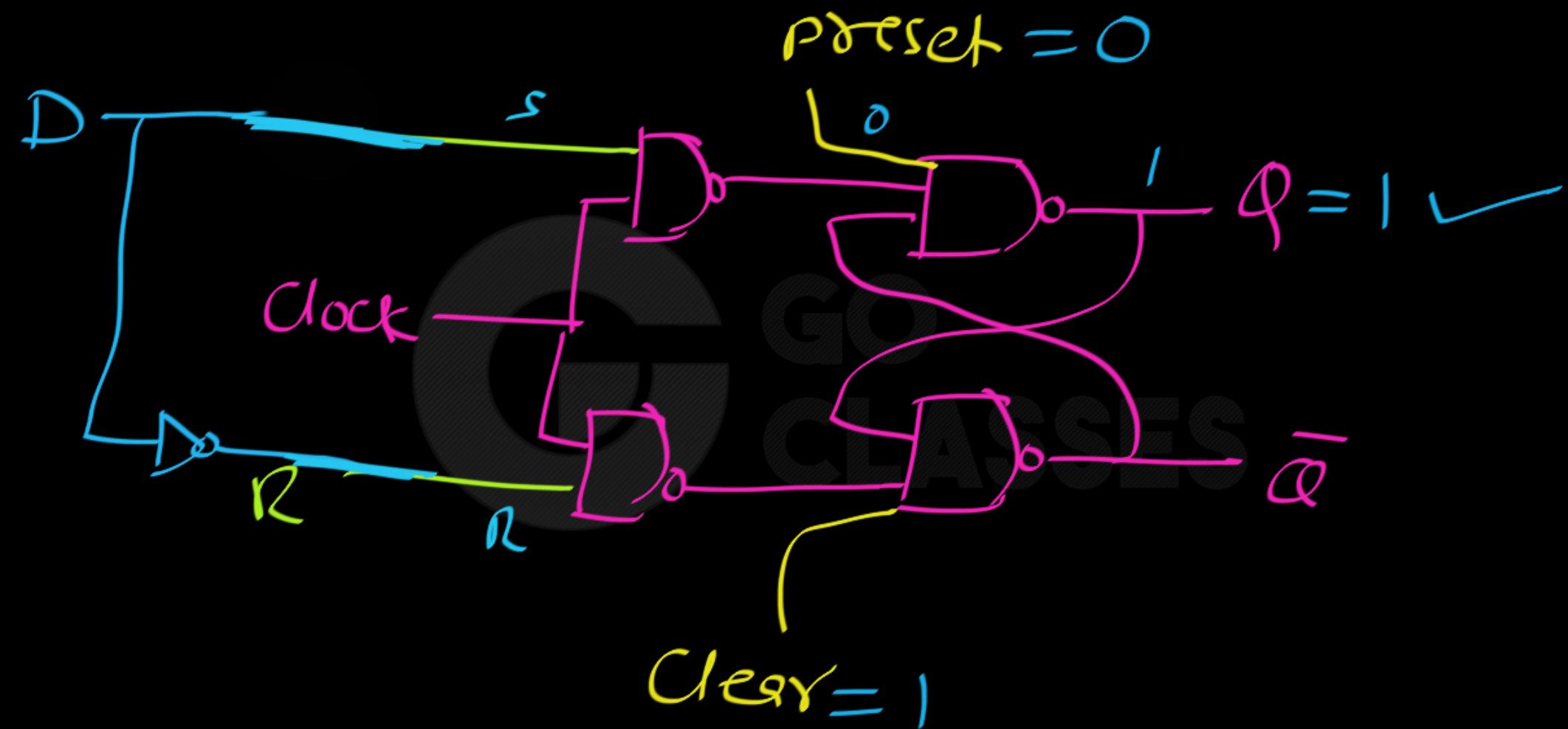
Asynchronous Preset Clear







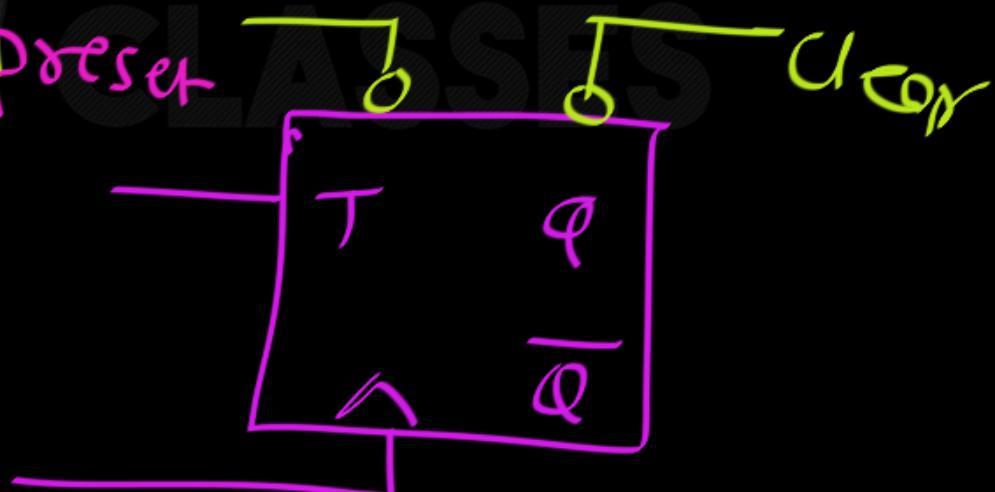




Preset, Clear → will Reset immediately

Additional inputs in ff

Set immediately





Preset, Clear:

by Default: { Asynchronous ✓
Active Low }

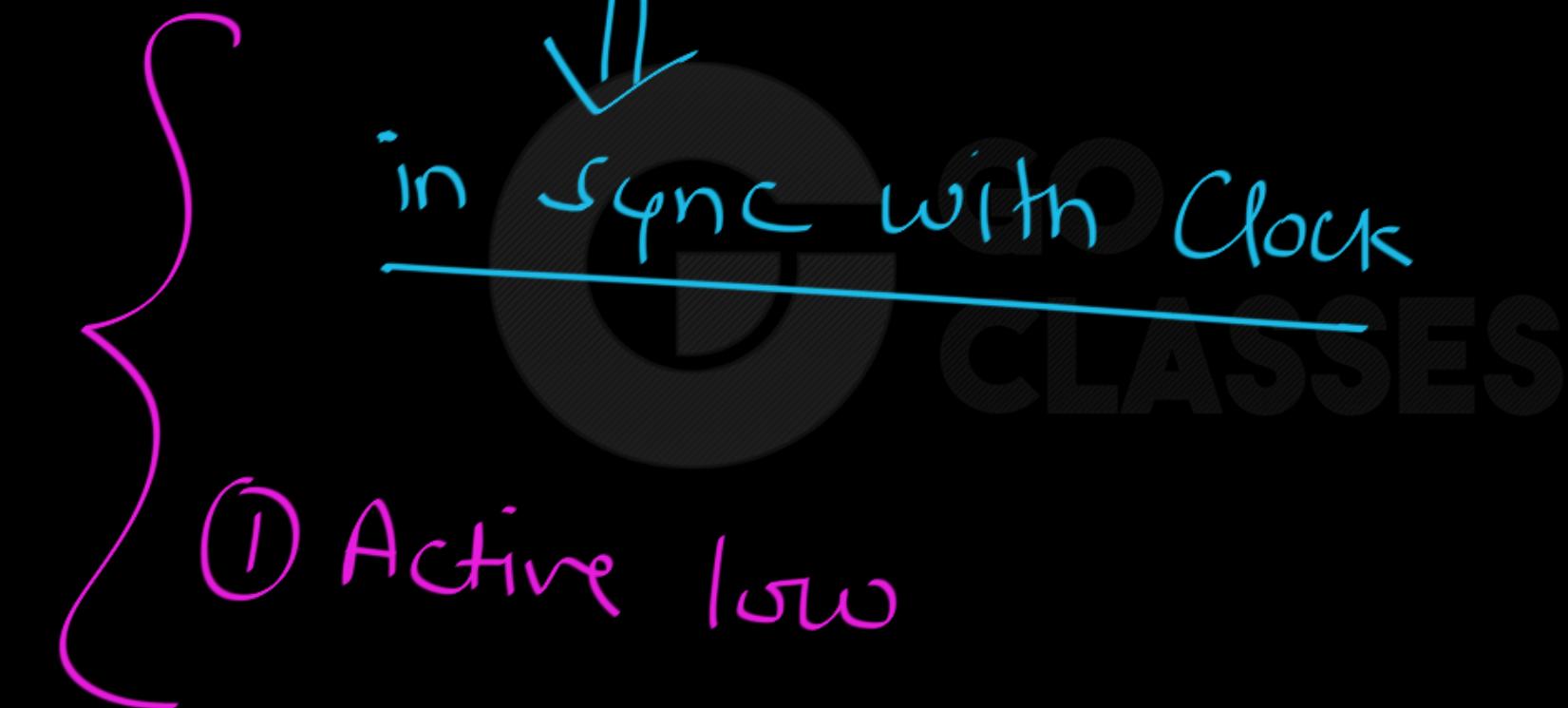


Digital Logic

Preset	Clear	clock	T	Φ_n
<u>0</u>	1	X	X	Preset
1	<u>0</u>	X	X	0 Clear
1	1			Normal T-ff working
0	0			forbidden

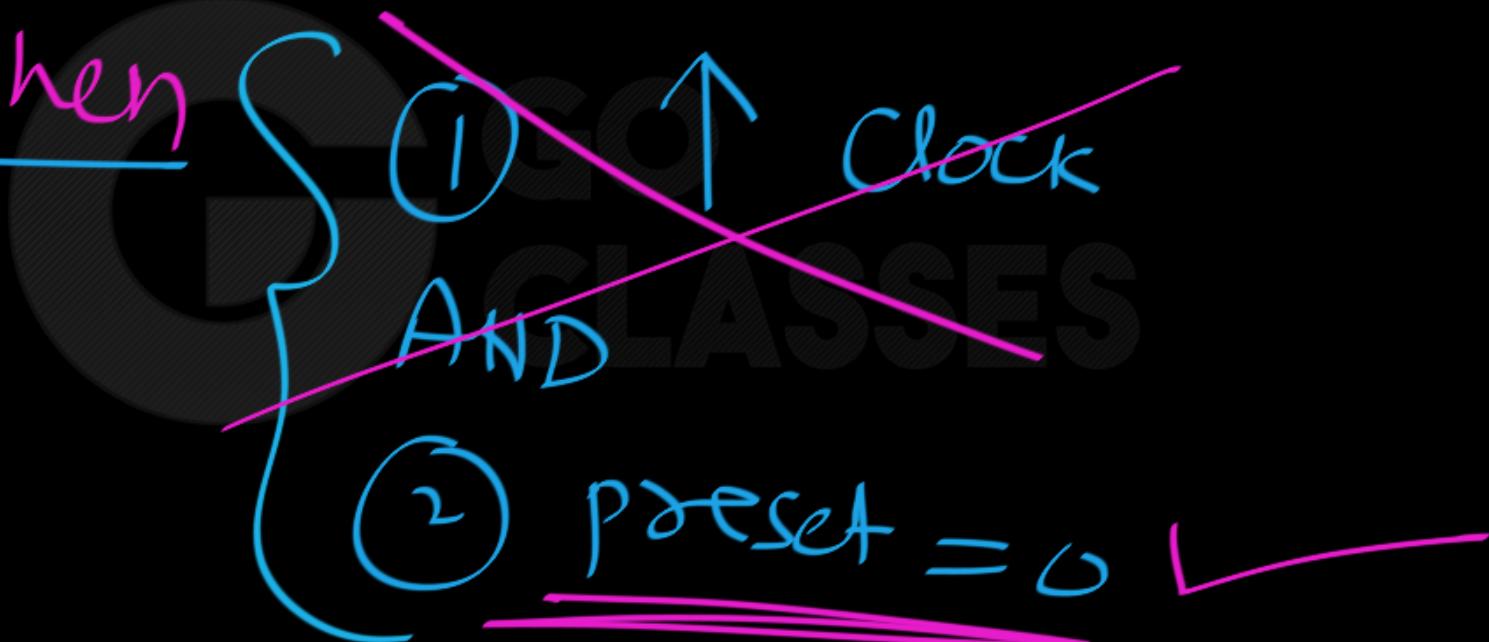


Synchronous Preset, Clear

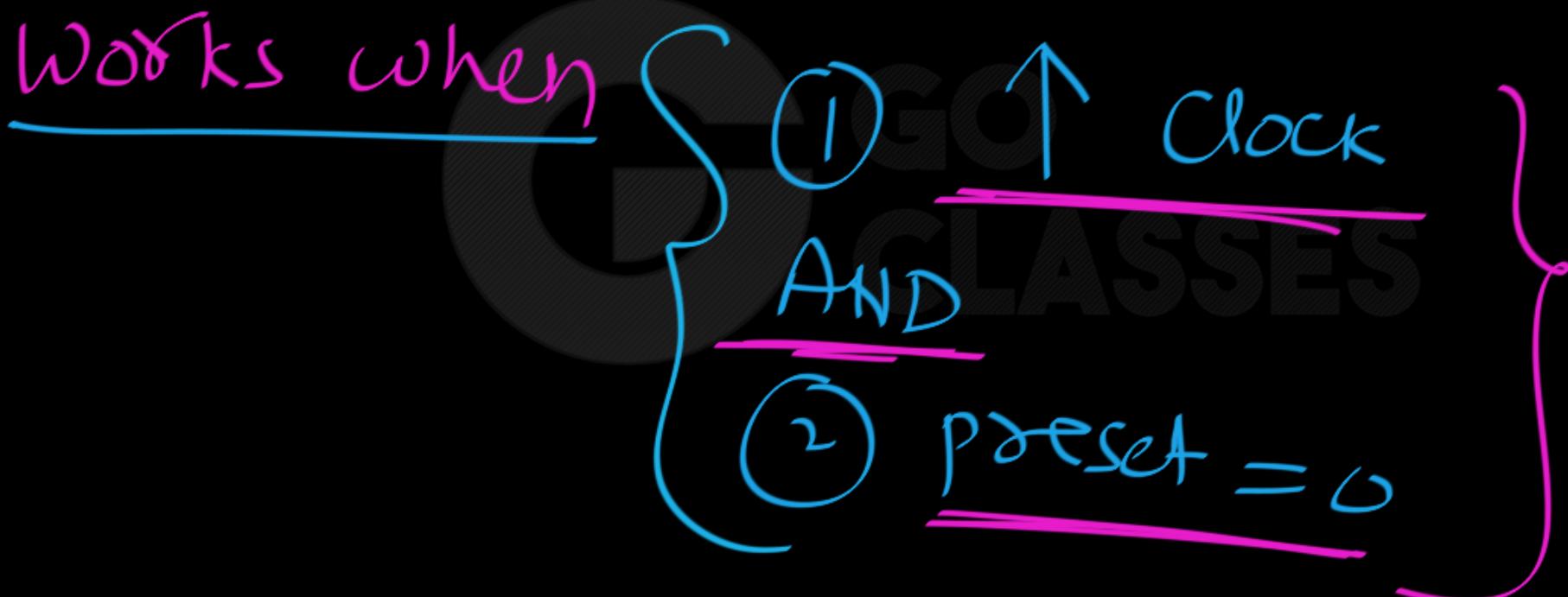


Asynchronous Preset : (Assume ff is
the Edge Triggered)

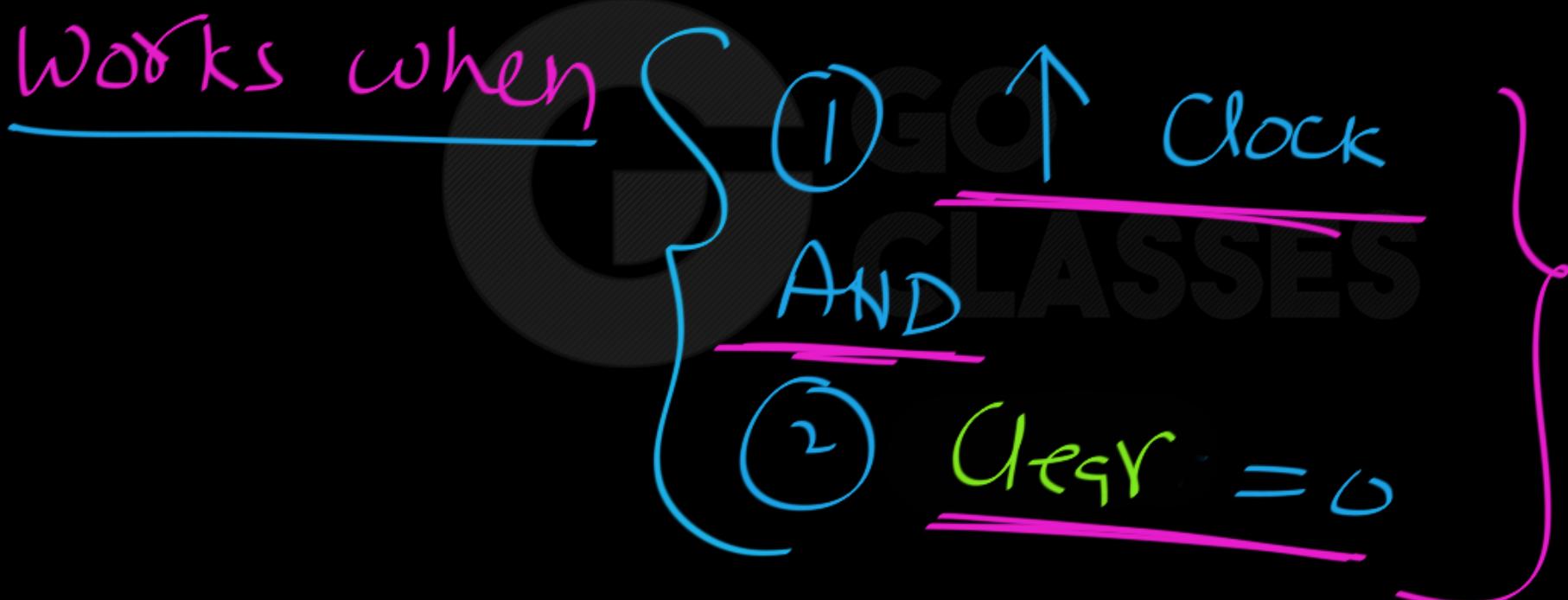
Works when



Synchronous Preset : (Assume ff is +ve Edge Triggered)



Synchronous Clear : (Assume ff is +ve Edge Triggered)





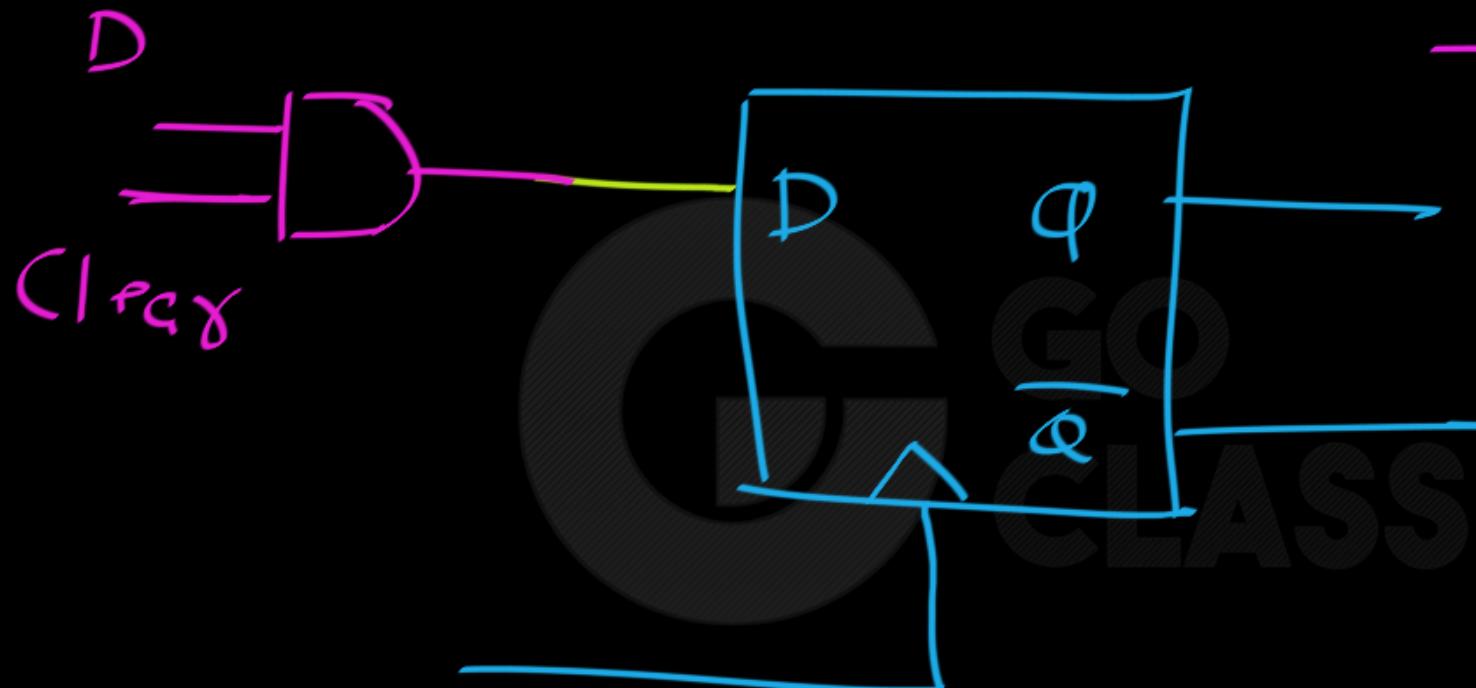
Q: D-ff with +ve \downarrow Triggering.
Edge

How to add Synchronous Clear }

works / \uparrow edges } { clock \uparrow
and
Clear = 0 }

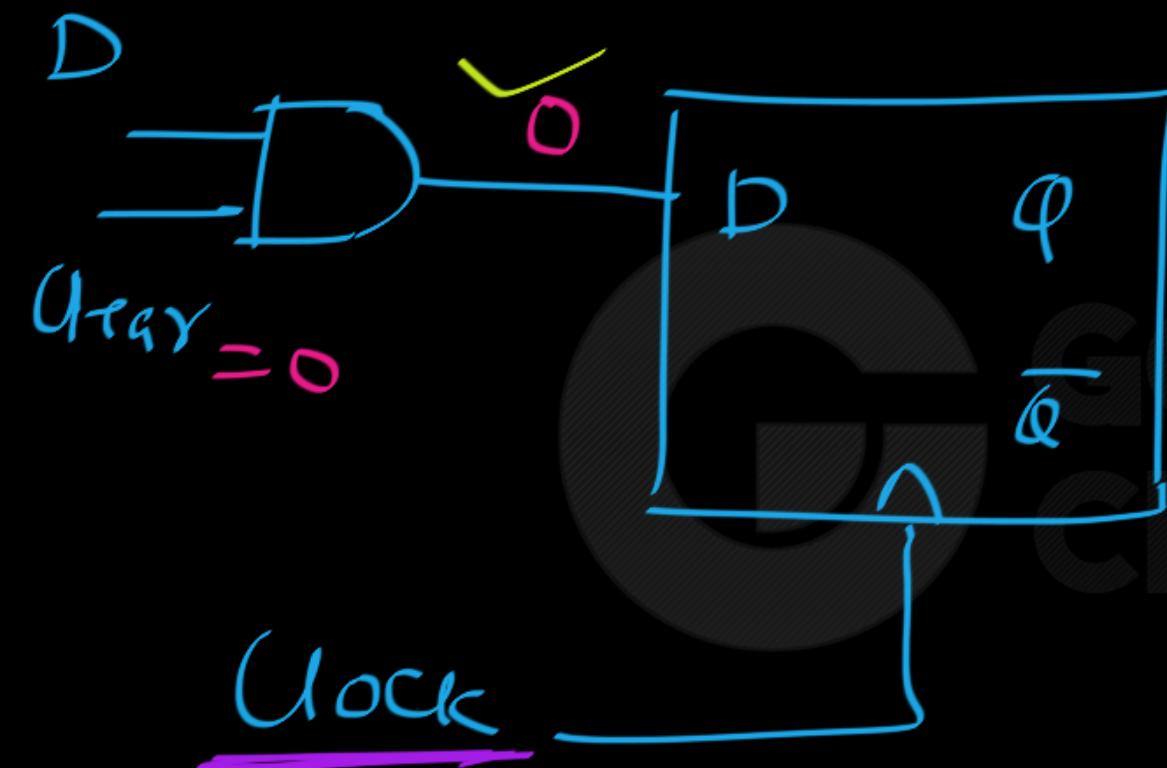


Digital Logic



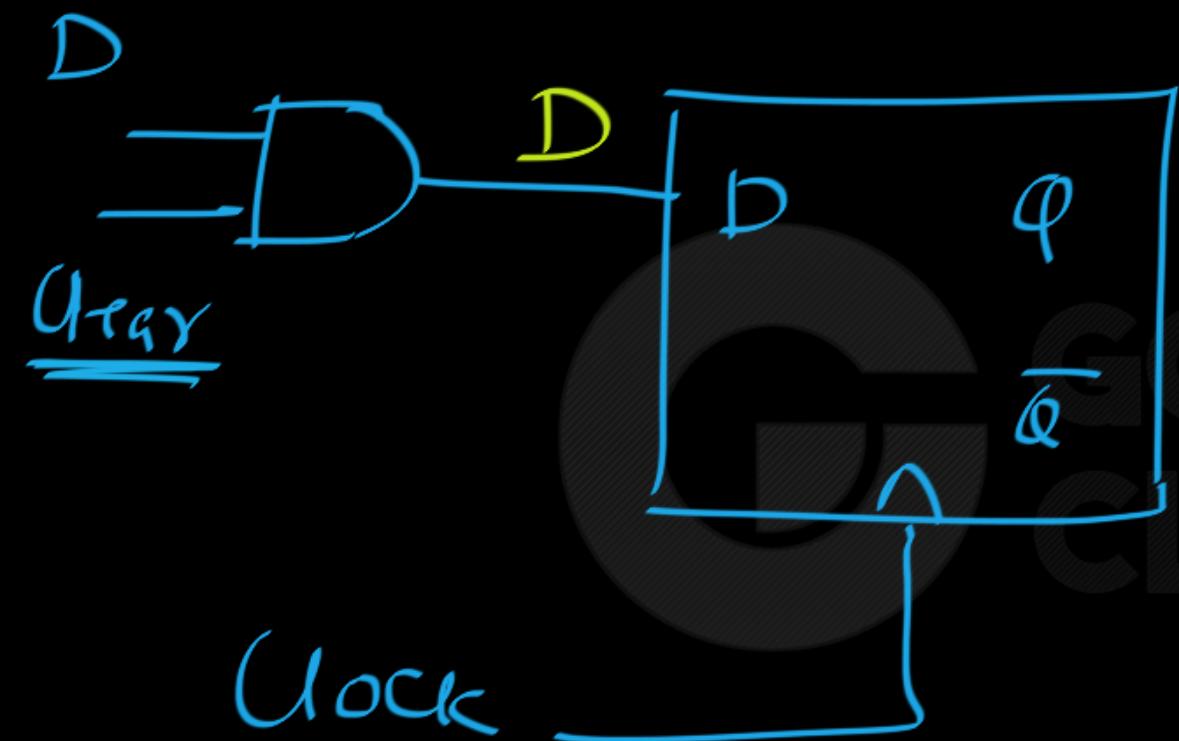
Clear	Q_n	D
0	0	0
1	D	D

$$\underline{D = D \cdot \text{Clear}}$$

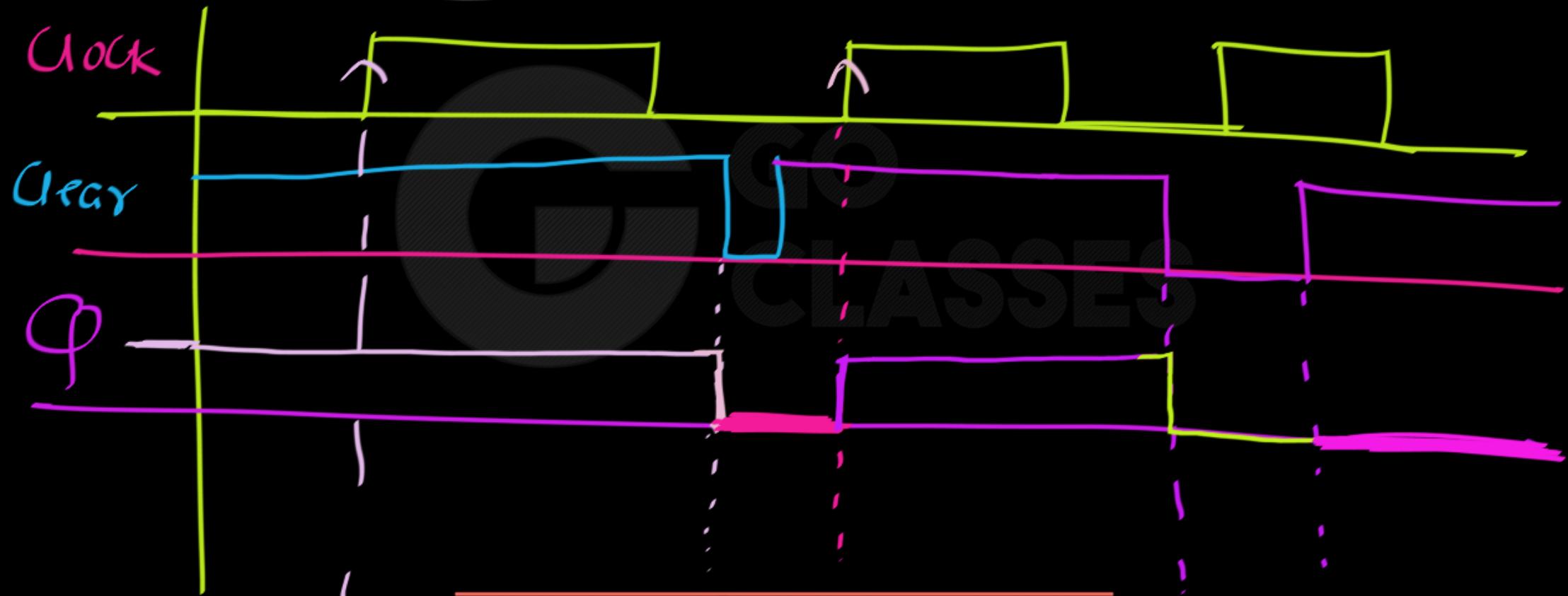


When Clear = 0

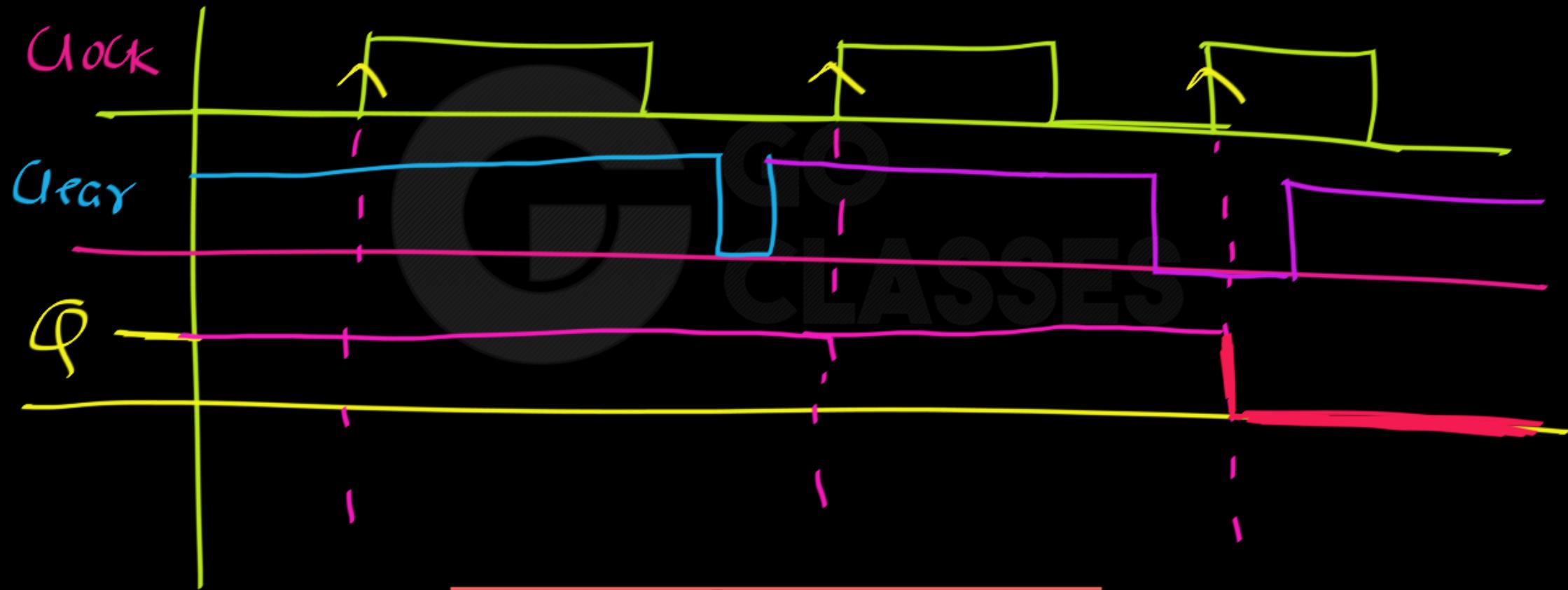
$Q = 0$ when
Clock \uparrow



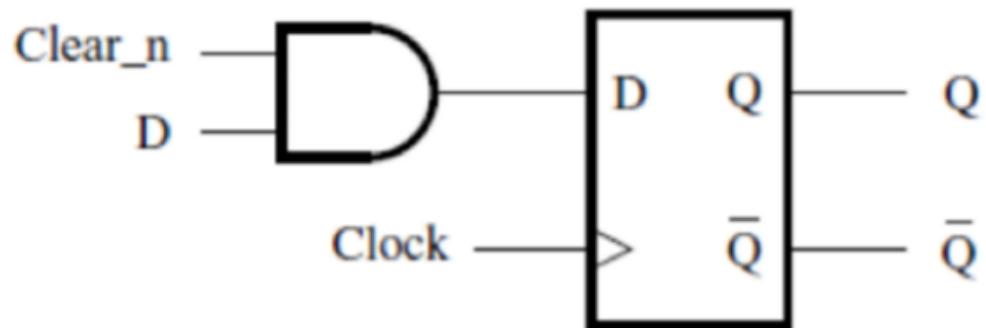
When Clear = 1
Normal D-ff behavior

D - ffAsynch clear :

D - ff Synch clear :



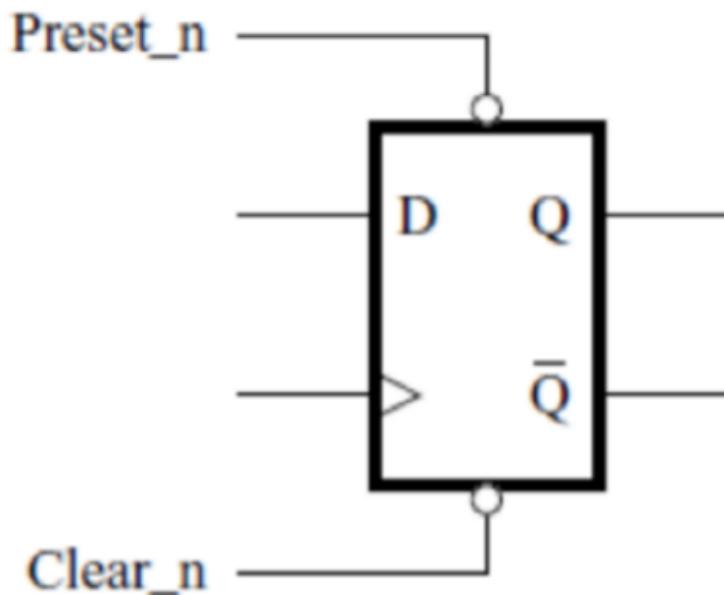
Positive-edge-triggered D flip-flop with Synchronous Clear



(c) Adding a synchronous clear

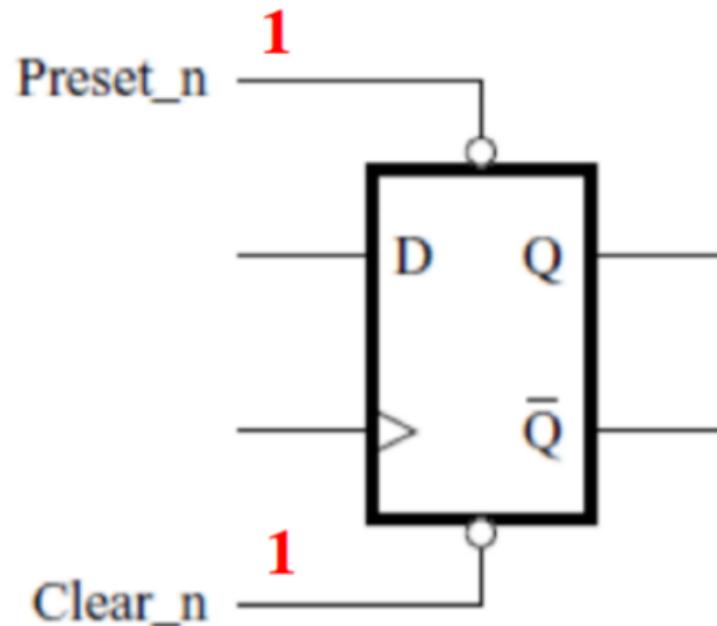
The output Q can be cleared only on the positive clock edge.

Positive-edge-triggered D flip-flop with asynchronous Clear and Preset



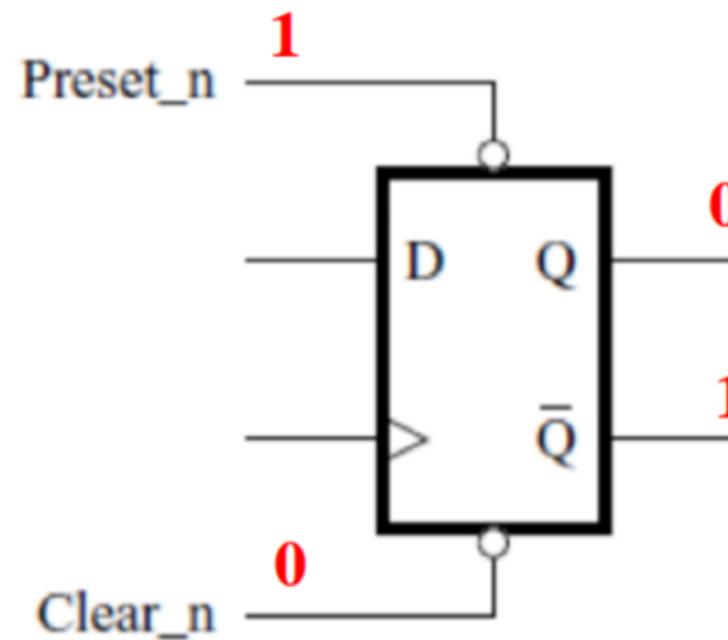
(b) Graphical symbol

For normal operation both must be set to 1



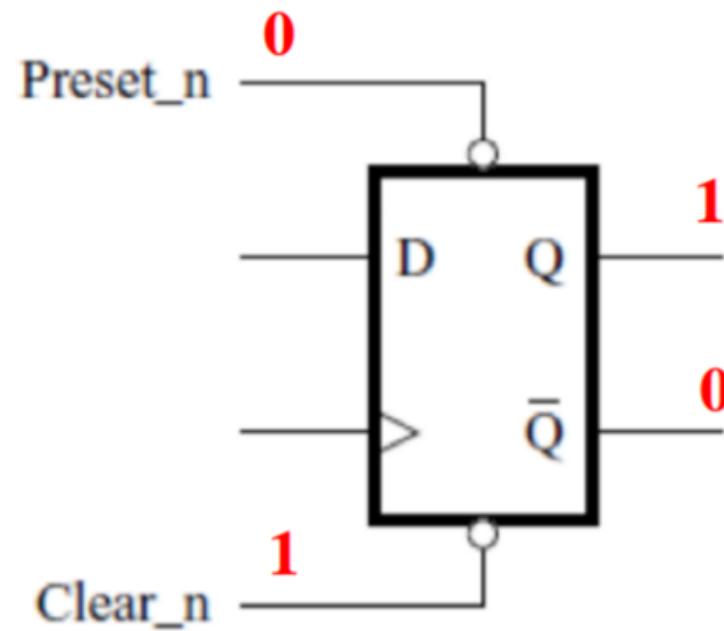
(b) Graphical symbol

A zero on clear_n drives the output Q to zero



(b) Graphical symbol

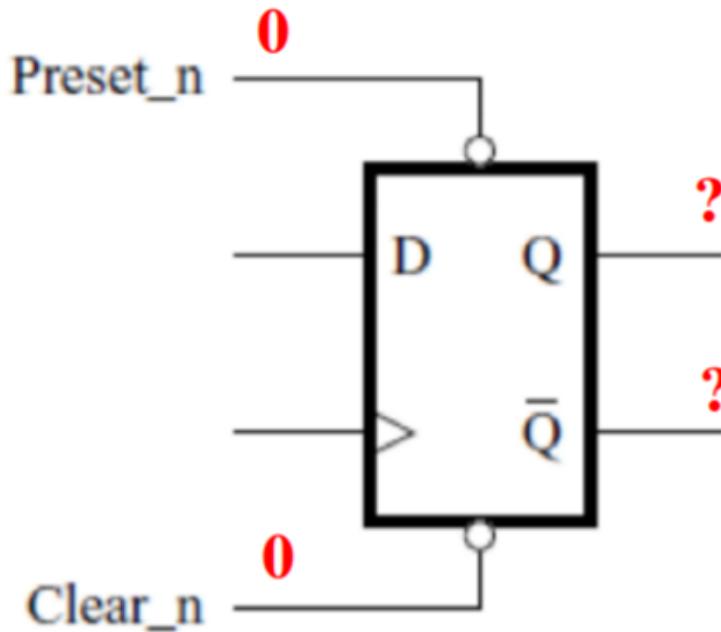
A zero on preset_n drives the output Q to one



(b) Graphical symbol

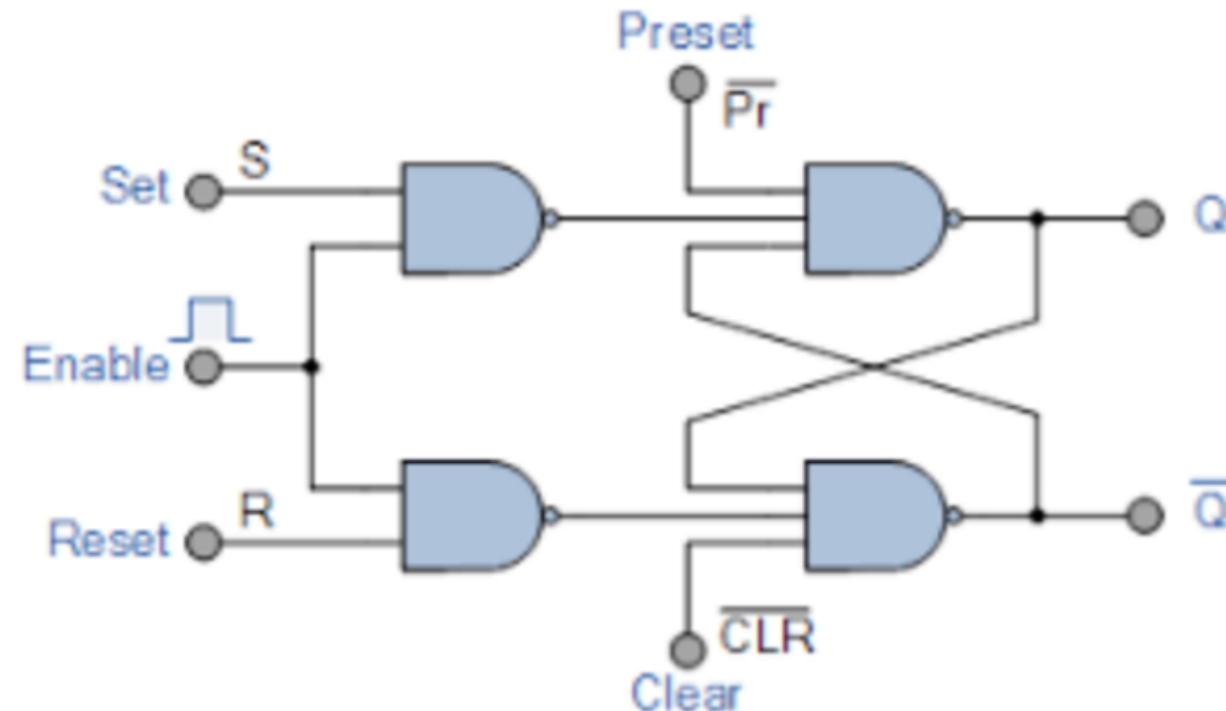
The output is indeterminate if both are zero

don't ever
use this one

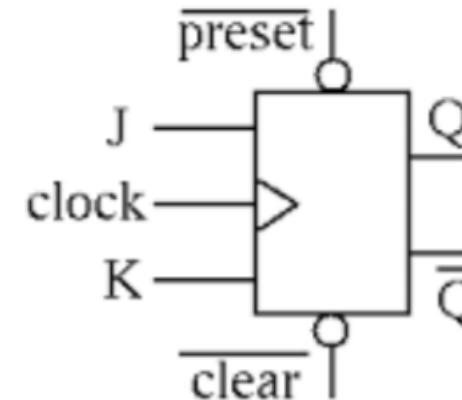
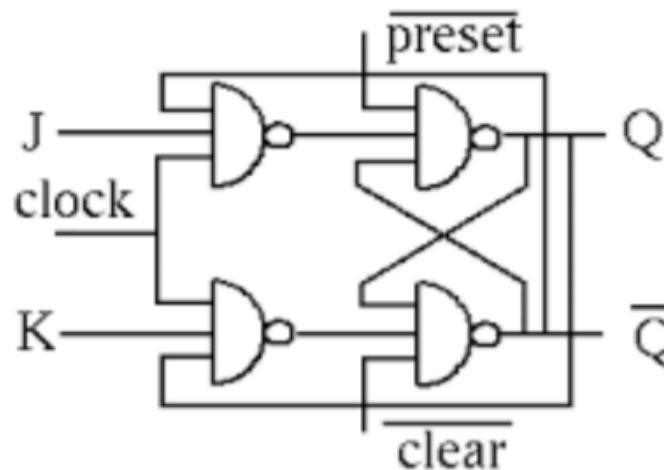


(b) Graphical symbol

SR Flip Flop with Asynchronous Inputs



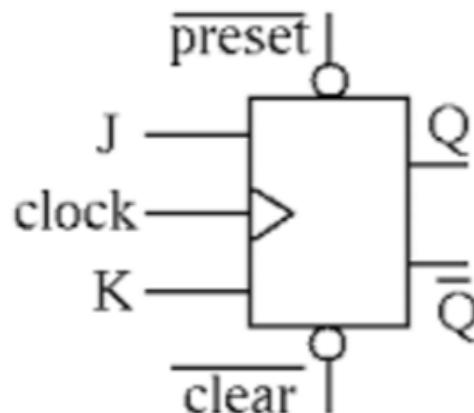
JK Flip Flop with Asynchronous Inputs



J	K	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	\bar{Q}_t

- The Pre and Clr inputs must both be kept High(1) for normal operation of JK flipflop
- If Pre =0 and Clr=1 → Q=1, $Q'=0$ → Set
- If Pre=1 and Clr =0→ Q=0, $Q'=1$ → Reset

JK Flip Flop with
Preset, Clear
(Asynchronous) Inputs :

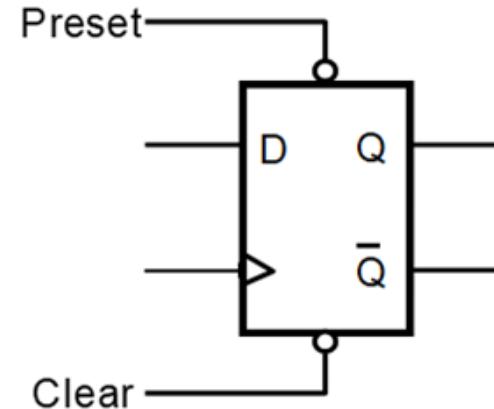
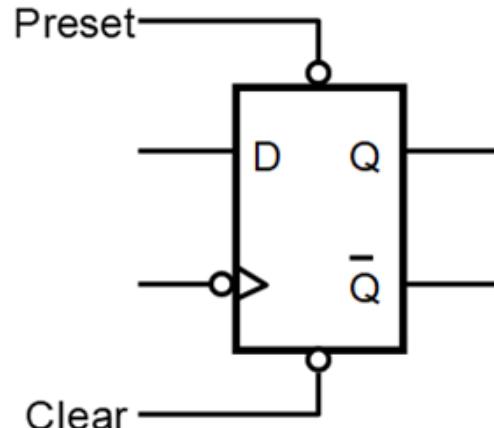


J	K	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	\bar{Q}_t

- The Pre and Clr inputs must both be kept High(1) for normal operation of JK flipflop
- If Pre =0 and Clr=1 $\rightarrow Q=1, Q'=0 \rightarrow$ Set
- If Pre=1 and Clr =0 $\rightarrow Q=0, Q'=1 \rightarrow$ Reset

D Flip-Flops with Clear and Preset (Section 7.4.3)

- D flip-flops are used in computers and other digital components to store bits.
- Sometimes it is desirable to clear ($Q = 0$) and preset ($Q = 1$) them.
- The symbols below are the D flip-flops with a Clear and Preset.
- The NAND gate implementations are shown in the book in Figures 7.13 and 7.14.
- Preset = 0 forces the flip-flop into the state $Q = 1$
- Clear = 0 forces the flip-flop into the state $Q = 0$
- The fact that the Preset and Clear occur when set to 0 is denoted by the inversion symbol (o) on the flip-flop input.



final Conclusion :

By Default :

Pre — Set

Preset → Asynchronous ✓

Clear Active low ✓

Reset \Rightarrow works immediately

- Determine the Q waveform relative to the clock if the signals shown in Fig. 4 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW.

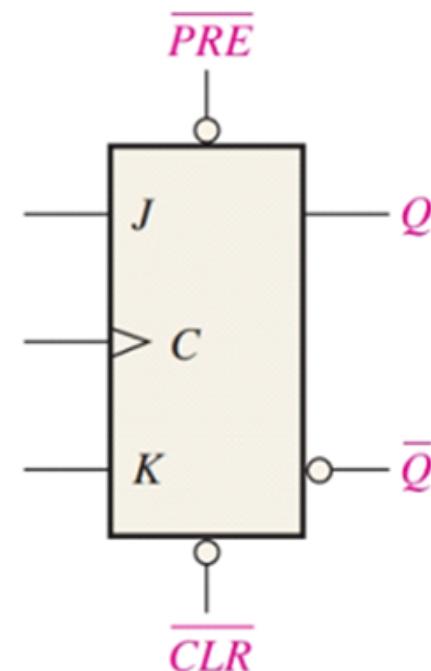
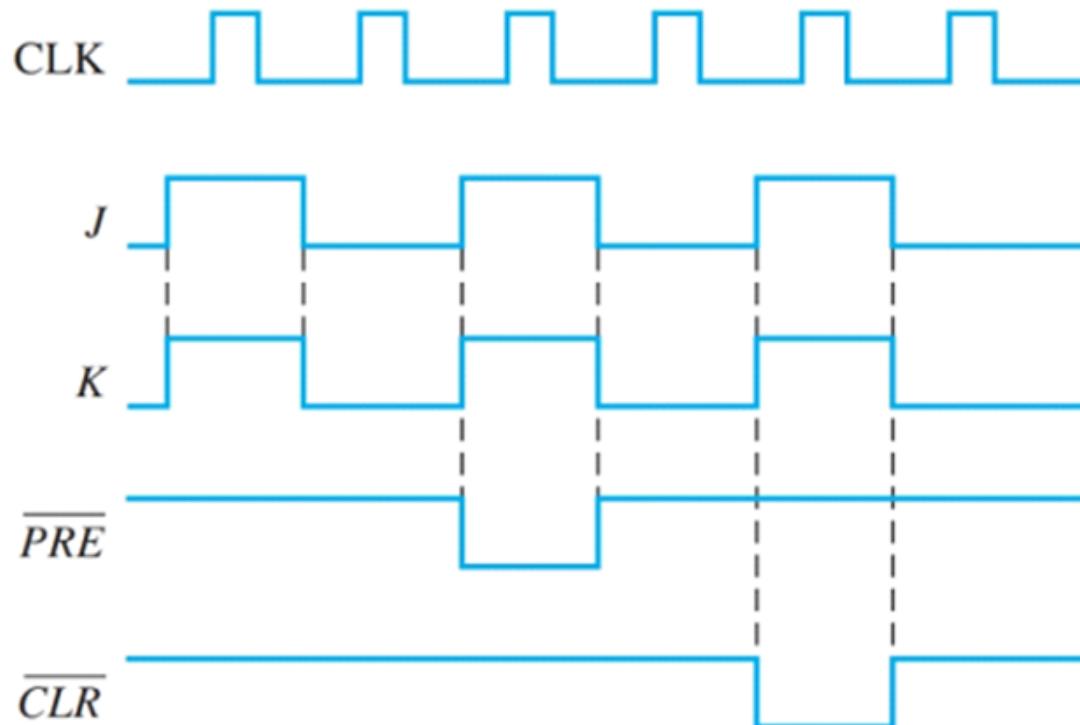
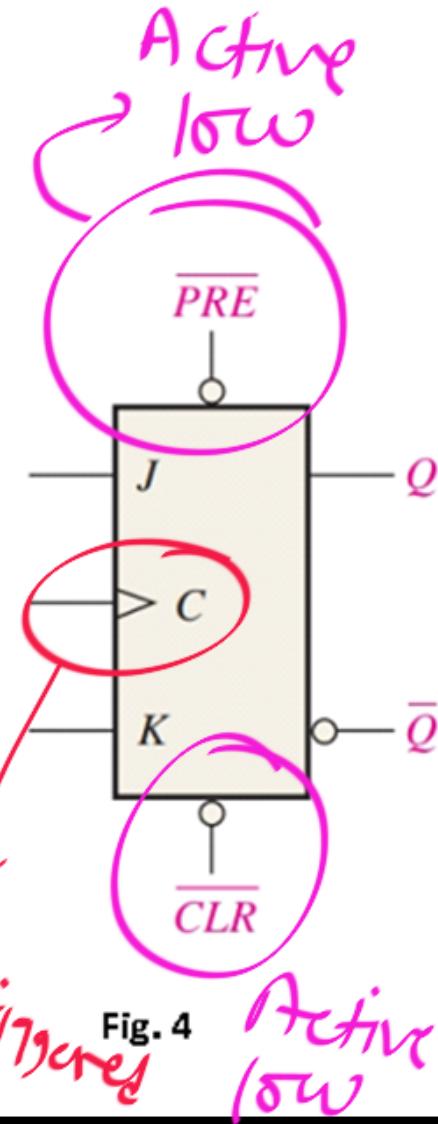
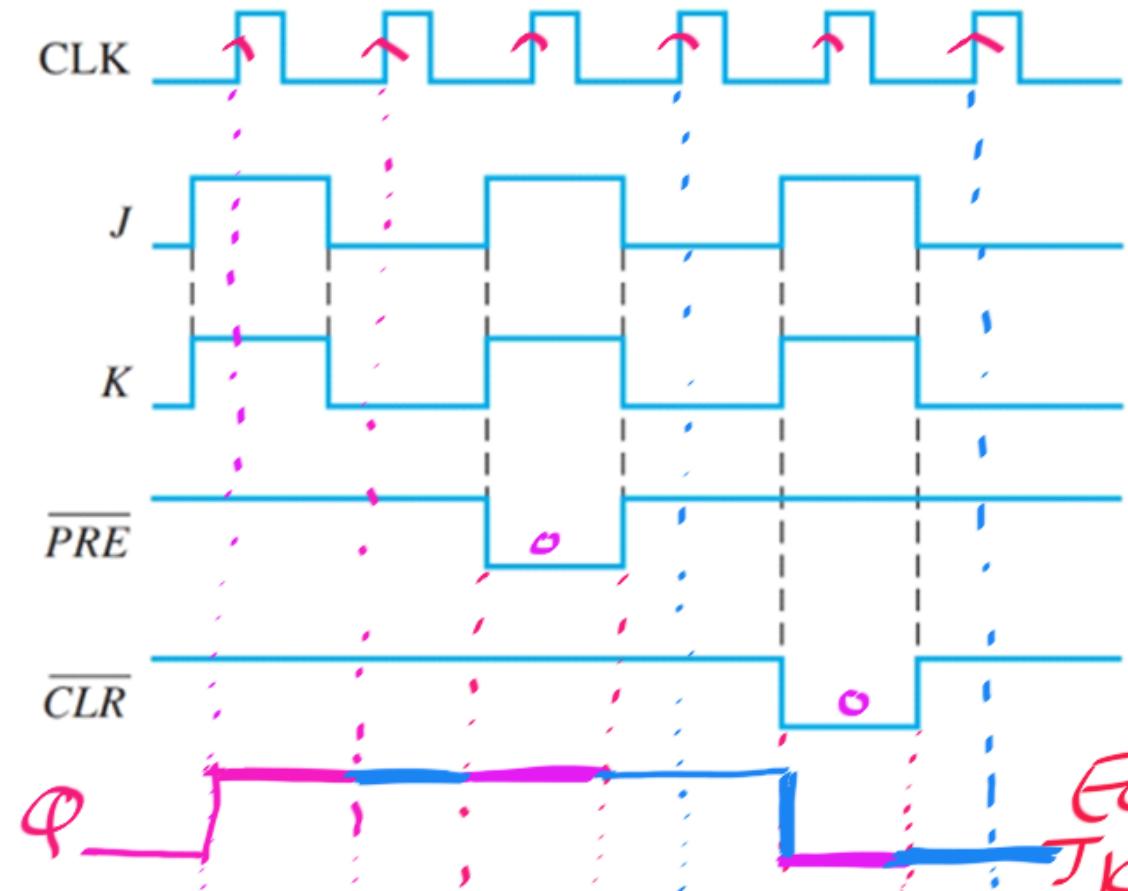


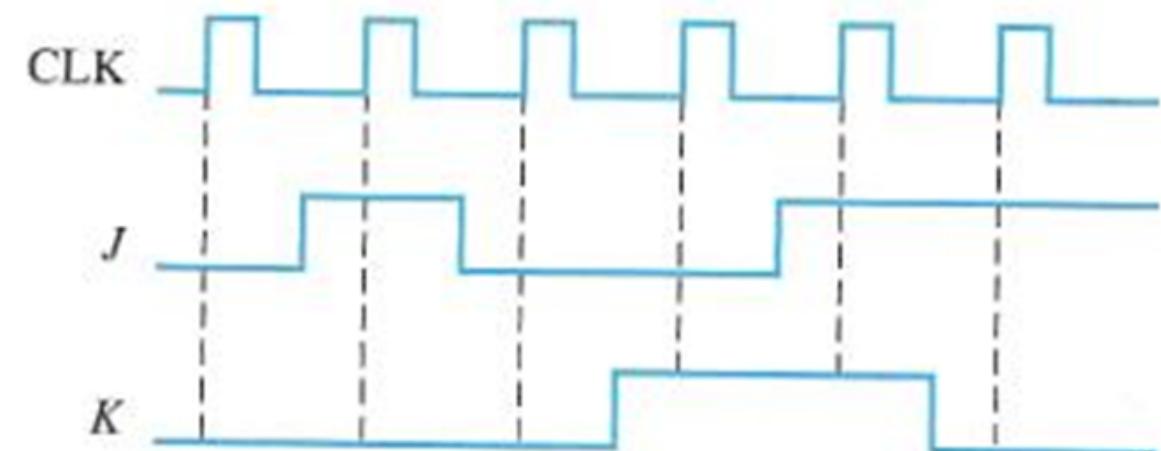
Fig. 4

- Determine the Q waveform relative to the clock if the signals shown in Fig. 4 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW.



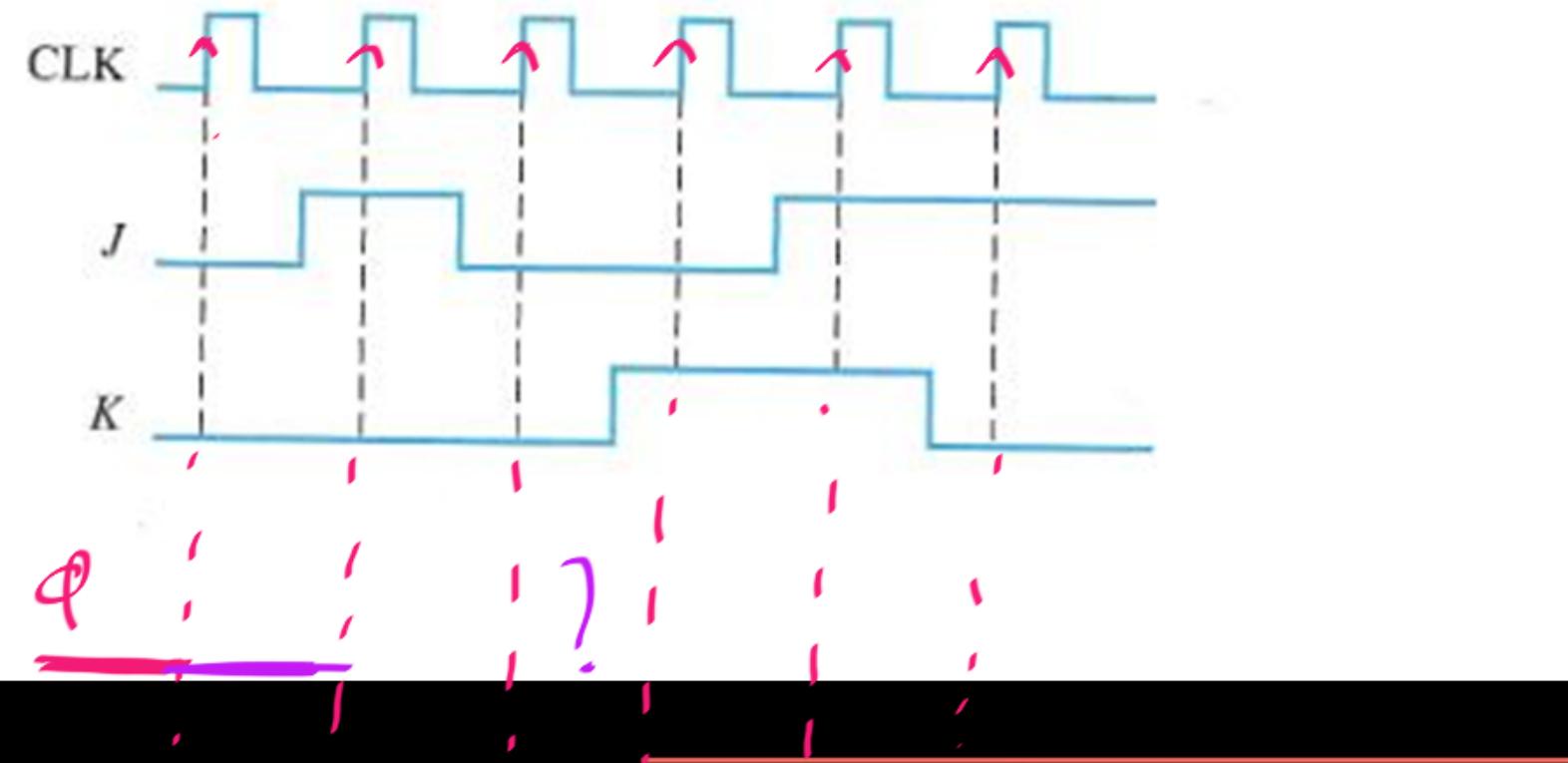


12. For a positive edge-triggered J-K flip-flop with inputs as shown in Figure 8–84, determine the Q output relative to the clock. Assume that Q starts LOW.



12. For a positive edge-triggered J-K flip-flop with inputs as shown in Figure 8–84, determine the Q output relative to the clock. Assume that Q starts LOW.

HW ✓





Asynchronous Preset, Clear :

Override the Clock, inputs
and Do their work immediately.

1. In flip-flops, asynchronous preset and clear inputs generally would:
 - a.) Cause the outputs to change states depending on the SR, JK, or similar controlling inputs
 - b.) Cause the outputs to change states as soon as the input clock makes the desired transition
 - c.) Act as manual overrides that cause the outputs to change states regardless of the inputs or clock transitions
 - d.) Clear the inputs so the flip flop can start over
2. In clocked flip-flops, setup time generally refers to
 - a.) the maximum amount of time that an output must remain stable after an active clock transition.
 - b.) the minimum amount of time that an input must remain stable after an active clock transition.
 - c.) the minimum amount of time than output must remain stable before an active clock transition.
 - d.) the minimum amount of time that an input must remain stable before an active clock transition.
3. A small internal triangle on the clock input of a standard flip-flop symbol that does not have external bubble indicates:
 - a.) The FF is the level active and can only change states when the clock = 1.
 - b.) The FF is an active low device and can only change states when the clock = 0.
 - c.) The FF is transition sensitive and can only change states when the clock goes from 1 to 0.
 - d.) The FF is transition sensitive and can only change states when the clock goes from 0 to 1.



1. In flip-flops, asynchronous preset and clear inputs generally would:
 - a.) Cause the outputs to change states depending on the SR, JK, or similar controlling inputs
 - b.) Cause the outputs to change states as soon as the input clock makes the desired transition
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2. In clocked flip-flops, setup time generally refers to

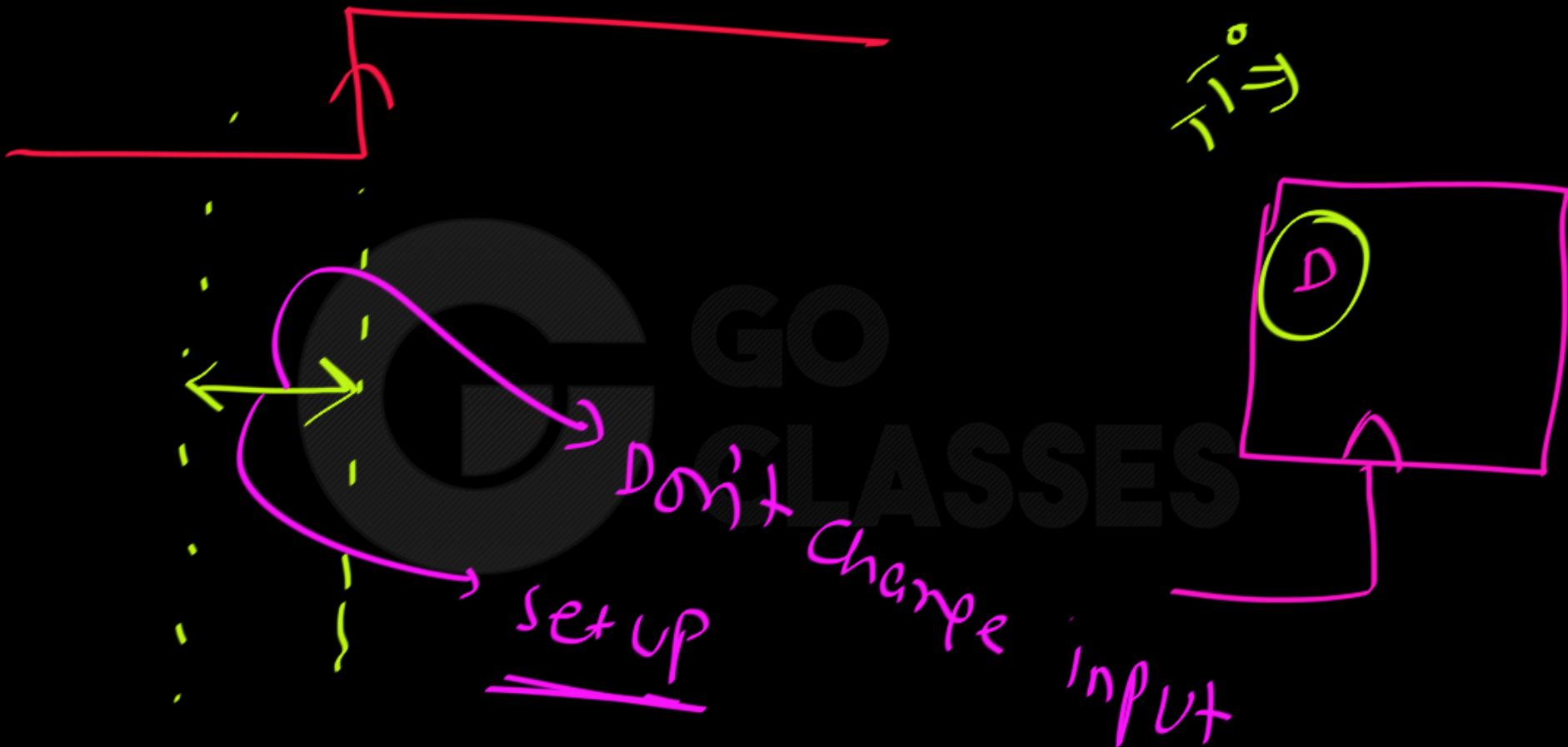
- a.) the maximum amount of time that an output must remain stable after an active clock transition.
 - b.) the minimum amount of time that an input must remain stable after an active clock transition.
 - c.) the minimum amount of time than output must remain stable before an active clock transition.
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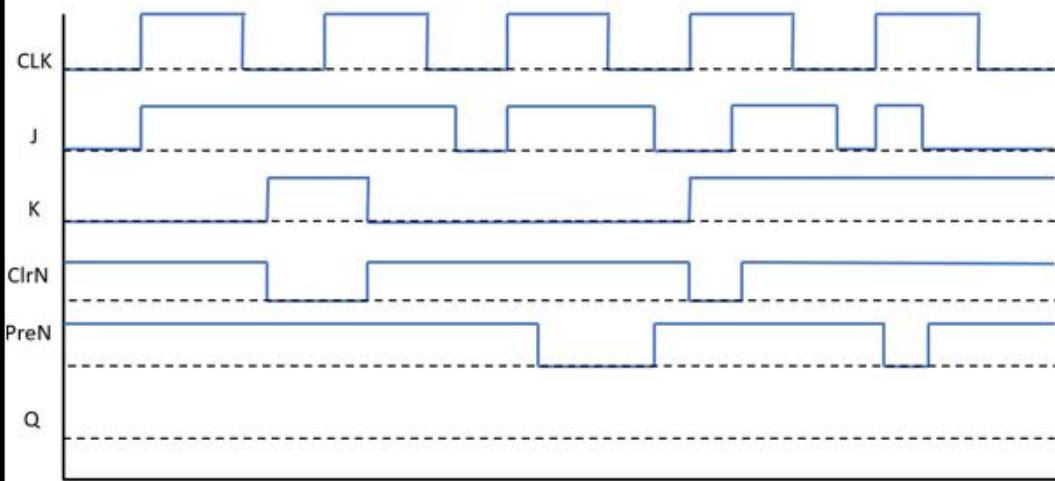
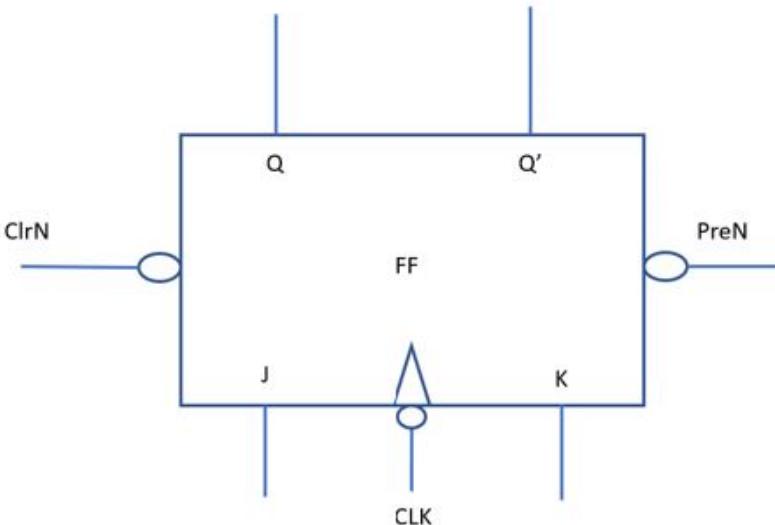
- a.) The FF is the level active and can only change states when the clock = 1.
 - b.) The FF is an active low device and can only change states when the clock = 0.
 - c.) The FF is transition sensitive and can only change states when the clock goes from 1 to 0.
 - d.) The FF is transition sensitive and can only change states when the clock goes from 0 to 1.

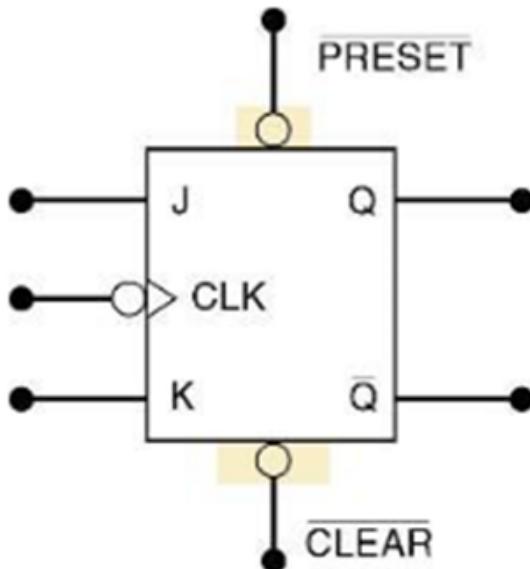
+ve Edge Trig
ff

After
Timing
constraints
Chapter



4. Given the edged-triggered J-K flip-flop with Clear and Preset. Complete the given timing diagram. Assuming initially $Q = 0$.



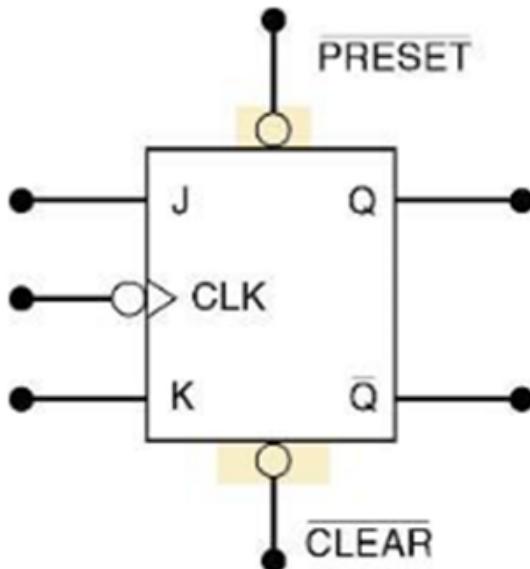


The preset
is true?

$= 1, \bar{Q}_{eq} = 0$

Which of the following is

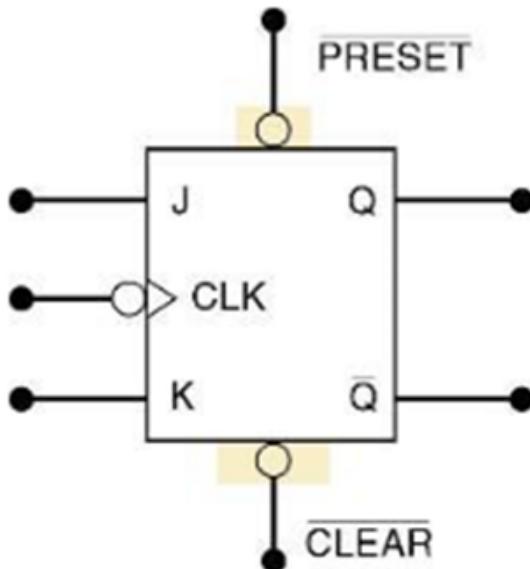
- The Q output is immediately set to 1.
- The flip-flop is free to respond to its J, K, and clock inputs.
- The Q output is in an ambiguous state.
- The Q output is immediately cleared.



The preset
= 1, clear = 0

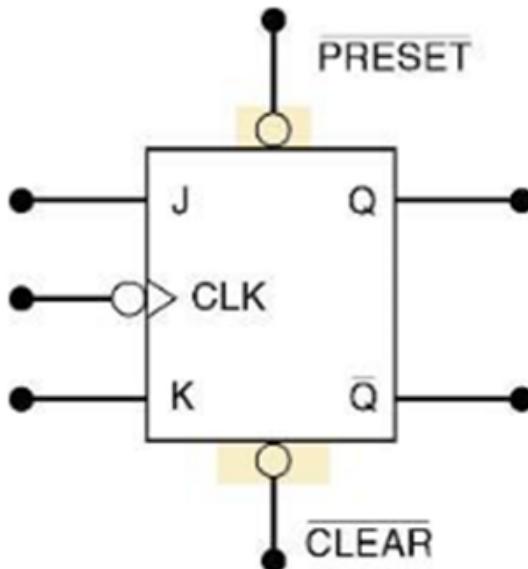
Which of the following is true?

- The Q output is immediately set to 1.
- The flip-flop is free to respond to its J, K, and clock inputs.
- The Q output is in an ambiguous state.
- The Q output is immediately cleared.



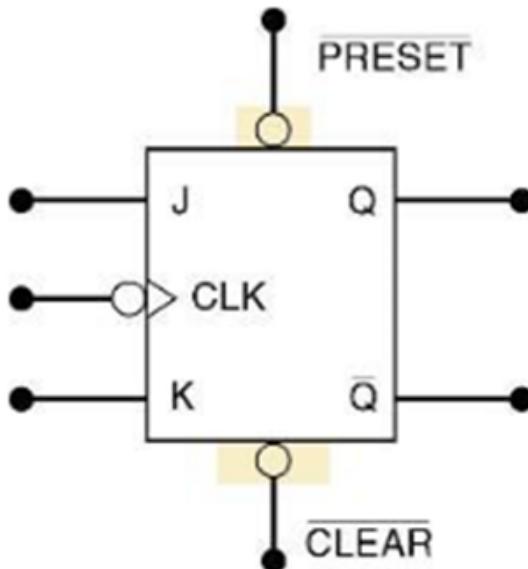
The preset and clear inputs to a J-K flip-flop are Which of the following is true?

- The Q output is immediately set to 1.
- The flip-flop is free to respond to its J, K, and clock inputs.
- The Q output is in an ambiguous state.
- The Q output is immediately cleared.



The preset and clear inputs to a J-K flip-flop are Which of the following is true?

- The Q output is immediately set to 1.
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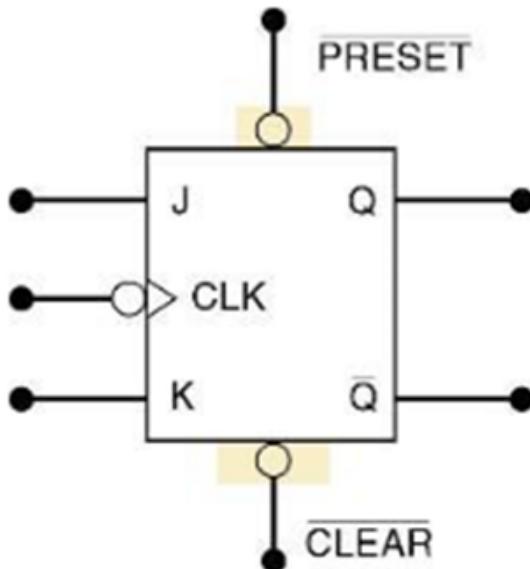


The preset
is 0, and
true?

$= 0, \bar{Q} = 1$

Which of the following is

- The Q output is immediately set to 1.
- The flip-flop is free to respond to its J, K, and clock inputs.
- The Q output is in an ambiguous state.
- The Q output is immediately cleared.

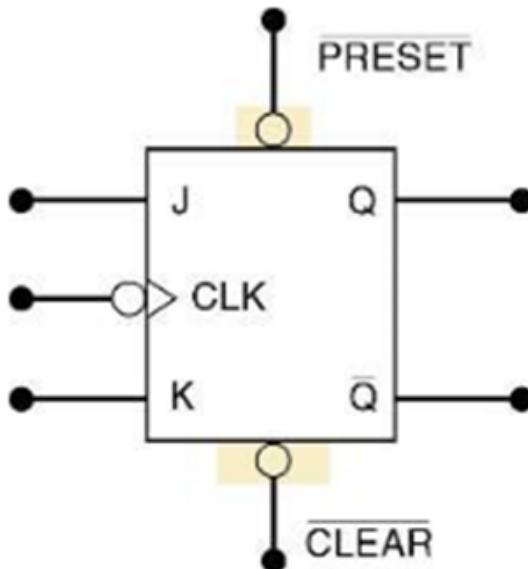


The preset is true?

$= 0, \bar{Q}eq = 1$

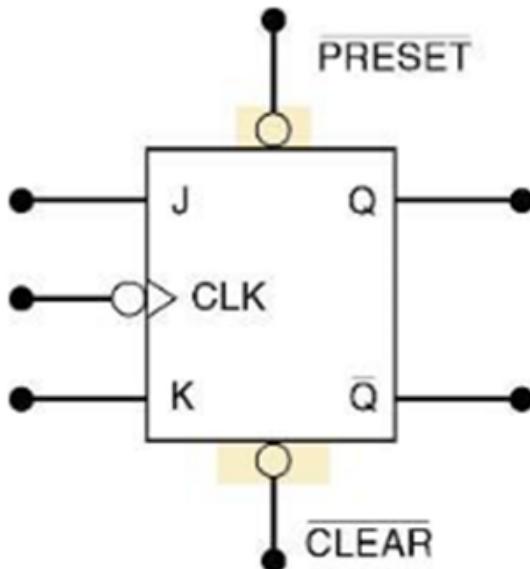
Which of the following is

- The Q output is immediately set to 1.
- The flip-flop is free to respond to its J, K, and clock inputs.
- The Q output is in an ambiguous state.
- The Q output is immediately cleared.



The preset and clear inputs to a J-K flip-flop are HIGH (1). Which of the following is true?

- The Q output is immediately set to 1.
- The flip-flop is free to respond to its J, K, and clock inputs.
- The Q output is in an ambiguous state.
- The Q output is immediately cleared.

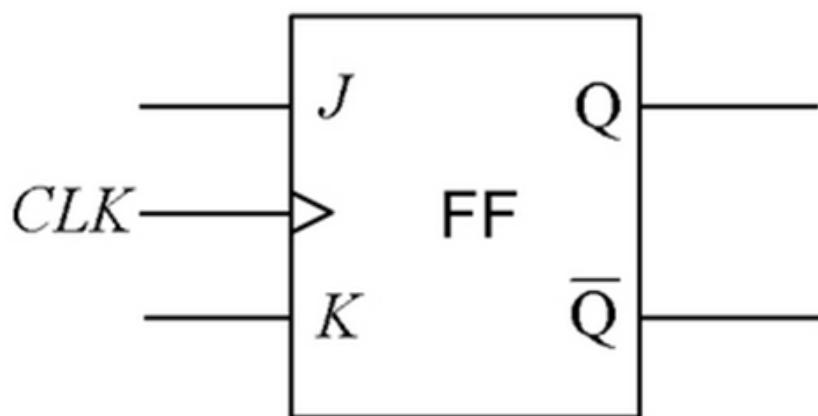


The preset and clear inputs to a J-K flip-flop are HIGH (1). Which of the following is true?

- The Q output is immediately set to 1.
- The flip-flop is free to respond to its J, K, and clock inputs.
- The Q output is in an ambiguous state.
- The Q output is immediately cleared.

QUESTION 11

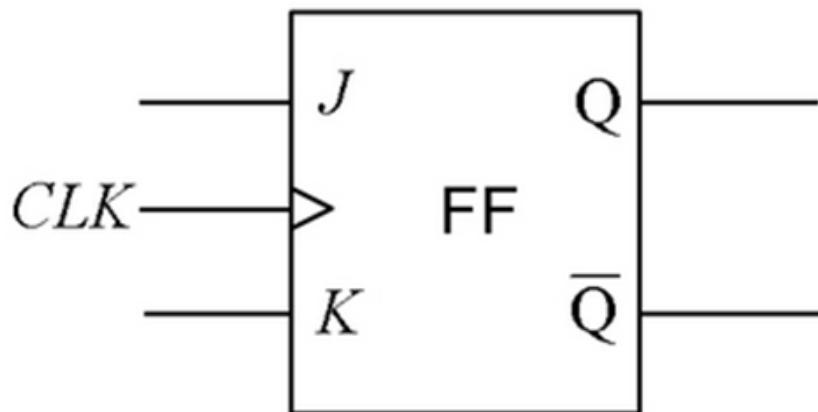
A JK flip flop is shown below. If inputs $J=1$ and $K=1$, what will happen on the next active clock edge?



- The Q output will toggle.
- The Q output will be 1.
- The Q output will be 0.
- There will be no change to the Q output.

QUESTION 11

A JK flip flop is shown below. If inputs $J=1$ and $K=1$, what will happen on the next active clock edge?



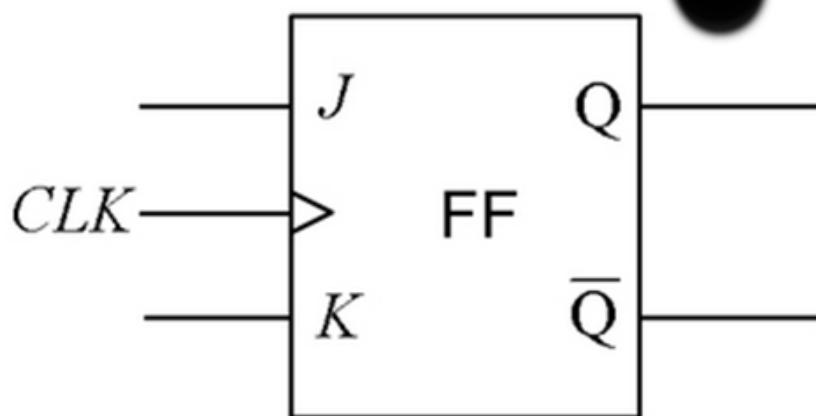
$k=1$

The Q output will toggle.

- The Q output will be 1.
- The Q output will be 0.
- There will be no change to the Q output.

QUESTION 11

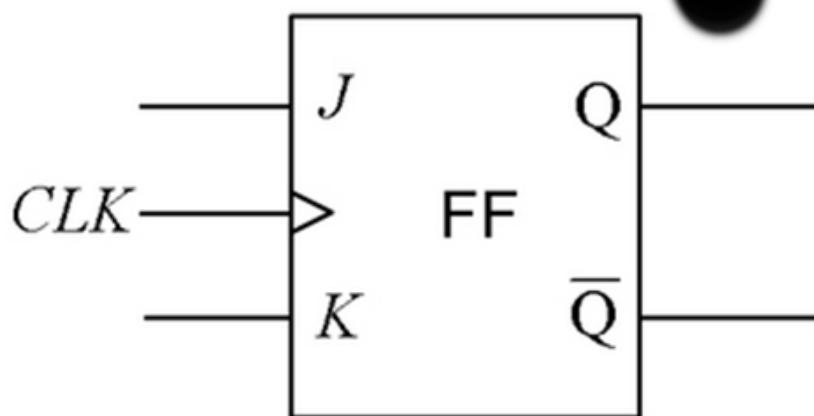
A JK flip flop is shown below. If inputs $J=1$ and $K=0$ what will happen on the next active clock edge?



- The Q output will toggle.
- The Q output will be 1.
- The Q output will be 0.
- There will be no change to the Q output.

QUESTION 11

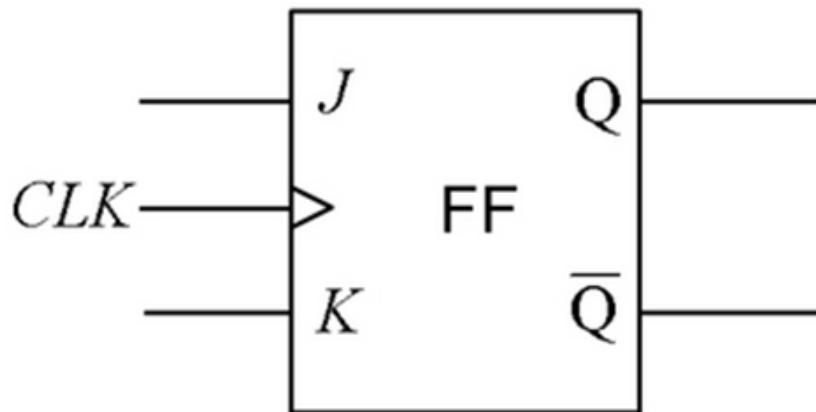
A JK flip flop is shown below. If inputs $J=1$ and $K=0$ what will happen on the next active clock edge?



- The Q output will toggle.
- The Q output will be 1.
- The Q output will be 0.
- There will be no change to the Q output.

QUESTION 11

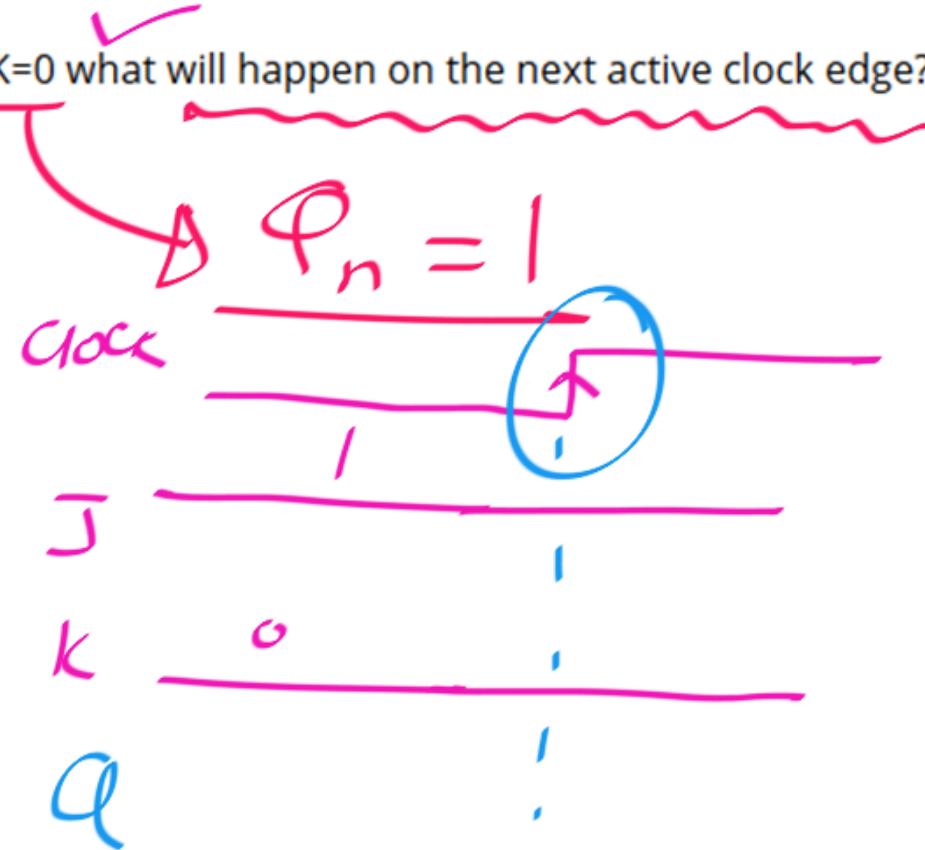
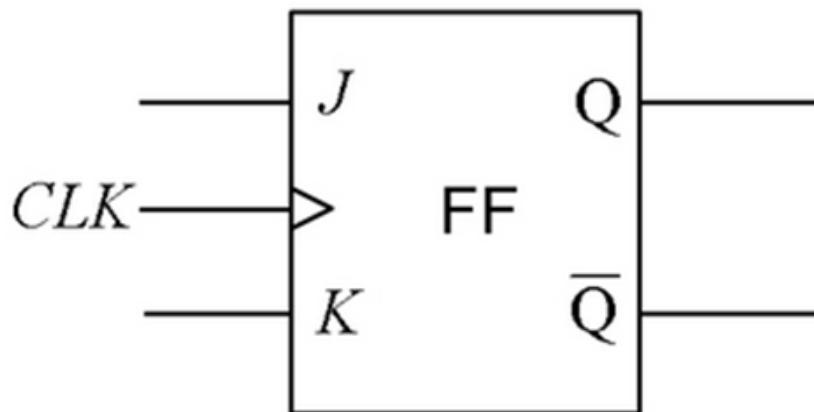
A JK flip flop is shown below. If inputs $J=1$ and $K=0$ what will happen on the next active clock edge?



- The Q output will toggle.
- The Q output will be 1.
- The Q output will be 0.
- There will be no change to the Q output.

QUESTION 11

A JK flip flop is shown below. If inputs $J=1$ and $K=0$ what will happen on the next active clock edge?



- The Q output will toggle.
- The Q output will be 1.
- The Q output will be 0.
- There will be no change to the Q output.



The preset and clear inputs don't need synchronization?

- a. True only for JK flip -flop
- b. True only for JK and D Flip flops
- c. True for all Flip-flops
- d. False



The preset and clear inputs don't need synchronization?

- a. True only for JK flip-flop
- b. True only for JK and D flip-flops
- c. True for all flip-flops
- d. False

Not in sync
with clock.



In which flip flop the present input will be the next output?

- a. S-R
- b. J-K
- c. D
- d. T





In which flip flop the present input will be the next output?

- a. S-R
- b. J-K
- c. D
- d. T

Date flip-flop