



# Lecture 40 :

## Sequential Circuits

# Master-Slave Flipflops

# Race Condition in JK, T



# Recap:

# Flipflops



# FlipFlop

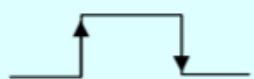
- The memory elements used in clocked sequential circuits are called flipflops. These circuits are binary cells capable of storing one bit of information.
- A flipflop circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states
- A bi stable device
- Have two outputs one complement of another
- Applications of Flipflops
  - Counters
  - Shift Registers
  - Storage Registers
  - Frequency Dividers

- Latches and Flip-Flops are devices that can have two internal states (0,1)
- The output of a latch or a Flip-Flop (FF) is dependent upon its
  - CURRENT STATE
  - CURRENT INPUTS.
- Latches and FFs are the simplest examples of sequential systems.
- State transitions based on

→ levels



→ edges

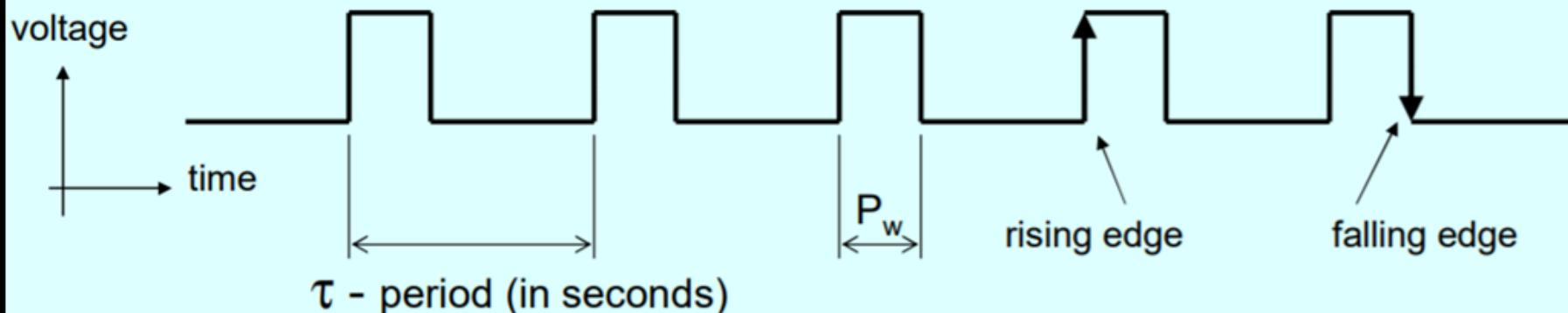




A flip-flop holds 1 bit.  
Bit = binary digit

CLASSES

## A Clock Waveform



f - frequency pulse width (in Hertz)

$P_w$  - pulse width (in seconds)

$$f = 1/\tau$$

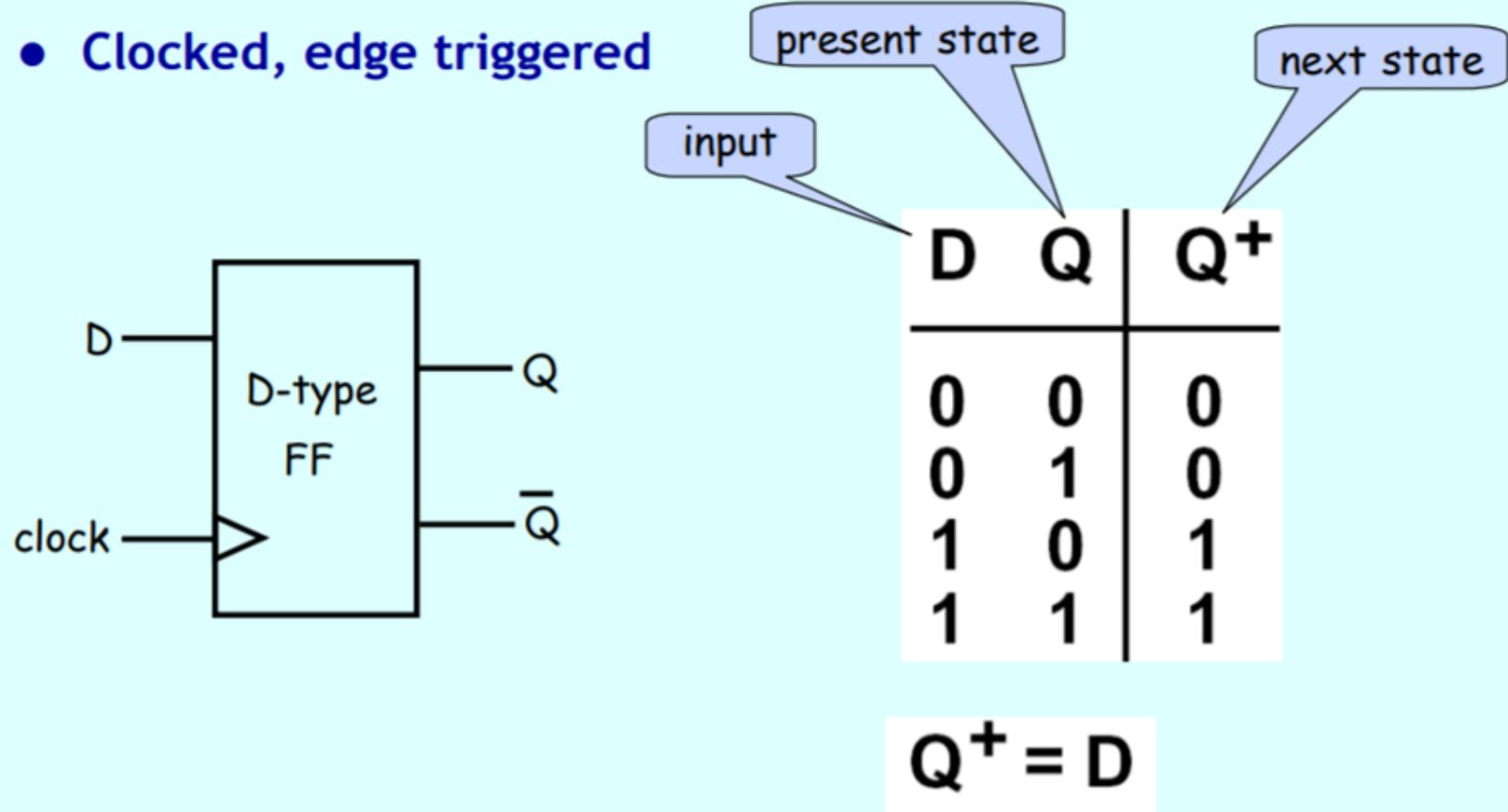
duty cycle - ratio of pulse width to period (in %)

$$\text{duty cycle} = P_w / \tau$$

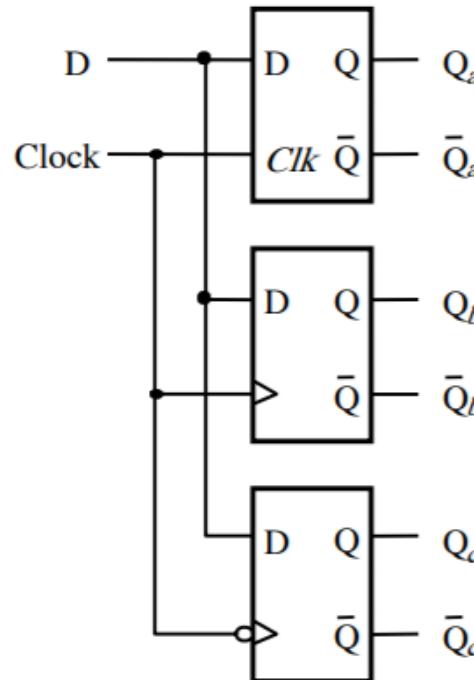
millisecond (ms) $10^{-3}$	Kilohertz (KHz) $10^3$
microsecond ( $\mu$ s) $10^{-6}$	Megahertz (MHz) $10^6$
nanosecond (ns) $10^{-9}$	Gigahertz (GHz) $10^9$

# D-type Flip-Flop

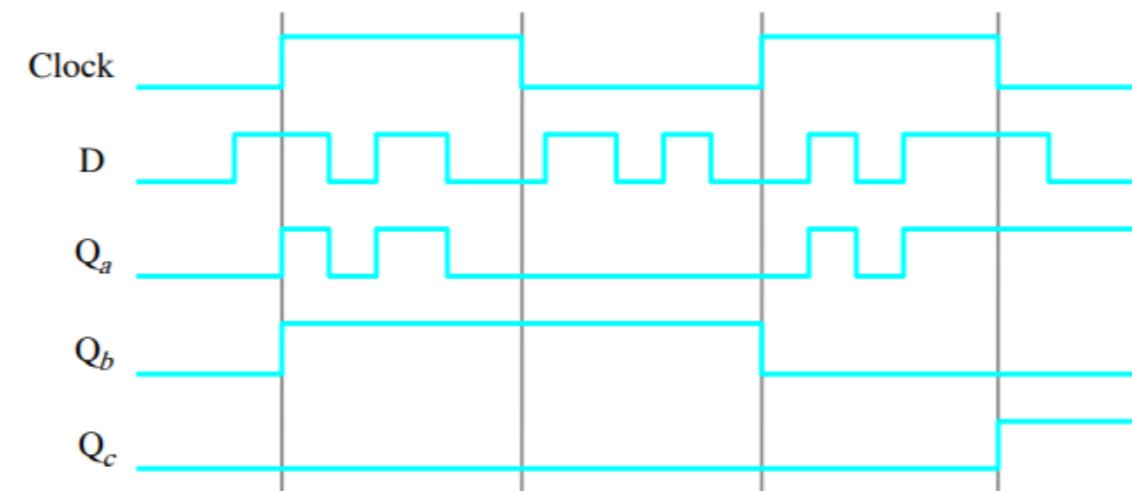
- Clocked, edge triggered

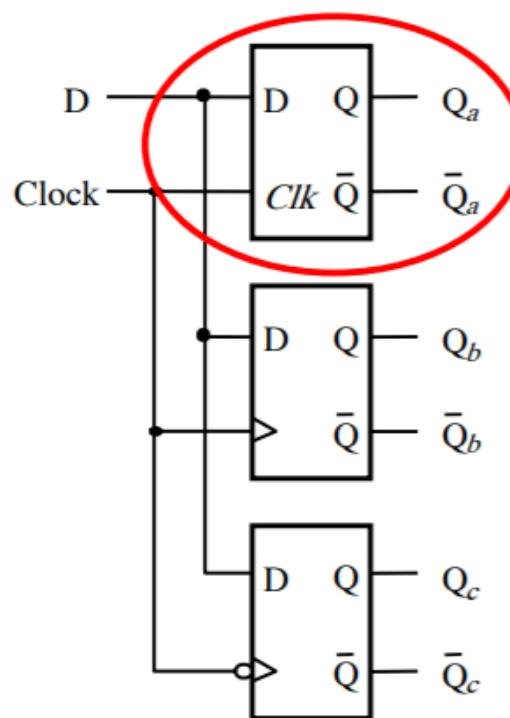


The next state in response to the rising edge of the clock is equal to the D input before the rising edge



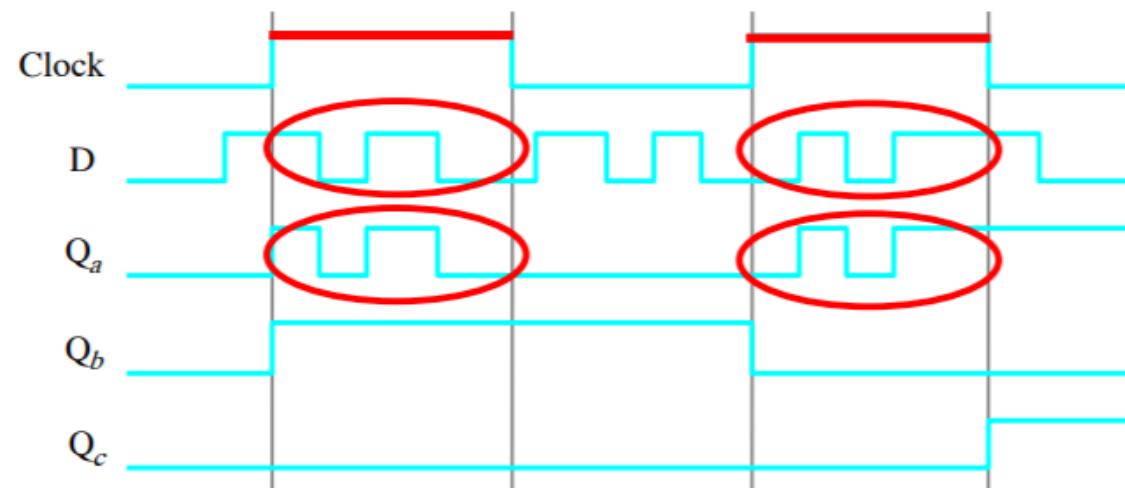
## Comparison of level-sensitive and edge-triggered D storage elements

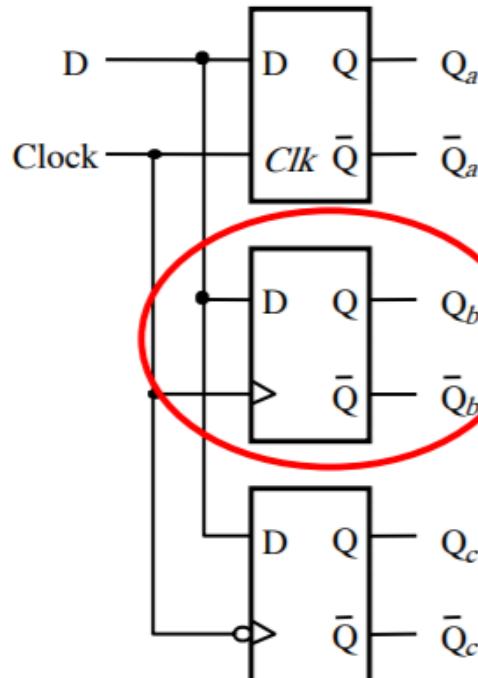




## Comparison of level-sensitive and edge-triggered D storage elements

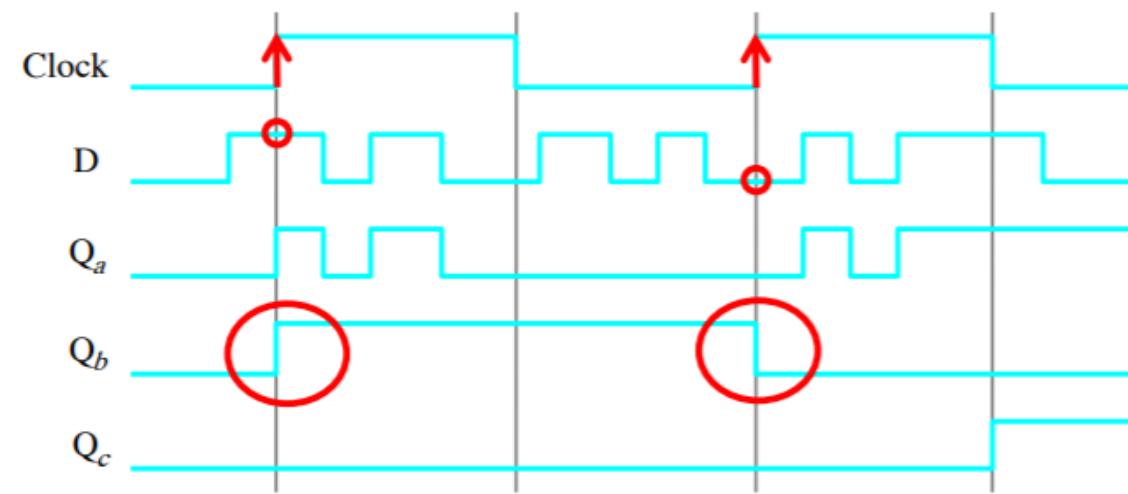
The D Latch is Level-Sensitive  
(the output mirrors the D input when  $Clk=1$ )

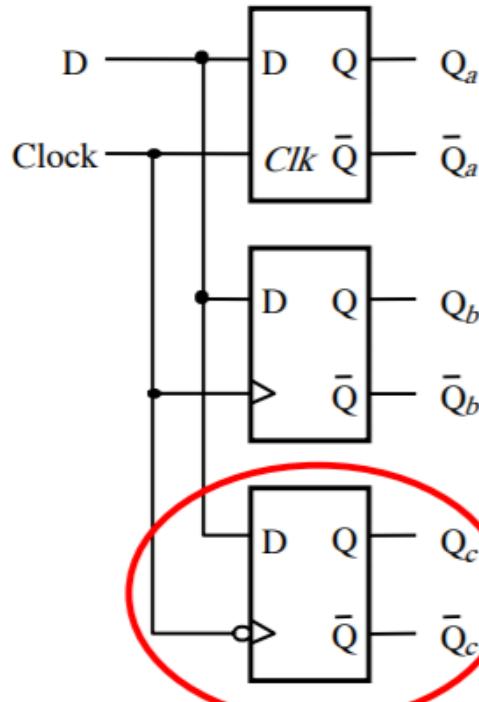




## Comparison of level-sensitive and edge-triggered D storage elements

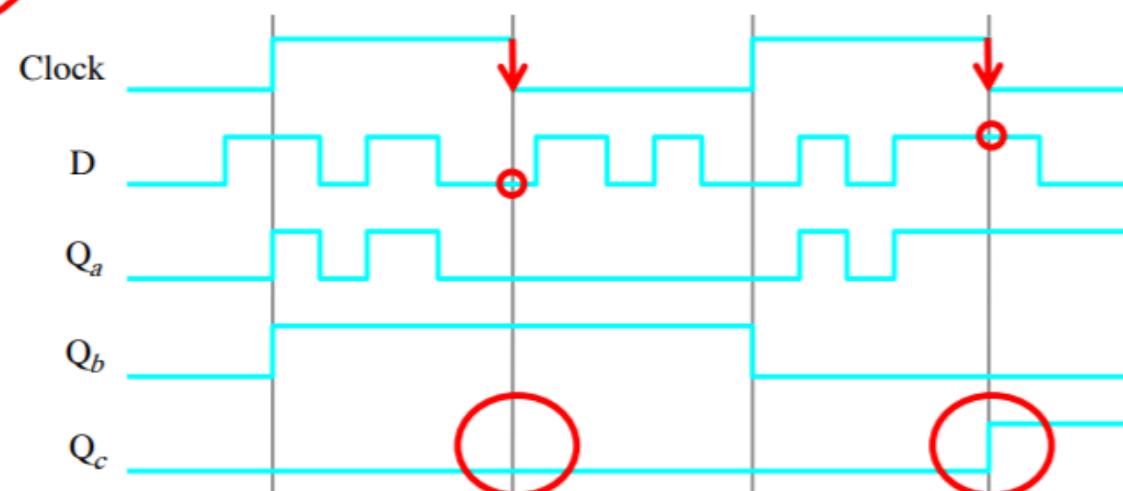
Positive-edge-triggered D Flip-Flop  
(the output is equal to the value of D right at the positive edge of the clock signal)





## Comparison of level-sensitive and edge-triggered D storage elements

Negative-edge-triggered D Flip-Flop  
(the output is equal to the value of D right at the negative edge of the clock signal)





Any flip flop :

- ① +ve level Triggered / Sensitive ff
  - ② -ve " "
  - ③ +ve Edge " "
  - ④ -ve " "
- } Possible Designs

SR flip flop:

- ① +ve level Triggered / Sensitive SR ff
  - ② -ve " "
  - ③ +ve Edge " "
  - ④ -ve " "
- SR " "      SR " "      SR " "
- possible designs

Implementation of any FF as a +ve level Triggered flipflop :

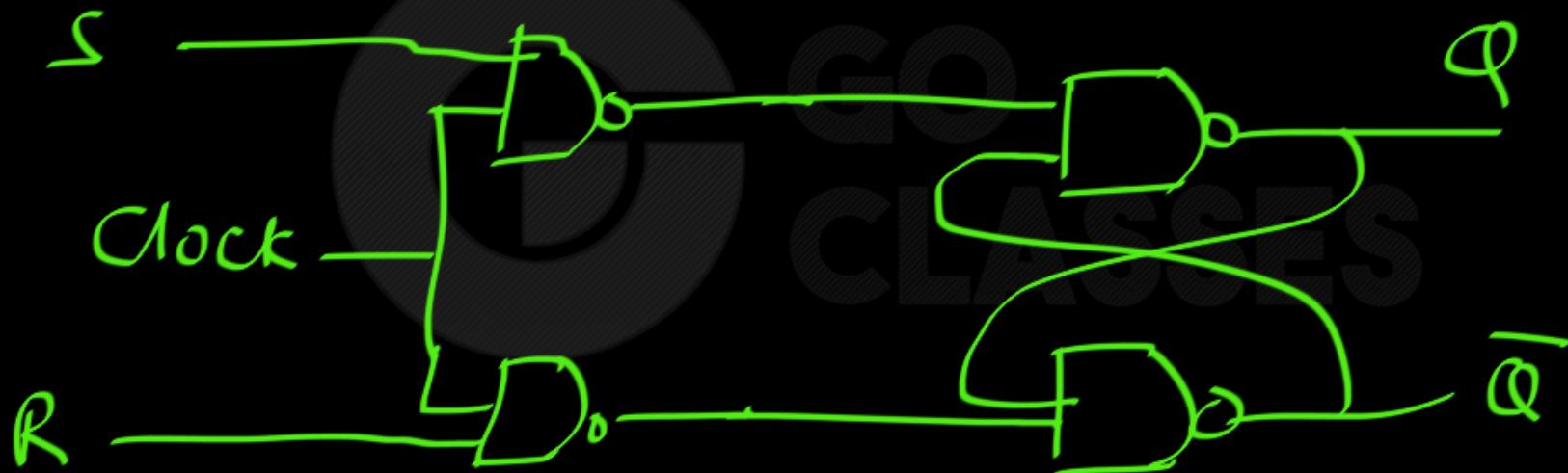
The (Basic) implementation we have already seen are +ve level Triggered flipflops.



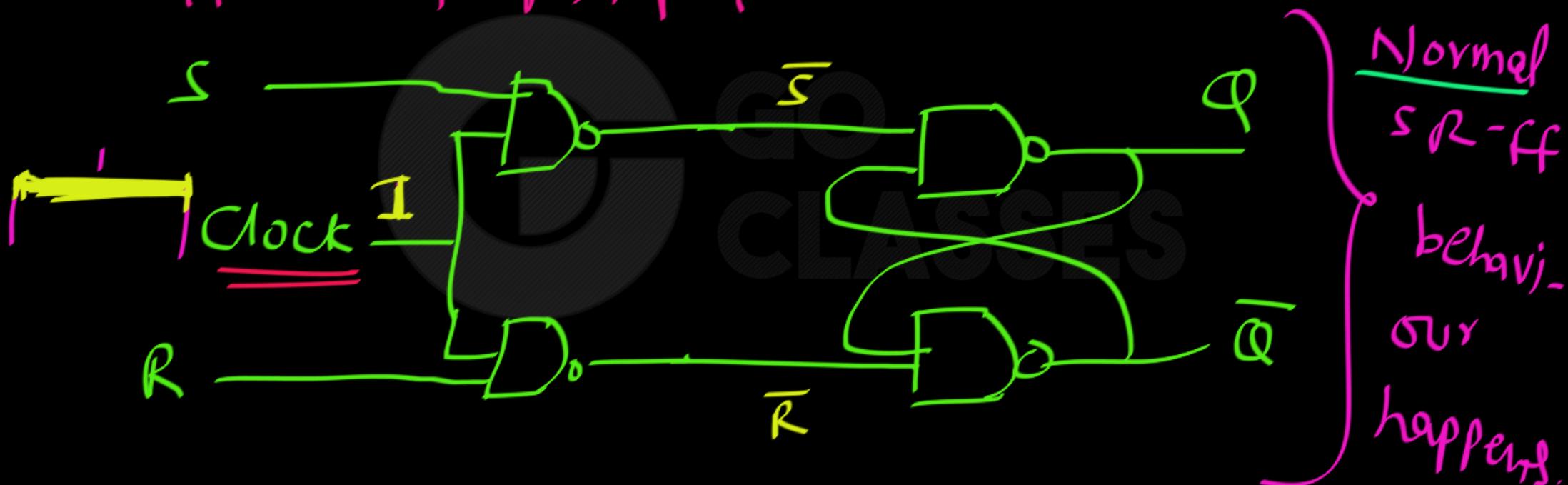
Implementation of SR-FF as a +ve level Triggered flipflop :

The (Basic) implementation we have already seen are +ve level Triggered flipflops.

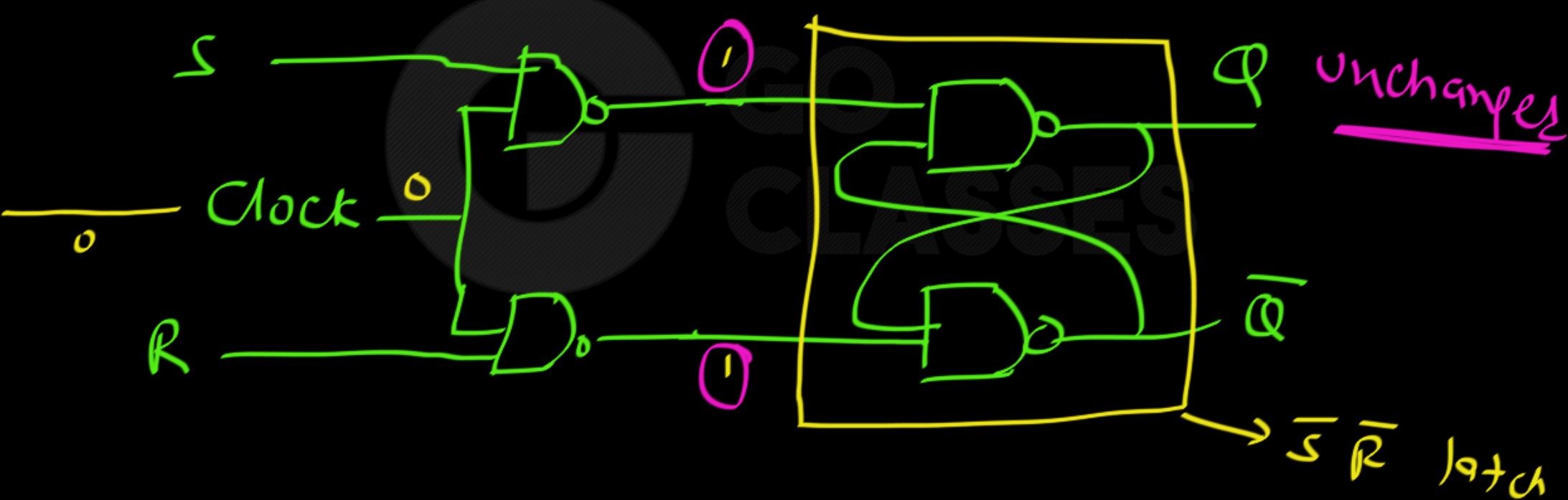
Implementation of SR-FF as a +ve level Triggered flip flop :



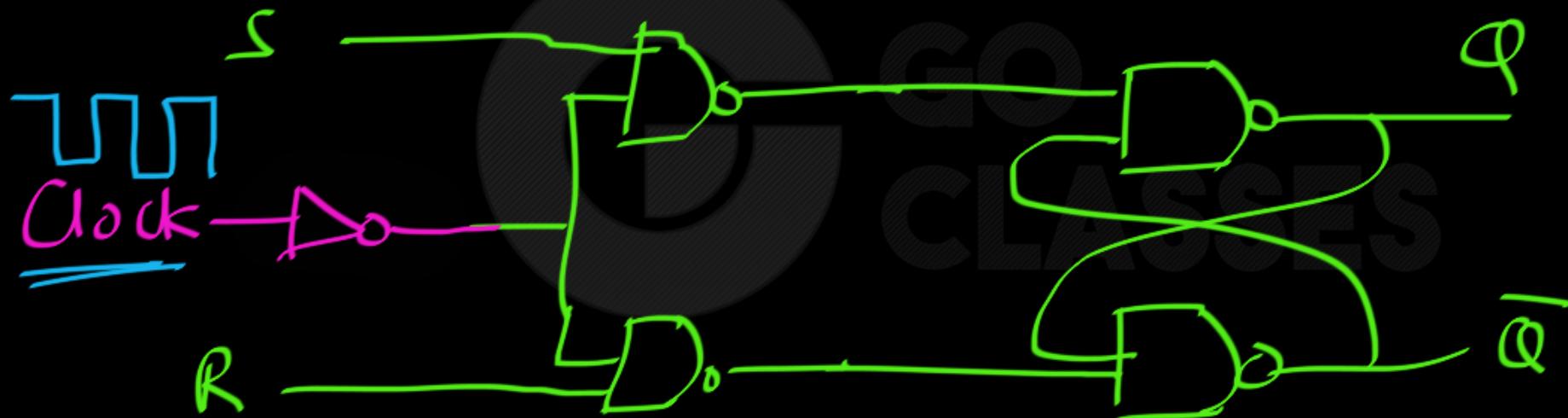
Implementation of SR-FF as a +ve level Triggered flip flop :



Implementation of SR-FF as a +ve level Triggered flip flop :



Implementation of SR-FF as a -Ve level Triggered flip flop :



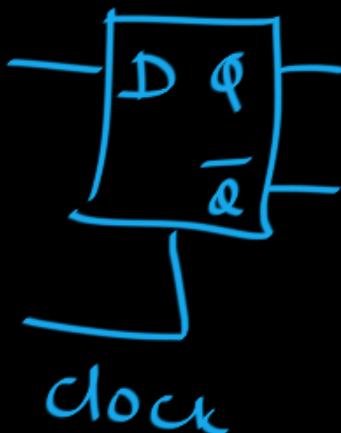
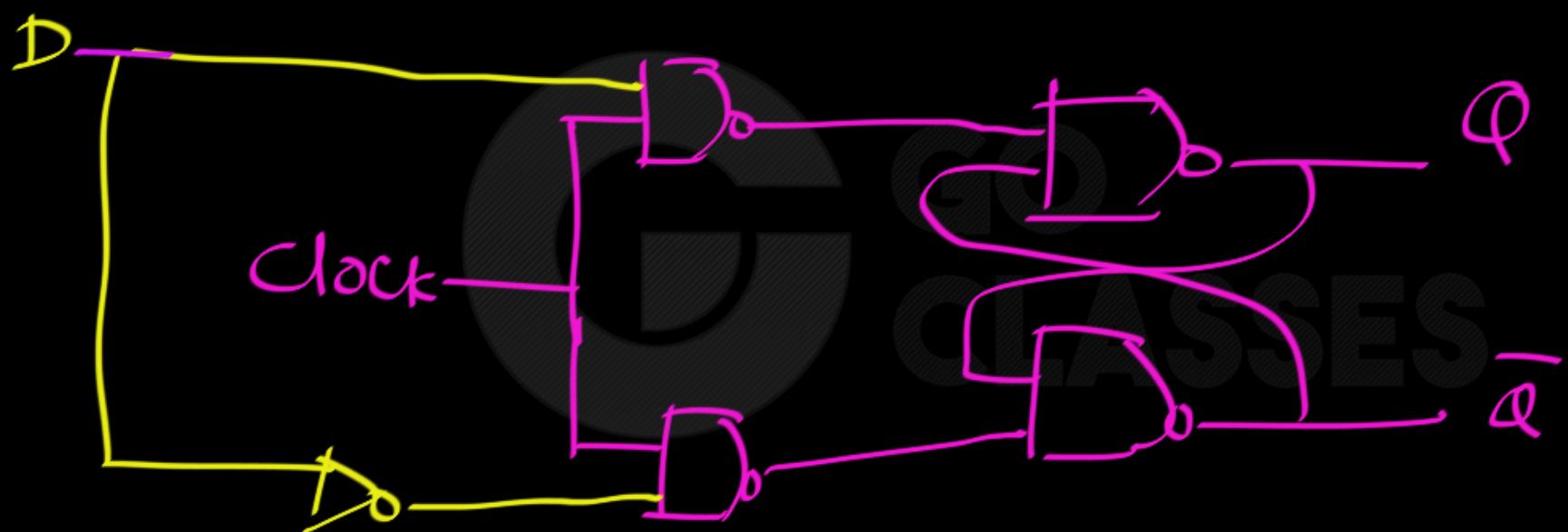


Any flip flop ( SR, JK, T, D )

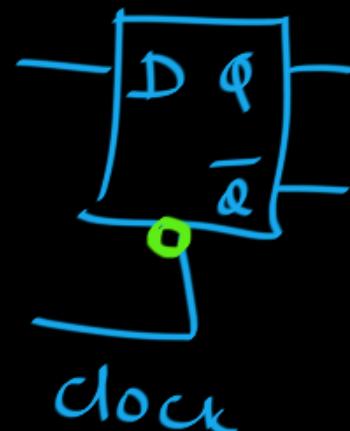
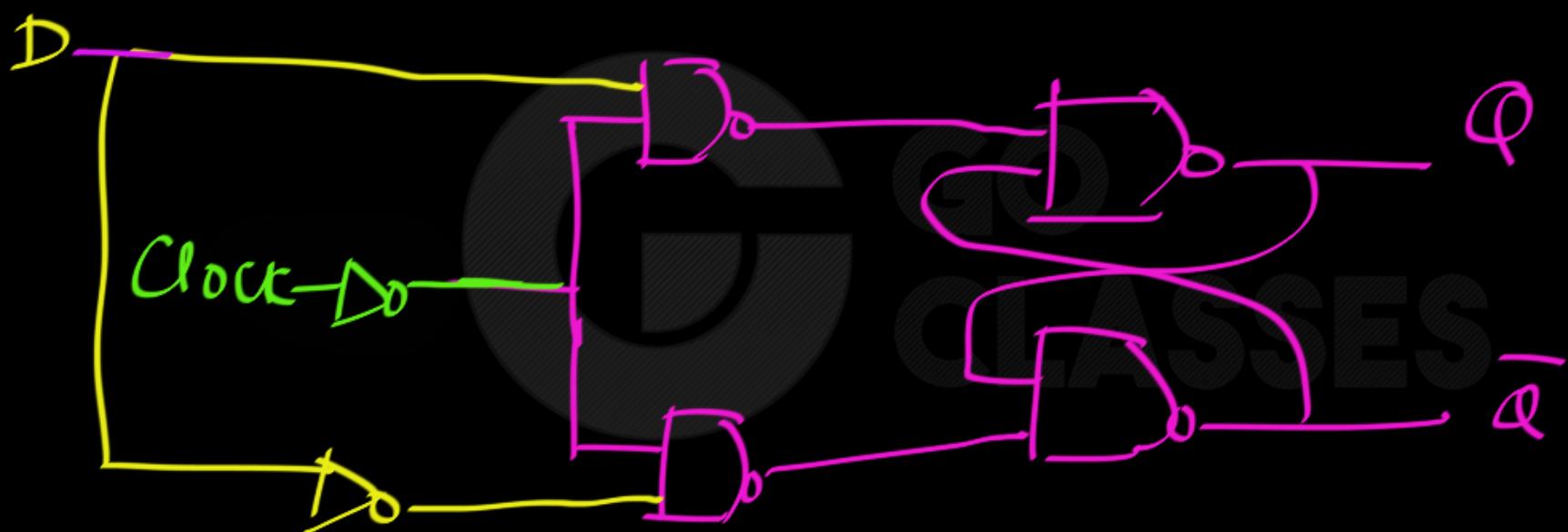
+Ve level, -Ve level Trig. Designs ;

Basic Implementations

D-ff with +ve level Triggering :

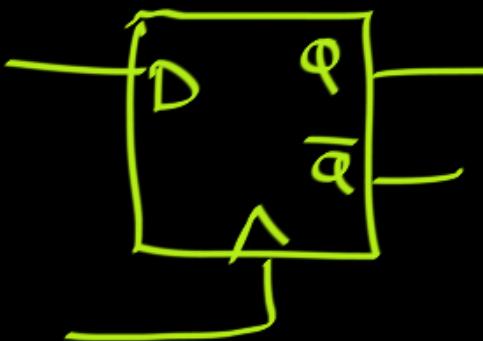


D-ff with -ve level Triggering :



Q: So we can implement ff as  
a level Triggered device ✓

But How to Create Edge Triggered FF ??





Answer :

There are several ways to implement  
Edge sensitive ff But the most  
important (in GATE syllabus) is  
Master Slave flipflop.



↑ M5 ff  $\equiv$  Edge Triggered ff

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So we have Level Triggered ff we have.

Target: Edge Triggered ff

How: by Creating Master Slave ff



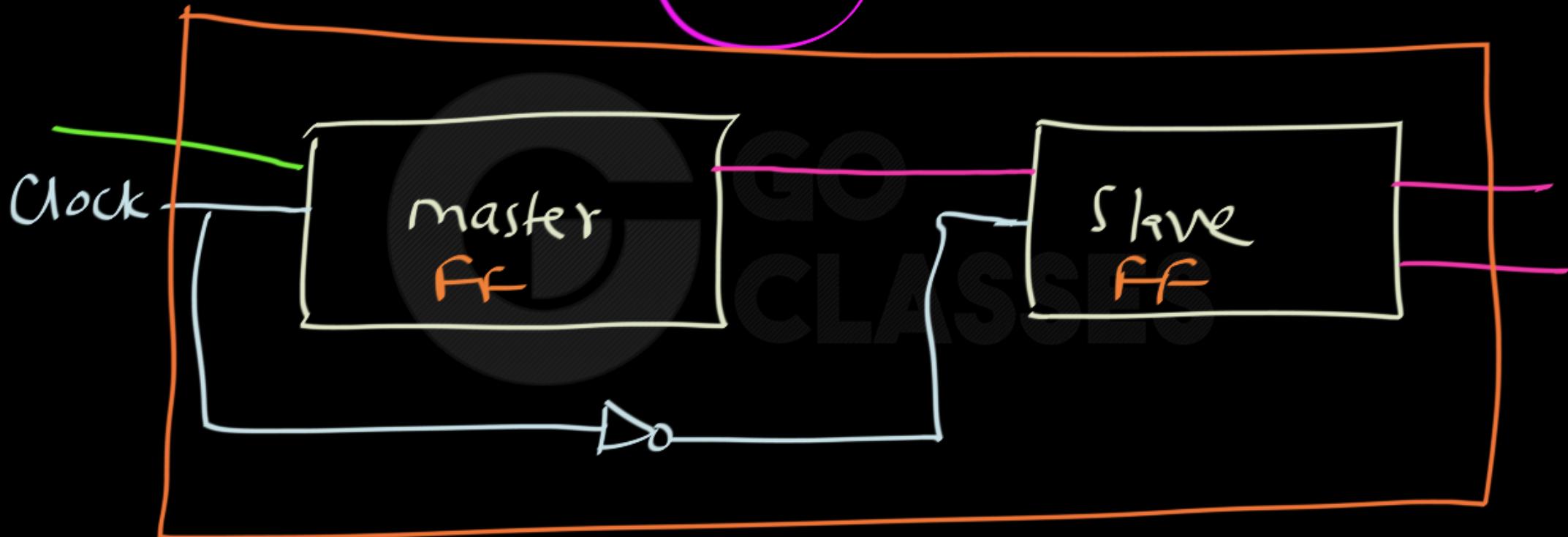
## Next Topic:

# Master Slave Flipflop

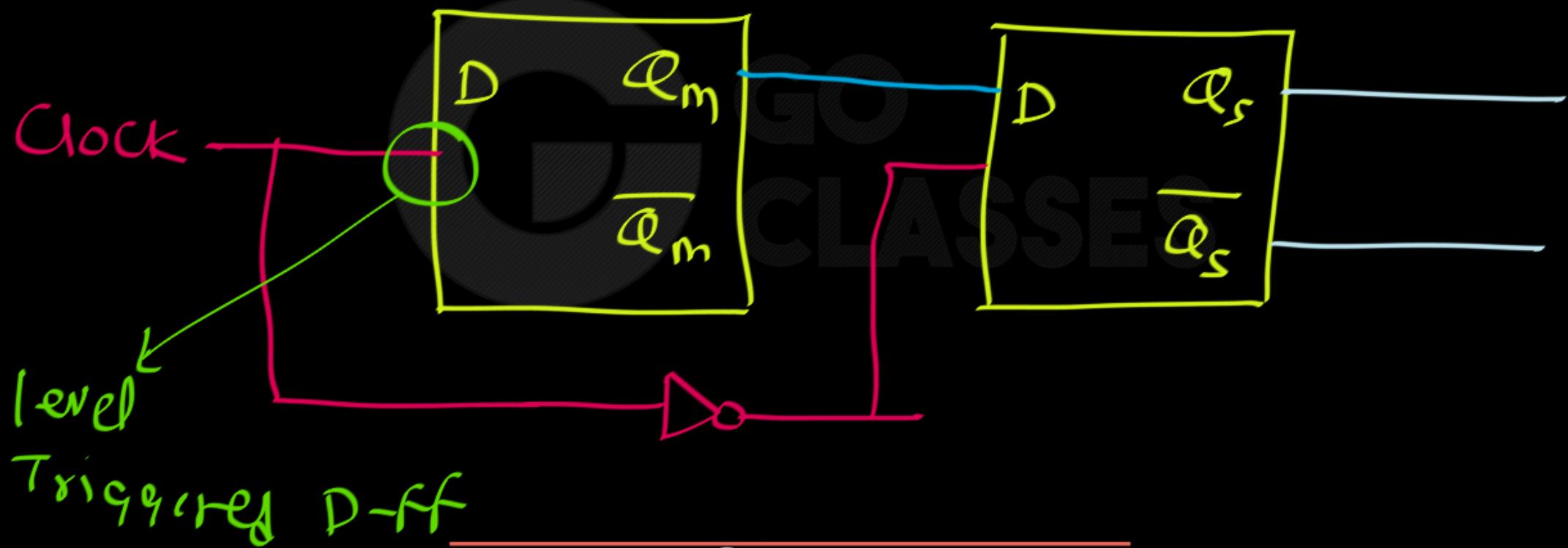
Master Slave ff Idea:



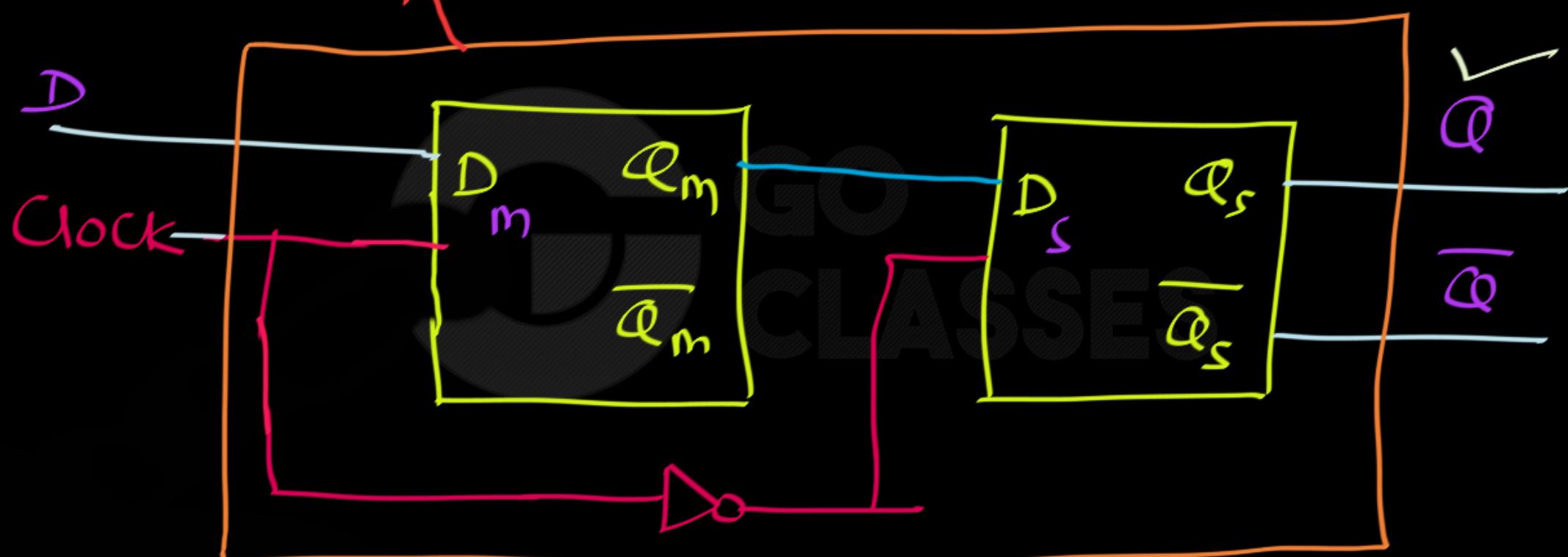
Master Slave ff Idea:



Master Slave D-ff :



Master Slave D -ff  $\Rightarrow Q = Q_s$ ; input =  $D_m$





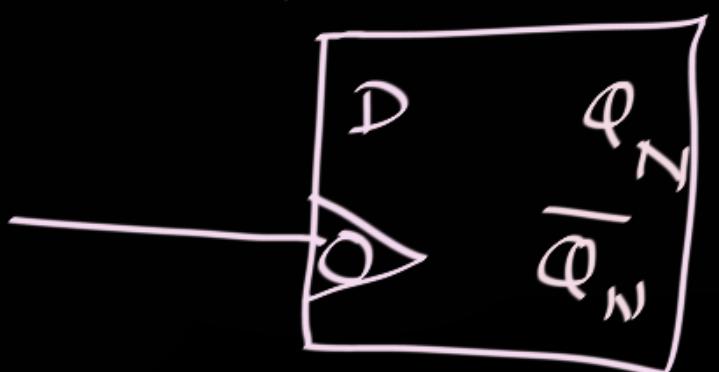
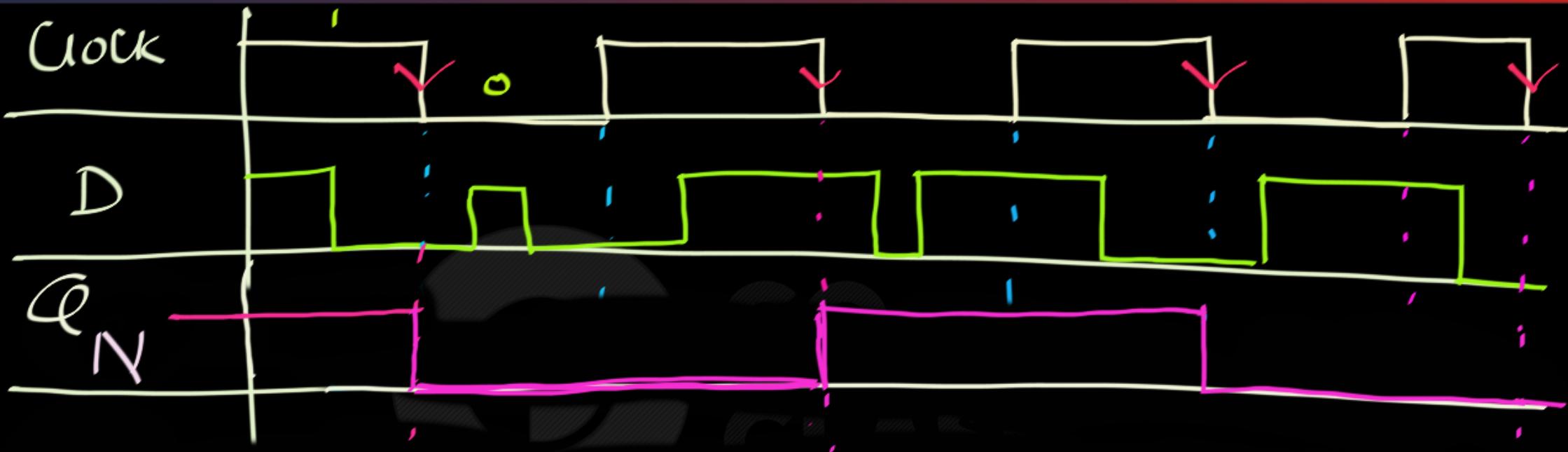
Master - D - ff : +ve level Triggered }

Slave - D - ff : -Ve " "

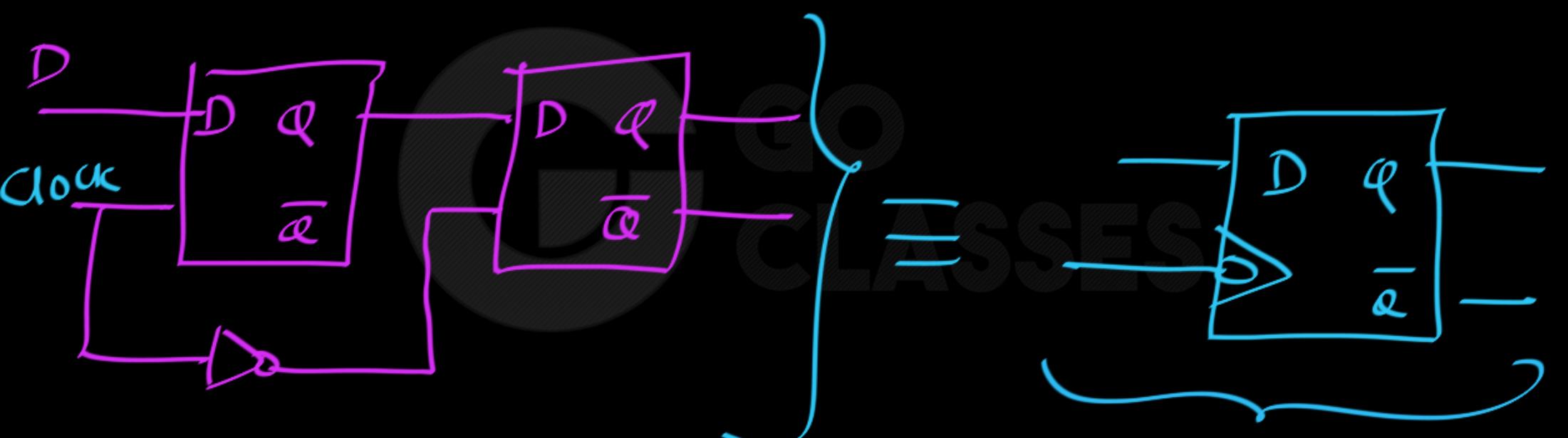
$$Q_m = (D, \underline{\text{+ve level of clock}})$$

$$Q_s = (Q_m, \underline{-ve level of clock})$$





M S - D FF  $\equiv$  -Ve Edge Triggered D-ff

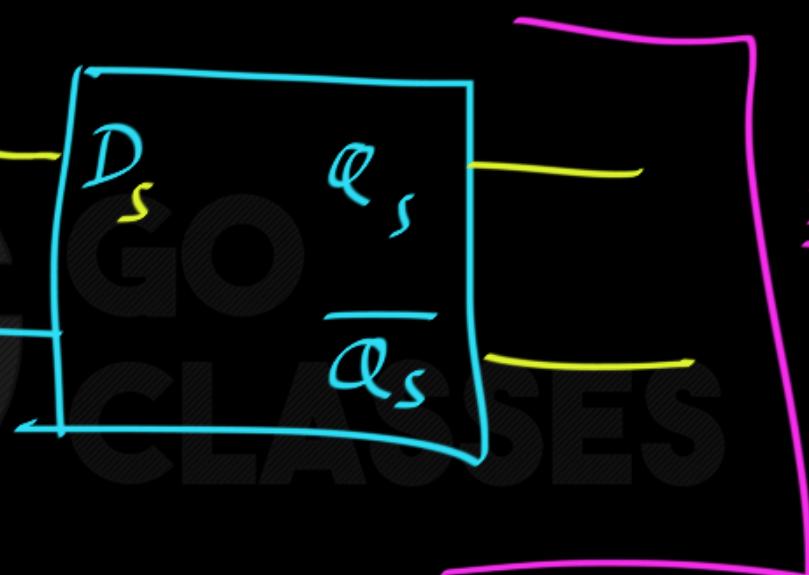
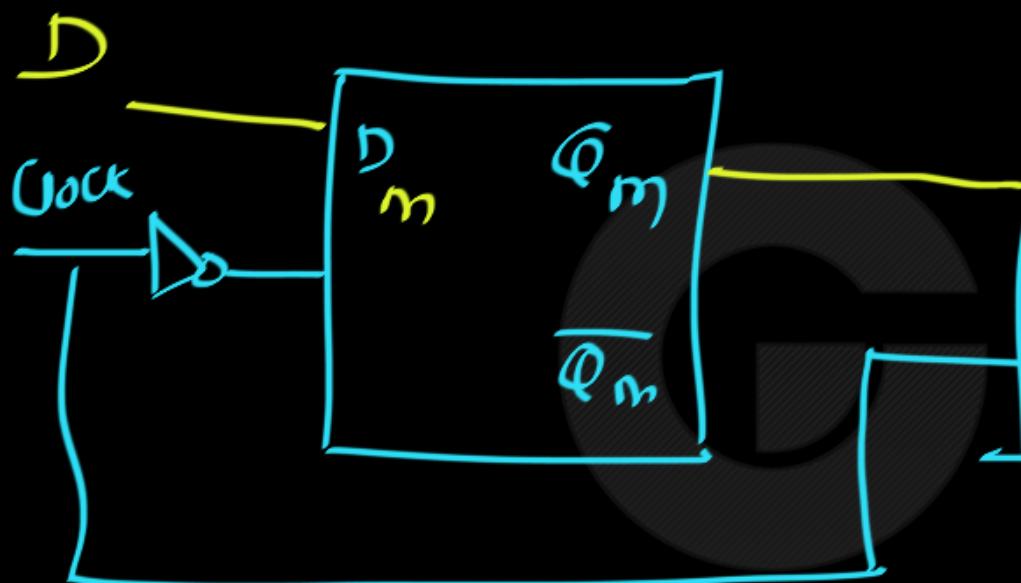


M S-D-FF

-Ve Edge Triggering D-ff



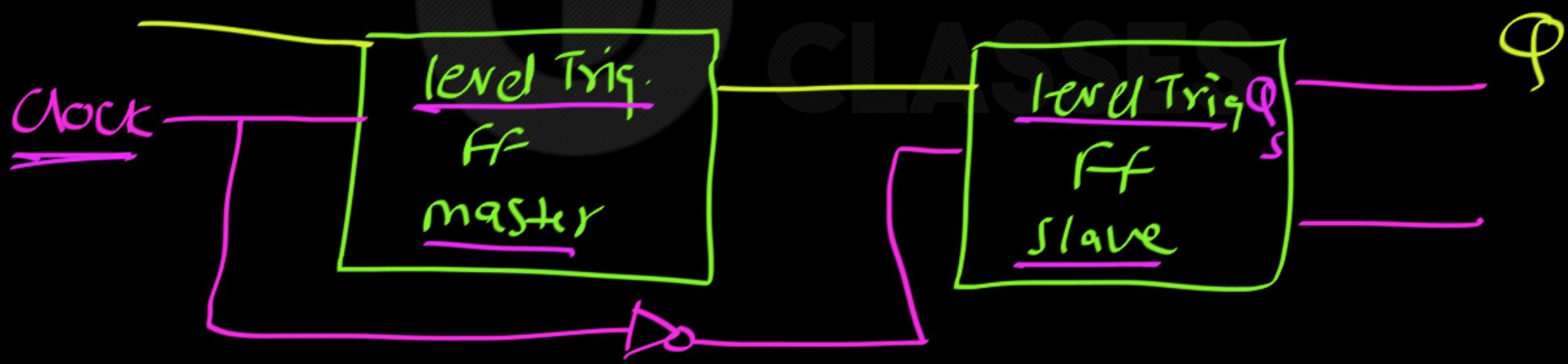
$\equiv$  +ve Edge D-FF



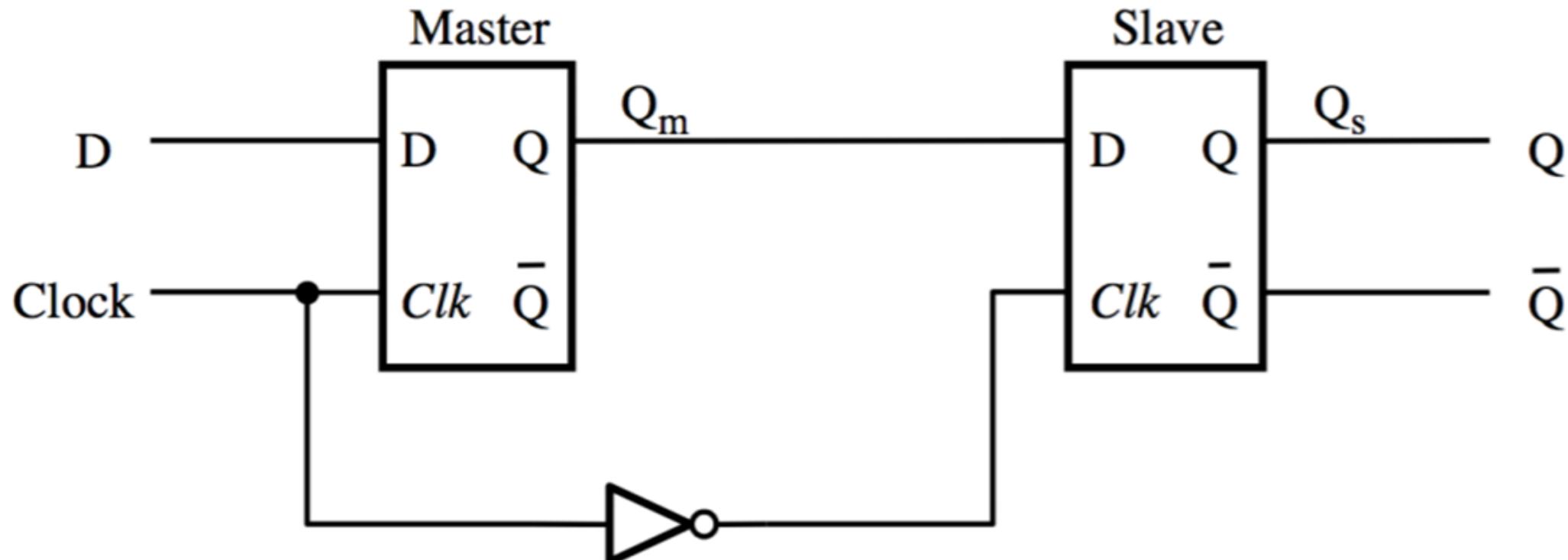
$\equiv$  +ve Edge  
D-FF

Idea of MS-FF to create to

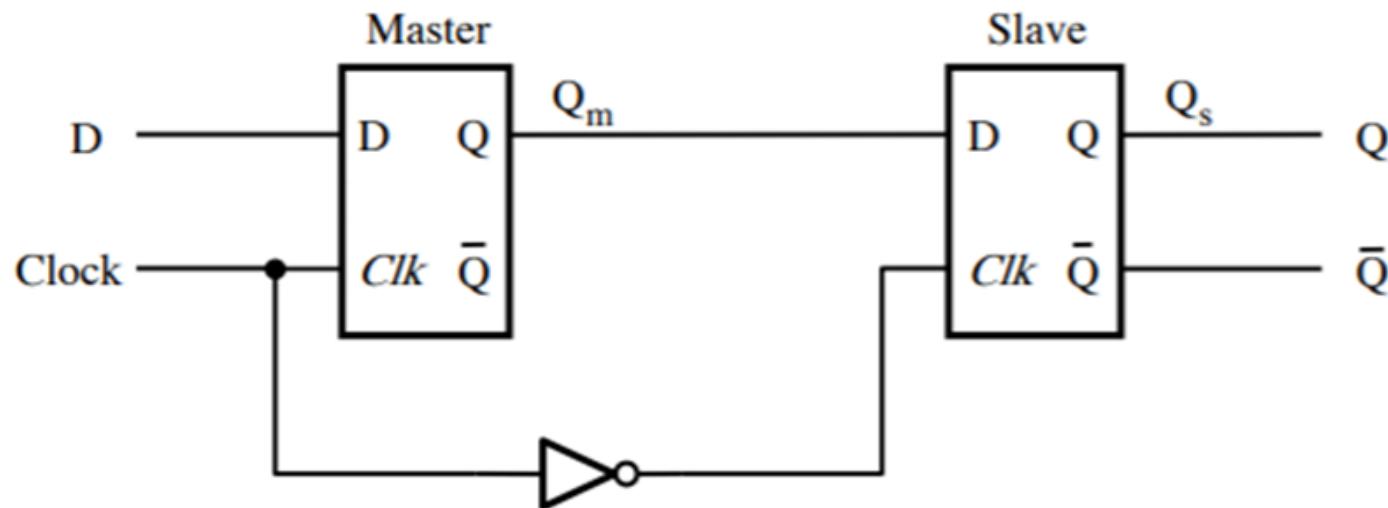
Create Edge Triggering behaviour :



# Constructing a Master-Slave D Flip-Flop From Two D Latches

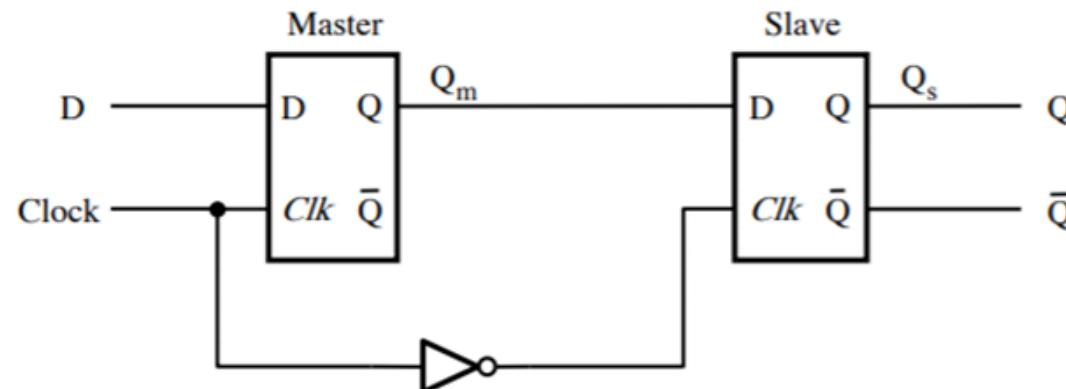


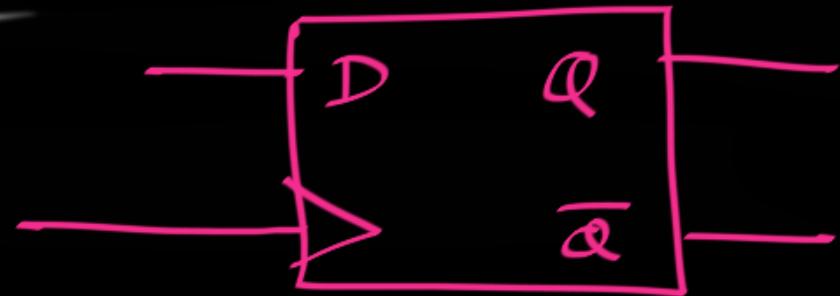
# Master-Slave D Flip-Flop



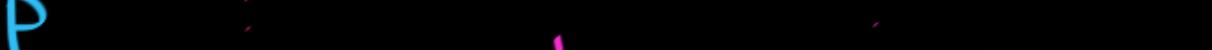
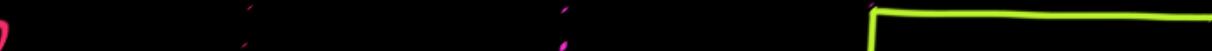
(a) Circuit

# Timing Diagram for the Master-Slave D Flip-Flop

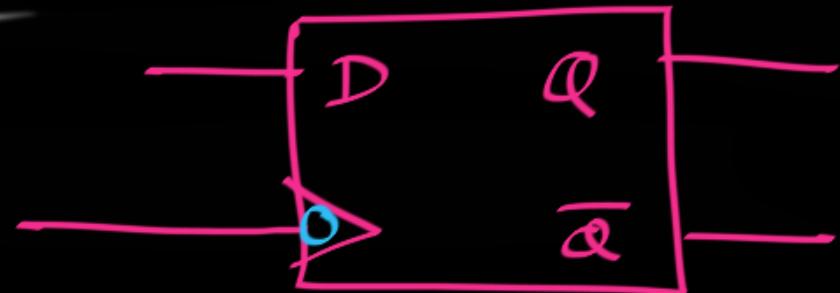




+ve Edge Trig. D - ff



$Q_P$

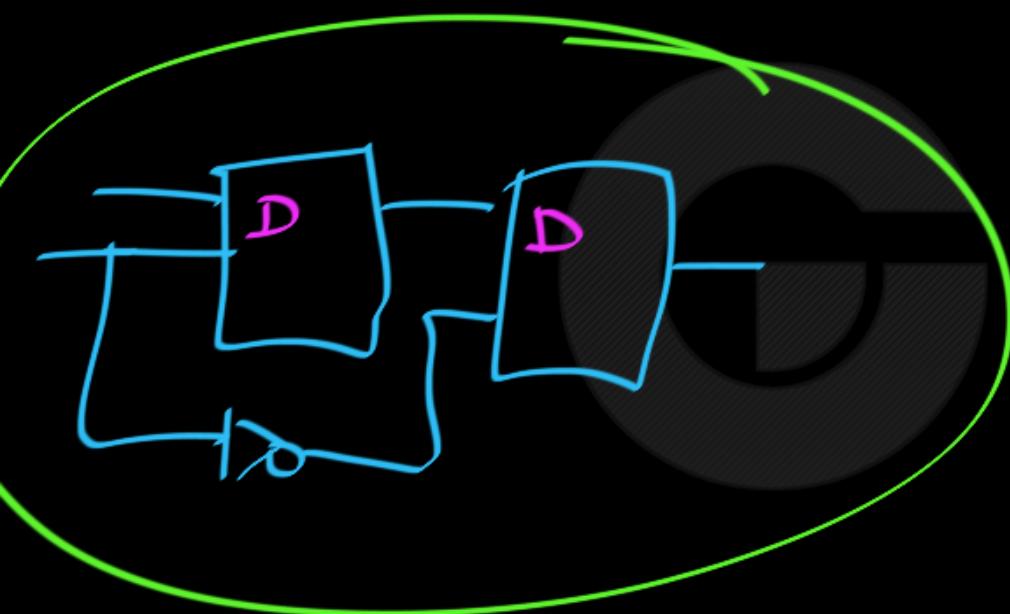


-ve Edge Trig. D - ff



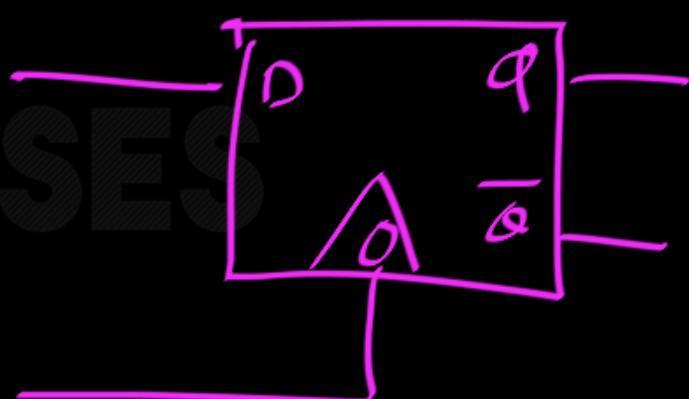


MS - D-FF = -Ve Edge Triggered  
D-FF

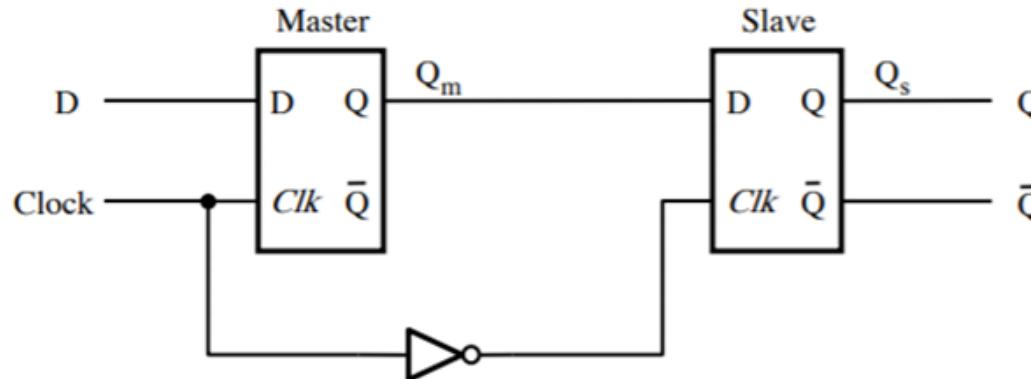


MS - D-FF

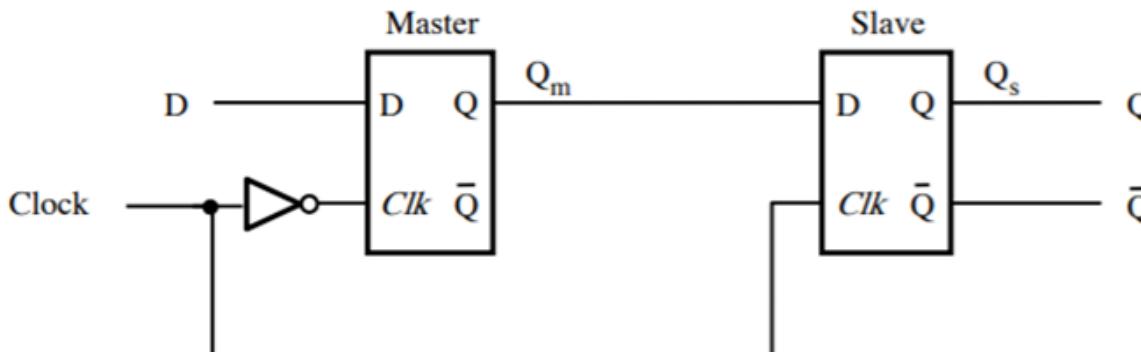
=



# Negative-Edge-Triggered Master-Slave D Flip-Flop



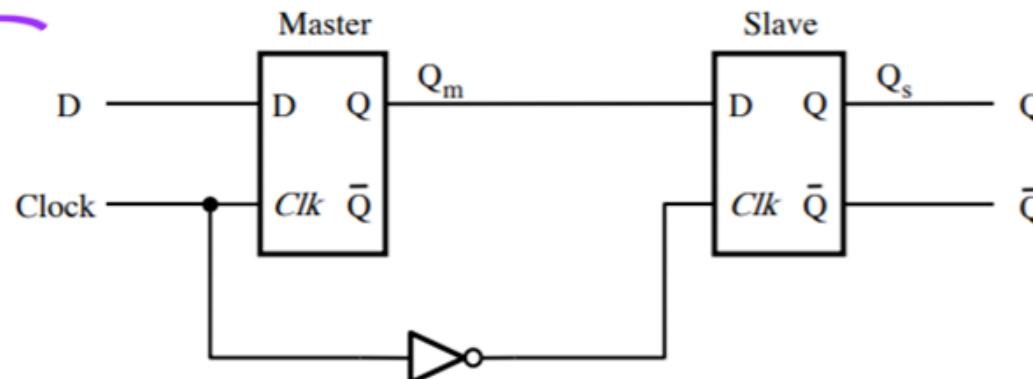
# Positive-Edge-Triggered Master-Slave D Flip-Flop



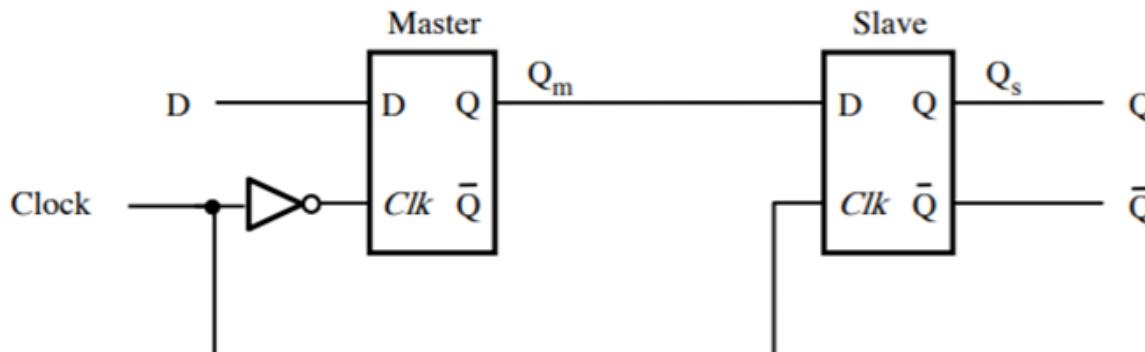
# Negative-Edge-Triggered Master-Slave D Flip-Flop

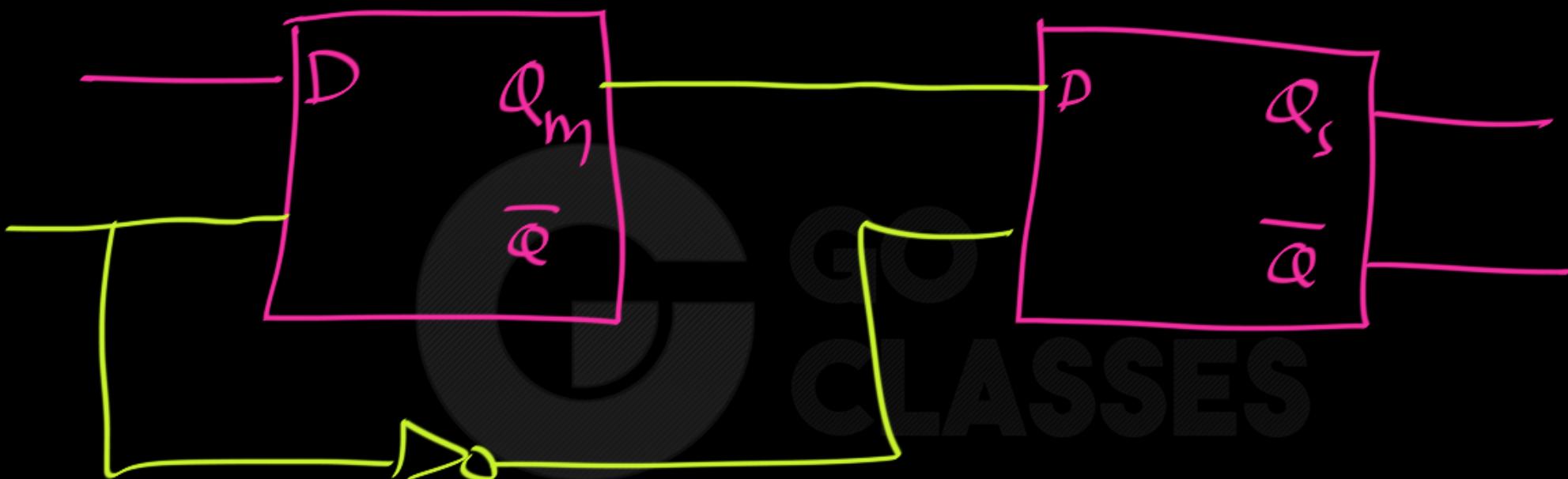
implementation

Block Diagram



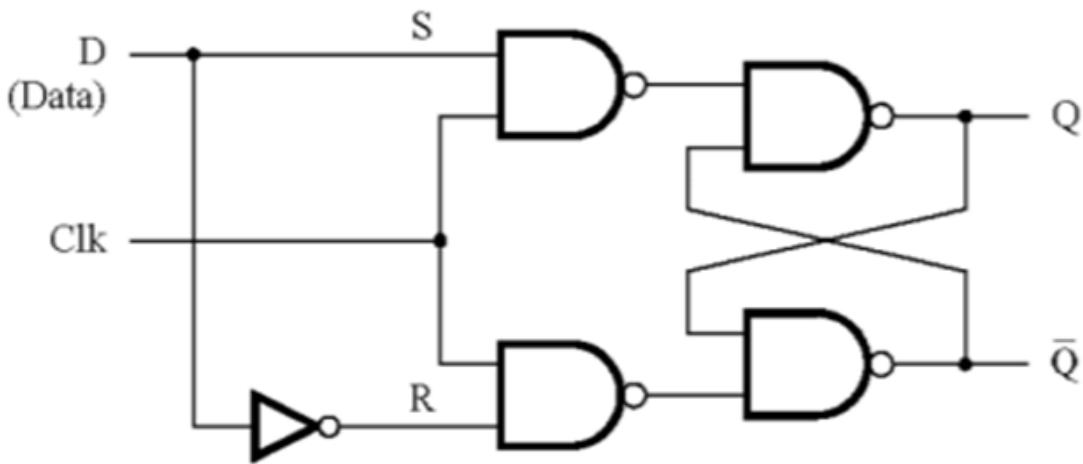
## Positive-Edge-Triggered Master-Slave D Flip-Flop



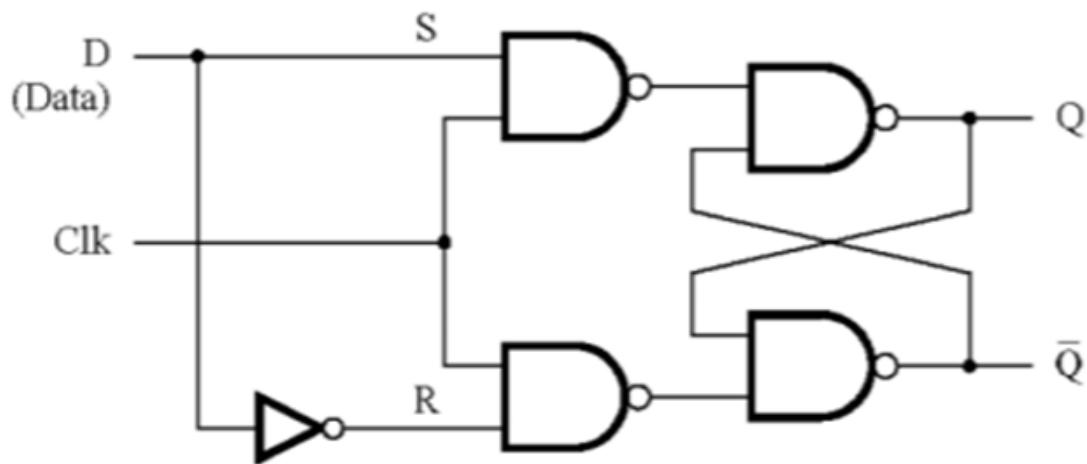


# Constructing a Master-Slave D Flip-Flop From Two D Latches

Master Latch

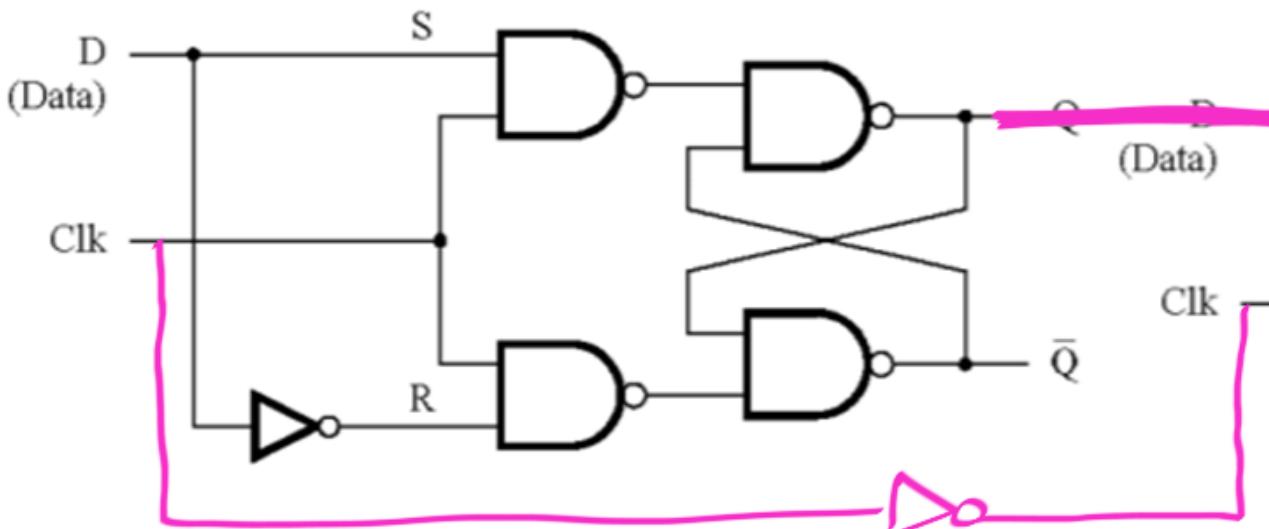


Slave Latch

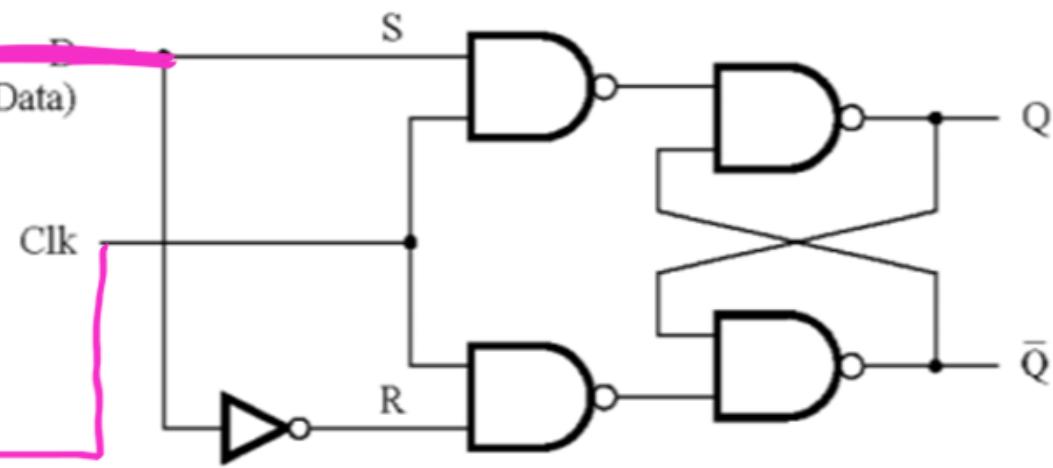


# Constructing a Master-Slave D Flip-Flop From Two D Latches

Master Latch

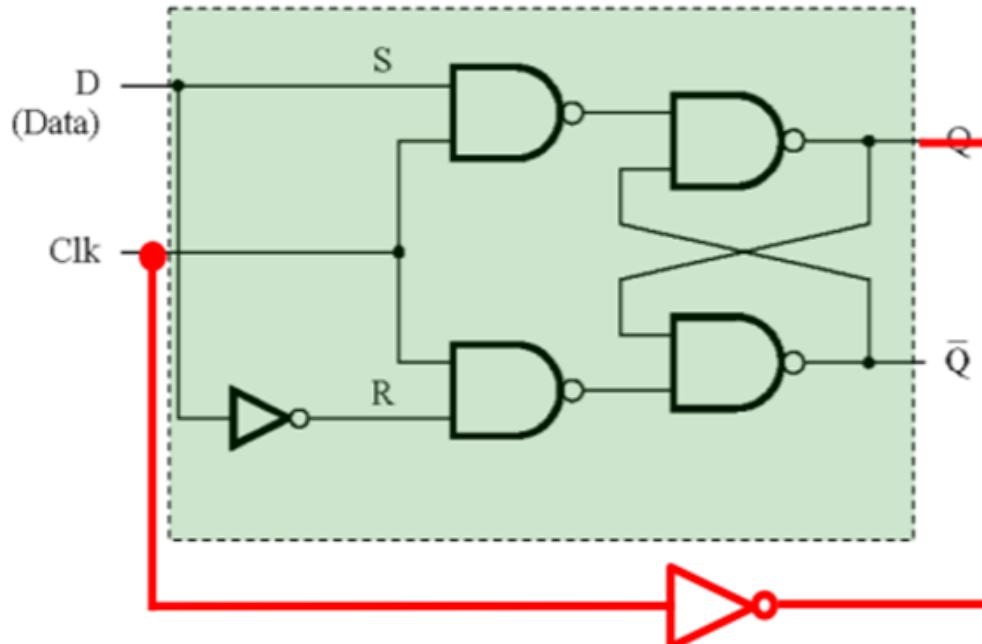


Slave Latch

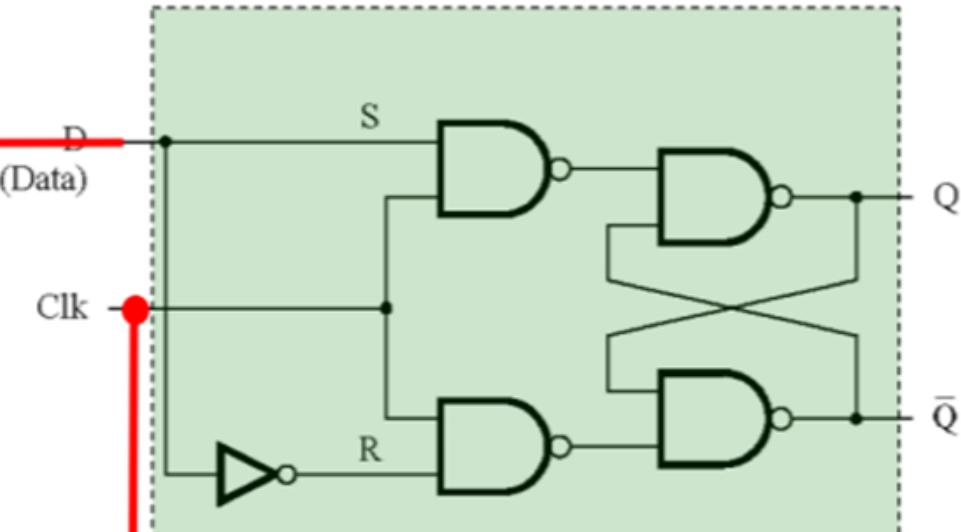


# Constructing a Master-Slave D Flip-Flop From Two D Latches

Master Latch



Slave Latch



1. Convert a *JK* flip-flop to an *SR* flip-flop. Show the conversion table and draw the circuit diagram.
2. A master-slave *D* flip-flop constructed with two positive level sensitive *D* latches (enabled when  $En=1$ ) and an inverter is shown in Figure 1. The clock pulses and the logical level changes at the input of the master flip-flop are given in Figure 2. Draw the logical levels at the *Y* and *Q* outputs of the *D* flip-flops on the same timing diagram.

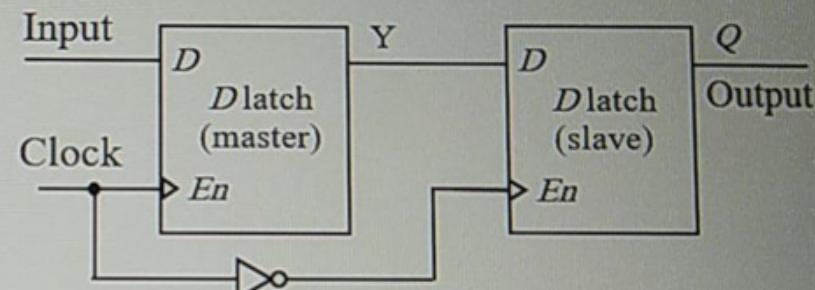


Figure 1 Master-Slave *D* Flip-Flop

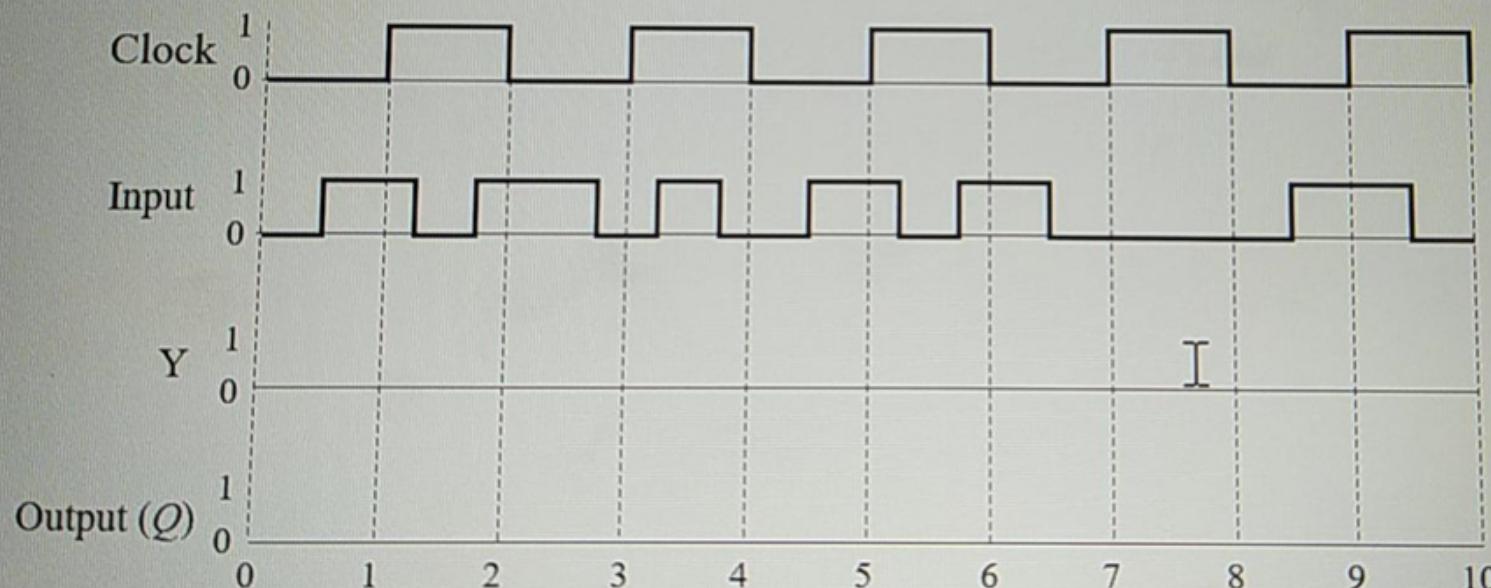


Figure 2 Timing diagram of the master-slave *D* flip-

① JK to SR :

JK is Already Same as SR

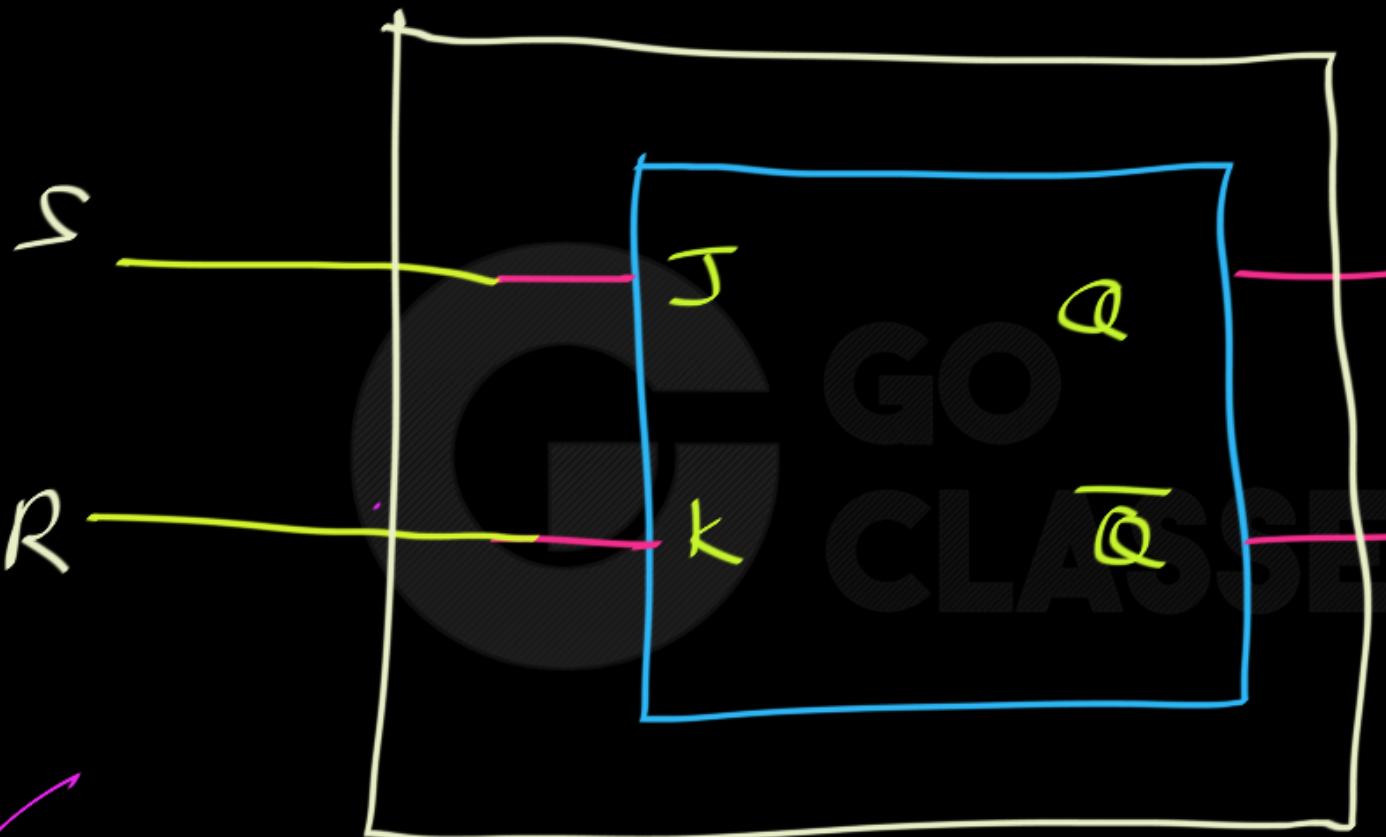
BUT

Don't Apply II Combination.

J — S

k — R

In SR, II combination  
is forbidden.



Note : Don't Apply (1) Combination .

- Convert a *JK* flip-flop to an *SR* flip-flop. Show the conversion table and draw the circuit diagram.
- A master-slave *D* flip-flop constructed with two positive level sensitive *D* latches (enabled when  $En=1$ ) and an inverter is shown in Figure 1. The clock pulses and the logical level changes at the input of the master flip-flop are given in Figure 2. Draw the logical levels at the *Y* and *Q* outputs of the *D* flip-flops on the same timing diagram.

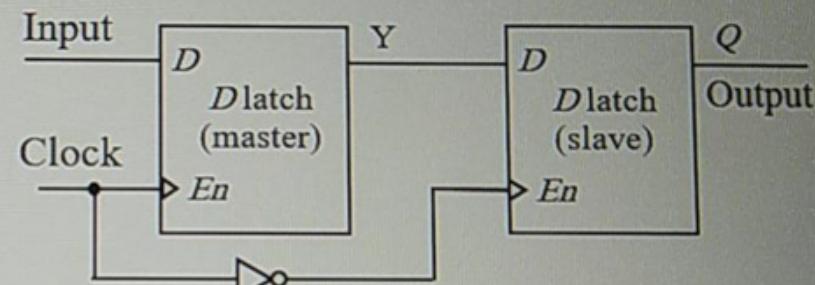


Figure 1 Master-Slave *D* Flip-Flop

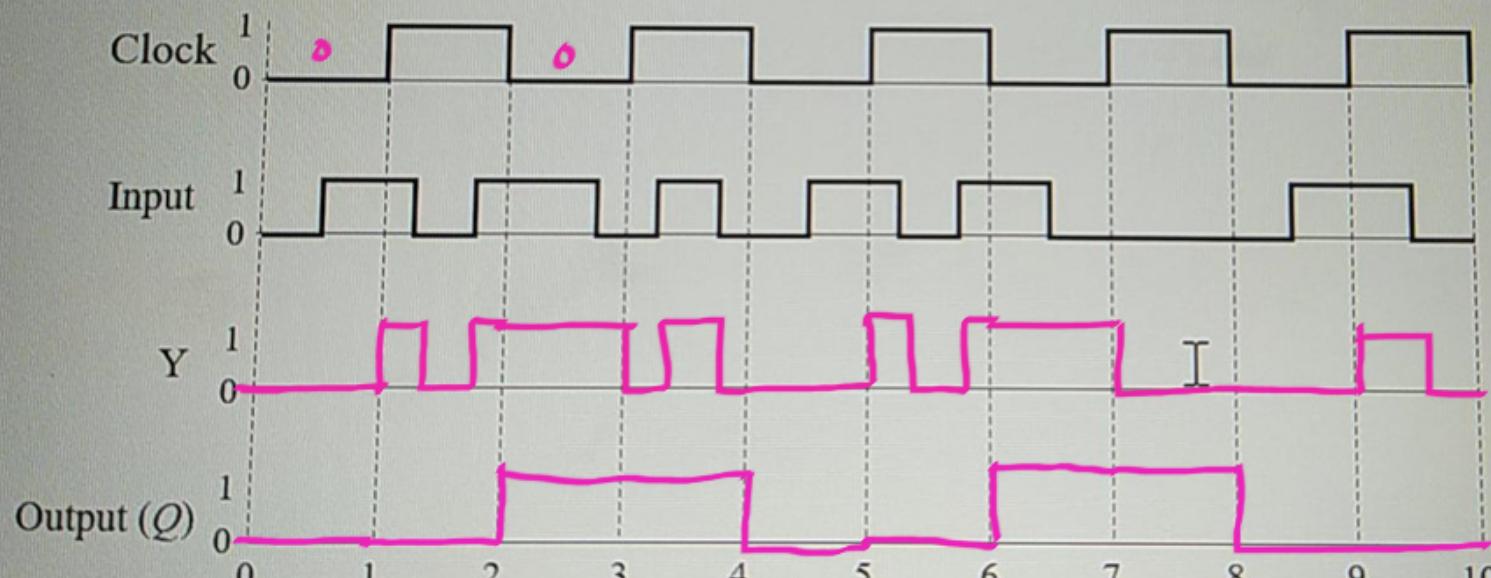
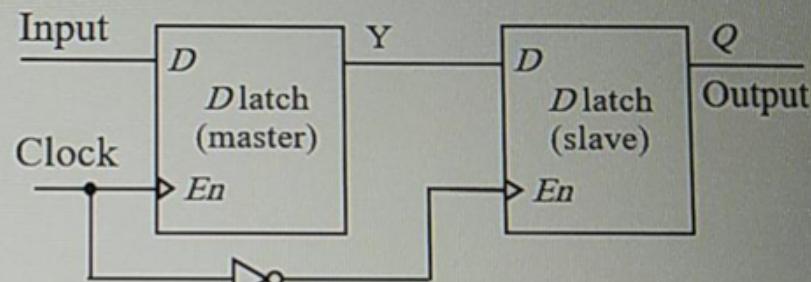


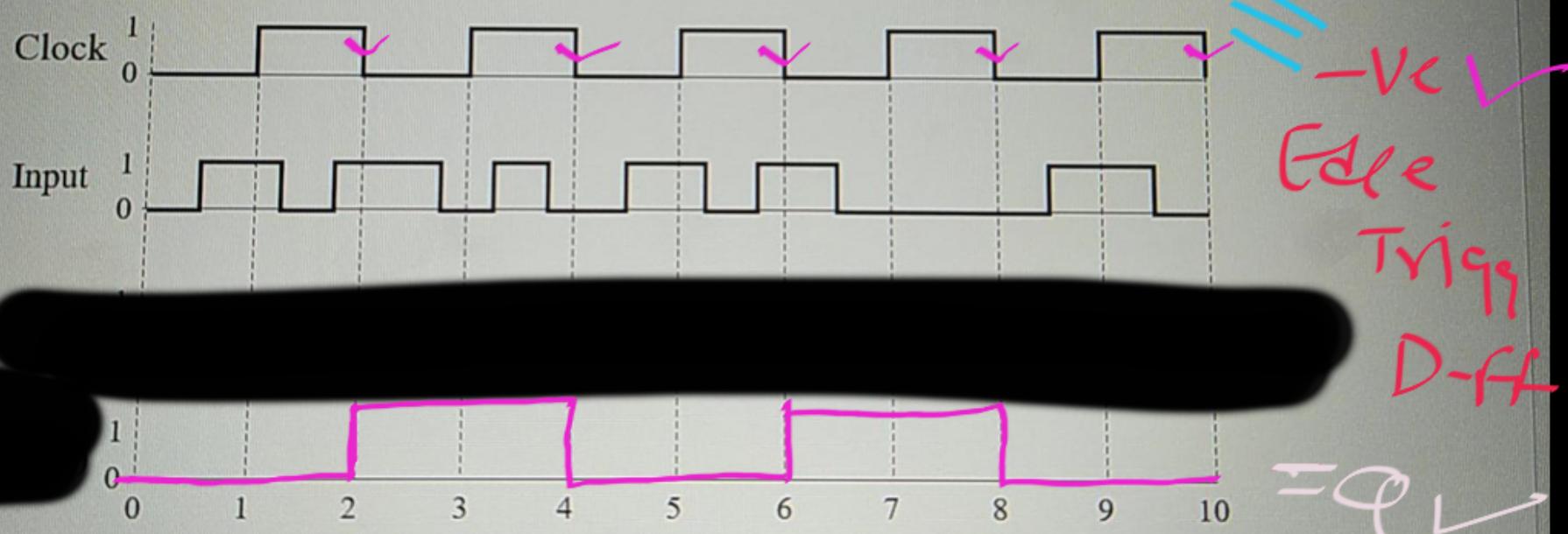
Figure 2 Timing diagram of the master-slave *D* flip-

$Q = f(Y)$ ,  
-Ve level  
of Clock

- Convert a *JK* flip-flop to an *SR* flip-flop. Show the conversion table and draw the circuit diagram.
- A master-slave *D* flip-flop constructed with two positive level sensitive *D* latches (enabled when  $En=1$ ) and an inverter is shown in Figure 1. The clock pulses and the logical level changes at the input of the master flip-flop are given in Figure 2. Draw the logical levels at the *Y* and *Q* outputs of the *D* flip-flops on the same timing diagram.



**Figure 1 Master-Slave *D* Flip-Flop**



**Figure 2 Timing diagram of the master-slave *D* flip-**

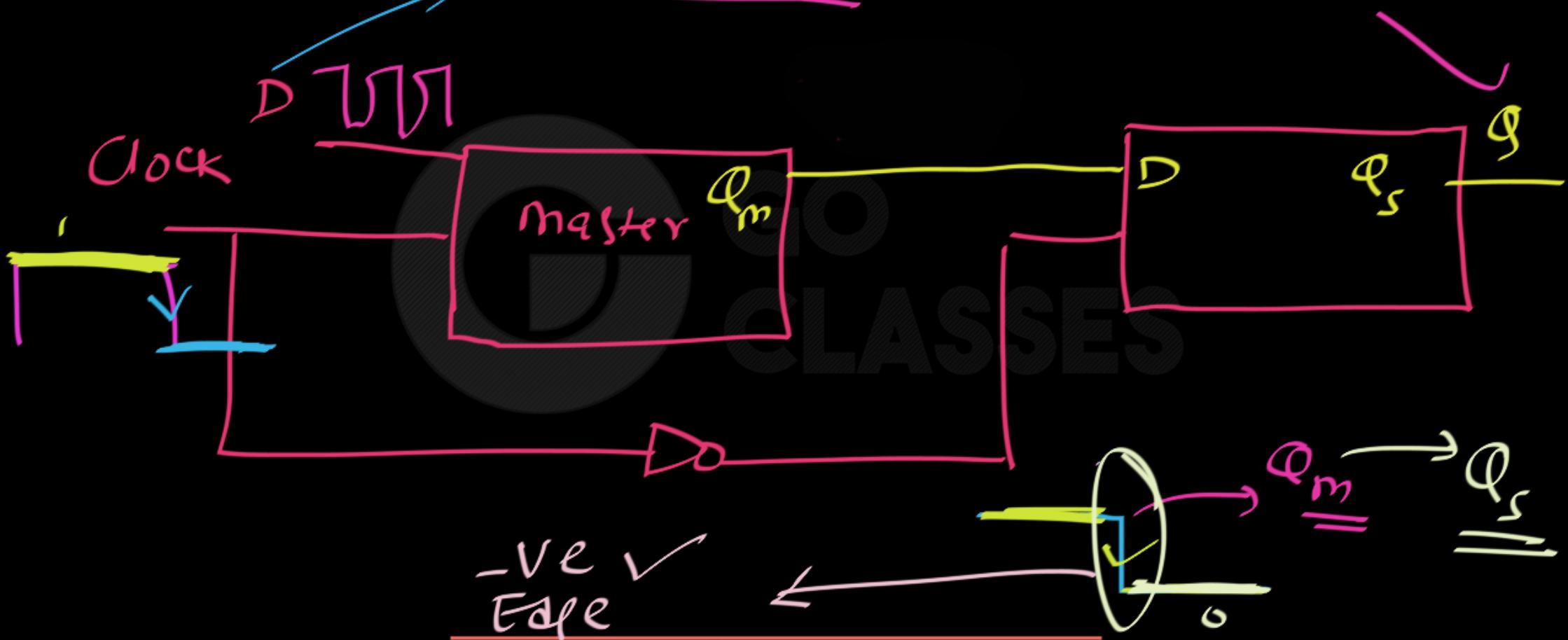


MS - ff is behaving like -Ve Edge

Triggered FF.

Why?    Intuition?

Intuition: in user control

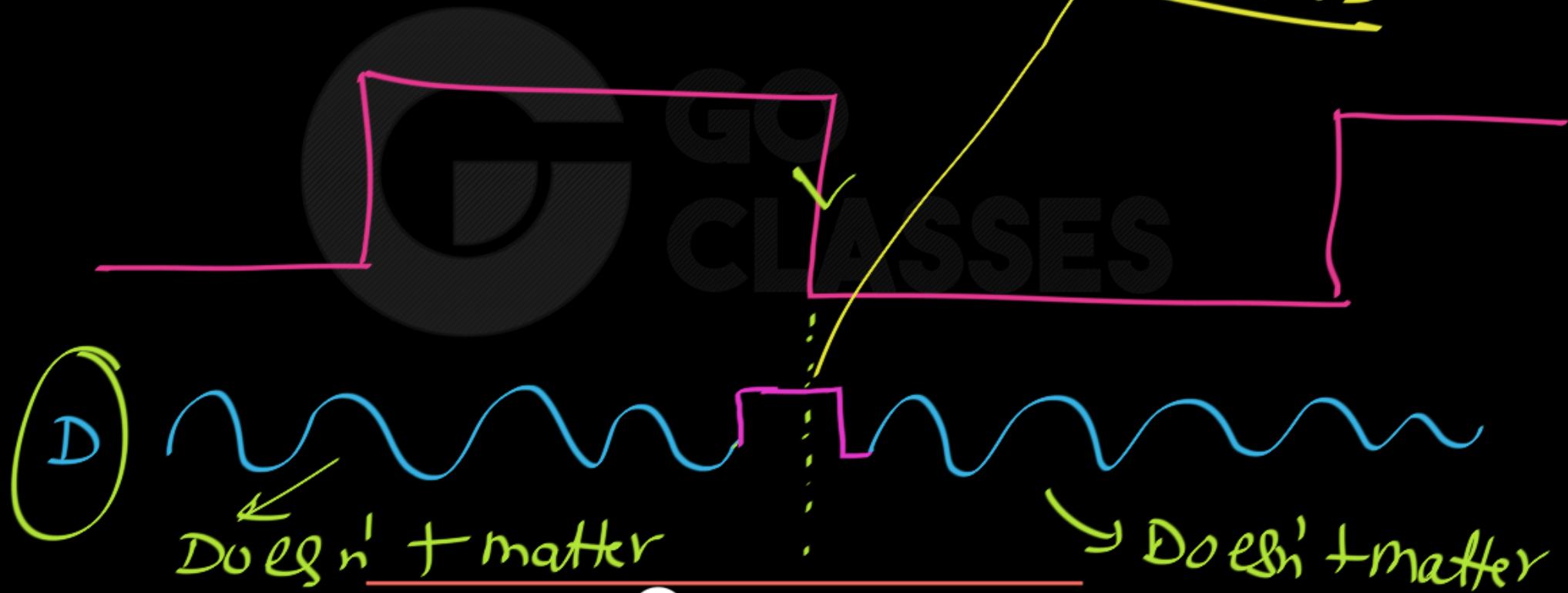


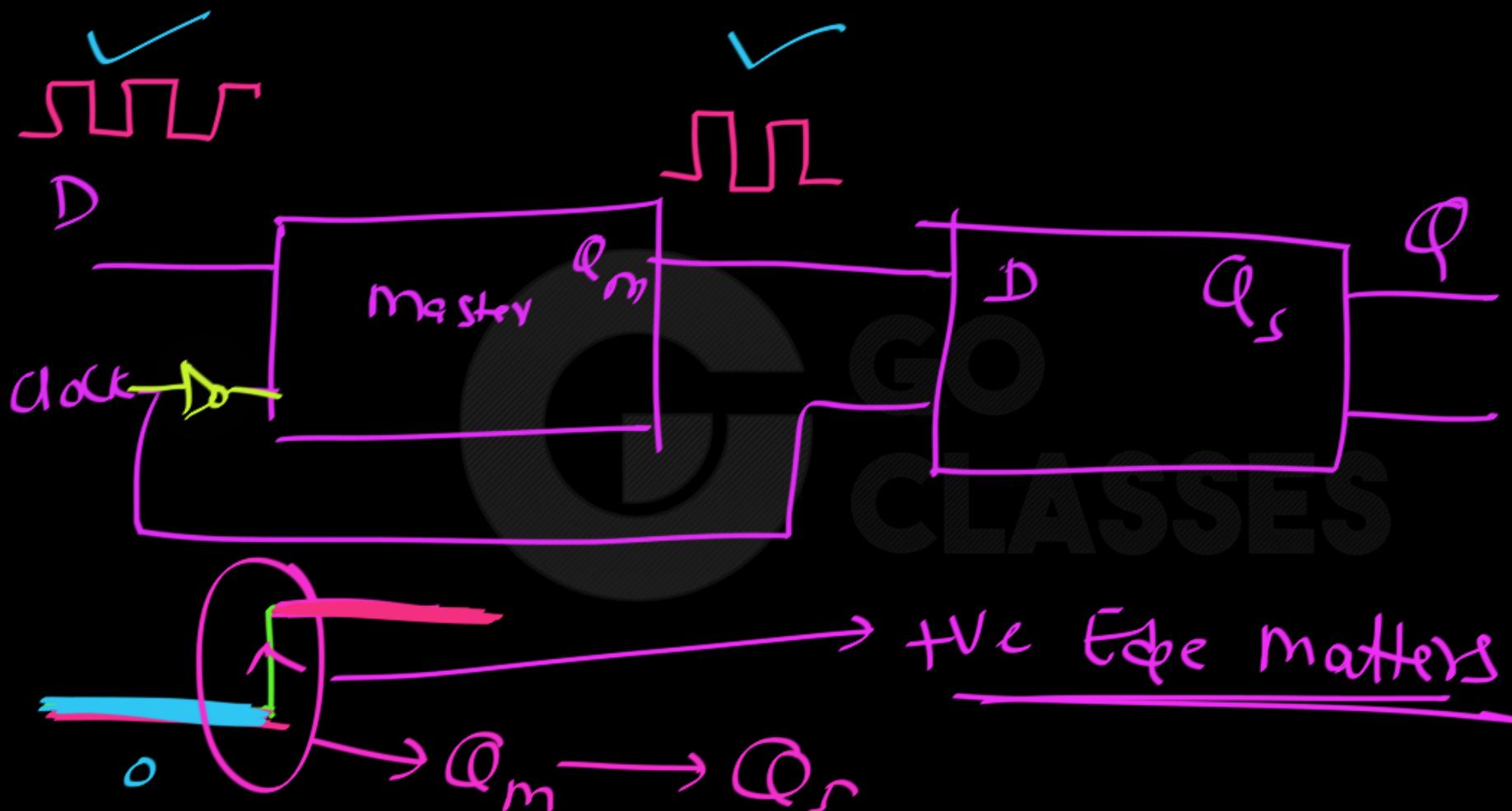


-Ve Edge Trig. D-ff:

only this

matters





Analogy: RRR movie



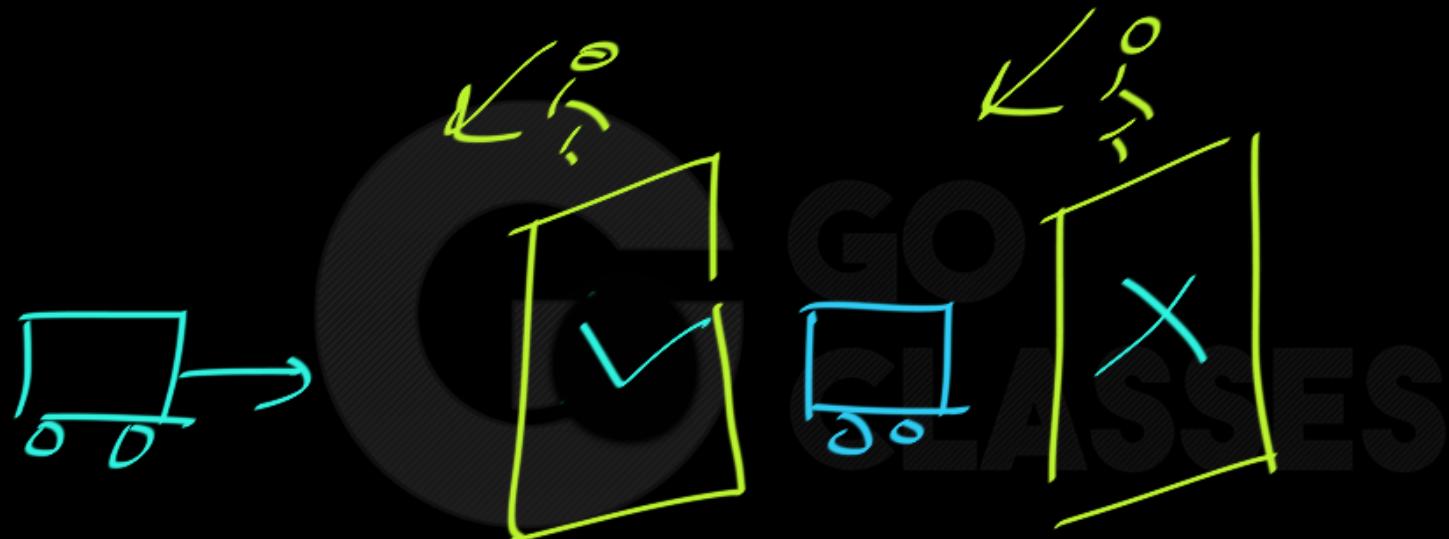


Analogy: Army Camps:



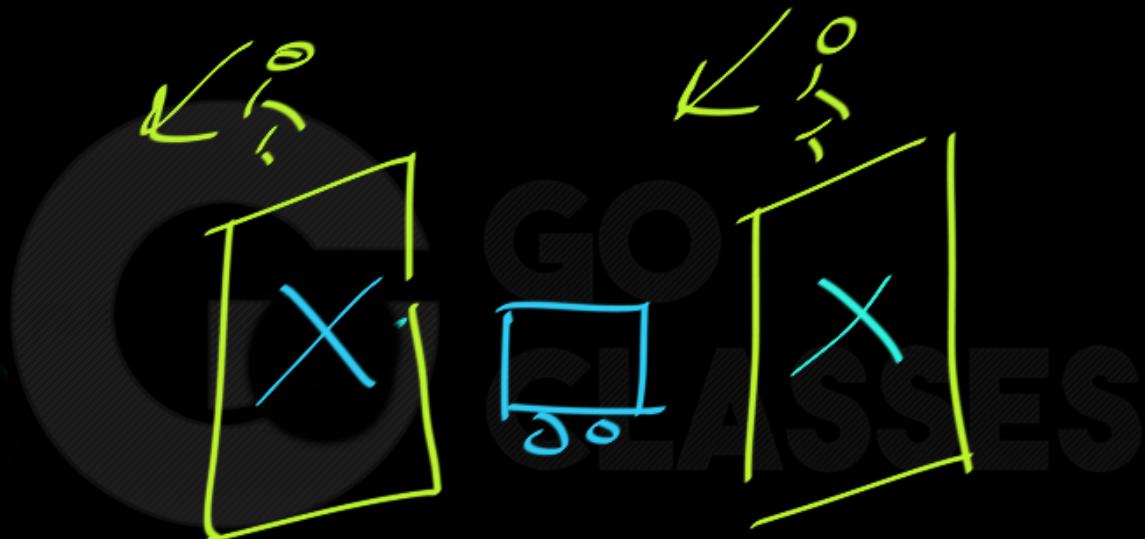


Analogy: Army Camps:





Analogy: Army Camps:



Analogy: Army Camps; Jammu





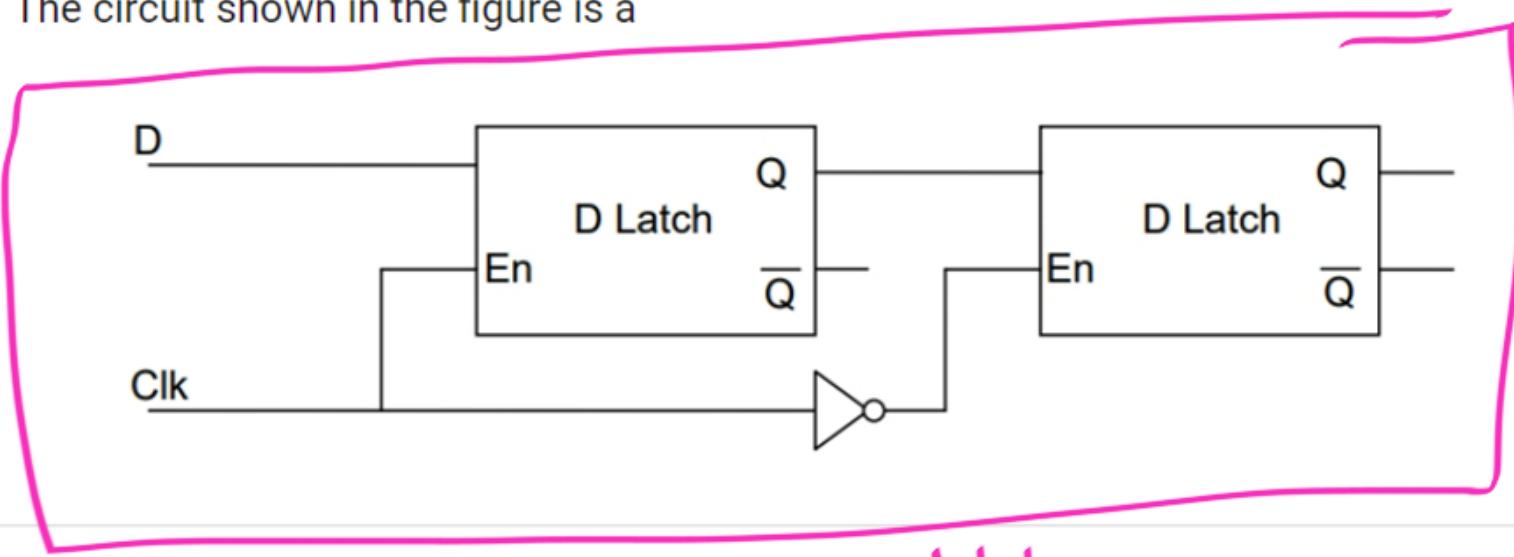
MS - FF



Double Door Analogy



The circuit shown in the figure is a



- A Toggle Flip Flop
- B JK Flip Flop
- C SR Latch
- D Master-Slave D Flip Flop

III

Equivalent to Neg-Edge  
Triggerses D-FF



# Next Topic:

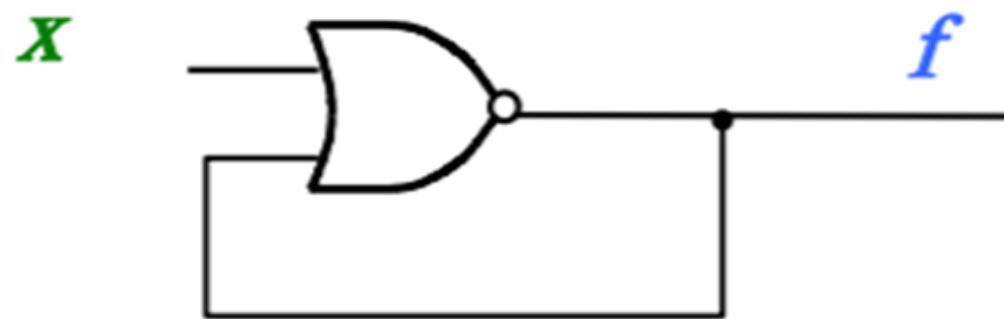
Can you analyse Sequential  
Circuits now?? **TRY!!!**



## Let's Look at a Two Simpler Examples with Feedback

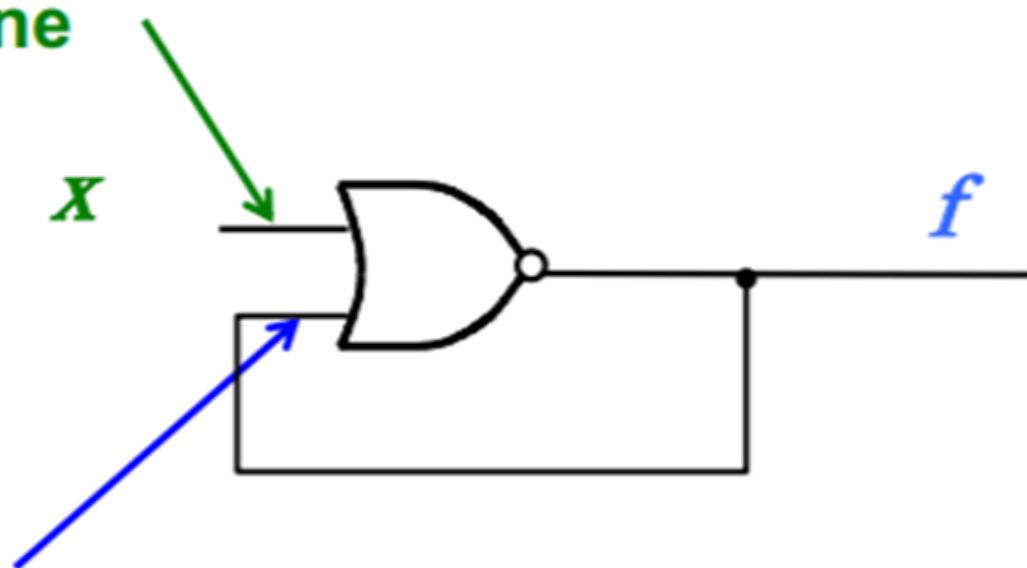


# Let's Try to Analyze This Circuit



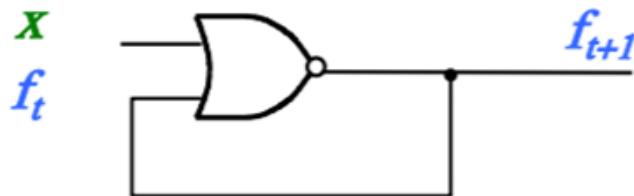
# Let's Try to Analyze This Circuit

Control Line



Data Line

# Let's Try to Analyze This Circuit

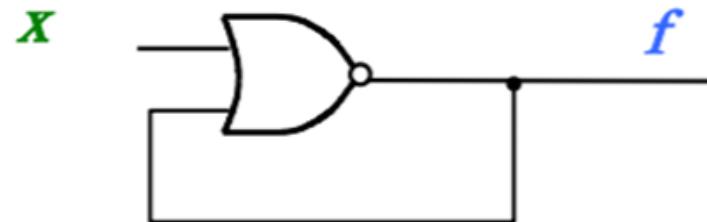


x	$f_t$	$f_{t+1}$
0	0	1
0	1	0
1	0	0
1	1	0

If  $x = 0$ , then  $f$  is negated.

If  $x = 1$ , then  $f$  is driven to 0.

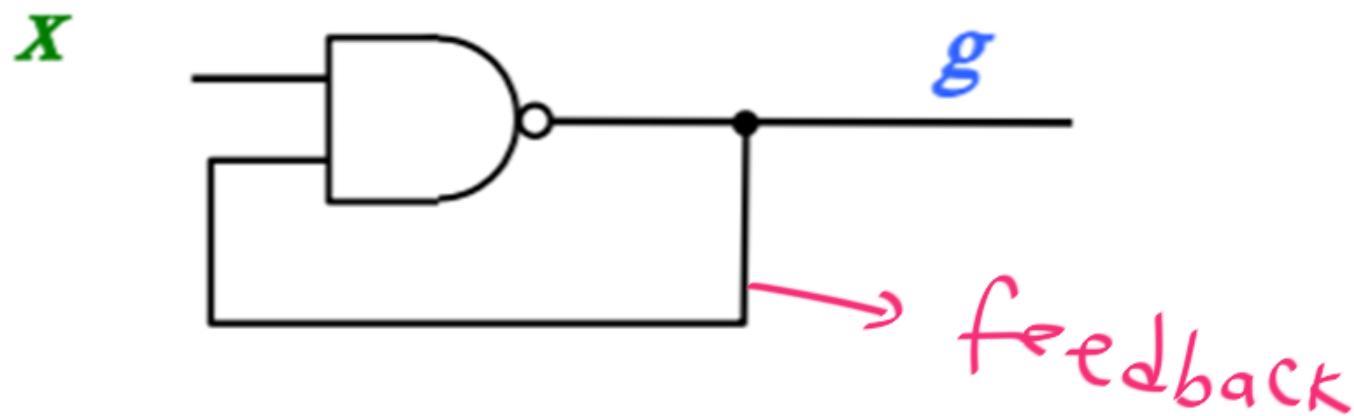
# Key Observation

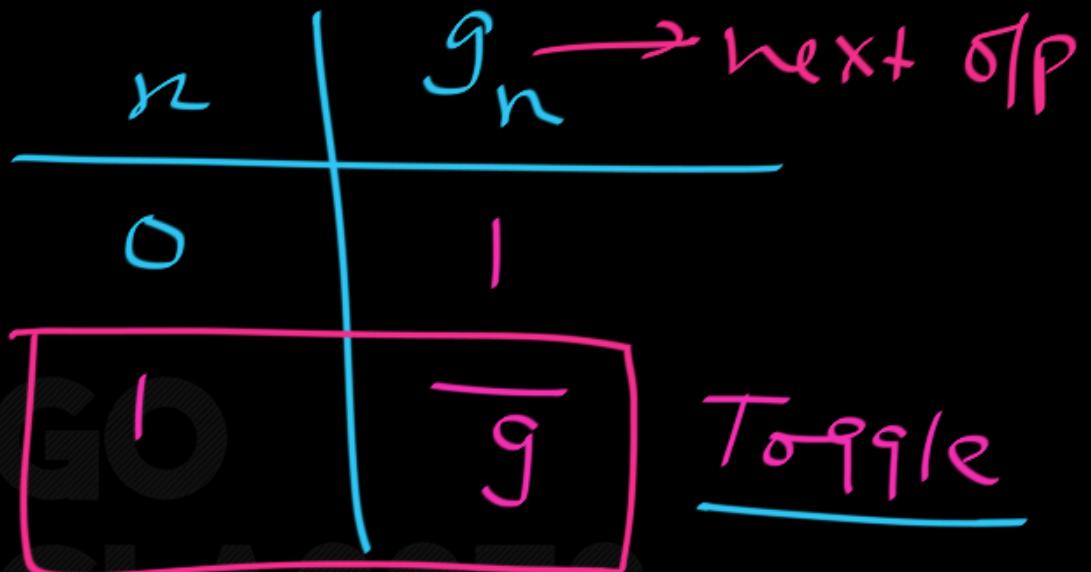
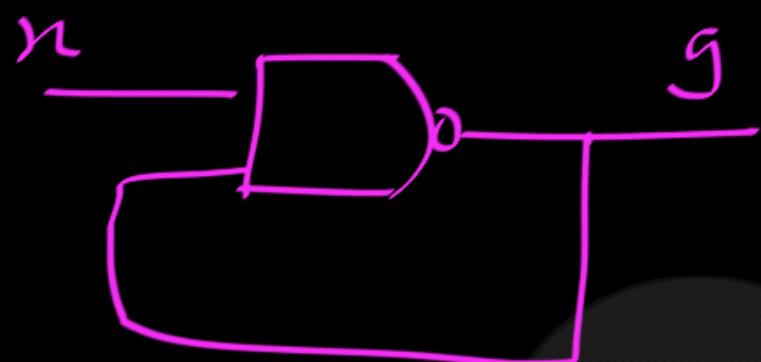


If a NOR's **control line** is 0, then that NOR just **negates its data line**. If the **control line** is 1, then the NOR's output is **driven to 0**, ignoring its **data line**.

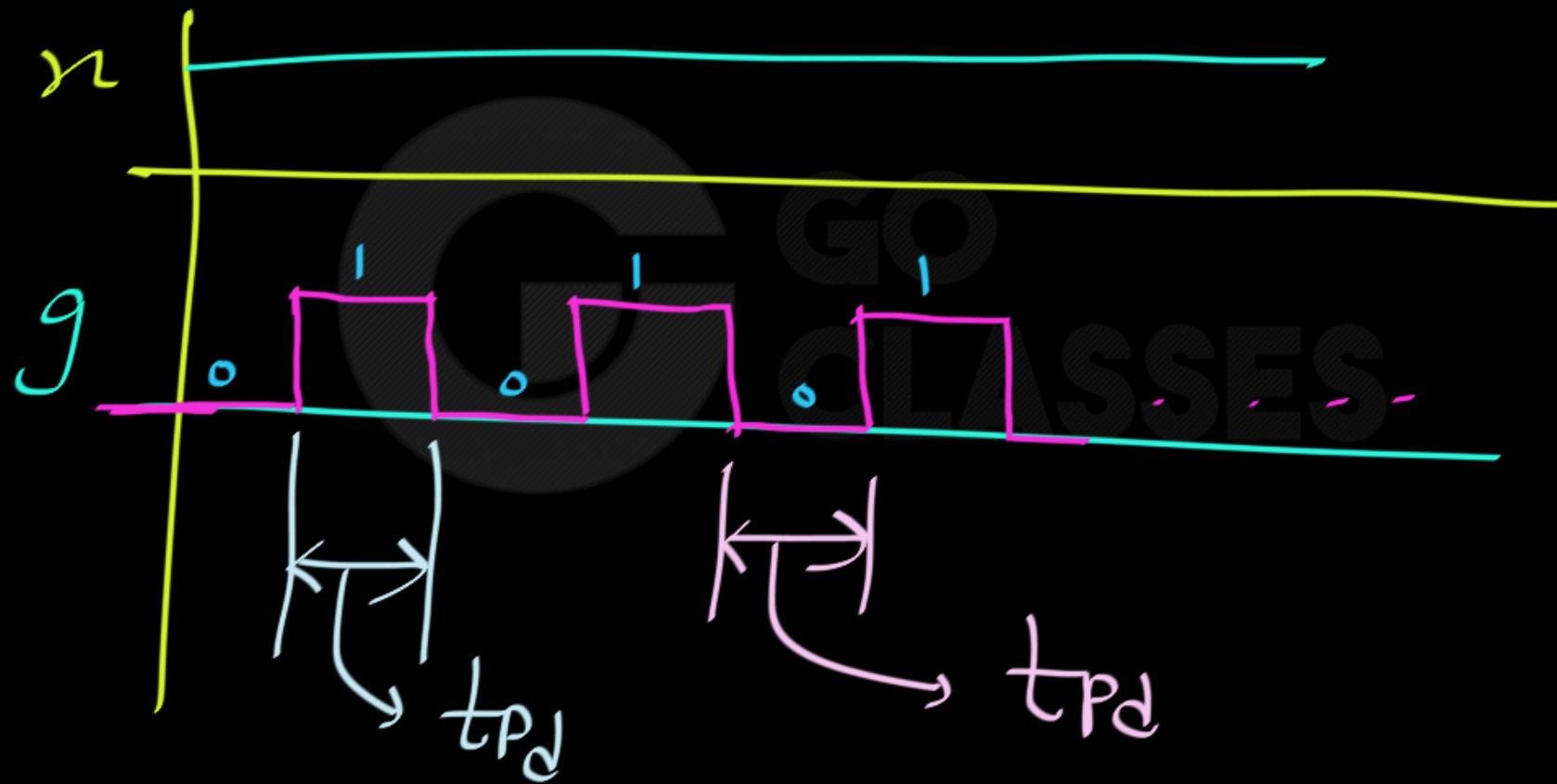


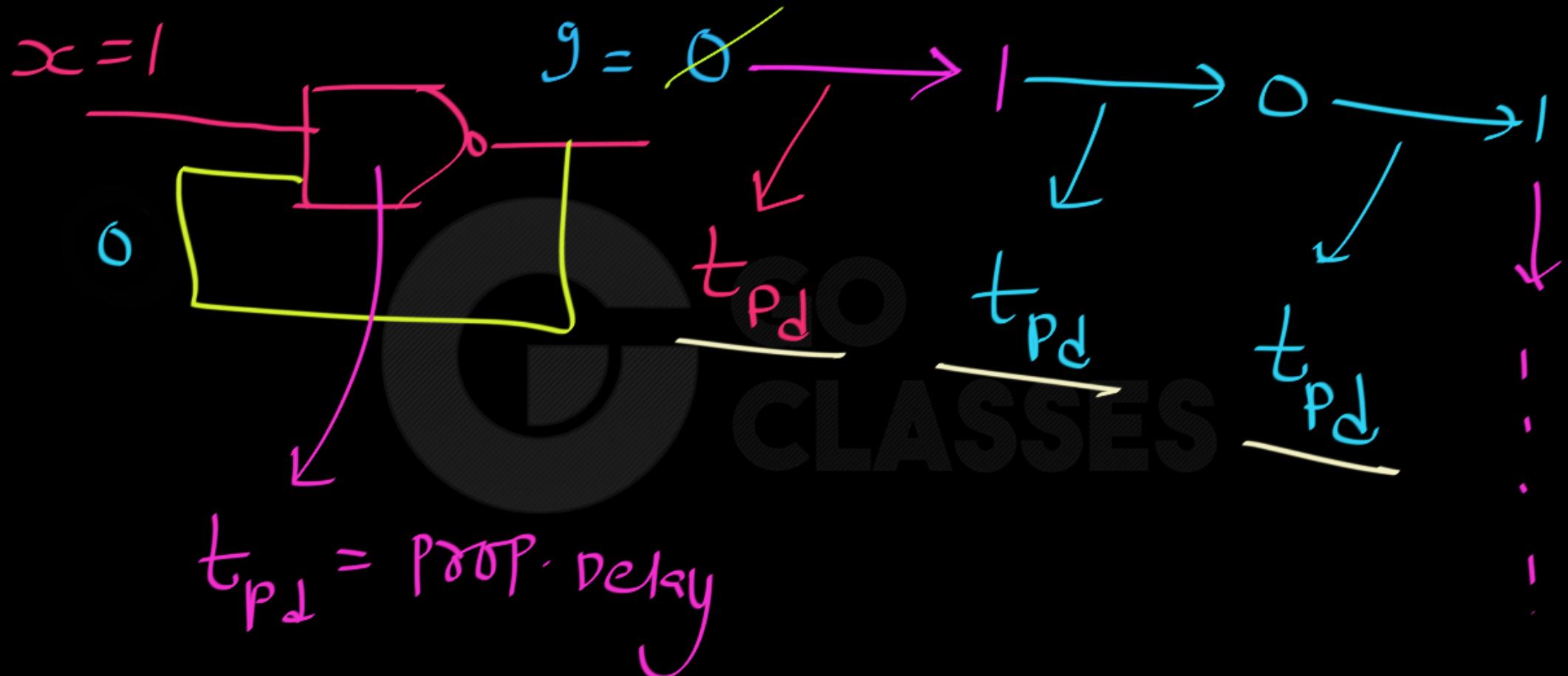
# Let's Try to Analyze This Circuit





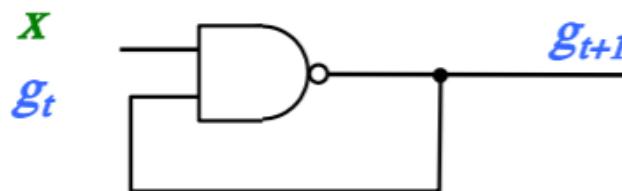
fix  $x=1$  for a long time :







# Let's Try to Analyze This Circuit

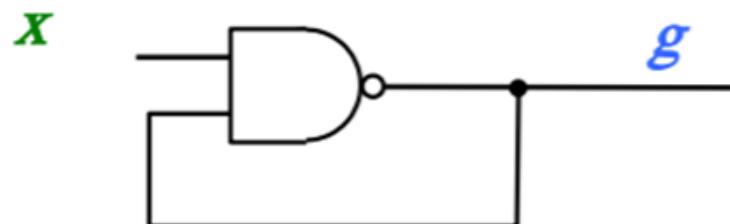


$x$	$g_t$	$g_{t+1}$	
0	0	1	
0	1	1	
1	0	1	
1	1	0	

If  $x = 0$ , then  $g$  is driven to one.

If  $x = 1$ , then  $g$  is negated.

# Key Observation

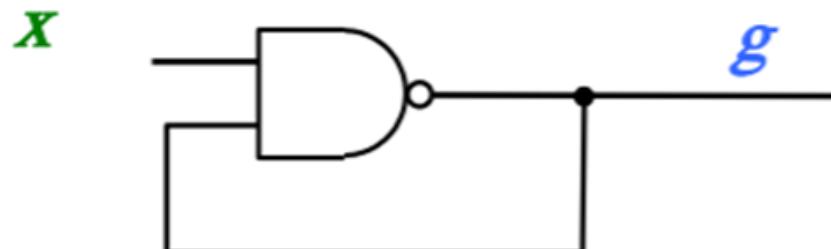


If a NAND's **control line** is 1, then that NAND just **negates** its **data line**. If the **control line** is 0, then the NAND's output is *driven* to 1, ignoring its **data line**.



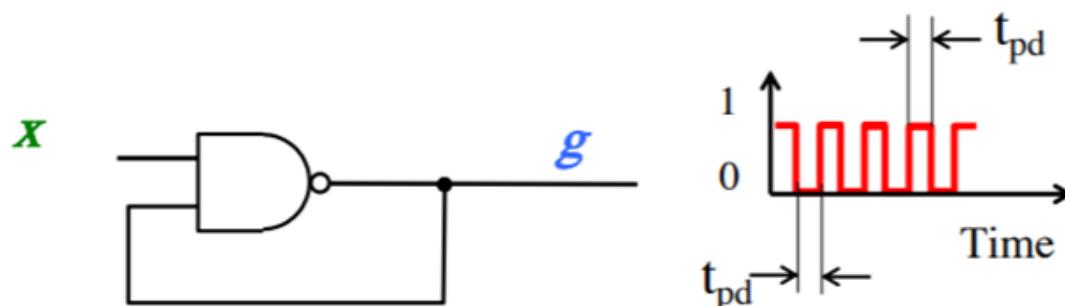
# Output Oscillations

What would happen to ***g*** if we keep ***x=1*** for a long time?



# Output Oscillations

What would happen to  $g$  if we keep  $x=1$  for a long time?

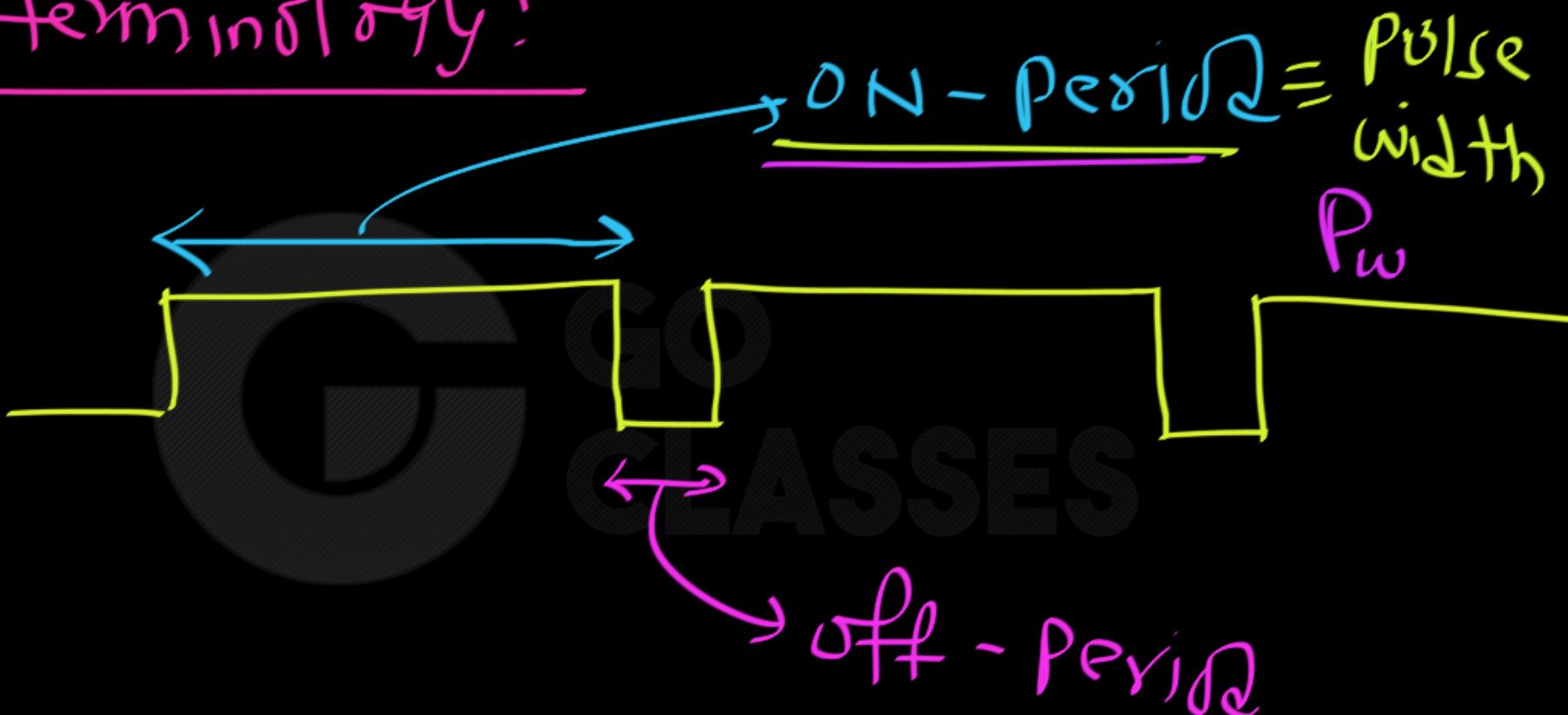


$t_{pd}$  is the propagation delay through the NAND gate, which is small, but not zero.



Some terminology:

Clock

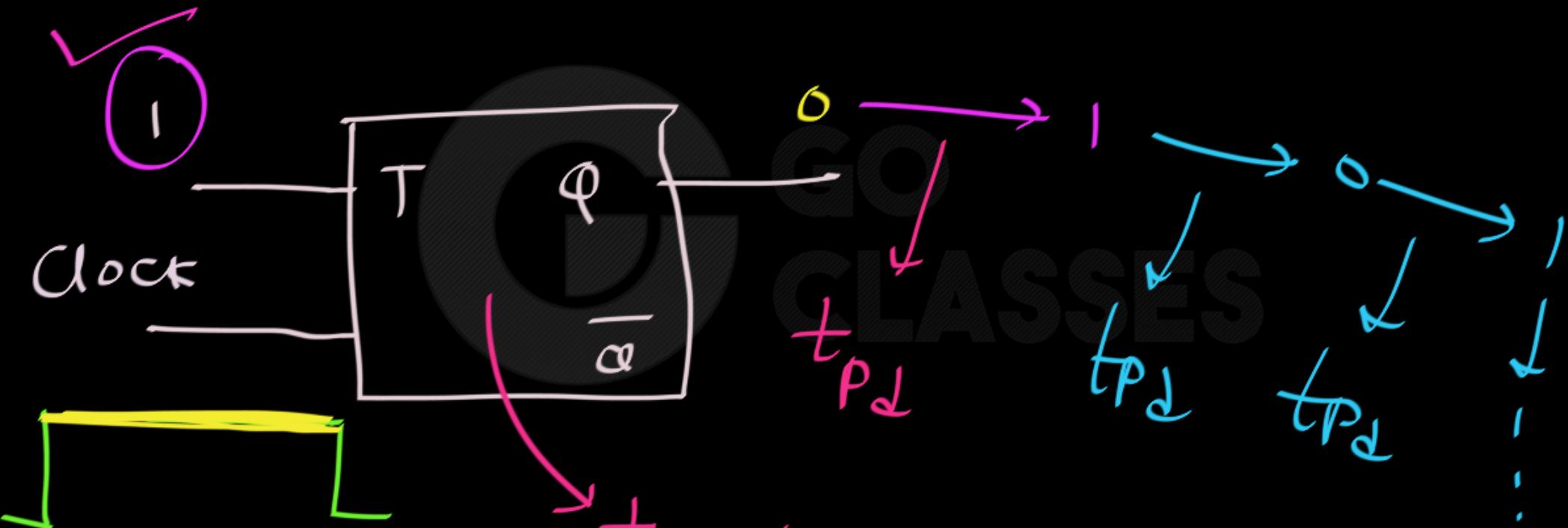




## Next Topic:

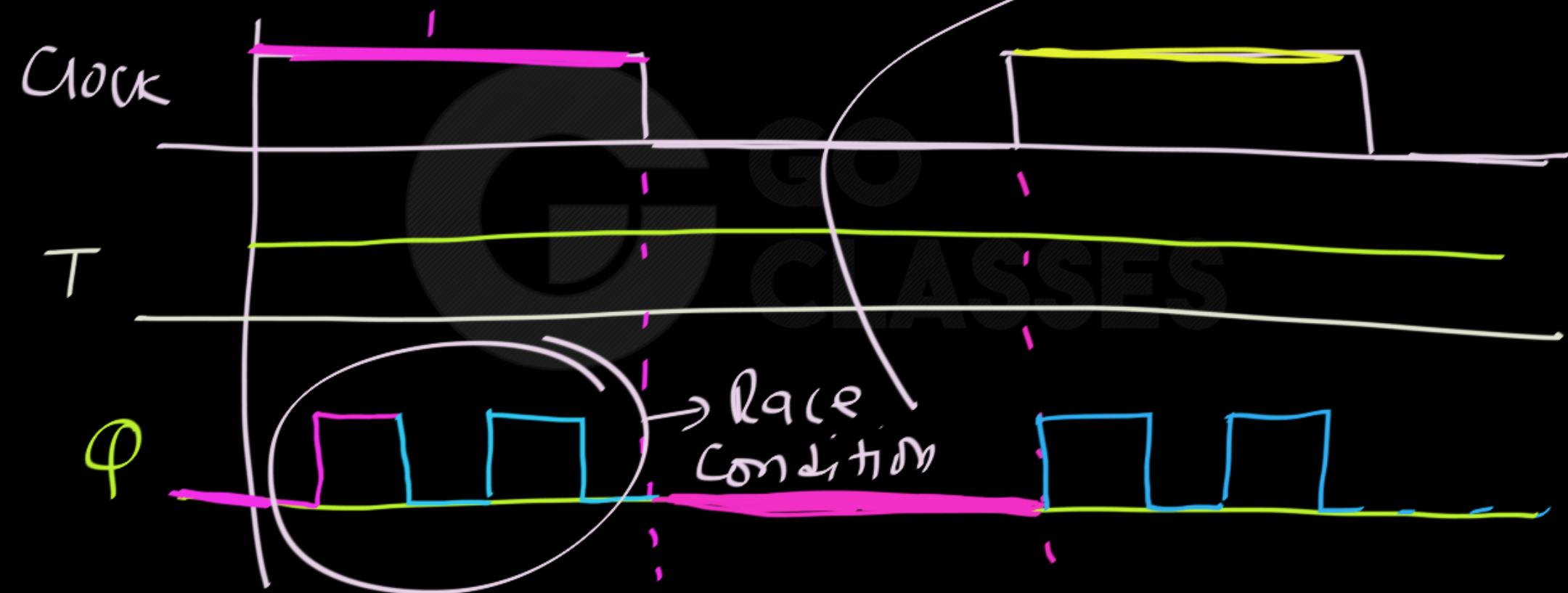
# Race Condition in JK, T Flipflop

the Level Triggers T-FF :



$t_{PD} = \text{prop. Delay of T-FF}$

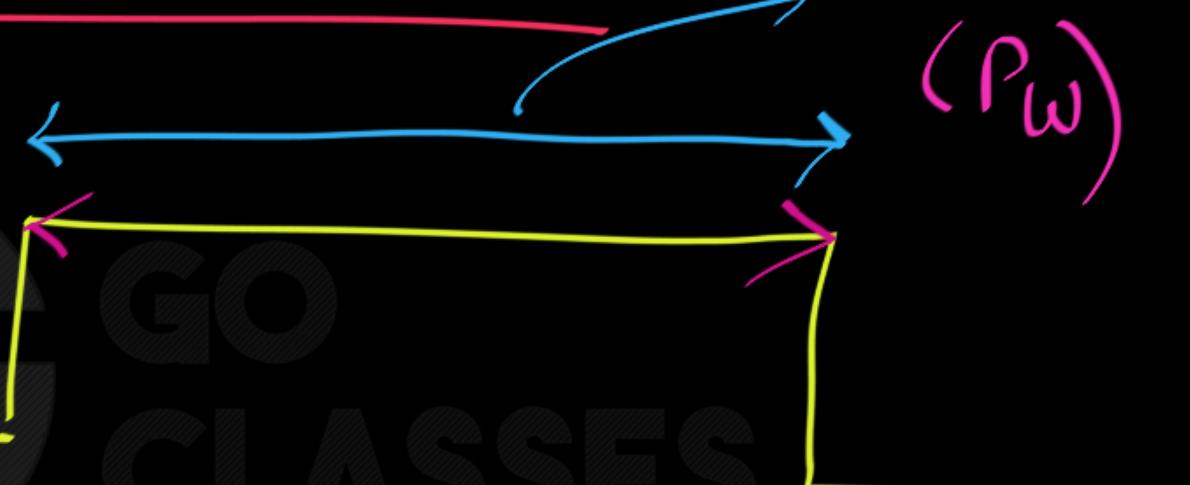
the Level Triggered T-FF : problem



+ve level Triggered T-ff ; on-period

Race Condition  
Problem.

Clock



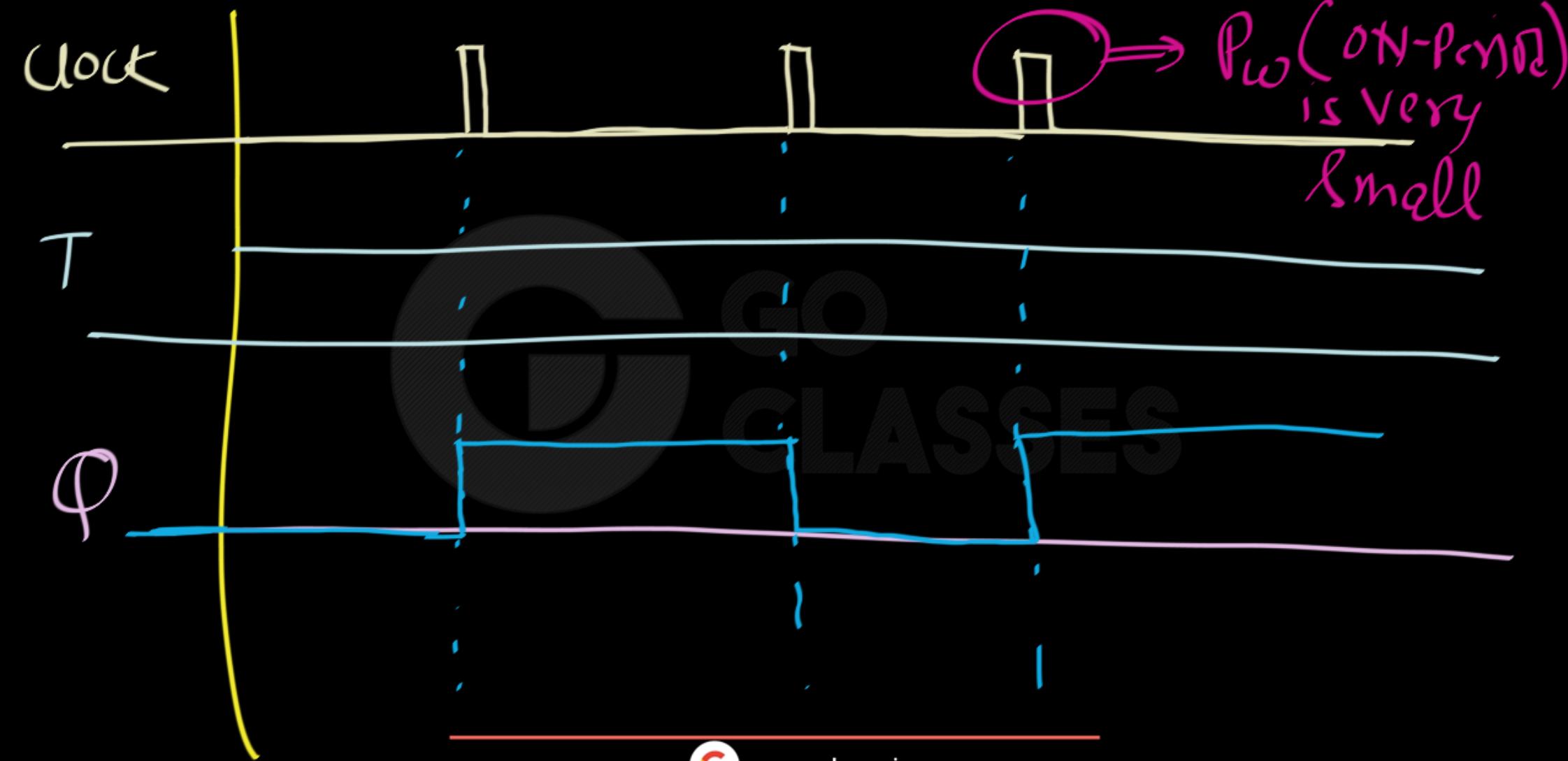
① level  
Triggering

AND

②  $T=1$

ANd

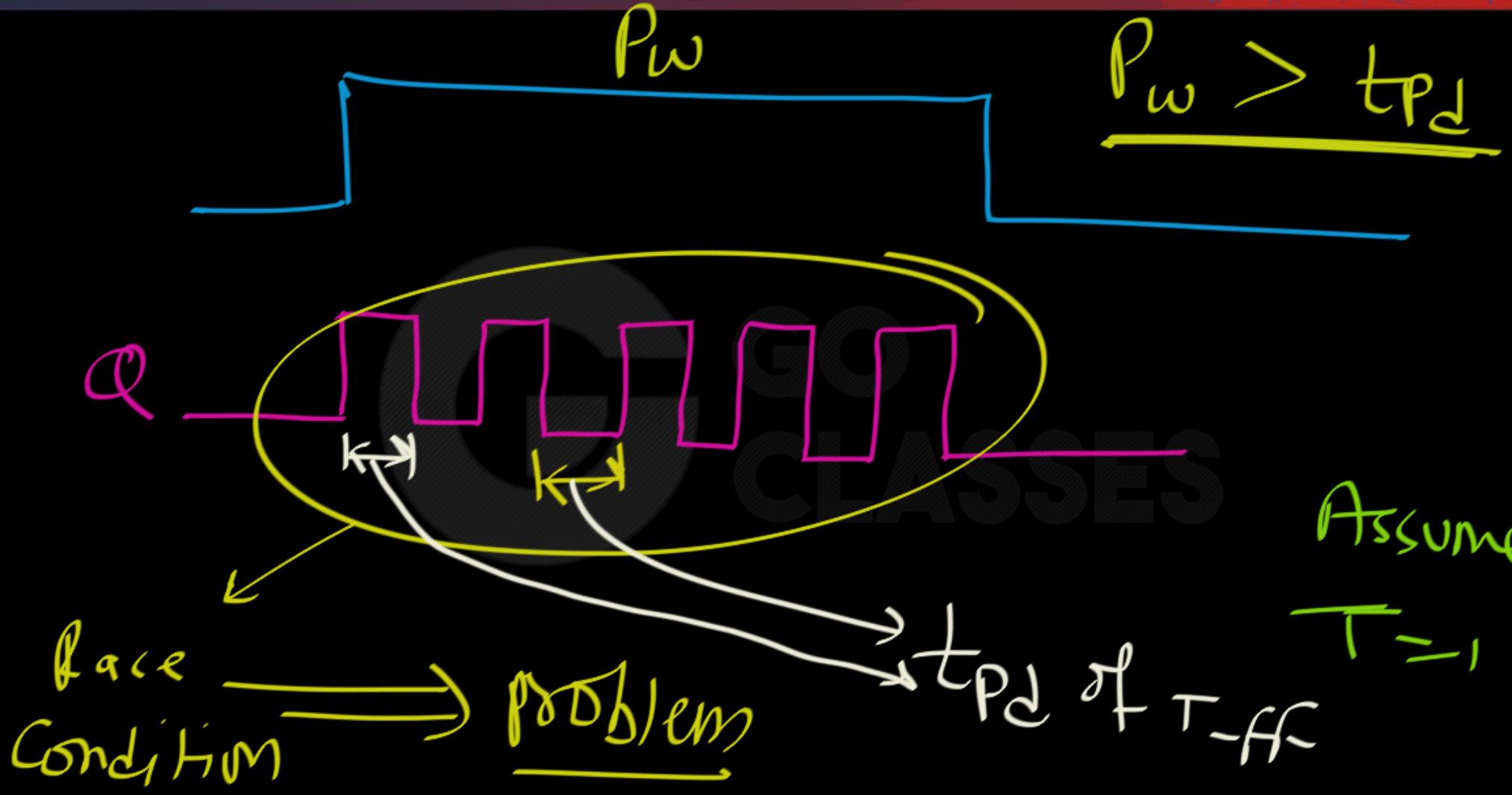
$P_w > t_{pd}$



T-ff suffers from Race Condition:

① Level Triggering

②  $P_w \text{ (on-N-period)} > t_{PL} \text{ of FF}$





Solutions:

$$\textcircled{1} \quad P_w(\text{on period}) < \frac{t_{PD}}{\tau}$$

Not Practical Solution

keeps changing  
(Reasons: Heat, Temp - - -)



Solution :

② Edge Triggered ff

✓ ✓ ✓



③ Use M-S CLASSES

✓ ✓ ✓

Clock

D<sub>0</sub>





Q: Edge Triggered FF

means

MS FF (?)

GO  
CLASSES



Q: Edge Triggered FF

means

MS FF (?)



Several ways to create Edge

Triggered FF

M5-FF is one of them



Race Condition Problem exists in

any ~~iff~~ which has a Toggle  
Condition.

Eg: T - ff ; Jk - ff



SR-FF

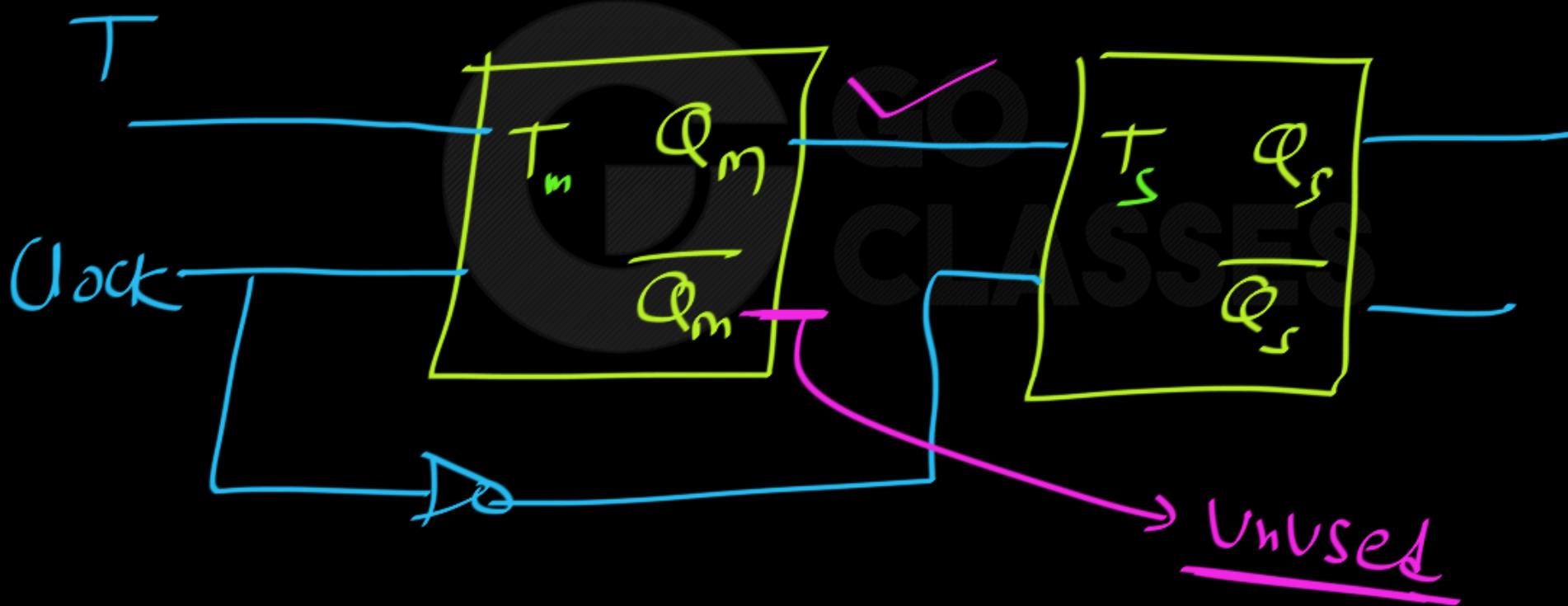
D-FF

Any Edge Triggered FF

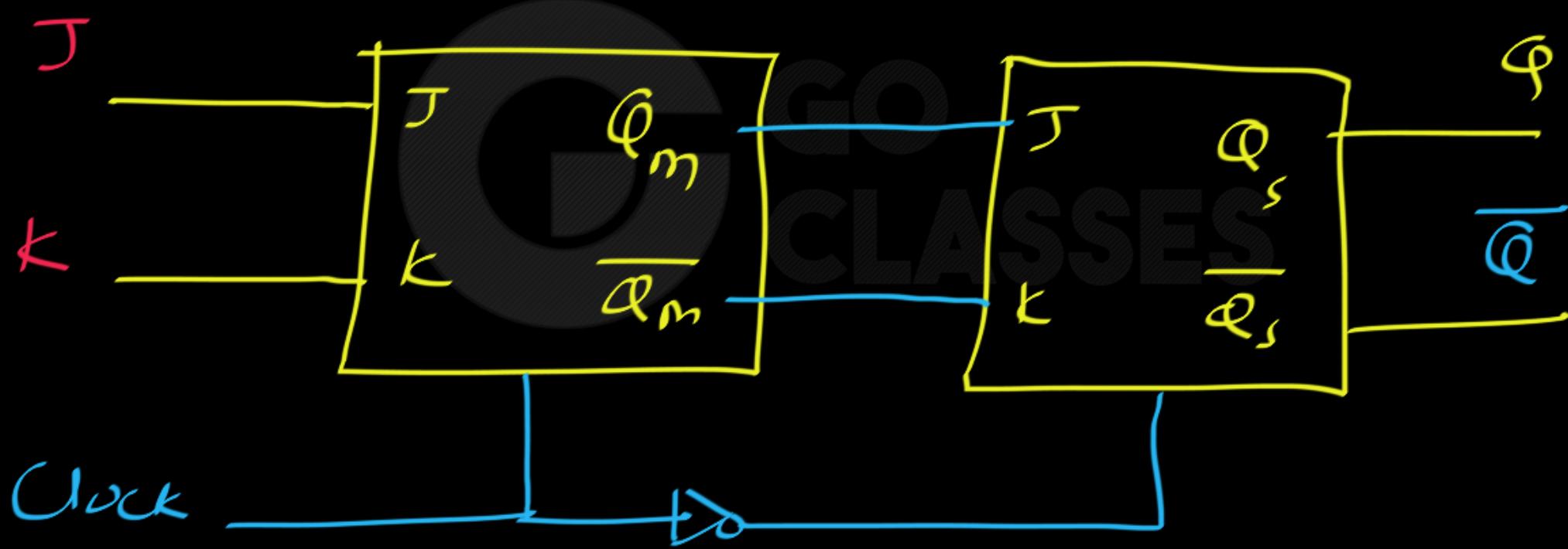
Any MS FF

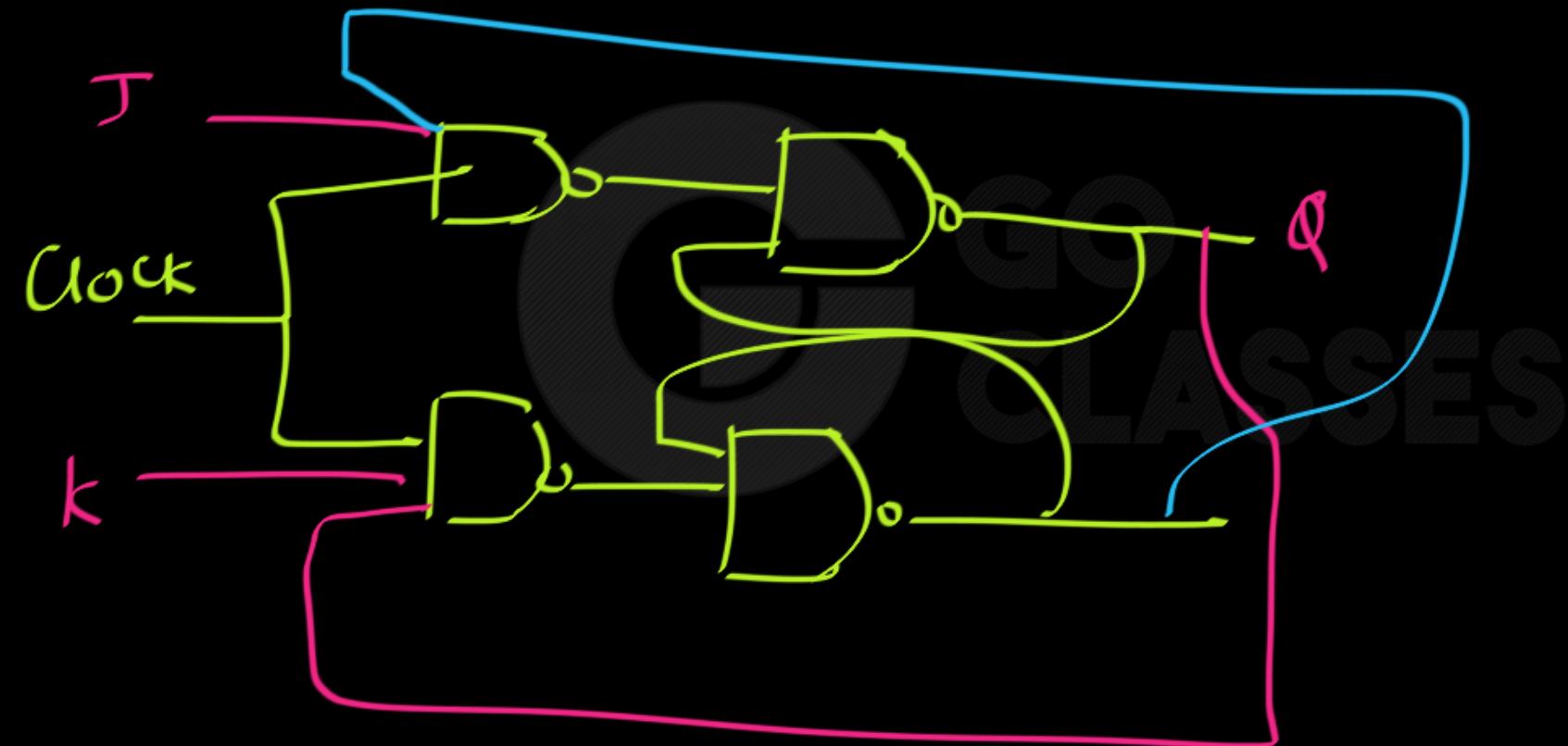
No  
⇒ Problem  
of  
Race Condition

M S - T - FF :

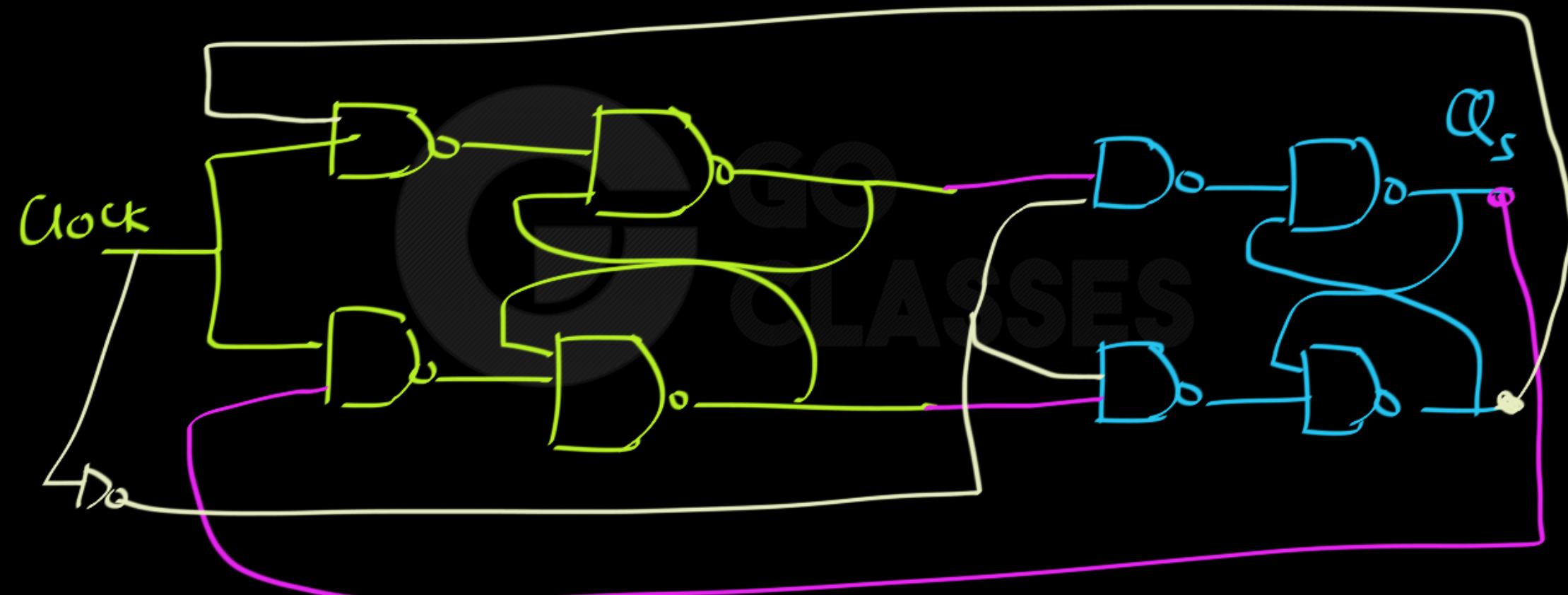


Ms-JK-ff :- Block Diagram:



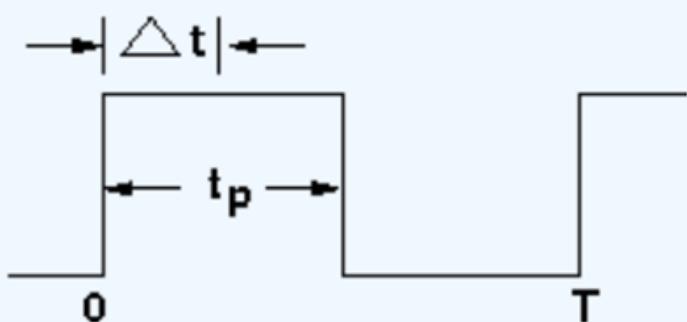
JkImplementation:

# M5-Tk Implementation:

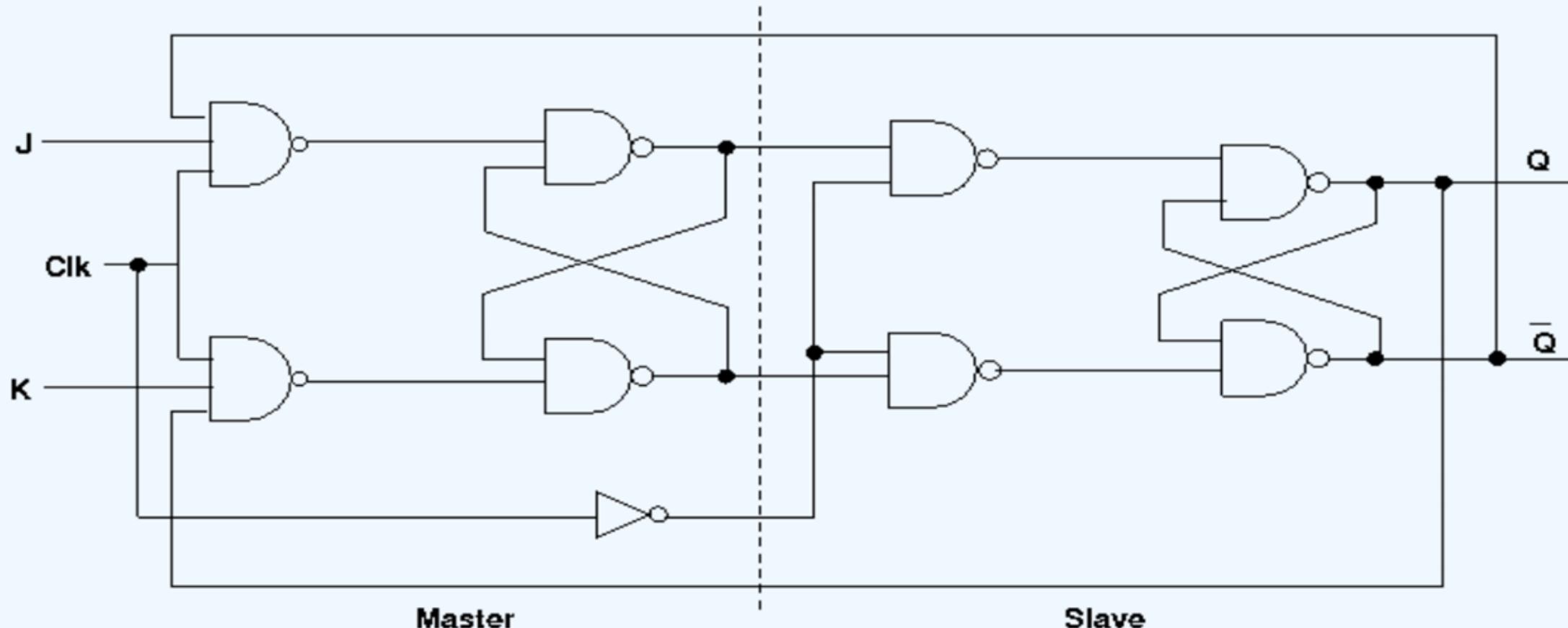




In level triggered JK flip-flops, at  $J=1$  and  $K=1$ , a timing problem, known as race around condition arises which can be explained by the following diagram. Let the width of a clock pulse is  $t_p$  and the current output  $Q$  is 1. When the clock is applied, after the propagation delay, say  $dt$ , the output will toggle and now the output  $Q$  will be 0. If  $dt$  is less than  $t_p$ , then after  $dt$  the output  $Q$  will again toggle and become 1. Thus the output will oscillate between 0 and 1 within the  $t_p$  interval, so at the end of the clock pulse  $t_p$ , the output will be ambiguous.



Master slave JK flip-flop overcome this race around condition. The following figure depicts the circuit diagram.





**Race Around Condition In JK Flip-flop** – For J-K flip-flop, if  $J=K=1$ , and if  $clk=1$  for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop. This problem (Race Around Condition) can be avoided by ensuring that the clock input is at logic “1” only for a very short time.



In JK flip-flop, while a Clock signal remains a 1 (while  $J=K=1$ ); after the outputs have been complemented once, will cause repeated and continuous transitions of the outputs.

To avoid this, the clock pulses must have a time duration less than the propagation delay through the flip-flop.

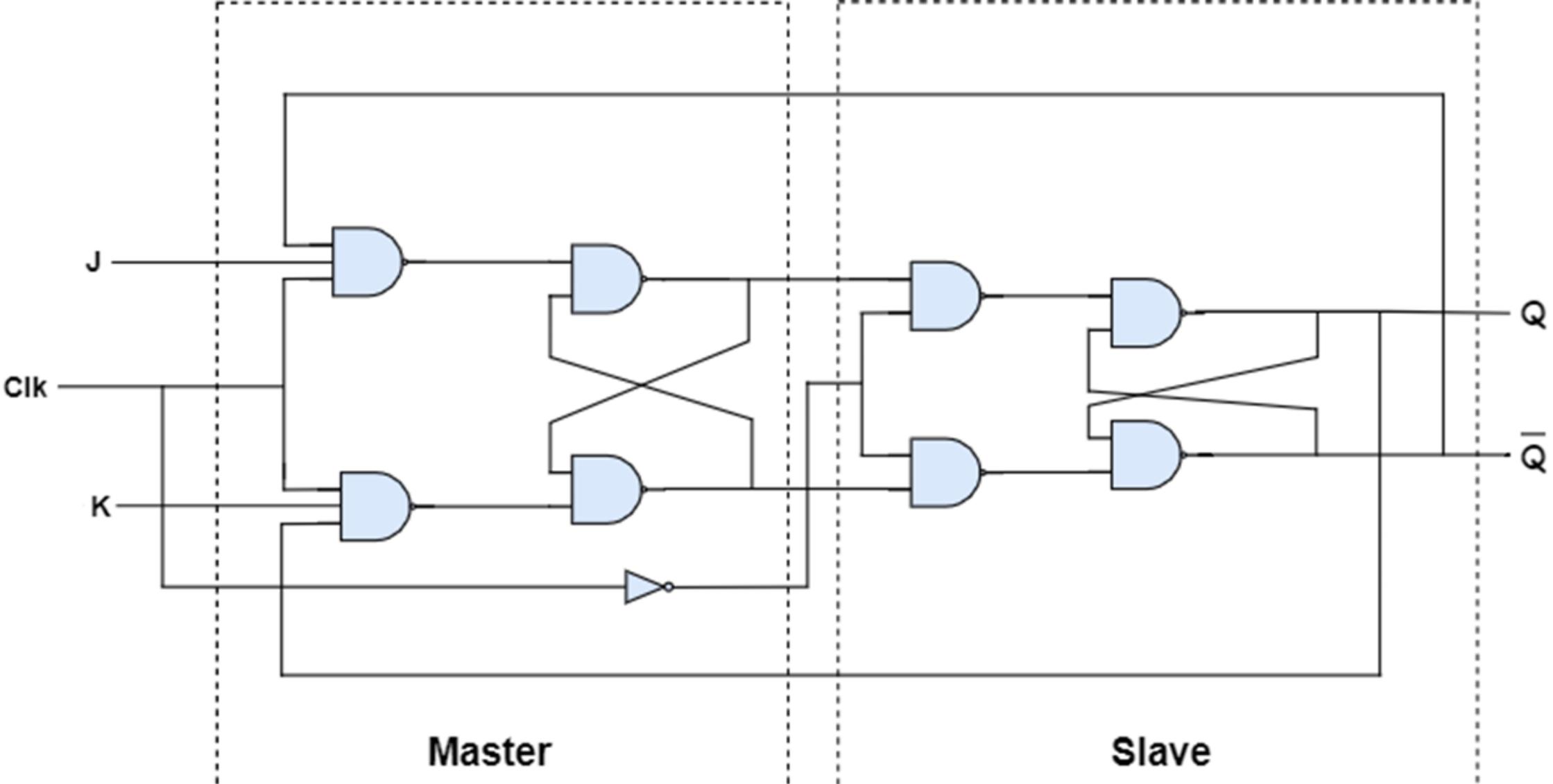
The restriction on the pulse width can be eliminated with a master-slave or edge-triggered construction.



## Master Slave JK Flip Flop

The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the “**master**” and the other as a “**slave**”. The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop.

In addition to these two flip-flops, the circuit also includes an **inverter**. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop. In other words if  $CP=0$  for a master flip-flop, then  $CP=1$  for a slave flip-flop and if  $CP=1$  for master flip flop then it becomes 0 for slave flip flop.





JK - ff  $\longrightarrow$  Suffers with  
Race cond? No



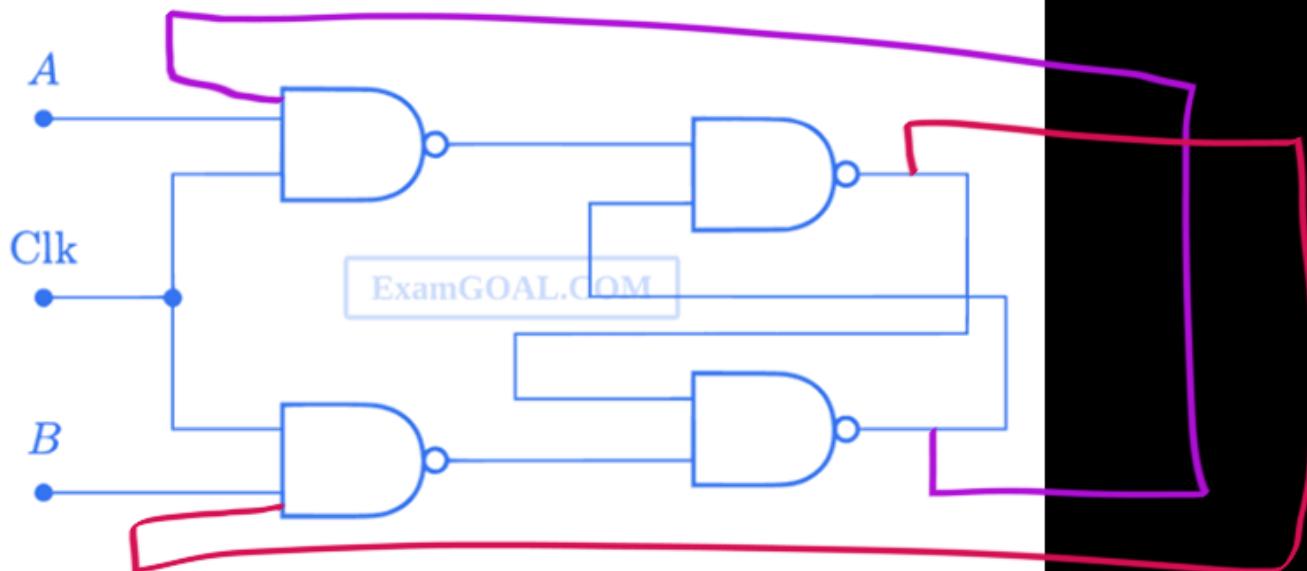


Level Triggers → Suffers with Race cond? Yes





Consider the given circuit. In this circuit, the race around

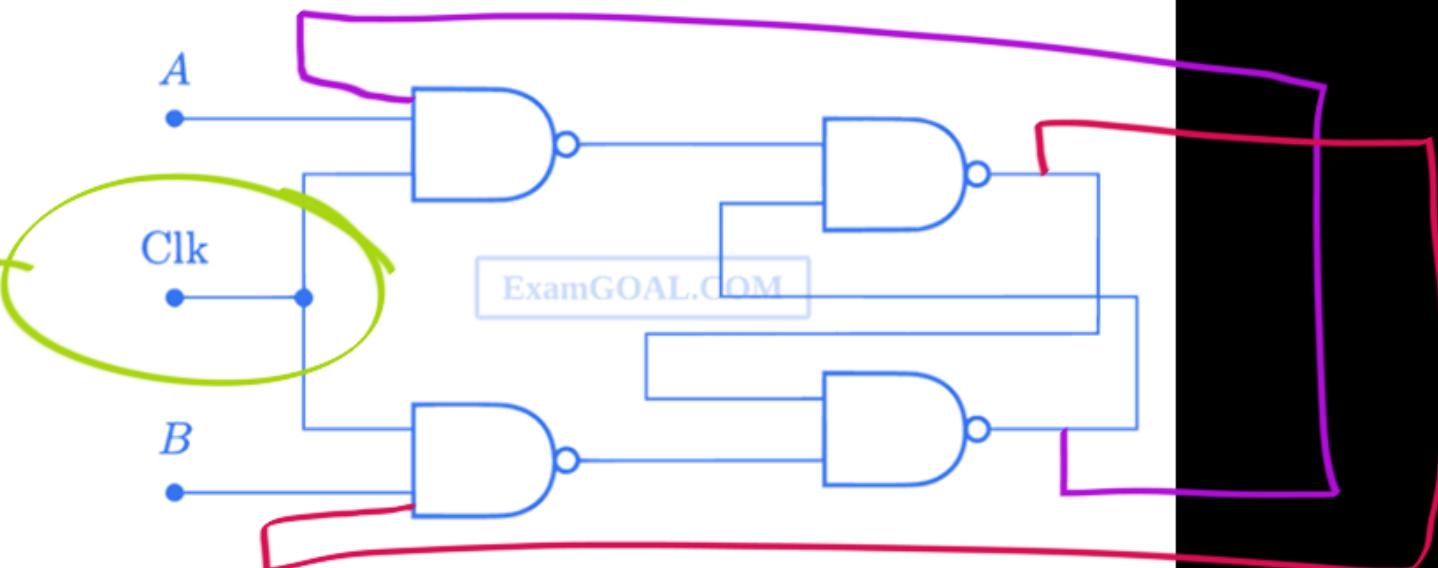


- A does not occur
- B occurs when CLK = 0
- C occurs when CLK = 1 and A = B = 1
- D occurs when CLK = 1 and A = B = 0

Consider the given circuit. In this circuit, the race around

Tk - ff

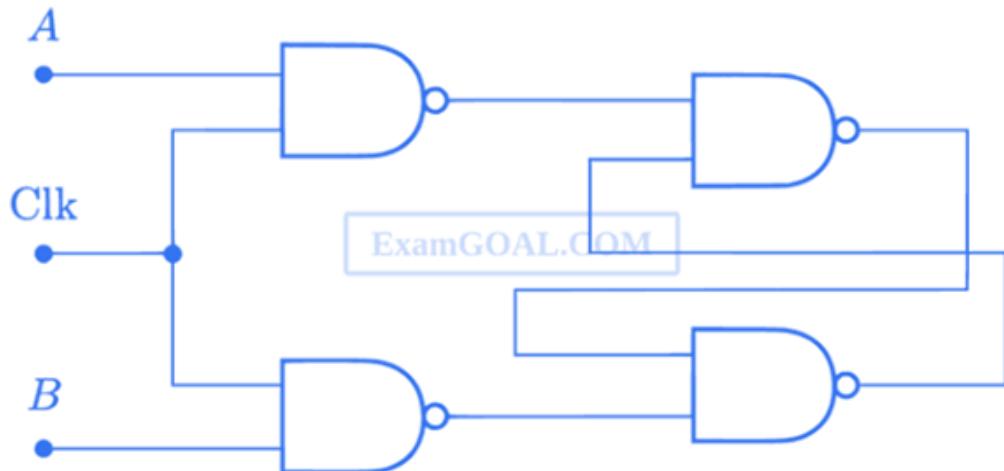
level  
triggered



- A does not occur
- B occurs when CLK = 0
- C occurs when CLK = 1 and A = B = 1
- D occurs when CLK = 1 and A = B = 0



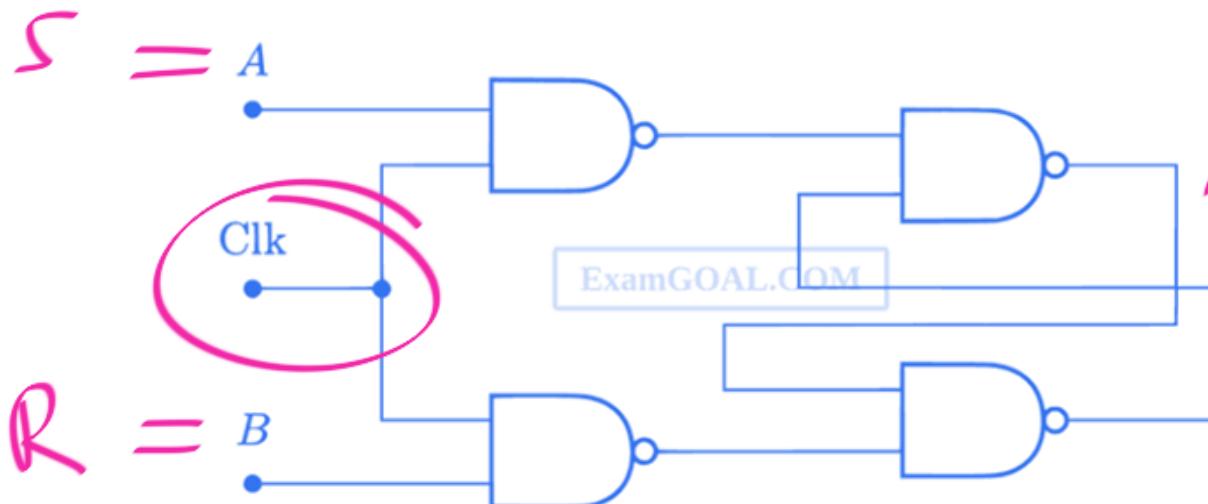
Consider the given circuit. In this circuit, the race around



- A does not occur
- B occurs when CLK = 0
- C occurs when CLK = 1 and A = B = 1
- D occurs when CLK = 1 and A = B = 0



Consider the given circuit. In this circuit, the race around



$$R = B$$

$$S = A$$

- A does not occur

- B occurs when CLK = 0

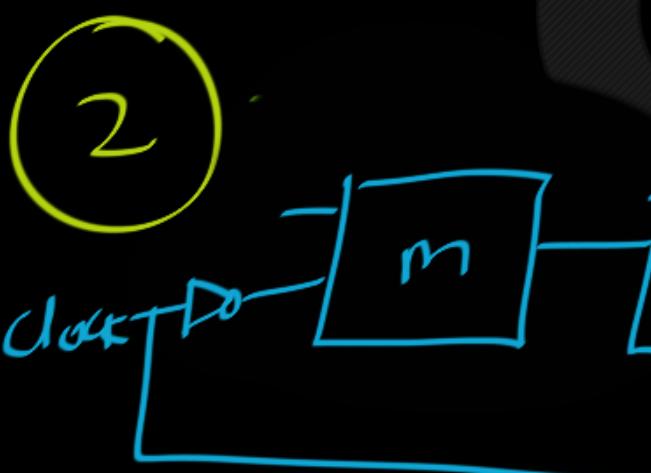
- C occurs when CLK = 1 and A = B = 1

- D occurs when CLK = 1 and A = B = 0



Conclusion : equivalent to

① MS -ff-  -Ve Edge Trig. ff

②   +Ve " "

- ③ Any "Level-Triggered" ff with "Toggle Condition" suffers from Race Condition.



(4)

SR - FF

D - FF

any Edge - Trig

FF

MS - FF

No

RaceCondition

Problem