



Timing Issues in flip flop : Hold Time, Setup Time

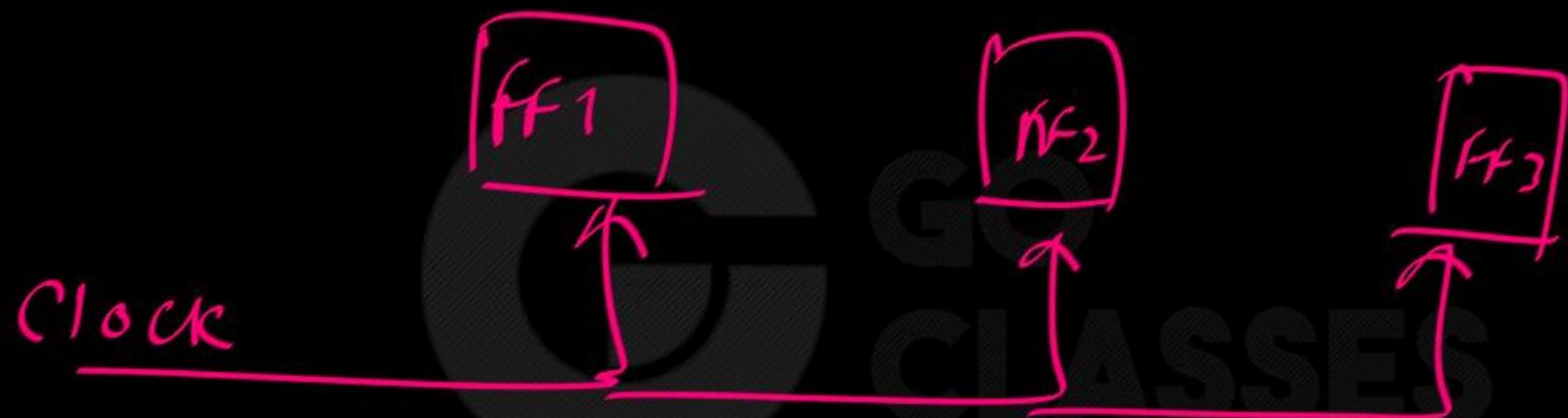
In the last few lectures if you recall, we had discussed the various types of latches and flip flops, and how they work. We talked about both edge triggered and the master slave variations of flip flops, which are very useful in designing synchronous sequential circuits. But there are some timing issues which you have not discussed so far; for instance, what should the clock frequency be, what is the maximum frequency with which a circuit can operate without any errors and so on and so forth. So, we shall try to address some of these issues in this lecture.



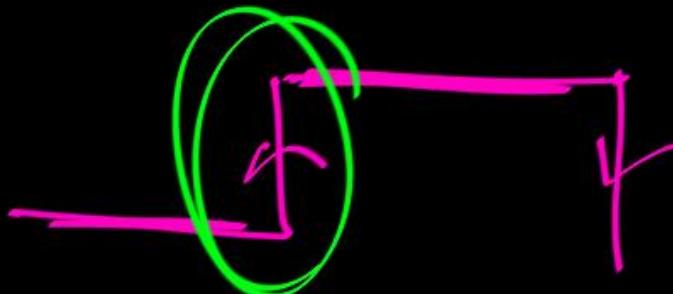
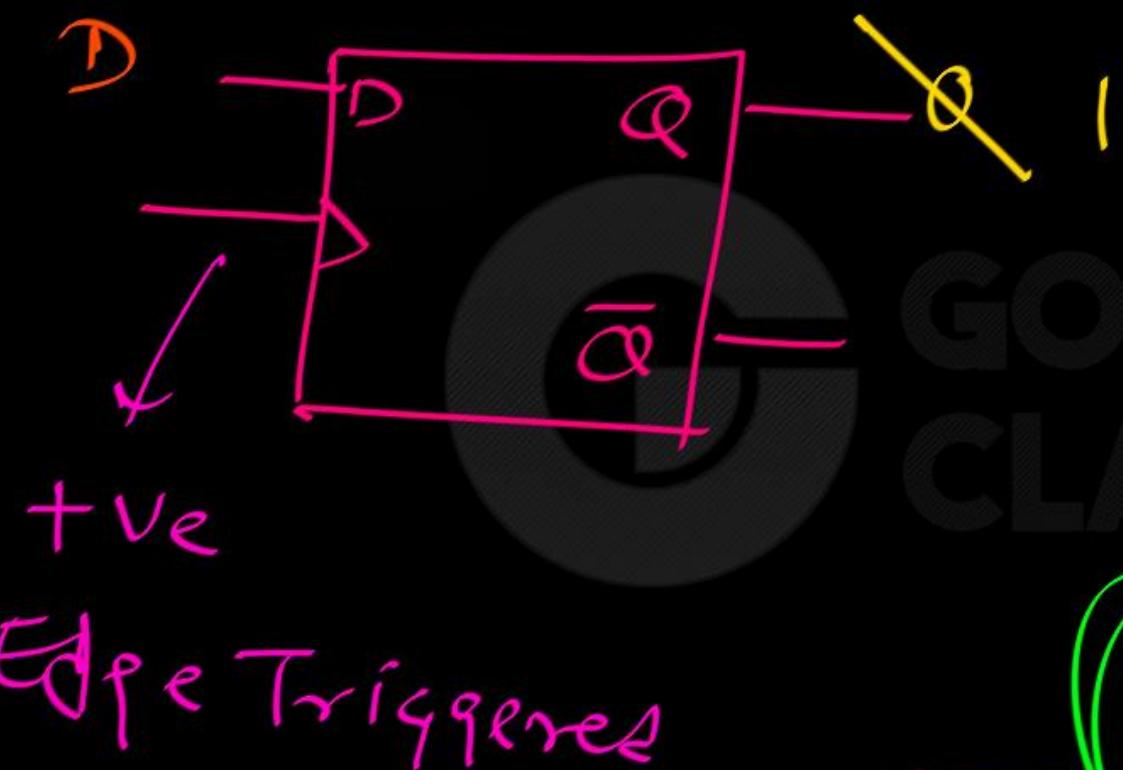
let us first try to understand why timing issues are important in a synchronous sequential circuit.

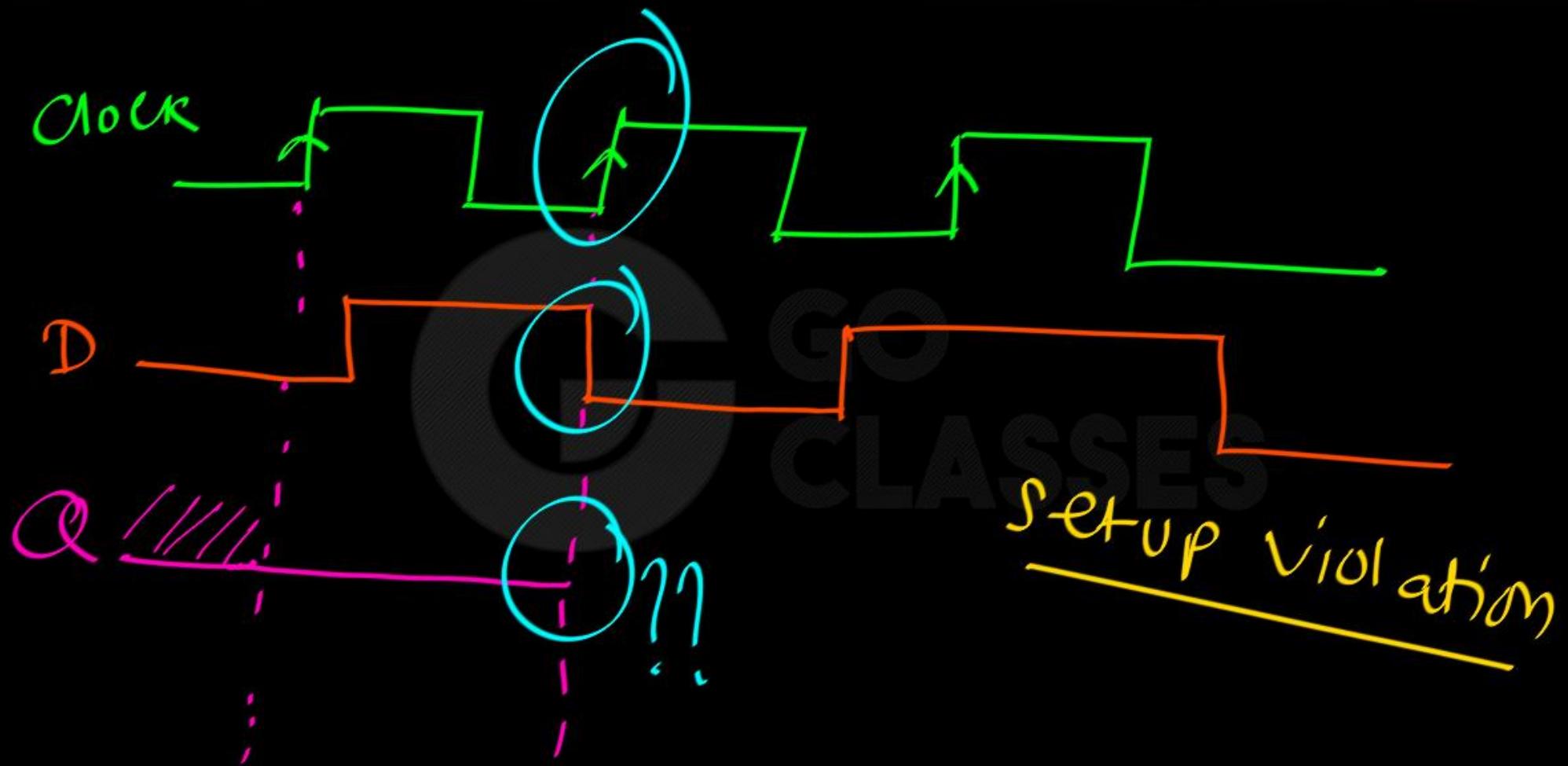
Now, remember that a sequential circuit is said to be **synchronous** if there is a clock, and this same clock is applied to all flip flops and all state changes and outputs are generated in synchronism with the clock. So, synchronous sequential circuit means that; there is a clock which is fed to all the flip flops, and the flip flops would be working, would be changing the states in synchronism with the clock edges.

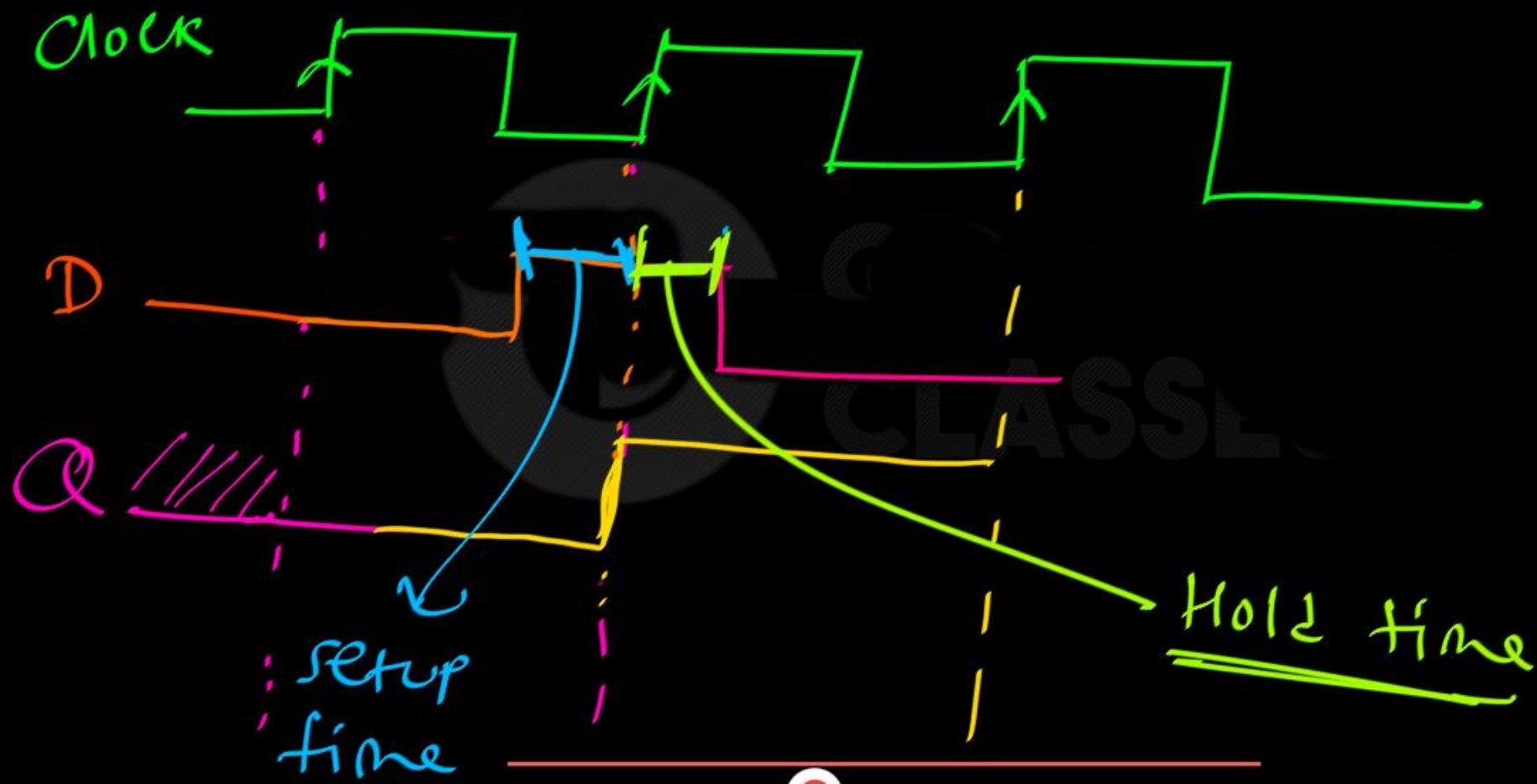
Synchronous Seq. ckt:

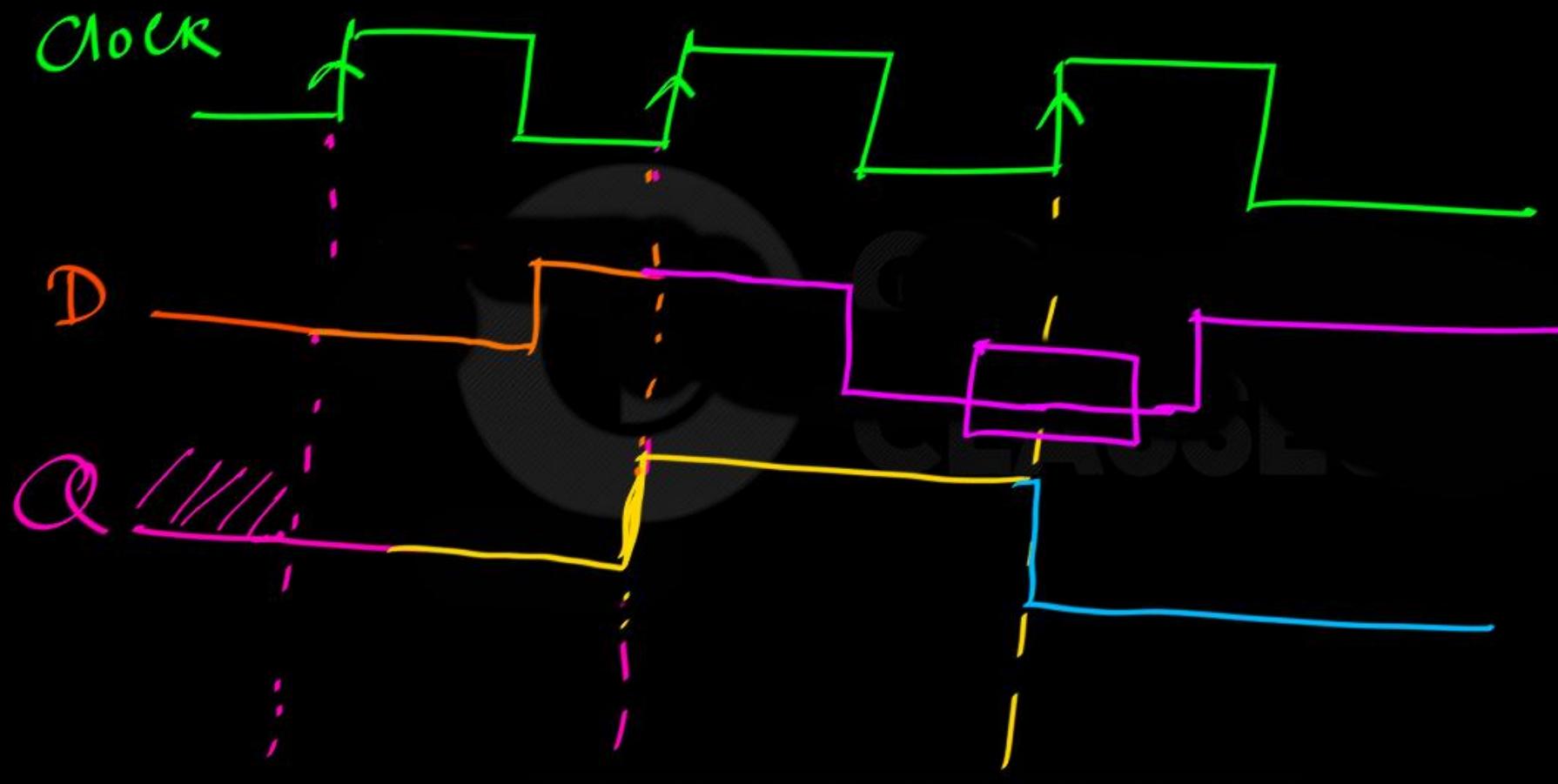


Timing Issues : { Hold time } edge triggered flip flops

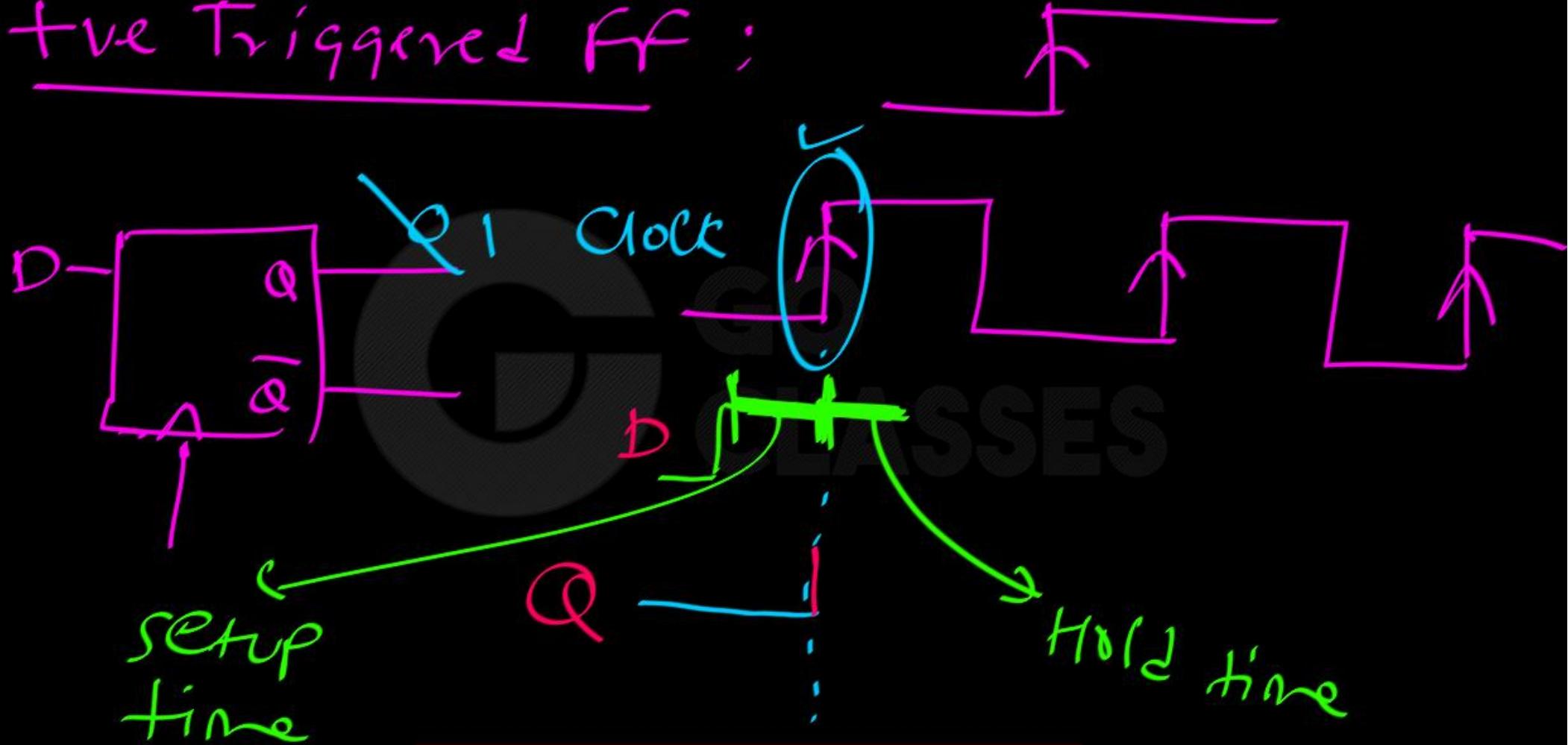








+ve Triggered FF :



Setup time: When the Triggering edge comes, minimum how much earlier our steady state is called setup time.

Hold time: After the Triggering edge comes, minimum how much longer our steady state is called Hold time.



Digital Logic

NOTE that flip flops are usually edge triggered.

Triggering edge can be either rising edge(positive edge) or falling edge(negative edge).





Now as we said there are several timing issues that need to be considered. Now these timing issues relate to some properties of the flip flops, for example :

Given a flip flop, when the clock edge arrives, the question is; when should we apply the data inputs ?

Consider a D flip flop; some value should be applied to D and then the clock pulse(edge) should be applied i.e. the triggering clock edge should come.



Now, minimum how much time before which the data should arrive, and only then the clock edge come, these timing constraints should be considered.

And also after the clock edge come, how much more time I should hold my input data steady so that the data can go inside the flip flop and flip flop can produce the output without any problem.

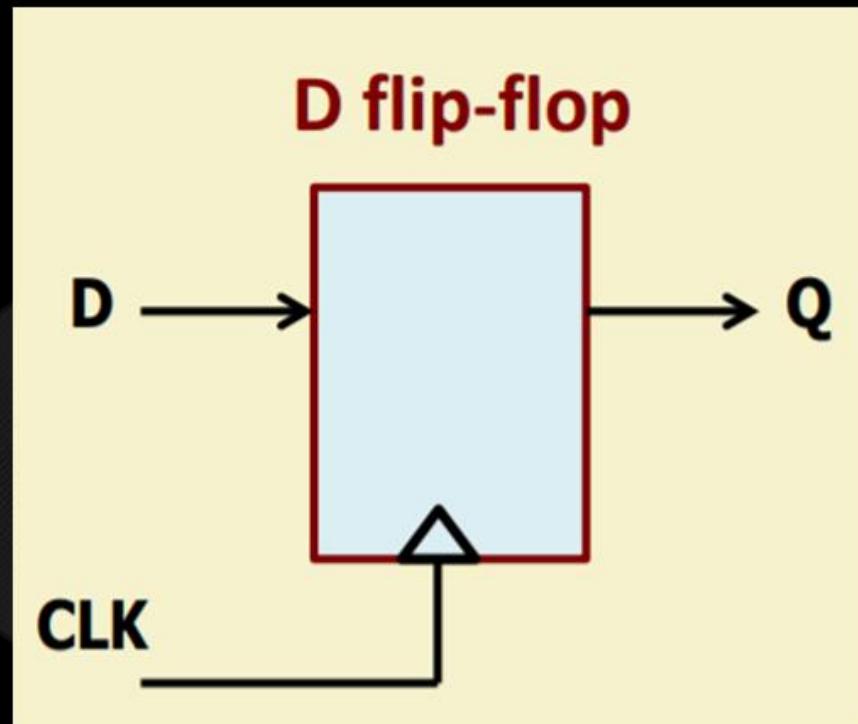
These are some issues which relate to the properties of flip flops, and decide how fast they are and so on.



Digital Logic

So, we shall be considering all of these, all of these taken together will determine the maximum speed of operation of the circuit and we normally designate the maximum speed of operation in terms of the clock frequency.





+ve Edge Triggers ff:

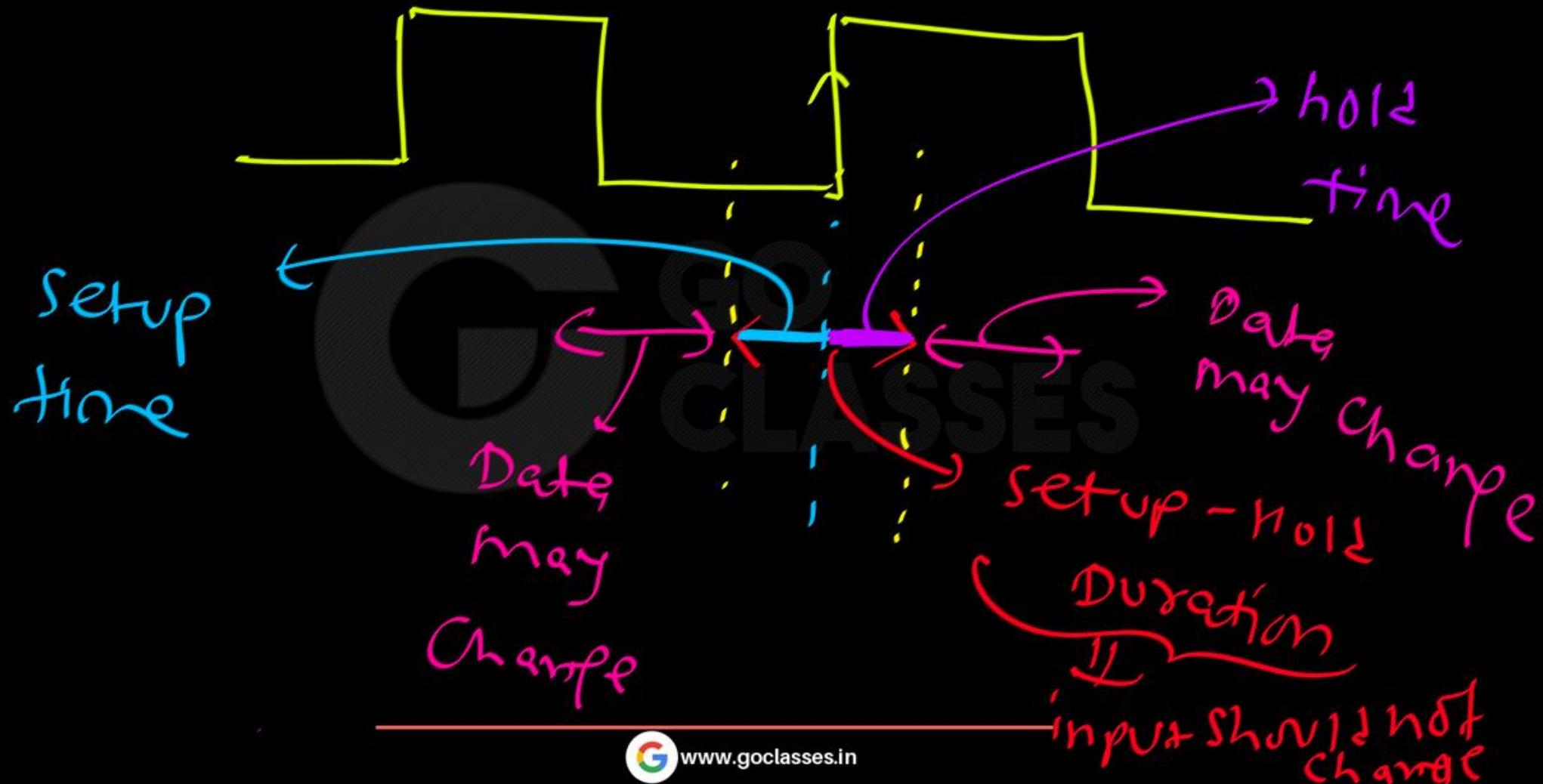


D ff ; input : D

SR ff ; " : S, R

JK ff ; " : J, K

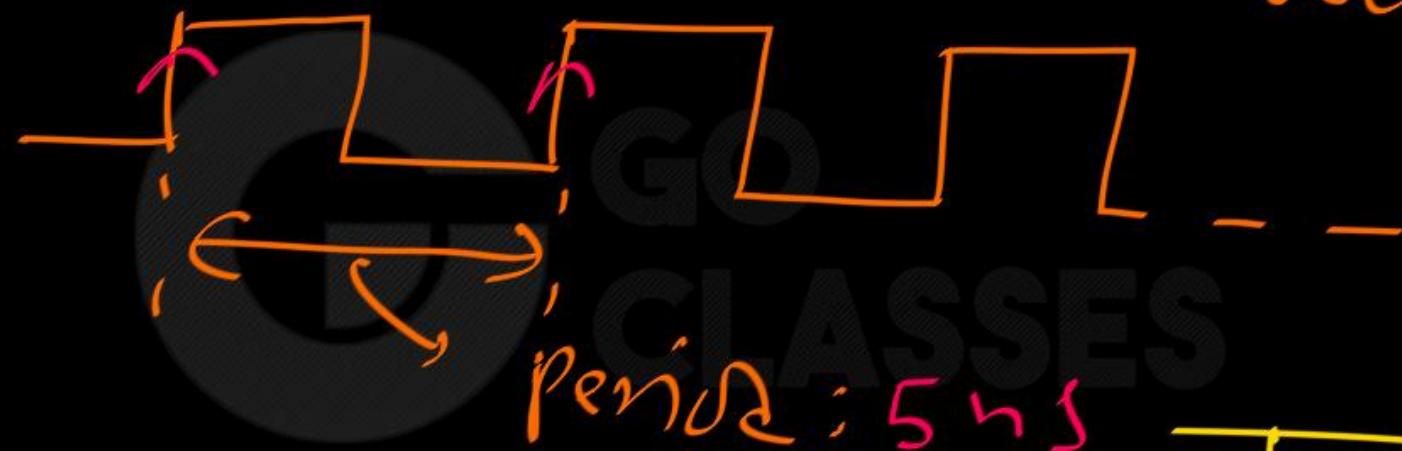
T ff ; " : T





period ↑
frequency ↓

Clock frequency: oscillations per second.



frequency:

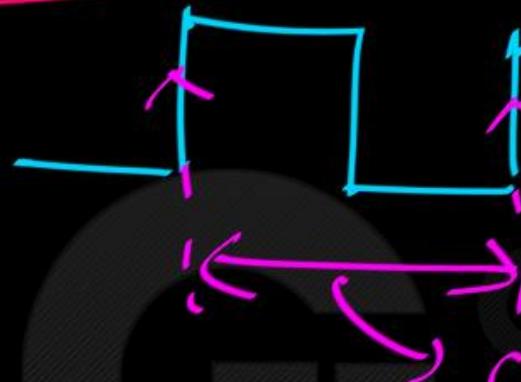
$$\frac{1}{\text{Period}} = \frac{1}{5 \text{ ns}} = \boxed{\frac{1}{5} \text{ GHz}}$$

$$h : 10^{-9}$$

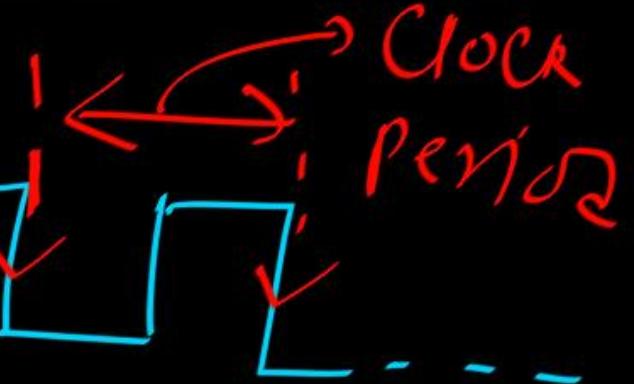
$$c : 10^9$$

$\cancel{s} : \text{per second} \doteq$  unit
of frequency

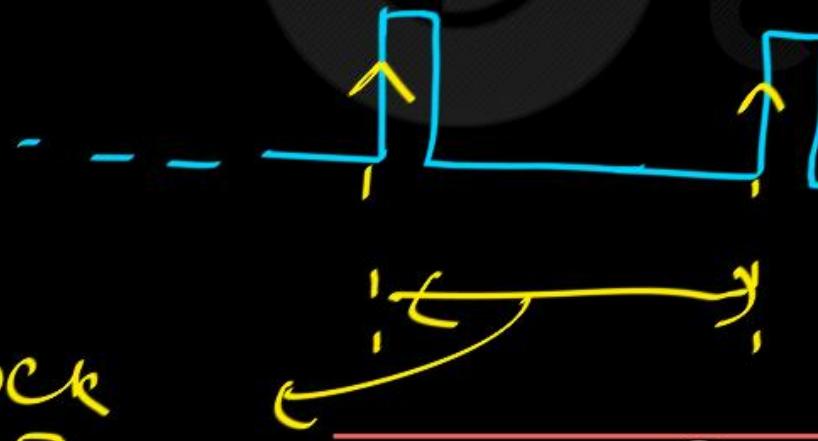
Clock period:



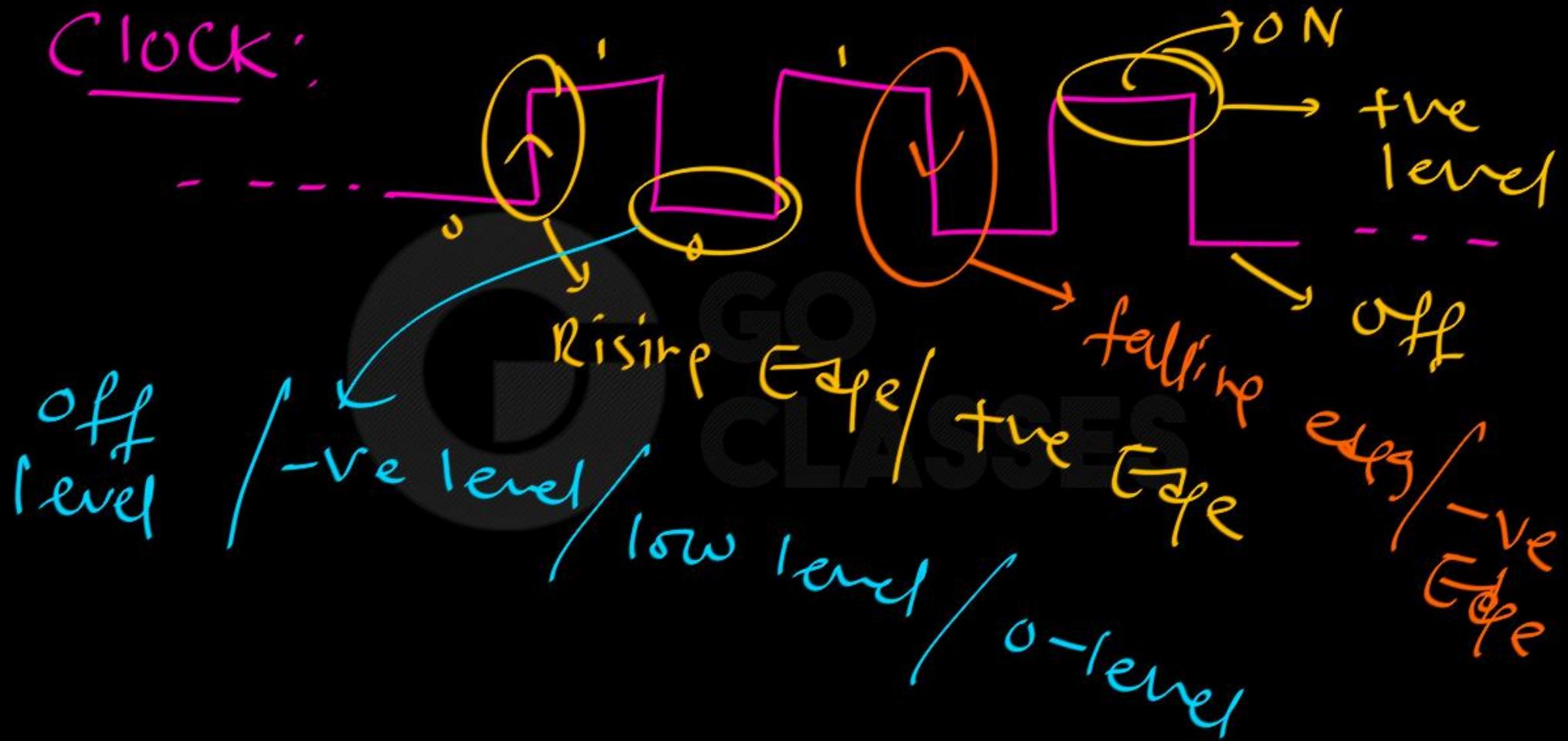
Clock period



Clock period



Clock period

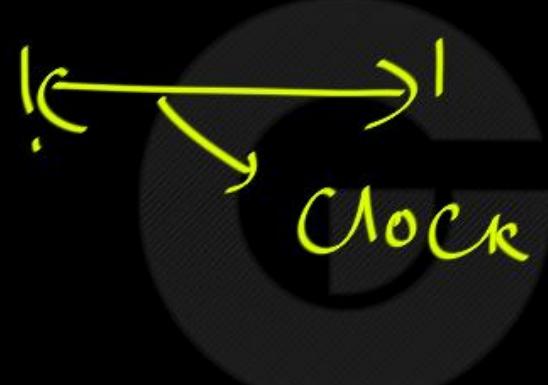
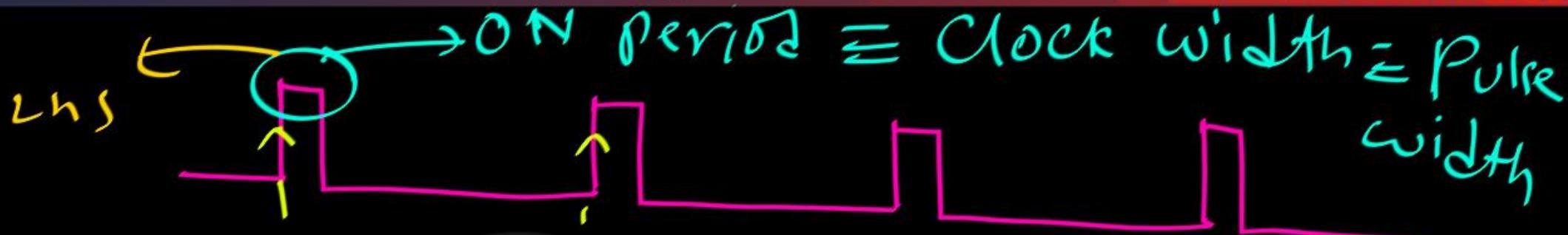


Some Definitions :

- Clock width/Pulse width (PW):

In a period, Time duration for which the clock signal is high.





GO
CLASSES

$$\text{Period} = 10\text{ns}$$

Duty cycle: $\frac{2\text{ns}}{10\text{ns}} \times 100\% = 20\%$



Some Definitions :

- Duty cycle or Power cycle :

Duty cycle of a clock is defined as the fraction of a period of clock during which the clock is in active/ON state.

Duty cycle of a clock is normally expressed as a percentage. For instance, figure below shows a clock having an active/ON state for 2 ns during its period of 10 ns. It is, therefore, said to have a duty cycle of 20%.



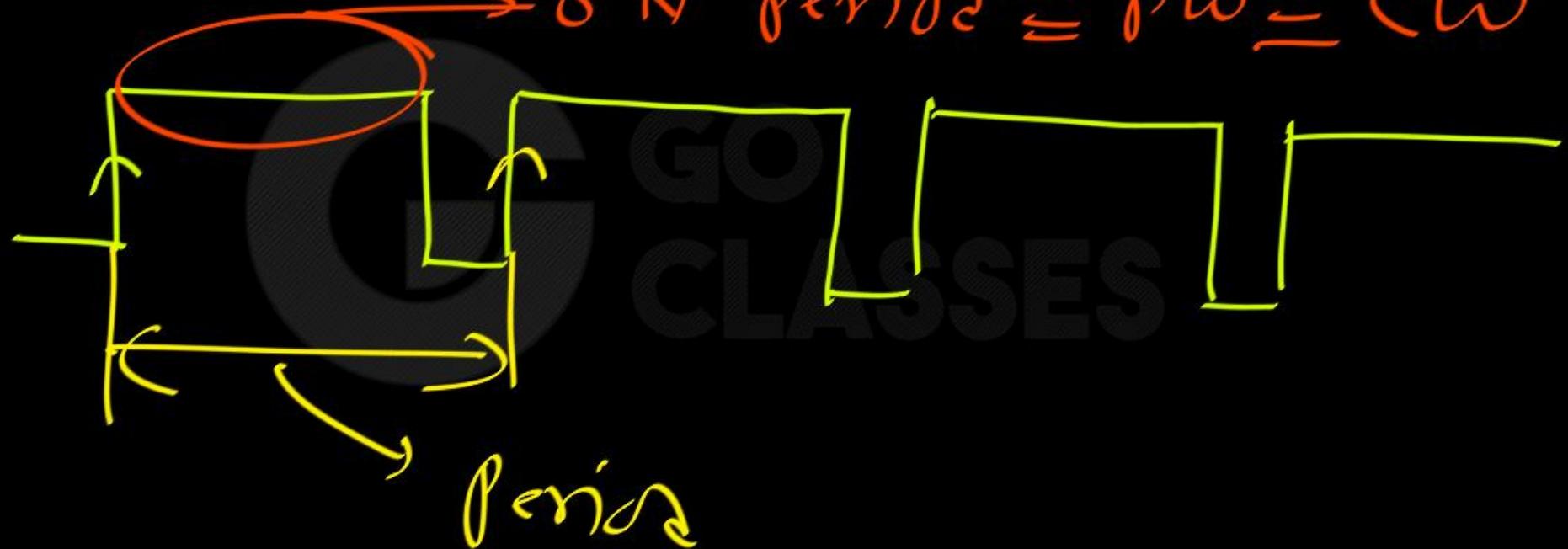
Clock with period of 10 ns and duty cycle of 20 %

Duty cycle: % of on time
in a clock period.

$$\text{Duty Cycle} = \frac{\text{Pw}}{\text{Clock Period}} = \frac{\text{ON period}}{\text{Clock Period}}$$

Duty cycle : 80%

On period = PW \equiv CW





Some Definitions :

- Setup time (T_{setup}):

Amount of time the input to a flip-flop must be stable before the clock transitions high (for positive-edge triggered), or transitions low (for negative-edge triggered).



The setup time is defined as the amount of time the input to a flip flop, the time the inputs of a flip flop must be applied and must be held stable before the clock transition comes.

Input to a flip flop means it can be a D input for a D flip flop, it can be S and R input for an SR flip flop, J and K for J K flip flop and so on.



So, this is the duration for which my data remains stable before the clock edge that is defined as the setup time. And setup time is a characteristic of the flip flop that you are using depending on the flip flop that you use, it has a specified setup time and the input must be applied at least before that amount of time.





Some Definitions :

- Hold time (T_{hold}): Amount of time the input to a flip-flop must be stable after the clock transitions high (for positive-edge triggered), or transitions low (for negative edge triggered).

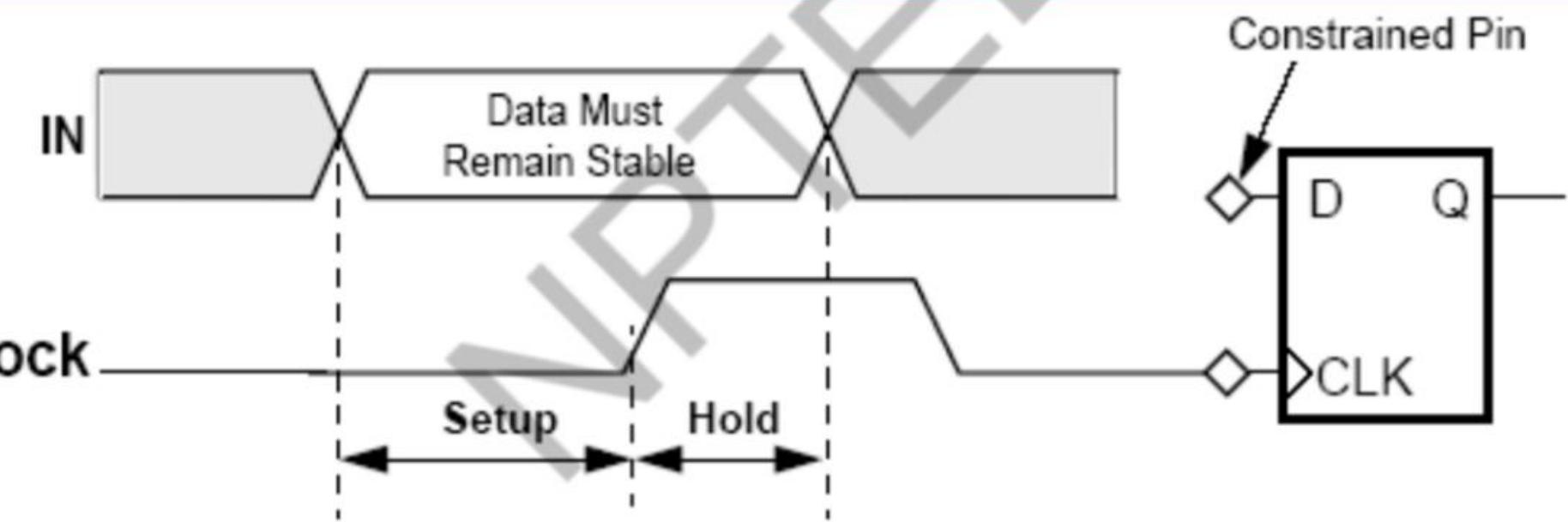




So in a similar way to setup time, you have another timing constraint called the Hold time denoted by T_{hold} . This is on the other side of the clock edge; this is the amount of time the input of the flip flop must be stable **after** the clock edge comes; that means, for a positive edge triggered the clock goes high or a negative edge triggered clock goes low.



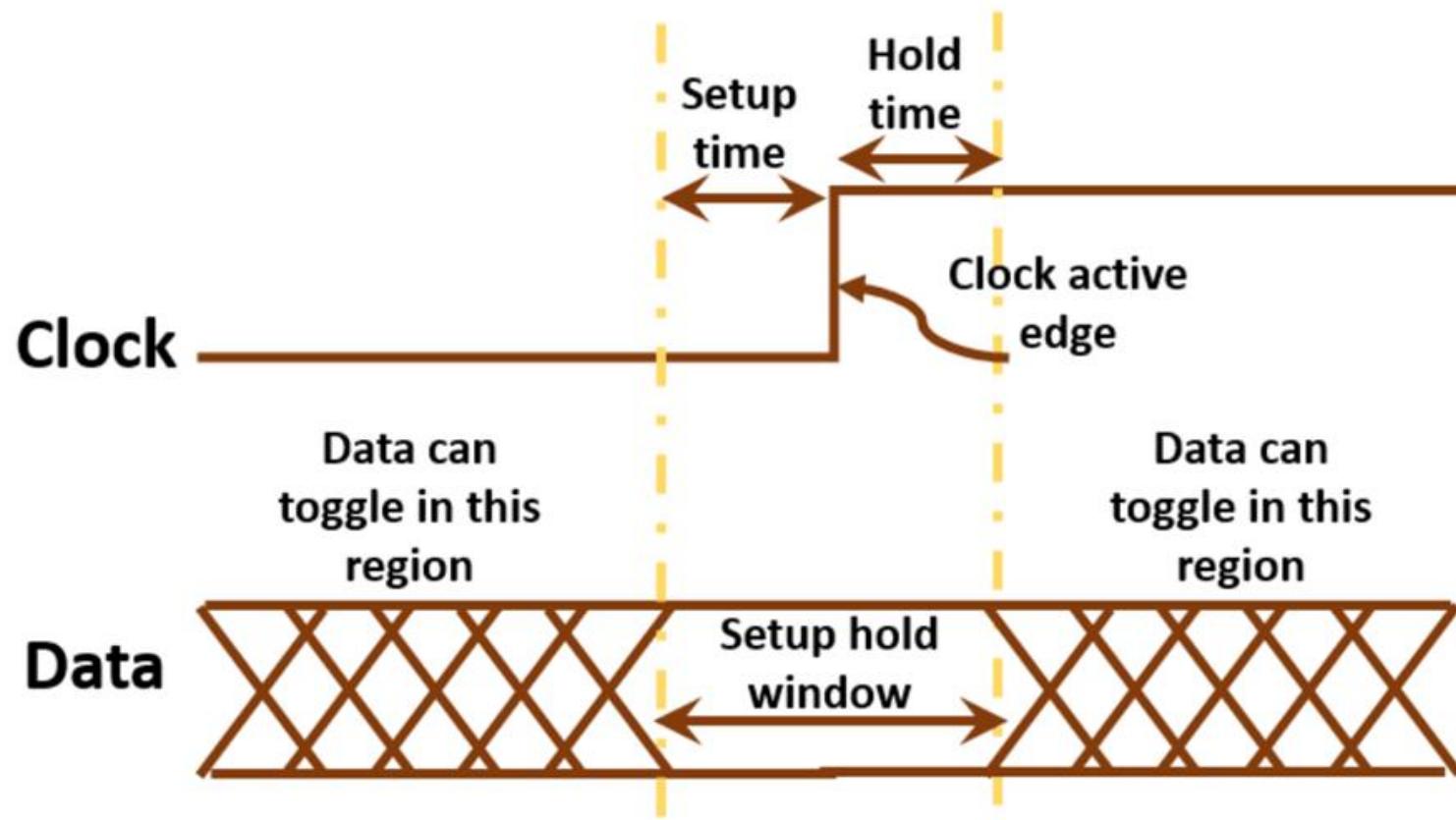
So, setup time specifies, with respect to clock edge how much before I must apply the inputs and hold time specifies, again with respect to the clock edge how much more I must maintain that input stable so that the flip flop works correctly. And of course, there is another delay to be considered it is the Propagation delay.





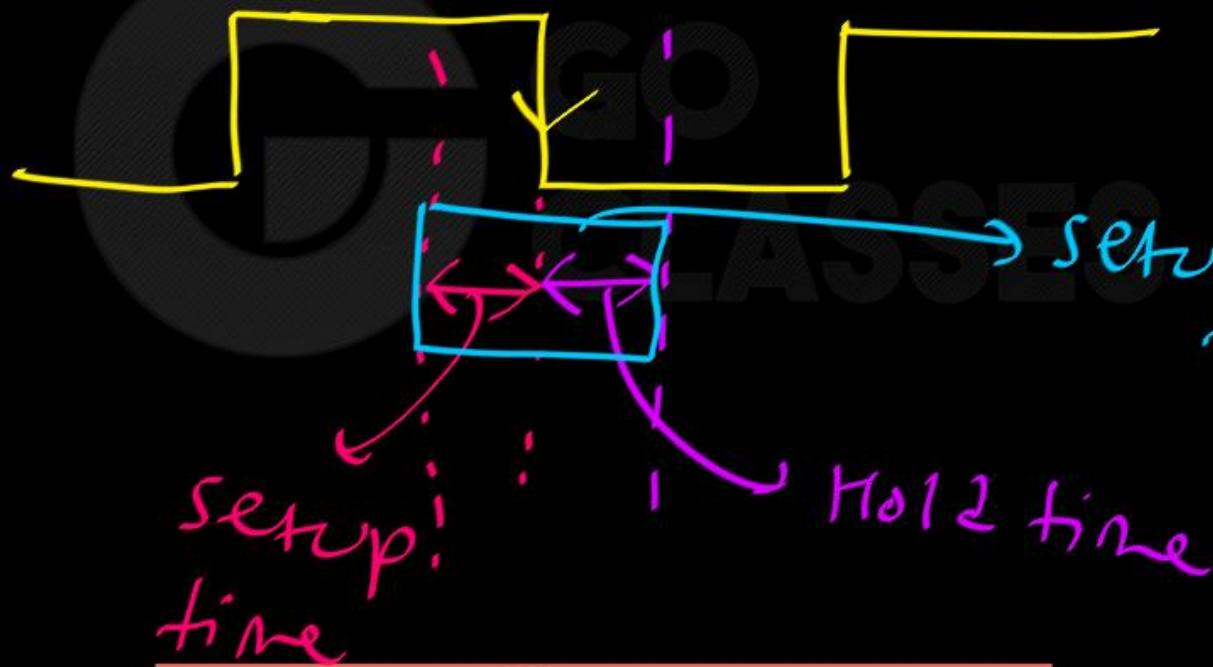
So, you see these are the constraints we talked about setup time, hold time, but the flip flop as a circuit it will be having its own delay. There are so many gates all the gates will be having some delay. So, what is the minimum time after the clock edge has come that the output will start to change that is, the propagation delay of flip flop.

If the flip-flop's setup time is 20 ns, it means that data has to be stable atleast 20ns before the capturing clock-edge. Similarly hold time is the amount of time, data has to remain stable after a clock edge has appeared. So together they define a "setup-hold-window", in which data has to remain stable.

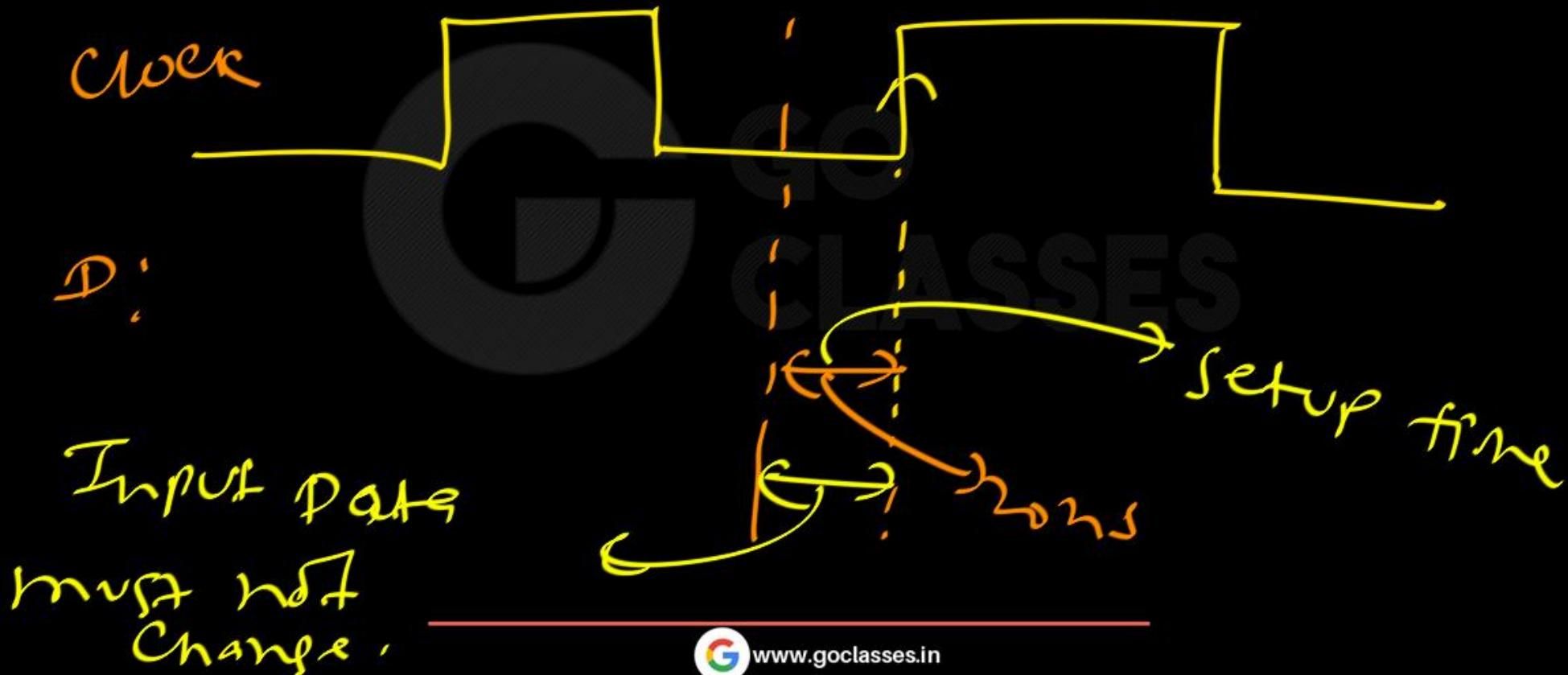


If the data changes/toggles within this window, the output is unpredictable or metastable.

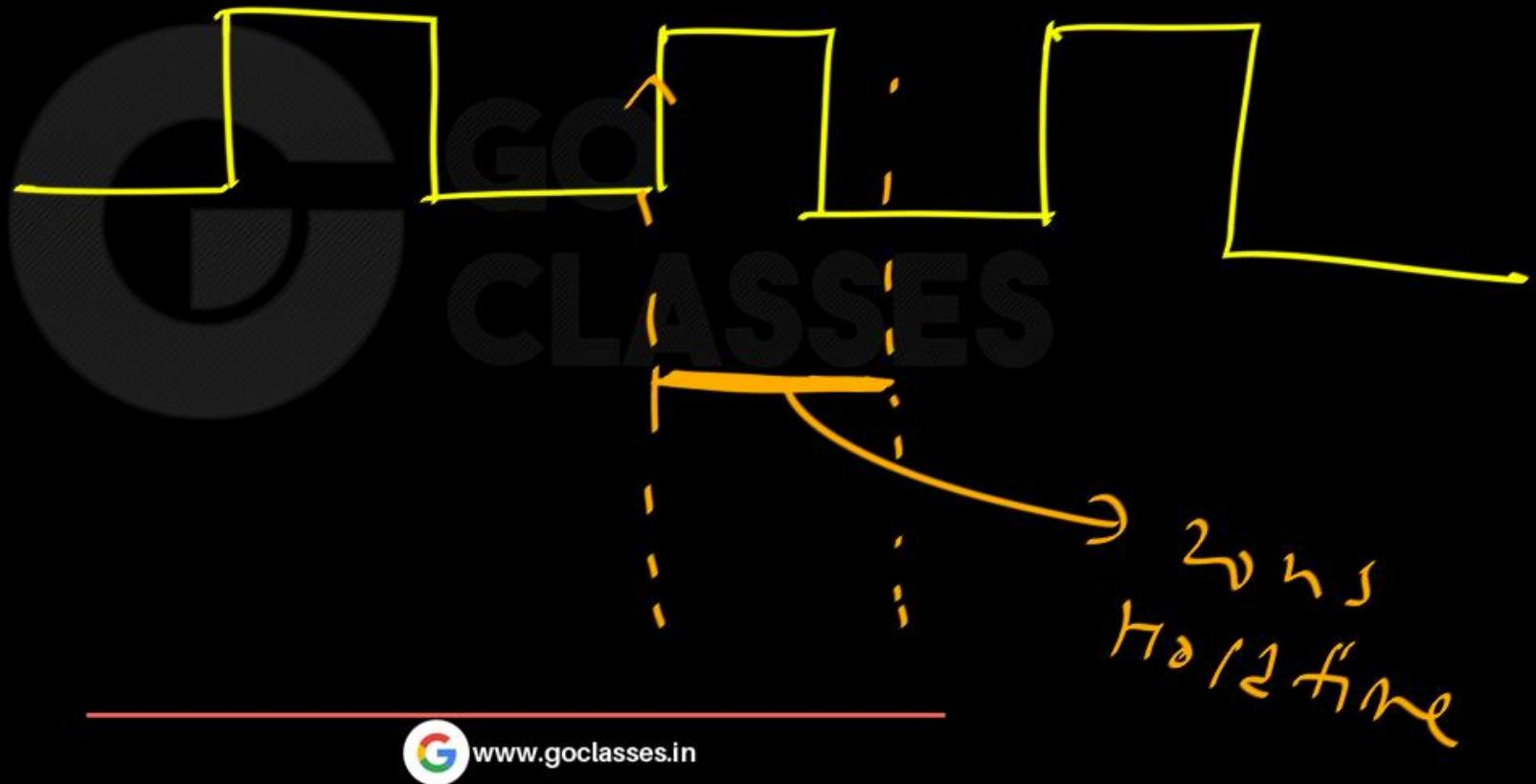
-Ve Edge Triggered:



Setup time = 20 ns ;



Hold time: 20 ns





Digital Logic

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Q 1. Consider a flip flop with a setup time of 3 ns and a hold time of 1 ns. If the clock input rises at time t, is it ok for the data input to change at time $t-2$? What about $t-4$? What about $t+1/2$? What about $t+2$? Explain why it is not acceptable for the data input to change at certain times.



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Q 1. Consider a flip flop with a setup time of 3 ns and a hold time of 1 ns. If the clock input rises at time t, is it ok for the data input to change at time $t-2$? What about $t-4$? What about $t+1/2$? What about $t+2$? Explain why it is not acceptable for the data input to change at certain times.

- If Data Changes at
- ① $t-2 \leq$ Setup violation
 - ② $t-4, t+2 \leq$ No problem
 - ③ $t+0.5 =$ Hold time violation

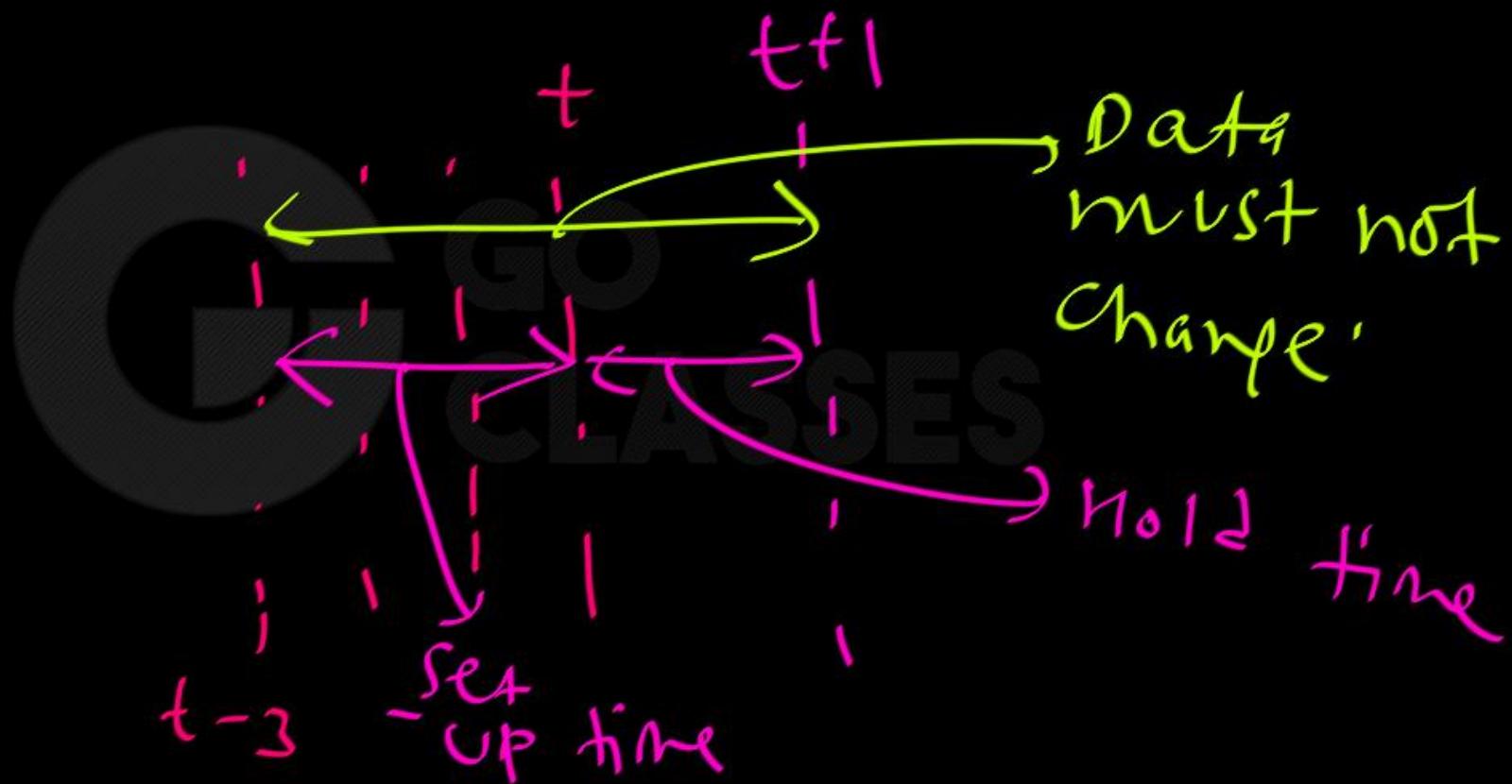
+ve Edge Triggered FF

Setup time: 3ns

Hold time: 1ns



at $t:$





Digital Logic

Q 2 . Consider a flip flop with a setup time of 5 ns and a hold time of 3 ns. The clock input rises at time 20 ns.

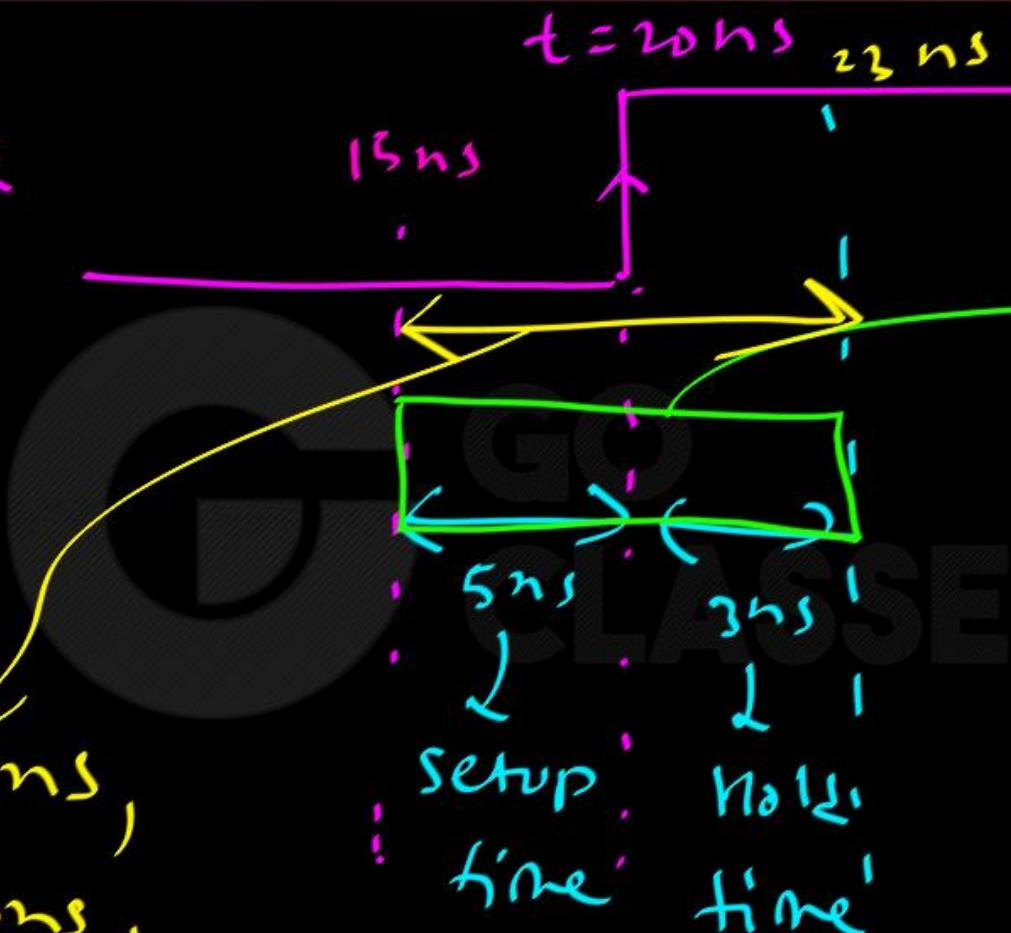
What is the latest time that the D input can change prior to the clock edge to ensure proper timing?

- A 15 ns B. 17 ns C. 19 ns D. 21 ns E. 23 ns

Clock

Input Data

After 15ns,
before 23ns,
Data must
be steady/consistent.



setup-Hold
window
Data
must
not change



Q 3. Consider a flip flop with a setup time of 5 ns and a hold time of 3 ns. The clock input rises at time 20 ns.

What is the earliest time that the D input can change after the clock edge to ensure proper timing?

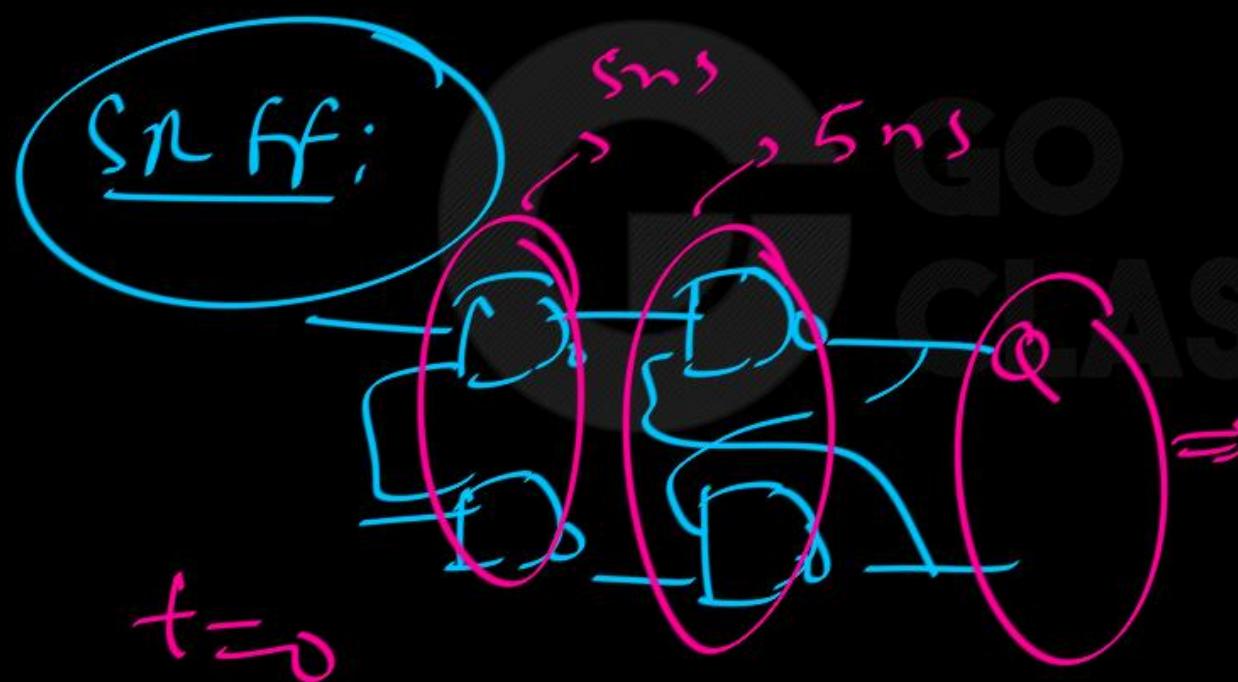
- A. 15 ns B. 17 ns C. 19 ns D. 21 ns E. 23 ns

at time $t \geq 23 \text{ ns}$; we can change D_{in}.

Propagation Delay(τ_D) of FF

V_s
Hold, setup time of FF.

PD of FF:

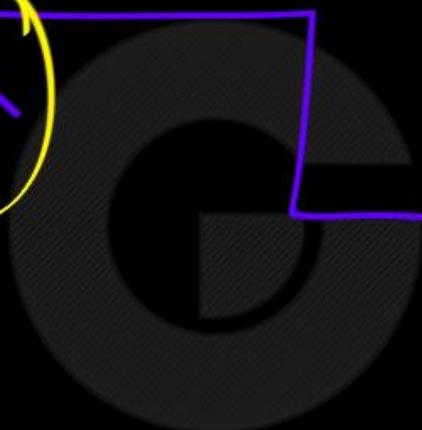


OUTPUT
Stable after
10ns = PD of
FF.



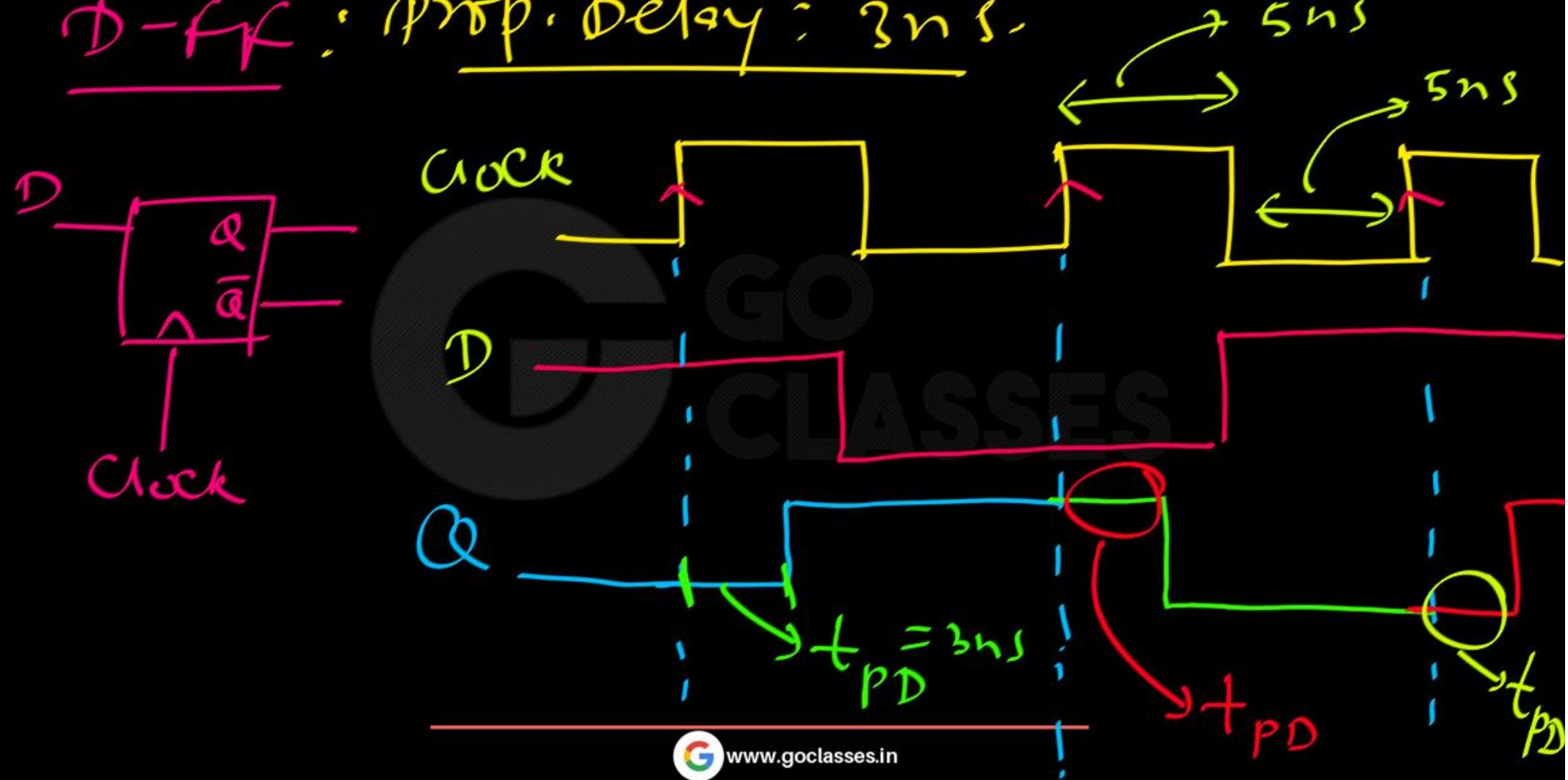
Propagation Delay of a FF:

Clock



PD of FF: When a triggering edge arrives, then after how much time, FF output will be stable/available/valid.

D-FF : Prop. Delay : 3ns



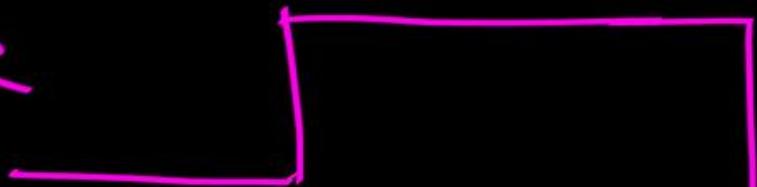
PD of ff Vs setup time of ff Vs

Hold of ff:

Hold time: 1ns } for input of
setup time: 5ns } flip flop.

t_{PD} of ff: 3ns } for output of ff.

clock



$$t_s \geq 5\text{ns}$$

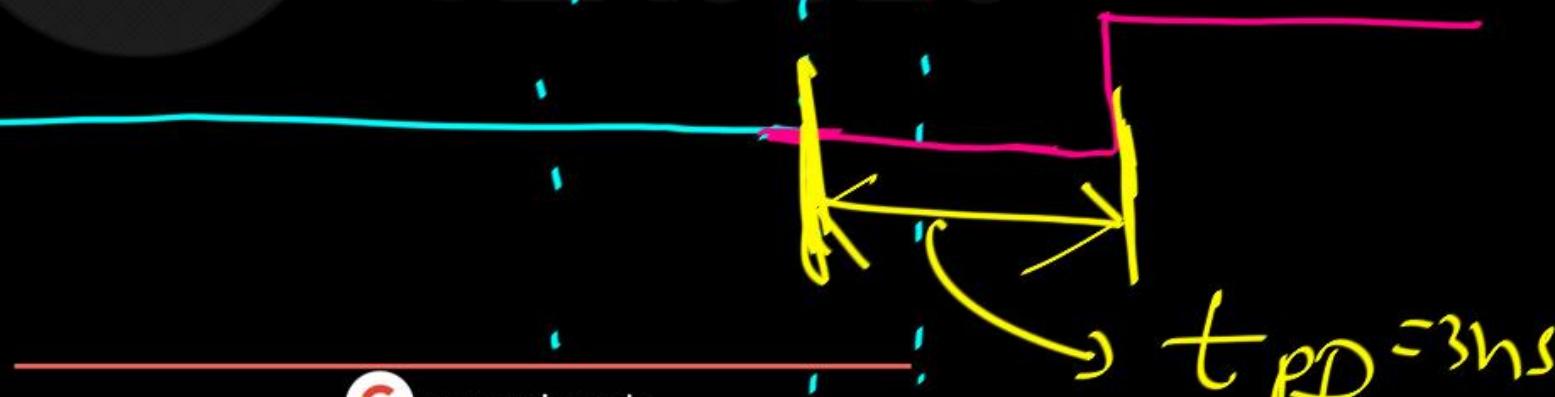
$$t_h = 1\text{ns}$$

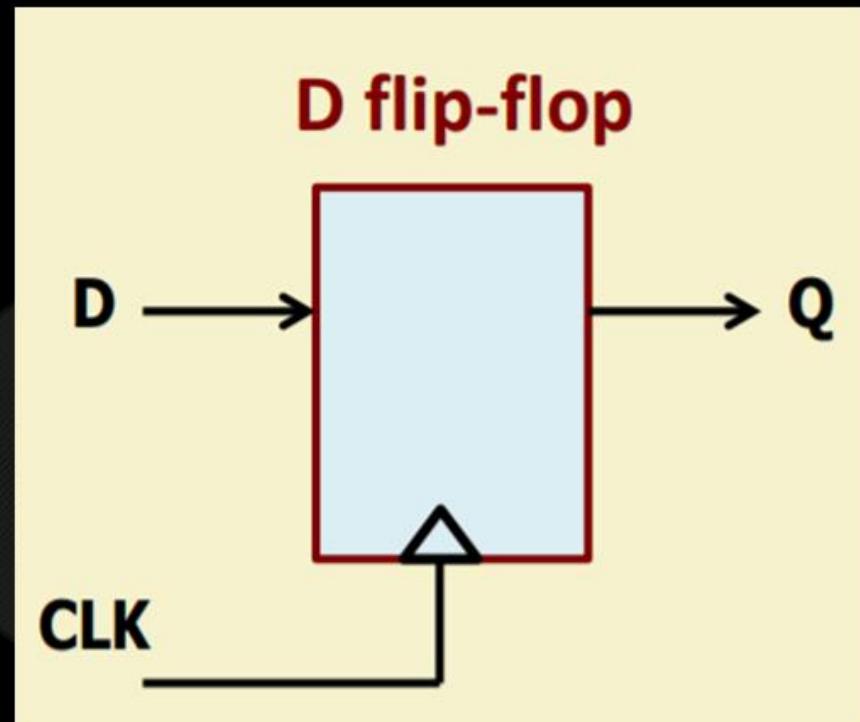


D



Q





PD of ff = t_{PD} = T
Ck \rightarrow Q

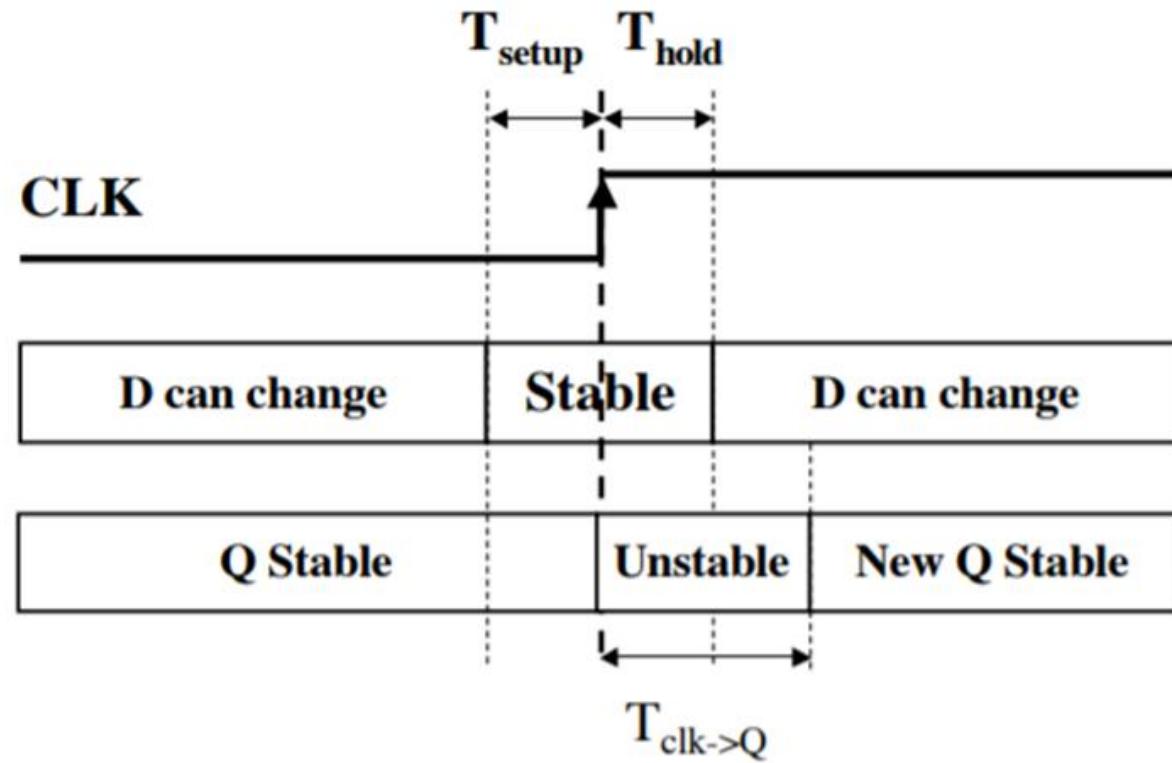
PD of ff;

from triggering edge arrival to
output (Q) becoming stable/available.

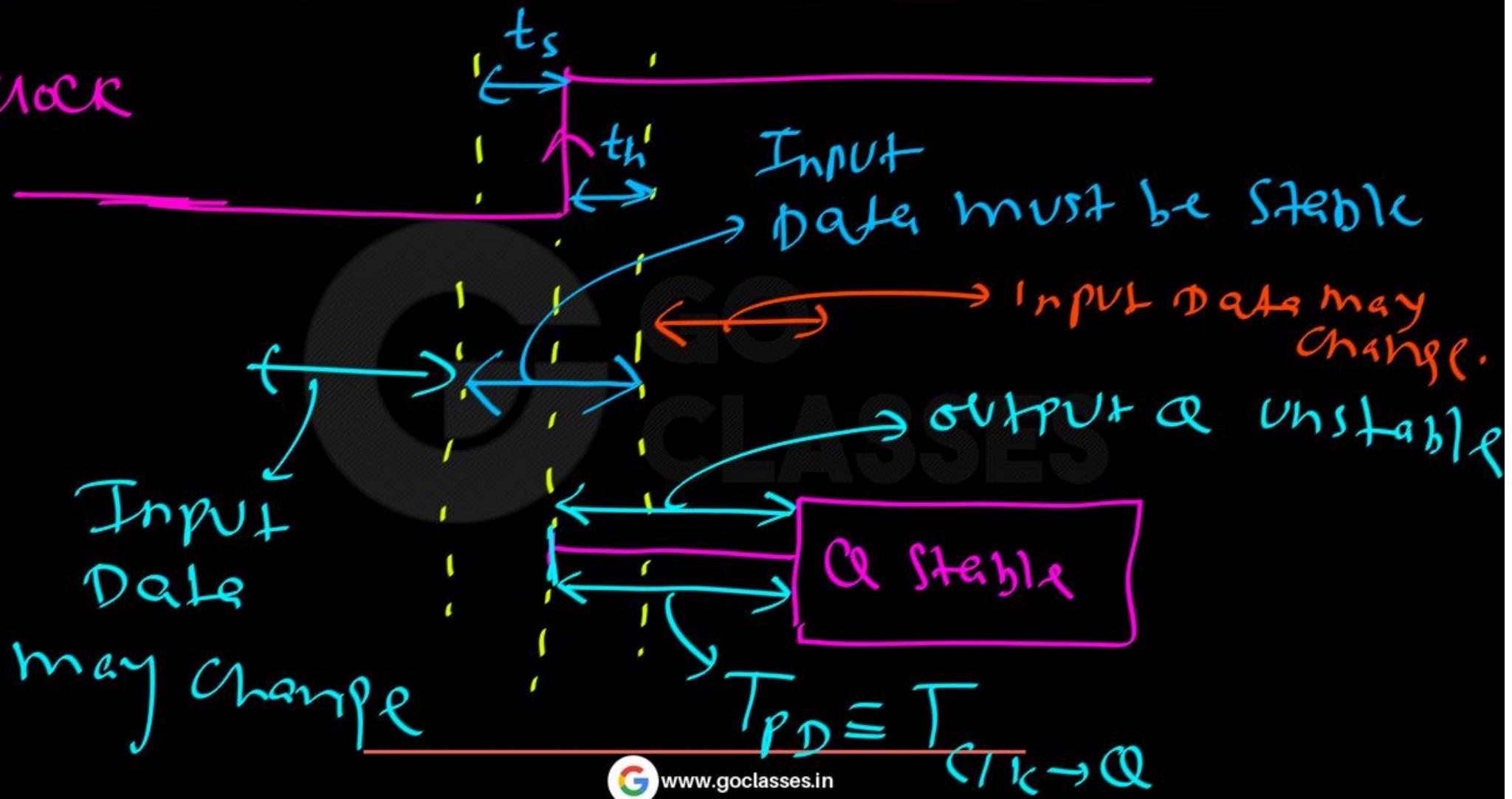
$T_{clk \rightarrow Q}$

- $T_{clk \rightarrow Q}$: the amount of time you have to wait after the CLK before the output (Q) is valid
- If you try to use the output before this you will get inconsistent results depending on if Q changes

$T_{clk \rightarrow Q}$ Diagram



CLOCK





Timing Issues :

- For correct operation of a synchronous sequential circuit, several timing issues need to be considered.

Some of these issues relate to the properties of flip-flops.

For eg, Hold time, Setup time.

All these taken together determines the maximum speed with which the circuit can operate.

- Typically specified in terms of the clock frequency.



Digital Logic

In general, the inputs must be applied a specified time before the active clock edge (the setup time), and they must be held constant a specified time after the active edge (the hold time).

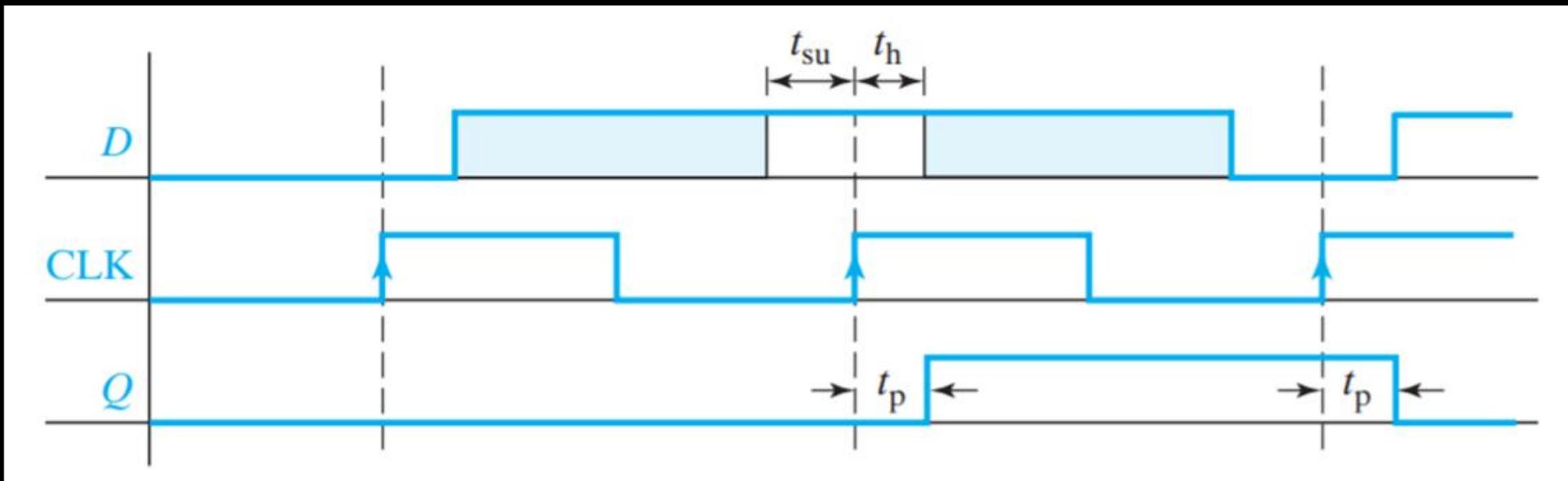




The timing of the response of a flip-flop to input data and to the clock must be taken into consideration when one is using edge-triggered flip-flops. There is a minimum time called the setup time during which the D input must be maintained at a constant value prior to the occurrence of the clock transition. Similarly, there is a minimum time called the hold time during which the D input must not change after the application of the positive transition of the clock. The propagation delay time of the flip-flop is defined as the interval between the trigger edge and the stabilization of the output to a new state.

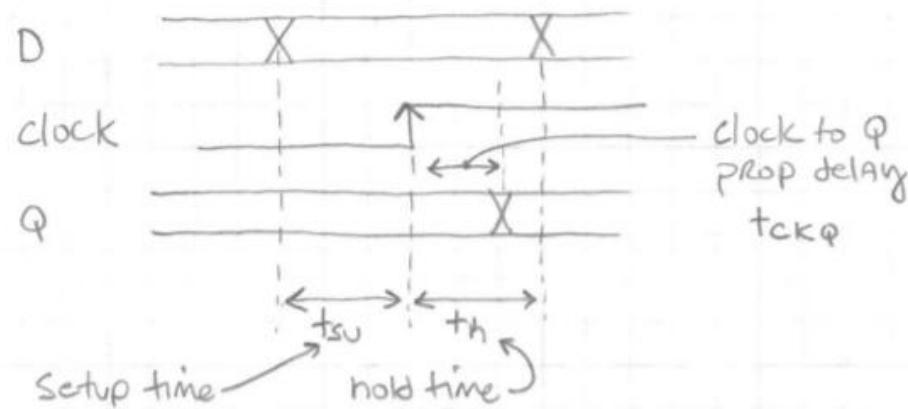


Because a flip-flop changes state only on the active edge of the clock, the propagation delay of a flip-flop is the time between the active edge of the clock and the resulting change in the output. However, there are also timing issues associated with the D input. To function properly, the D input to an edge-triggered flip-flop must be held at a constant value for a period of time before and after the active edge of the clock. If D changes at the same time as the active edge, the behavior is unpredictable. The amount of time that D must be stable before the active edge is called the setup time (t_{su}), and the amount of time that D must hold the same value after the active edge is the hold time (t_h). The times at which D is allowed to change during the clock cycle are shaded in the following timing diagram :



Flip Flop Setup and Hold Time

- ▶ Considering D-type edge-triggered, Flip Flops (FF's)
- ▶ Just before and just after the clock edge, there is a critical time region where the D input must not change.



- ▶ The region just before the clock edge is called *setup time* (t_{SU})
- ▶ The region just after the clock edge is called *hold time* (t_h)

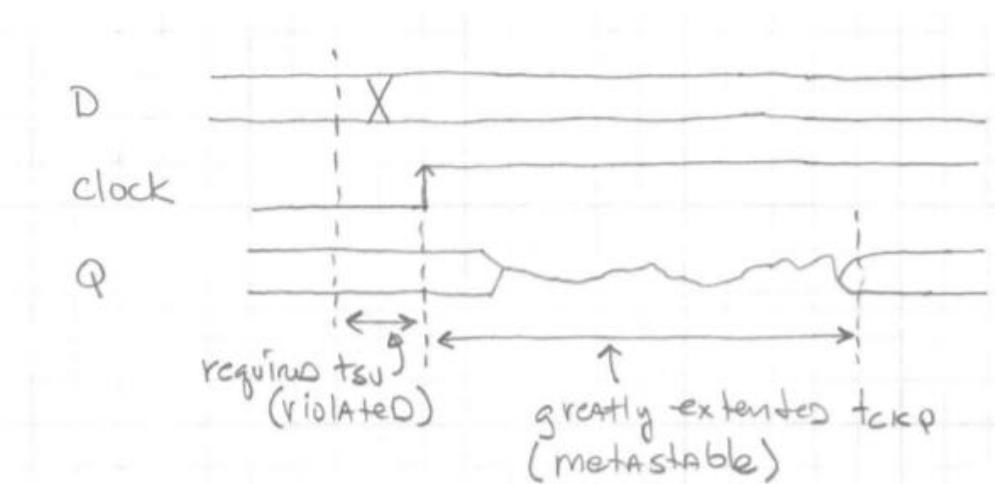


- ▶ Every FF has minimum required values for t_{su} and t_h .





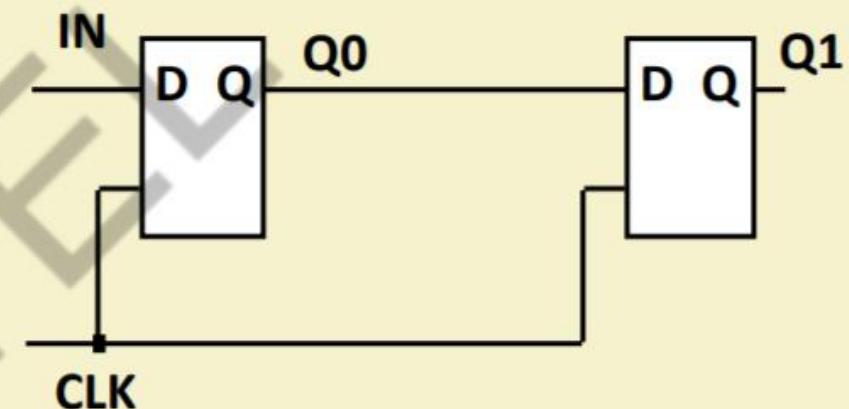
- ▶ If the D input changes within the t_{su} and t_h window, Q may:
 - ▶ Follow D correctly
 - ▶ Follow D incorrectly
 - ▶ Assume a metastable state for an indeterminate time followed by a transition to logic 1 or logic 0.

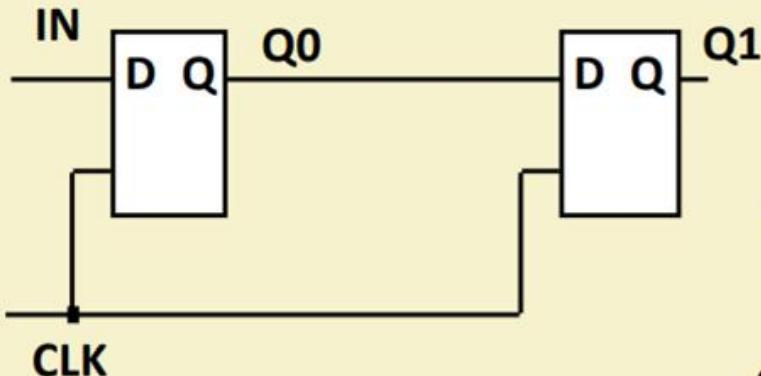


- ▶ For correct operation, D inputs must be stable for a t_{su} prior to clock and stay stable for a t_h afterwards.

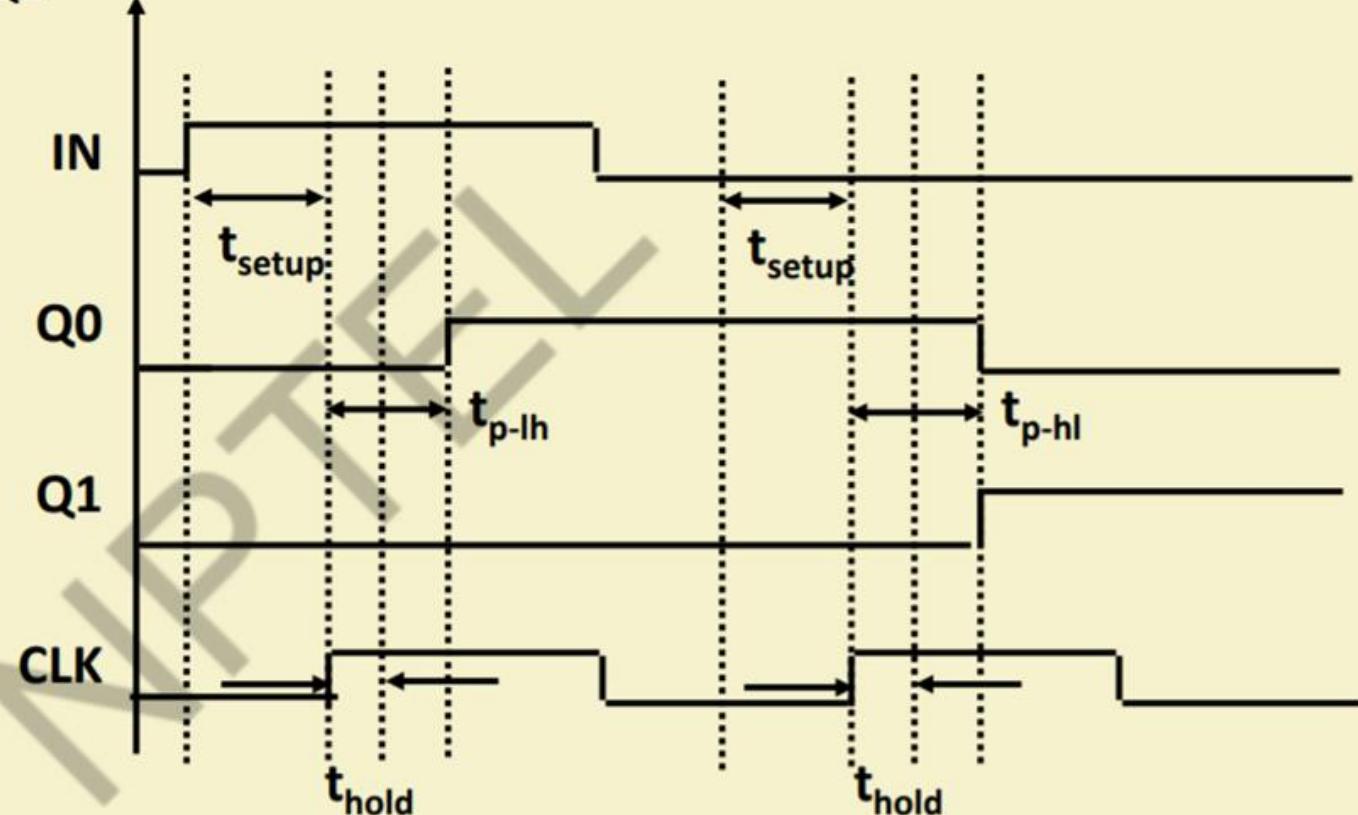
Cascading Flip-flops

- Suppose that the flip-flop propagation delay exceeds the hold time.
- Second stage can commit its input before Q0 changes.





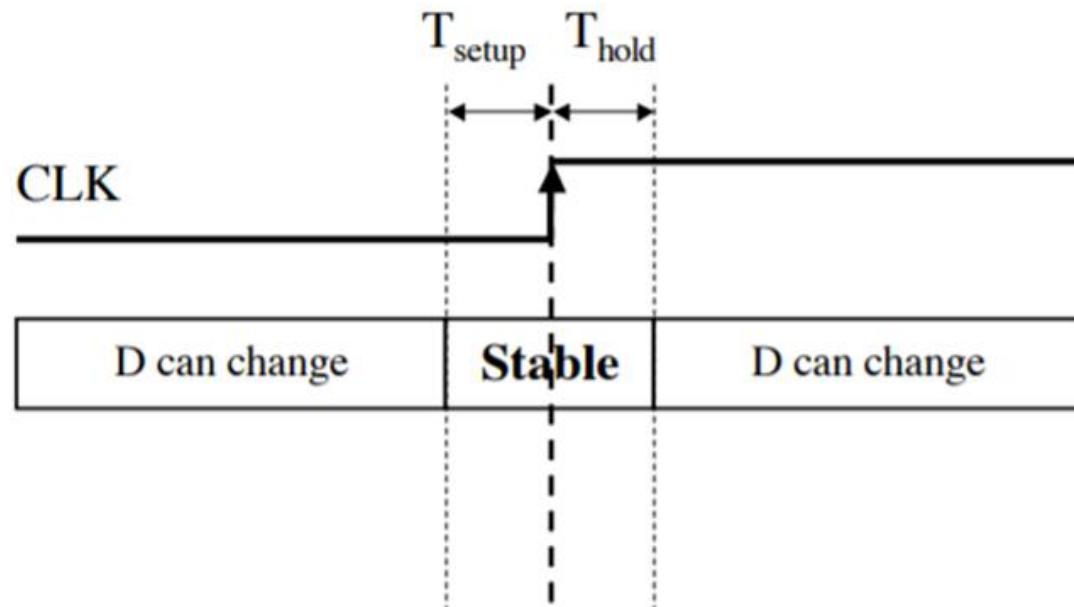
The correct scenario



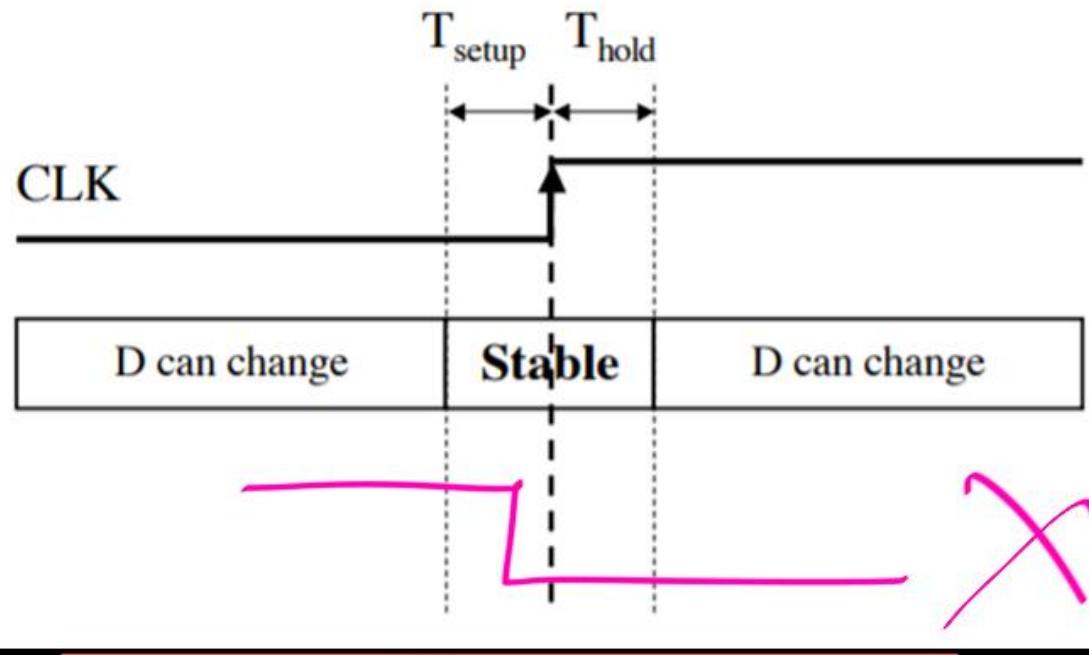
Setup and Hold Times

- Setup Time: the amount of time the synchronous input (D) must be stable **before** the active edge of the clock
- Hold Time: the amount of time the synchronous input (D) must be stable **after** the active edge of the clock
- If either is violated correct operation of the FF is not guaranteed
- Metastability can result.

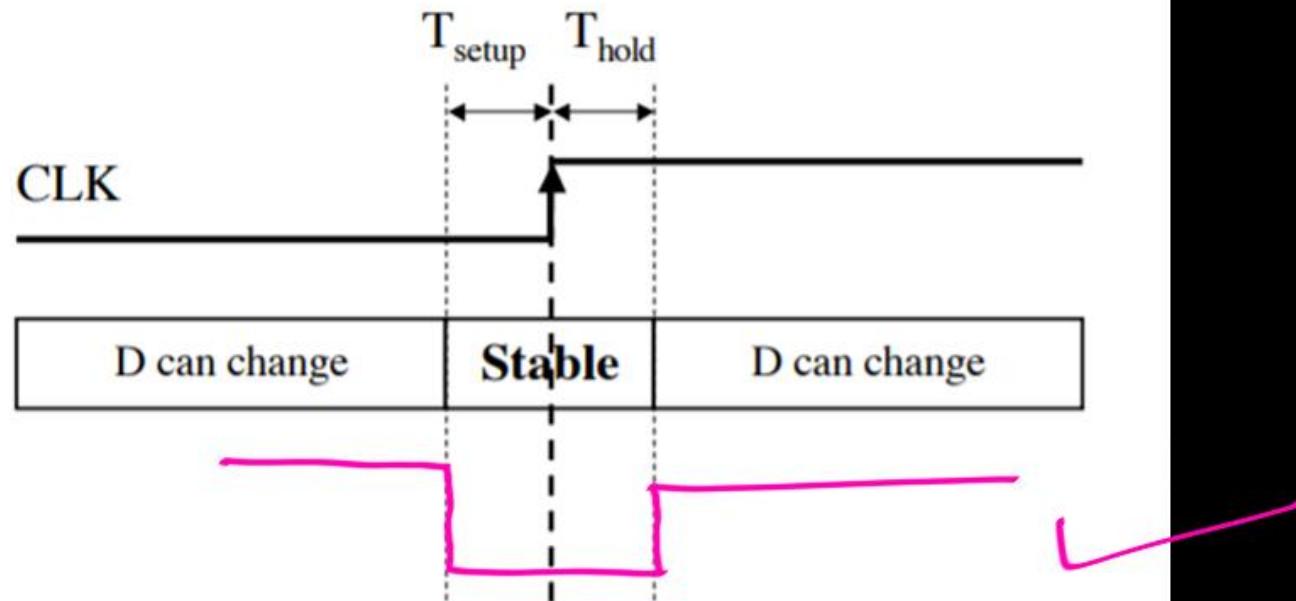
Setup and Hold Diagram



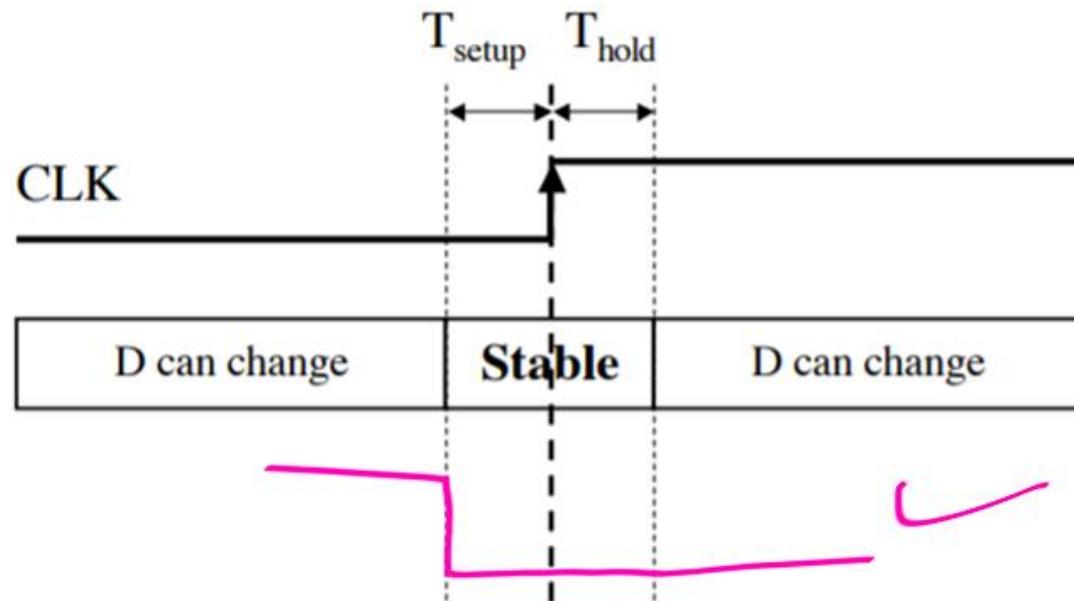
Setup and Hold Diagram



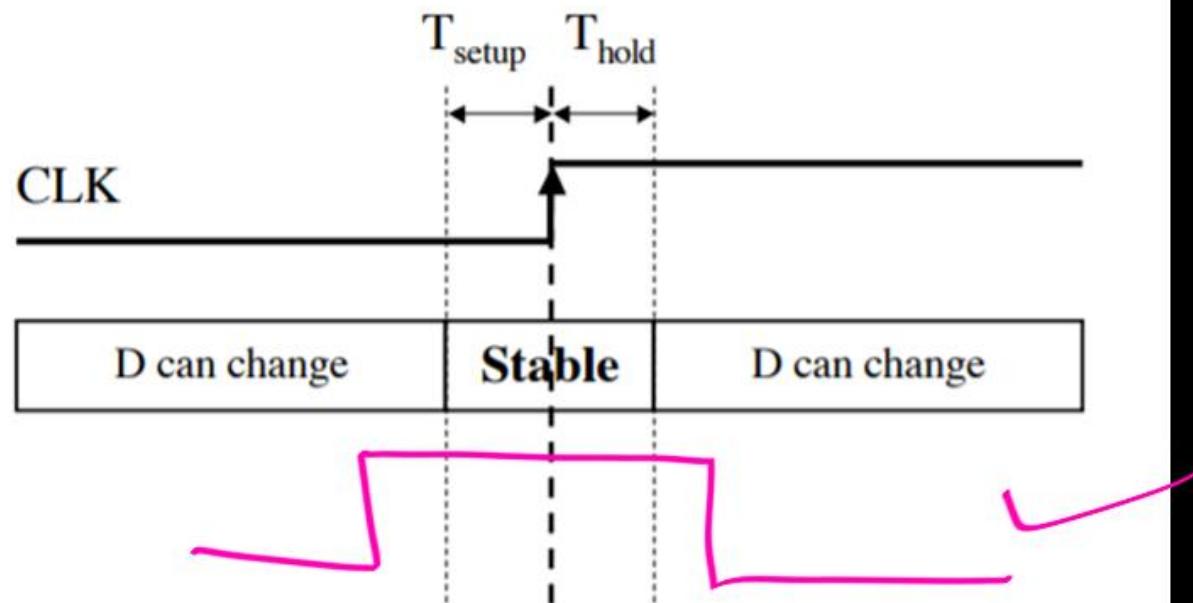
Setup and Hold Diagram



Setup and Hold Diagram



Setup and Hold Diagram



FF Timing Constraints

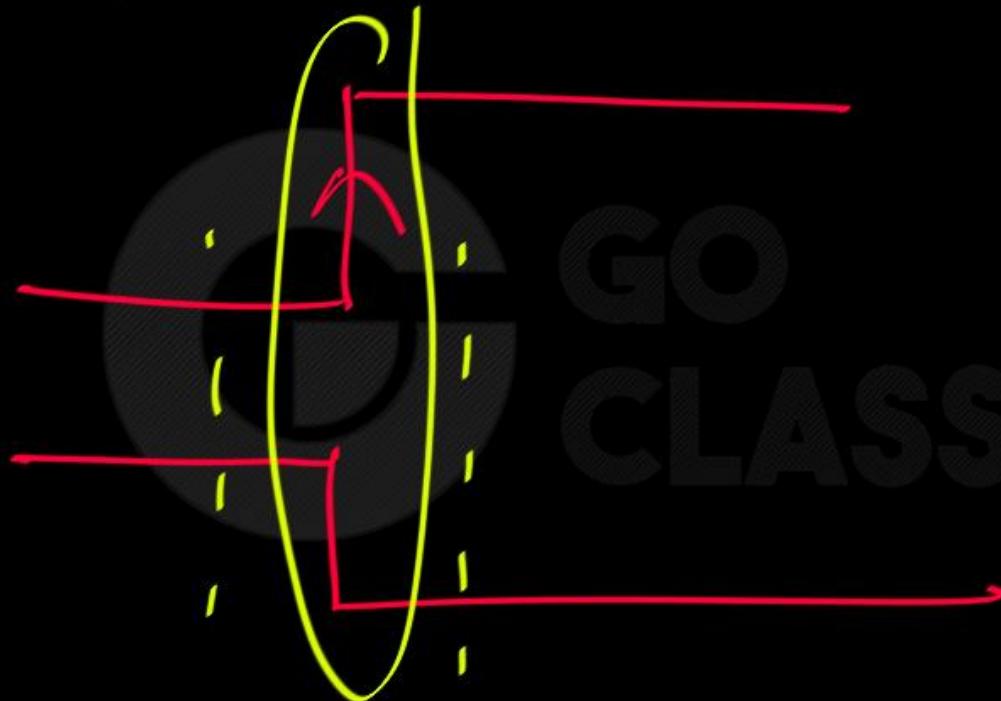
- ① ■ What happens if D and CLK change at the same time? \Rightarrow Unpredictable behaviour Due to
 - How close can these get? Hold, Setup Time Violation.
 - Determined by the Setup and Hold times
- ② ■ What happens if we try to use Q right after the clock? \Rightarrow Unpredictable behaviour Due to
 - How long do we have to wait? Propagation delay of FF.
 - Determined by $T_{clk \rightarrow Q}$

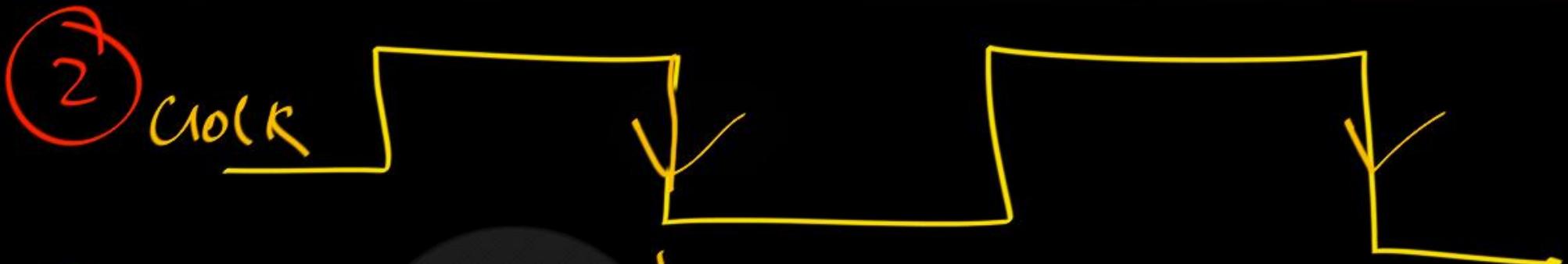


① setup time, Hold time Violation.

clock

D





D



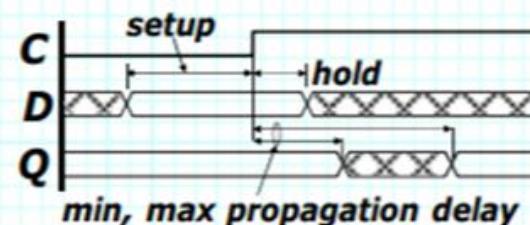
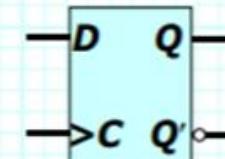
Q

$$T_{\text{clk} \rightarrow Q} = T_{PD}$$

During this period,
output Q is unstable

Edge-Triggered D Flip Flop

- **D** flip flop stores value at **D** input when clock rises
- Most widely used storage element for sequential circuits
- **Propagation time** is time from rising clock to output change
- If input changes when clock rises, new value is uncertain
 - » output may oscillate or may remain at intermediate voltage (**metastability**)
- Timing rules to avoid metastability
 - » **D** input must be stable for **setup time** before rising clock edge
 - » must remain stable for **hold time** following rising clock edge



maximum clock frequency f ?

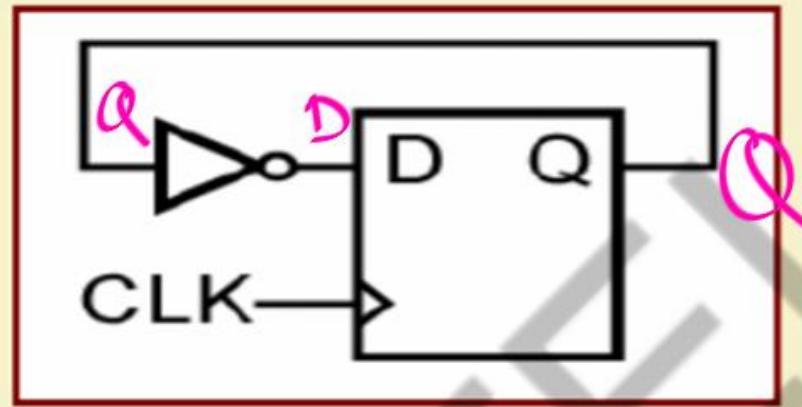
Minimum clock period T ?

$$t_{pINV} = 2 \text{ ns}$$

$$t_{pFF} = 5 \text{ ns}$$

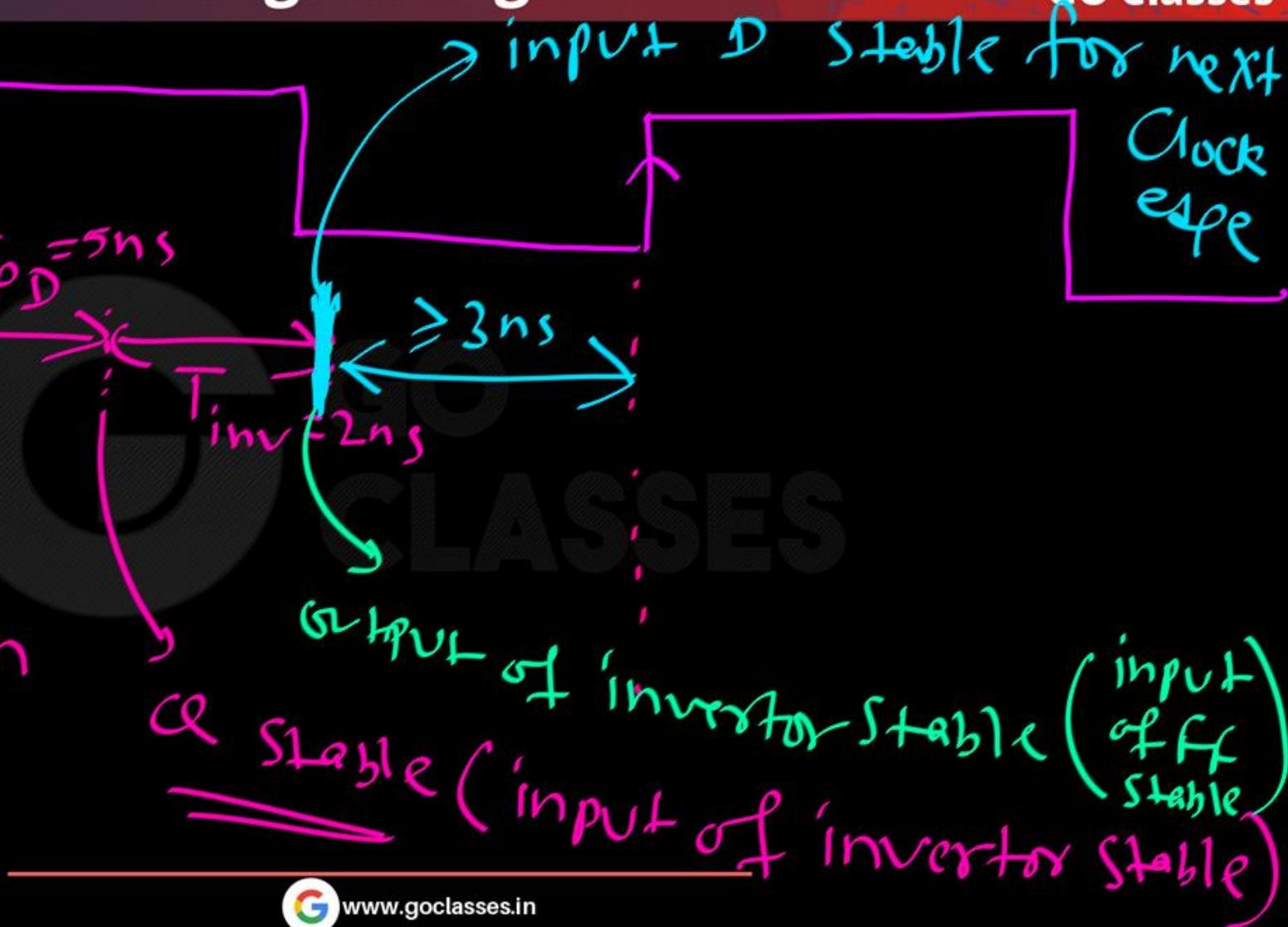
$$t_{\text{setup}} = 3 \text{ ns}$$

$$t_{\text{hold}} = 1 \text{ ns}$$



Data(input) D is available/stable at least 3 ns before the rising edge.

Clock
Stable state
D
Data
Stable state
t_h



$$T_p \geq T_{PDFF} + T_{PDI_{nv}} + T_s$$

Hold time does not affect time period.

$$T_P \geq 2 + 5 + 3 \text{ ns}$$

$$T_P \geq 10 \text{ ns}$$

$$\begin{aligned} \frac{1}{10 \text{ ns}} &= \frac{1}{f_0} \text{ GHz} \\ &= 10^8 \text{ Hz} = 10 \text{ MHz} \end{aligned}$$

minimum Period of Clock : 10 ns

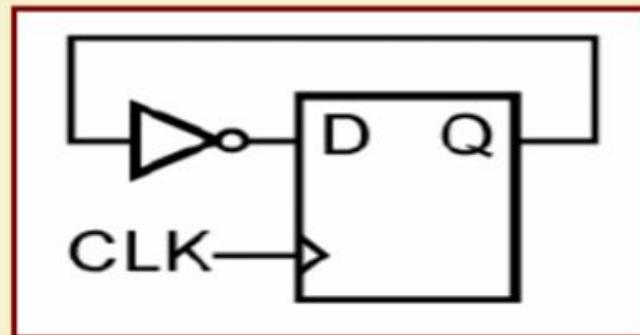
maximum frequency of Clock : $\frac{1}{10 \text{ ns}} = 100 \text{ MHz}$

$$T_p \geq T_{PDFF} + T_{PD\text{com}} + T_s$$

Note: Hol 1 time Does not affect
time period because T_{PDFF} , T_h
Overlaps.

Note:

$$\text{Hold time} \leq t_{\text{PDF}}$$



$$t_{pINV} = 2 \text{ ns}$$

$$t_{pFF} = 5 \text{ ns}$$

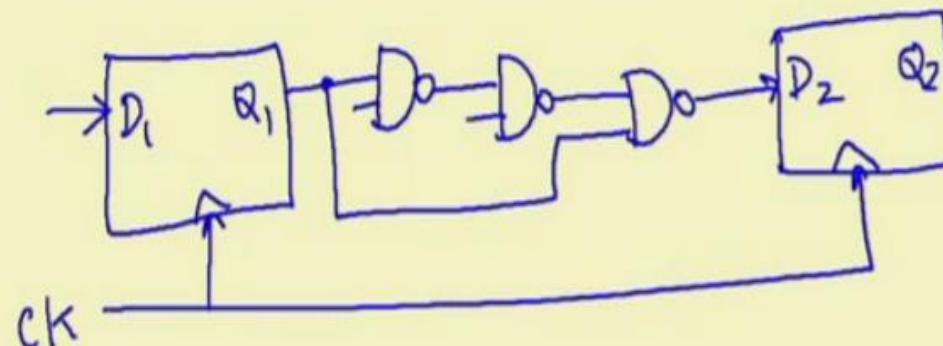
$$t_{setup} = 3 \text{ ns}$$

$$T_{min} = t_{pFF} + t_{pINV} + t_{setup} = 10 \text{ ns}$$

$$f_{max} = 1 / T_{min} = 100 \text{ MHz}$$

t_{hold} does not affect the calculation here

Another Example

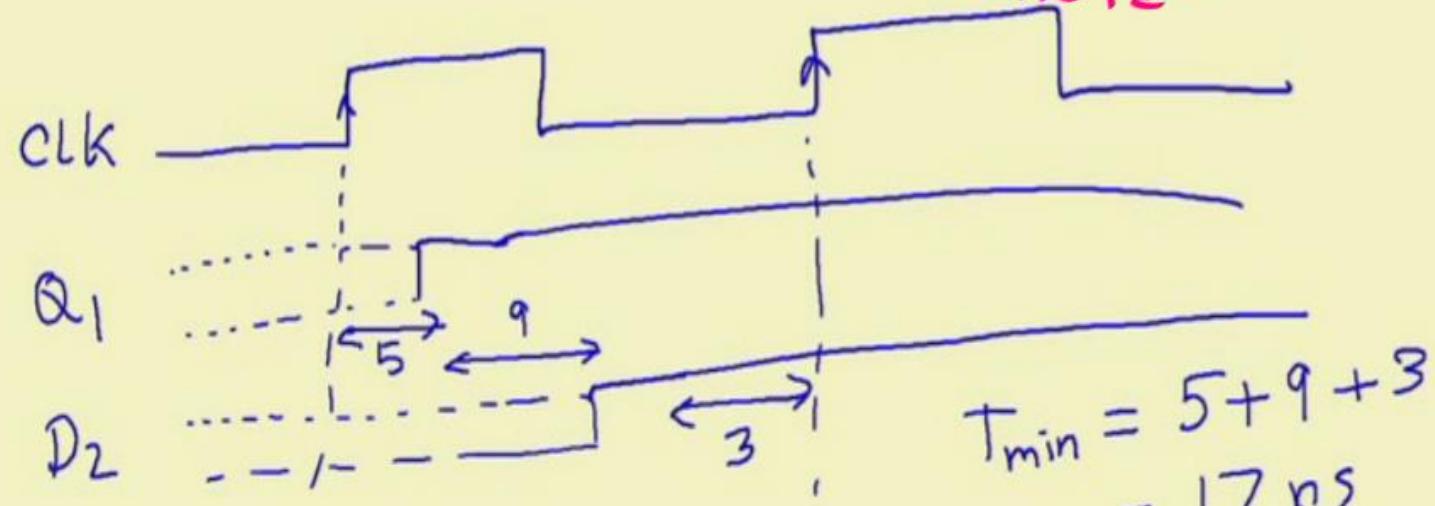


$$t_{PNAND} = 3\text{ns}$$

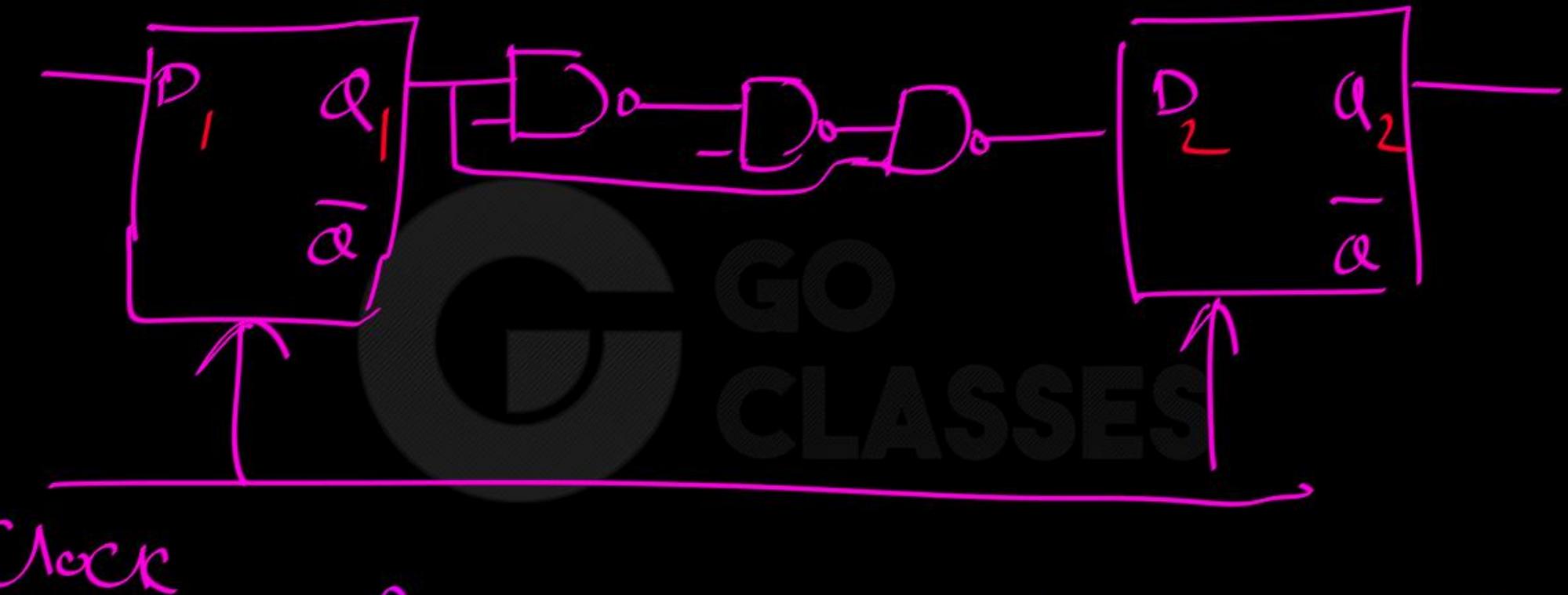
$$t_{FF} = 5\text{ns}$$

$$t_{\text{setup}} = 3\text{ns}$$

$$t_{\text{hold}} = 2\text{ns}$$

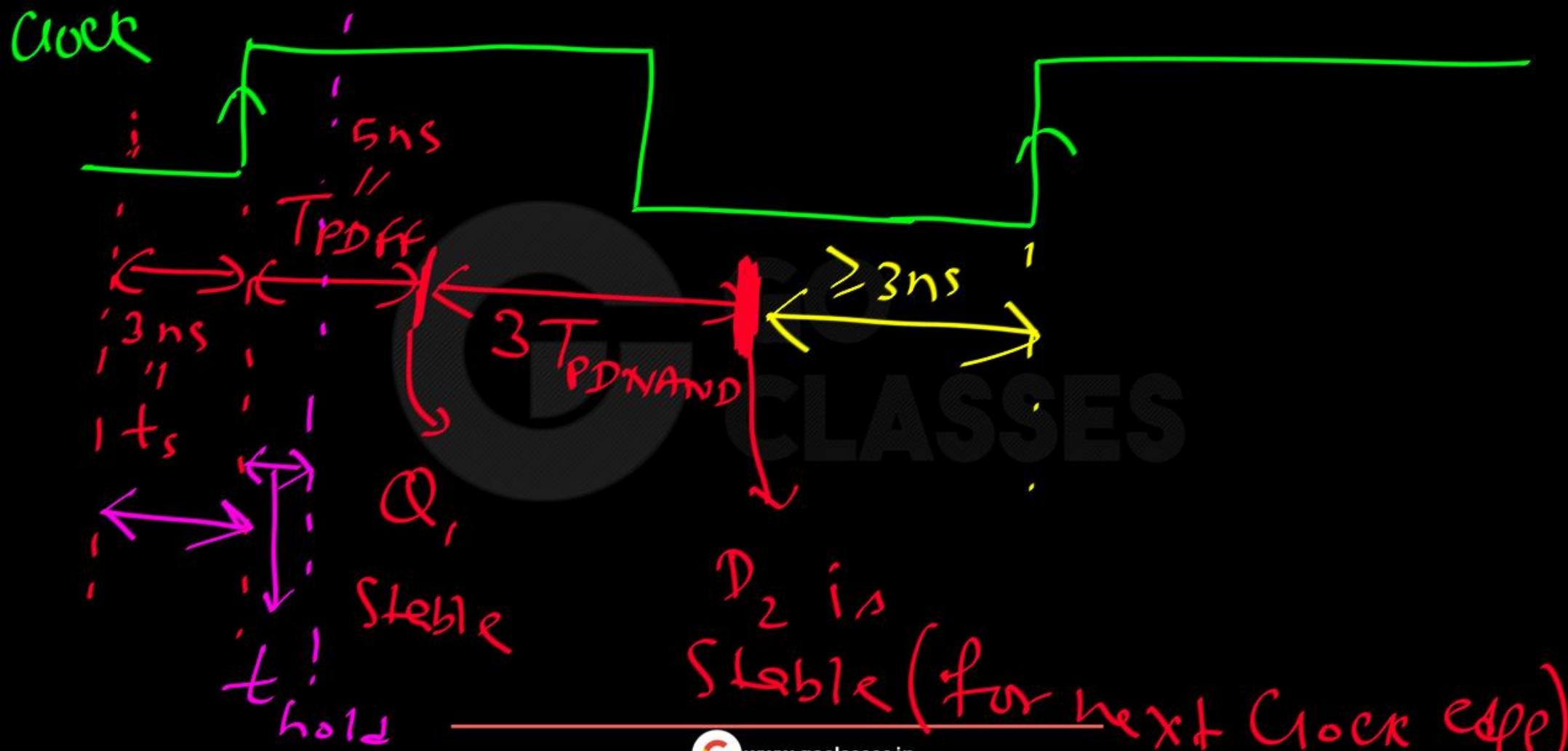


$$\begin{aligned} T_{\min} &= 5 + 9 + 3 \\ &= 17 \text{ ns} \end{aligned}$$



Clock

find the max. frequency of
this circuit?



$$T_P \geq 5 + 3(3) + 3$$

t_{PDFF}

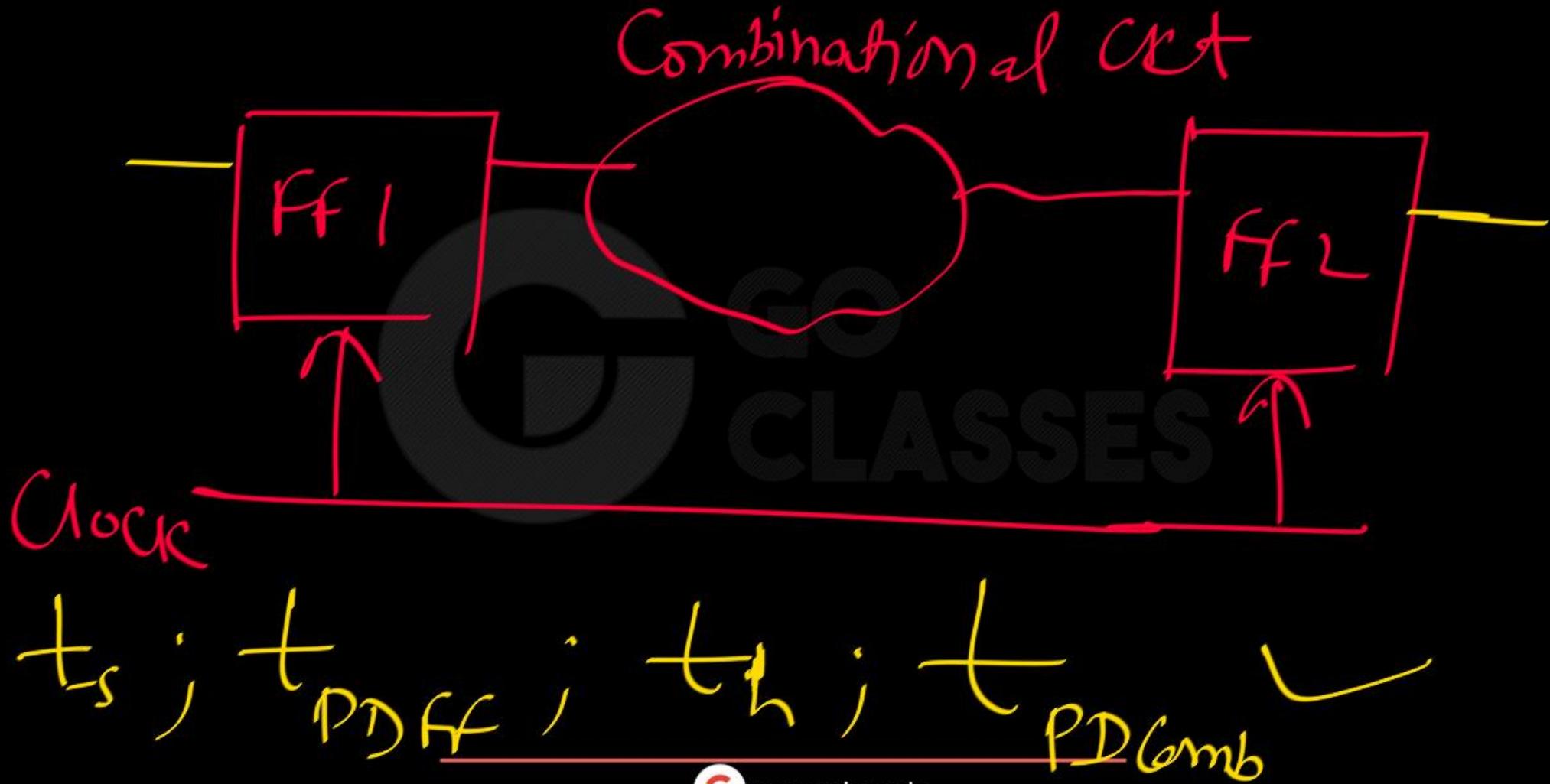
t_s

$$T_P \geq 5 + 9 + 3 ; T_P \geq 17 \text{ ns}$$

$$T_p \geq 17 \text{ ns} ; \min T_p = 17 \text{ ns}$$

max frequency

$$f_{\max} = \frac{1}{\min T_p}$$
$$= \frac{1}{17 \text{ ns}} = \frac{1}{17} \text{ GHz}$$

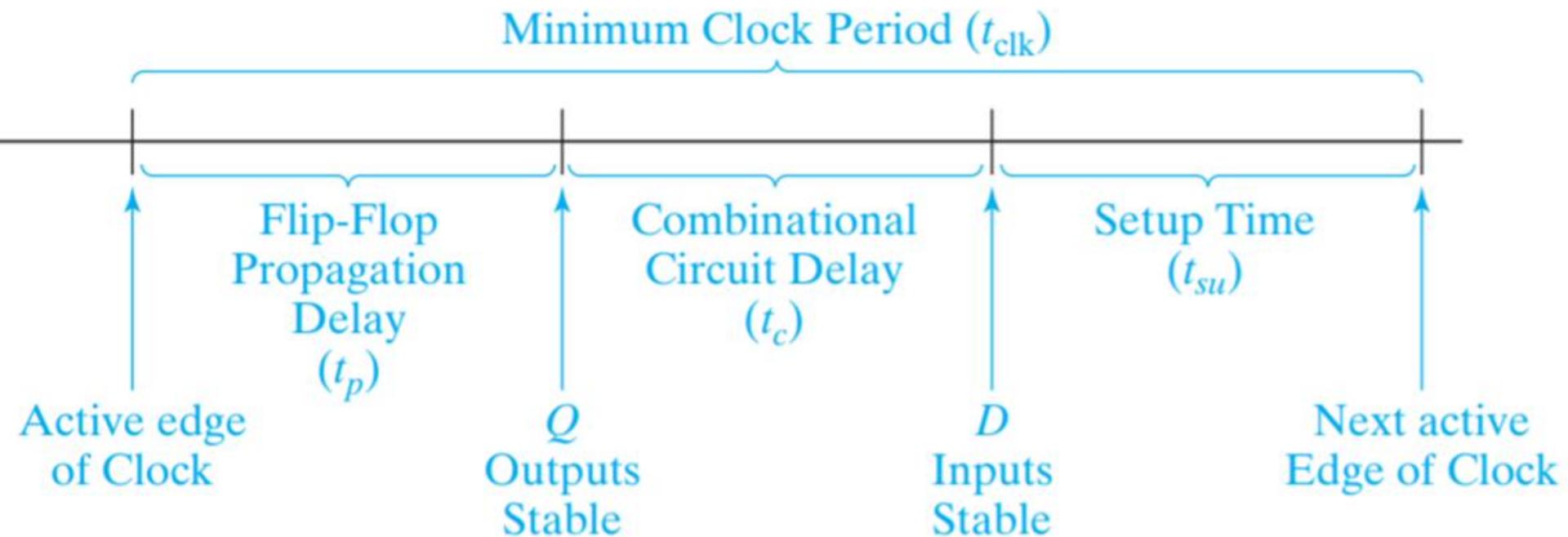


Clock Period:

$$t_p > T_{PDFF} + T_{PD\text{ comb}} + T_s$$

Note: T_{hol2} Does not affect time period of clock.

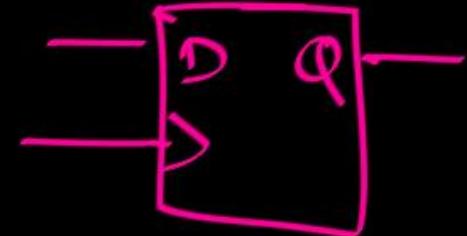
Setup time of FF



- ▶ Synchronous circuit minimum cycle time is effected by setup time.
- ▶ Between clock edges, the path between two FFs is composed of:
 - ▶ clock to Q delay of FF0 (t_{ckq})
 - ▶ propagation delay through combo logic (t_{pd})
 - ▶ the required setup time (t_{su}) of FF1
- ▶ t_{ckq} and t_{pd} are both delays. t_{su} is a constraint of FF operation.



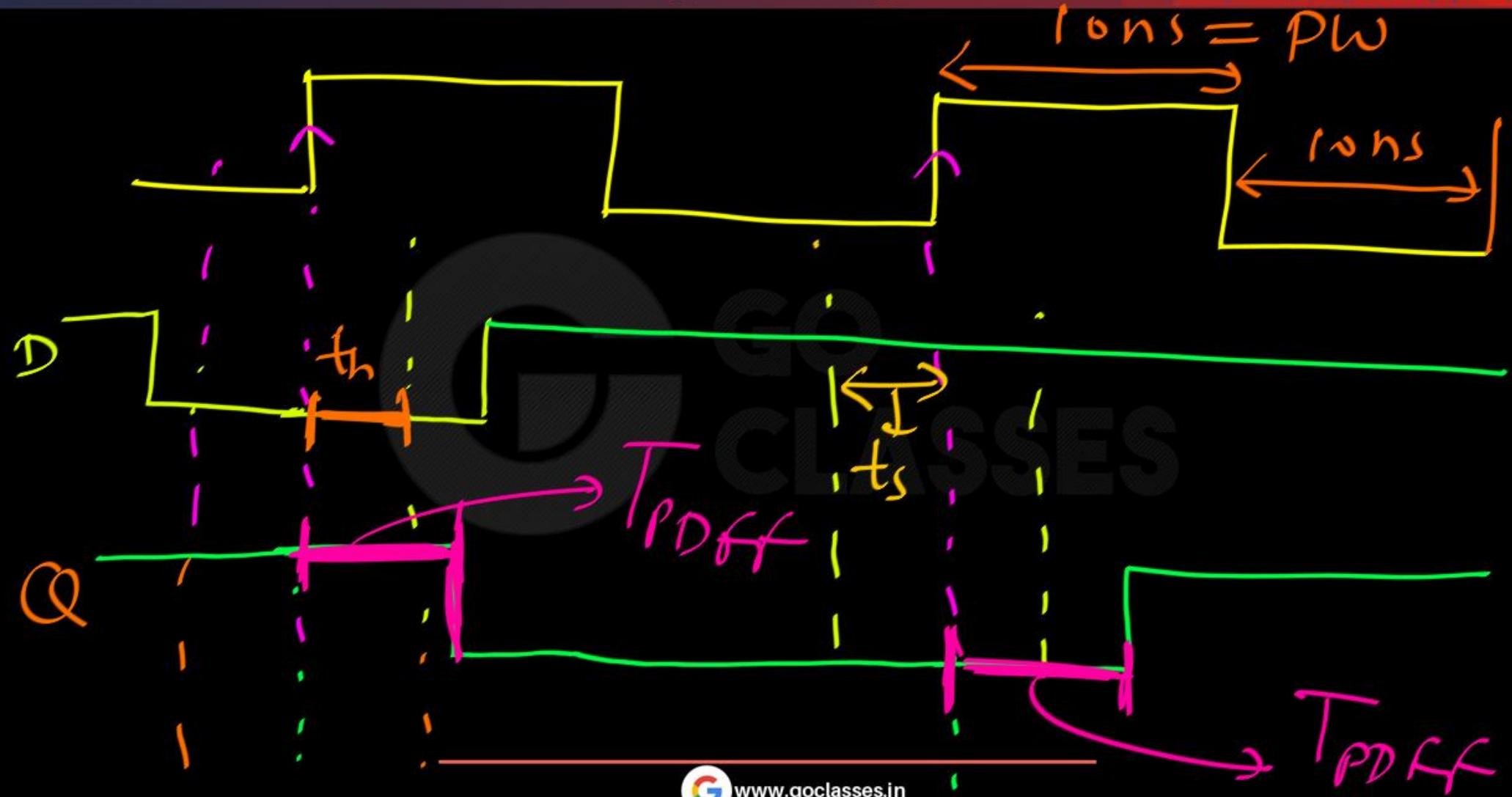
Setup time slack:



Ex: DFF ; the Edge triggered.

$$t_s = 2 \text{ ns} ; t_h = 2 \text{ ns} ; t_{PDFF} = 5 \text{ ns}$$

$$t_p = 20 \text{ ns} ; \text{ ON period} = \text{Pulse width} \\ \text{Period of Clock} = 10 \text{ ns}$$



$$T_p \geq T_{PDff} + T_{PD(\text{Com})} + T_s$$

$$T_p = \text{Q_one}$$

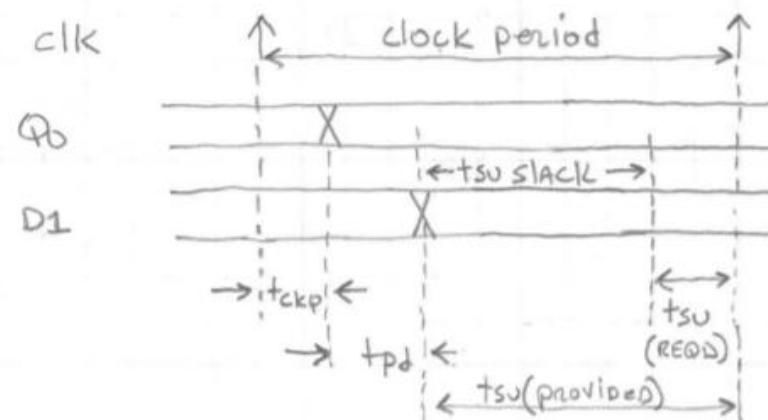
$$T_p \geq 5 \text{ ns} + 2 \text{ h}$$



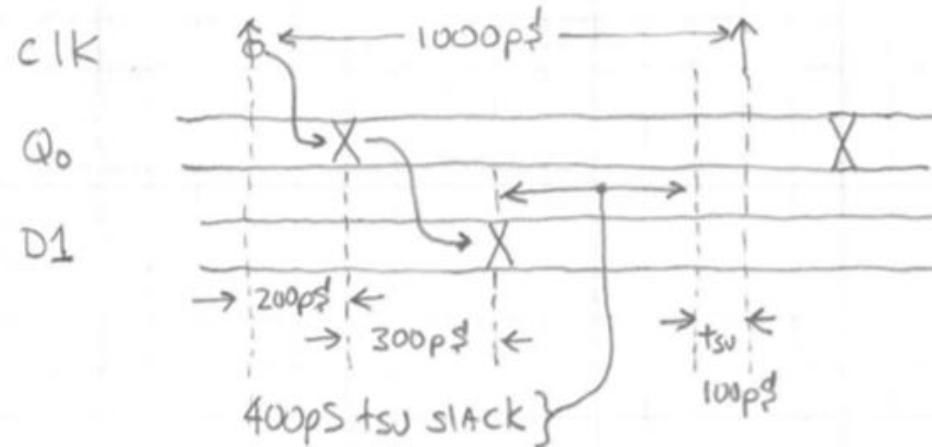
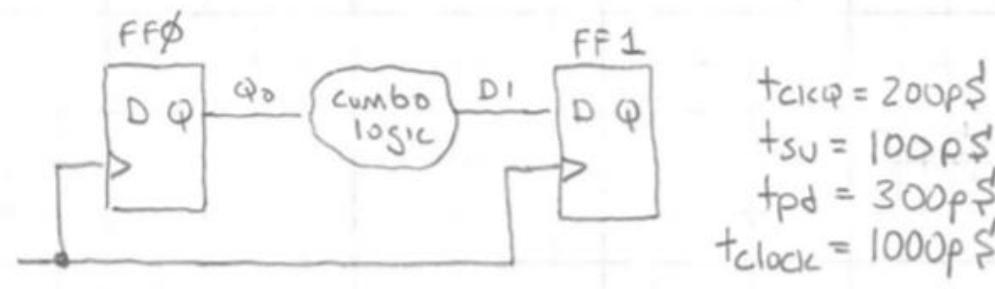
Setup Slack time :

$$\overline{T_p} - \left(T_{PDT} + T_{PDCom} + T_s \right)$$

- ▶ The circuit provides setup time as a function of the clock period, t_{ckq} and combo logic delay t_{pd} .
- ▶ The FF requires a specified t_{su} to operate correctly.
- ▶ The difference between the two is called *setup time slack*.
 - ▶ setup time slack = (provided setup time) - (required setup time)
 - ▶ We always want positive slack.



- ▶ An example: find the setup slack



$$T_P \geq T_{PD_{HC}} + T_{PD_{Comb}} + T_S$$

$$\begin{aligned} T_{SS} &= T_P - (200 + 300 + 100) \\ &= 1000 - 600 \\ &= 400 \text{ PD} \end{aligned}$$

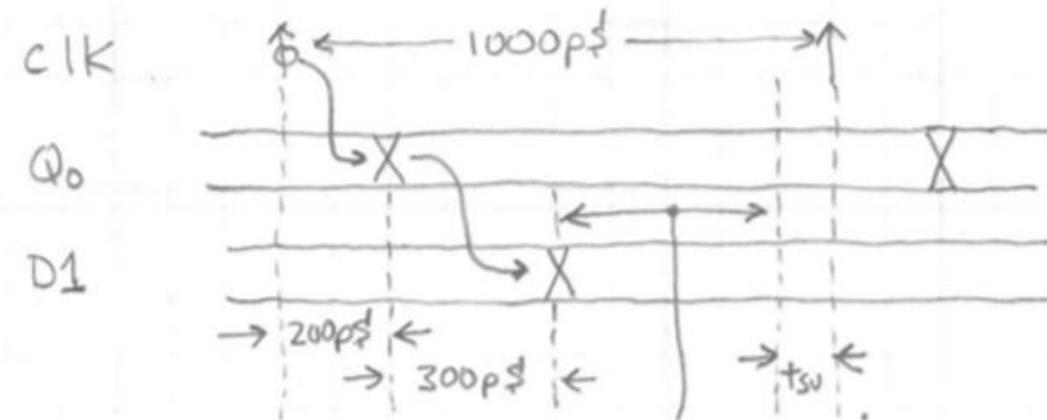
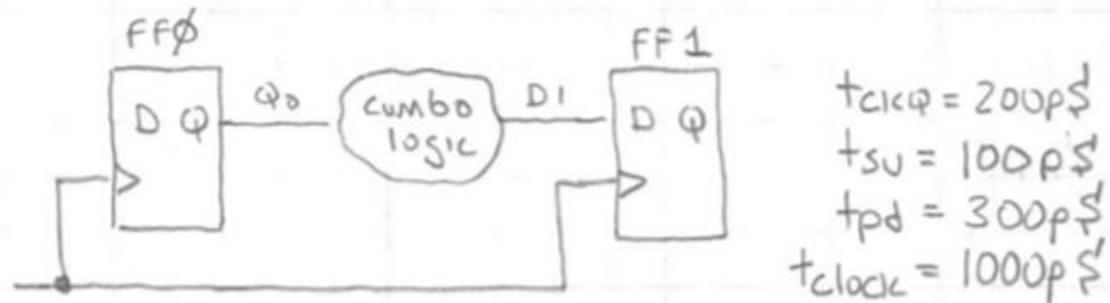
$$\text{TP} \geq T_{PD_{HC}} + T_{PD_{Comb}} + T_S$$

ISS
 T_J
Setup
Slack
time

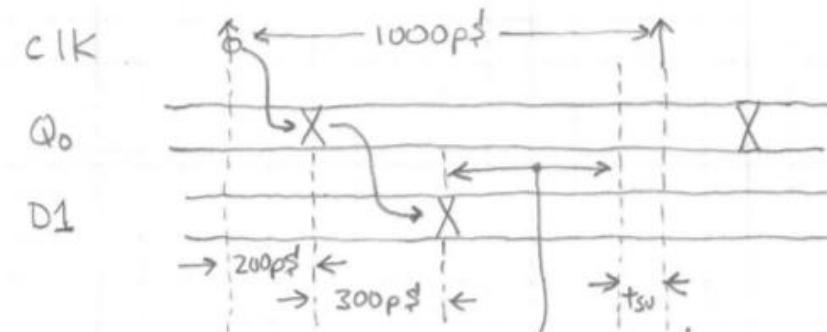
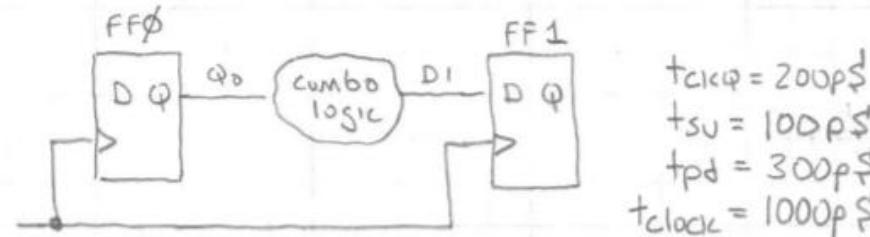
\rightarrow minimum clock period required

$$\begin{aligned} &= 1\text{ns} - 6\text{ns} \\ &= 4\text{ns PD} \checkmark \end{aligned}$$

- ▶ What is the minimum cycle time for the circuit?



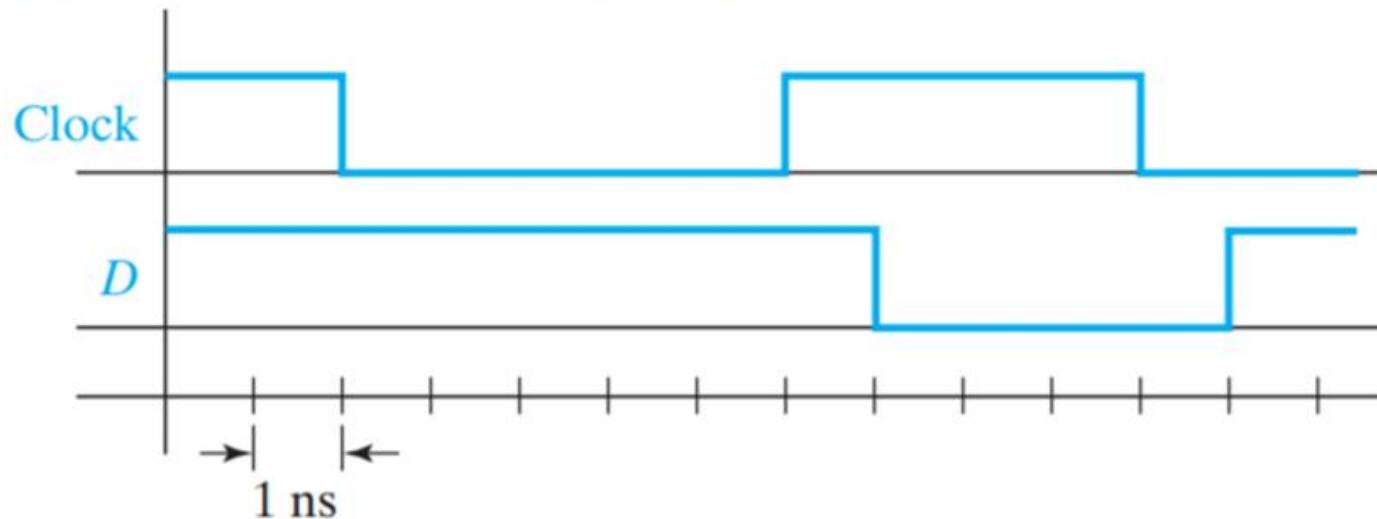
- ▶ What is the minimum cycle time for the circuit?



- ▶ minimum cycle time
 $= t_{clkq} + t_{pd} + t_{su}$
 $= 200 + 300 + 100$
 $= 600\text{pS}$

Charles H. Roth, Jr. Fundamentals of Logic Design 7th Ed. Chapter 11, 4(D) :

A D flip-flop with a falling-edge trigger is behaving erratically. It has a setup time of 2 ns and a hold time of 2 ns. The figure shows the inputs to the flip-flop over a typical clock cycle. Why might the flip-flop be behaving erratically?



- A. Hold time violation
- B. Setup time violation



Digital Logic

GO Classes

Answer :

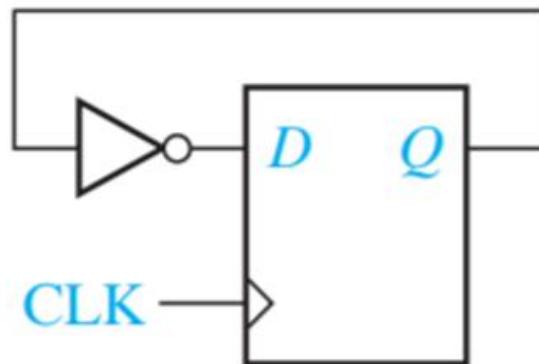
Hold time violation (D is not stable for 2 ns after second falling clock edge.)



www.goclasses.in

Charles H. Roth, Jr. Fundamentals of Logic Design 7th Ed. Chapter 11, 4(E) :

Q : The propagation delay of the inverter is 1.5 ns, and the propagation delay, hold times and setup times of the flip-flop are 3.5 ns, 1ns and 2 ns, respectively. What is the shortest clock period for the circuit which will not violate the timing constraints?



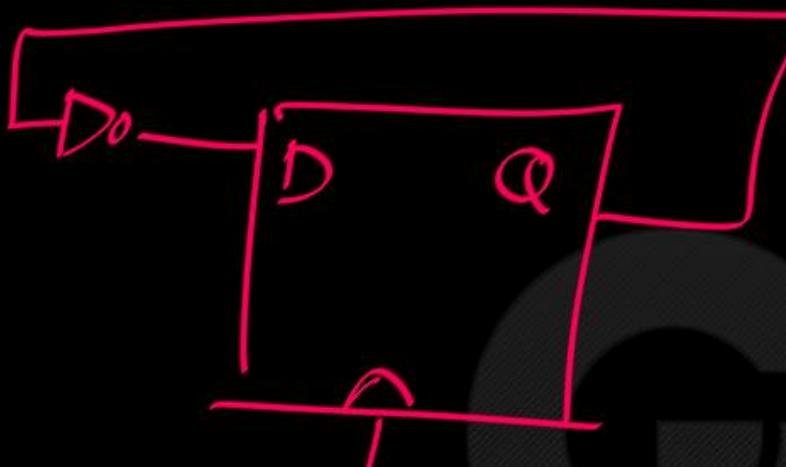
(a) Simple flip-flop circuit



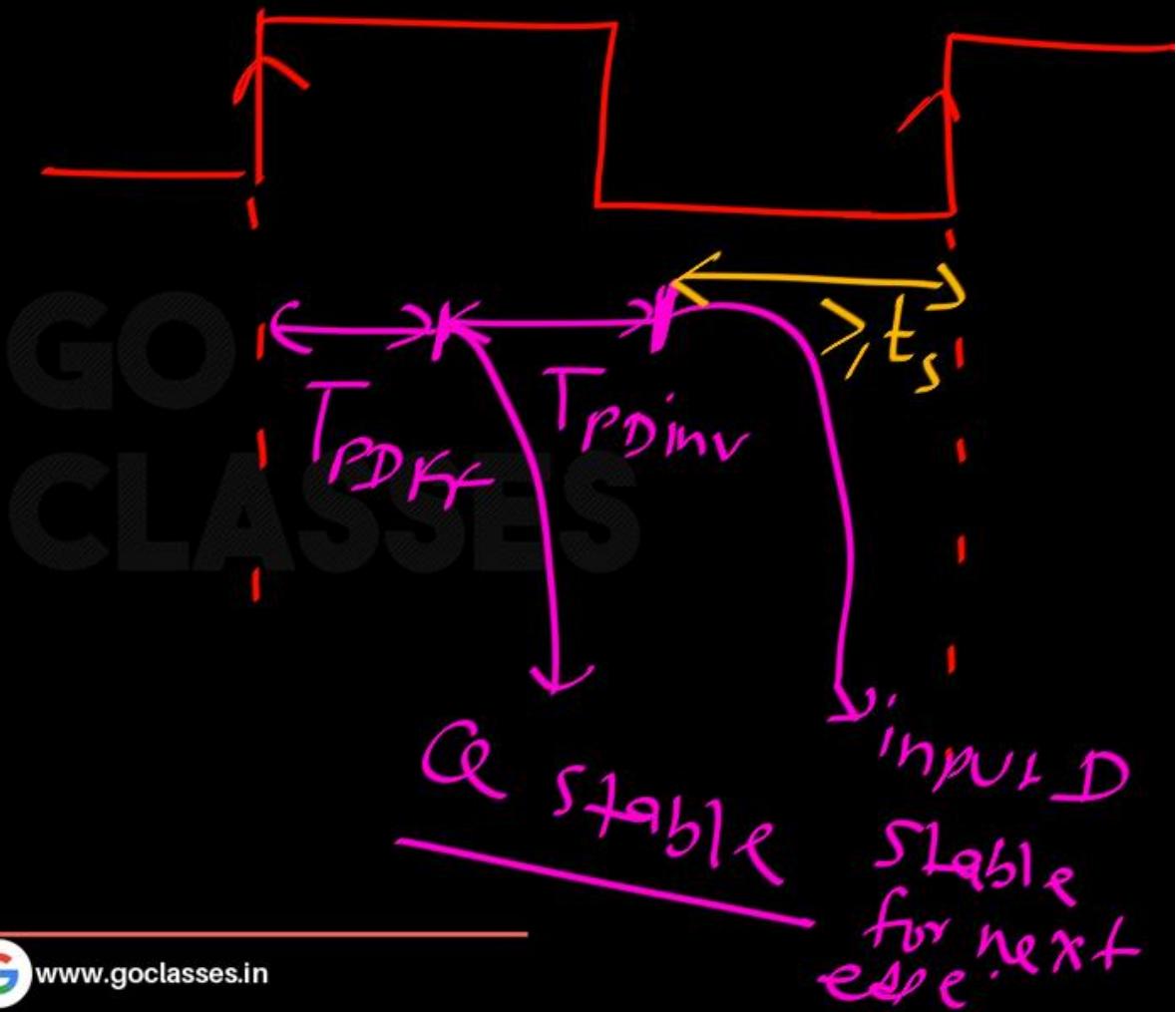
Ans : 7ns

The hold time does not affect this calculation.

3.5 ns after a clock edge, the flip-flop output will change, and 1.5 ns after that, the output of the inverter will change. Therefore, the input to the flip-flop will change 5 ns after the rising edge, which should be 2 ns before the next rising edge which is the setup time of the flip-flop which requires that the input be stable 2 ns before the rising edge; therefore, the circuit will operate correctly if minimum period of clock is 7ns.



Clock



Clock period:

$$t_p \geq T_{PDFF} + T_{PD\text{inv}} + T_s$$

$$\frac{t_p \geq 3.5 + 1.5 + 2}{}$$

$$\boxed{t_p \geq 7 \text{ ns}}$$

min. clock period = 7 ns
 max " freq = $\frac{1}{7 \text{ ns}} = 142 \text{ Hz}$

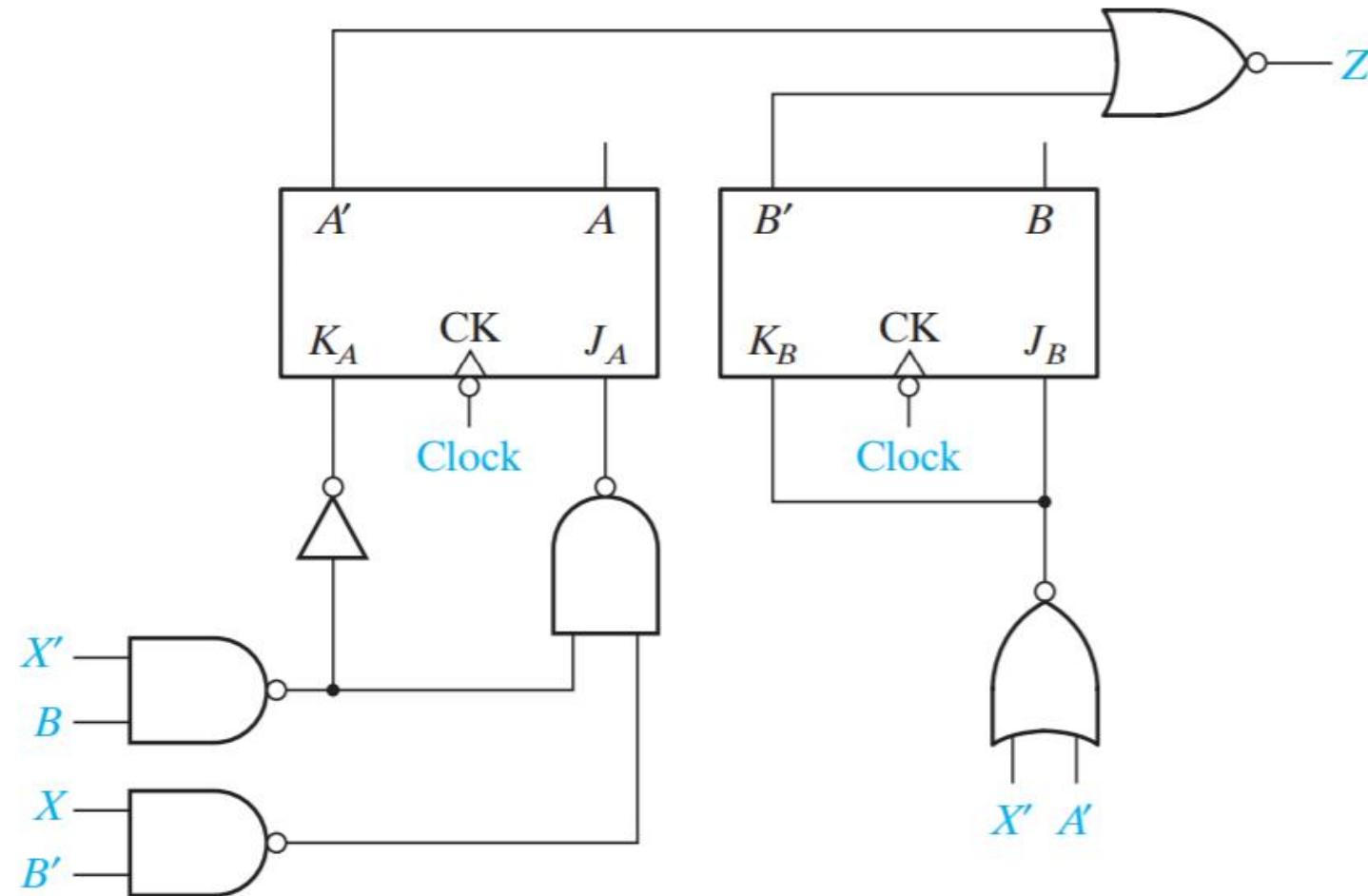


Charles H. Roth, Jr. Fundamentals of Logic Design 7th Ed. Problem 13.28 :

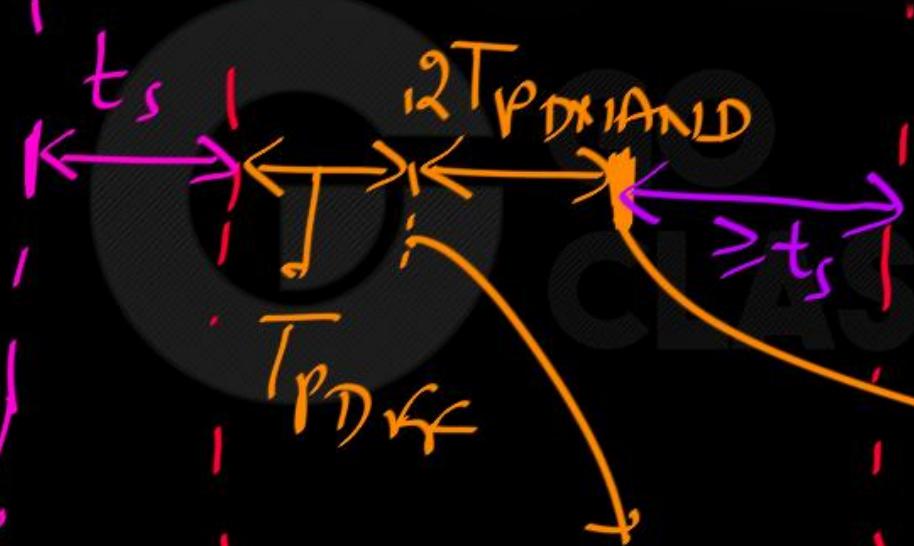
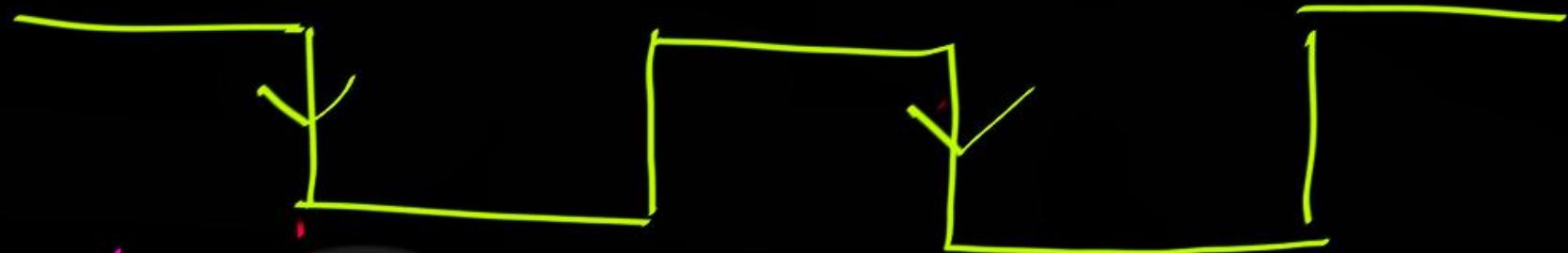
Q:

For the following circuit , assume the delays of the NAND gates and NOR gates are 3 ns, and assume the delay of the inverter is 2 ns. Assume the propagation delays and setup times for the J-K flip-flops are 4 ns and 2 ns, respectively.

What is the minimum clock period for this circuit, if X is changed early enough?



Clock



J_A, k_A, J_B, k_B
are stable.

A_1, B_1, A'_1, B'_1 are stable
for next falling edge
 J_Q, J_B, k_A, k_B are stable

$$t_p \geq t_{PDFF} + (t_{PDComb}) + t_s$$

$$t_p \geq 4\text{ ns} + 2(3\text{ ns}) + 2\text{ ns}$$

$$t_p \geq 12\text{ ns}$$

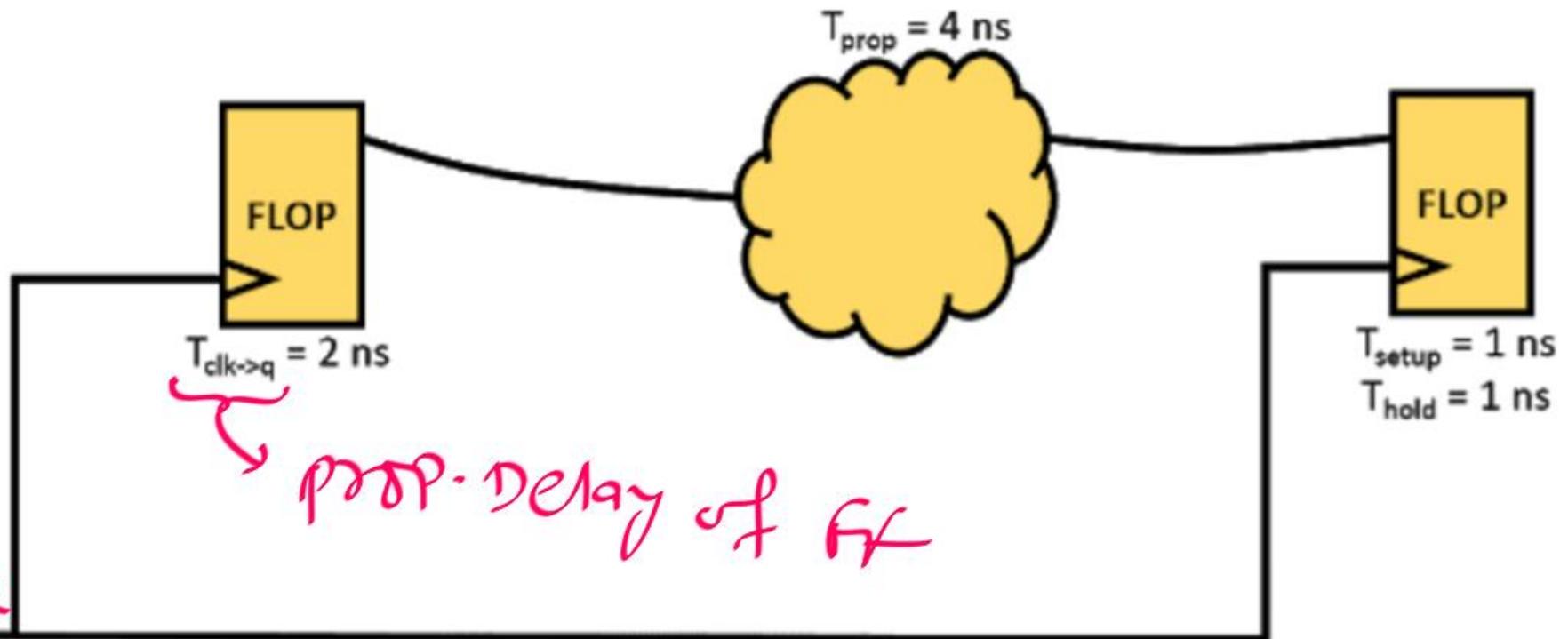
min. $t_p = 12\text{ ns}$

max freq = $\frac{1}{12\text{ ns}} = \frac{1}{12}\text{ Hz}$



NPTEL Assignment Question :

Figure below shows a timing path from a positive edge-triggered flip-flop to a positive edge-triggered flip-flop. Considering ideal clocks, and clock frequency of 100 MHz, find the setup slack for this timing path.





Ans : 3

As the clock frequency is given as a 100 MHz, time period = 1/frequency = 10 ns.



$$f = 100 \text{ MHz}$$

$$\text{tp} = \text{Clock Period} = \frac{1}{f} = \frac{1}{100 \text{ MHz}}$$
$$= \frac{1}{10^8} \text{ sec} = 10 \text{ ns}$$

$$t_p \geq t_{PDFF} + t_{PD\text{Comb}} + t_s$$

actual clock period $t_o \geq 2 + 4 + t_p$

$t_o \geq 7$

minimum setup time t_s

Setup slack time :

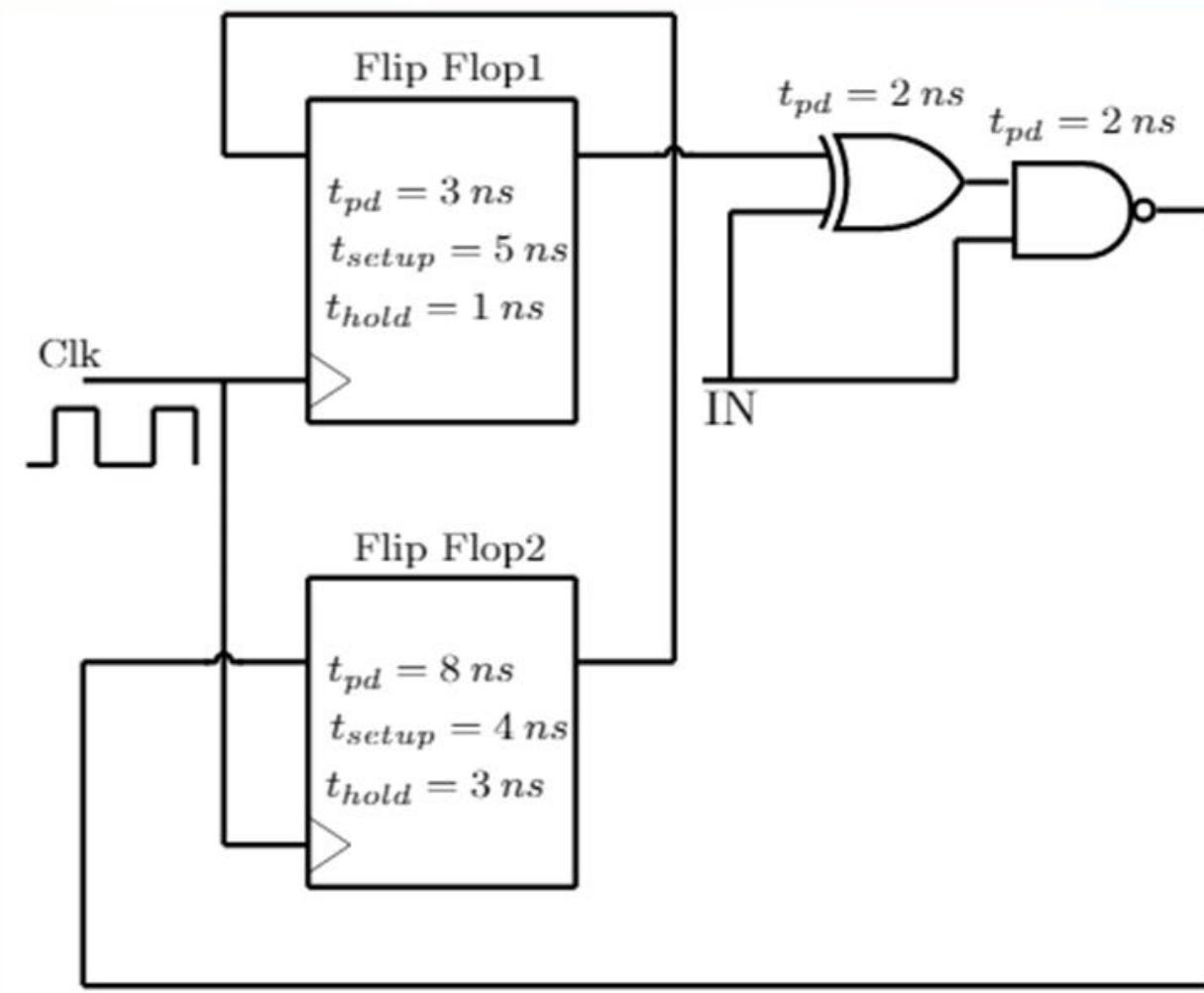
actual t_p - (minimum required t_p)
long - t_{ss}
 $= 3ns = t_{ss} = \text{setup slack time}$



<https://ec.gateoverflow.in/1473/gate-ece-2020-question-50>

GATE ECE 2020:

For the components in the sequential circuit shown below, tpd is the propagation delay, t_{setup} is the setup-time, and t_{hold} is the hold time. The maximum clock frequency (rounded off to the nearest integer), at which the given circuit can operate reliably, is _____ MHz.



ff1:

$$t_p \geq t_{PD\text{FF1}} + t_{PD\text{Comp}} + t_{S-FF2}$$

$$t_p \geq 3 + (2+2) + 4$$

$$t_p \geq 11 \text{ ns}$$

ff₂:

$$t_P \geq t_{PDFF_1} + t_{PD\text{Com}_1} + t_{S-FF_1}$$

$$t_P \geq 8 + 0 + 5$$

$$t_P \geq 13 \text{ ns.}$$

$t_p \geq 11\text{ns}$ } (ff₁ point of view)

$t_p \geq 13\text{ns}$ } (ff₂ point of view)

$t_p \geq 13\text{ns}$

min. time period:

13 ns

$$\frac{\text{max. freq. } f_{\text{max}}}{\cancel{\text{max. freq. }}} = \frac{1}{t_p(\text{min})}$$

$$= \frac{1}{13 \text{ ns}} = \frac{1}{13} \text{ GHz}$$

$$= \frac{10^9}{13} \text{ MHz} = \underbrace{76.92}_{\text{MHz}}$$

$\left. \begin{array}{l} C = 10^9 \\ m = 10^6 \end{array} \right\}$