



Counters

CLASSES



A counter is essentially a register that goes through a predetermined sequence of binary states. The gates in the counter are connected in such a way as to produce the prescribed sequence of states. Although counters are a special type of register, it is common to differentiate them by giving them a different name.

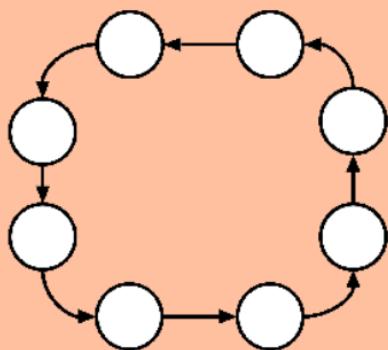
Counters are simple type of sequential circuit. A counter is usually constructed from two or more flip-flops which change states in a prescribed sequence when input pulses are received.

Counters are very widely used in almost all computers and other digital electronic systems.

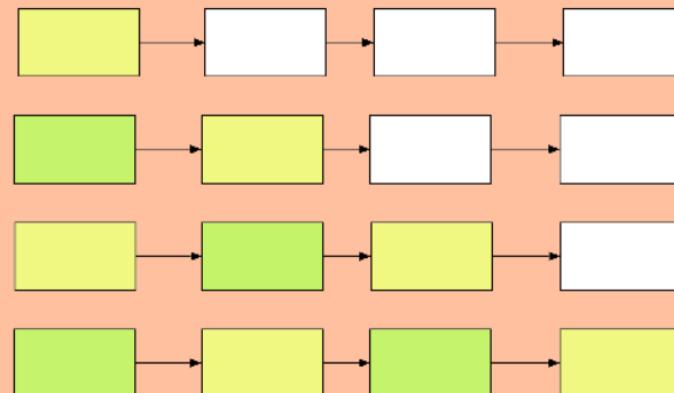
In this chapter, we will learn procedures for deriving flip-flop input equations for counters. These procedures can be applied to more general types of sequential circuits.



Counter & Shift Register



VS





A Sequential Circuit that goes through a prescribed sequence of states upon the application of input pulses is called a counter.

The input pulses may be clock pulses, or they may originate from some external source and may occur at a fixed interval of time or at random.

The sequence of states may follow the binary number sequence or any other sequence of states.

Example :

A counter that follows the binary number sequence is called a binary counter . An n -bit binary counter consists of n flip-flops and can count in binary from 0 through $(2^n) - 1$.

sequential circuits : Circuits with flipflops.

① Registers

② Counters

③ Sequence detectors





A counter, just like any Sequential Circuit, can be represented by State Diagram, State Table etc..

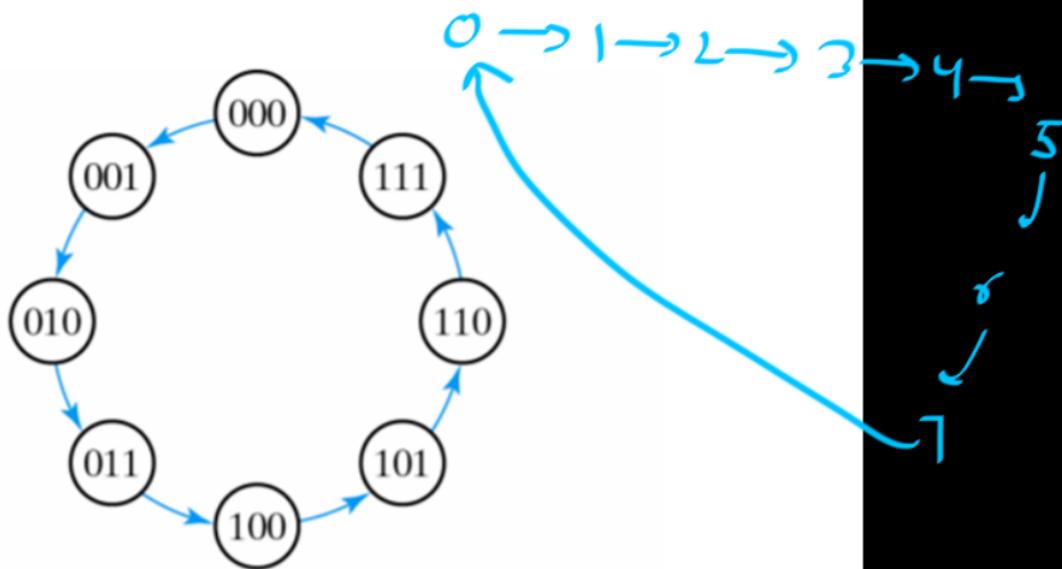




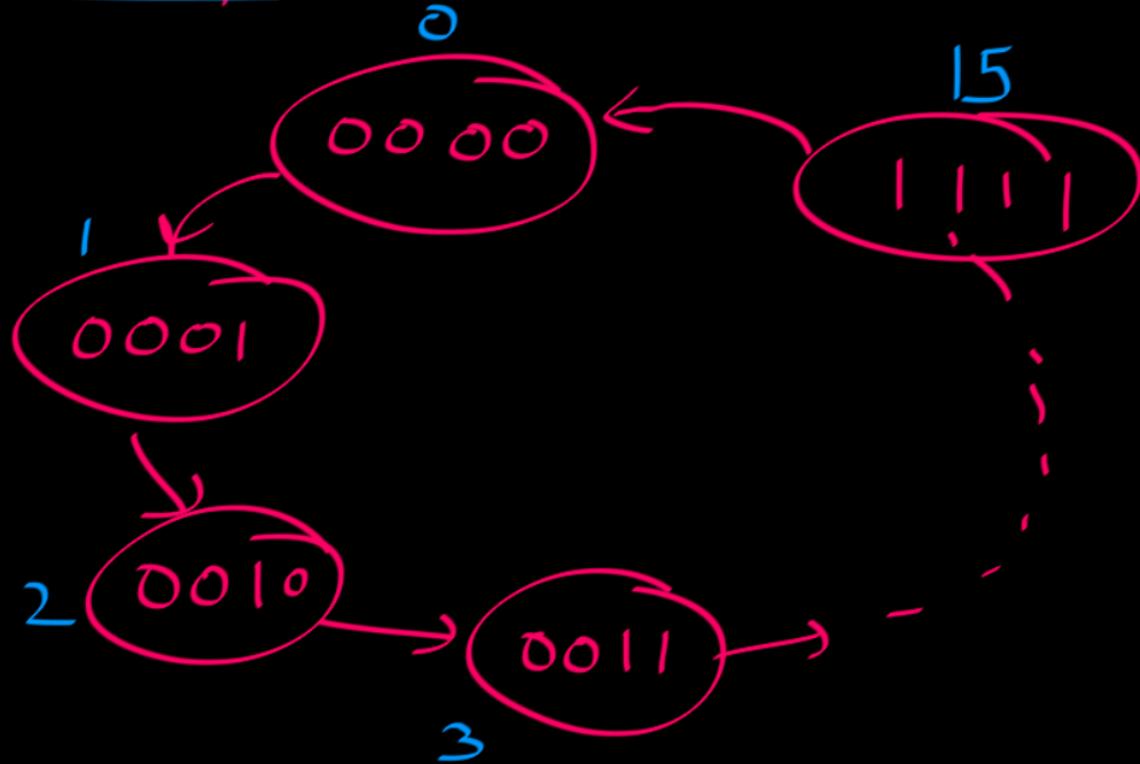
Example 1 :

state diagram of a counter (this counter is called Binary Counter):

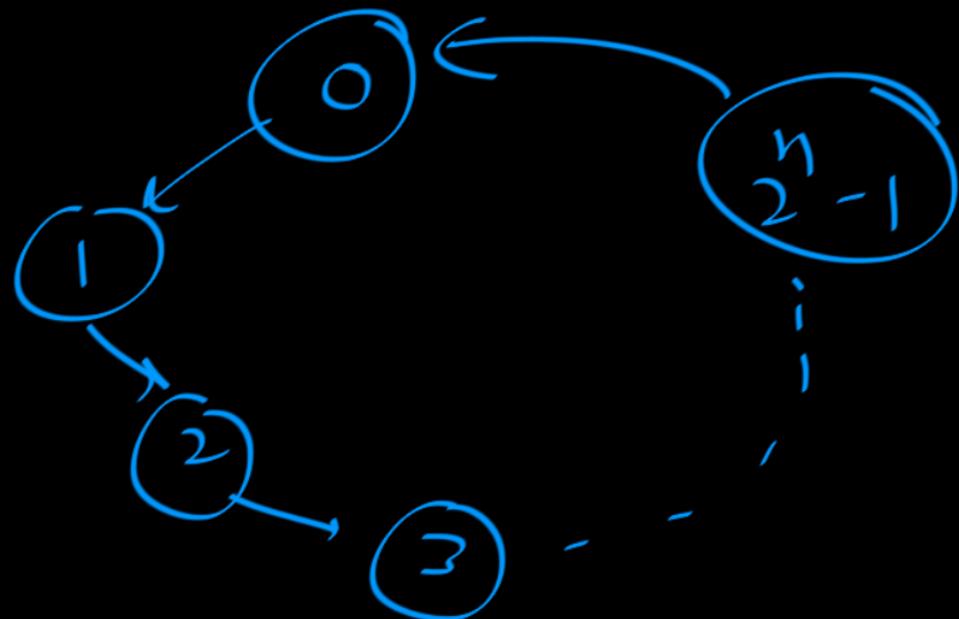
The state diagram and state table of a 3-bit binary counter are:



4-bit binary Counter



n-bit binary Counter :





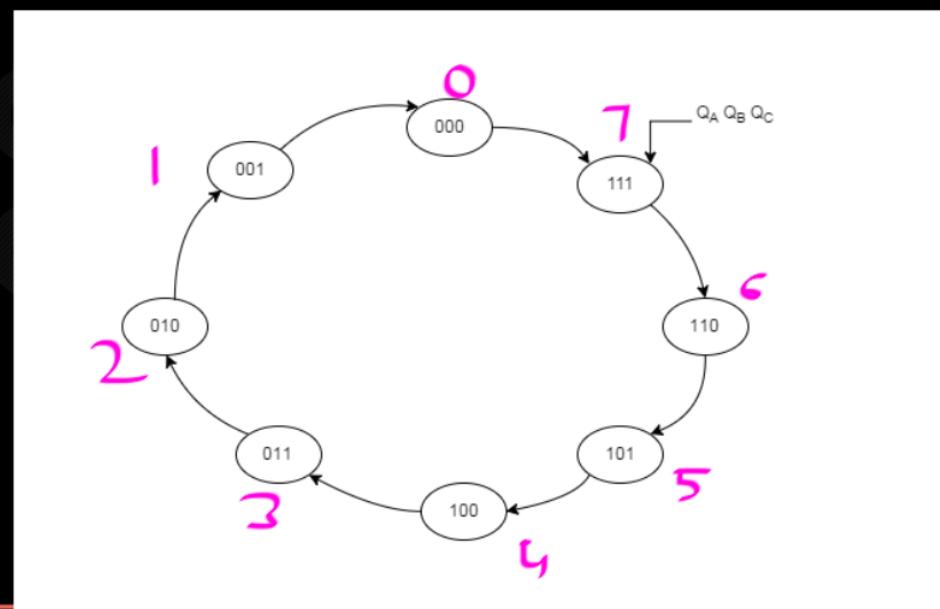
Example 2 :

state diagram of a counter (this counter is called Binary countdown Counter) :

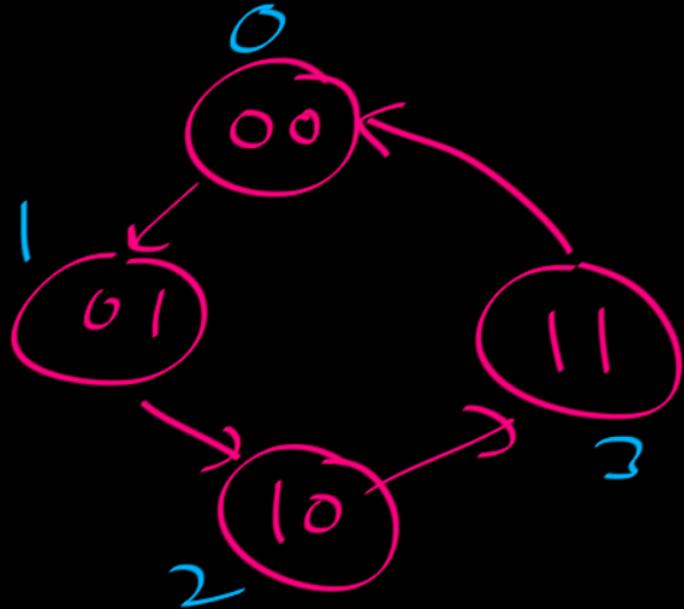
A binary counter with a reverse count is called a binary countdown counter . In a countdown counter, the binary count is decremented by 1 with every input count pulse.

The count of a four-bit countdown counter

starts from binary 15 and continues to binary counts 14, 13, 12, . . . , 0 and then back to 15.

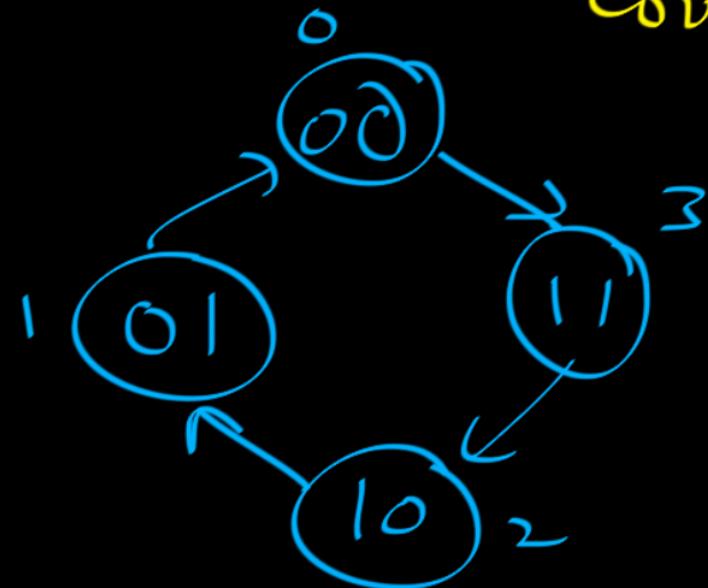


2-bit binary Counter



$0 \rightarrow 1 \rightarrow 2 \rightarrow 3$

2-bit binary Countdown Counter

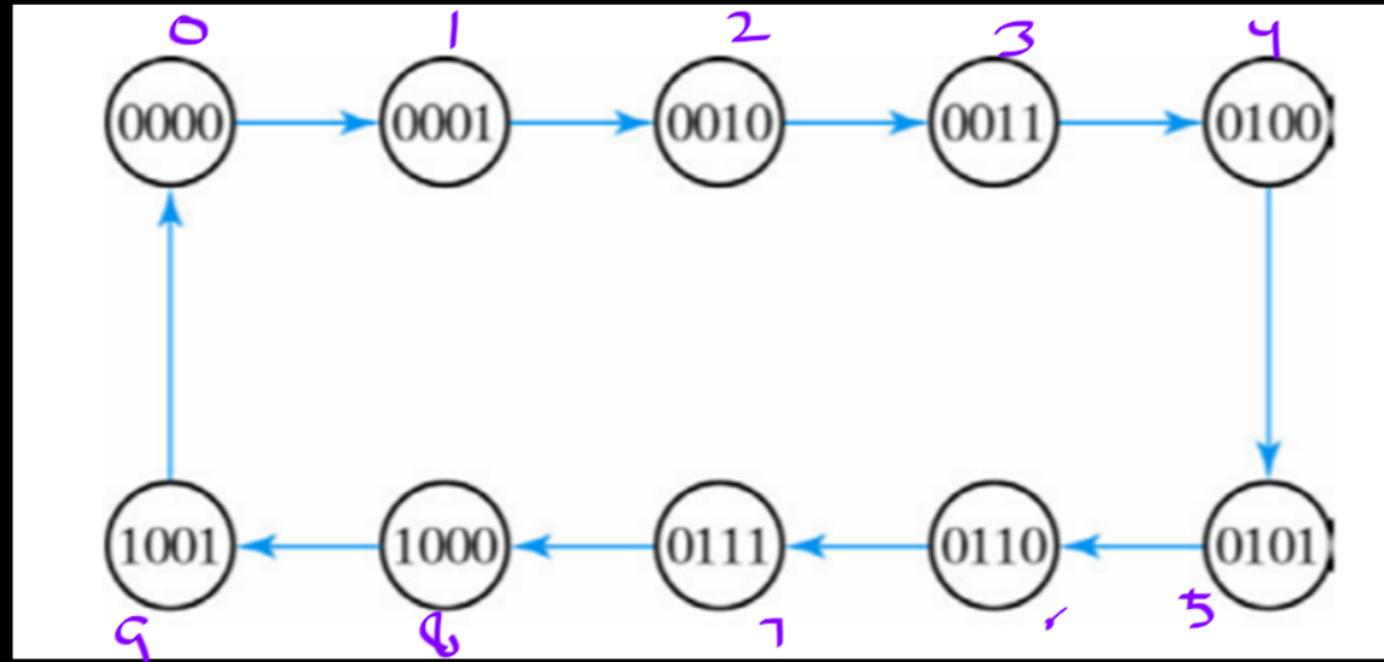


$3 \rightarrow 2 \rightarrow 1 \rightarrow 0$



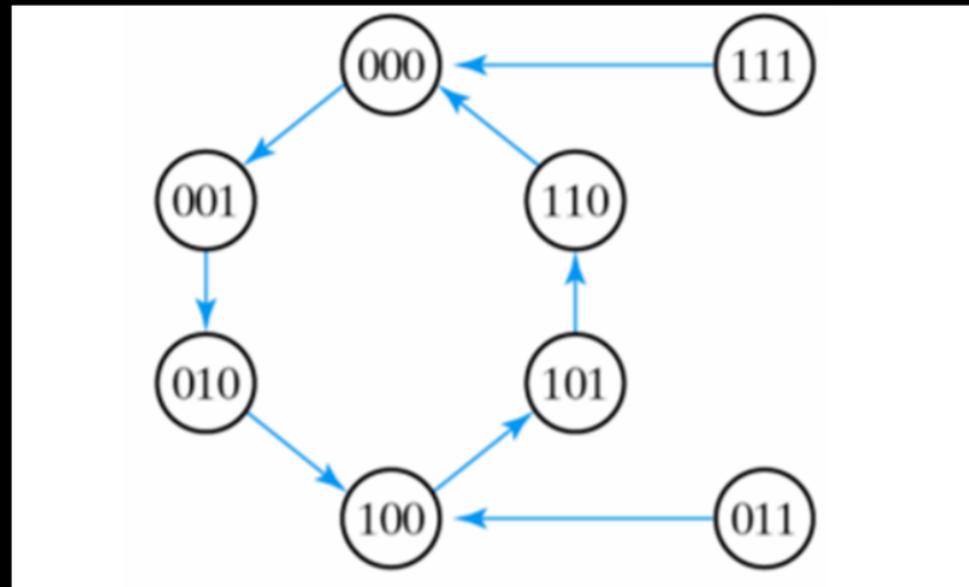
Example 3 :

A decimal counter follows a pattern of 10 states:



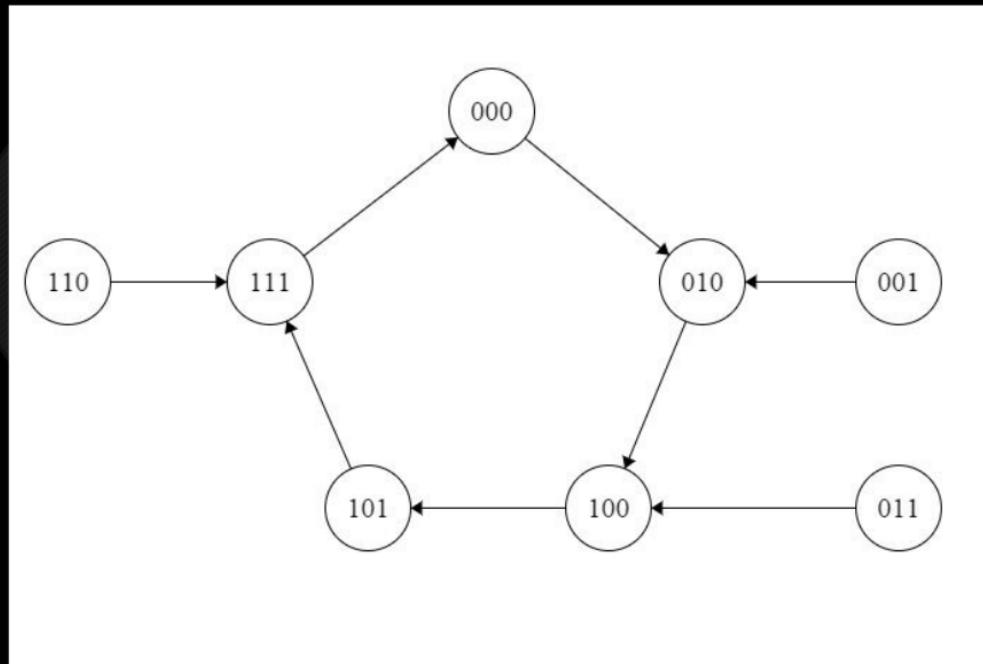


Example 4 :
state diagram of a counter :



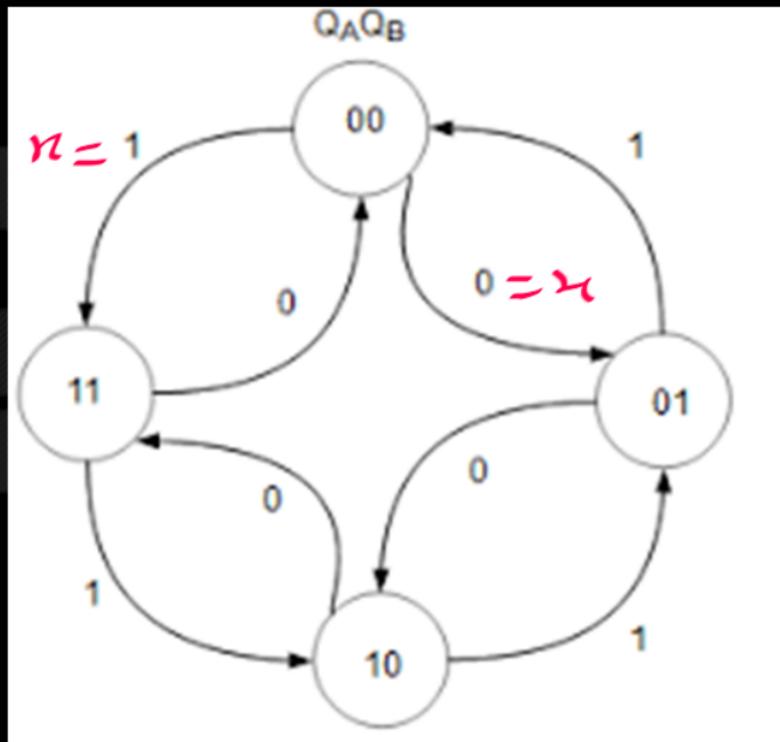


Example 5 :
state diagram of a counter :



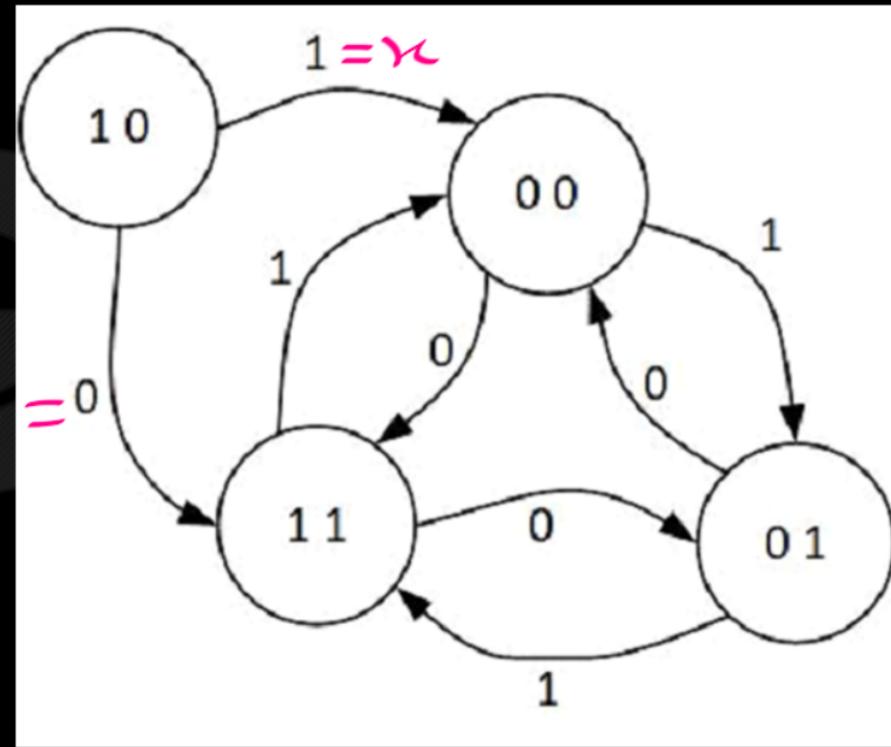
Example 6 :

state diagram of a counter :



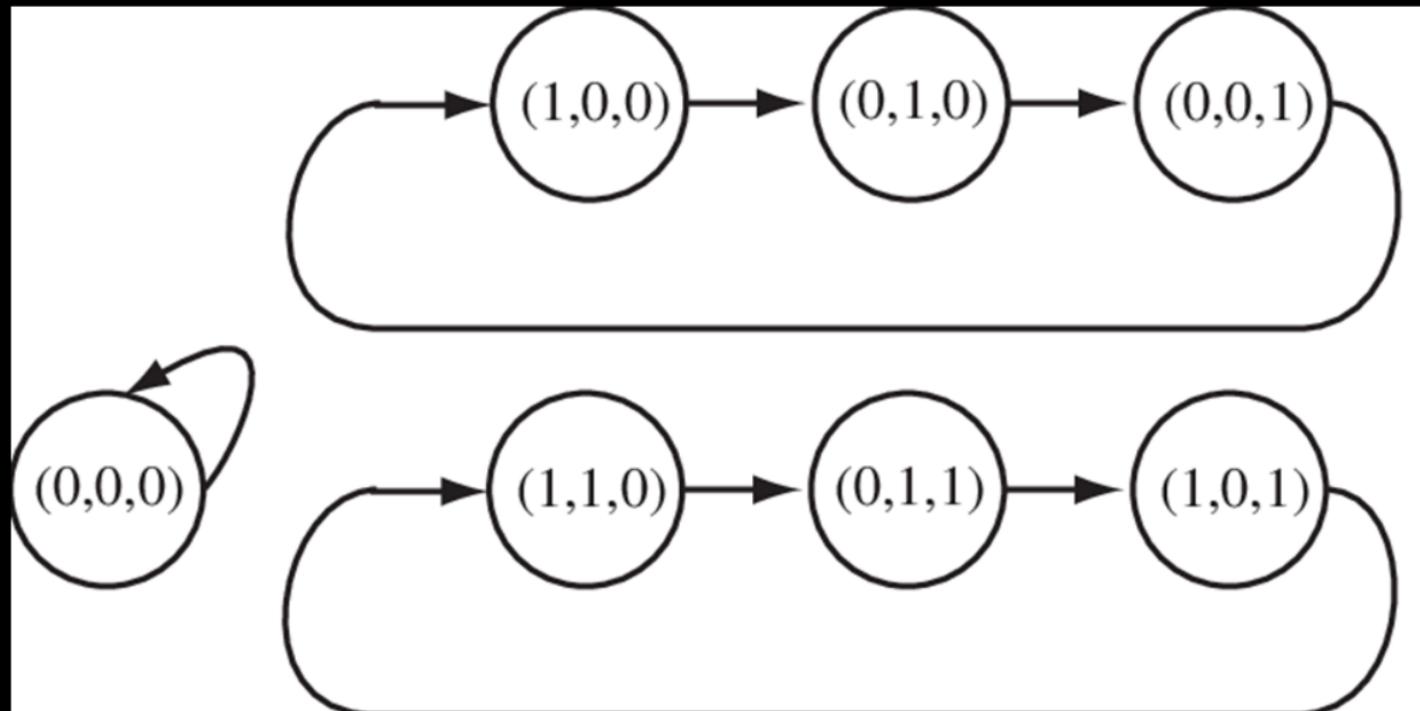
Example 7 :

state diagram of a counter :





Example 8 :
state diagram of a counter :





Registers and Counters

A circuit with flip-flops is considered a sequential circuit even in the absence of combinational logic. Circuits that include flip-flops are usually classified by the function they perform. Two such circuits are *registers* and *counters*:

- **Register** – is a group of flip-flops. Its basic function is to hold information within a digital system so as to make it available to the logic units during the computing process. However, a register may also have additional capabilities associated with it.
- **Counter** – is essentially a register that goes through a predetermined sequence of states. The gates in the counter are connected in such a way as to produce the prescribed sequence of binary states.

Applications of registers include serial addition, convolutional encoders for error-control coding, and pseudo-random binary sequence generators.

Counters are primarily used as pattern generators.

Counter:

a sequential circuit

that

goes through a pre-defined

Sequence of States.





Types of Counter :

Counter can be broadly divided into synchronous and asynchronous types.

Synchronous counter has its flip-flops clocked at the same time, whilst asynchronous counter is not. In Asynchronous counter, the clock of a flip-flop is fed from the output of the previous flip-flop.

Asynchronous counter suffers delay problem whilst, synchronous counter will not.

Asynchronous Counter is also referred as ripple counter for the reason of delay feeding of the clock pulse from one flip-flop to another.



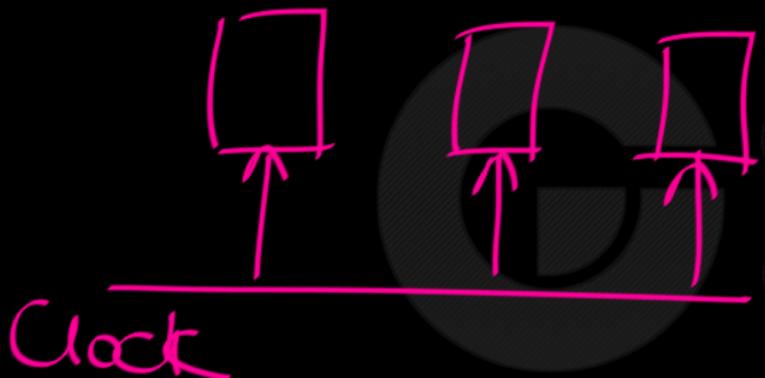
Types of Counter :

Counter can be broadly divided into synchronous and asynchronous types.

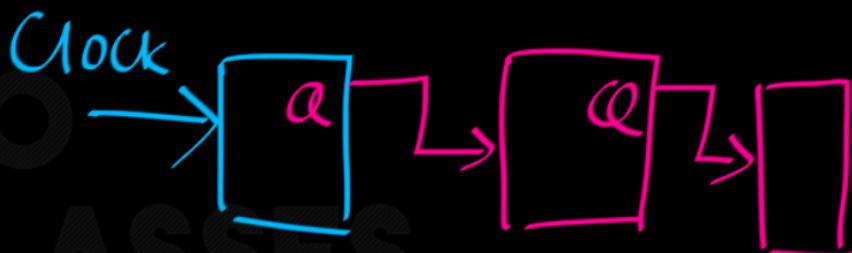
Asynchronous Counters :

Counters arranged so that the output of one flip-flop generates the clock input of the next higher stage are generally called asynchronous counters (or ripple counter). In other words, in asynchronous counters, the CLK inputs of all flip-flops (except the first one) are triggered not by the incoming pulses but rather by the transition that occurs in other flip-flops. Therefore, the change of state of a particular flip-flop is dependent upon the present state of other flip-flops.

Synch. Counter



Asynch. Counter:



Types of Counter :

Counter can be broadly divided into synchronous and asynchronous/ripple counters.

In a ripple counter, a flip-flop output transition serves as a source/clock for triggering other flip-flops. In other words, the input of some or all flip-flops are triggered, not by the common clock pulses, but rather by the transition that occurs in other flip-flop outputs.

In a synchronous counter, the inputs of all flip-flops receive the common clock. Figure 9.1 and 9.2 respectively show a modulus 4 synchronous and asynchronous counters.

Modulus of a counter is defined as the number of unique states that a counter will sequence through.

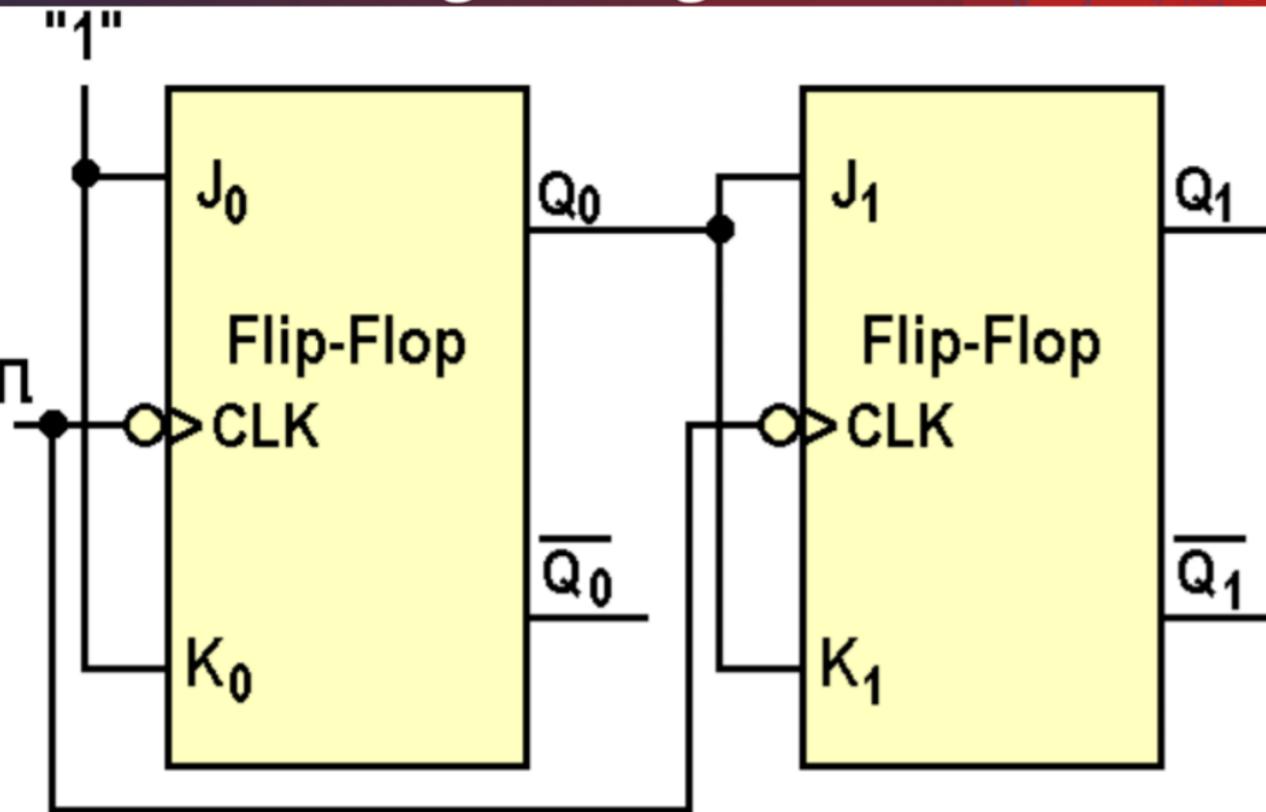
Clock

Figure 9.1: A modulus 4 2-bit synchronous counter

Clock

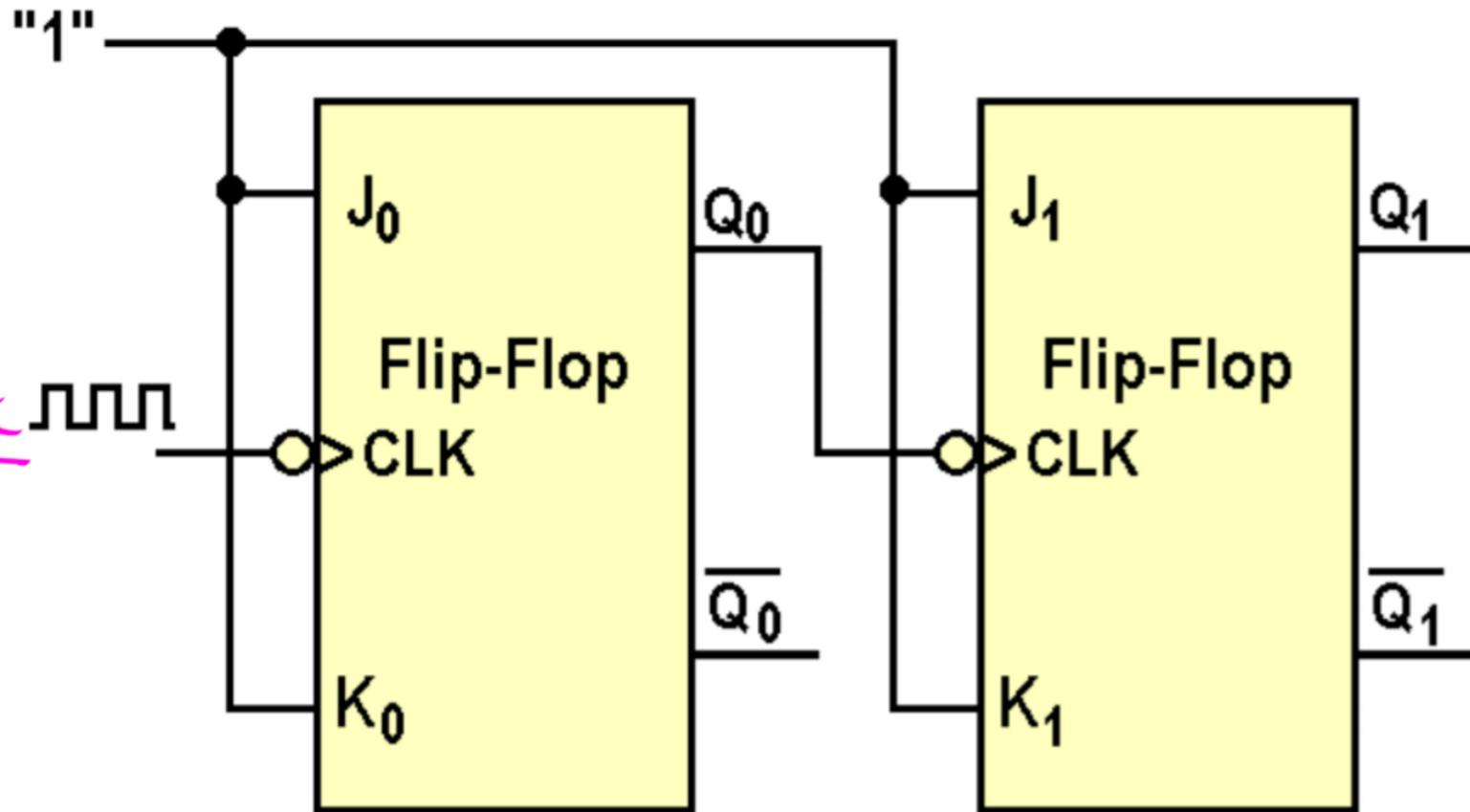
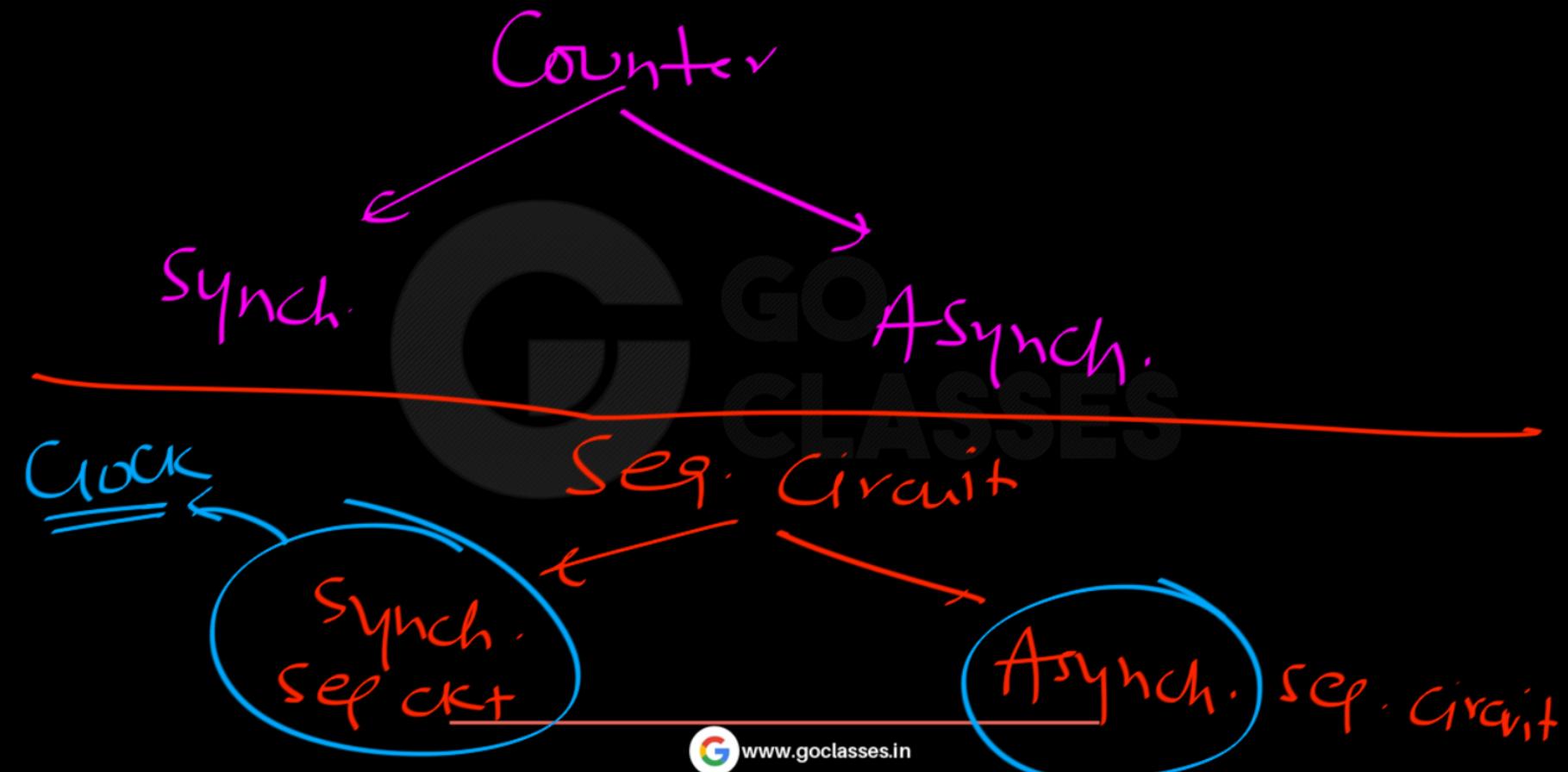
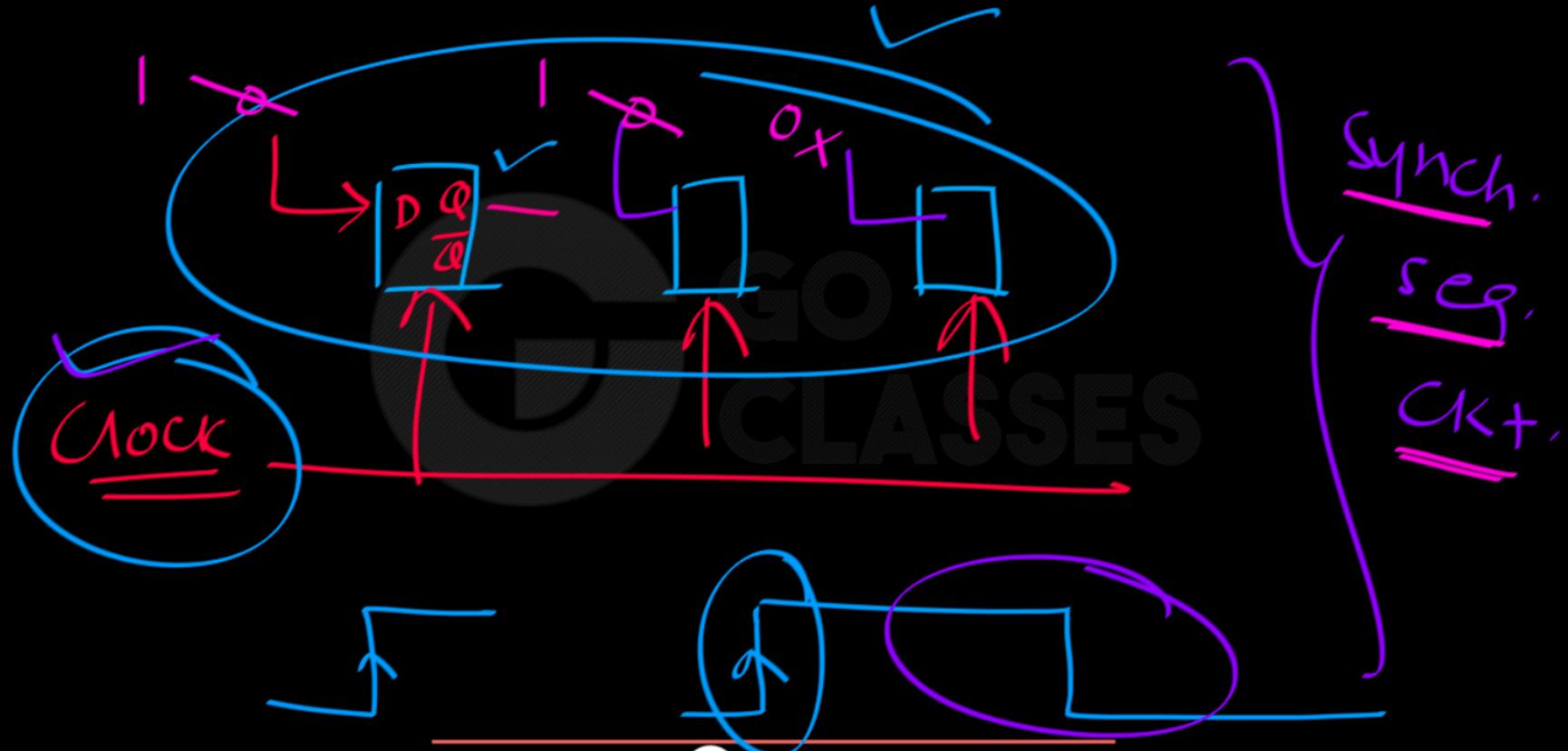


Figure 9.2: A modulus 4 2-bit asynchronous counter



- Depending upon the way the states change, **sequential circuits can be categorized into two types:**
 - a) Synchronous: The states change in synchronism with a clock pulse.
 - b) Asynchronous: There is no clock pulse for synchronism; all state changes occur depending on the delays of the circuit elements (e.g. gates).





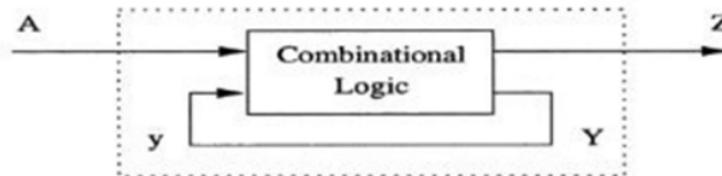
Asynch. Seq. Circ.:

As soon as inputs change,
outputs change immediately,
without waiting for any clock or
something.

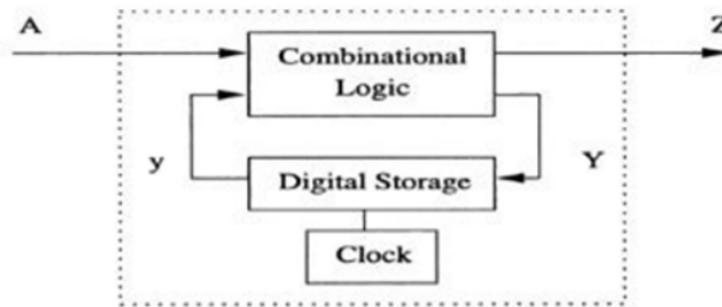
Types of Sequential Circuits

In Asynchronous sequential circuits the output of the logic circuit can change state at any time, as soon as any input changes its state whereas in the case of synchronous systems a signal namely clock signal is used to determine/control the exact time at which any output can change its state. These are also called as clocked sequential circuits.

Asynchronous



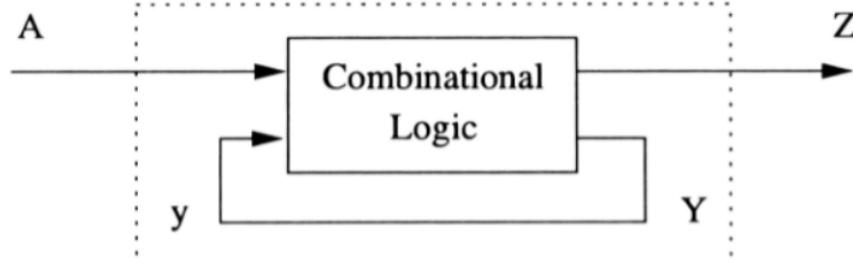
Synchronous



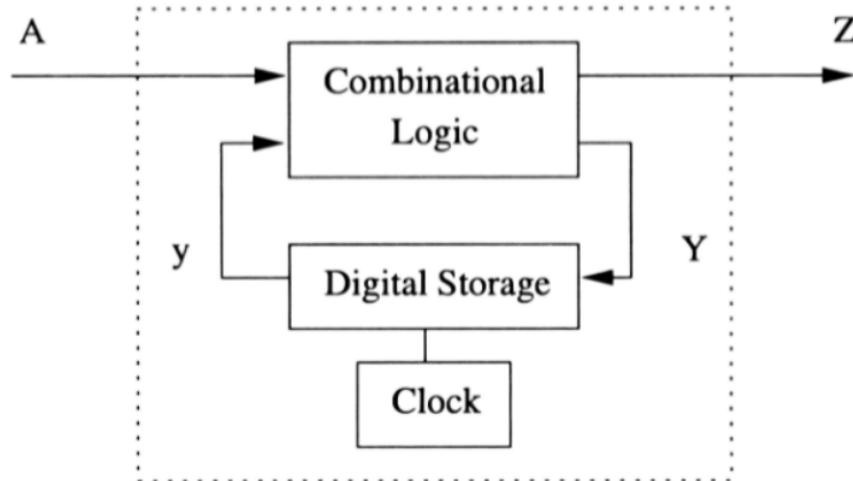


Digital Logic

Asynchronous



Synchronous





Synchronous vs. Asynchronous

- Synchronous circuits have sequential elements whose outputs change at the same time.
- Asynchronous circuits have sequential elements whose outputs change at different times.
- Disadvantages of Asynchronous Circuits
 - Difficult to analyze operations
 - Intermediate states that are not part of the desired design may be generated



Asynchronous/Ripple Counters

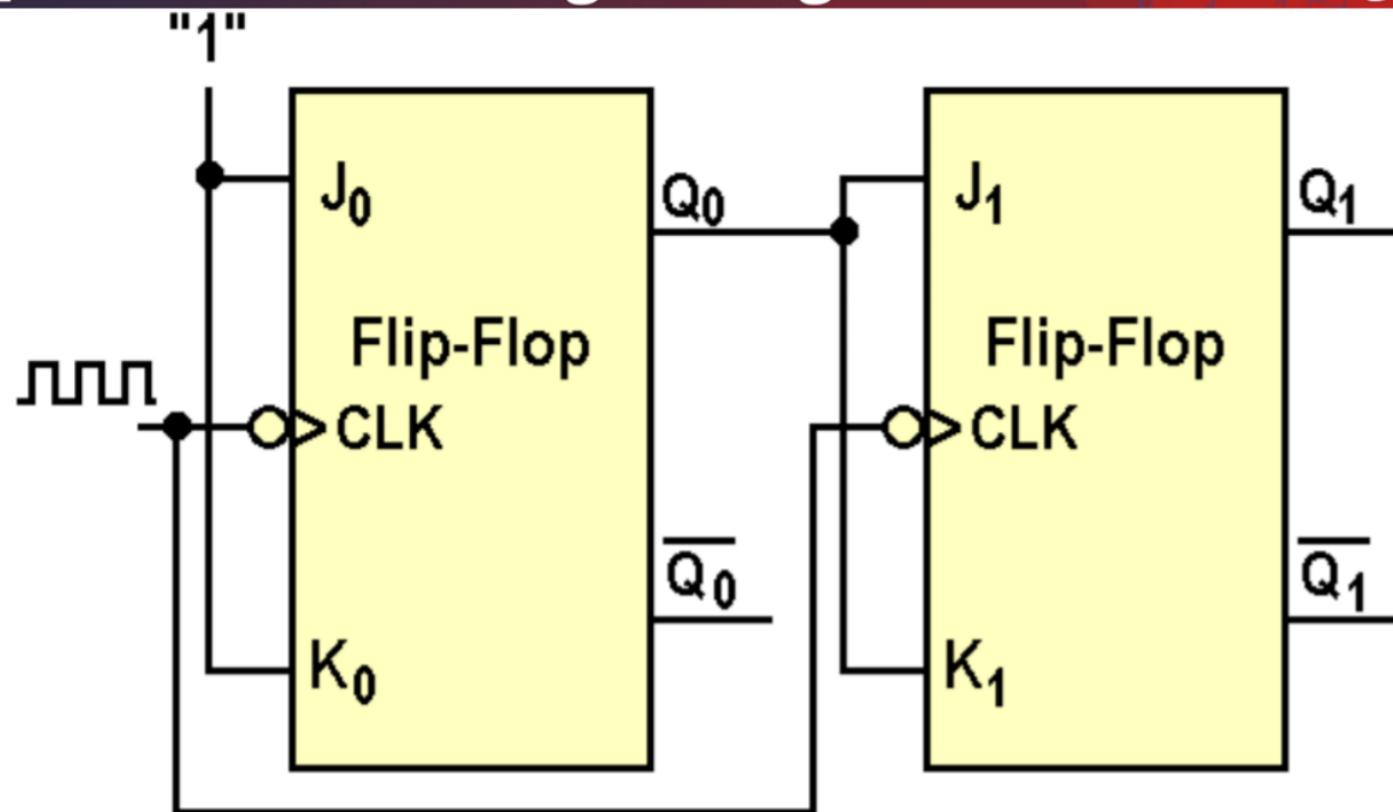


Figure 9.1: A modulus 4 2-bit synchronous counter

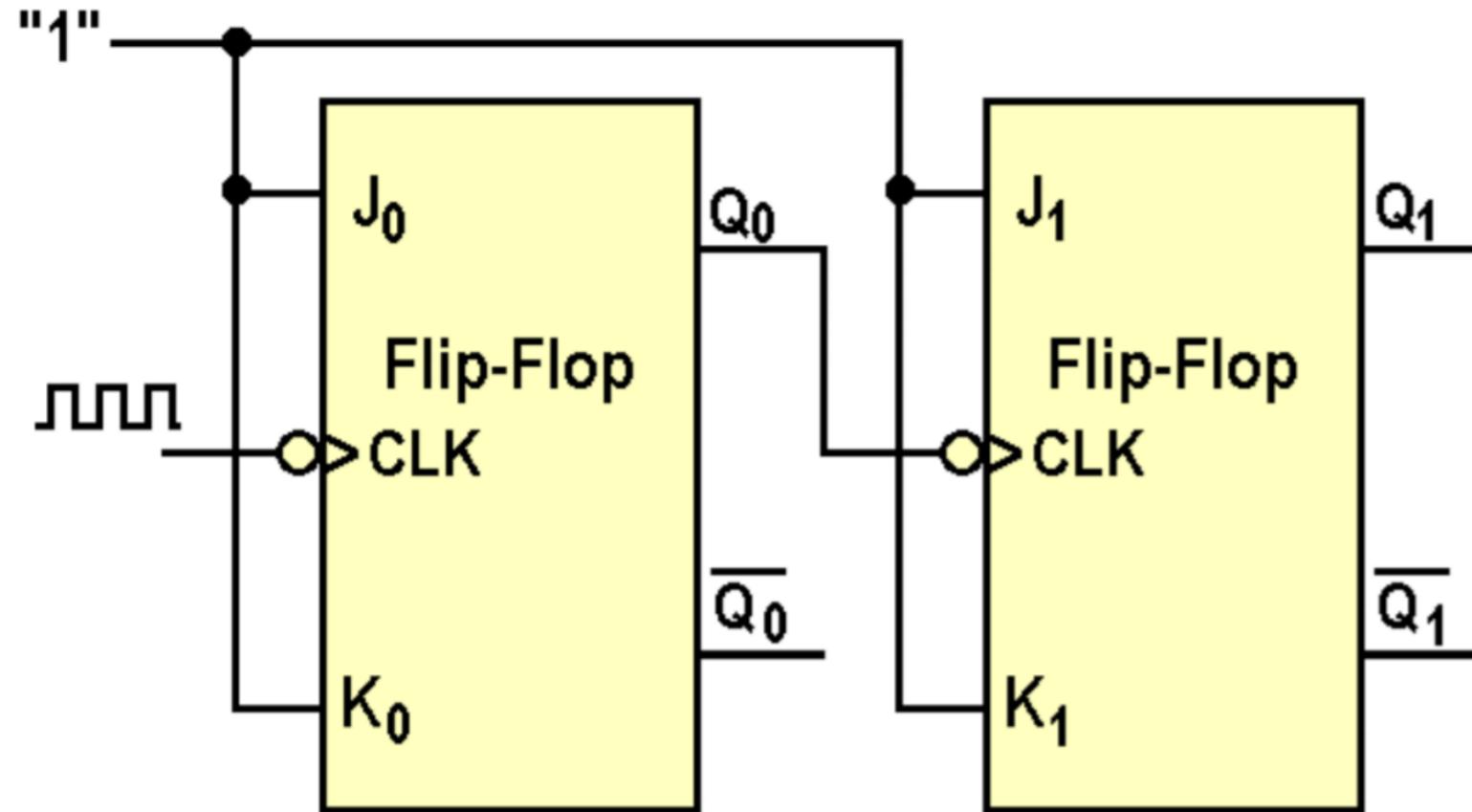


Figure 9.2: A modulus 4 2-bit asynchronous counter



FlipFlop

- The memory elements used in clocked sequential circuits are called flipflops. These circuits are binary cells capable of storing one bit of information.
- A flipflop circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states
- A bi stable device
- Have two outputs one complement of another
- Applications of Flipflops
 - Counters ?
 - Shift Registers ✓
 - Storage Registers ✓
 - Frequency Dividers ?



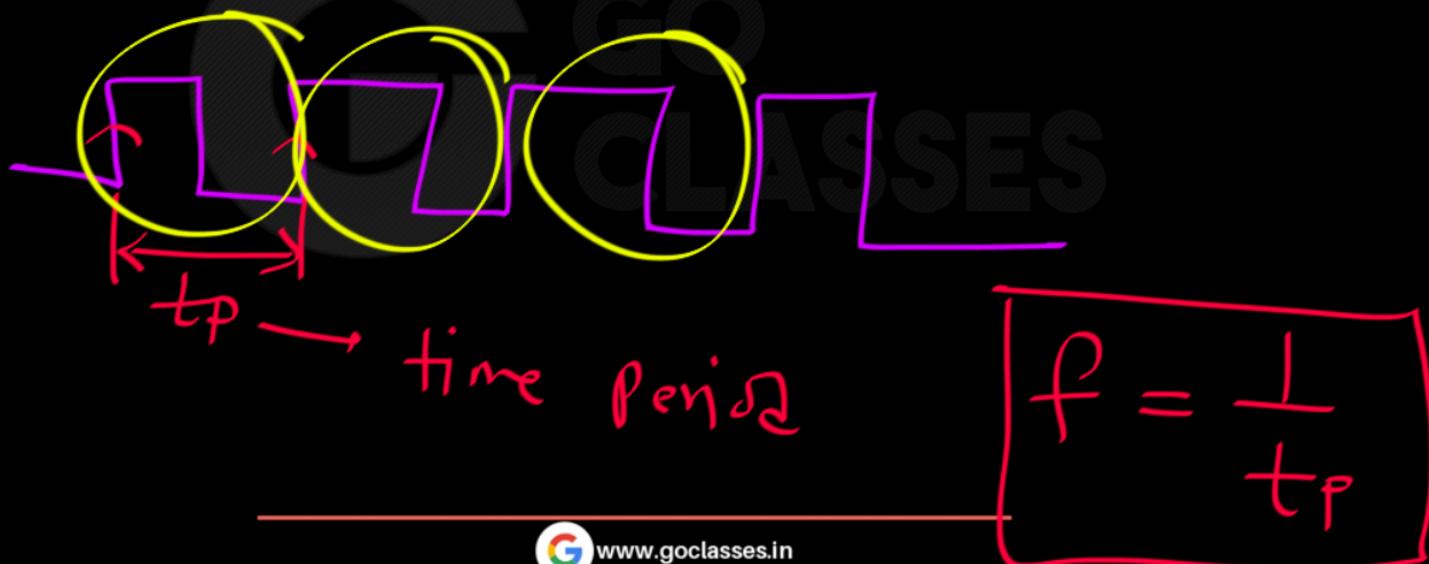
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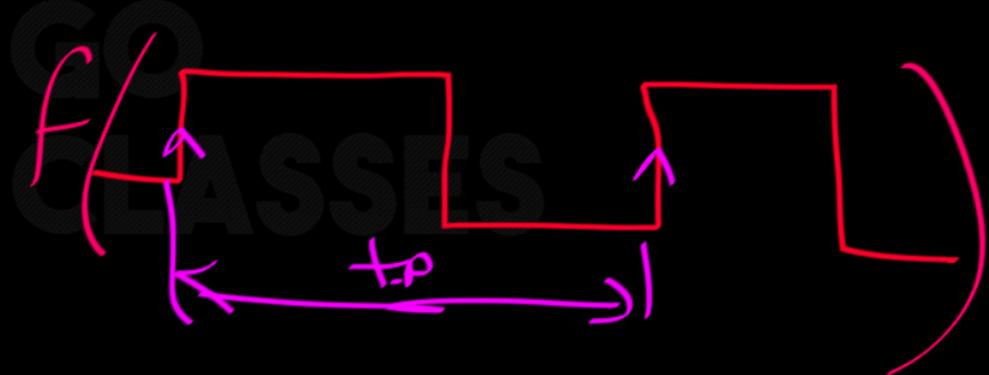
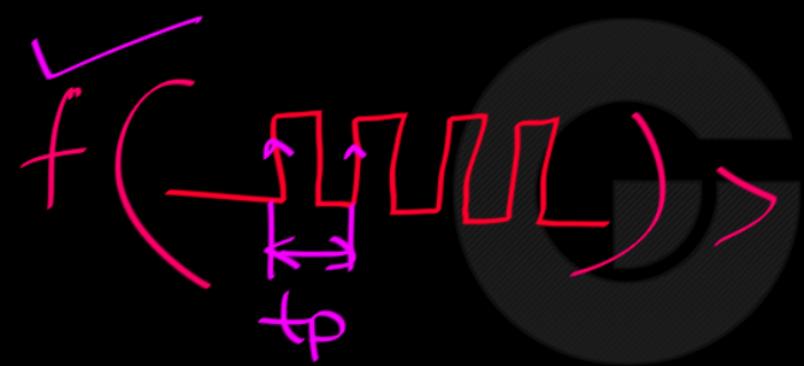
Q :

Given a clock signal of frequency f Hz, how to generate another clock of frequency f/2 Hz. i.e. Frequency division circuit.

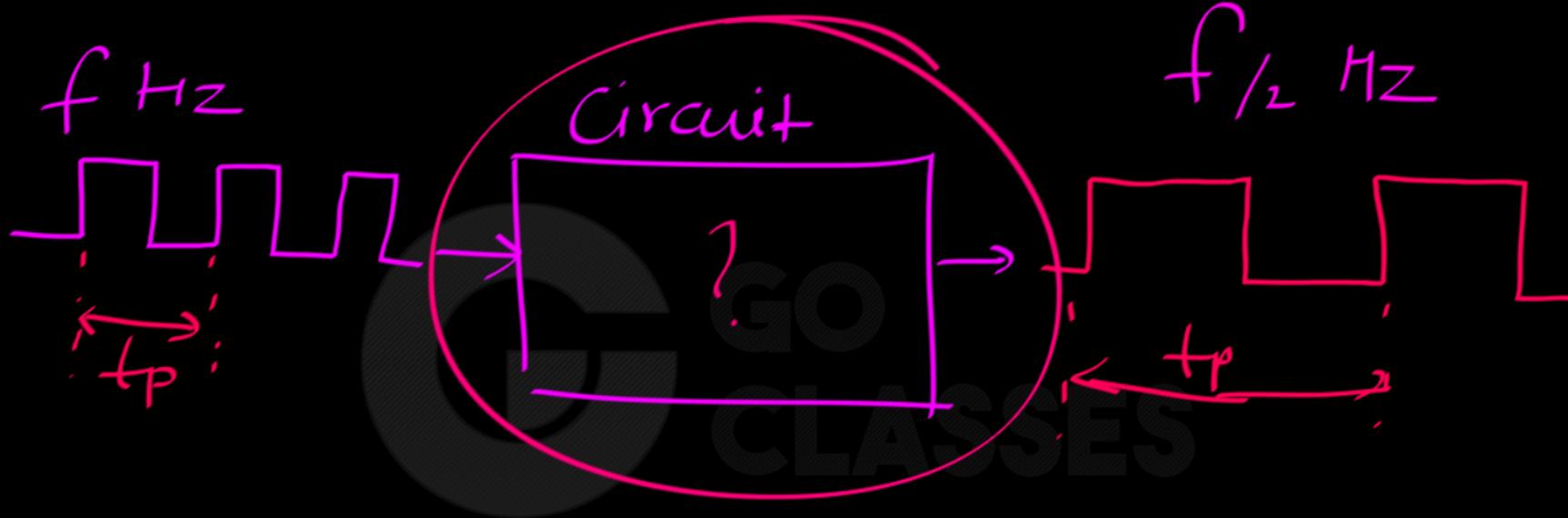




frequency : $f \text{ Hz} = f \text{ oscillations}$
per second.

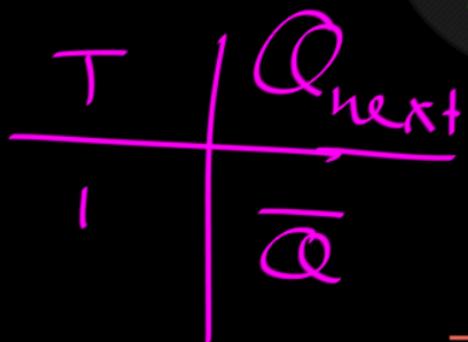
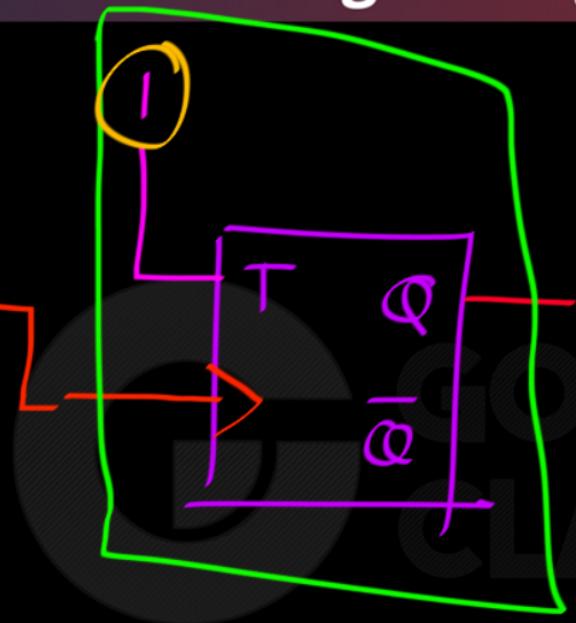


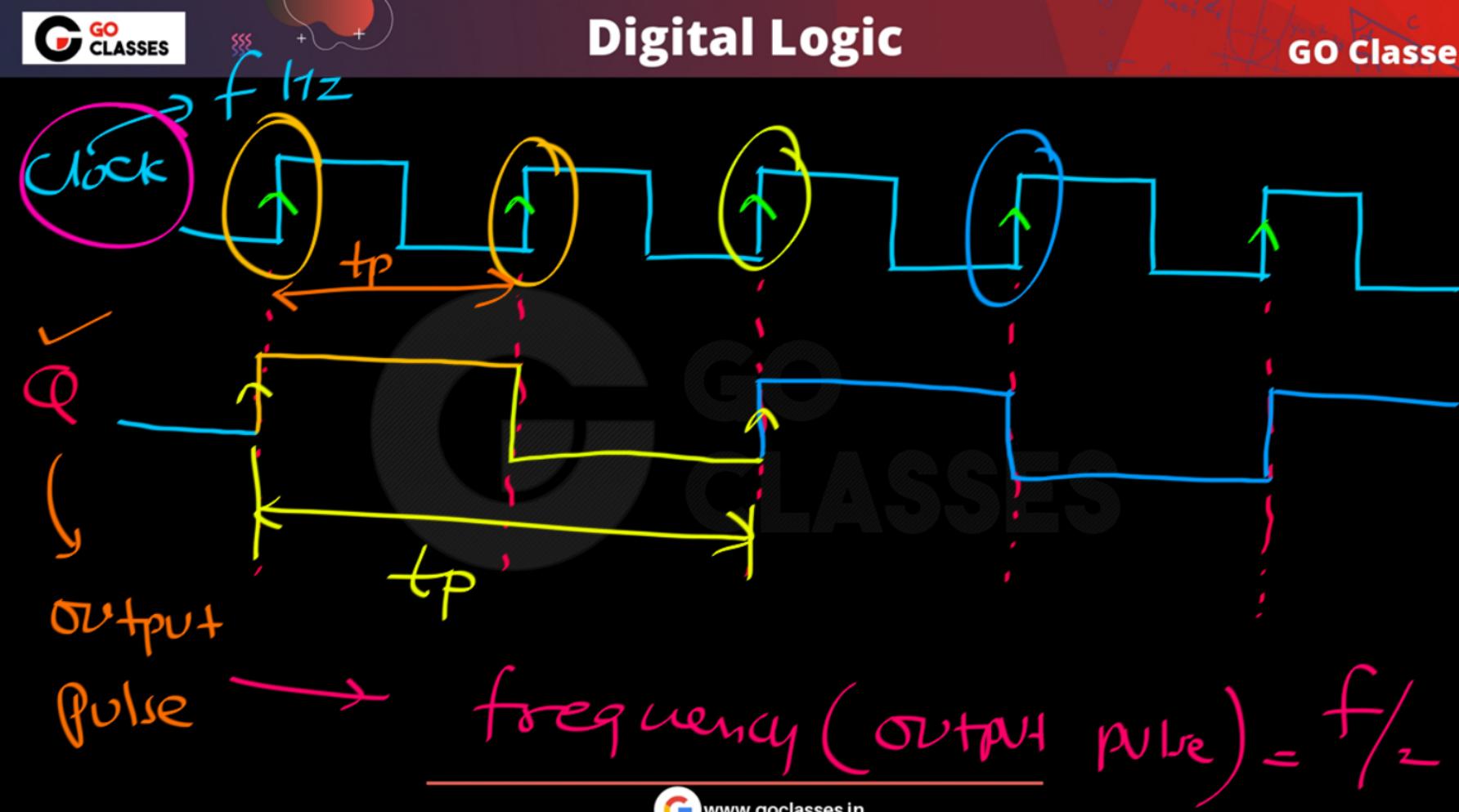
$$f = \frac{1}{t_p}$$





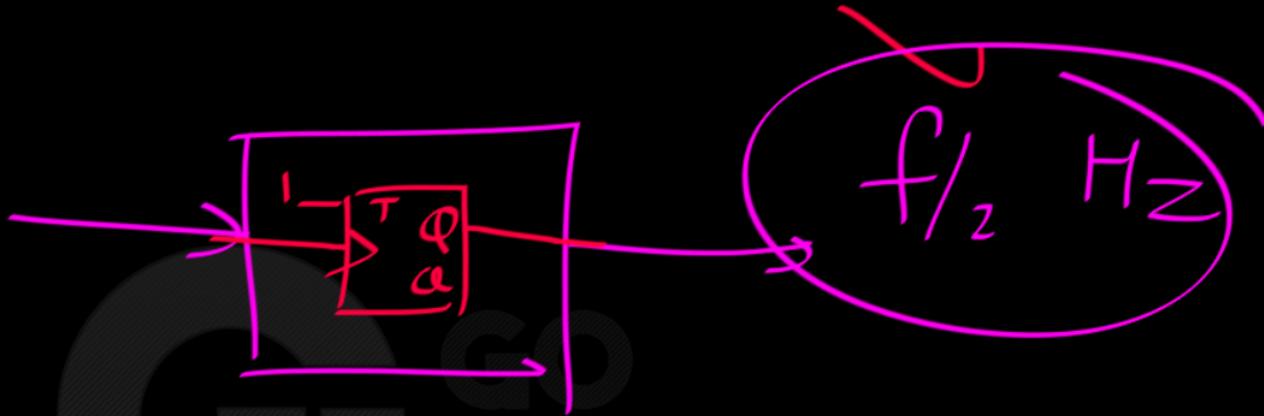
f_{Hz} ✓







f_{Hz}



T-ff

by 2.

Divides the Clock frequency



Duty cycle :

$$\frac{\text{On period}}{t_p} = \frac{4}{6} = \frac{2}{3}$$

$$t_p = 6 \text{ ns}$$

$$= \frac{2}{3} \times 100 \% \\ = 66.66 \%$$



Perfect square wave:

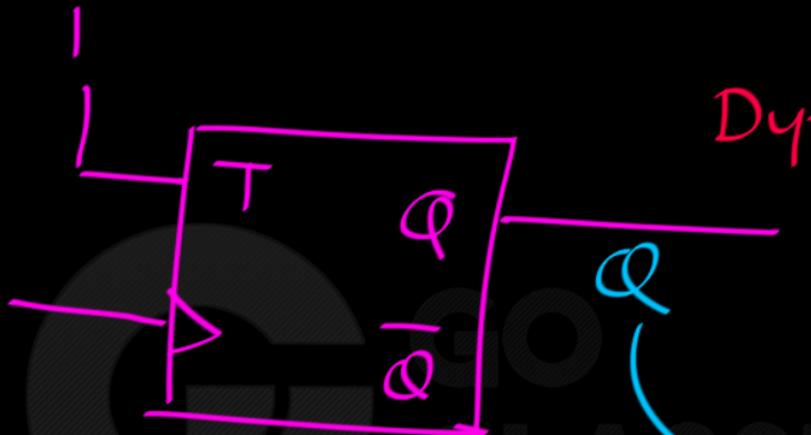
Duty cycle = 50%
on-period = off-period





Clock
↓
Duty Cycle

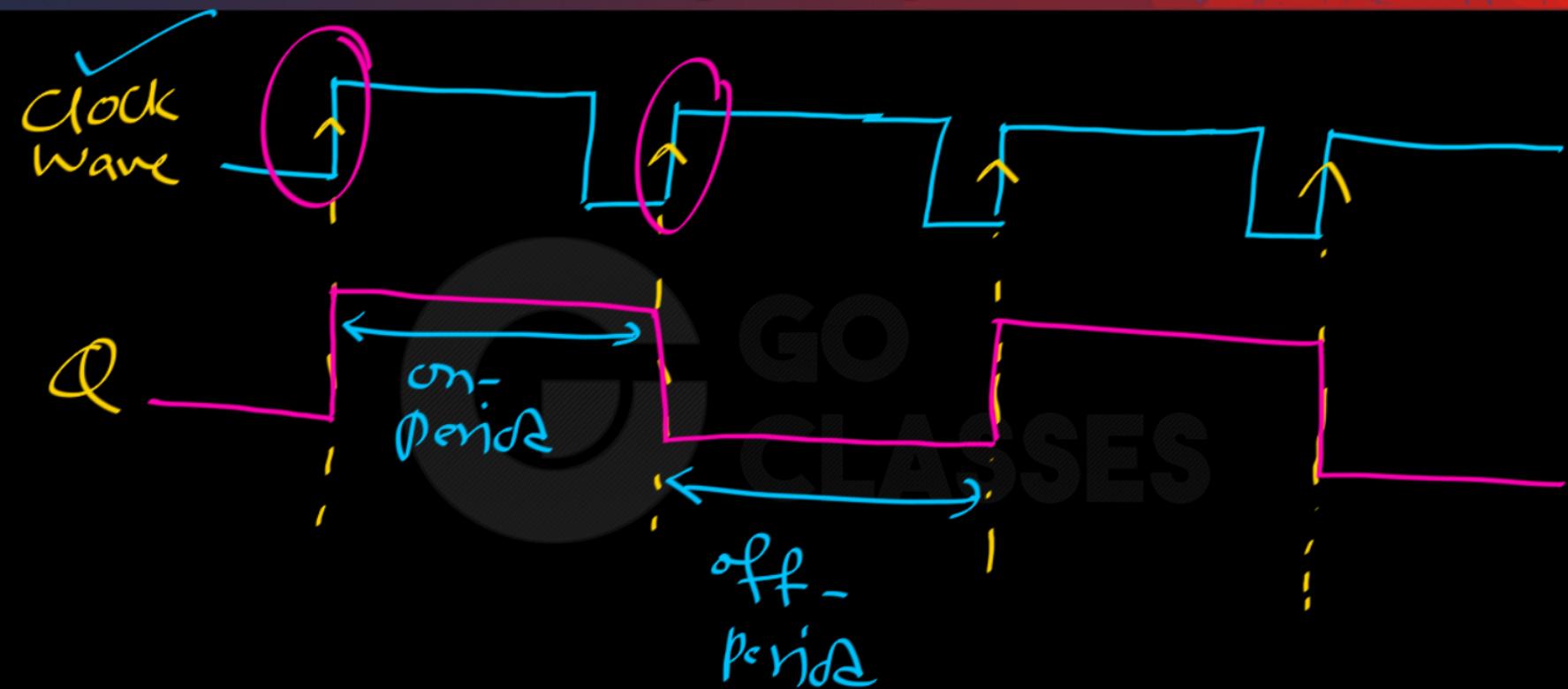
k %

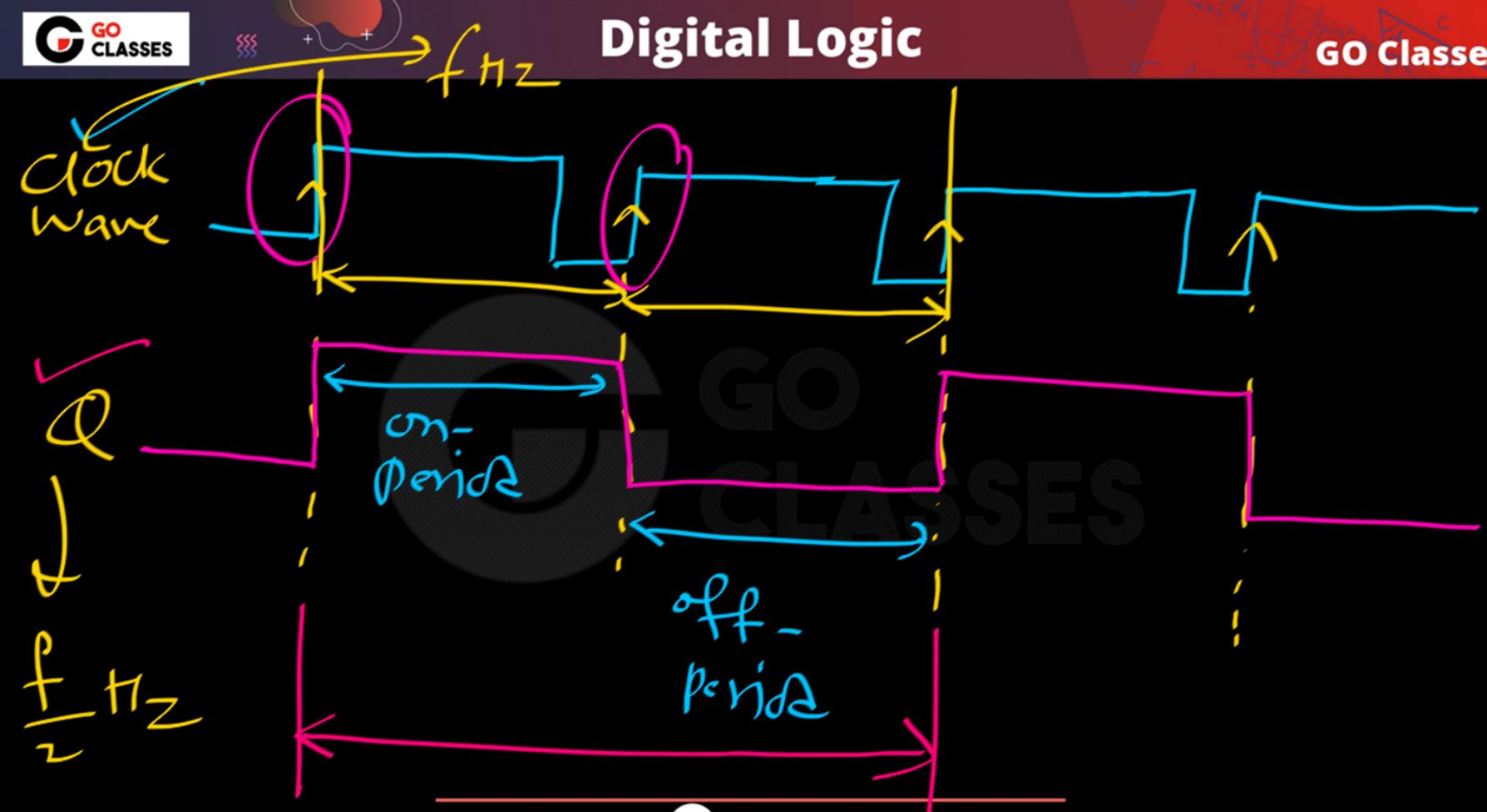


Duty Cycle

= 50%.

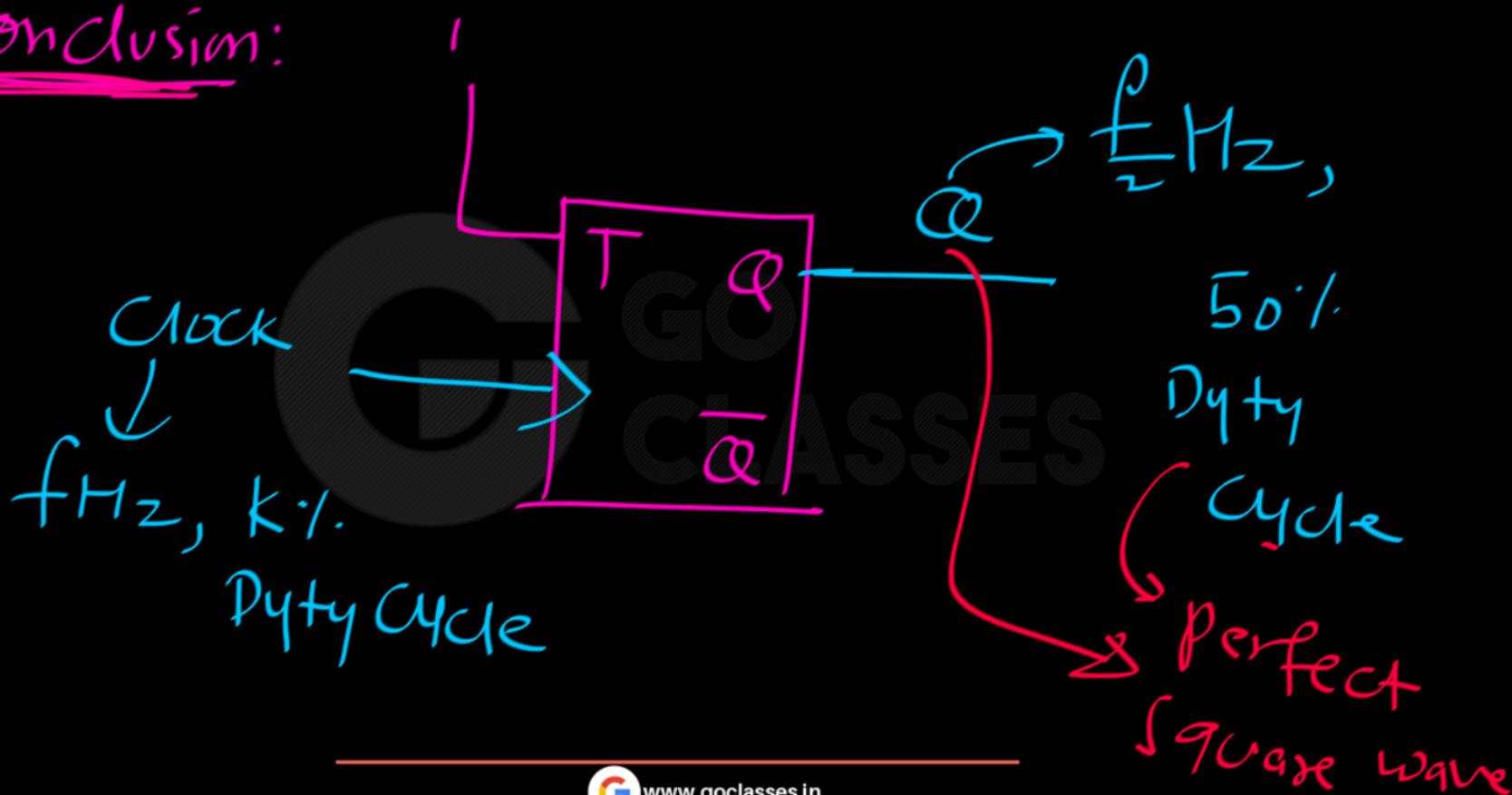
↓
Perfect
square
wave



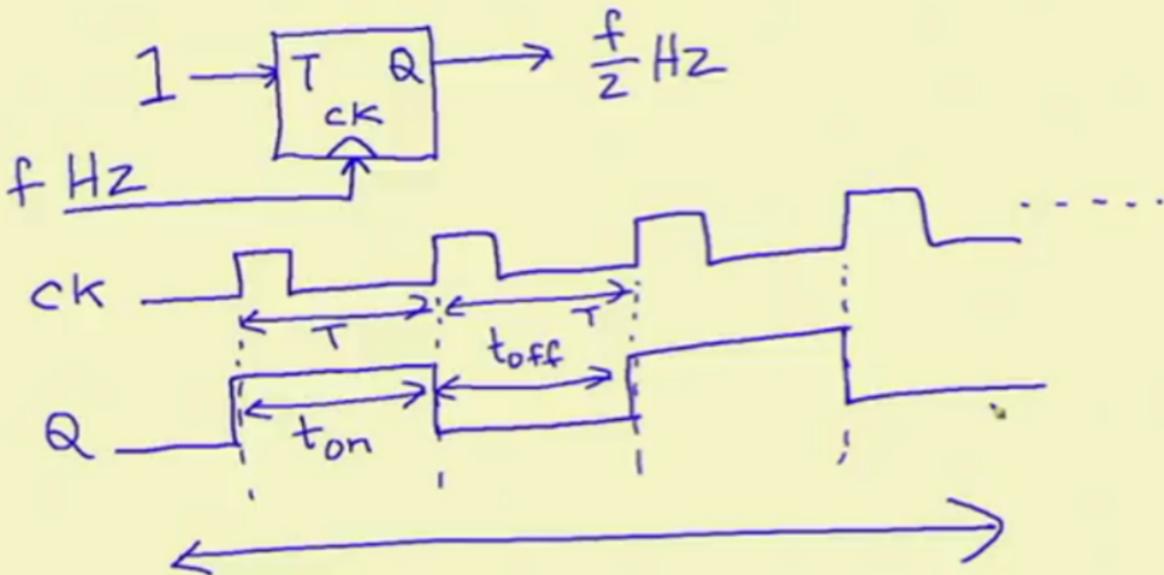




Conclusion:



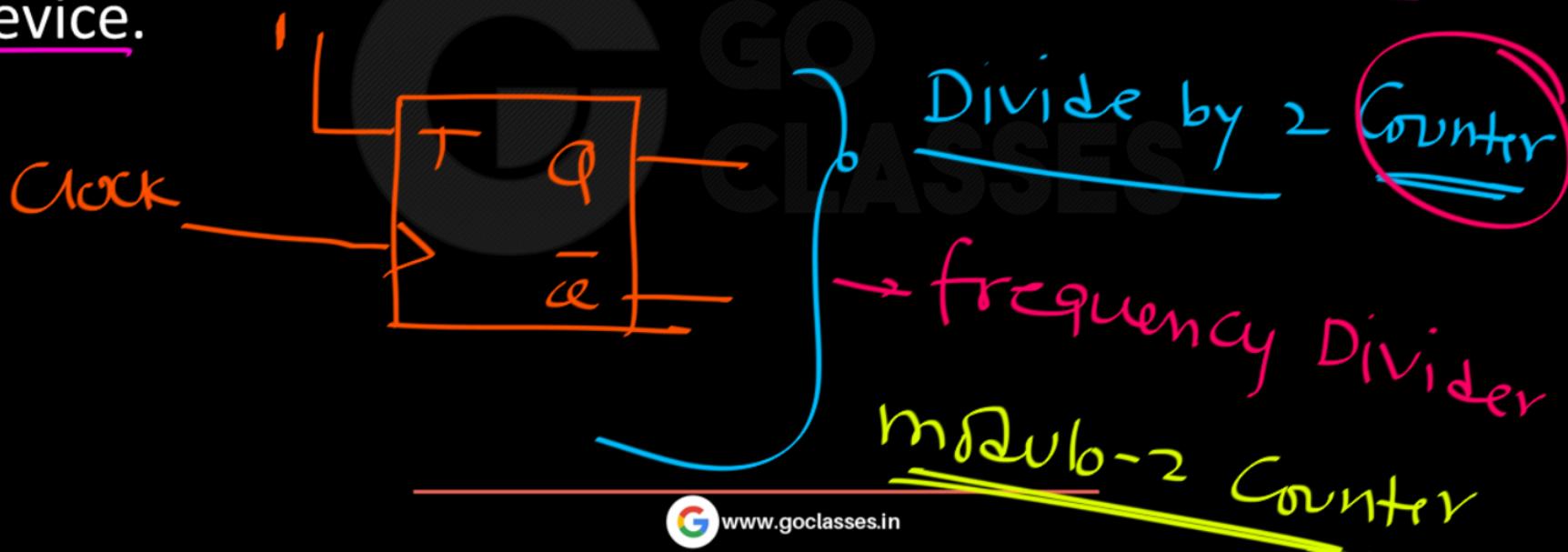
- Given a clock signal of frequency f Hz, how to generate another clock of frequency $f/2$ Hz.
 - Frequency division.





NOTE :

The output of the T Flip-Flop divides the frequency of the clock by 2, Hence, T-flipflop is also called Divide by 2 device.



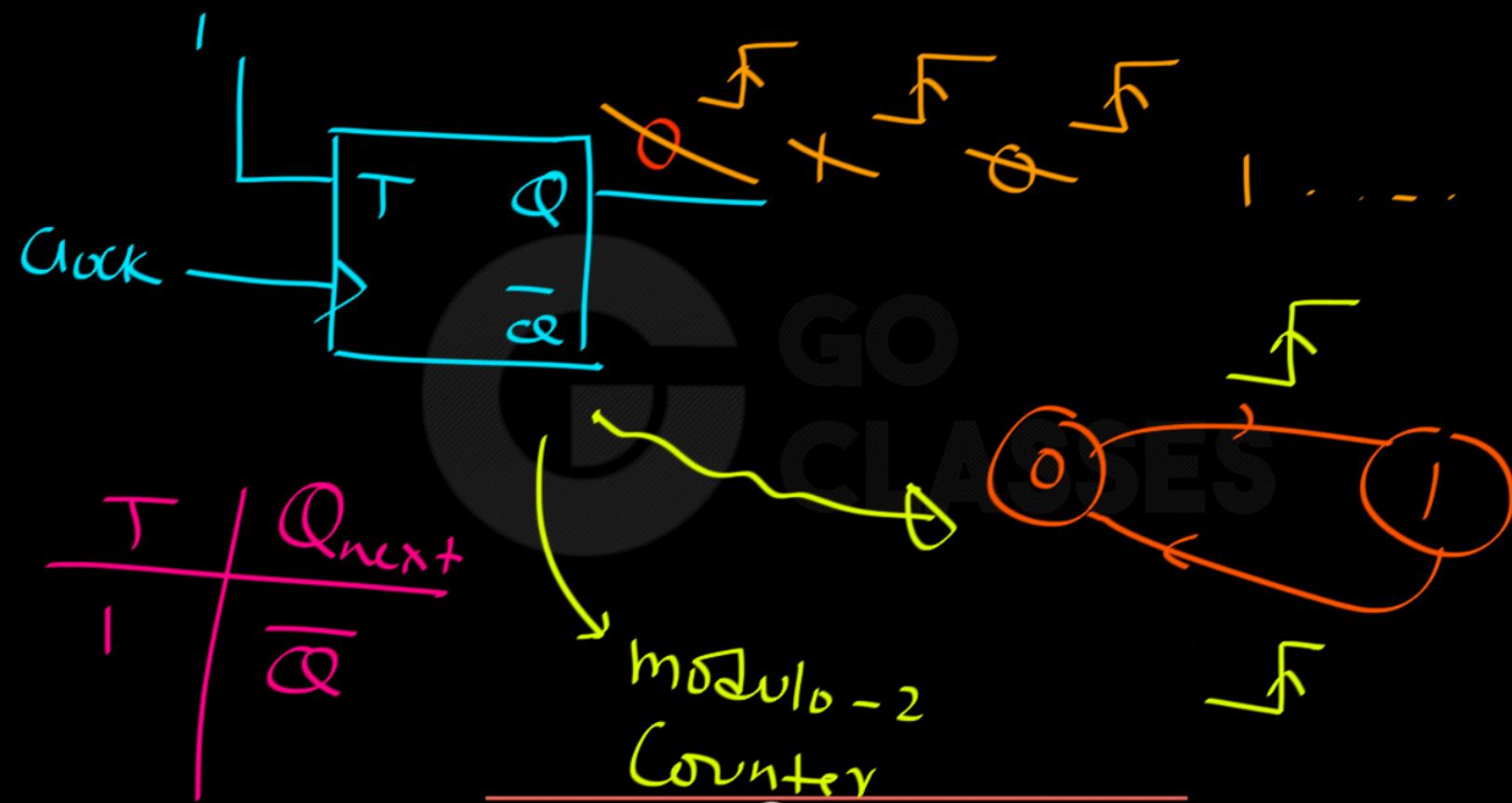


So, clearly there's some division going on. But how do we interpret this as counting?

Counter:
↓

Counts
Something

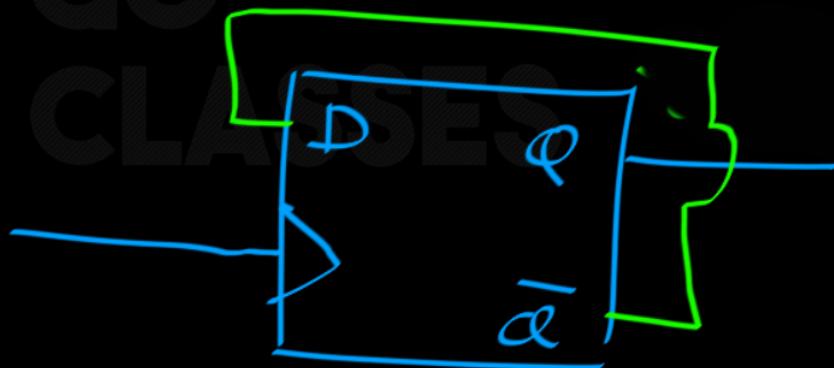


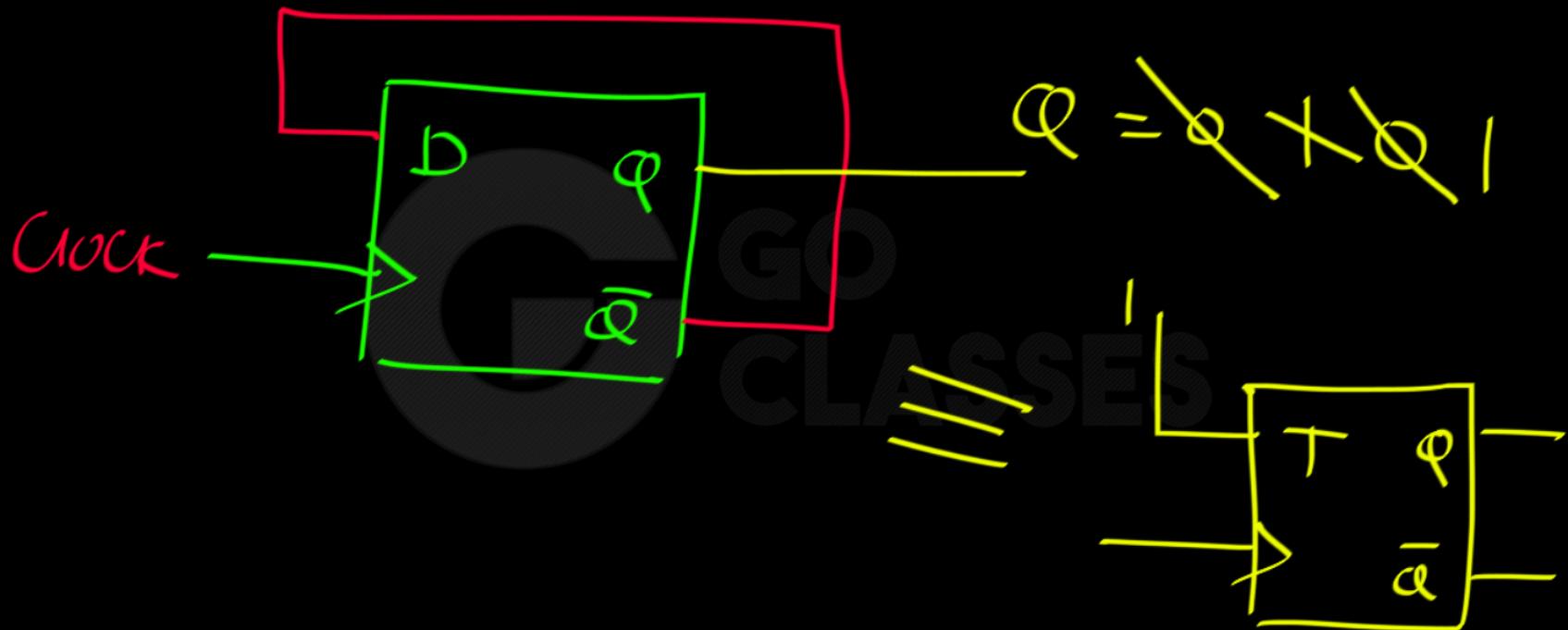




Q: Can we use D-ff to
Divide the Clock frequency
by 2?

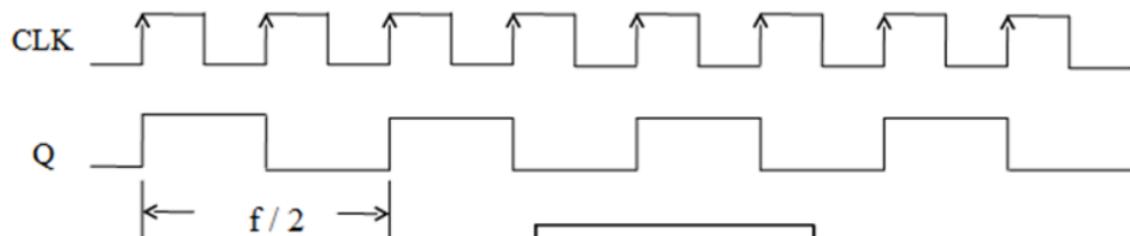
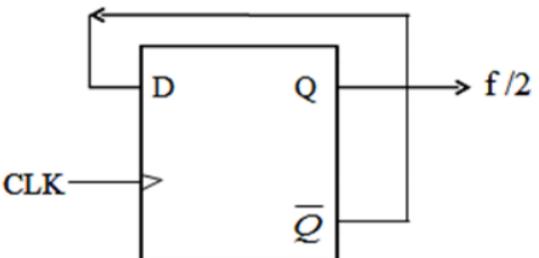
Yes.



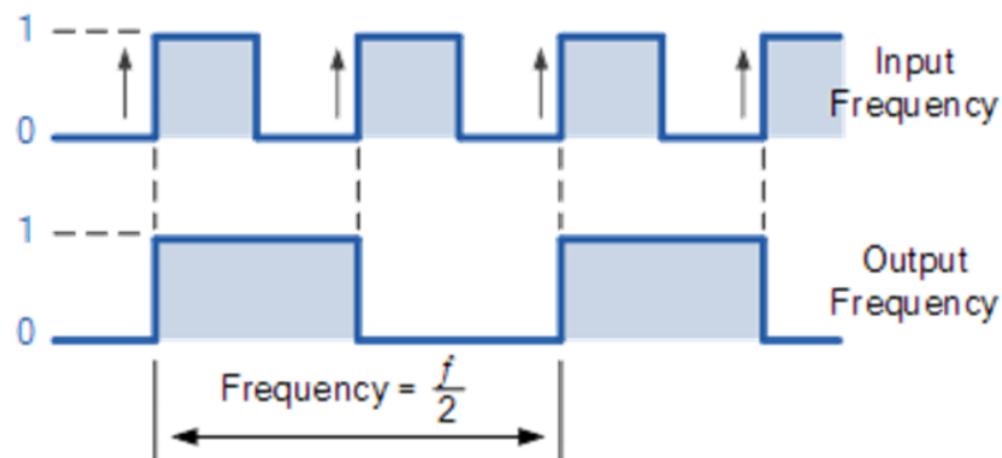
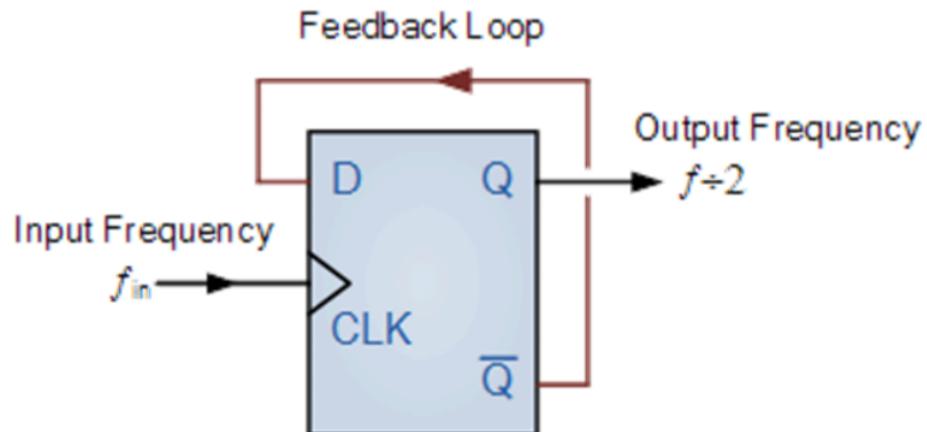


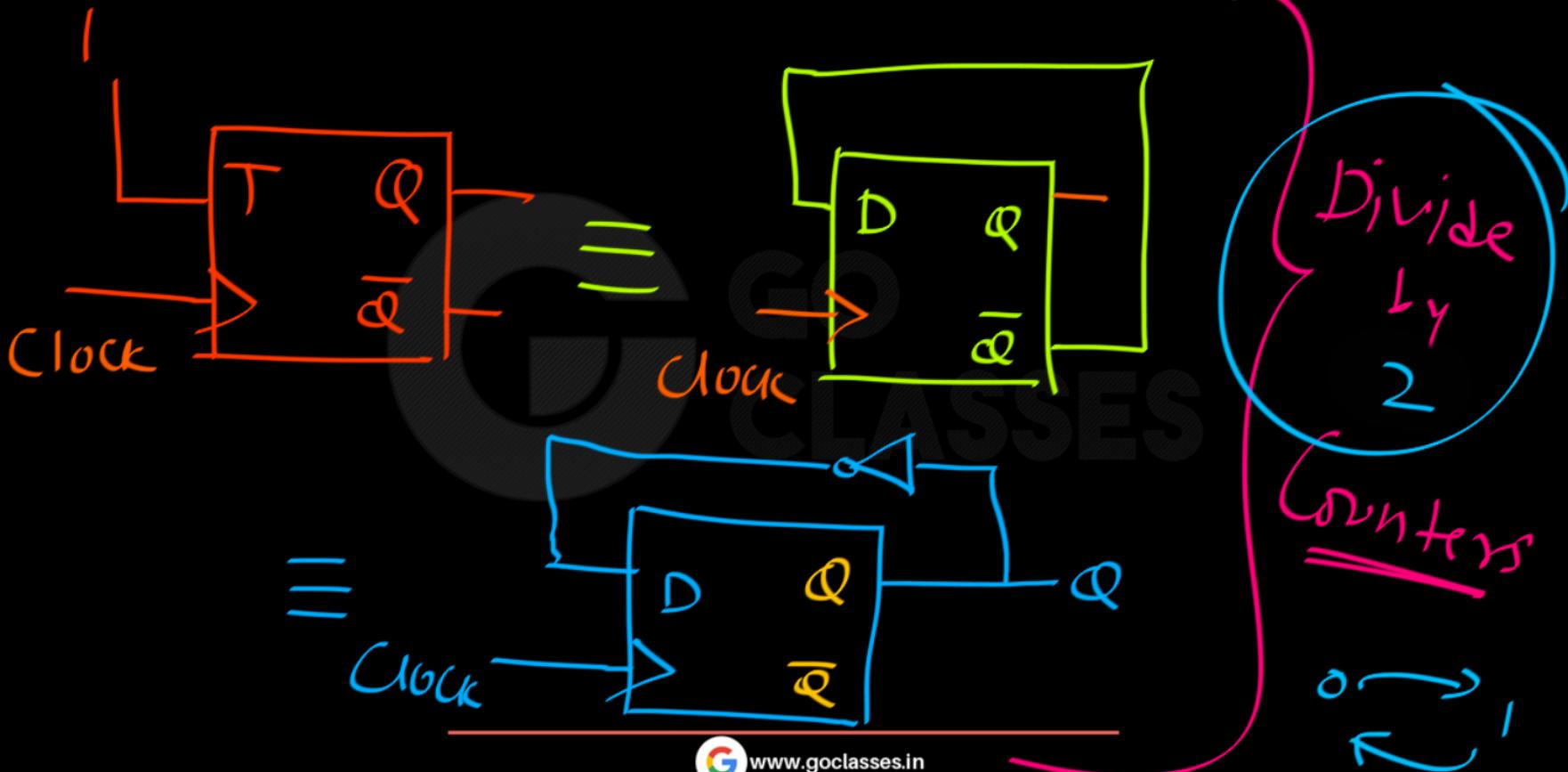


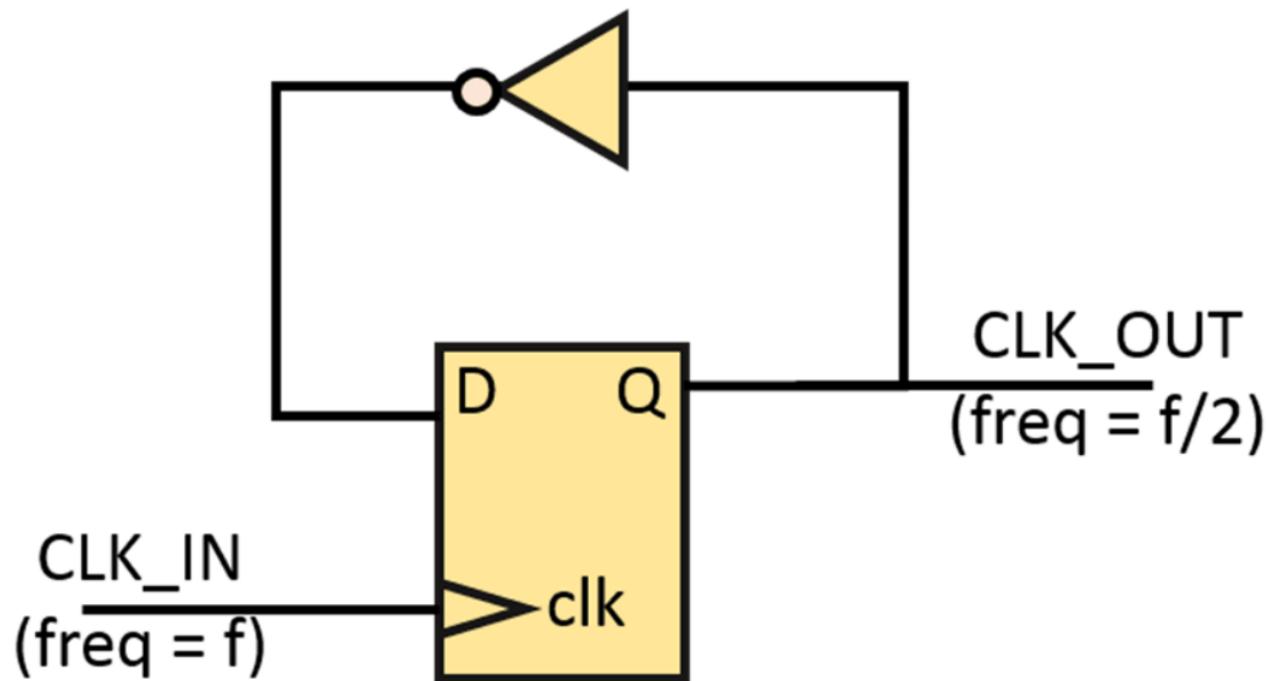
Frequency Divide by 2 ($f/2$)



Duty cycle of 50%
(ON- 1, OFF- 1)





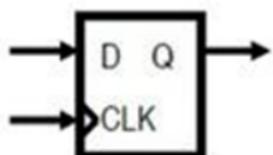




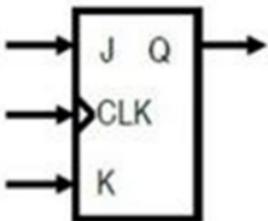
Build a frequency divider, divide-by-2 and divide-by-4 circuits using

1. D Flip Flops
2. JK Flip Flops

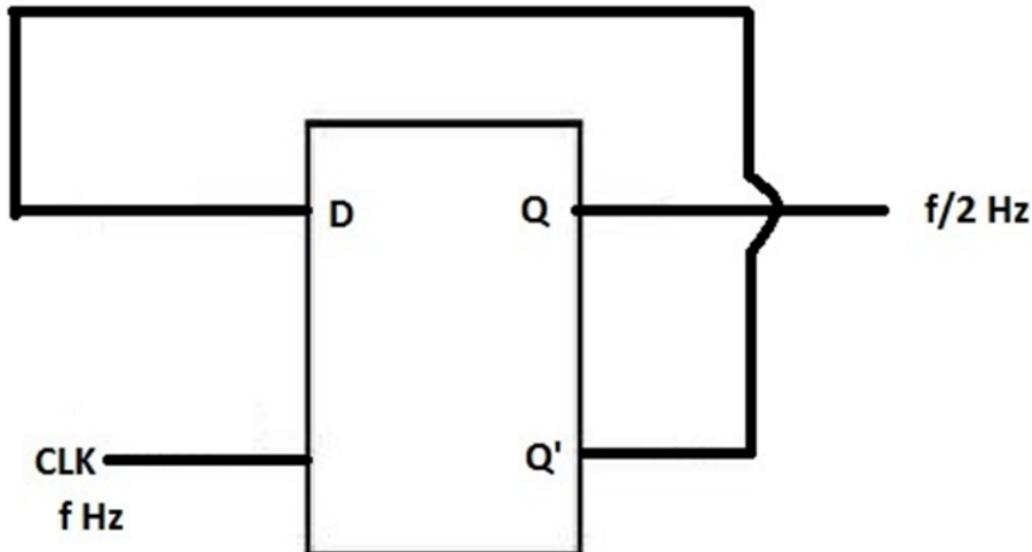
D Flip-Flop



JK Flip-Flop



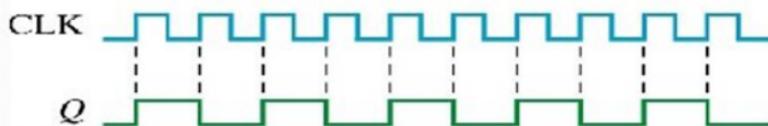
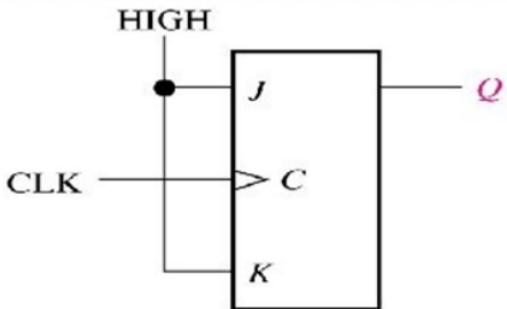
You will build four circuits in total. Draw the truth table and diagram of this design and observe the output waveform.

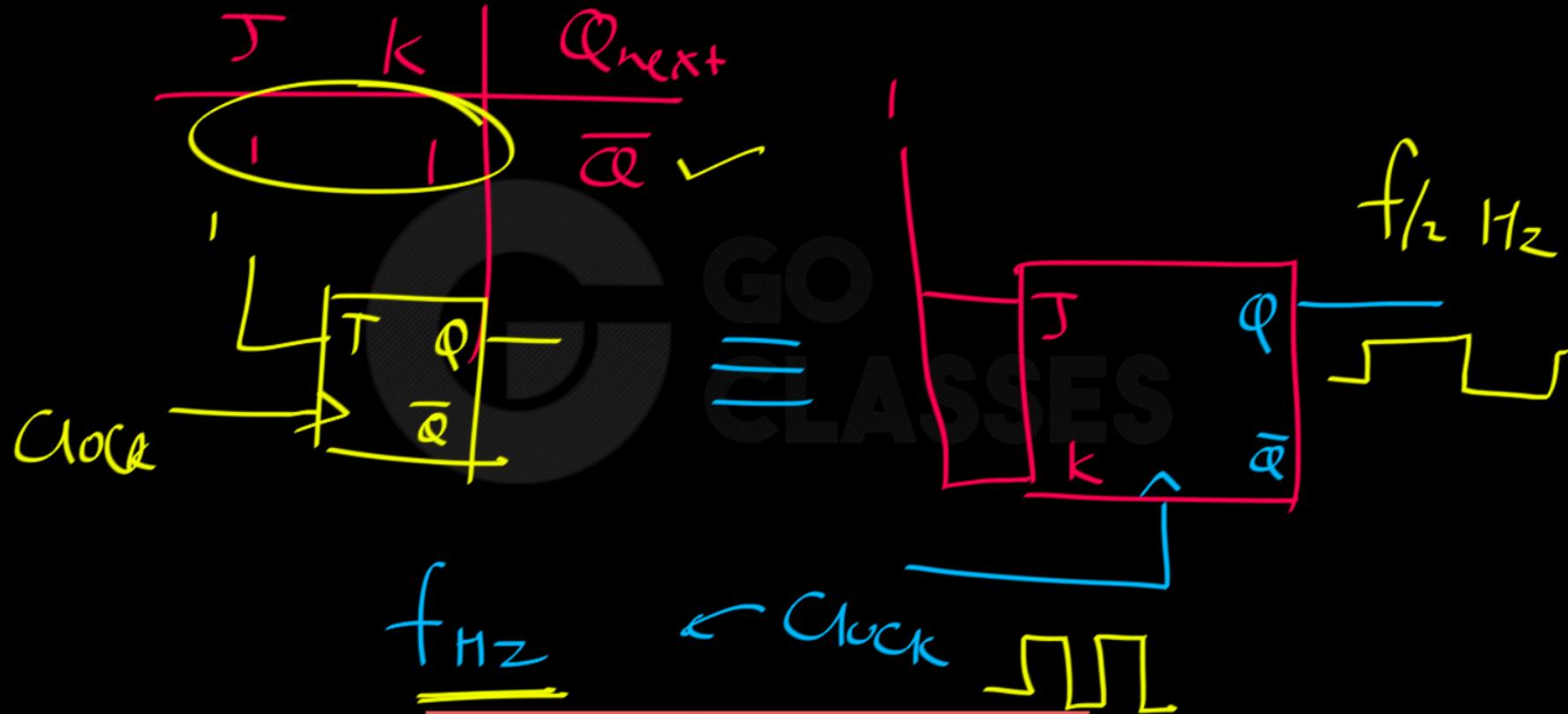


FREQUENCY DIVIDER USING D FLIP FLOP



J-K flip-flop as a divide-by-2 device. Q is one-half the frequency of CLK.







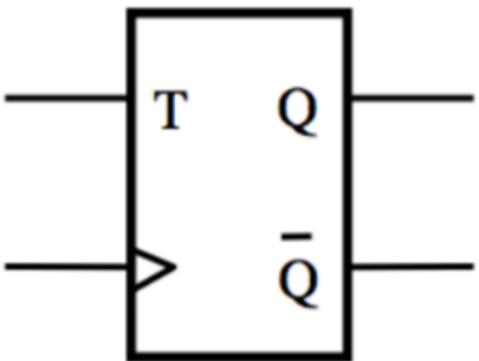
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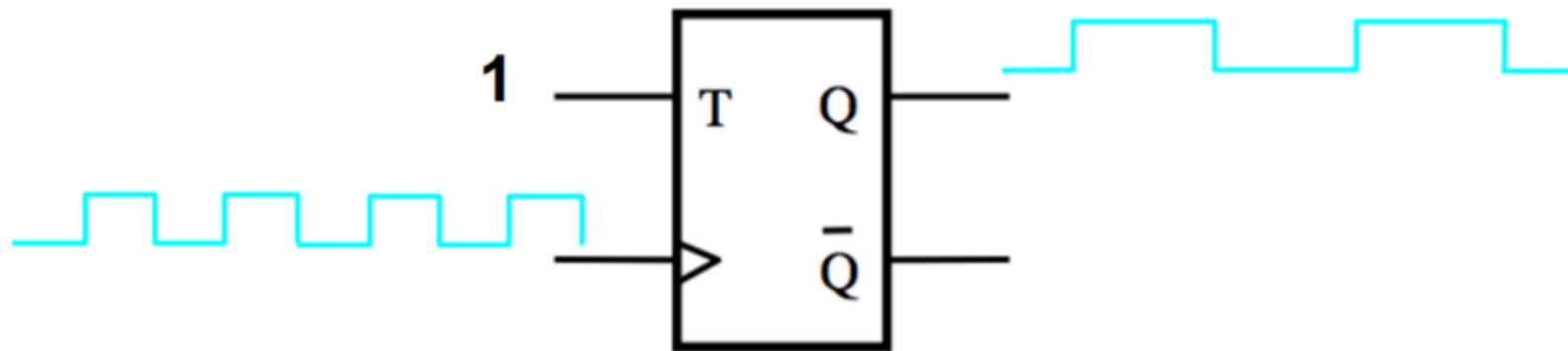


The output of the T Flip-Flop divides the frequency of the clock by 2





The output of the T Flip-Flop divides the frequency of the clock by 2





So, the previous circuit is :

Frequency Divider by 2 ✓

Modulo 2 Counter ✓

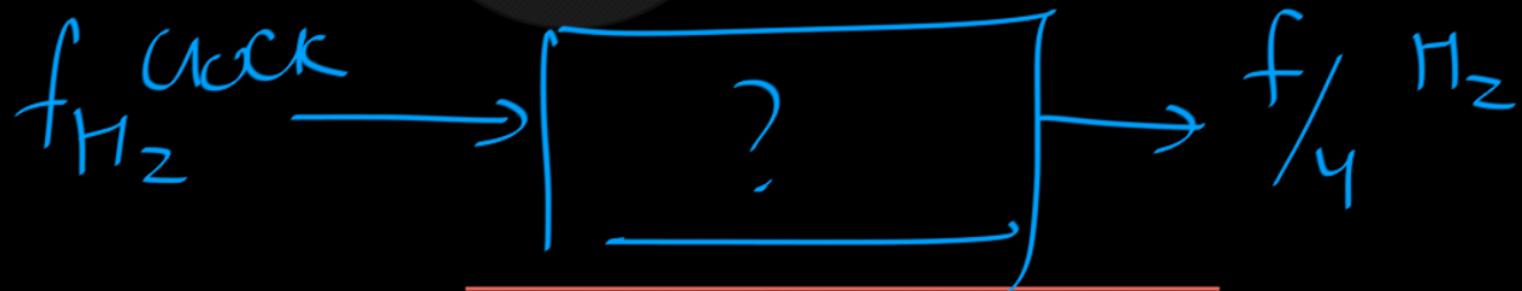
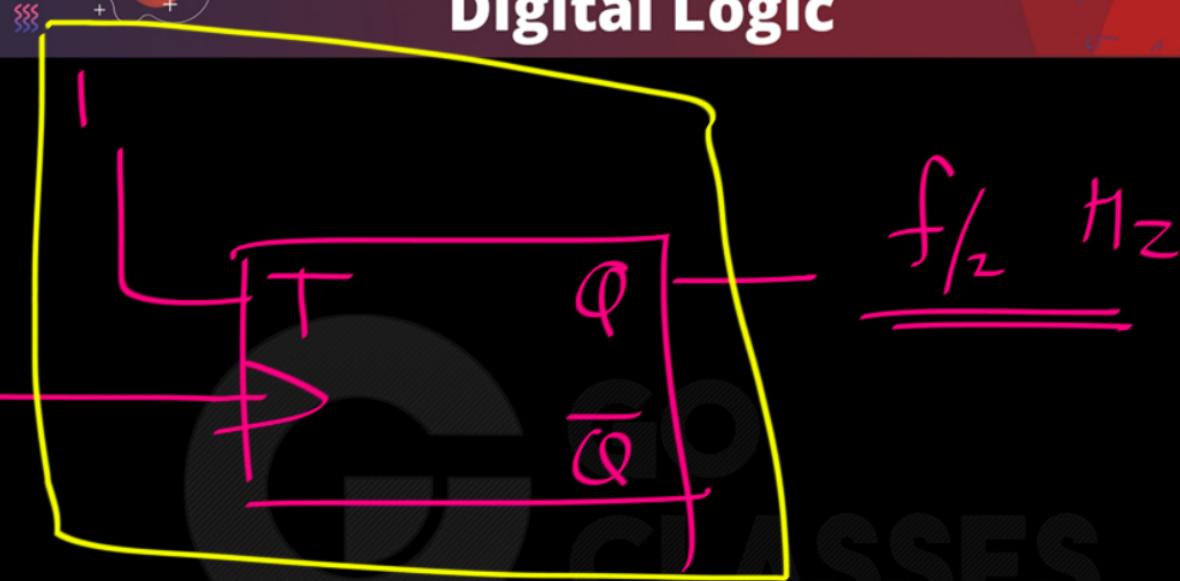
Divide-by-2 Counter ✓

Modulus of a counter is defined as the number of unique states that a counter will sequence through.

Counter: \rightarrow modulo-n Counter

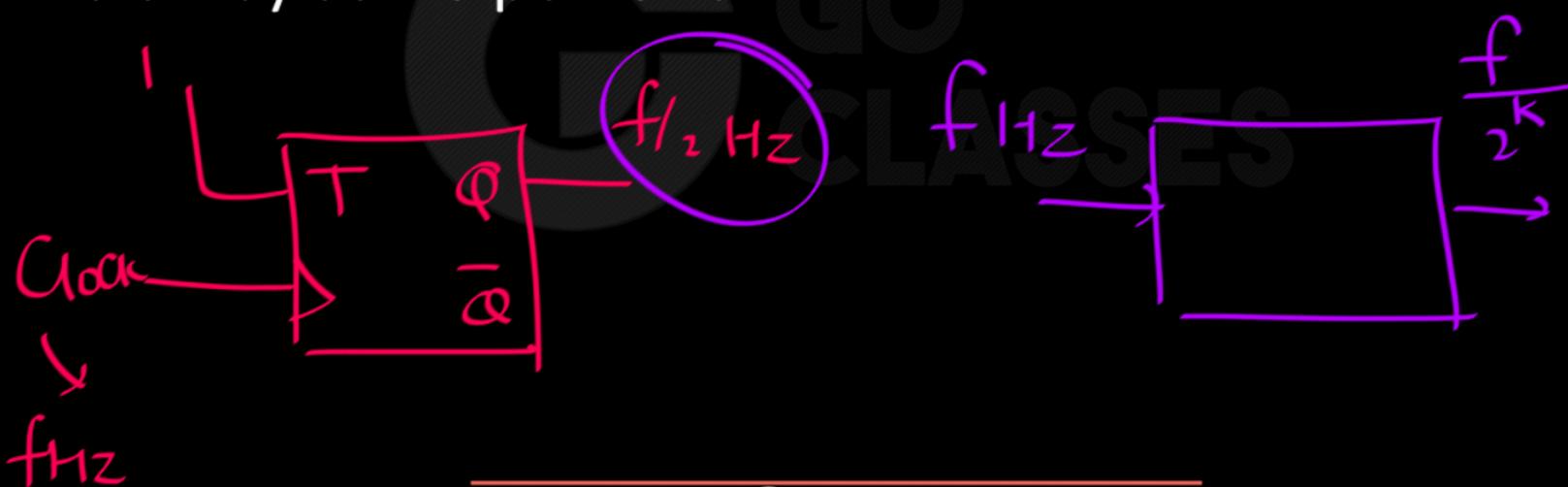


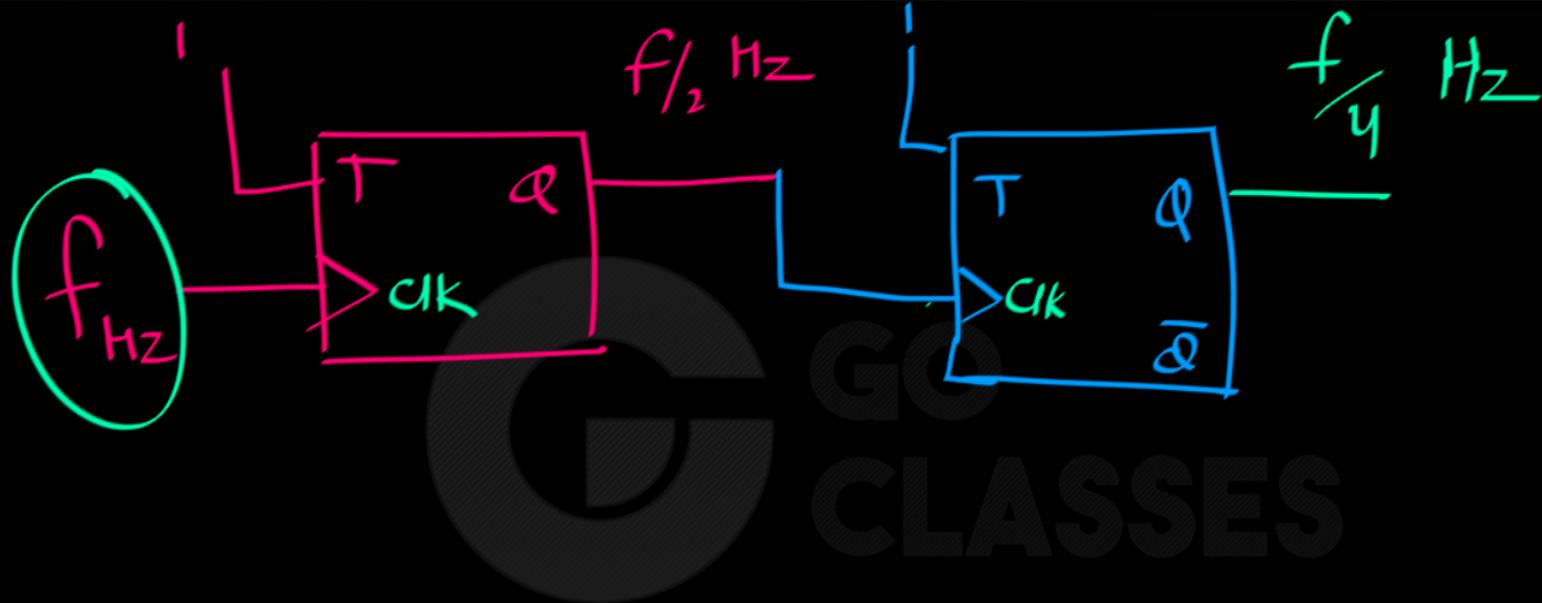
Clock
 f_{Hz}

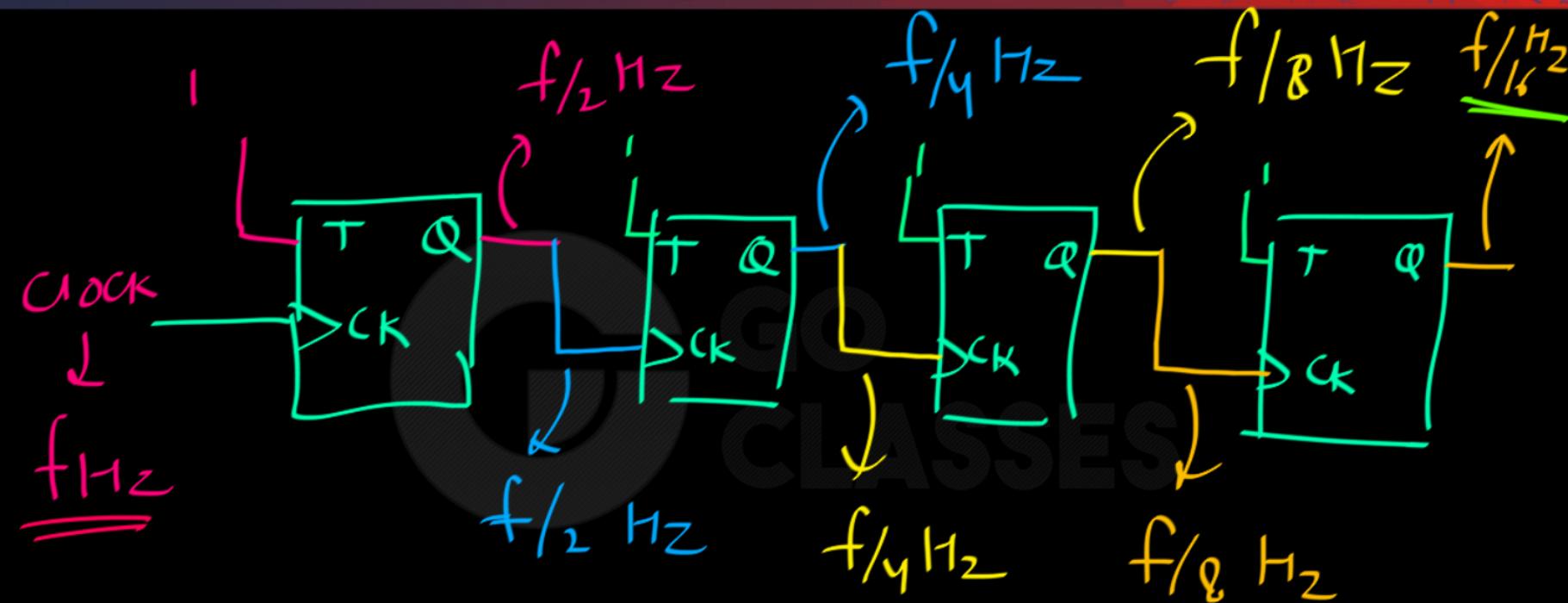


Q :

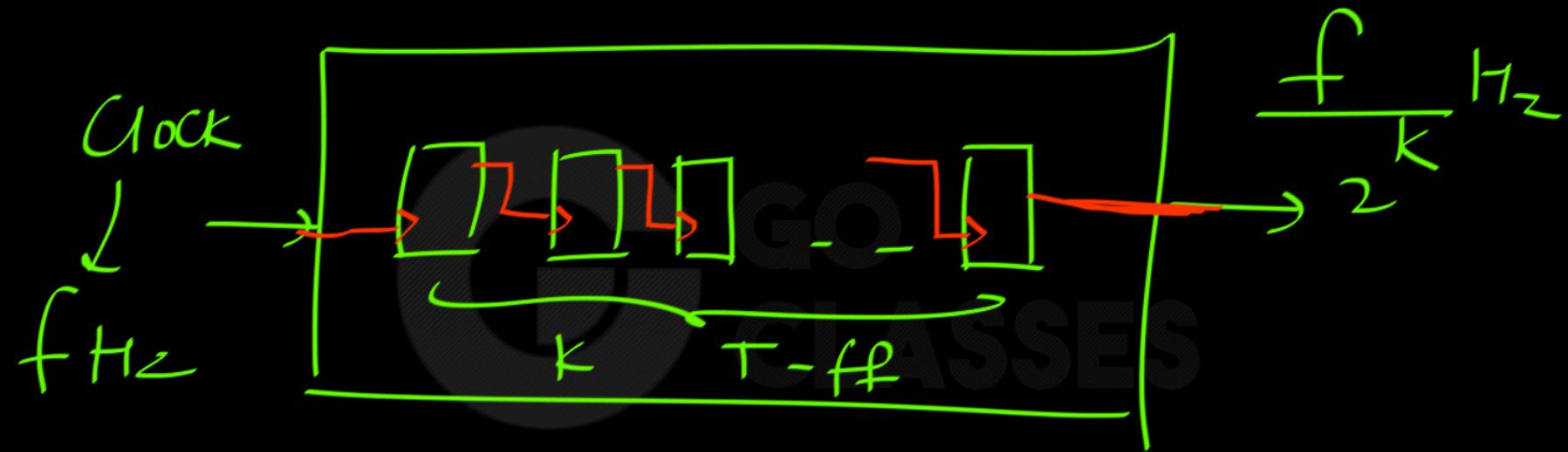
Given a clock signal of frequency f Hz, how to generate another clock of frequency $f/2^k$ Hz. i.e. Frequency division by some power of 2.

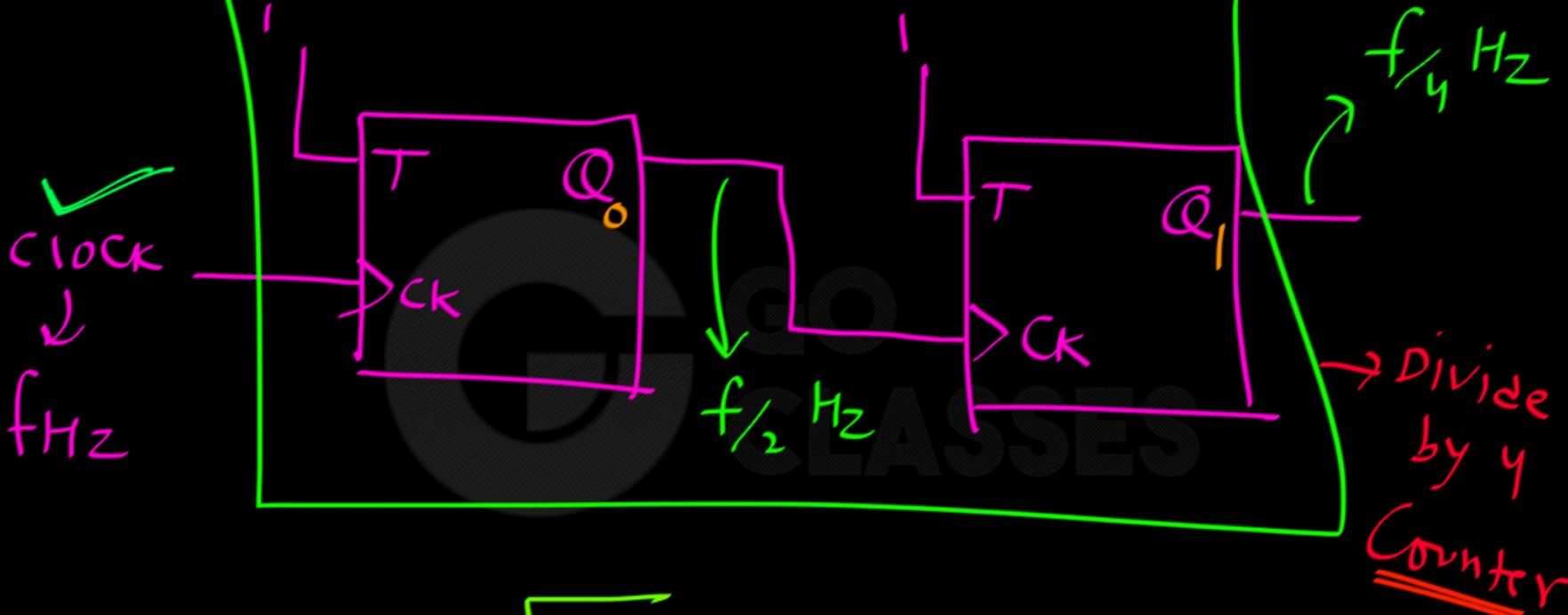




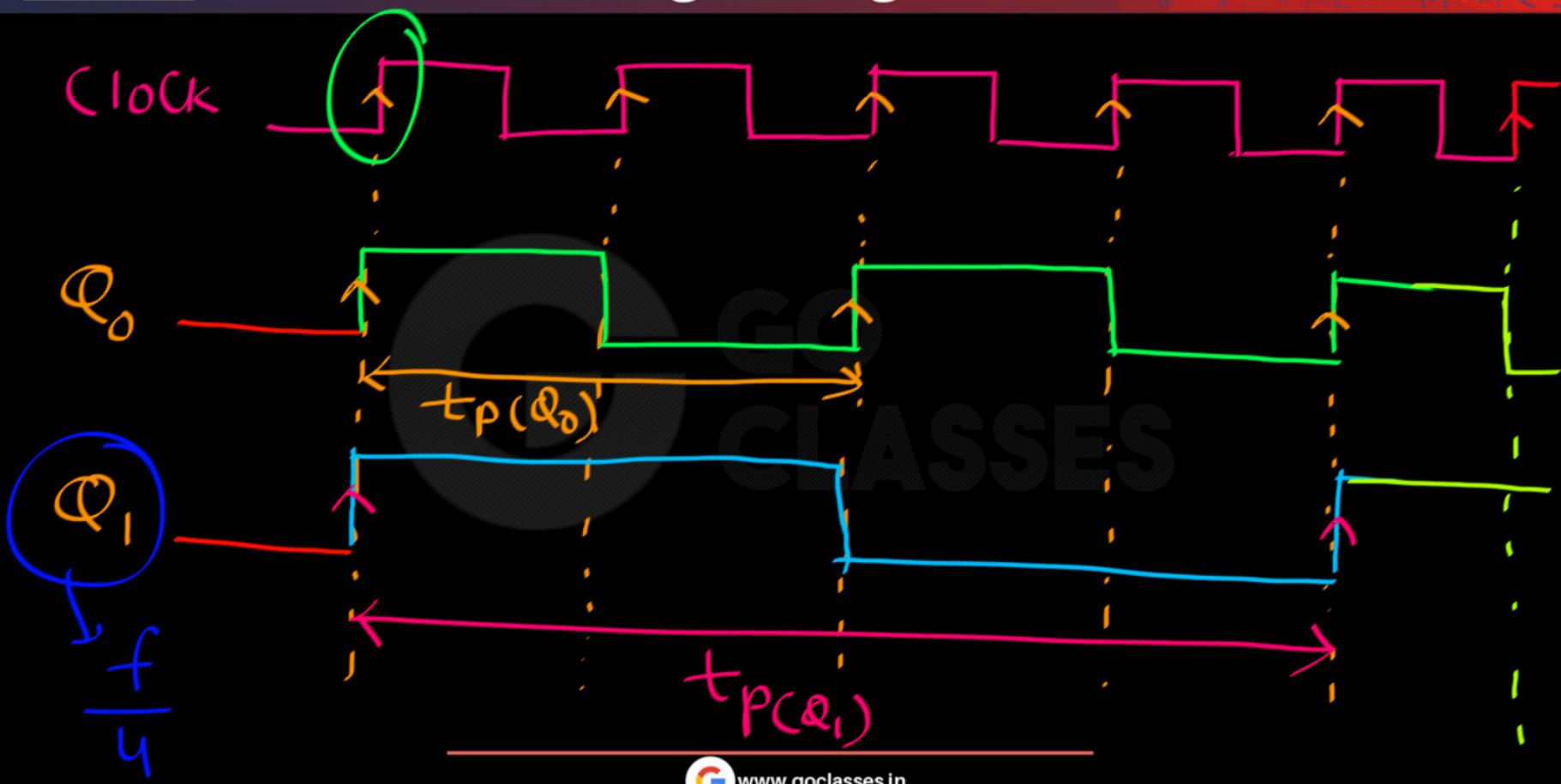


Async. Counter





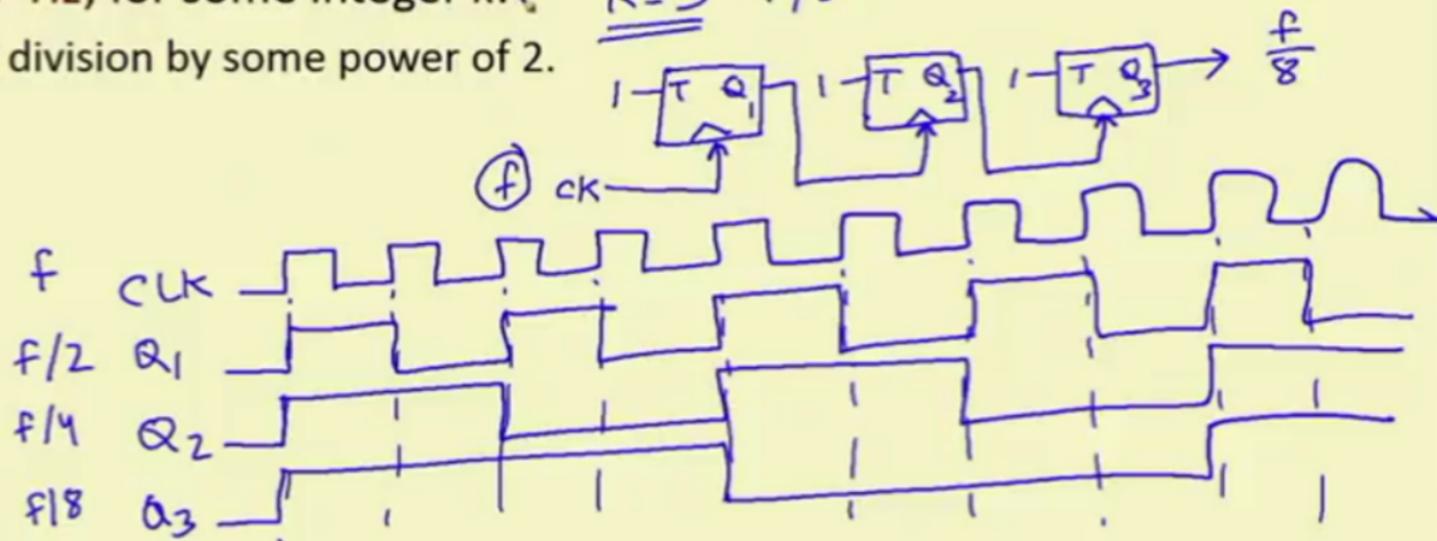
When $Q_0 \downarrow$ then Q_1 will toggle.





- Given a clock signal of frequency f Hz, how to generate another clock of frequency $f/2^k$ Hz, for some integer k .
 - Frequency division by some power of 2.

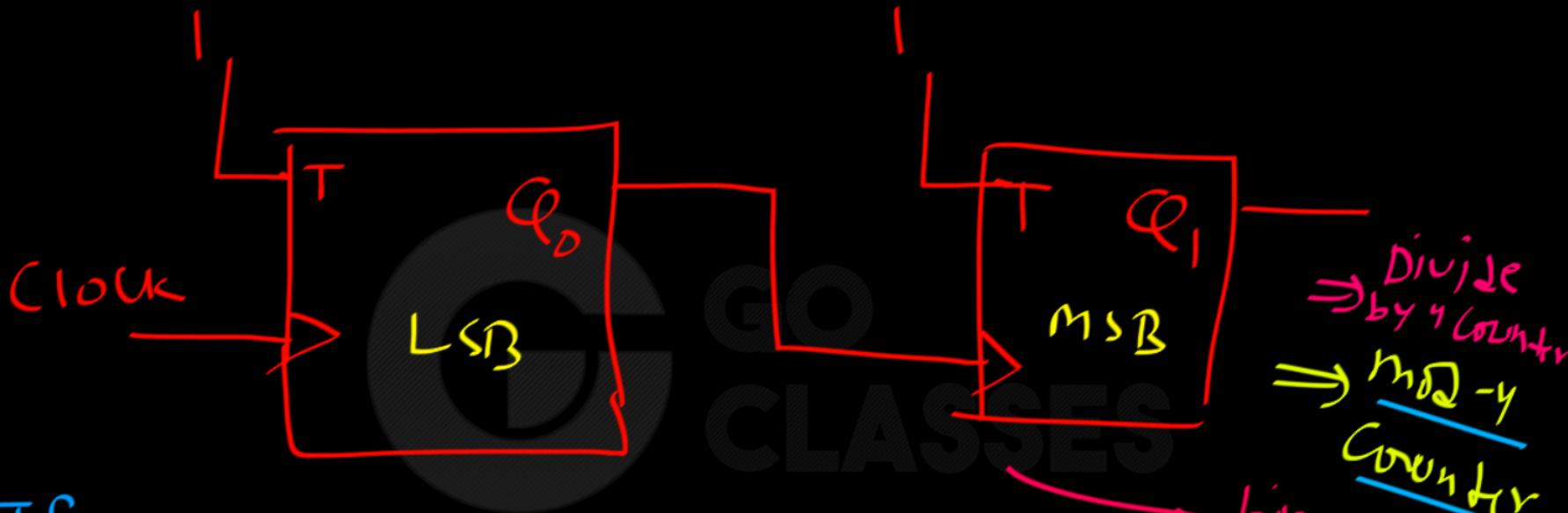
$$\underline{k=3} \quad f/8$$





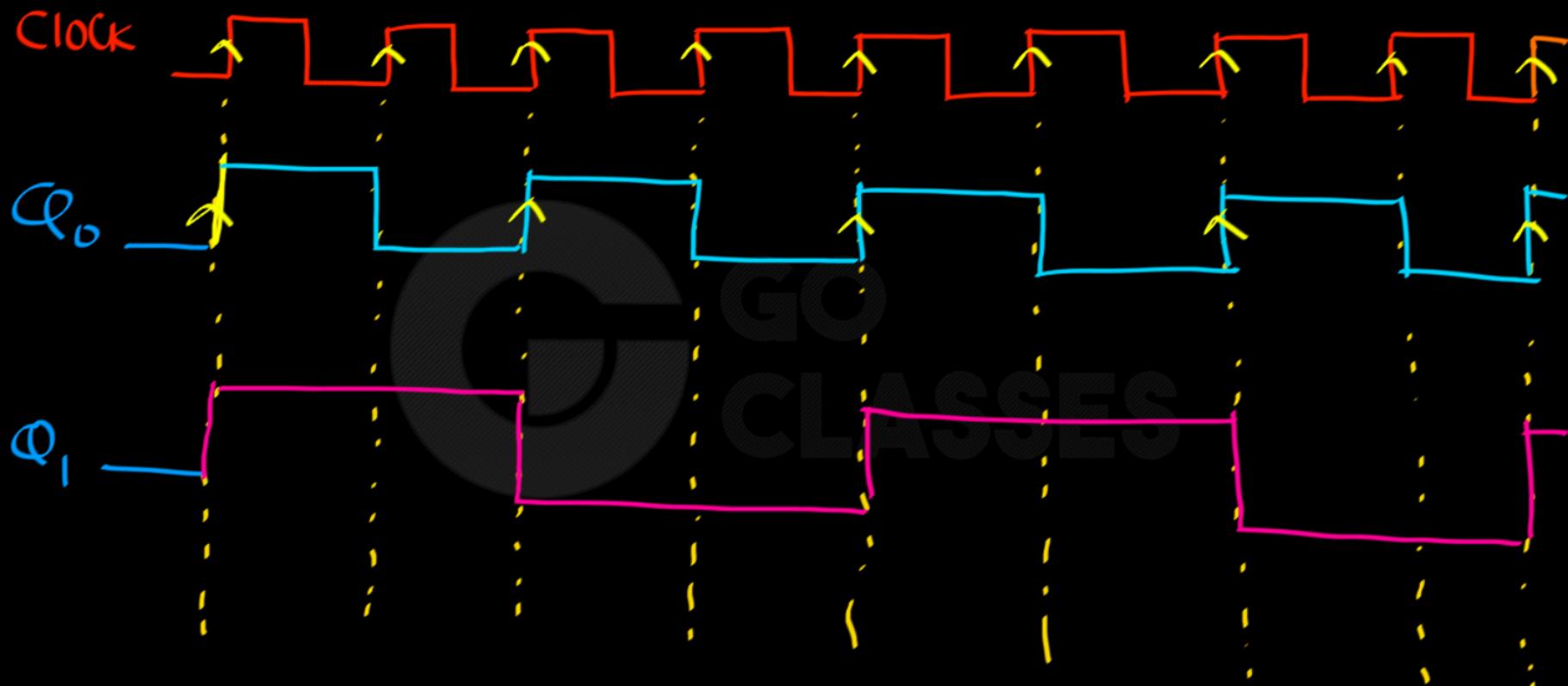
So, clearly there's some division going on. But how do we interpret this as counting?

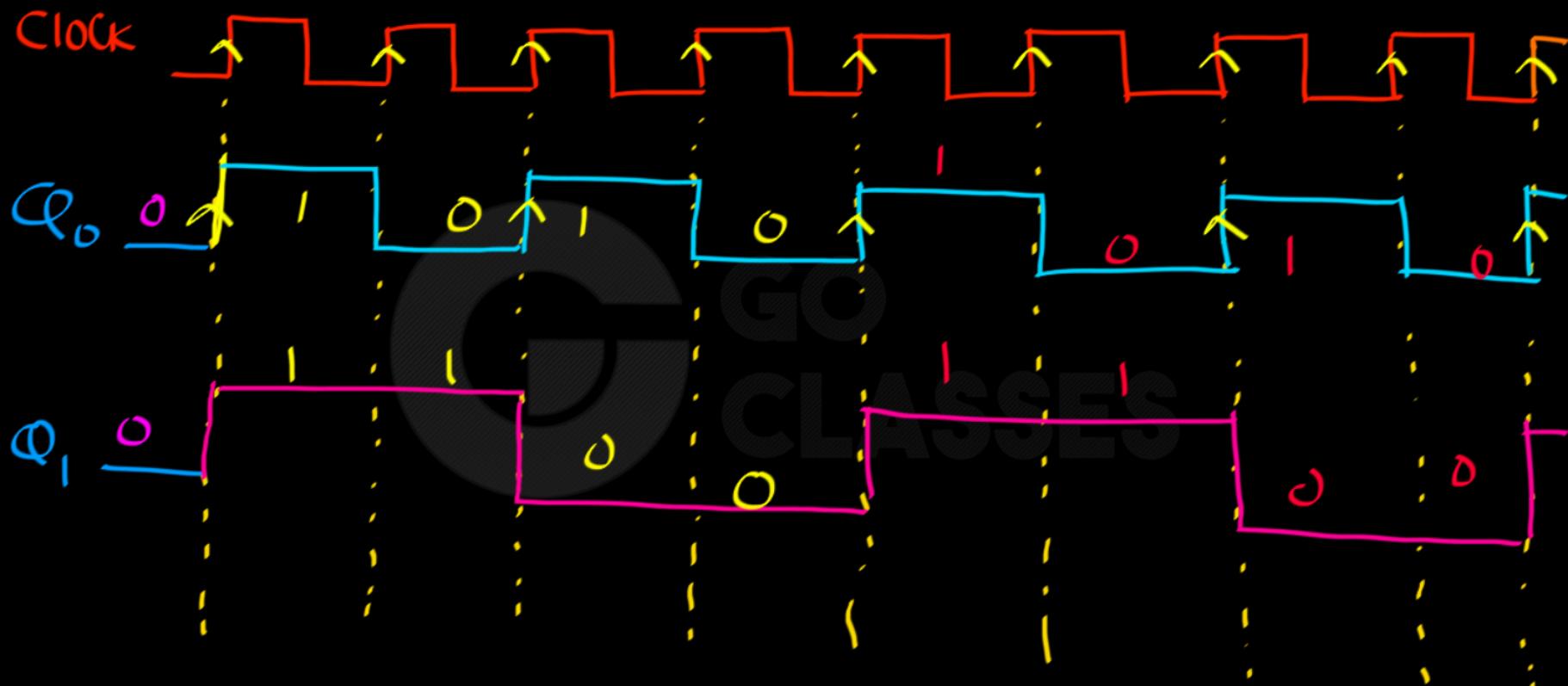


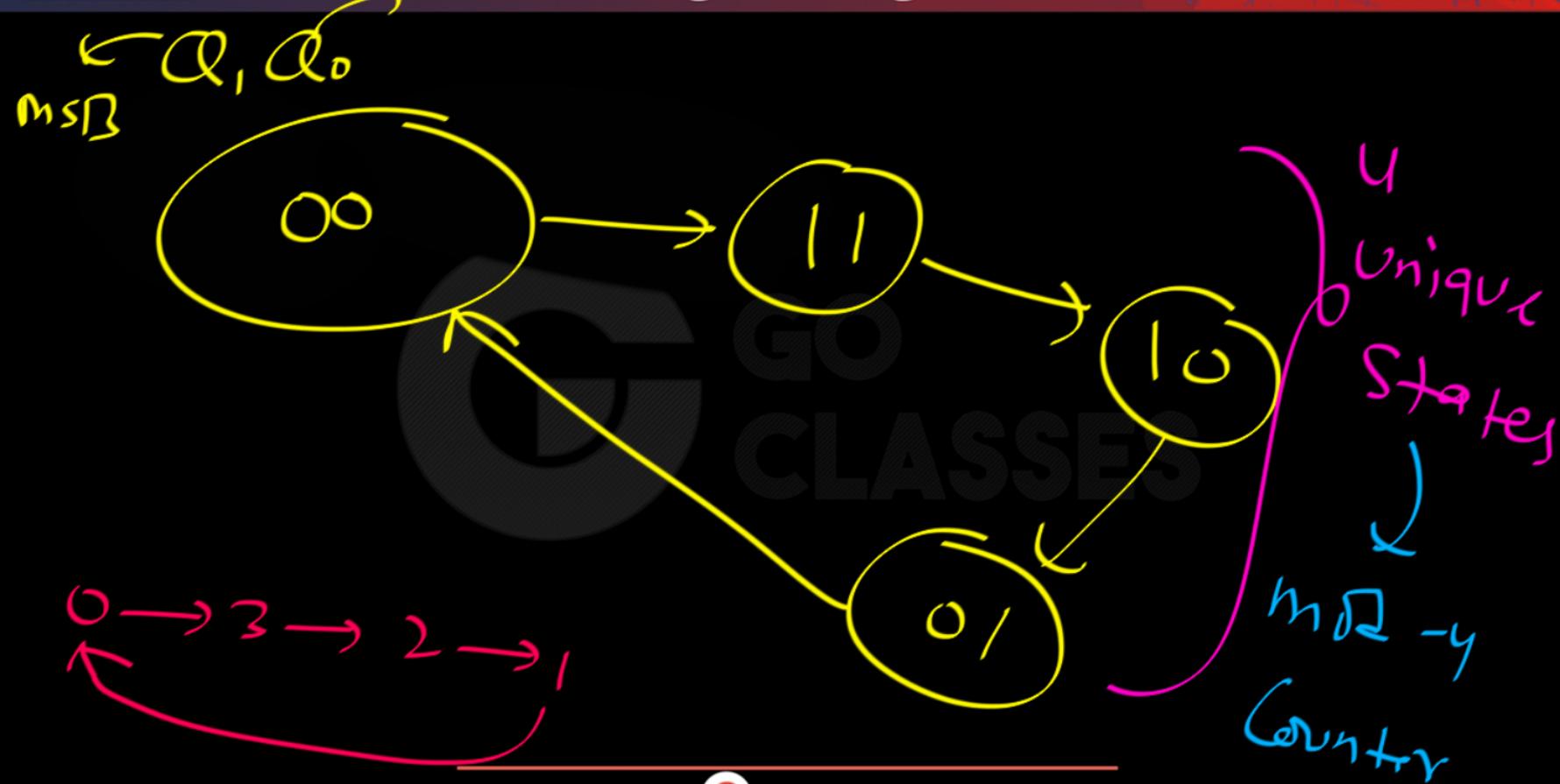


If
Clock \searrow then Q_0 will toggle.

If $Q_0 \searrow$ then Q_1 will toggle.



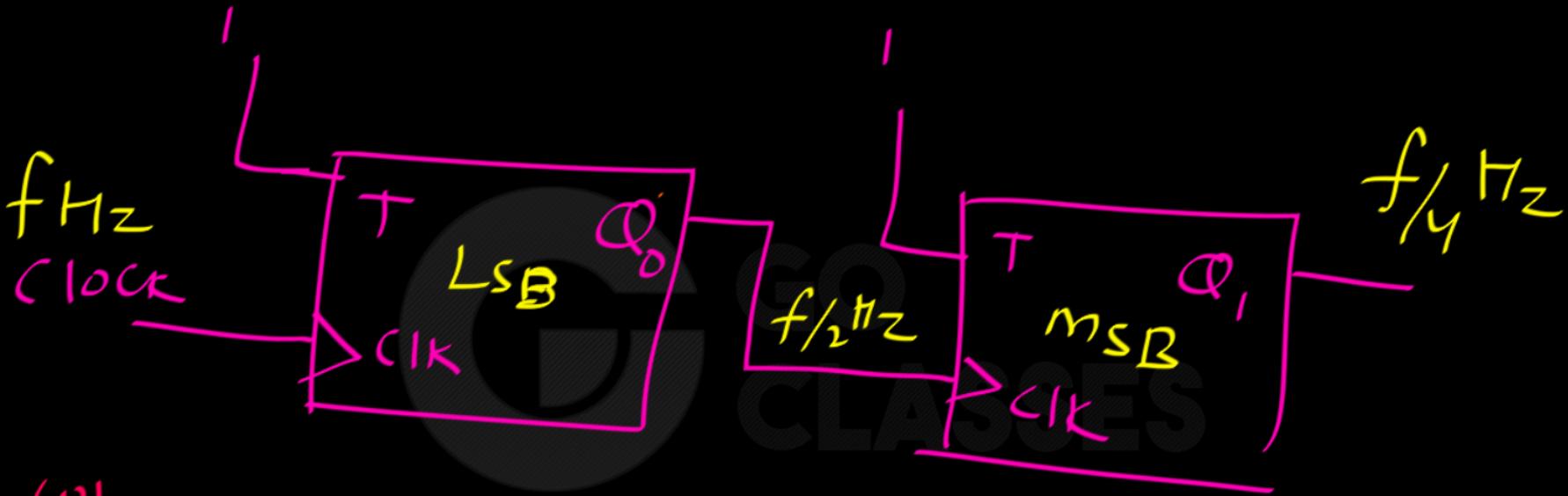






In real, every flipflop has some Propagation Delay.

Let's Assume our ff's have Propagation Delay t_{PD} .

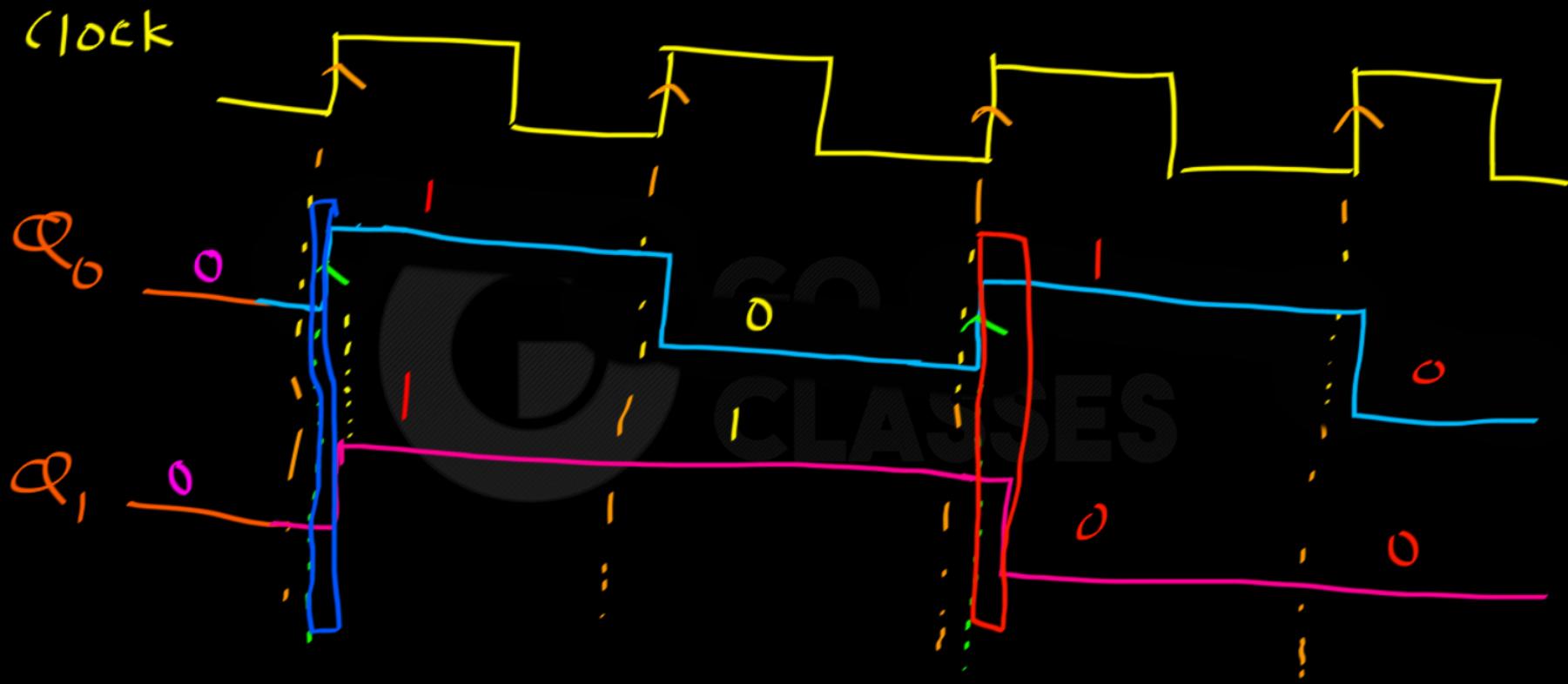


When clock \downarrow then Q_0 toggles.
When Q_0 \downarrow then Q_1 toggles.



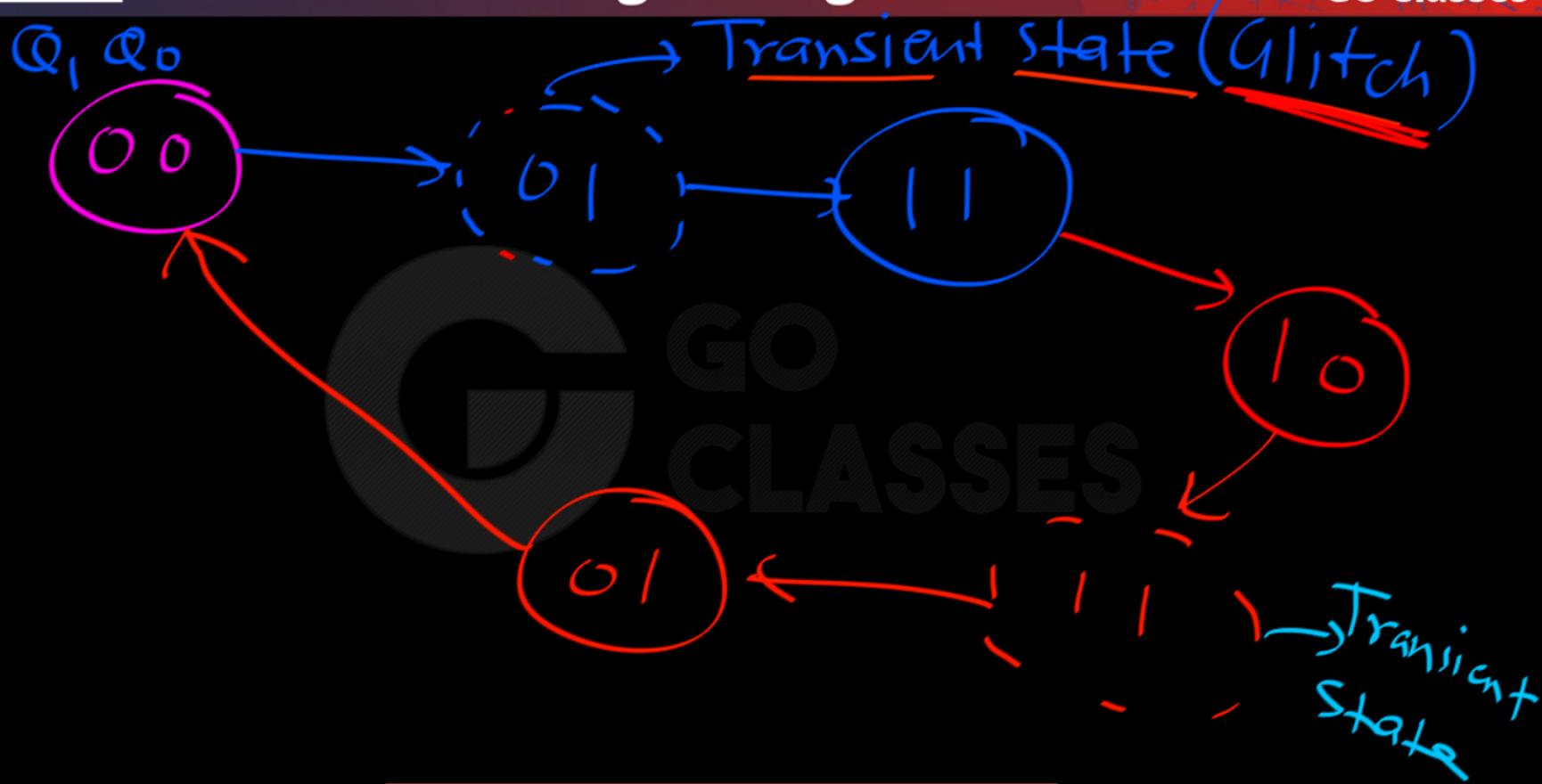
clock

 Q_0 Q_1 



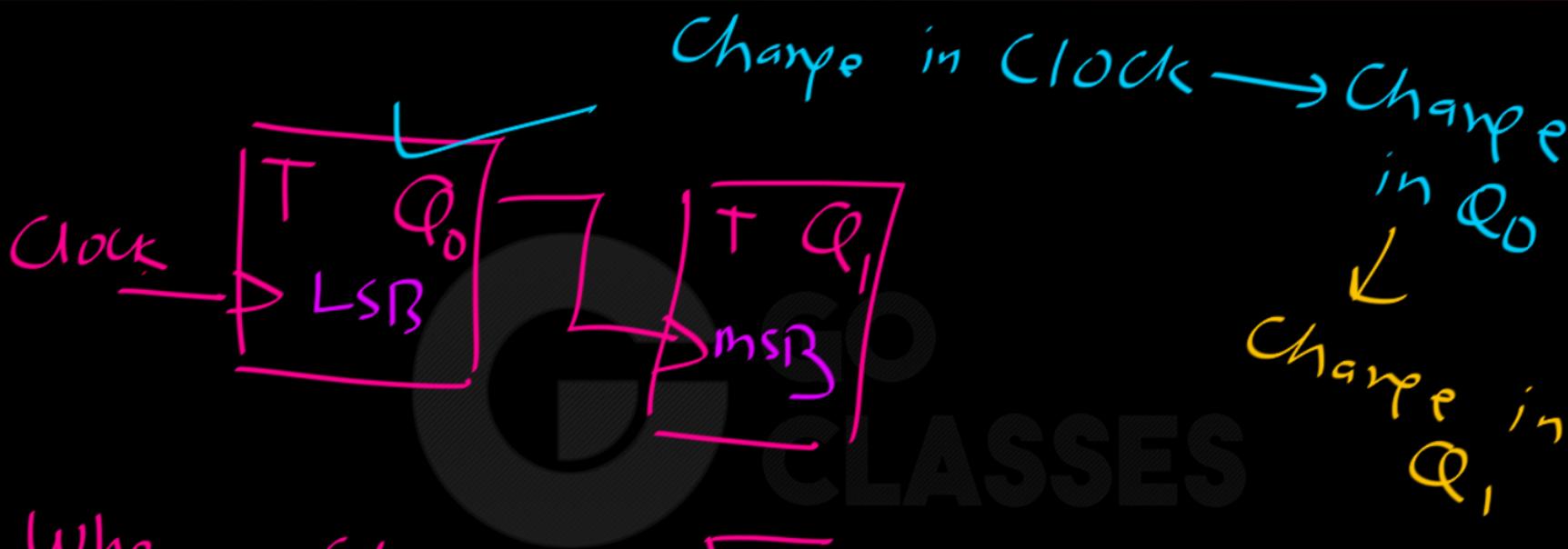


Digital Logic





Because of Propagation Delay of
ffs, we get Transient states
(Glitches)
in Asynch Counter.



When Clock \rightarrow Σ then Q_0 toggles
" Q_0 \rightarrow Σ " " Q_1 " "



Clock

1

1



2

1

0

0

1

0

1

1

0

1



3

0

0

1

1

0

1



4

0

0

0

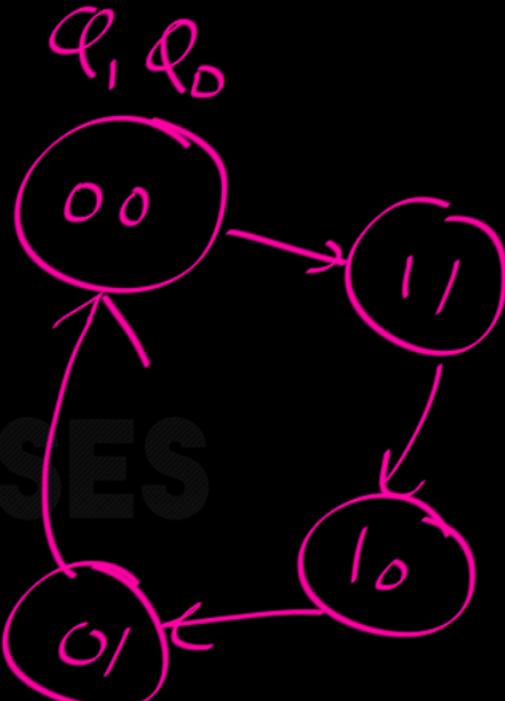
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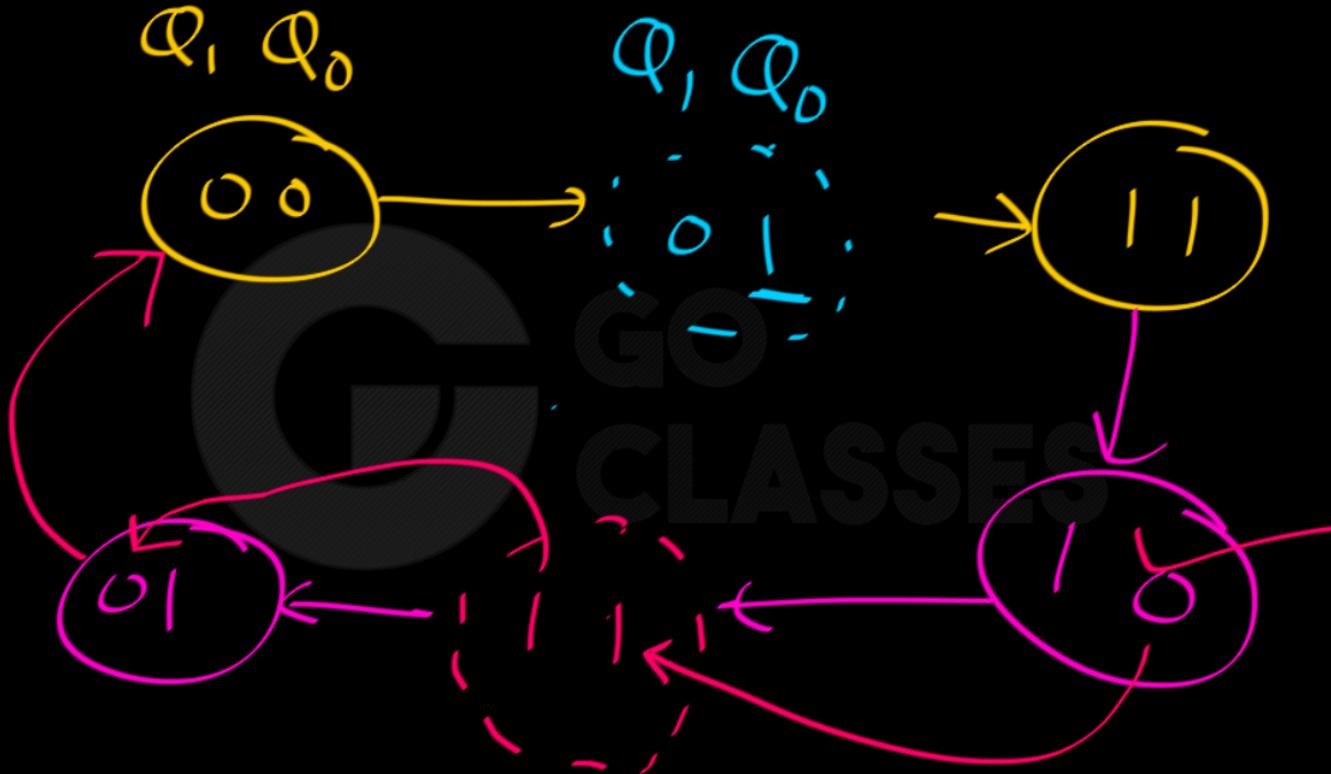


5

1

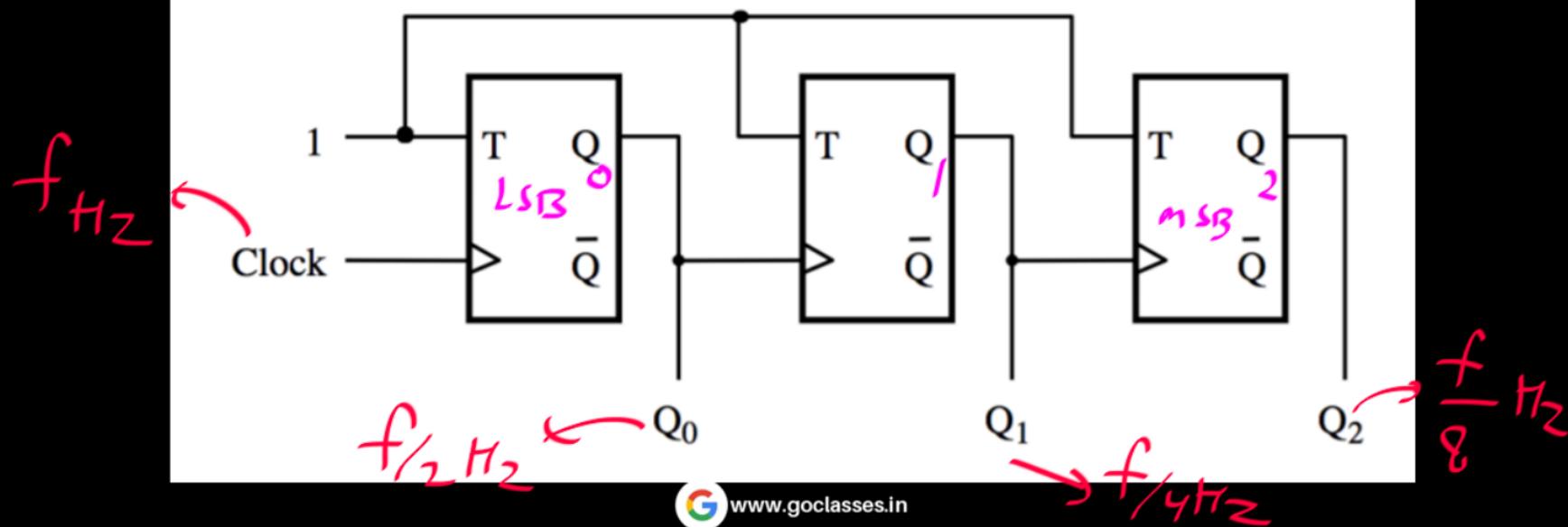
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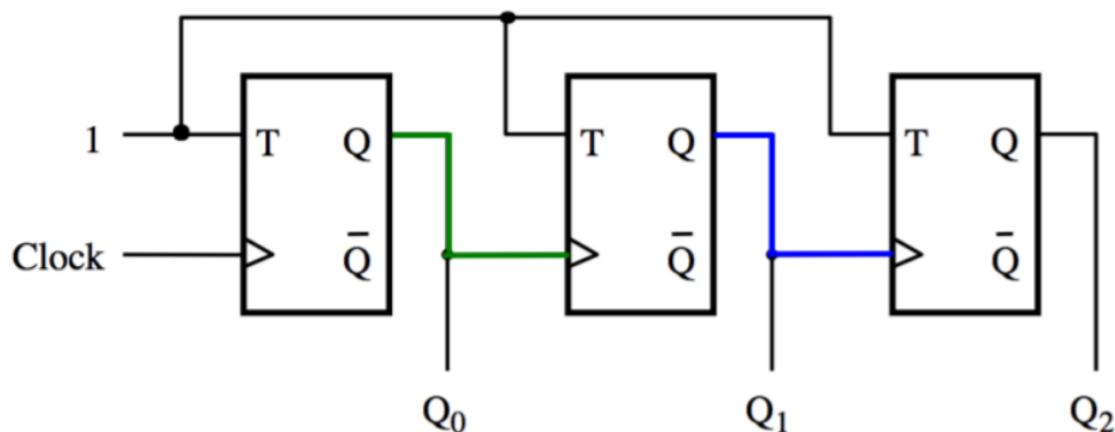


A three-bit down-counter

Divide by 8 counter



A three-bit down-counter

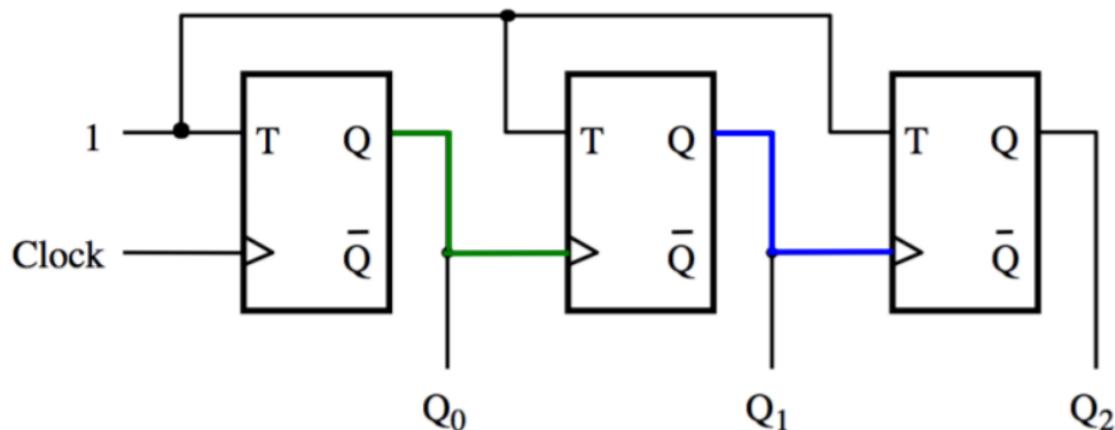


The first flip-flop changes
on the positive edge of the clock

The second flip-flop changes
on the positive edge of Q_0

The third flip-flop changes
on the positive edge of Q_1

A three-bit down-counter



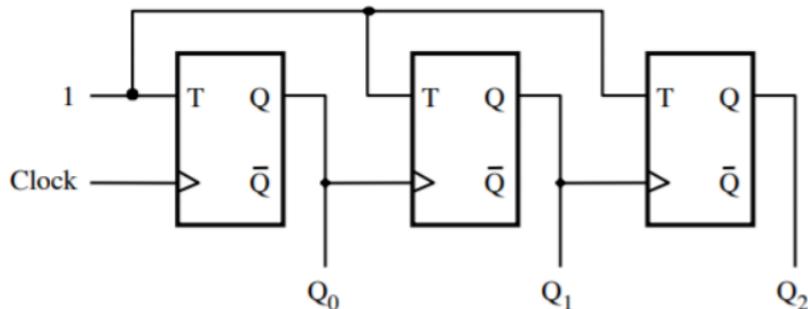
The first flip-flop changes
on the positive edge of the clock

The second flip-flop changes
on the positive edge of Q_0

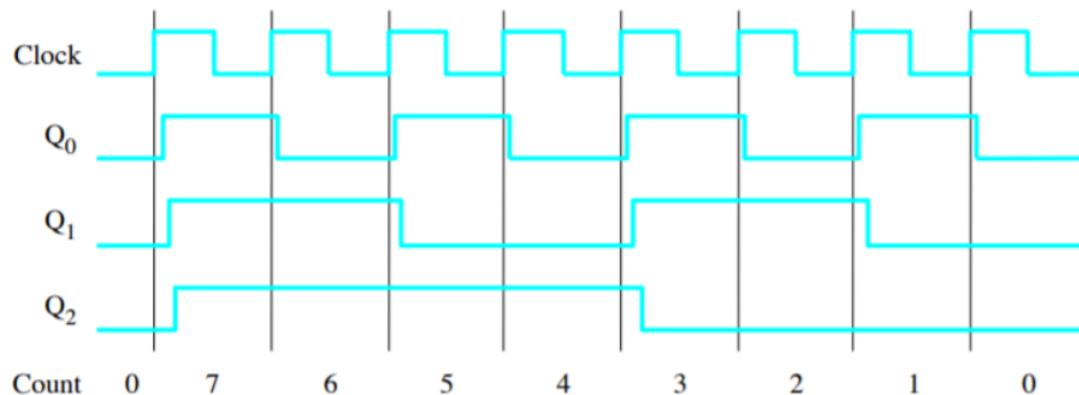
The third flip-flop changes
on the positive edge of Q_1



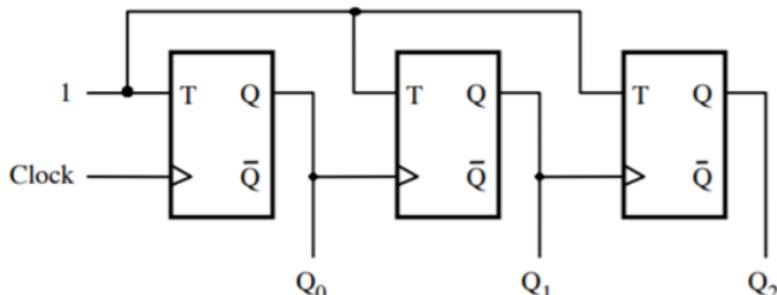
A three-bit down-counter



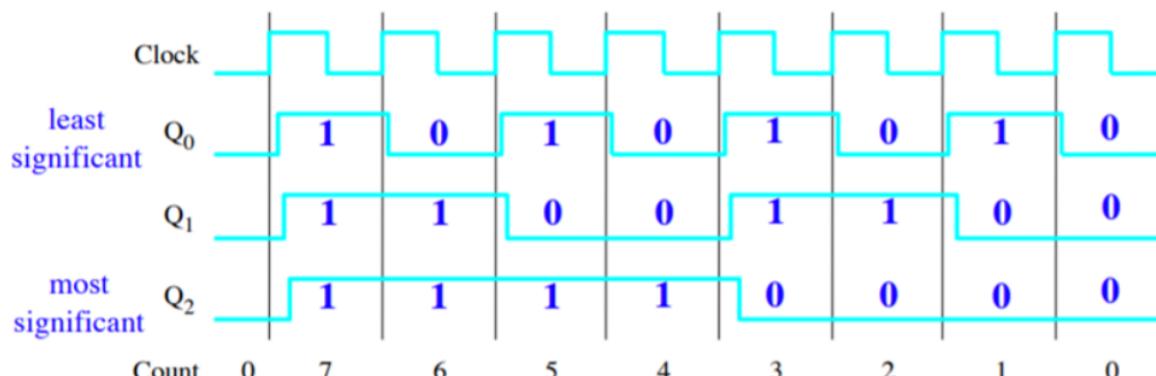
(a) Circuit



A three-bit down-counter

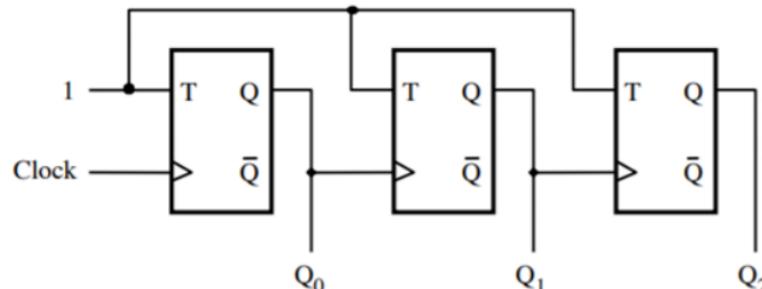


(a) Circuit

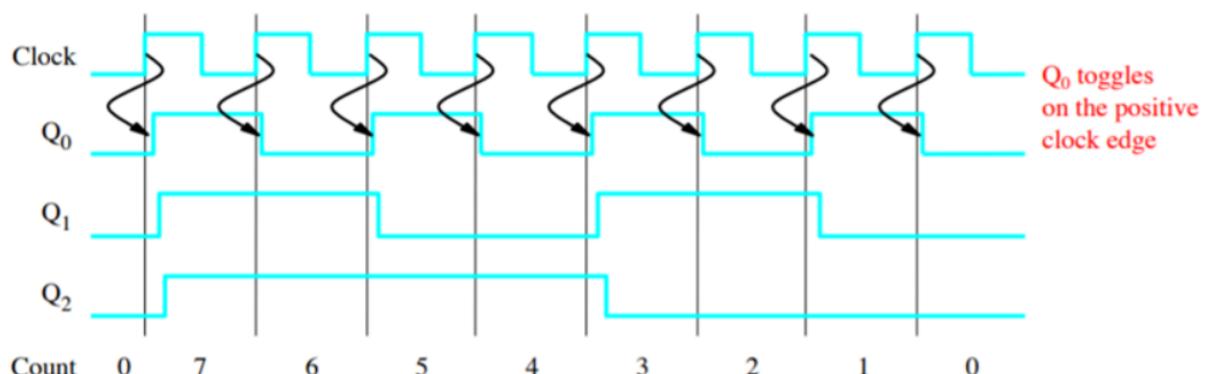


(b) Timing diagram

A three-bit down-counter

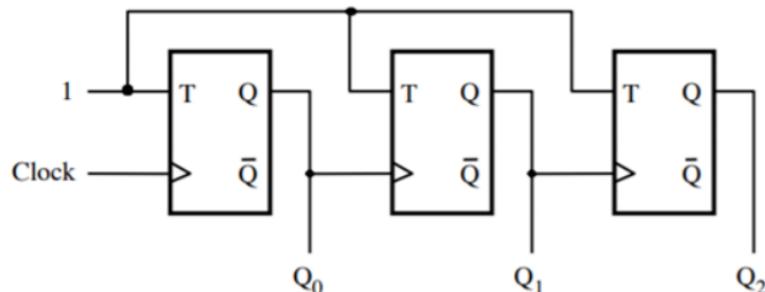


(a) Circuit

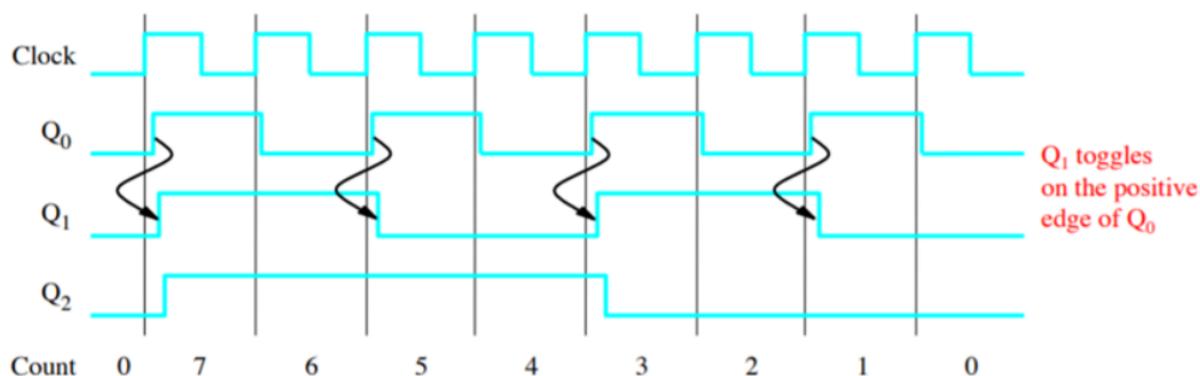


(b) Timing diagram

A three-bit down-counter

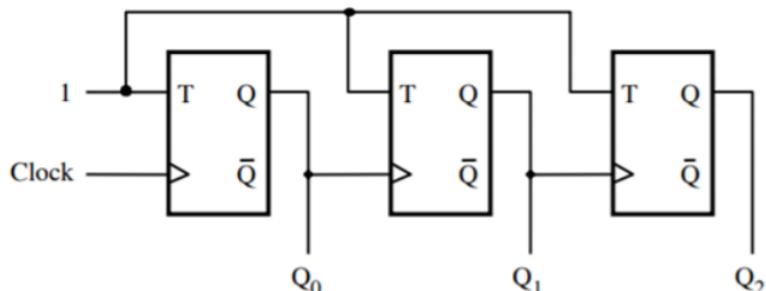


(a) Circuit

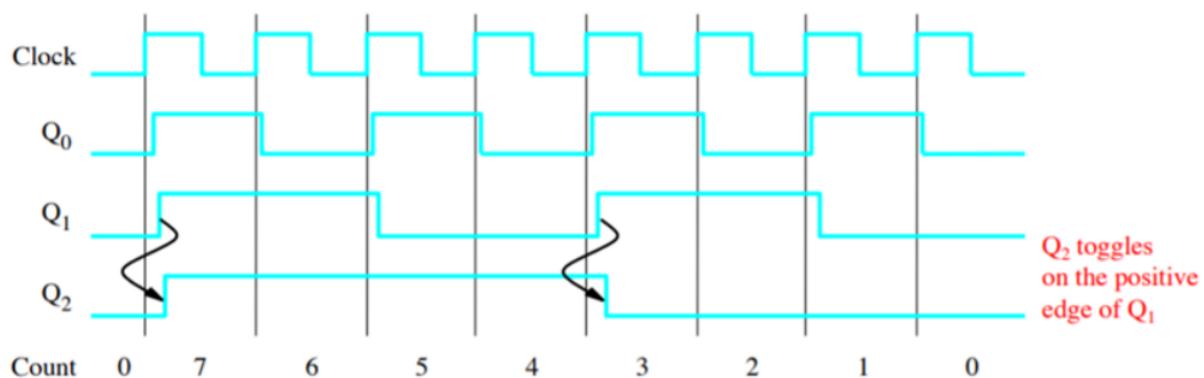


(b) Timing diagram

A three-bit down-counter

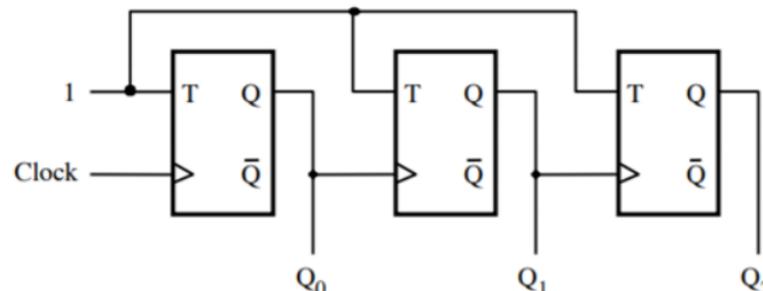


(a) Circuit



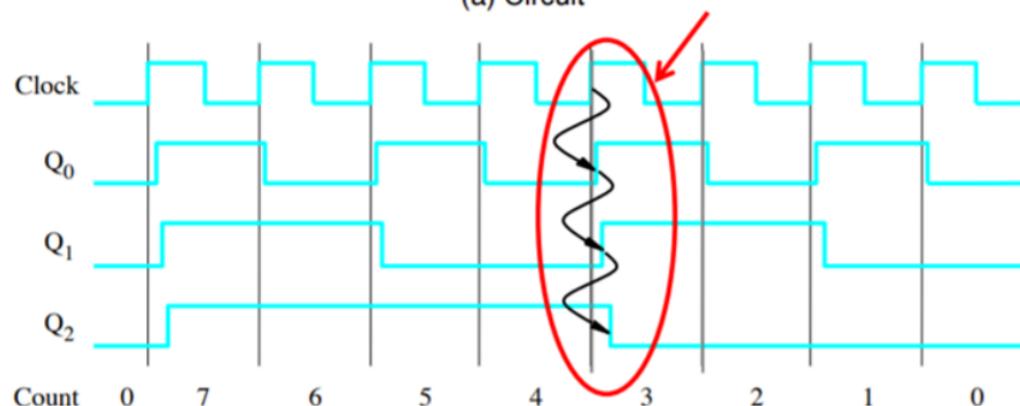
(b) Timing diagram

A three-bit down-counter



(a) Circuit

The propagation delays get longer



(b) Timing diagram