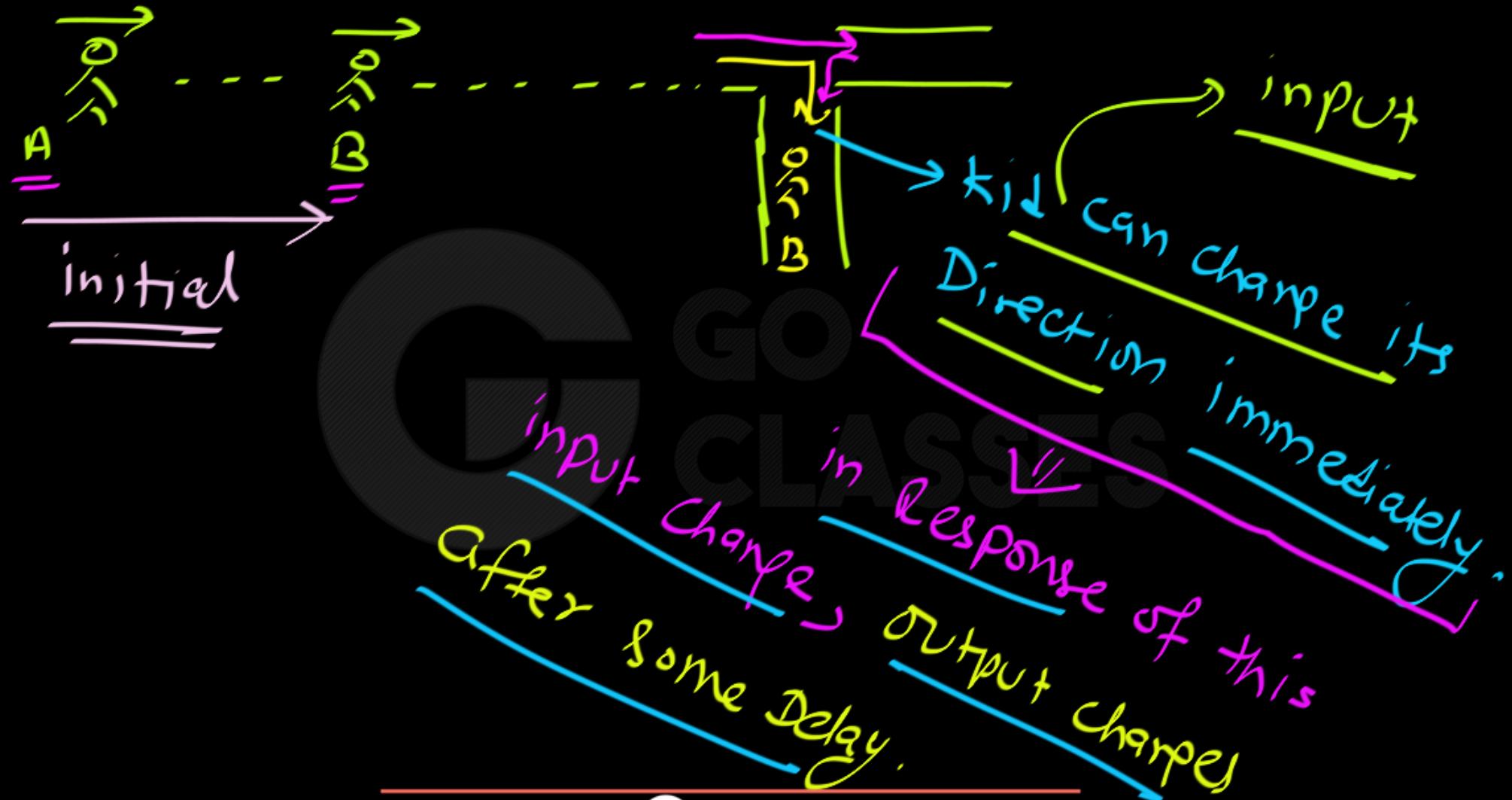


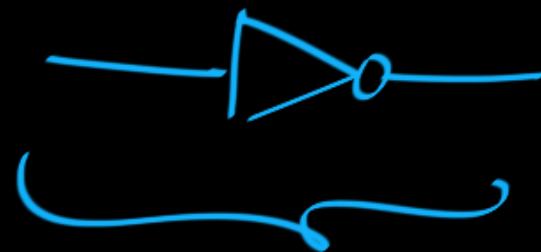


## Next Topic:

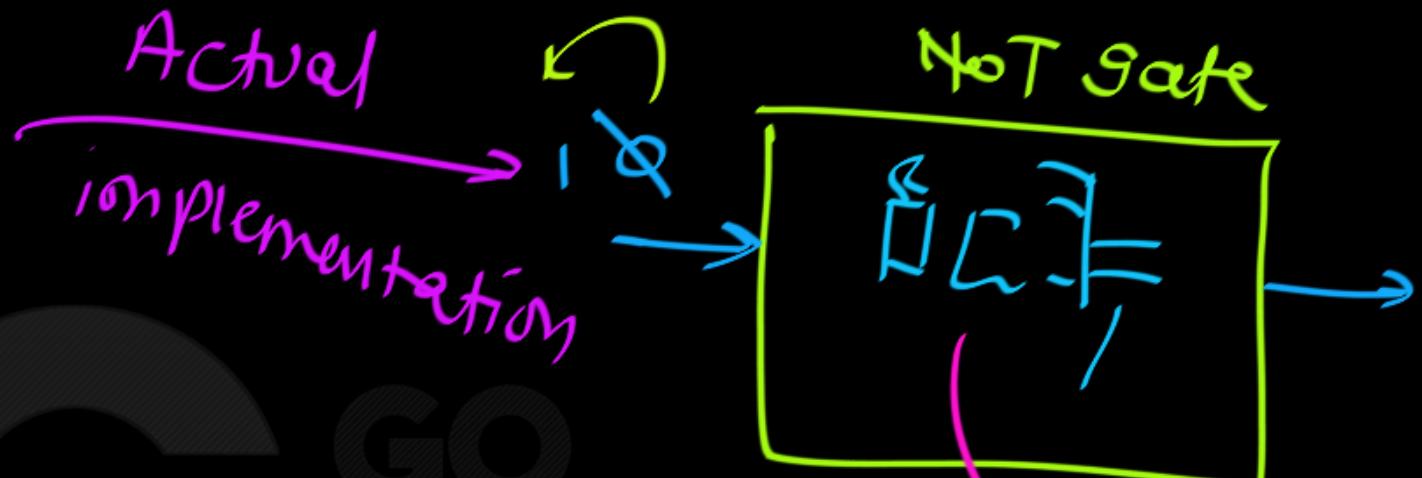
# Propagation Delay

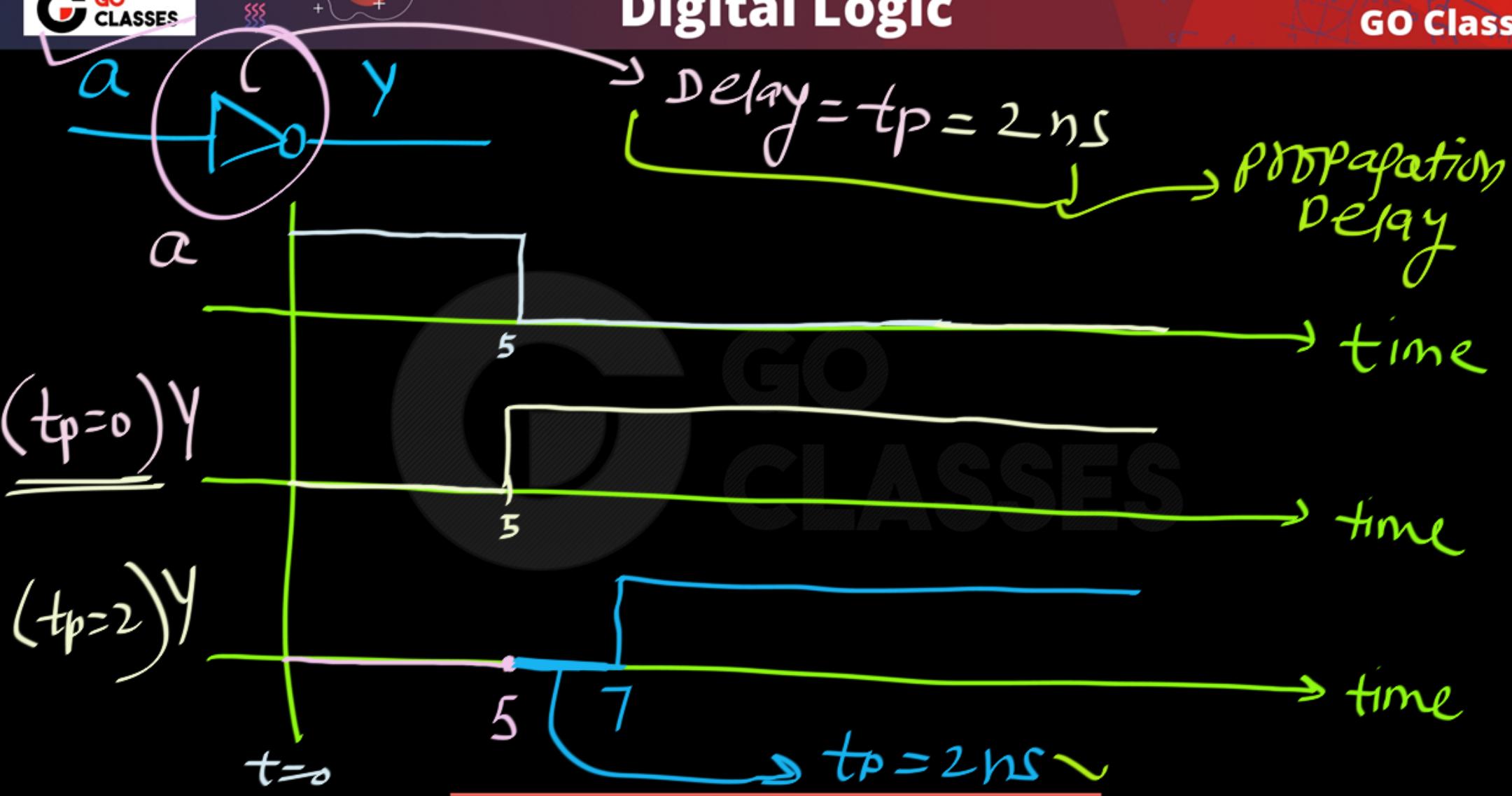
# Timing Diagrams





Just a  
Symbol of  
NOT gate







## Gate Delays and Timing Diagrams





## Propagation Delay(Gate Delay) :

When the input to a logic gate is changed, the output will not change instantaneously. The transistors or other switching elements within the gate take a finite time to react to a change in input, so that the change in the gate output is delayed with respect to the input change.

If the change in output is delayed by time,  $\epsilon$ , with respect to the input, we say that this gate has a propagation delay of  $\epsilon$ .

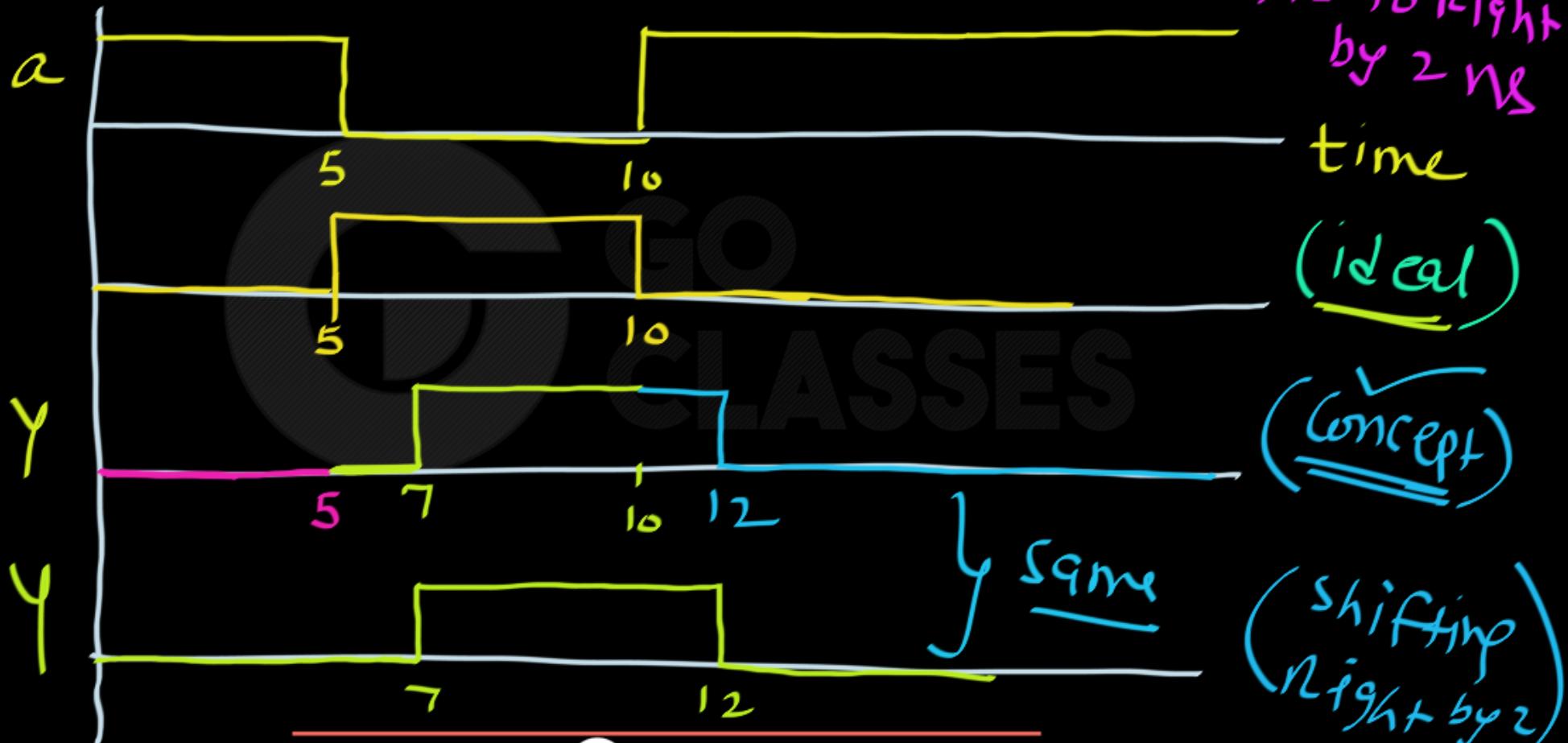
$\delta, \Delta, \epsilon$   
symbols for  $t_p$

# Digital Logic



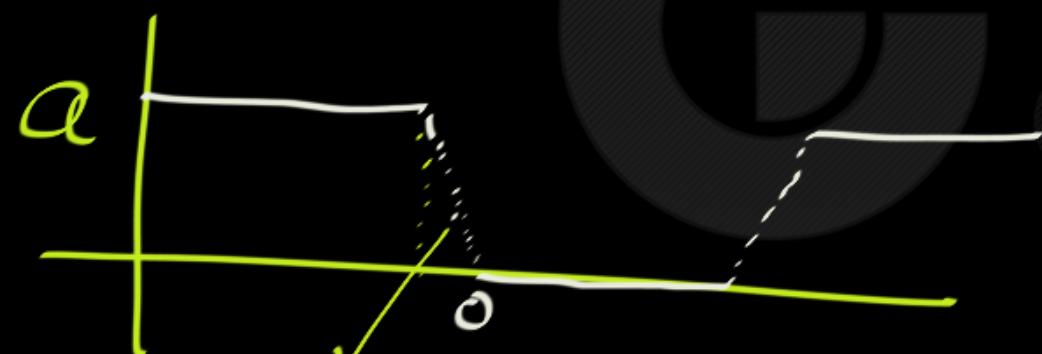
$$t_p = 2 \text{ ns}$$

ideal  $\rightarrow$  OP waveform shifts to Right by  $2 \text{ ns}$



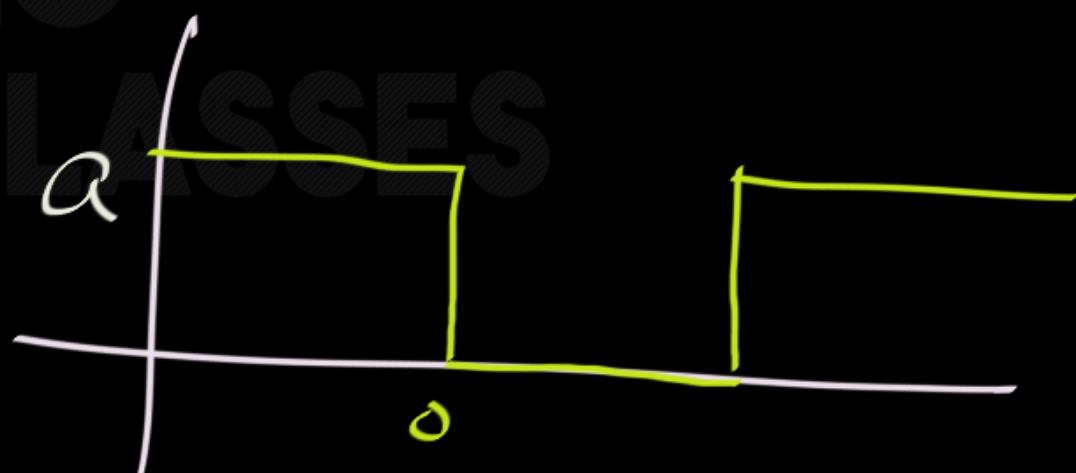
When input  $0 \rightarrow 1$  (or  $1 \rightarrow 0$ )

Practically



Negligible

Theoretically



Note:  most standard books

We will Assume  Input Can

Change Immediately.

$T_P$  : Propagation Delay.

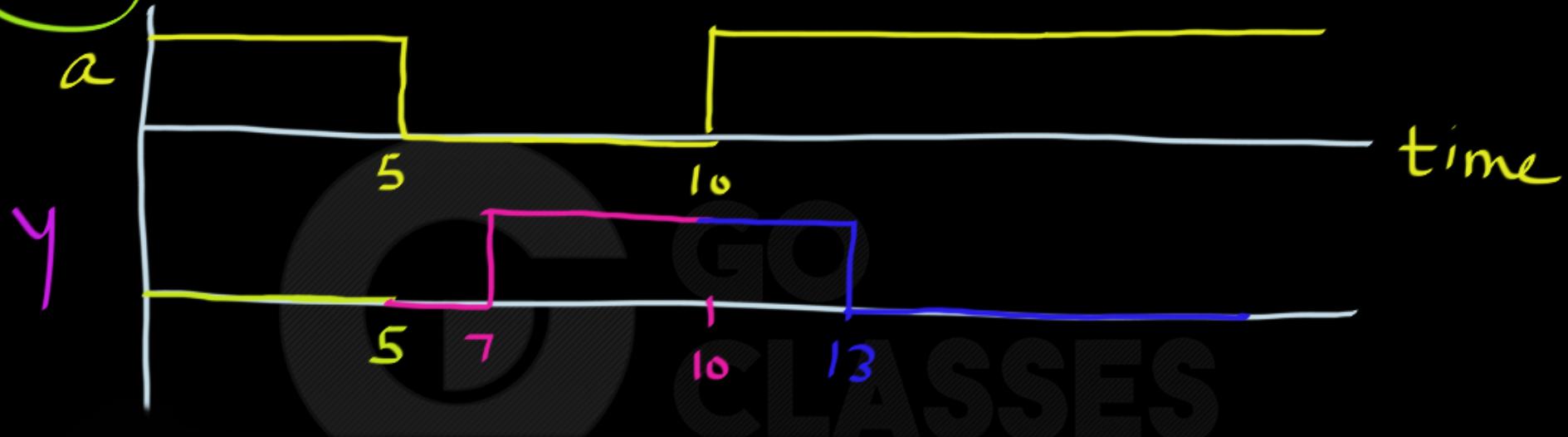
$T_{PLH}$  : Prop. Delay when  $\delta P$  goes  
from low to High

$T_{PHL}$  : Prop. Delay when  $\delta P$  goes from  
High to Low.

# Digital Logic



$$T_{PLH} = 2 \text{ ns}; \quad T_{PHL} = 3 \text{ ns}$$





Practically,

$$t_{PLH} \neq t_{PHL}$$

Theoretically,

We will Assume

$$\overline{T}_{PLH} = \overline{T}_{PHL} = T_P$$



## Propagation Delay(Gate Delay) :

In practice, the propagation delay for a 0 to 1 output change may be different than the delay for a 1 to 0 change.

But we will assume that they are same and hence, we will only consider propagation delay of a gate.

CLASSES



## Assumptions:

① Input can change immediately.

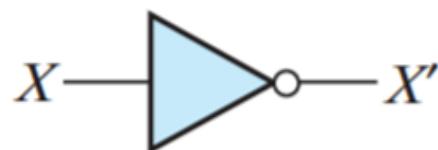
②  $\boxed{\overline{T}_{PLH} = \overline{T}_{PHL} - \overline{T}_P}$  ✓



# Propagation Delay

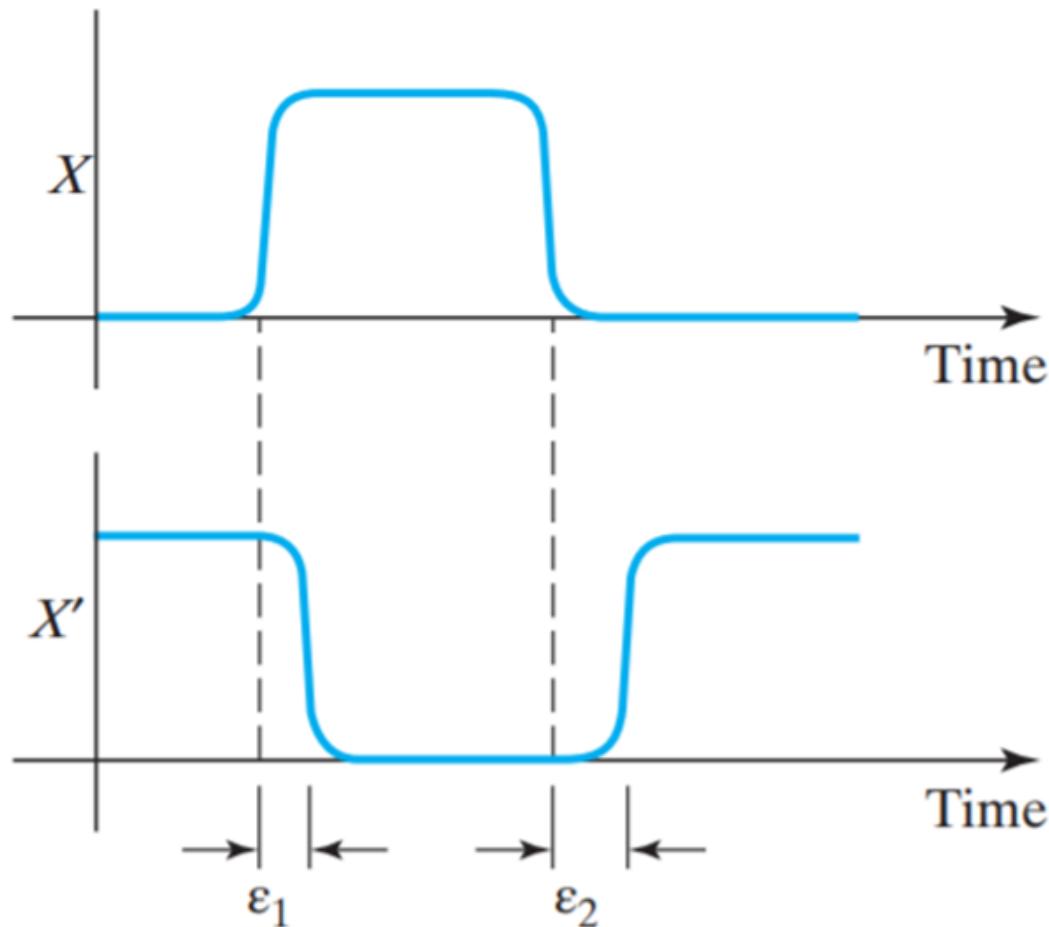
- When gate inputs change, outputs don't change instantaneously
  - This delay is known as “gate” or “propagation” delay

## Propagation Delay in an Inverter



$$\epsilon_1 = T_{PHL}$$

$$\epsilon_2 = T_{PLH}$$

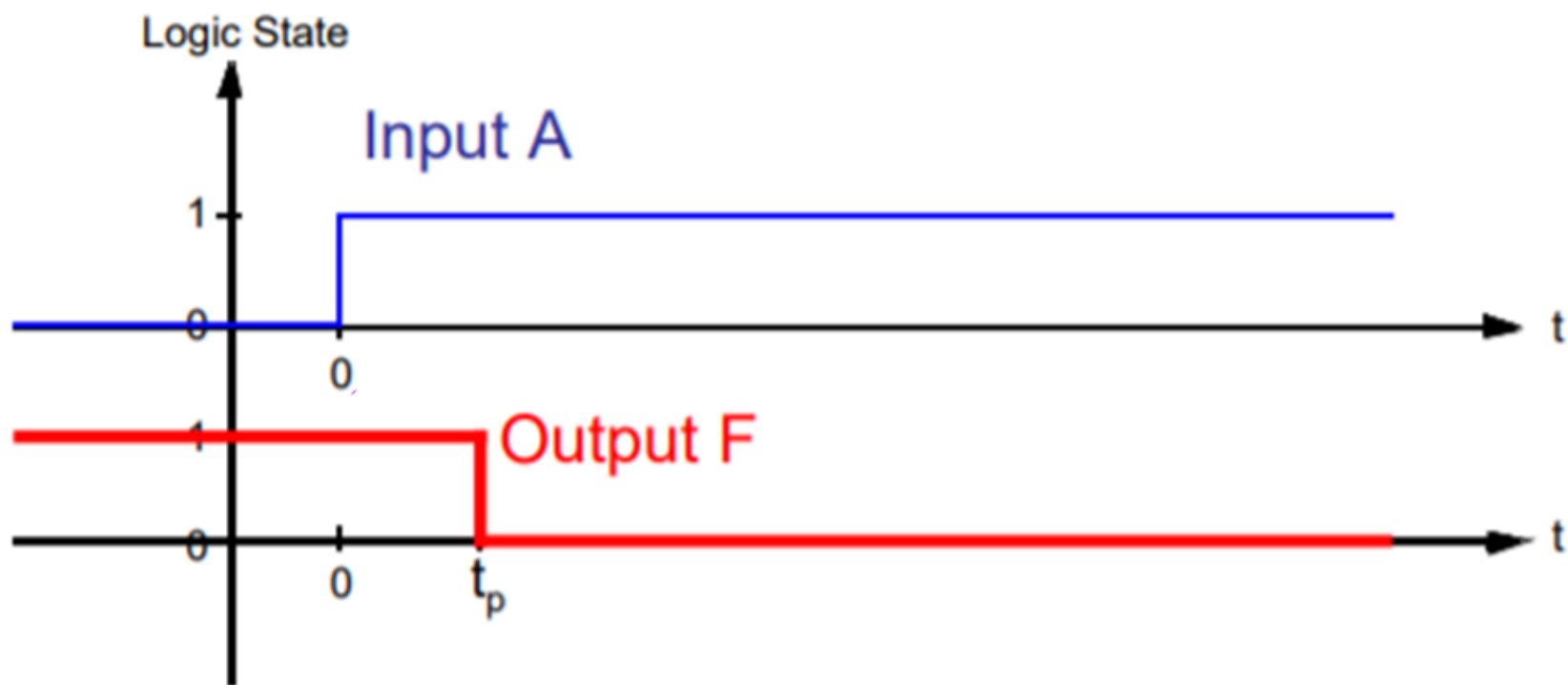




# Propagation Delay

- $\varepsilon_1$  is the propagation delay from input going high to output going low (inverting logic)
  - $t_{PHL}$
- $\varepsilon_2$  is the propagation delay from input going low to output going high (inverting logic)
  - $t_{PLH}$

Example 1 :





## Example 2:

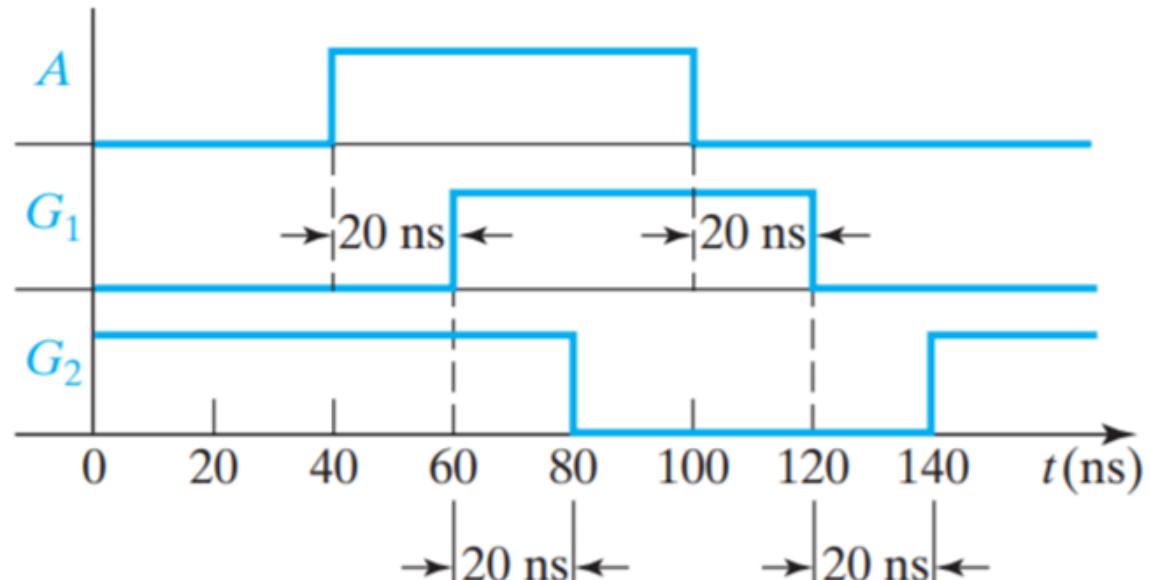
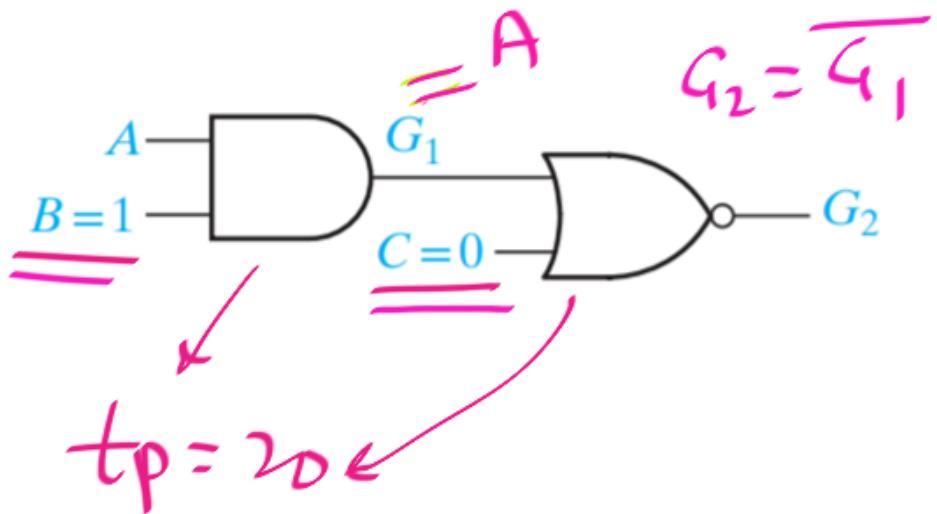
Figure 8-5 shows the timing diagram for a circuit with two gates. We will assume that each gate has a propagation delay of 20 ns (nanoseconds). This timing diagram indicates what happens when gate inputs  $B$  and  $C$  are held at constant values 1 and 0, respectively, and input  $A$  is changed to 1 at  $t = 40$  ns and then changed back to 0 at  $t = 100$  ns. The output of gate  $G_1$  changes 20 ns after  $A$  changes, and the output of gate  $G_2$  changes 20 ns after  $G_1$  changes.

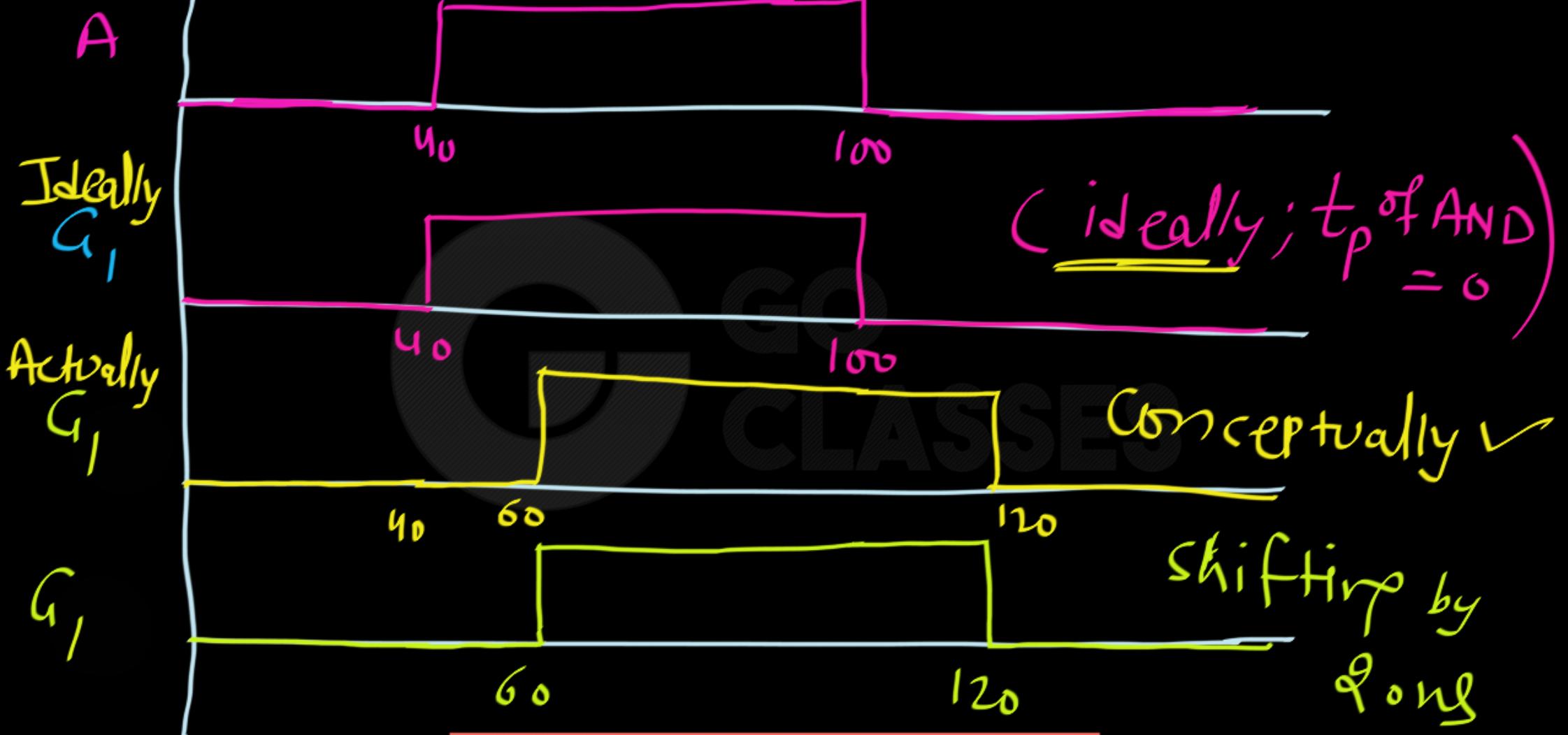


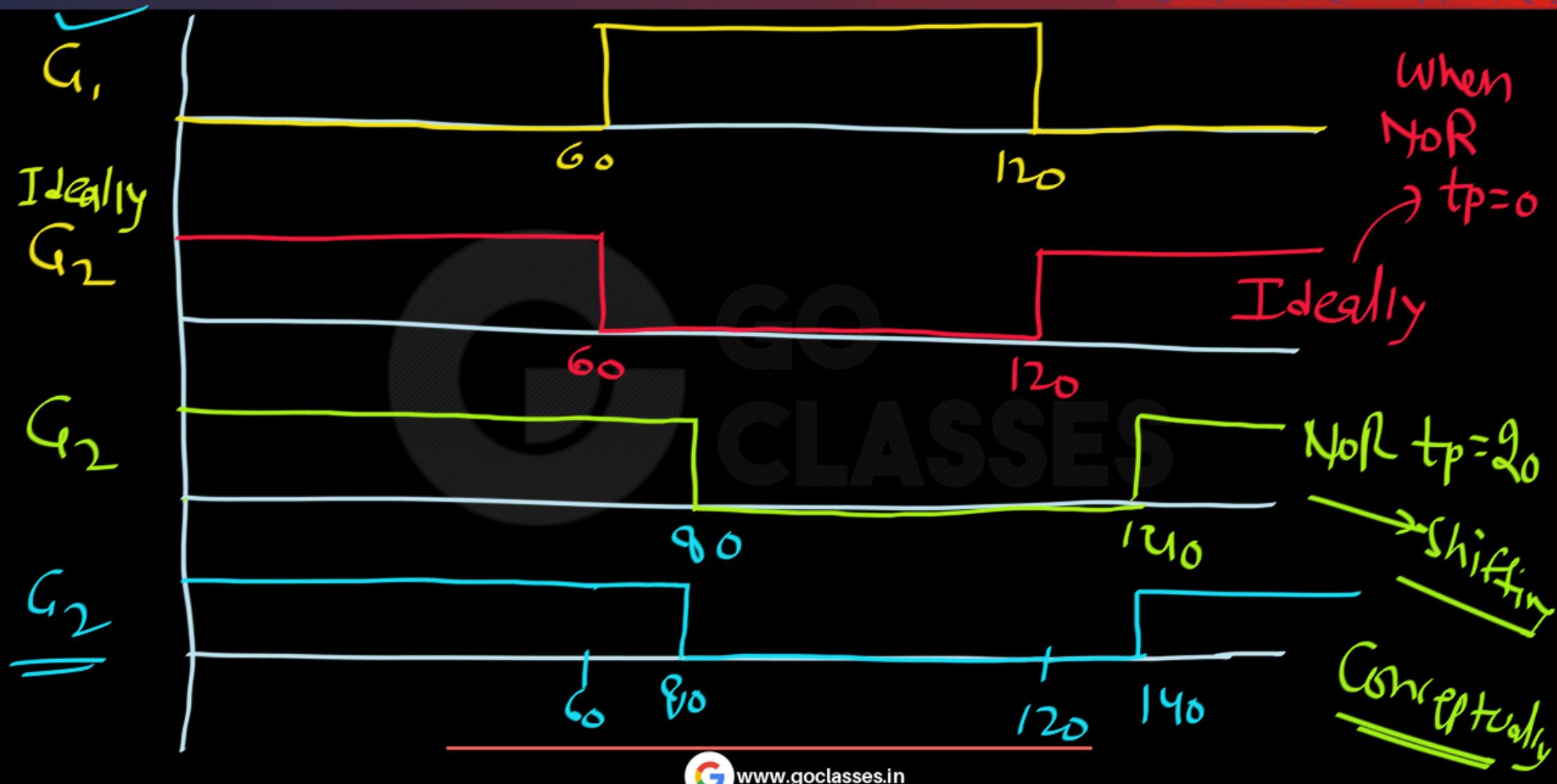


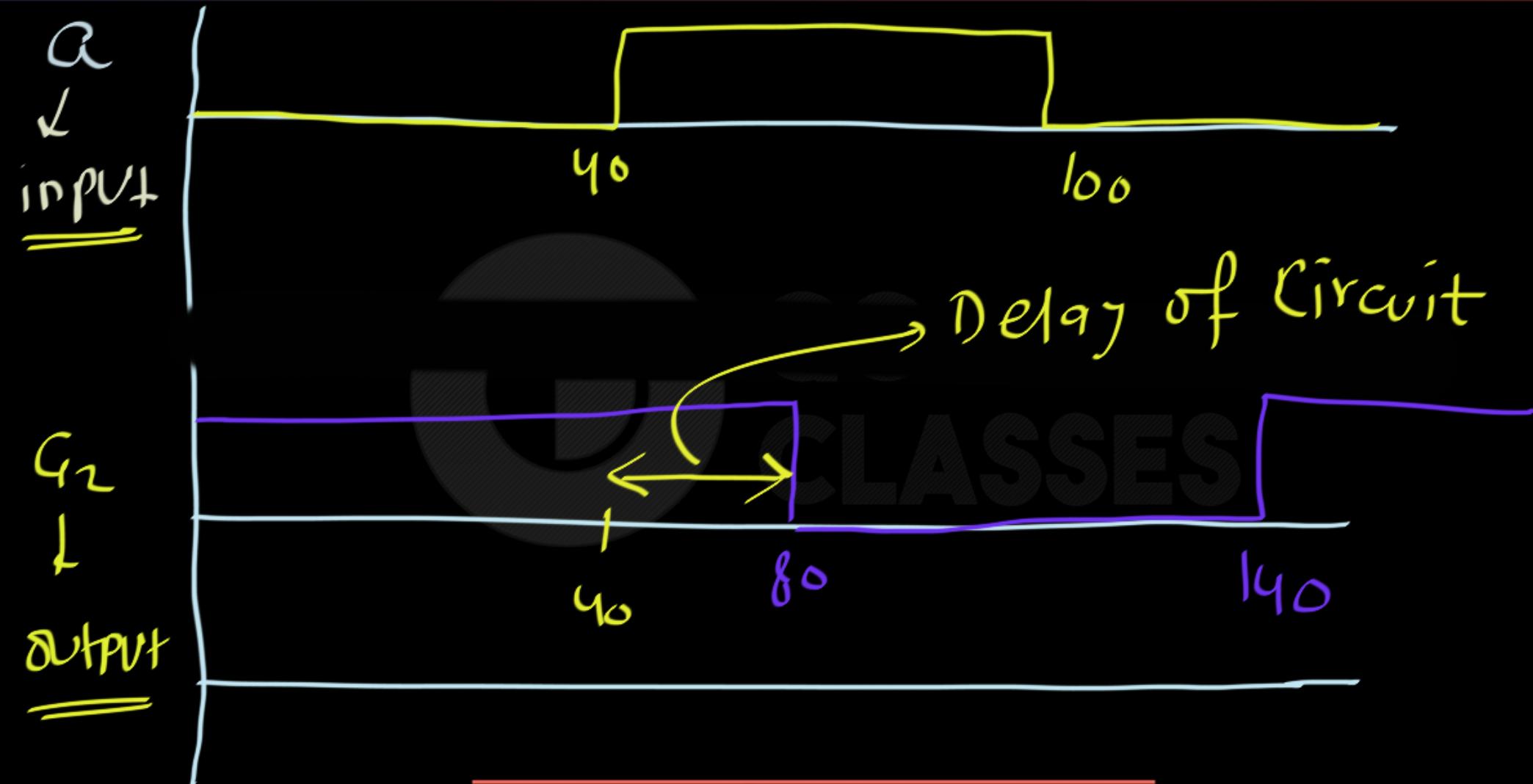
FIGURE 8-5

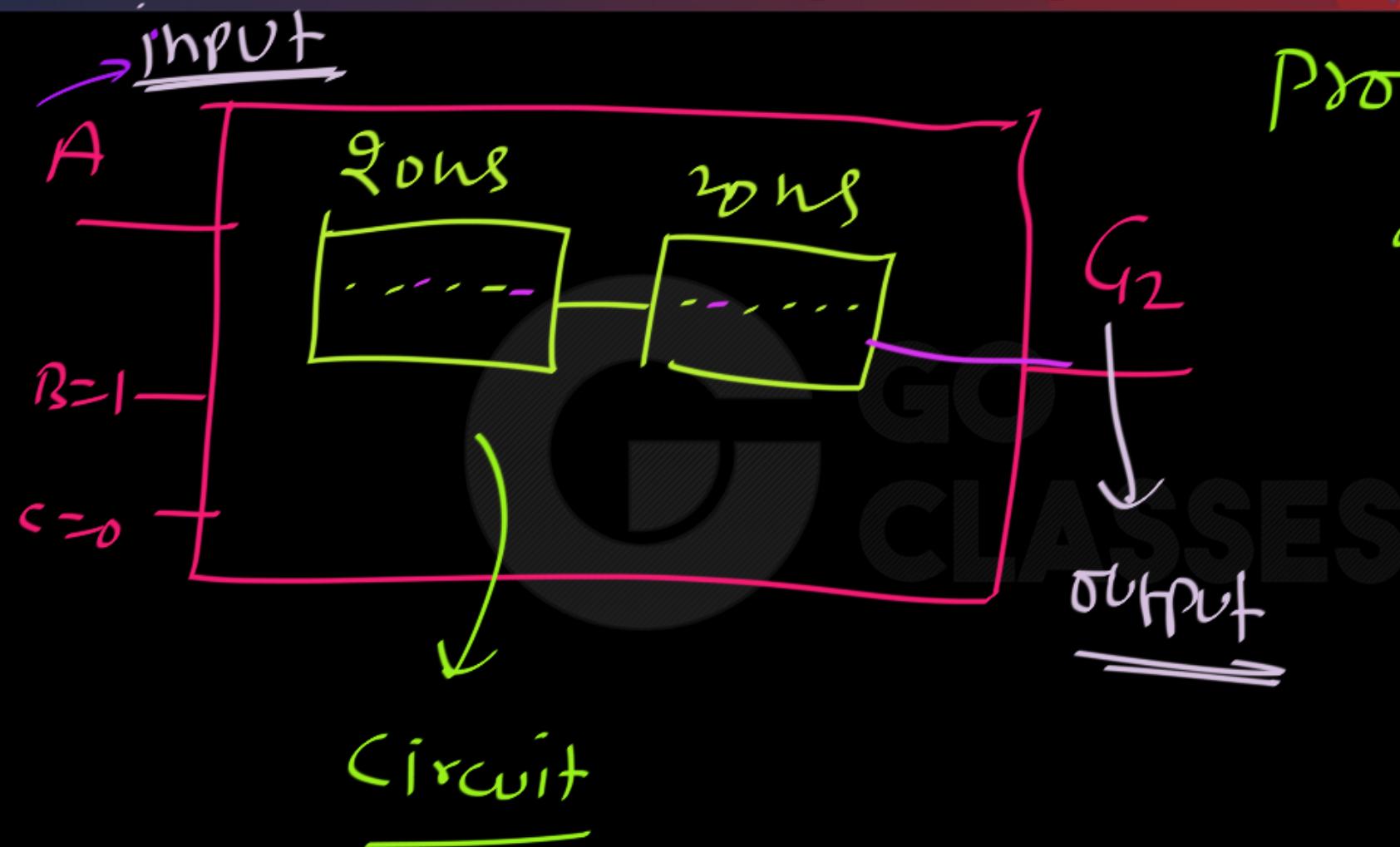
Timing Diagram for AND-NOR Circuit











Prop. Delay  
of this  
Circuit:

Y0 ns



## Next Topic:

# Propagation Delay of a Circuit

# Propagation Delay

- Maximum propagation delay is the longest delay between an input changing value and the output changing value
- The path that causes this delay is called the critical path
  - The critical path imposes a limit on the maximum speed of the circuit



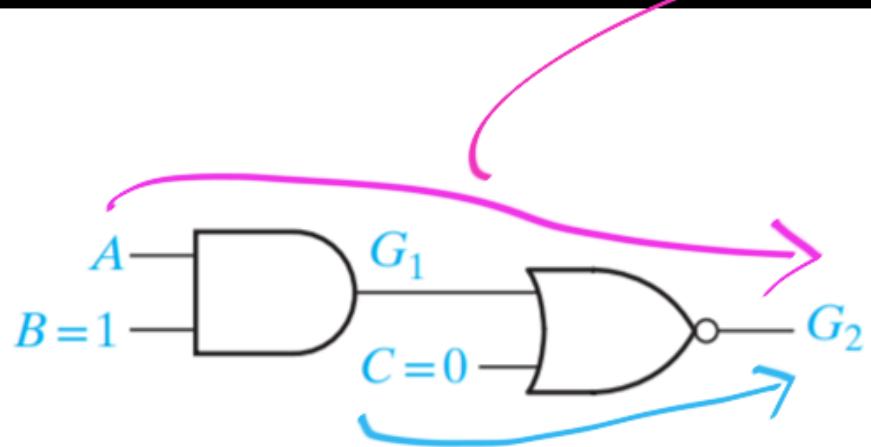
The propagation path that determines the delay through the circuit is called the critical path.

Delay(circuit) = Delay of critical path



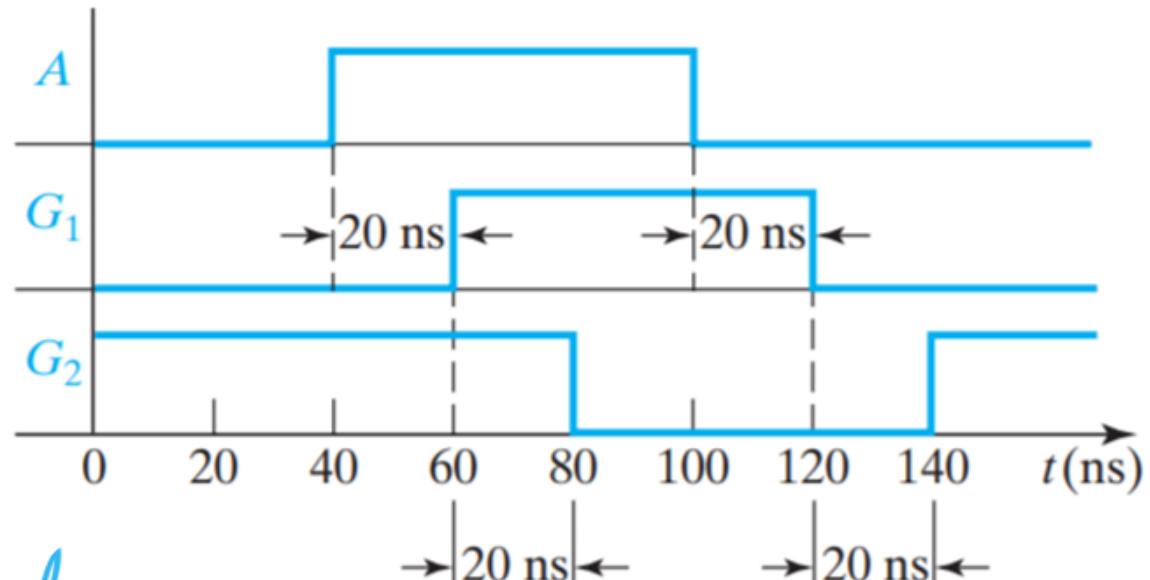
FIGURE 8-5

Timing Diagram for  
AND-NOR Circuit



Not critical  
Path

critical Path





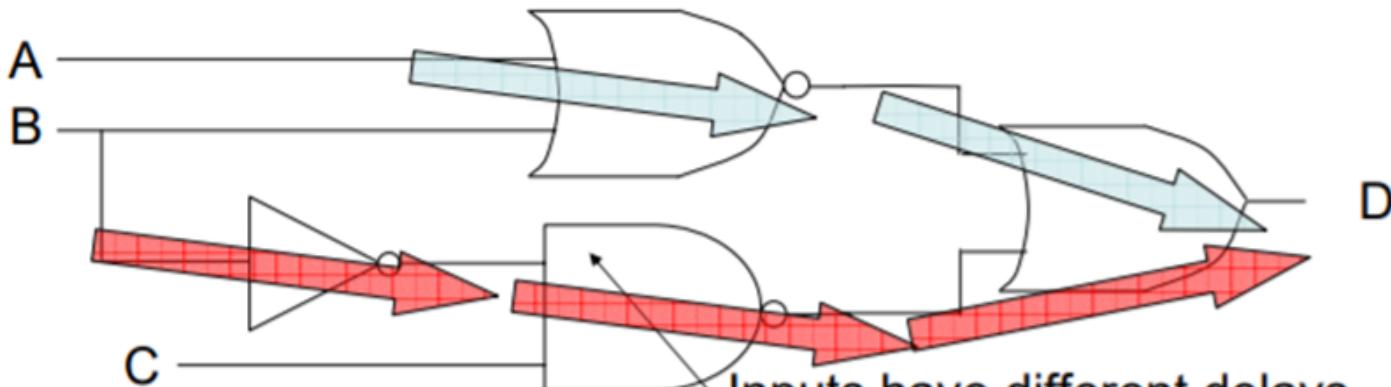
# Propagation Delay

- For example circuit, critical path is from any change in the A input resulting in a change in  $G_2$ 
  - Circuit is inverting (from A to  $G_2$ )
    - With B = 1 and C = 0,  $A \uparrow$  causes  $G_2 \downarrow$  ( $t_{PHL} = 20$  ns) and  $A \downarrow$  causes  $G_2 \uparrow$  ( $t_{PLH} = 20$  ns)
  - Maximum propagation delay
    - $20$  ns +  $20$  ns =  $40$  ns

# Digital Logic

## PROPAGATION DELAY

$$t_p(\text{circuit}) = 3 t_p$$

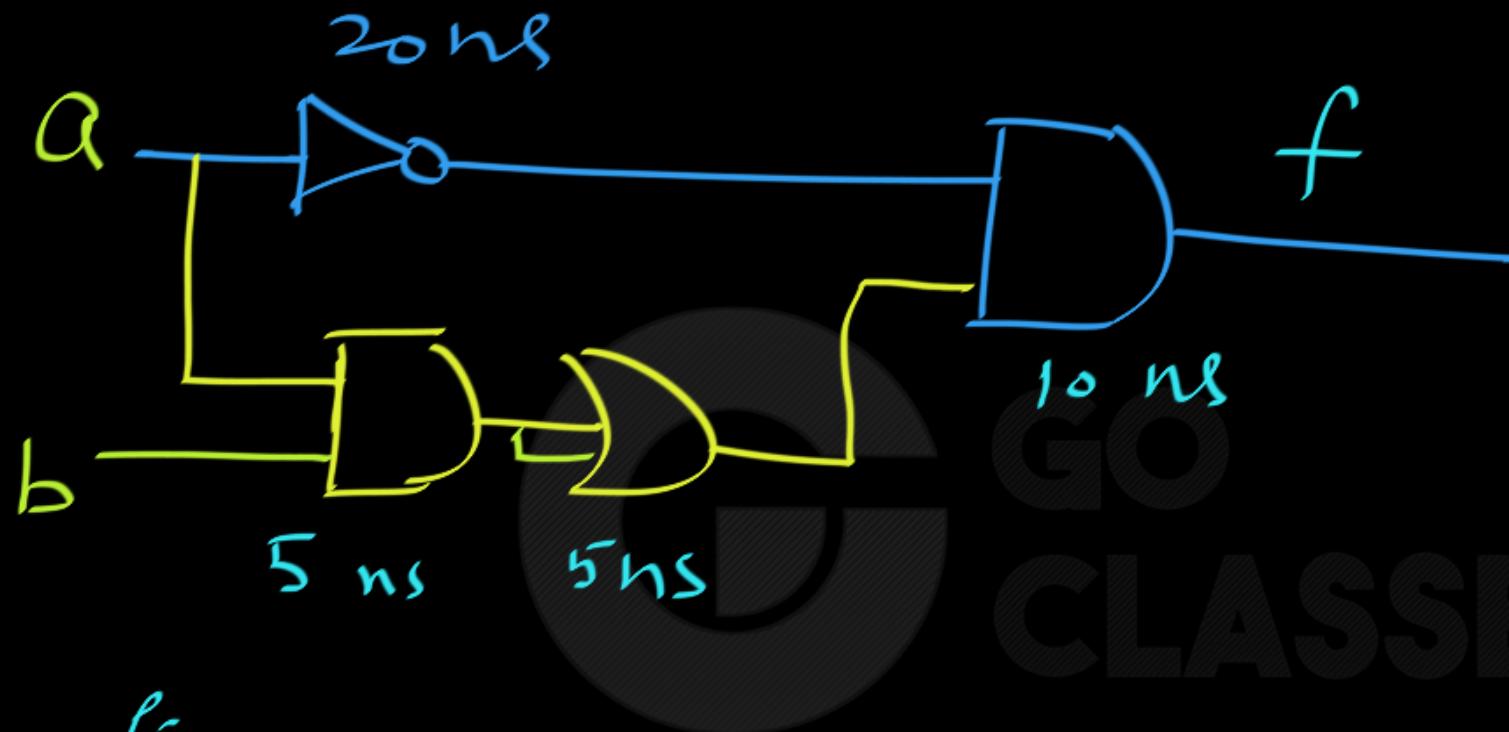


Inputs have different delays,  
but we ascribe a single worst-case delay  $t_p$  to every gate

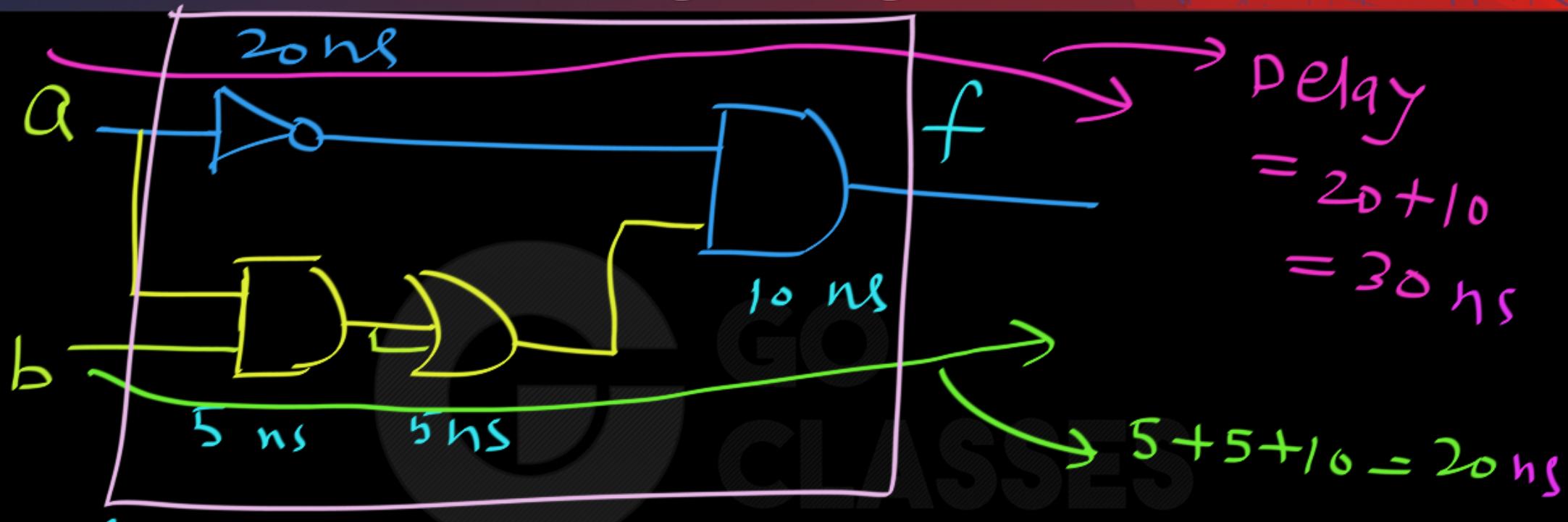
How many gate delays for shortest path? **ANSWER : 2**

How many gate delays for longest path? **ANSWER : 3**

Critical Path

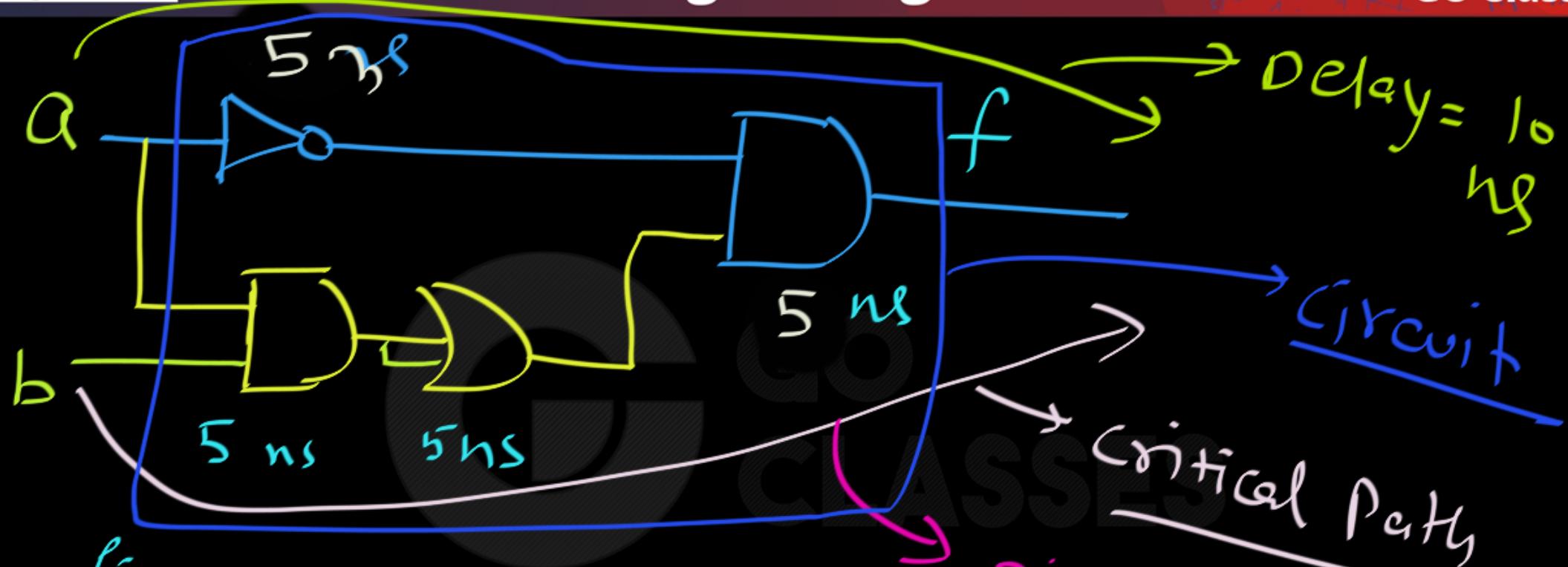


find Critical Path ?



find Critical Path  $\Rightarrow$  blue Path (pink Path)

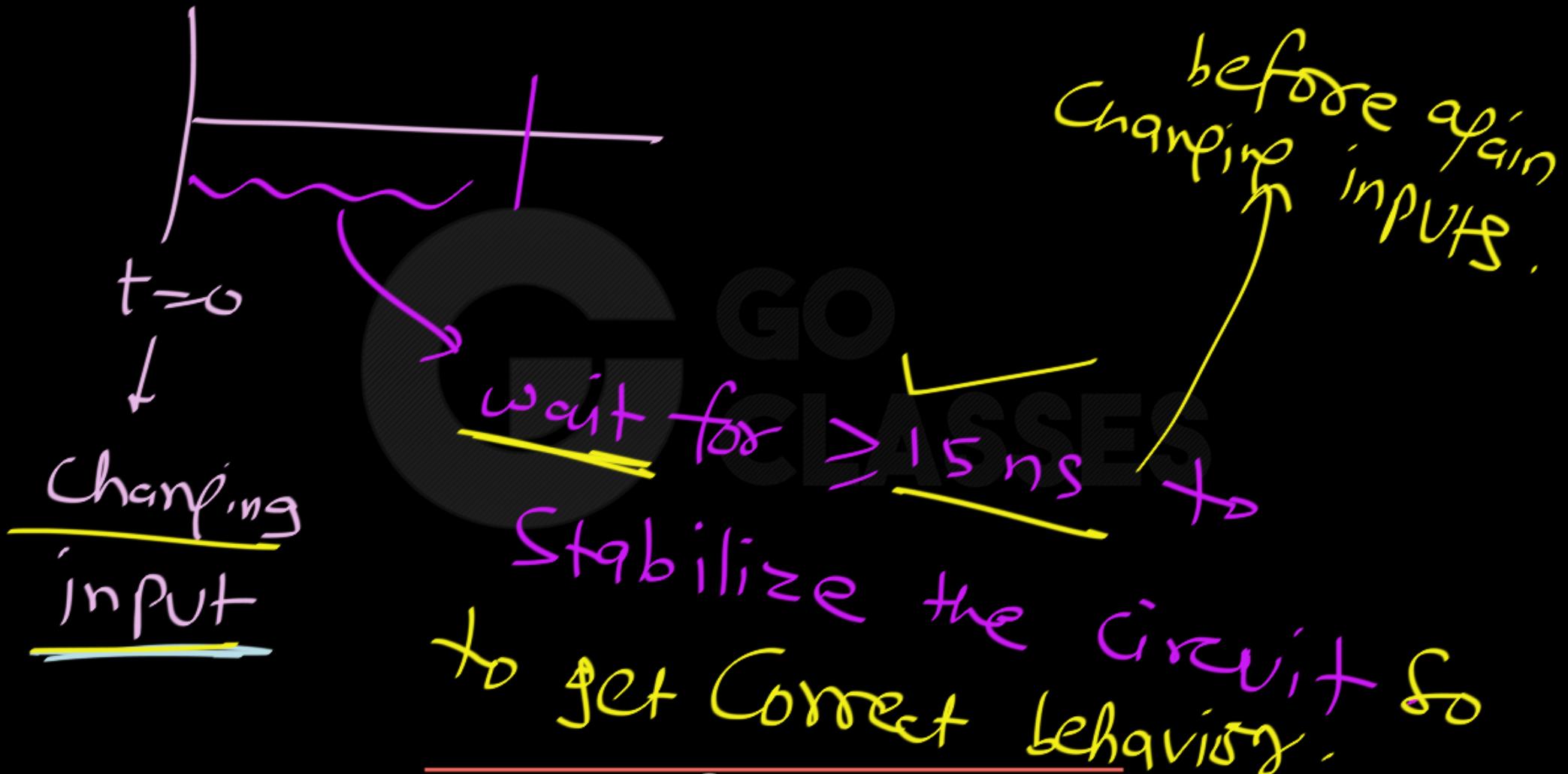
$t_p(\text{circuit}) = 30 \text{ ns}$  ✓

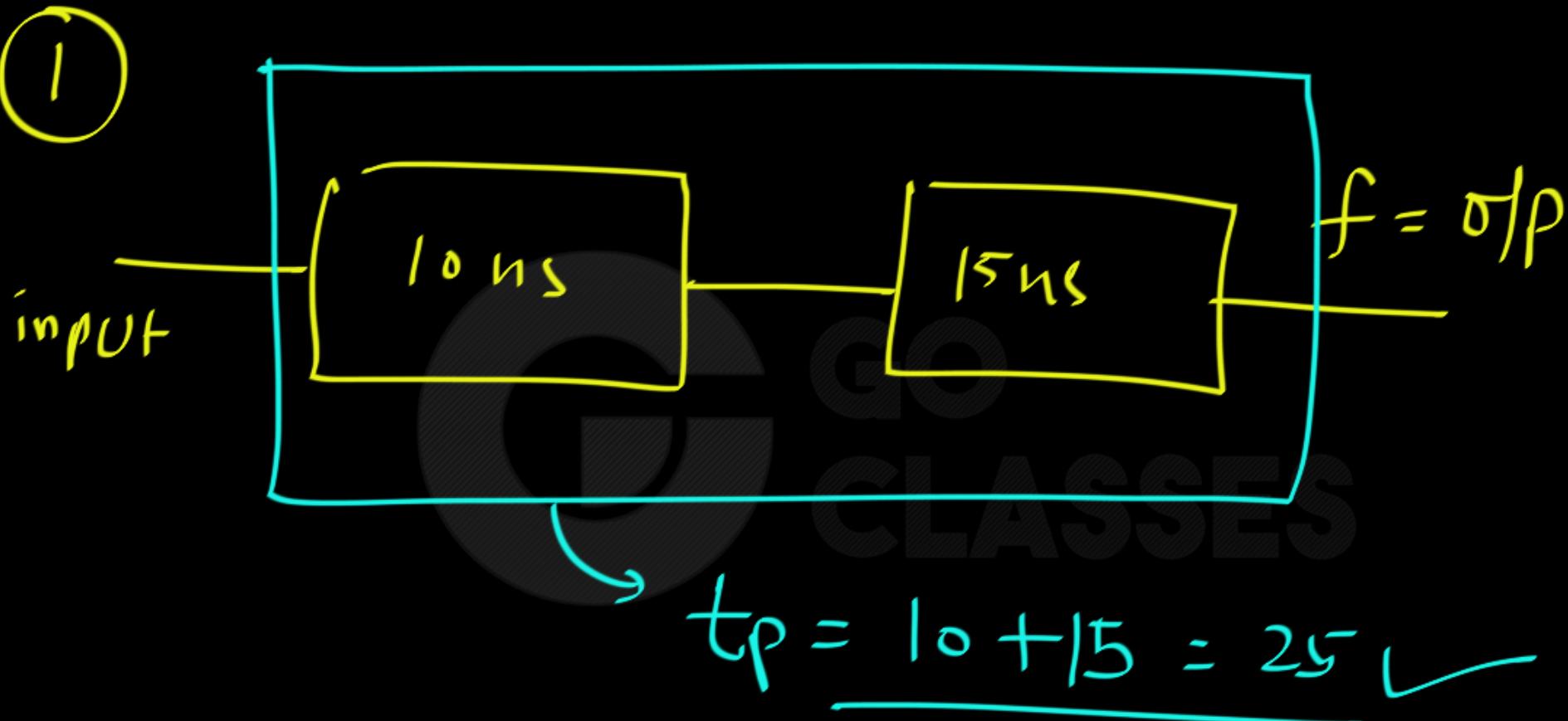


find Critical Path

$$t_p(\text{circuit}) = 15 \text{ ns}$$

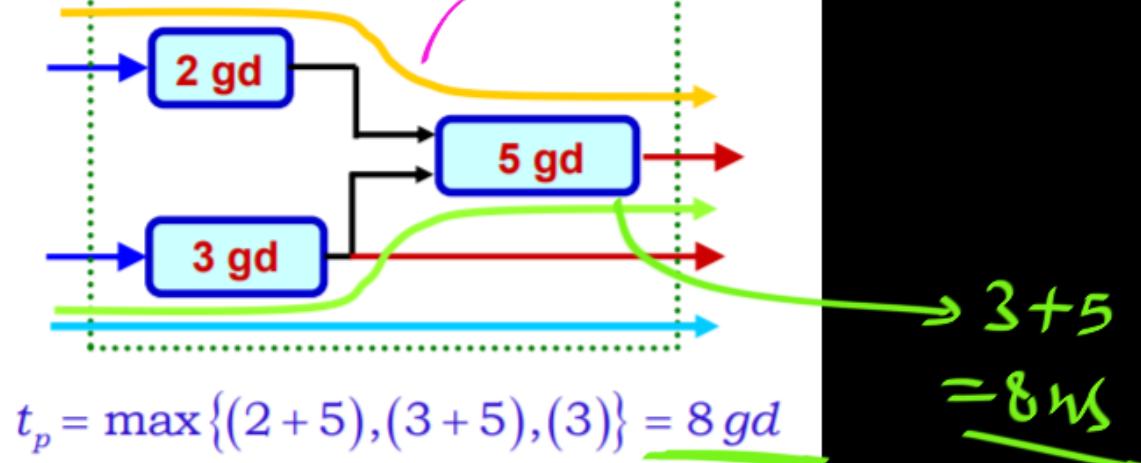
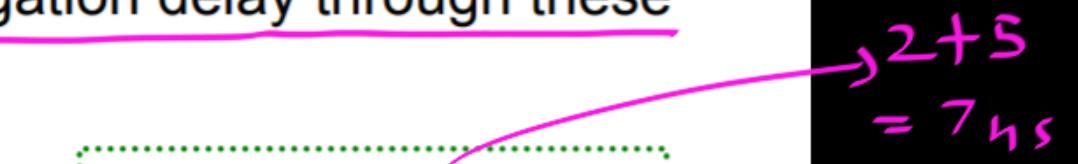
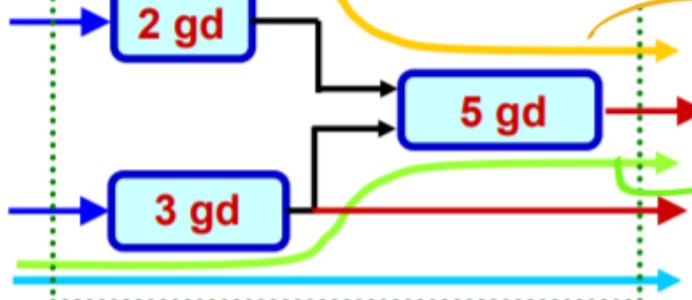
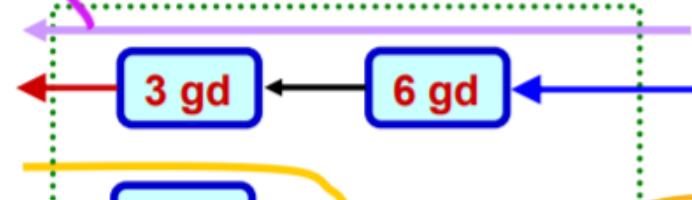
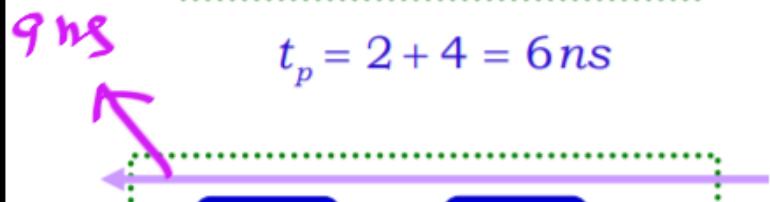
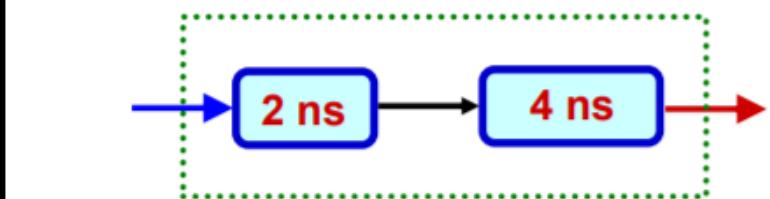
Delay =  $5 + 5 + 5$   
 $= 15 \text{ ns}$





# Example: Gate delay

- Determine the *worst case* propagation delay through these circuits.



$t_p = \max \{(2 + 5), (3 + 5), (3), (6 + 3)\} = 9 \text{ gd}$



Note:

wire Prop. delay , we Assume = 0





## Example :

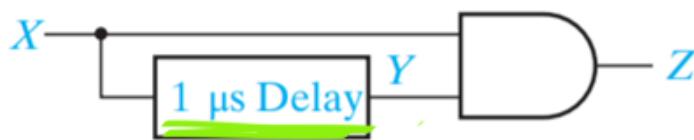
Figure 8-6 shows a timing diagram for a circuit with an added delay element.

The delay element has an output  $Y$  which is the same as the input except that it is delayed by 1 microsecond. That is,  $Y$  changes to a 1 value 1 microsecond after the rising edge of the  $X$  pulse and returns to 0 1 microsecond after the falling edge of the  $X$  pulse. The output ( $Z$ ) of the AND gate should be 1 during the time interval in which both  $X$  and  $Y$  are 1. If we assume a small propagation delay in the AND gate ( $\epsilon$ ), then  $Z$  will be as shown in Figure 8-6.

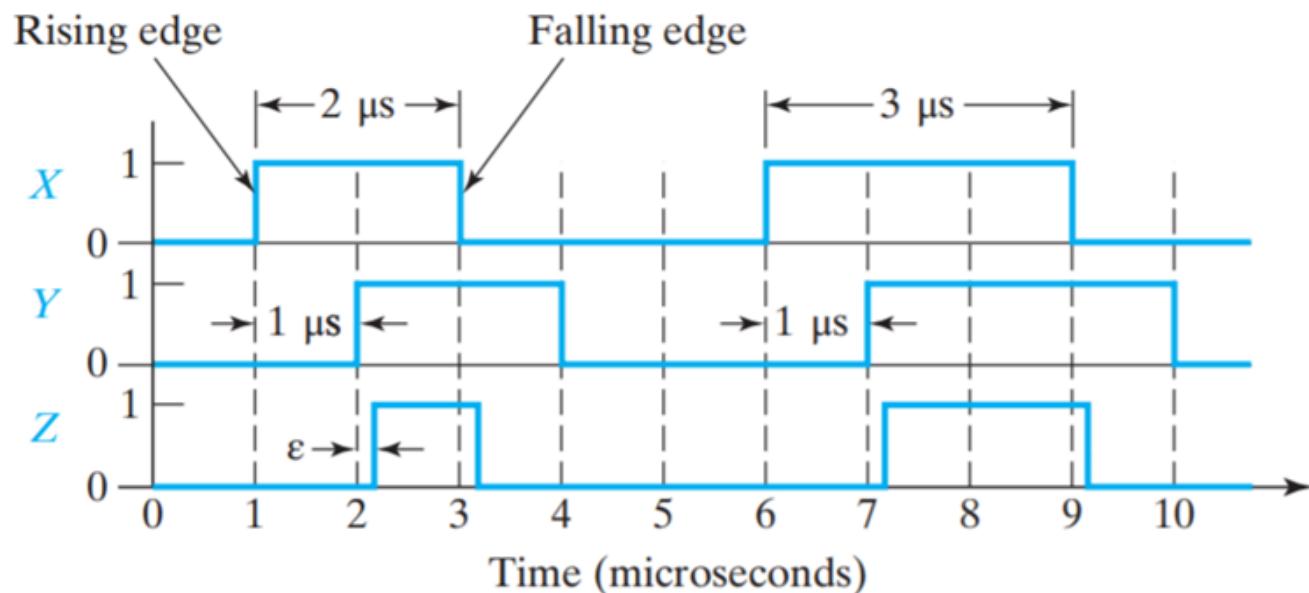


FIGURE 8-6 Timing Diagram for Circuit with Delay

$$Z = XY$$



$$Y = X$$



Waveform of  $Y = \text{Shift } X \text{ waveform by } 1 \mu\text{s.}$

