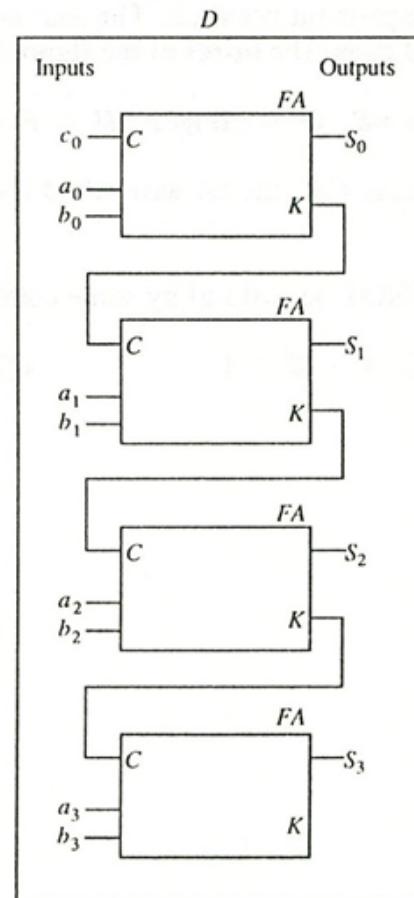
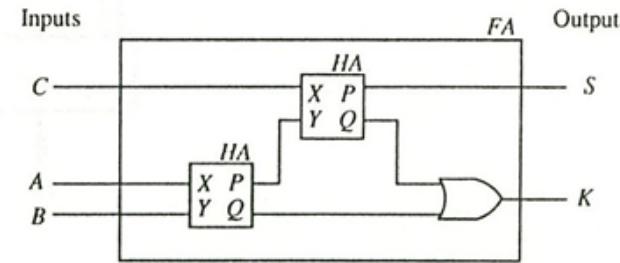
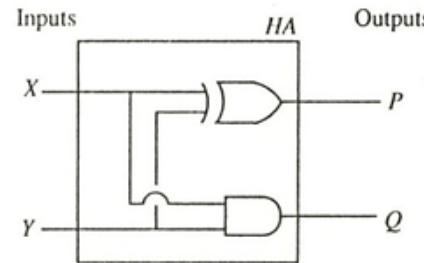


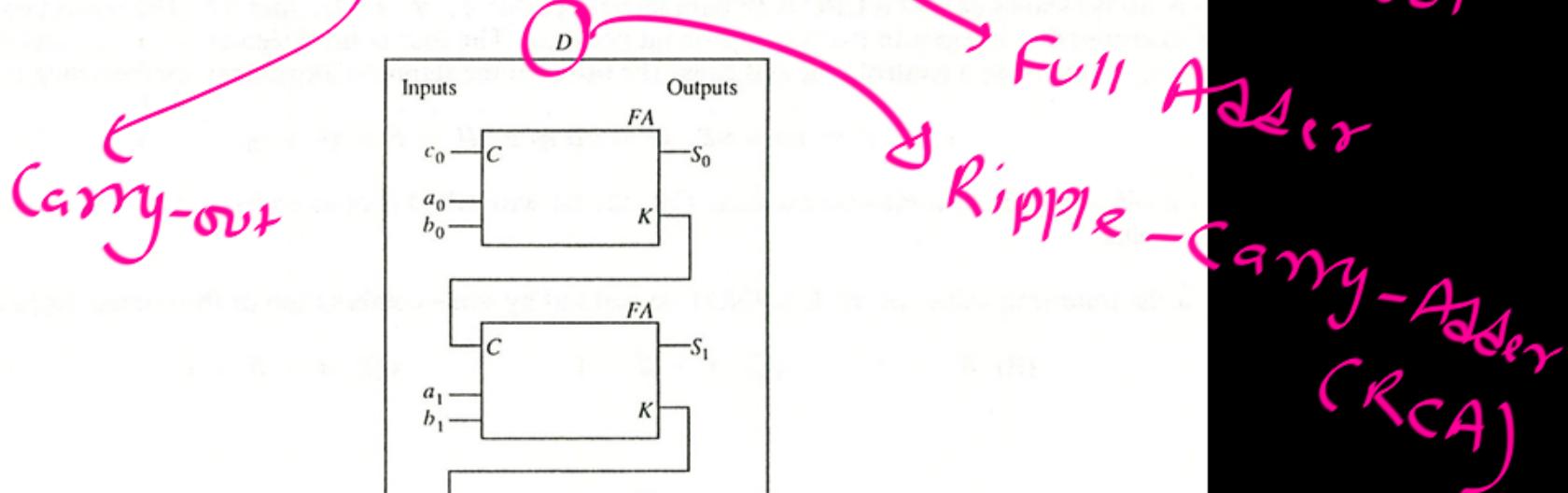
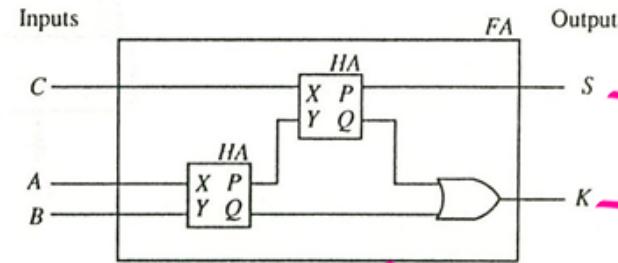
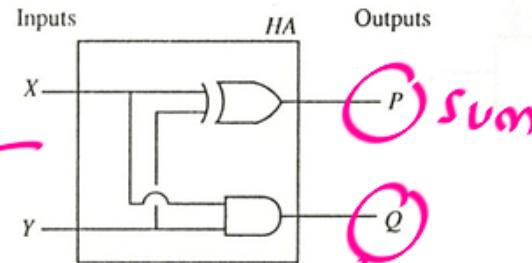
Q: → GRE Comp Sc. Exam

As shown in the three diagrams below, device FA makes use of Two copies of device HA, and device D makes use of four copies of device FA. Assume that all gates have the same delay T. If all inputs to device D become available simultaneously, what is the delay before S2 must be valid?

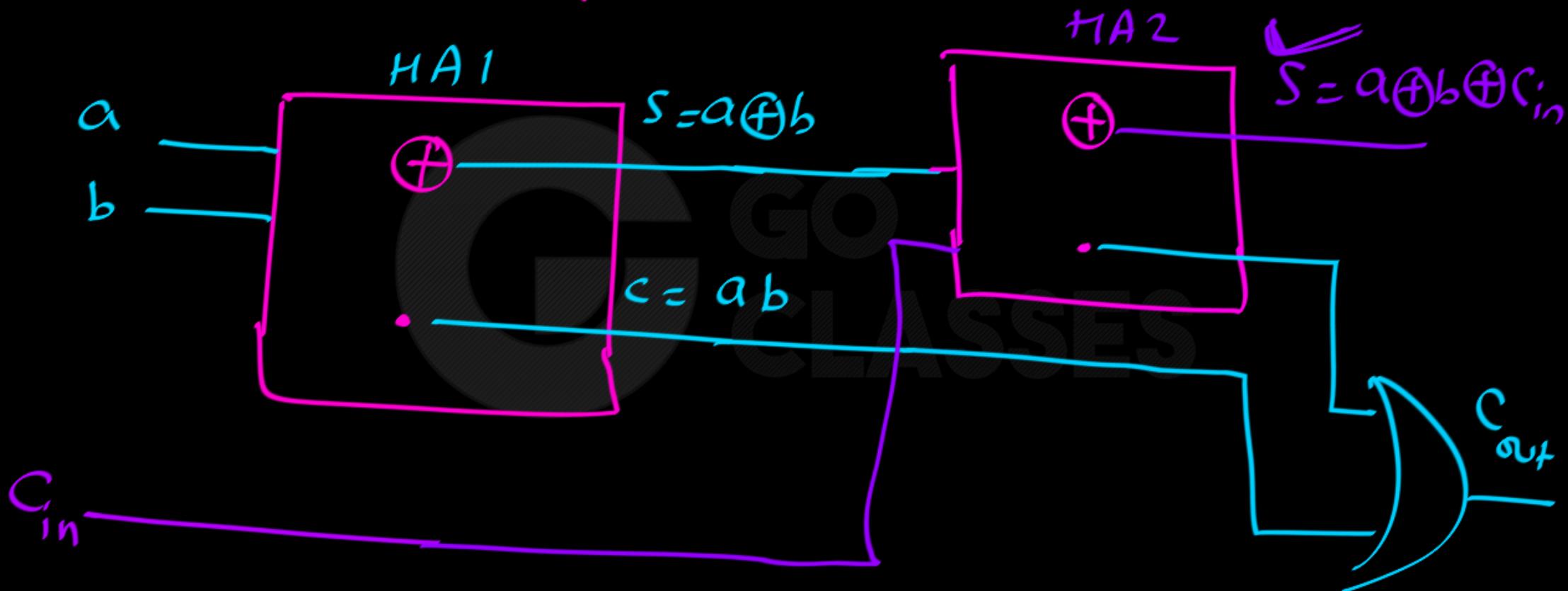
- A. 2 T
- B. 6 T ~~4~~
- C. 8 T
- D. 9 T



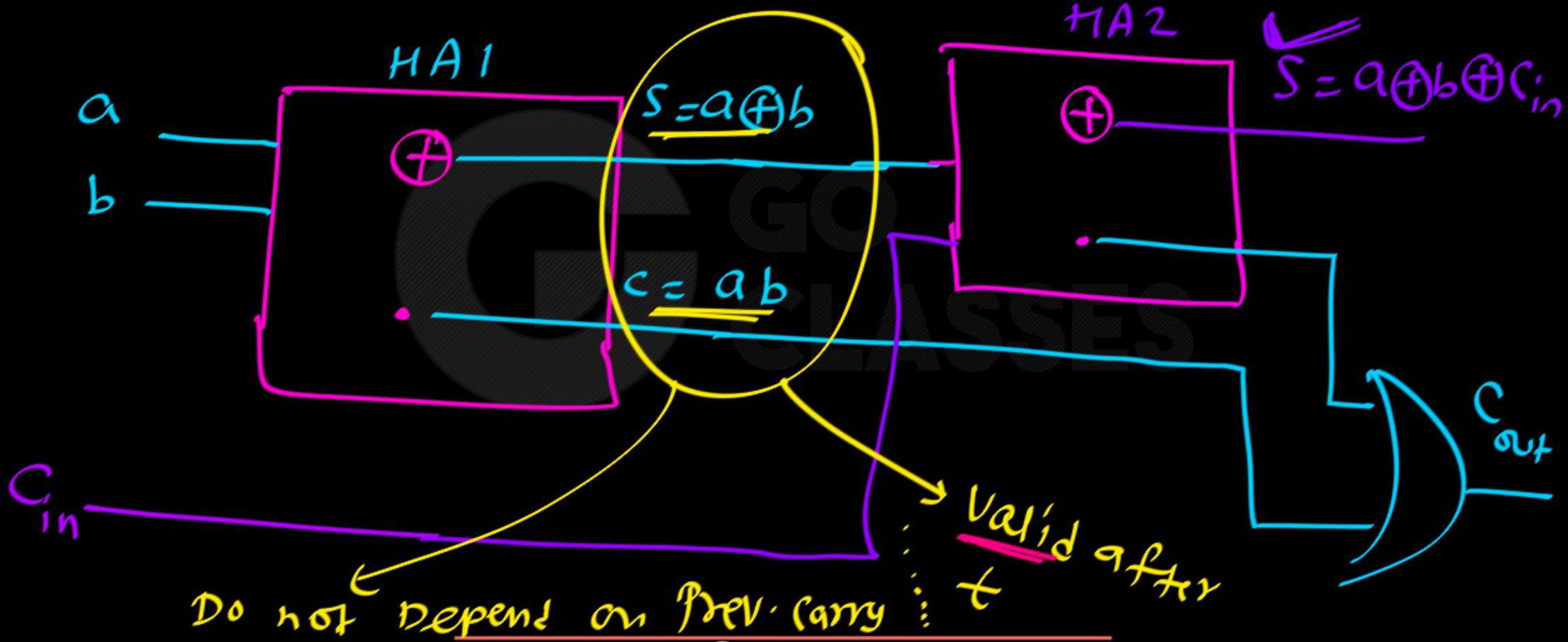
Half
Adder

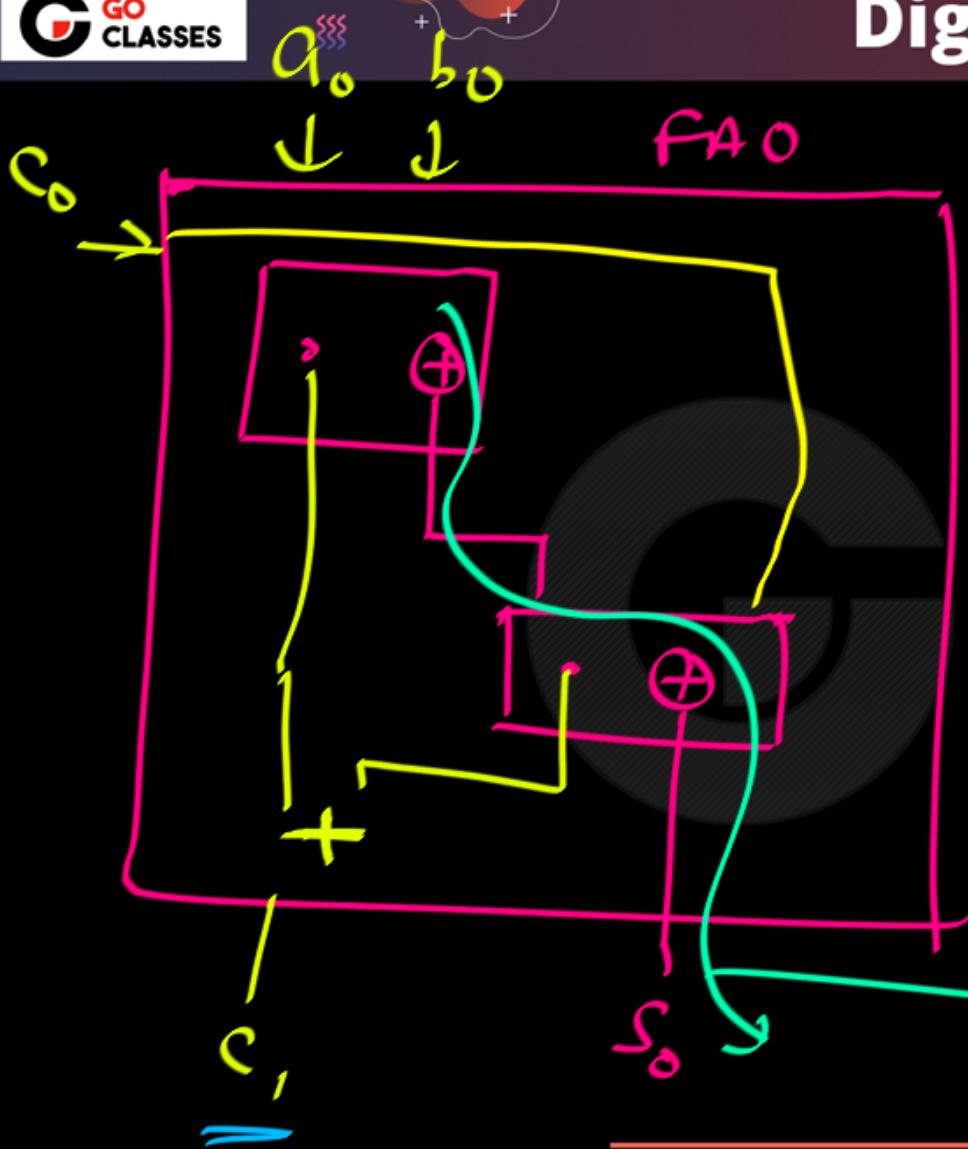


FA using 2 HA, 1 OR gate; Sum = a ⊕ b ⊕ c_{in}



FA using 2 HA, 1 OR gate; Sum = a ⊕ b ⊕ c_{in}





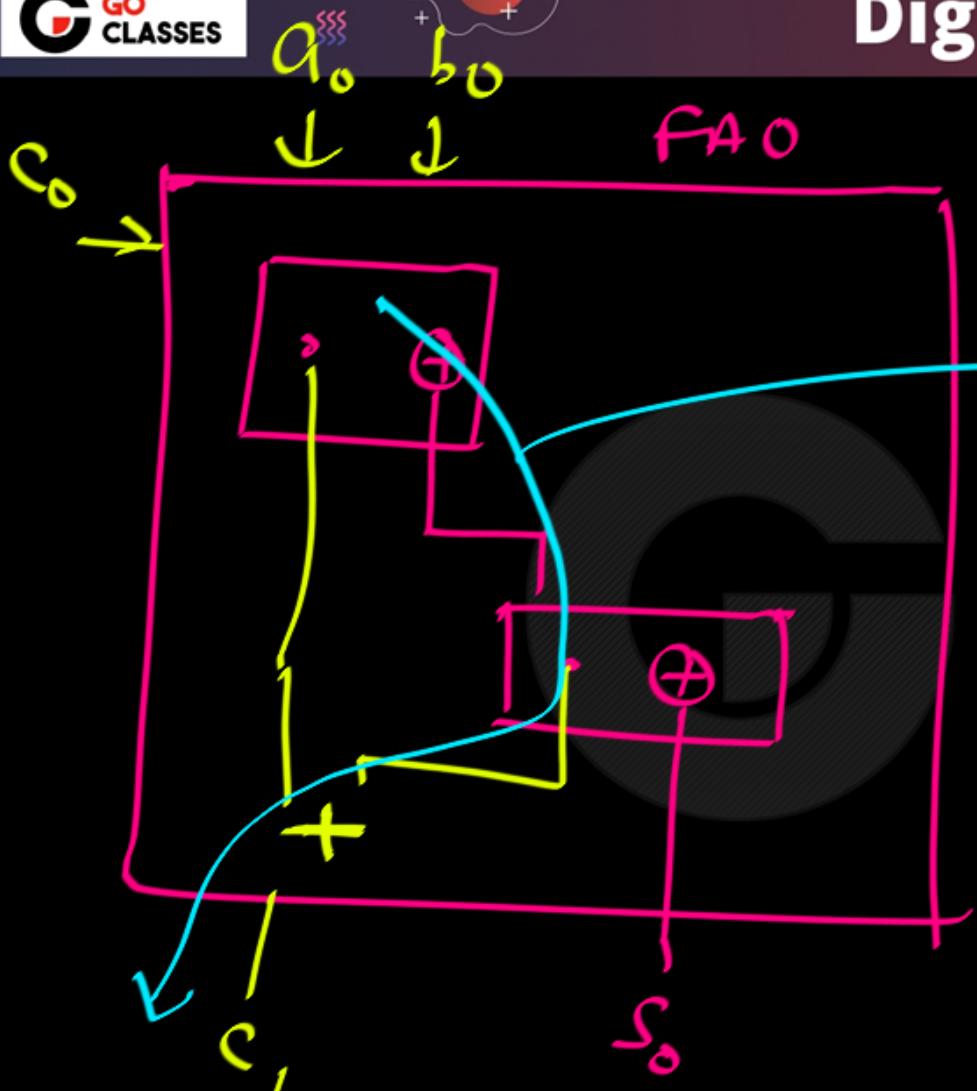
Critical Path for s_0 :

$$\underbrace{\oplus}_{\text{HA1}} \rightarrow \underbrace{\oplus}_{\text{HA2}}$$

Critical Path for c_1 :

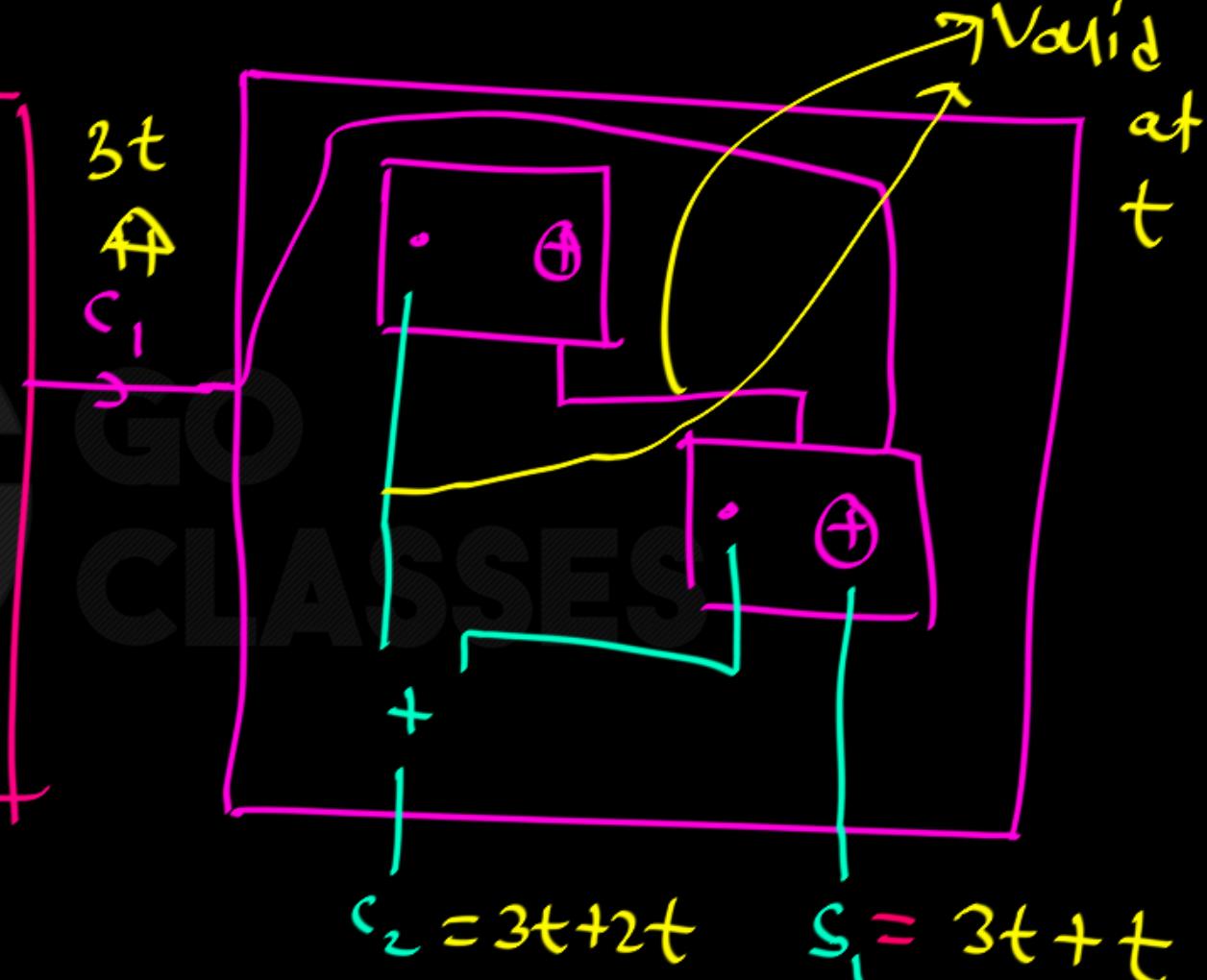
$$\underbrace{\text{EXOR}}_{\text{HA1}} \rightarrow \underbrace{\text{AND}}_{\text{HA2}} \rightarrow \text{OR}$$

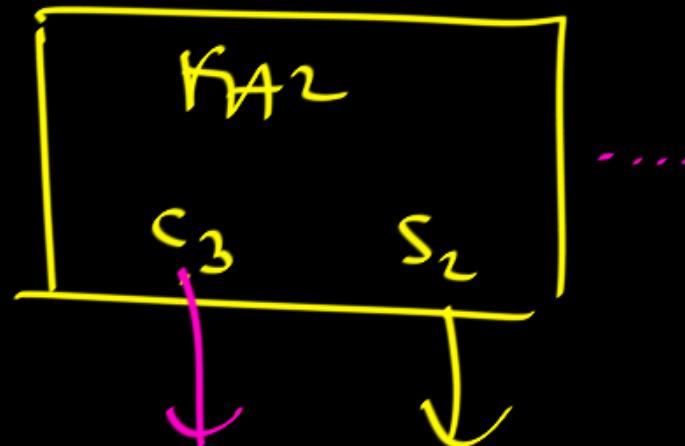
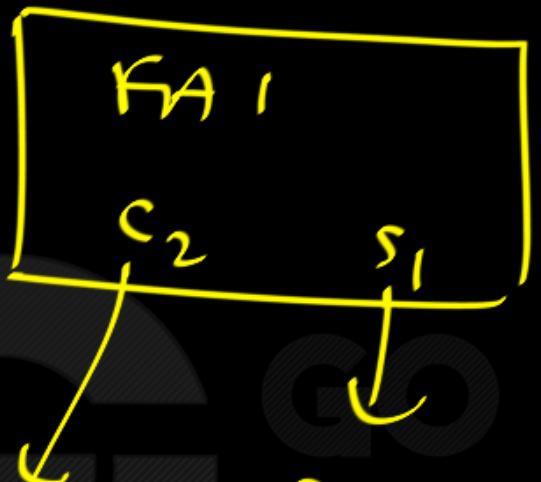
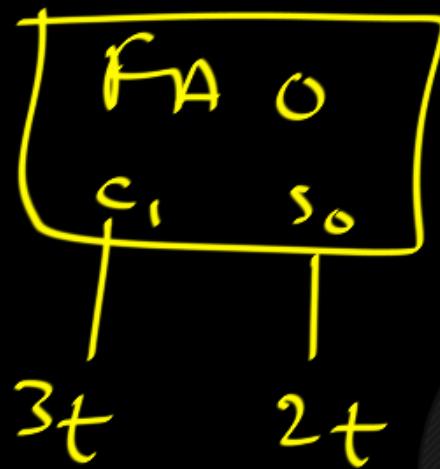
Critical Path for s_0
 $c_1 = a_0 b_0 + (a_0 \oplus b_0) c_0$



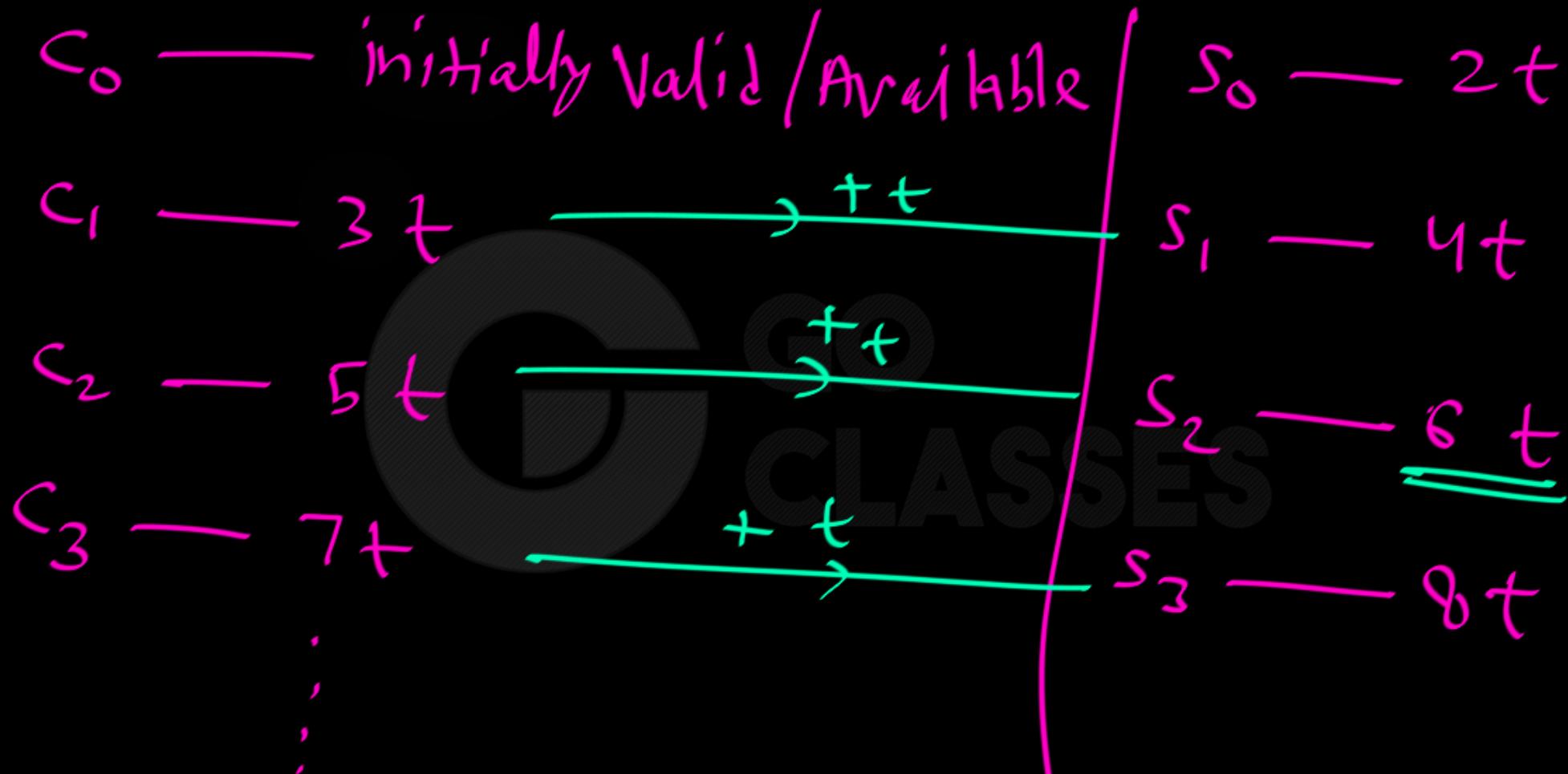
Critical Path for c_0

ExOR (H_A1) → AND (H_A2) → OR





$$\left\{ \begin{array}{l} Delay(c_2) \\ + Delay(c_1) \\ + 2t \end{array} \right\} + \left\{ \begin{array}{l} Delay(c_2) \\ + Delay(c_1) \\ + 2t \end{array} \right\}$$



So far ; we have seen Adder

for Unsigned Addition.

RCA { CLA }

If fan-in limited (fan-in = 4)
RCA $\Rightarrow \Theta(n)$ time ; CLA $\Rightarrow \Theta(\log n)$ time.

1's Comp Addition:

i/p : 1's Comp form
o/p : "

A + B

A + B = C

Input must
be provided
in 1's Comp

O/p must
be inter-
preted
in 1's Comp.

$$(+5) + (-3) \quad \text{Add} \quad \underline{+5, -3} \quad \text{Using } \underline{1's \text{ Comp}}$$

$$\begin{array}{r} +3 = 0011 \\ -3 = 1100 \\ \hline \end{array}$$

Diagram illustrating the addition of $+5$ and -3 using 1's complement:

The numbers are aligned vertically:

$+5$	0 1 0 1	-3
-3	1 1 0 0	
$\underline{\underline{+}}$		

A red circle highlights the first column where a carry is generated from the bottom row. A green arrow points from the bottom row's 1 to the top row's 1, indicating the propagation of the carry.

The result is shown as 0010 , with a green bracket below it labeled $+2$.

for +ve number x

1's Comp rep = binary of x

+5 → binary: 101

101 → -2
1's Comp



for +ve numbers ;

$$\underbrace{1's \text{ Comp Rep}}_{+5} = \underbrace{2's \text{ Comp Rep}}_{0101} = \underbrace{\text{Sign-mag. Rep.}}_{0101}$$

How to find 1's Comp of -ve numbers?

e.g:

- 6

$$\text{1's Comp } (-6) = \text{Comp.}(\text{1's Comp } (+6))$$

$$\begin{array}{r} 0110 \\ +6 \\ \hline \end{array} \rightarrow \begin{array}{r} 1001 \\ -6 \text{ in 1's Comp} \end{array}$$

2's Comp of Neg. number ; \Rightarrow 3 ways

Ex: $-6 \checkmark$

$$\begin{array}{r} \text{is Comp } (-6) \\ +1 \\ \hline 1010 \end{array}$$

$$\begin{array}{l} +6; \quad 0110 \\ -6; \quad 1010 \end{array}$$

$$\begin{array}{l} \text{Weighted code} \\ -6 = -8 + 2 \end{array}$$

$$\begin{array}{r} 1 \underline{0} \underline{1} \underline{0} \\ \downarrow \\ -8 \end{array}$$

1's Comp Addition: Given inputs in 1's Comp

$$\left\{ \begin{array}{l} \text{Adder } (\overbrace{A, B}) = I \\ \text{Adder } (I, \text{final carry}) = R \end{array} \right.$$

final result
(in 1's Comp)

Adder
RCA / CLA



1's Comp Addition using RCA:

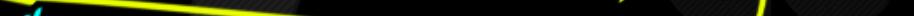
Given input in 1's Comp, A, B :

RCA(A, B) — $O(n)$ time

RCA(I, find carry) — $O(h)$ time

1's Comp Addition

10000 — -15

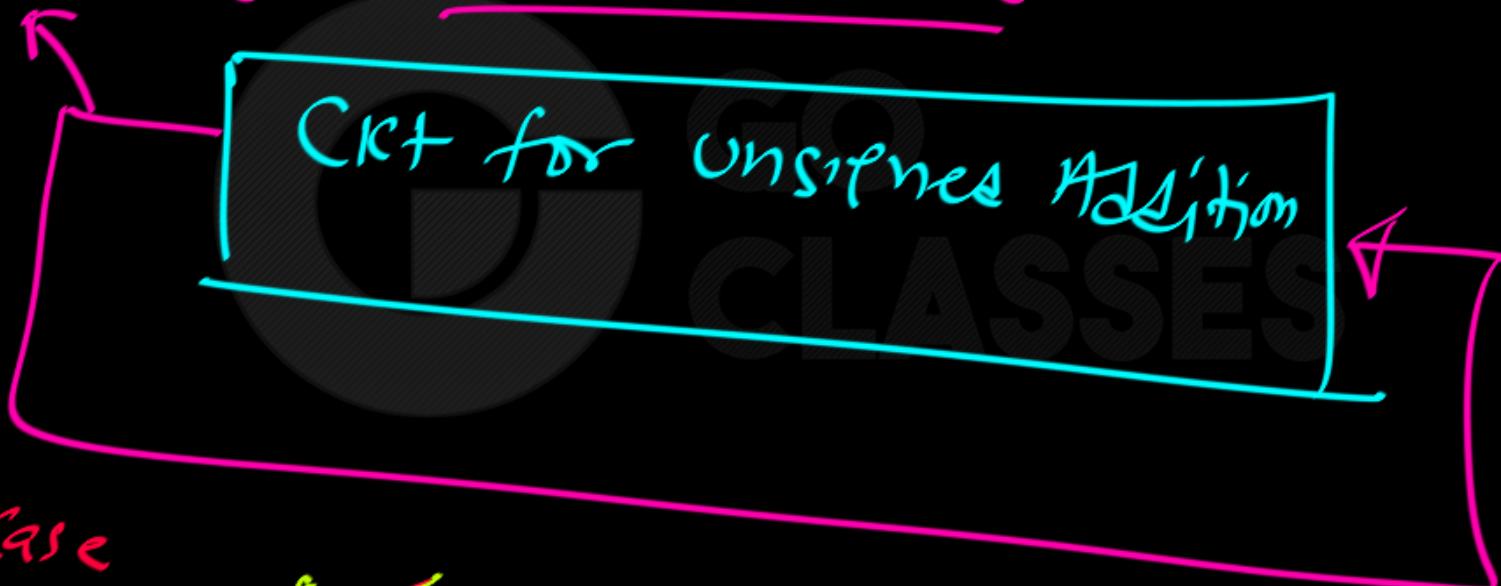
①  — $O(n)$ time

1 0 0 0 0 — $O(n)$ time

Final Result ✓

Circuit for 1's Comp Addition:

final carry = End Arrows carry



worst case
time: Double of Unsigned Addition

2's Comp Addition:

{ Given i/p in 2's Comp.
You need to do addition using the
(Unsigned) adder we have seen
⇒ Just Do it. (No additional work)}

In 2's Compj the End-Around carry is discarded.

So some (unsigned) adder CKT we can use for signed Addition in 2's Comp form.

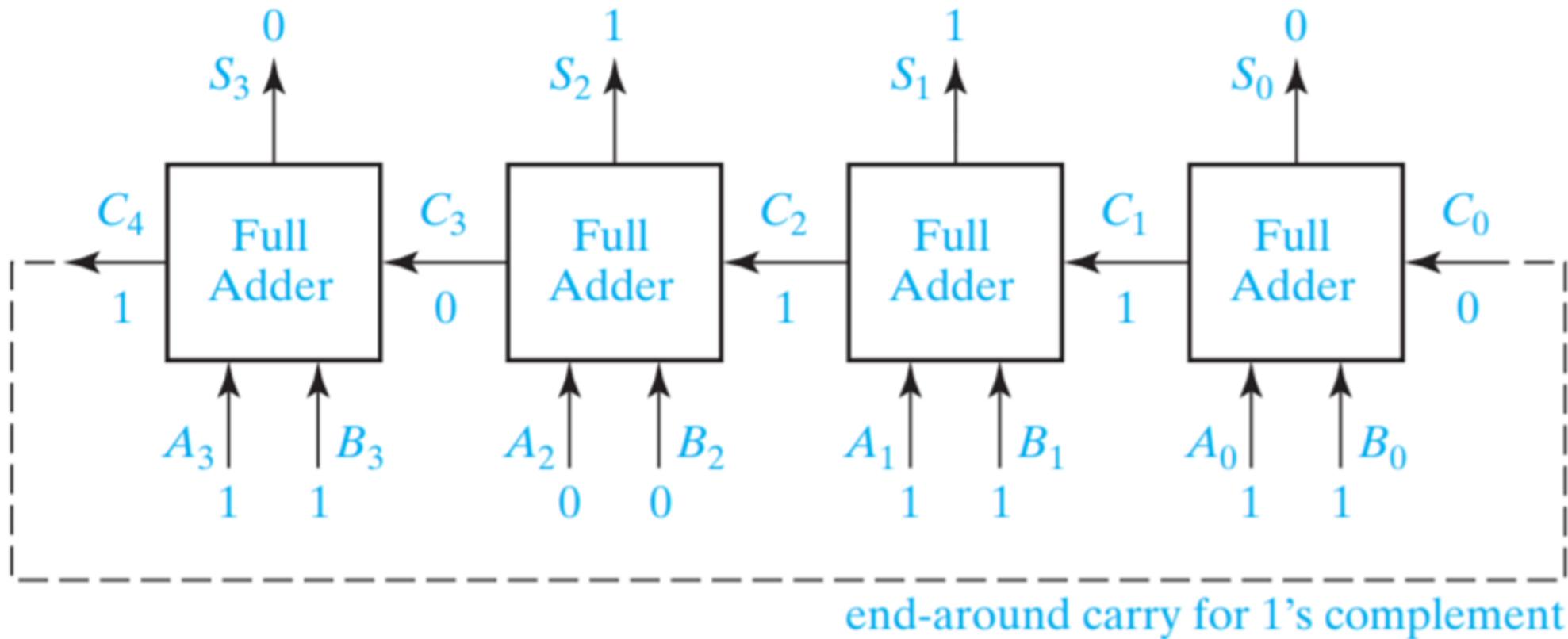


Signed Addition :

1's Comp Addition : Given two number in 1's comp form, add, and final carry is added back to the circuit.

2's Comp Addition : Given two number in 2's comp form, add, and final carry is discarded.

Ckt for 1's Comp Addition:





- ◆ The main reason for using 2's complement notation for signed numbers is that:

Signed and unsigned numbers can use
identical circuitry for add or subtract



To build a 4-bit adder from 1-bit full adders, we can connect four of these serially as shown here. It is important to appreciate that this 4-bit adder works for both signed and unsigned input, provided that signed numbers are using 2's complement representation. In other words, if you interpret input as unsigned 4-bit numbers, then the adder produces unsigned 5-bit output (including the carry out signal).

If you interpret the input as 2's complement signed numbers, then the output is correct as a 4-bit SIGNED output. (In this case, you cannot use C3 as the 5th bit).