RAMATENKI SHASHI KUMAR

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PROFILE

Hello,

I'm **RAMATENKI SHASHI KUMAR** , a recent Graduate of Bachelors in Technology, specialized in **ELECTRONICS AND COMMUNICATION ENGINEERING**, parallely I completed my 6 months **PHYSICAL DESIGN ENGINEERING,VLSI** Course at SumedhaIT in Kukatpally. I'm very Passionate and Dedicated Engineer. I always wanted to Start my Career in VLSI Industry, that interest pushed me to select **ECE** among various branches in Diploma as well as in Engineering. I started learning VLSI from different crash courses and finally landed in SumedhaIT, where Physical Design Engineering grabed my Focus and Interest. Finally, I want to be an Passionate & Hardworking Physical Design Engineer, and I would like to work in Creative and Challenging environment where there is scope for upgrading my Skills and Knowledge, would like to have an opportunity to contribute effectively in Organization to best of my knowledge. Thank you.

PROFESSIONAL SUMMARY

- Trained for 6 months on VLSI-Physical Design Course at Institute of Sumedha IT, Hyderabad.
- Comprehensive knowledge on Synthesis and STA.
- Hands-on experience in complete backend flow - Logical Synthesis, Floor Planning, Place & Route, Clock Tree Synthesis, Timing Closure, ECO flow.
- Have hands on experience on DRC, DRV fixes and basic understanding on Antenna, EMIR and LVS.
- Good in basics with TCL to handle various requirements in design.
- Ability to multi-task and flexibility to work in global environment.

ACADEMIC QUALIFICATION

Qualification	Specialization	University/Board	Institute	Year	CGPA/Percentage
B.Tech	ECE	JNTUH	Pallavi Engineering College	2023	67.4%
Diploma	ECE	SBTET	Govt. Polytechnic Medchal	2020	78%
Matriculation	SSC	TSBSE	Vijaya Ratna High School	2017	80%

TECHNICAL SKILLS

- CMOS Logic Design.
- Physical Design flow.
- SSTA.
- Digital Electronics.
- **Languages:** C, TCL, TCSH.
- **Operating System:** Linux/Unix , Windows.
- **TOOLS:** Design Compiler (Synopsis), Genus (Cadence), Innovus (Cadence)

TOOLS USED

Synopsys	Design Compiler & Prime Time
Floorplan, Place & Route	GENUS & INNOVUS
Timing analysis	TEMPUS
Scripting Language	TCL
Programming Language	Python

PROJECTS

Block-I

Technology Node : TSMC 28nm Tool : DC Compiler ,GENUS,INNOVUS

Number of clocks : 1 Macro count : 29

Description : Block level optimization which consists of 280K cells instances, operating frequencyz500Mhz (2ns)

Challenges :

- Executed a block independently from RTL to GDSII.
- Proper macro placement at Floor planning for minimal congestion issues and better PG planning for minimal IR drop without any PG DRCs.
- Analyzed congestion maps and performed different techniques like placement blockages and Cell padding
- Clock tree synthesis using CCD and Independently performed ECO fixes for setup and hold violations to meet the timing.

Block-II

Technology Node : TSMC 28nm Tools : DC Compiler ,GENUS,INNOVUS

Number of clocks : 2

Description : Block level Physical Design consisting of gate count 421, operating on a Clock frequency of 200MHz.

Challenges :

- Involved in RTL synthesis flow to generate Gate Level Netlist.
- Validate the timing constraints, perform sanity checks, to synthesize the RTL.
- Applied path groups for timing critical paths and improved timing Qor.

Block-III

Technology Node : TSMC 28nm Tools: DC Compiler ,GENUS,INNOVUS

Number of clocks : 1 Macro count : 6

Description : Block level Physical Design consisting of gate count 60k, operating on a Clock frequency 400MHz.

Challenges:

- Executed a block independently from RTL to GDSII
- Creating bounds, analyzed congestion map and performed incremental placement optimization techniques
- Clock-tree building is done with NDR to make sure proper clock is reaching to all the sequential cells and to minimize the skew.

ACADAMIC PROJECTS

- **Automated paralysis patient care system**
  Developed an Automated Paralysis Patient Care System to monitor patient health and provide timely assistance through automated mechanisms. Integrated sensors for vitals tracking and an alert system for emergencies. The project aimed to enhance the quality of care and improve response times for paralyzed patients.

- **Fruit disease detection using image processing**
  Designed a Fruit Disease Detection system using image processing techniques to identify and classify diseases in fruits. Implemented algorithms for image segmentation and feature extraction to detect patterns indicative of diseases. The project focused on early detection to minimize crop loss and improve agricultural efficiency.

CERTIFICATION

- BASIC STATIC TIMING ANALYSIS – CADENCE
- ADVANCE EMBEDDED TECHNOLOGY -CITD

LANGUAGES

- ENGLISH
- HINDI
- TELUGU

DECLARARTION

I do hereby declare that the above particulars of facts and information stated are true, correct and complete to the best of my belief and knowledge.

Place: Hyderabad RAMATENKI SHASHI KUMAR