Silicon
https://doi.org/10.1007/s12633-023-02755-2

RESEARCH

Improved Switching and Analog/RF Behaviour of SiGe Heterojunction Dielectric Modulated Dual Material Nano Silicon Tunnel FET for Low Power Applications

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Received: 10 August 2023 / Accepted: 2 November 2023

Abstract
In the present work, an optimization technique of dielectric material and gate metal for the Silicon Tunnel Field Effect Transistor (Si TFET) is proposed in order to increase the coupling of the electric fields along the channel, i.e., to enhance the electrical properties. This investigation delineates a methodology for alleviating the ambipolar phenomenon and enhancing the on-state current in Tunnel Field-Effect Transistors (TFETs) through the utilization of the advantageous properties provided by a low bandgap material layer positioned proximate to the source region. To decrease the depletion region width a heavily doped $Si_{0.6}Ge_{0.4}$ material layer is deposited in channel at source channel junction which in turn boost the ON current. The ON current equals 8.16×10^{-4} A/μm and the OFF current equals 5.62×10^{-18} A/μm is achieved. Constant current approach is used for threshold voltage extraction and the device's performance is examined for low power applications as well. A diverse set of performance metrics, including analog and RF parameters i.e., on–off ratio (I_{ON}/I_{OFF}), transconductance (g_m), parasitic capacitances (C_{gd} and C_{gs}), cut-off frequency (f_T), and gain band-width product (GBW) also assessed and compared with single metal gate double gate Tunnel Field Effect Transistor (SMG-DGTFET), single metal gate hetero dielectric double gate Tunnel Field Effect Transistor (SMG-HD DGTFET) and dual metal gate hetero dielectric double gate Tunnel Field Effect Transistor (DMG-HD DGTFET) structures. Enhanced on-off ratio 1.45×10^{14} reported for suggested device. Gain bandwidth product 14.7 GHz and device cut-off frequency 80.5 GHz were also obtained. Also, the improvement in TGF and TFP was reported by 12.3% and 24.1%, respectively.

Keywords Hetero-dielectric material · Dual metal gate (DMG) · Tunnel FET · Band to band tunnelling · SiGe · Silicon materials

1 Introduction

Miniaturization has led to a shrinkage in the size of silicon materials to the nanoscale dimensions [1]. According to the International Roadmap for Devices and Systems (IRDS), the implementation of Moore's scaling encounters substantial challenges in technical nodes below 22 nm [2]. The field of nanoscale semiconductor devices has seen rapid development in the recent few of decades and their performance is approaching to the optimum level. But constant energy crunch enforced the researchers to introduce some potent alternatives [3–6]. But short channel effects and higher leakage current restricted the performance of devices. So, the tunnel field effect transistor was introduced as an alternative to the MOS's inherent scaling problems. TFET has gained significant traction in the semiconductor industry due to its novel properties lower leakage current and lesser

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Published online: 14 November 2023

subthreshold swing (< 60 mV/decade), as it was not possible with MOSFET. Aside from these benefits, it exhibits two significant deficiencies, low on current and ambipolarity i.e., it can conduct for high positive and negative gate bias both. To control ambipolar behaviour [7, 8] and to increase the on current Dielectric engineered, Gate engineered and Bandgap engineered techniques had been adapted. Researchers had explored many techniques through proposing several architectures to increase the device reliability [9–11]. Few eminent works have premised on using high-k dielectric materials [12–14], hetero-dielectric materials [15, 16], Dual [17–20] and triple material gate [21, 22], III-IV group compound materials near source i.e., hetero-junction TFETs [23–34], L-shaped gate TFET [35, 36], TFET on SELBOX [37], to obtain the preponderate characteristics. Based on the WKB approximation, the tunnelling probability has been derived as;

$$T(E) \propto \exp\left(-\frac{4\sqrt{2m^*}\left(E_g^{\,3}/2\right)}{3q\hbar\left(E_g+\Delta\Phi\right)}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}}t_{ox}t_{Si}\right)\Delta\Phi \quad (1)$$

The Eq. (1) implies that the tunnelling rate could be maximised using high-k dielectrics. The doping concentration and dimensions of the device affect I_{ON} and tunnelling width [23, 24]. Higher doping and lower band gap material at source channel junction enhance the I_{ON} and current on-off ratio. Hetero-dielectric material has been investigated for use, wherein a high-k dielectric material is utilized in the vicinity of source side to enhance the I_{ON}, while a low-k material is employed in proximity to the drain side to mitigate ambipolarity [16]. Boucart et. al. [12] explored Double gate TFET (DGTFET) using high-k dielectric material and reported the improved device characteristics as higher on current, subthreshold swing and I_{ON}/I_{OFF} ratio. Kavalieros et al. [14] demonstrated the benefits of high-k materials with tri-gate transistors for achieving enhanced device performance and to control the short channel effects. Choi et al. [16] proposed hetero-dielectric tunnel FET (HD DGTFET) and reported using heterogeneous dielectric materials suppressed the ambipolar current significantly due to which the abrupt transition between on-off states is achieved. Pravin et al. [19] presented dual material gate JLMOSFET with different high-k dielectrics for low powered applications. Their study revealed that the use of dual metal gate together with high-k dielectrics has a positive impact on the device transconductance and TGF, eventually leading to a reduction in power consumption in circuits at the nanoscale level. Priya et al. [17] presented effect of dual metal gate in junctionless TFET (DMDG JLTFET) reported reminiscent reduction of SCEs. Ahish et al. [24] illustrated heterojunction DG tunnel FET (H-DGTFET). They introduced narrow bandgap (III-V group) material at source-channel junction and examined the improved RF performance of device. Goswami et al. [34] carried an analysis on the performance characteristics of a p-i-n tunnel field-effect transistor (TFET) in comparison to a silicon-on-insulator (SOI) double gate TFET with an L-shaped gate configuration, incorporating a back gate. Their study revealed that the SOI DG-TFET possesses a strong ON state current and a steep SS, made it suitable for low power applications. Barah et al. [36] suggested the use of a tunnel FET on a substrate consisting of SELBOX. The investigation revealed that the implementation of SELBOX as a substrate material yields a notable reduction in the OFF current, while leaving the ON current unaffected.

Hence, to increase the reliability we presented a double gate TFET that uses dual metal hetero dielectric with Silicon-Germanium ($Si_{1-x}Ge_x$) pocket at source-channel interface (SiGe-DMG-HD DGTFET). The device performance for single metal gate with high-k dielectric (SMG-DGTFET), single metal gate with hetero dielectric (SMG-HD DGTFET), dual metal gate with hetero dielectric (DMG-HD DGTFET) has been investigated along with the proposed structure. Analog/RF performance along with important FOMs is also assessed and compared with other structures. Low bandgap material at source channel interface reduces the subthreshold slope, improving I_{ON}/I_{OFF} ratio, I_{ON} and I_{OFF} of proposed device. Impact of length (L_1) and mole fraction (x) variations on transfer characteristics with miller capacitance (C_{gd}), gate to source capacitance (C_{gs}), transconductance (g_m) and various possible RF parameters also been assessed and analysed.

2 Si Tunnel Fet Structure and Simulation Setup

Schematic views of all TFET structures i.e., SMG-DGTFET, SMG-HD-DGTFET, DMG-HD-DGTFET and SiGe-DMG-HD-DGTFET are depicted in Fig. 1. For SMG double gate TFET dielectric HfO_2 ($\varepsilon = 21\varepsilon_0$) with metal gate work function 4.12 (it relates to Indium, In). is used. Hetero TFET structures consist of the combination of high-k dielectric HfO_2 near source side and SiO_2 at drain side with tunnelling gate work function $M_1 = 4.0$ eV (it relates to Tantalum,Ta) and auxiliary gate work function $M_2 = 4.4$ eV (it relates to Tin, Sn). Proposed structure amalgamates the benefits of using two metal gates (M_1 and M_2) and hetero gate dielectrics with SiGe pocket at source/channel interface. Pocket length (L_p) = 1 nm is selected to optimise the designed structure characteristics. To suppress ambipolar issues source and drain are asymmetrically doped. The design parameters used are given as channel length (L_g) = 50 nm, body thickness

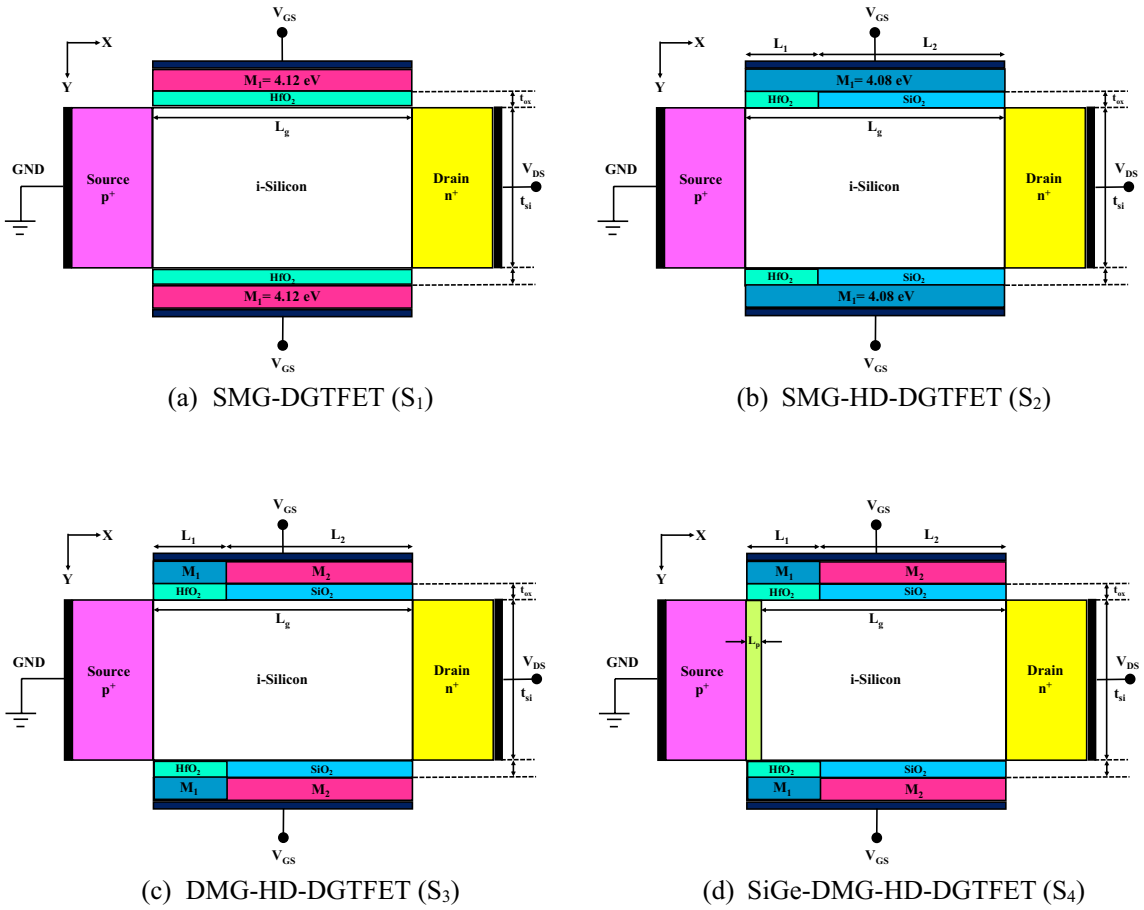


Fig. 1 Schematic diagrams of **a** SMG-DGTFET **b** SMG-HD-DGTFET **c** DMG-HD-DGTFET and proposed structure **d** SiGe-DMG-HD-DGTFET

(t_{si}) = 10 nm, oxide thickness(t_{ox}) = 3 nm, n^+ SiGe pocket length (L_p) = 1 nm, pocket doping = 10^{19}/cm^3, source doping = 10^{20}/cm^3, drain doping = 5×10^{18}/cm^3, channel doping = 10^{15}/cm^3, tunnel gate length (L) = 6 nm, auxiliary gate length (L_2) = 44 nm, tunnelling gate work function (Φ_{M1}) = 4.0 eV, auxiliary gate work function (Φ_{M2}) = 4.4 eV. All the structures have been optimised for threshold voltage equals to 0.22 V. To keep the threshold voltage same, work functions of SMG-DGTFET and SMG-HD-DGTFET are kept as 4.12 eV and 4.08 eV(it relates to Aluminium, Al). respectively. All simulations have been performed on 2-D ATLAS by Silvaco International [38] with its default parameters. The nonlocal BTBT model which depends on band diagram calculation and uniform doping profile were invoked for simulations. Along with band gap narrowing model, other physical models such as Fermi-Dirac statistics (FERMI) model, recombination (SRH) model [30], field dependent mobility (FLDMOB) model, concentration dependent (CONMOB) model have been incorporated. The design parameters of all stated structures for simulation are summarised in Table1.

Table 1 Dimensions of S_1, S_2, S_3 and S_4 structures

Parameters	Symbol	Values
Body thickness (nm)	t_{si}	10
Source Doping (cm^{-3})	N_A^+	1×10^{20}
Drain doping (cm^{-3})	N_D^+	5×10^{18}
Channel doping (cm^{-3})	N_A	1×10^{15}
Length of channel (nm)	L_g	50
Length of high-k dielectric (nm)	L_1	6
Length of S_iO_2 (nm)	L_2	44
Gate length under metal M_1 (nm)	L_1	6
Gate length under metal M_2 (nm)	L_2	44
Oxide thickness (nm)	t_{ox}	3
Tunnelling Gate Work function (eV)	Φ_{M1}	4
Auxiliary Gate Work function (eV)	Φ_{M2}	4.4

The integration of the process flow previously described for asymmetric dielectric [39] and gate materials [40, 41] may be utilized to fabricate DMG HD DGTFET. The complexity and challenges associated with the device

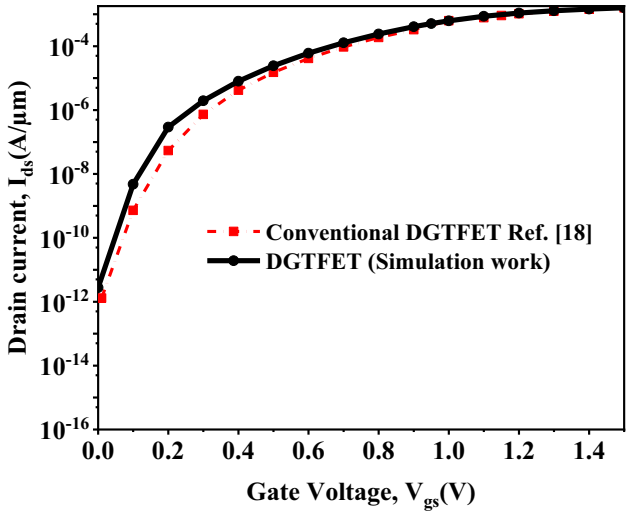


Fig. 2 Calibration of the double gate tunnel FET model used in simulation work with ref. [18]

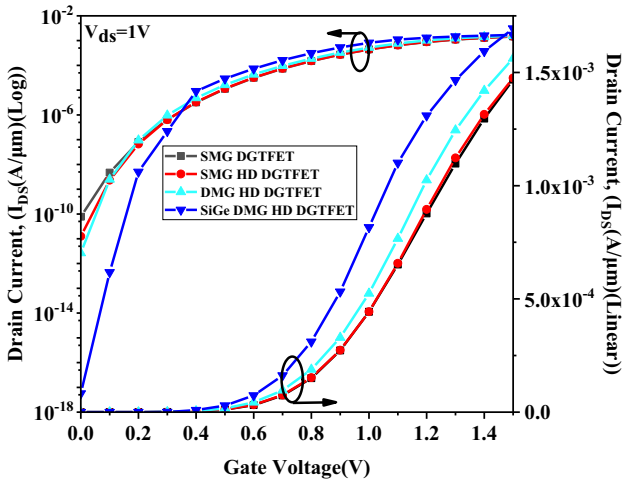


Fig. 3 I_d-V_{gs} characteristics of S_1, S_2, S_3 and S_4 structures in on state i.e., V_{gs} = 1.5 V and V_{ds} = 1 V

processing are expected to be overcome by employing HD DGTFET process steps, as well as the stated technique for DMG FETs. The device model utilized in this study has been calibrated with reference to the source cited as [18], and the resulting calibration curve is represented in Fig. 2. Similar parameters were selected for the purpose of calibration.

3 Result and Discussion

3.1 DC Characteristics

The transfer characteristics of stated TFET structures are compared in Fig. 3. The SiGe-DMG-HD-DGTFET structure exhizbits superior on-current and lesser off-current as compared to others, as evidenced by simulation results. The increased ON and OFF current observed in the proposed structure can be attributed to the presence of SiGe material layer and dual metal gate respectively. These components contribute to both vertical and lateral BTBT effects, as well as band gap narrowing.

Table 2 shows the comparative analysis of proposed structure and other TFET structures across multiple performance parameters. It can be depicted that SiGe-DMG-HD-DGTFET gives better ON and OFF current as compared to others, which can be validated through surface potential plots of all structures in Fig. 7. Hence, higher I_{ON}/I_{OFF} ratio (10^{14}) has been obtained which is quite adequate for digital applications. Low threshold voltage (0.22 V) is also favourable for low power applications. However, SMG-DGTEFET and SMG HD-DGTFET provides better subthreshold swing. Due to presence of doped pocket at source slope of transfer characteristic is reduced, which in turn increases the SS in SiGe-DMG-HD-DGTFET.

In this study, we investigate the impact of varying the drain bias, Vds, on the drain characteristic of a SiGe DMG-HD DGFET with a pocket length of 1 nm. When the drain bias is raised, the Fermi potential also increases, leading to a steady decrease in the inversion charge in the channel and an increase in the emergence of BTBT (band-to-band tunneling) owing to the enhanced electric field. This phenomenon exhibits similarity to the amplification of gate voltage V_{gs}, particularly noticeable when the device is OFF. During ON condition, the increased gate biasing effectively improves the impact of BTBT, serving as the regulating parameter. Consequently, the drain bias is not the sole reason for boosting the current. The V_{ds}-dependent transfer characteristics (I_d-V_{gs}) of suggested

Table 2 Comparison of Analog performance parameters of various TFET structures

Different TFET structures	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/I_{OFF}	SS (mV/decade)	V_{th} (V)
SMG DGTFET	4.43×10^{-4}	7.75×10^{-11}	5.72×10^{6}	17	0.221
SMG-HD DGTFET	4.44×10^{-4}	1.26×10^{-11}	3.53×10^{7}	22	0.221
DMG-HD DGTFET	5.24×10^{-4}	2.26×10^{-12}	1.97×10^{8}	29	0.221
SiGe DMG-HD DGTFET	8.16×10^{-4}	5.62×10^{-18}	1.45×10^{14}	48	0.224

design (SiGe-DMG-HD-DGTFET) are depicted in Fig. 4. It depicts the minimal variation in I_d with the increase in the V_{gs}, suggesting effective regulation of the gate during tunnelling. In Table 3 variation in V_{th} with varying drain bias is mentioned which clearly depicts a minimal variation in V_{th} as the gate voltage is increased.

One significant obstacle in achieving scalability of MOSFETs is the occurrence of Drain Induced Barrier Lowering (DIBL) phenomenon, which may be mathematically expressed as

$$DIBL = \frac{V_{th1} - V_{th2}}{V_{ds2} - Vds_1} \tag{2}$$

The drain-induced barrier lowering (DIBL) was determined by measuring the drain bias at two different levels: 0.3 V (as Vds1) and 1.0 V (as Vds2). The measured value is determined to be 2.5 mV/V.

The energy diagram of the pocket doped DMG-HD-DGTFET design is depicted in Fig. 5 b. Figure 5 a compares the energy diagram of proposed design with other conventional structures. At a gate voltage, $V_{gs} = 0$ V and a drain-source voltage, $V_{ds} = 1$ V, the tunnelling barrier is wider between the source and channel region. Consequently, the initial absence of tunnelling probability of charge carriers from the source's valence band to the channel's conduction band results in the device being in the OFF-state. As the gate voltage, V_{gs} is raised to 1 V, the tunnelling barrier will decrease in width, allowing for the transfer of charge carriers. This will result in a significant hike in the tunnelling current. Therefore, turns on the device as illustrated in Fig. 5 b.

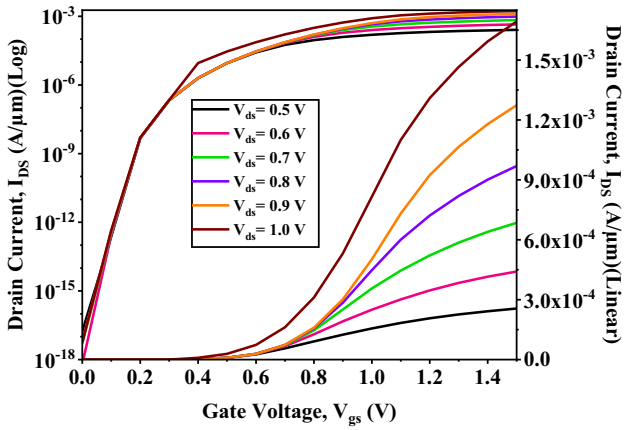


Fig. 4 Drain voltage (V_{ds}) dependent transfer characteristics of SiGe-DMG-HD-DGTFET

Figure 6 points out the transfer characteristics of SiGe layered double metal tunnel FET in context with high-k dielectric length (L_1) variation. The DMG-HD DGTFET is proposed with a variable SiO_2 length ranging from 0 to 50 nm. A comparison is drawn between the drain current of a proposed SiGe DMG-HD DGTFET with $L_1 = 6$ nm and L_1 equals to 0 nm, 16 nm and 50 nm. The proposed DMG-HD DGTFET ($L_1 = 6$ nm) exhibits a drain current of 8.16×10^{-4}A/μm, while with length 0 nm, 16 nm, 25 nm and 50 nm the it displays drain current 3.75×10^{-6}A/μm, 5.64×10^{-4}A/μm and 5.64×10^{-4}A/μm respectively, as shown in Table 4. The observed improvement can be ascribed to a decrease in the tunnelling energy gap due to HfO_2 in the source/channel junction, with an increase in the tunnelling energy gap by SiO_2 in the channel/drain junction. The proximity of the L_1 to the source results in a lower OFF current in comparison to the others. The lack of available electrons for current conduction can be attributed to their confinement within the unoccupied density of states that is formed at the tunnel junction [36]. Inadequate density of states at the tunneling junction for the tunneling electrons will occur when Length L1 is increased. The unconfined electrons exhibit a high susceptibility to the drain voltage, resulting in an escalation of the I_{OFF}. The lowest OFF current of 5.62×10^{-18}A/μm is achieved when the length L_1 is 6 nm (Fig. 7).

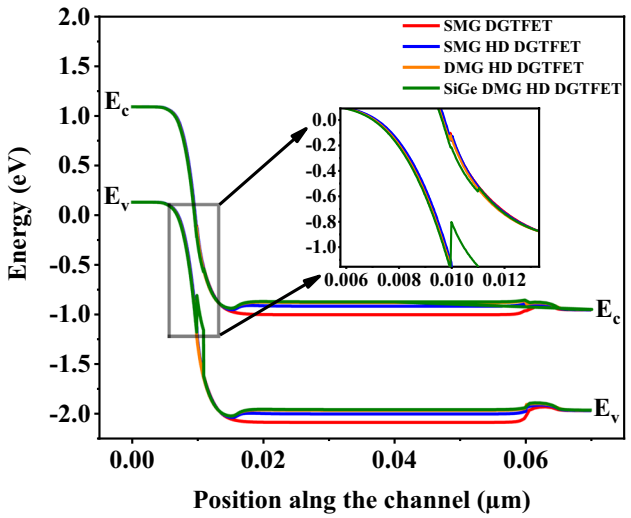
It can be inferred that a significant reduction in the length (< 6 nm) of high-k on the source side brought a considerable decrease in the on-current.

$Si_{1-x}Ge_x$ pocket was added to DMG-HD-DGTFET to enhance the drive current. The alteration of the bandgap and band alignment in heterojunctions of SiGe semiconductors may be readily achieved by altering the mole-fraction of germanium [42]. The effective bandgap in the heterojunction TFET is considerably reduced as a result of the alignment of the bands in the source and the channel. Nevertheless, as a result of the larger bandgap present in the channel, the off-state current (I_{OFF}) of the Tunnel Field-Effect Transistor (TFET) is maintained at a low level. This effectively optimizes both the on-state current (I_{ON}) and the off-state current (I_{OFF}) concurrently.

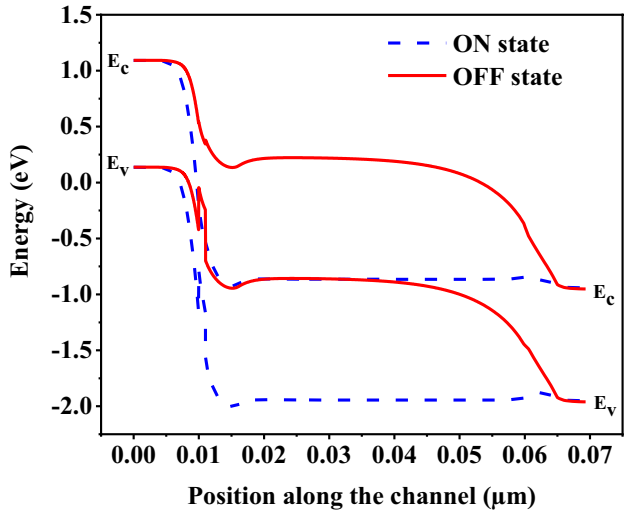
The length of the pocket is adjusted within the range of 0 nm to 3 nm in order to achieve optimal operation for the device. Figure 8 illustrates the impact of variations in pocket length. The graph clearly demonstrates that as the pocket length is increased by 1 nm, there is an apparent decrease in

Table 3 Effect of Drain voltage, (V_{ds}) variation on threshold voltage, (V_{th})

V_{ds} (V)	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
V_{th} (V)	0.226198	0.225691	0.2254	0.225043	0.224812	0.224577	0.224339	0.224124



(a)



(b)

Fig. 5 **a** Energy diagram of S_1, S_2, S_3 and S_4 structures and **b** SiGe DMG-HD TFET for ON state ($V_{gs}=1.5$ V, $V_{ds}=1$ V) and OFF state ($V_{gs}=0$ V, $V_{ds}=1$ V)

device performance. The maximum current in the ON state and the minimum current in the OFF state are attained when the length of L_1 is equal to 1 nm.

The results of varying the Ge mole fraction are depicted in Fig. 9. It was observed that source channel interface stress increases with Ge mole fraction (x = 0.1 to 0.4). This led to a gradual reduction in the bandgap near source, resulting in a decrease in the tunnelling width which leads to an enhanced tunnelling probability. Maximum on current is obtained at x = 0.4.

The present study examines the transconductance to evidence its effect on device linearity as well as the unity current-gain cut-off frequency (f_T), GBP and other FOMs. Transconductance of a TFET can be calculated as

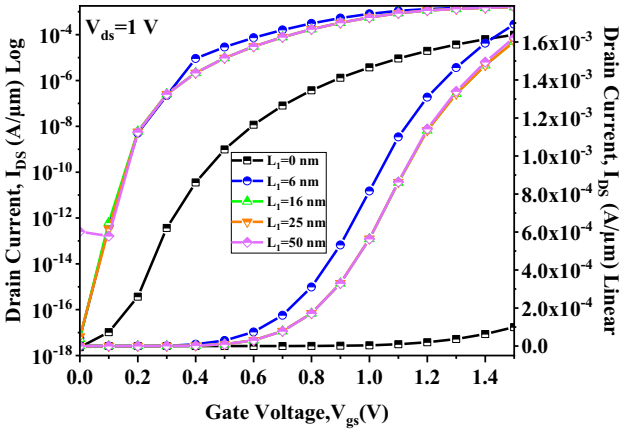


Fig. 6 SiGe-DMG-HD DGTFET transfer characteristics with high-k dielectric length variation

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{3}$$

3.2 Transconductance

Figure 10 depicts the extracted transconductance (GM) for the proposed DMG-HD DGTFET and other conventional TFET structures. The inclusion of a sleek, heavily doped SiGe pocket at the SiGe/Si interface enhances the tunnelling rate, thus results in increased transconductance (gm). Transconductance is enhanced in the proposed design compared to other TFET structures.

3.3 Capacitive Analysis

In TFET, Parasitic capacitances is a vital control parameter that affects RF parameters also. Parasitic capacitances comprising C_{gs} and C_{gd}, impact device performance. Total gate-to-gate capacitance (C_{gg}) is represented by C_{gd} in TFETs, while C_{gs} remains relatively modest. This is in contrast to MOSFETs, where C_{gs} is virtually equal to C_{gd} (in linear region). C_{gd} rises as gate bias is applied because the potential barrier between the channel and drain is lowered. Because it is the primary component influencing the transient response, Miller capacitance, C_{gd} [29] is one of the biggest challenges in constructing digital circuits. Therefore, C_{gg} and C_{gd} ought to be minimised. DMG-HD DGTFET, SMG-HD DGTFET, and SMG DGTFET are all compared with SiGe DMG-HD DGTFET in Fig. 11 a and b for their parasitic capacitances. At $V_{ds}=V_{gs}=1$ V, it has been observed that the SiGe DMG-HD DGTFET has the lowest C_{gd} value, while the SMG DGTFET has the highest value.

The C_{gd} versus V_{gs} plot for SiGe DMG-HD DGTFET, as a function of high-k length (L_1) variation, is

Table 4 Comparison of Analog performance of proposed structure, S_4 for dielectric length (L_1) variations

Dielectric length	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/I_{OFF}	SS (mV/decade)	V_{th} (V)
$L_1 = 0$ nm	3.75×10^{-6}	2.29×10^{-18}	1.63×10^{12}	29	0.7
$L_1 = 6$ nm	8.16×10^{-4}	5.62×10^{-18}	1.45×10^{14}	48	0.22
$L_1 = 16$ nm	5.64×10^{-4}	5.49×10^{-18}	1.03×10^{14}	50	0.23
$L_1 = 50$ nm	5.64×10^{-4}	2.54×10^{-13}	2.22×10^{9}	45	0.23

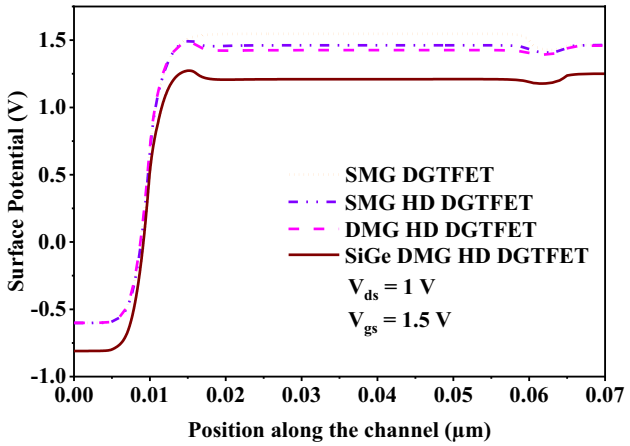


Fig. 7 Surface Potential of all design structures, S_1, S_2, S_3 and S_4 across the length

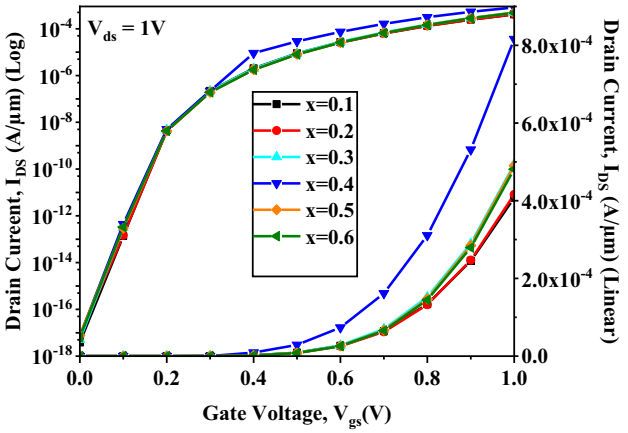


Fig. 9 Effect of SiGe mole fraction (x) variation on drain characteristics for proposed structure S_4

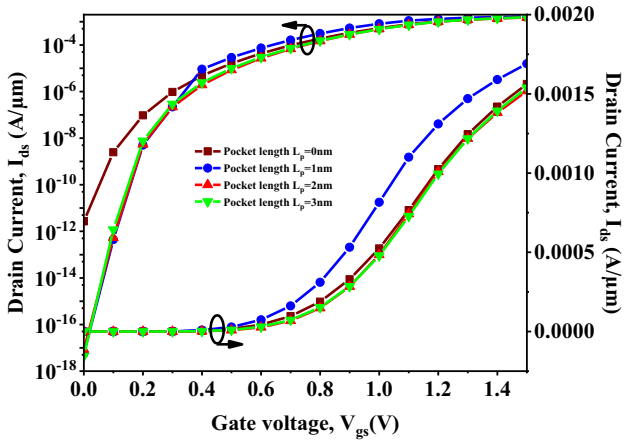


Fig. 8 Effect of SiGe pocket length variation on drain characteristics for proposed structure S_4

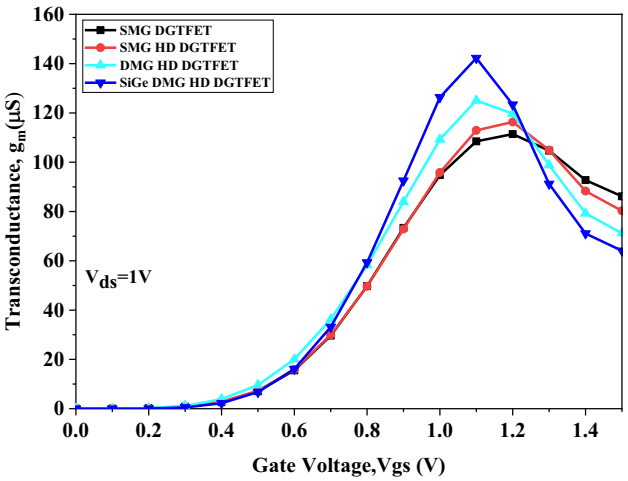


Fig. 10 Transconductance of all design structures S_1, S_2, S_3 and S_4

depicted in Fig. 12. It reveals that the C_{gd} starts increasing at V_{gs} 0.22 V, as tunnelling commences at V_{th}. The capacitance (C_{gd}) of TFET with $L_1 = 0$ nm, $L_1 = 6$ nm, $L_1 = 16$ nm, $L_1 = 25$ nm, and $L_1 = 50$ nm is plotted. The Proposed design with dielectric length ($L_1 = 6$ nm) shows a diminution in C_{gd} among all others. The reduction in capacitance observed in the suggested TFET design is owing to the reduction in length of the high-k dielectric. The reduction of C_{gd} is needed to attain a diminished time delay within the digital circuit.

3.4 RF Performance

Figure 13 shows the cut-off frequency curve for various mentioned TFET structures. Cut-off frequency refers to the frequency at which the current gain is 1 and it is also

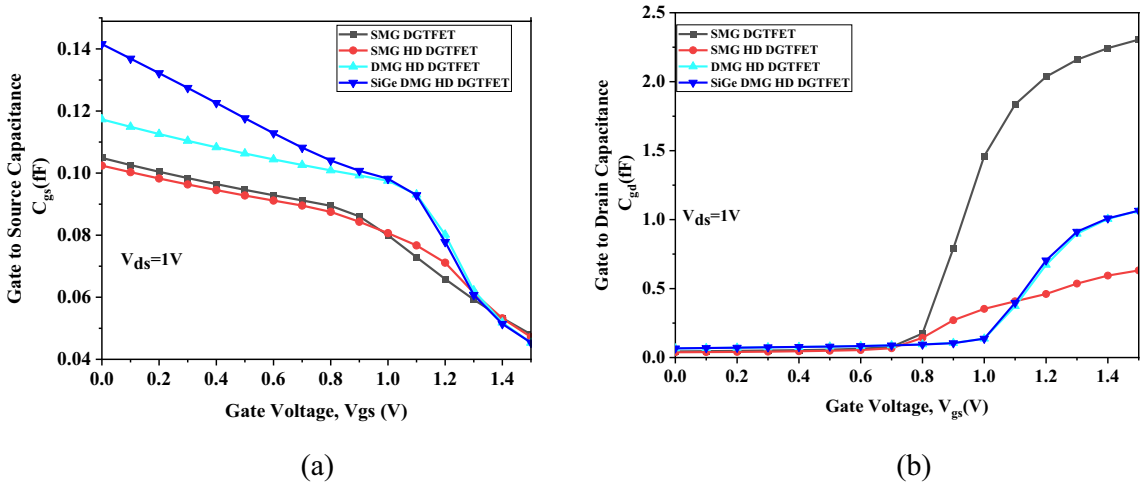


Fig. 11 Variation of **a** gate to source capacitance, C_{gs} and **b** gate to drain capacitance, C_{gd} for all four structures S_1, S_2, S_3 and S_4 with gate voltage (V_{gs})

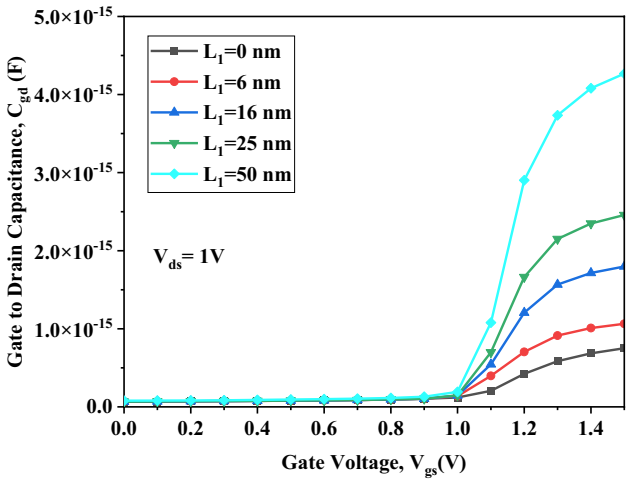


Fig. 12 Variation of gate to drain capacitance, (C_{gd}) for SiGe-DMG-HD-DGTFET with high-k dielectric length variation

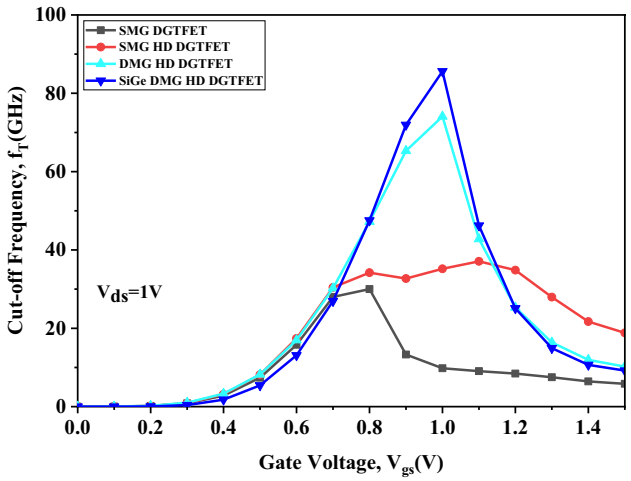


Fig. 13 Cut-off frequency (f_T) of all structures S_1, S_2, S_3 and S_4 at $V_{gs} = 1.5$ V and $V_{ds} = 1$ V

essential to analyse the switching behaviour of TFET. It can be expressed as;

$$f_t = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{4}$$

SiGe DMG-HD DGTFET gives better performance at gate voltage 1 V. At $V_{gs} = V_{ds} = 1$ V, the obtained cut-off frequency for the proposed design and DMG-HD DGTFET are 85 GHz and 74 GHz, respectively. Increase in f_T is due to presence of high-K material near source and heavily doped III-V compound material ($Si_{1-x}Ge_x$) at source/channel interface.

The device operating frequency range can be defined by gain-bandwidth product as;

$$GBP = \frac{g_m}{20\pi C_{gd}} \tag{5}$$

GBP graph for all mentioned structures is plotted in Fig. 14. Due to increased g_m and reduced C_{gd} SiGe DMG-HD DGTFET displays the improved results over other compared structures.

Some essential RF parameters like gain frequency product (GFP), gain transconductance frequency product (GTFP) and trans conductance frequency product (TFP) have also been explored and evaluated as given by Eqs. (6–8) respectively. It is crucial to emphasize that GFP holds significance in the high frequency applications pertaining to operational amplifiers (OPAMPs). The utilization of the gain transconductance frequency product

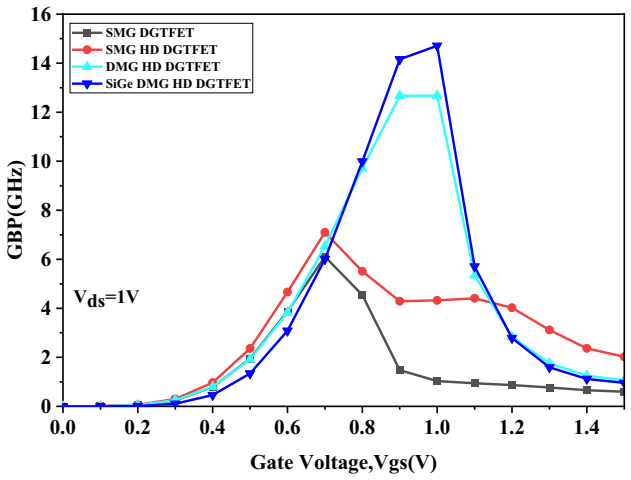


Fig. 14 Gain bandwidth product, GBP of all four structures at $V_{gs} = 1.5$ V and $V_{ds} = 1$ V

(GTFP) serves to establish a trade-off between power consumption and operational speed.

$$GFP = A_v x f_t \tag{6}$$

$$GTFP = TGFxGFP \tag{7}$$

$$TFP = TGFxf_t \tag{8}$$

In Fig. 15 a, the gain frequency product (GFP) is depicted as a function of the gate bias voltage for all the mentioned DGTFET structures, while maintaining a constant drain voltage of $V_{DS} = 1.0$ V. Based on the analysis of Fig. 13 a, GFP behaves in a linear way as the applied gate bias goes up in the sub-threshold region. This linear increment persists until reaching a peak value, after which a decline is observed within the saturation region. Also, it has been seen that the SiGe DMG-HD DGTFET has the highest value, making it a very good choice for improving the RF performance of FET devices.

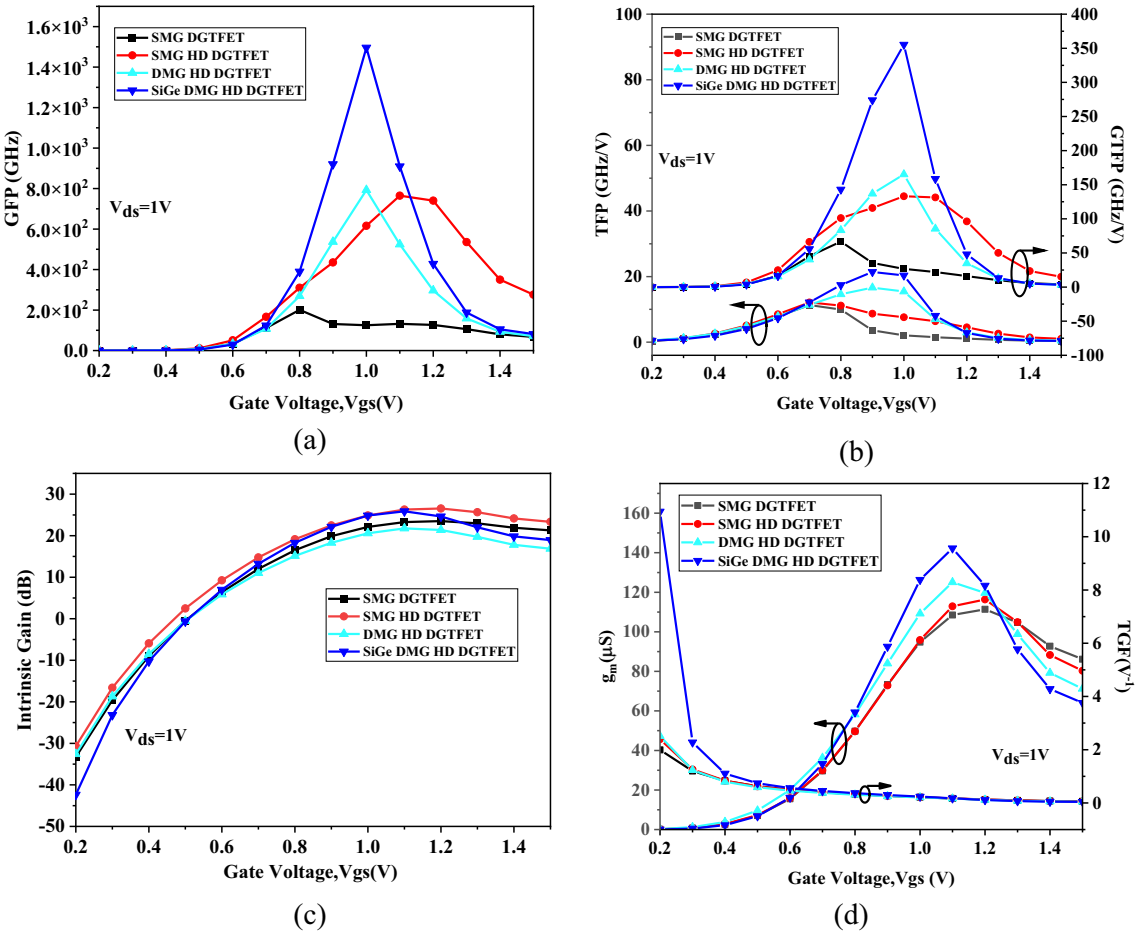


Fig. 15 Comparision of **a** GFP **b** TFP and GTFP (**c**) Intrinsic gain (**d**) TGF and g_m for various conventional TFET structures S_1, S_2, and S_3 with proposed design structure S_4

Figure 15 b shows TFP and GTFP variation as a function of gate bias voltage for all mentioned DGTFET structure at a constant drain voltage $V_{DS} = 1.0$ V. The gain-transconductance-Frequency product (GTFP) has been used to find the desired operational region. This is done by taking speed, transconductance, and gain into careful consideration. The term "transconductance frequency product (TFP)" refers to the multiplication of the cut-off frequency and the transconductance gain factor (TGF). It is observed from Fig. 13 b that the TFP and GTFP both behaves in a linear way as the applied gate bias goes up in the sub-threshold region holding the peak value before decreasing in saturation region. Further, it has been noticed that SiGe DMG-HD DGTFET obtained higher value among structures which is desirable for better RF performance of the devices.

The intrinsic gain, denoted as A_V, holds significant importance as an analog performance metric. It serves to quantify the variation in transconductance with respect to output conductance**.** Figure 15 c illustrates the variation in intrinsic gain as a function of applied gate bias voltage for all DGTFET structures mentioned while maintaining a constant drain voltage of VDS = 1.0 V. The observation can be made from the graphical representation in Fig. 13 c that the intrinsic gain exhibits an upward trend as the applied gate bias voltage is increased within the linear region, while it demonstrates a downward trend within the saturation region. Further, it has also been observed that intrinsic gain is higher for SiGe DMG-HD DGTFET structure. TGF, an essential parameter for evaluating transconductance generation efficiency, is expressed as,

$$TGF = \frac{g_m}{I_{ds}} \tag{9}$$

The gain per unit value of power dissipation is rendered by TGF. TGF plot for mentioned structures is shown in Fig. 15 d. Figure shows that in weak inversion regime TGF has highest value for proposed design, but it goes down as gate voltage increases which indicates steeper subthreshold swing at lower gate voltages. From Fig. 13 it has been determined that the proposed design improvement is improved in TGF by 12.3%, TFP by 24.1%, GFP by 47% and GTFP by 53.5% as compared to DMG-HD DGTFET structure.

4 Conclusion

A dual metal hetero dielectric double gate TFET with SiGe pocket has been thoroughly analysed for analog and RF performance. To increase the drive current bandgap modulated pocket of SiGe has been incorporated at source channel interface. Ambipolarity is reduced via hetero-dielectric material and inequal doping of source and drain. The proposed TFET design have shown enhanced performance respecting increased ON current and current switching ratio (order of 10^{14}). Optimised hetero dielectric length, SiGe pocket length and mole fraction improve electrostatic properties. It is also reported that cut-off frequency is improved by 13.5%, GBW by 13.8% when to DMG-HD-DGTFET. Hence, SiGe-DMG-HD-DGTFET is adequate for RF and low-power applications.

Acknowledgements We express our heartfelt gratitude to the anonymous reviewers for their valuable comments and insightful suggestions to enhance the overall quality of the manuscript. The authors are grateful to the Integral University, Lucknow, Uttar Pradesh, India, for providing them manuscript number IU/R&D/2023-MCN0002175 for the current research work.

Authors' Contributions Vedvrat: Conceptualization, Methodology, TCAD Software, Data curation, Analysis and Interpretation of data, Writing- Original draft preparation, Visualization, Investigation, Validation. Mohd Yusuf Yasin: Supervision and Reviewing. Vidyadhar Gupta: Revision and editing. Digvijay Pandey: Revision and editing.

Funding The author(s) received no financial support for the research, authorship, and/or publication of this article.

Data Availability The data and material are available within the manuscript.

Declarations The authors declare that all procedures followed were in accordance with the ethical standards.

Ethics Approval Not applicable.

Consent to Participate All the authors declare their consent to participate in this research article.

Consent for Publication All the authors declare their consent for publication of the article on acceptance.

Competing Interests The authors declare no competing interests

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