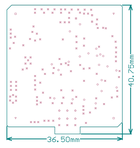
| Symbol | Count | Hole Size | Plated | Hole Type | Drill Layer Pair | Via/Pad | Pad Shape | Template |
|---|---|---|---|---|---|---|---|---|
| □ | 2 | 94.49mil (2.400mm) | NPTH | Round | Top Layer - Bottom Layer | Pad | Rounded | c10hn240 |
| ▽ | 2 | 118.11mil (3.000mm) | NPTH | Round | Top Layer - Bottom Layer | Pad | Rounded | c10hn300 |
| ⊠ | 3 | 39.37mil (1.000mm) | NPTH | Round | Top Layer - Bottom Layer | Pad | Rounded | c100hn100 |
| ○ | 6 | 33.86mil (0.860mm) | PTH | Round | Top Layer - Bottom Layer | Pad | (Mixed) | (Mixed) |
| ○ | 22 | 10.00mil (0.254mm) | PTH | Round | Top Layer - Bottom Layer | Via | Rounded | v51h25m0mx0 |
| ⊞ | 128 | 12.00mil (0.305mm) | PTH | Round | Top Layer - Bottom Layer | Via | Rounded | (Mixed) |
| | 163 Total | | | | | | | |

| Layer | Name | Material | Thickness | Constant | Board Layer Stack |
|---|---|---|---|---|---|
| 1 | Top Overlay | | | | |
| 2 | Top Solder | Solder Resist | 0.020mm | 3.5 | |
| 3 | Top Layer | Copper | 0.035mm | | |
| 4 | Dielectric 1 | PP-006 | 0.128mm | 4.2 | |
| 5 | Dielectric 2 | | 0.088mm | 4.2 | |
| 6 | PWR | Copper | 0.035mm | | |
| 7 | Dielectric 3 | FR-4 | 1.000mm | 4.2 | |
| 8 | GND | Copper | 0.035mm | | |
| 9 | Dielectric 4 | PP-006 | 0.088mm | 4.2 | |
| 10 | Dielectric 5 | | 0.128mm | 4.2 | |
| 11 | Bottom Layer | Copper | 0.035mm | | |
| 12 | Bottom solder | Solder Resist | 0.020mm | 3.5 | |
| 13 | Bottom Overlay | | | | |

Total Pcb Thickness = 1.612MM +/- 10%

Finished cu Thickness: 1 OZ




FABRICATION NOTES:

1. LATEST VERSION OF ALL REFERENCED IPC SPECIFICATIONS TO BE USED.
2. ALL MULTILAYER PC BOARDS MUST BE PRODUCED IN ACCORDANCE IPC-A-600, CLASS 2.
3. INSPECT ALL MULTILAYER PC BOARDS IN ACCORDANCE WITH IPC-6012, CLASS 2.
4. MATERIAL: THIN LAMINATE, FR4 COPPER CLAD 1 OZ PER LAYER
   1.6 MM +/-10% THICK, COLOR GREEN,
   MINIMUM CTI (PER IEC 60112 USING SOLUTION A) = 175.
5. FABRICATE BOARDS USING THE GERBER FILES CONTAINED IN FABRICATION FOLDER.
6. DRILL DATA ARE CONTAINED IN THE FABRICATION FOLDER.
7. ALL HOLE DIAMETERS MUST BE PER DRILL CHART +/-0.003 INCHES TOLERANCE,
   UNLESS OTHERWISE SPECIFIED.
8. PLATED-THRU HOLES TO HAVE COPPER WALL THICKNESS NOT LESS THAN 0.001 INCHES.
   THICKNESS TO BE DETERMINED BY IPC-6012, CLASS 2.
9. SURFACE FINISH PROCESS MUST BE HAL LEAD-FREE
10. SILKSCREEN BOTH SIDES WITH WHITE EPOXY NON-CONDUCTIVE INK.
    SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. SOLDER MASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE SOLDER MASK (LPI),
    MEETING IPC-SM-840, CLASS 2, HIGH PERFORMANCE SPECIFICATIONS.
    FINISH: SOLDER MASK OVER BARE COPPER (SMOBC).
12. WARP AND TWIST SHALL BE LESS THAN 0.0075 INCH PER INCH.
    INSPECT PER IPC-TM-650, 2.4.22.
13. ALL BOARDS MUST BE DATE CODED USING A FOUR DIGIT CODE,
    YEAR FOLLOWED BY WEEK (e.g. 0449 = 49TH WEEK OF 2004).
14. ALL DIMENSIONS AND HOLE DIAMETERS APPLY TO THE FINISHED BOARD.
15. PADS MUST BE FINISHED TO WITHIN +/-0.0015 INCHES OF THE MINOR DIMENSION (PAD WIDTH)
    AND +/-0.002 INCHES OF THE MAJOR DIMENSION (PAD LENGTH).
16. FIDUCIALS MUST BE FREE OF ANY MARKINGS.
17. BARE BOARD TO BE ELECTRICALLY TESTED IN ACCORDANCE WITH IPC-ET-652 AND MARKED AS TESTED.
18. BOARDS SHALL BE UL-RECOGNIZED AND UL-MARKED. UL FIRE RETARDANT RATING 94V-0 OR HIGHER.
19. ROHS: ALL MATERIALS MUST BE COMPLIANT WITH THE ROHS DIRECTIVE.
20. EACH PCB MUST BE INDIVIDUALLY BAGGED.
21. ALL VIA MUST BE TENTED.



CUSTOMER: LUMAX

UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS ARE IN INCHES
TOLERANCES (DECIMAL):
.X +/-0.1
.XX +/-0.01
.XXX +/-0.005
ANGLES +/-0.5

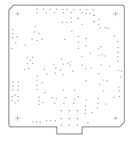
Drawn By : Harshavardhan K — DATE 15-Jun-20
Designed By : Aravinth D — DATE 15-Jun-20
Checked By : Uday Kumar K — DATE 15-Jun-20
REF ID

Design Partner:
Embdes Engineering Solutions Pvt Ltd

PROJECT NAME: LMAT_AMT_V3

LAYER NAME: Board Outlines Drill Drawing

Scale 1:1 | DO NOT SCALE DRAWING | Sheet 1 of 1 | Size D | DWG NO | REV 1.0





CUSTOMER: LUMAX

UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS ARE IN INCHES
TOLERANCES (DECIMAL):
.X +/-0.1
.XX +/-0.01
.XXX +/-0.005
ANGLES +/-0.5

| | | |
|---|---|---|
| Drawn By : Harshavardhan K | DATE 15-Jun-20 | Design Partner: Embdes Engineering Solutions Pvt Ltd |
| Designed By : Aravinth D | DATE 15-Jun-20 | |
| Checked By : Uday Kumar K | DATE 15-Jun-20 | PROJECT NAME: LMAT_AMT_V3 |
| REF ID | | LAYER NAME: Board Outline Bottom side |
| Scale 1:1 | DO NOT SCALE DRAWING | Sheet 1 of 1 / Size D / DWG NO / REV 1.0 |