

N588JP Data Sheet

1-Channel Speech PowerSpeech® Series

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1. General Description

The N588JPxxx is an 8-bit 65C02 based, 1-ch Voice Synthesizer OTP, to implement sophisticated applications with high level of sound quality.

The N588JPxxx improves the structure to minimize the external components for various applications. In addition, it allows customers to use internal Rosc with precise frequency control to save BOM cost and gain lower frequency deviation.

Furthermore, the N588JPxxx provides lots of function includes 16 ~ 24 I/Os where one port with high drive current, 128 ~ 192 bytes RAM, H/W IR carrier, and Low Voltage Detection. Meanwhile, N588JPxxx builds in 3-pair output pins with 64-level control for the applications of motors tiny control. The N588JPxxx also build in Watch Dog Timer and Low Voltage Reset to prevent latch-up situation occurring.

The N588JPxxx family contains several items with different playback ROM size and duration as shown below table:

Part No.	ROM (KB)	Duration (Sec.) (6KHz)	СН	Fsys	Rosc	Audio	I/O Pins	H/W PWM	RAM (Byte)	IR Carrier	U_IO	WDT	LVR	LVD
N588JP062	206	65	1	4,6,8MHz	TRIM	PWM	16 I/O	3-pair	128	Yes	Yes	Yes	Yes	2.2, 2.4, 2.7, 3.3V
N588JP082	254	80	1	4,6,8MHz	TRIM	PWM	16 I/O	3-pair	128	Yes	Yes	Yes	Yes	2.2, 2.4, 2.7, 3.3V
N588JP122	414	131	1	4,6,8MHz	TRIM	PWM	16 I/O	3-pair	128	Yes	Yes	Yes	Yes	2.2, 2.4, 2.7, 3.3V
N588JP172	510	162	1	4,6,8MHz	TRIM	PWM	16 I/O	3-pair	128	Yes	Yes	Yes	Yes	2.2, 2.4, 2.7, 3.3V
N588JP202	704	223	1	4,6,8MHz	TRIM	PWM	24 I/O	3-pair	192	Yes	Yes	Yes	Yes	2.2, 2.4, 2.7, 3.3V
N588JP252	830	263	1	4,6,8MHz	TRIM	PWM	24 I/O	3-pair	192	Yes	Yes	Yes	Yes	2.2, 2.4, 2.7, 3.3V
N588JP342	1022	324	1	4,6,8MHz	TRIM	PWM	24 I/O	3-pair	192	Yes	Yes	Yes	Yes	2.2, 2.4, 2.7, 3.3V

Note: The duration (Sec.) is based on 4-bit NM4 algorithm at 6KHz and deducted synthesis library



2. Features

- VDD range:
 - ➤ 4, 6, 8MHz: 2.0 ~ 5.5V
- System clock: 4, 6, 8MHz
- Oscillator: builds in internal Rosc (TRIM)
- RAM: 128B ~ 192B
- 16~24 bi-directional I/O pins
 - ▶ BP00 ~ BP07, BP10 ~ BP17 can be set as Input or Output status individually
- Provides 8-pin with high sink current capability to drive LEDs
- 3-pair H/W PWM I/O pins with 6-bit resolutions to control motor
 - ➤ BP00/02/04 are defined as 3 H/W PWM I/O pins. They can be paired with BP01/03/05 respectively by same (or opposite) phase of output waveform
- Builds in IR carrier generation circuit for simplifying firmware IR application
- Algorithm: 4-bit NM4, 4-bit MD4, 5-bit MDM, 8-bit LP8
- Audio output: 12-bit PWM
- Channel: 1-channel Voice
- Built-in Watch-Dog Timer (WDT)
- 3 voltage levels of Low Voltage Reset (LVR) by mask option
 - > LVR: 2.0V, 2.2V, 2.7V
- Builds in Low Voltage Detection (LVD) with 4 voltage levels
 - > LVD: 2.2V, 2.4V, 2.7V, 3.3V
- Support *PowerScript*TM for developing codes in easy way
- Full-fledged development system
 - ➤ Source-level ICE debugger (Assembly & *PowerScript*TM format)
 - ➤ *Ultra I/OTM* tool for event synchronization mechanism



3. Pin Description

Pin Name	I/O	Function	
/RESET	I	IC reset input, low active.	
BP00 ~ BP07	I/O	 General input/output pins. Each pin can be set as Input or Output individually. When the pin will be set output by BP0D, user needs to set BP0x value of 0/1 first. For output pin, BP0 provides high-sink current. For input pin, it can be set as pull-high or floating BP00/02/04 can be set as 3-pin H/W PWM output with 64-level resolution. They can be paired with BP01/03/05 (also H/W PWM output) respectively with same or opposite phase of output waveform 	
		BP07 can be configured as IR carrier output	
BP10 ~ BP17	I/O	 General input/output pins. Each pin can be set as Input or Output individually. When the pin will be set output by BP1D, user needs to set BP1x value of 0/1 first. For input pin, it can be set as pull-high or floating. BP1 can generate interrupt request to release IC from STOP mode BP11/12 can be writer interface (SCLK/SDIO) on writer mode 	
*BP20 ~ BP27	I/O	 General input/output pins. Each pin can be set as Input or Output by group, BP20 ~ BP23 configured by BP2D[0], and BP24 ~ BP27 by BP2D[1]. When the pins will be set output by BP2D, user needs to set BP2x value of 0/1 first. 	
PWM+	О	PWM driver positive output to drive speaker directly	
PWM-	О	PWM driver negative output to drive speaker directly	
VDD	Power	Positive power supply for uP and peripherals	
VSS	Power	Negative power supply for oscillation, uP and peripherals	
VDD_IO	Power	Positive power supply for I/O	

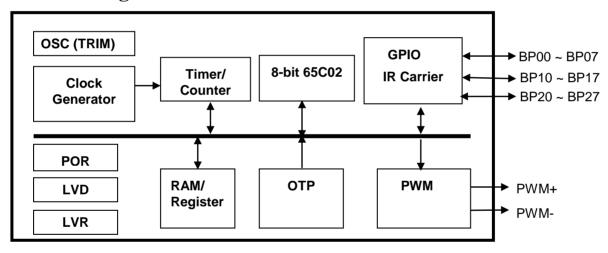


Pin Name	I/O	Function
VSS_IO	Power	Negative power supply for I/O
VDD_SPK	Power	Positive power supply for speaker driver
VSS_SPK	Power	Negative power supply for speaker driver
V33O	Power	3.3V Regulator output.
VPP	Power	8.5V input during program OTP memory on writer mode. Let it be NC for normal operation mode.

Note1: BP20 ~ BP27 only provides in N588JP202 ~ N588JP342

Note2: OTP program pad: BP11 (SCLK), BP12 (SDIO), VDD, VPP, VSS

4. Block Diagram



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rated Value	Unit
Power Supply	VDD-VSS	-	-0.3 to +7.0	V
Input Voltage	Voltage VIN All Inputs		VSS -0.3 to VDD +0.3	V
Storage Temp.	TSTG	-	-55 to +150	°C
Operating Temp.	TOPR	-	0 to +70	°C

Note: Exposure to conditions beyond those listed under the Absolute Maximum Ratings table may adversely affect the life and reliability of the device.



5.2 D.C. Characteristics

 $(V_{DD} - V_{SS} = 4.5V, TA = 25^{\circ} C, No Load unless otherwise specified)$

Parameter	Sym	Conditions	Min	Тур	Max	Unit
		$F_{OSC} = 4 \text{ MHz}$	2.0	-	5.5	V
Operating Voltage	V_{DD}	$F_{OSC} = 6 \text{ MHz}$	2.0	-	5.5	V
		$F_{OSC} = 8 \text{ MHz}$	2.0		5.5	V
Operating Current	I_{OP1}	No load, $F_{OSC} = 8 \text{ MHz}$	-	8	10	mA
Standby Current (STOP)	I_{DD1}	No load	-	3	10	μΑ
Input Low Voltage	V_{IL}	All input pins	V_{SS}	-	$0.3 \text{ V}_{\text{DD}}$	V
Input High Voltage	V_{IH}	All input pins	$0.7~V_{DD}$	-	V_{DD}	V
	I_{OL}	$V_{DD} = 3V$, $V_{OUT} = 0.4V$	8	12	-	mA
Output Current	I_{OH}	$V_{DD} = 3V, V_{OUT} = 2.6V$	-4	-6	-	mA
(BP0)	I_{OL}	$V_{DD} = 4.5V, V_{OUT} = 1.0V$	-	25	-	mA
	Іон	$V_{DD} = 4.5V, V_{OUT} = 3.5V$	-	-12	-	mA
	I_{OL}	$V_{DD} = 3V$, $V_{OUT} = 0.4V$	4	6	-	mA
Output Current	I_{OH}	$V_{DD} = 3V, V_{OUT} = 2.6V$	-4	-6	-	mA
(BP1, BP2)	I_{OL}	$V_{DD} = 4.5V, V_{OUT} = 1.0V$	-	12	-	mA
	I_{OH}	$V_{DD} = 4.5V, V_{OUT} = 3.5V$	-	-12	-	mA
Output Current	I_{OL1}	$RL=8\Omega$	+250	-	-	mA
PWM+ / PWM-	I_{OH1}	[PWM+][RL][PWM-]	-250	-	-	mA
		2.2V Option		2.2		
LVD detect voltage	V_{LVD}	2.4V Option		2.4	_	V
L V D detect Voltage	V LVD	2.7V Option	_	2.7	_	'
		3.3V Option		3.3		

5.3 A.C. Characteristics

(VDD = 4.5V, TA = 25°C, No Load unless otherwise specified)

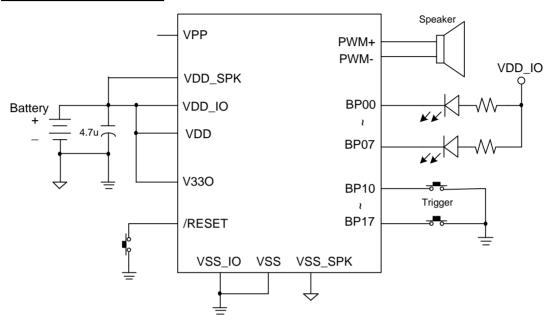
Parameter	Sym	ym Conditions		Тур	Max	Unit
		$F_{OSC} = 4 \text{ MHz}$	3973	4096	4219	
Main Clock Frequency	Fosc	$F_{OSC} = 6 \text{ MHz}$	5960	6144	6328	KHz
		$F_{OSC} = 8 \text{ MHz}$	7946	8192	8438	
Frequency Deviation by Voltage Drop	$\frac{\Delta F_{OSC}}{F_{OSC}}$	(Fmax – Fmin)/Fmin @VDD: 2.4 ~ 4.5V	-	2	-	%



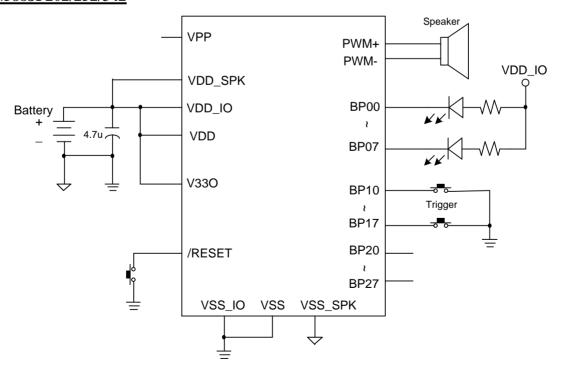
6. Application Circuit

6.1 2-battery Application:

N588JP062/082/122/172



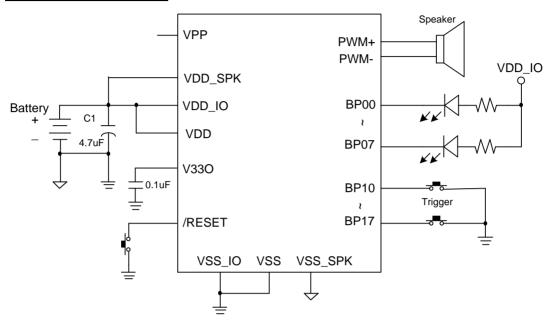
N588JP202/252/342



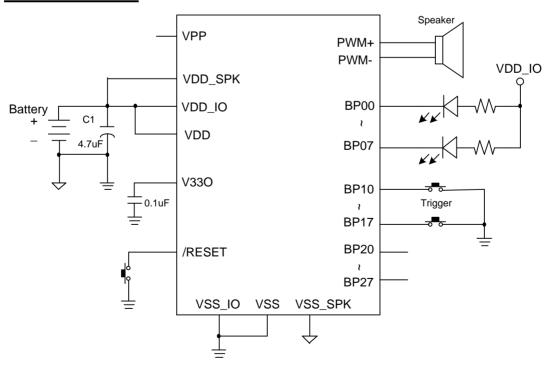


6.2 3-battery Application with Normal Loading:

N588JP062/082/122/172



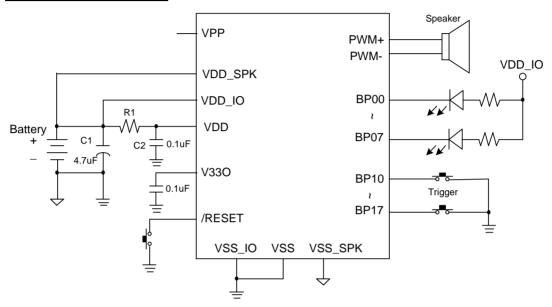
N588JP202/252/342



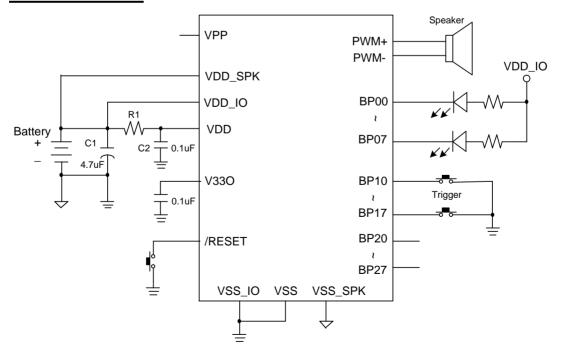


6.3 3-battery Application with Heavy Loading (Motor):

N588JP062/082/122/172



N588JP202/252/342





Note:

- 1. For general applications, C1 (4.7uF) is must to stable system power
- 2. For motor application, the C1 (4.7uF), C2 (0.1uF), and R1 (10 Ω) are all necessary
- 3. C1 value need to be adjusted according to loading, such as motor control application

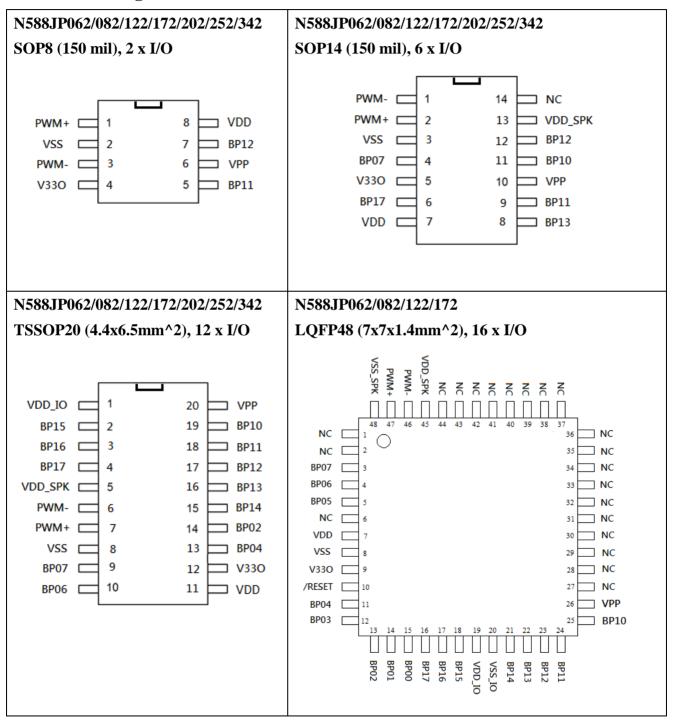
7. PCB LAYOUT GUIDE

In PCB layout, the IC substrate should be connected to VSS, and VSS_SPK and VSS/VSS_IO should have its own path to connect with negative of battery; and VDD_SPK and VDD/VDD_IO should have its own path to connect with positive of battery also

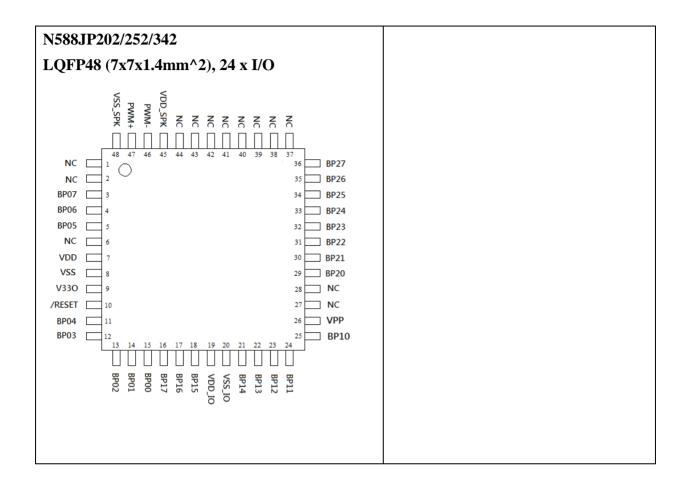


8. Package Information

8.1 PIN Assignment



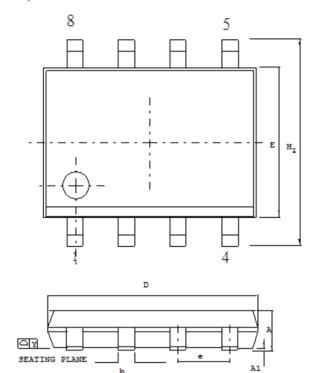


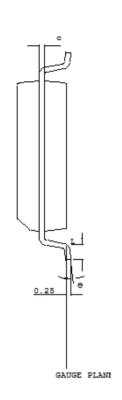




8.2 Package Dimension

SOP8, 150 mil



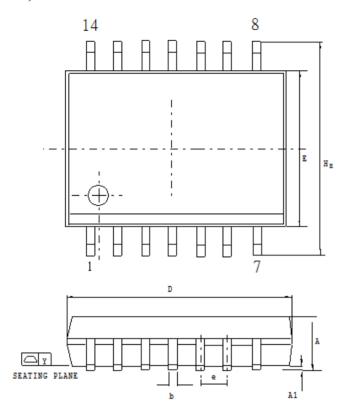


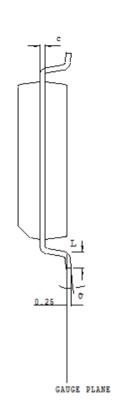
Control demensions are in milmeters .

	DIMENSION I	N MM	DIMENSION I	N INCH	
SYMBOL	MIN.	MAX.	MIN.	MAX.	
A	1.35	1.75	0.053	0.069	
Al	0.10	0.25	0.004	0.010	
ď	0.33	0.51	0.013	0.020	
c	0.19	0.25	0.008	0.010	
E	3.80	4.00	0.150	0.157	
D	4.80	5.00	0.188	0.196	
e	1.27 B	SC	0.050 BSC		
HE	5.80	6.20	0.228	0.244	
Y		0.10		0.004	
L	L 0.40		0.016	0.050	
θ	θ 0		0	10	



SOP14, 150 mil



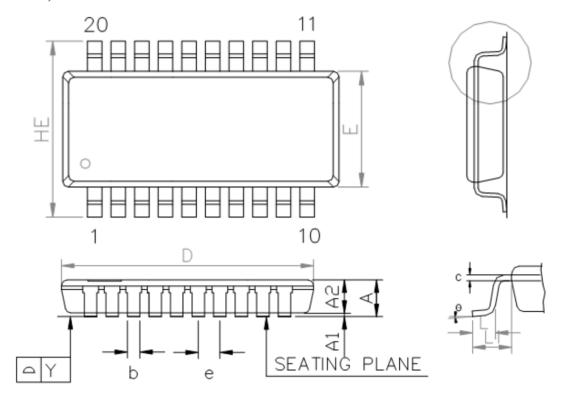


Control demensions are in milmeters .

	DIMENSION I	N MM	DIMENSION IN INCH		
SYMBOL	MIN.	MAX.	MIN.	MAX.	
A	1.35	1.75	0.053	0.069	
A1	0.10	0.25	0.004	0.010	
b	0.33	0.51	0.013	0.020	
С	0.19	0.25	0.008	0.010	
E	3.80	4.00	0.150	0.157	
D	8.55	8.75	0.337	0.344	
e	1.27 B	5C	0.050 BSC		
HE	5.80	6.20	0.228	0.244	
Y		0.10		0.004	
L	0.40	1.27	0.016	0.050	
θ	0	8	0	8	



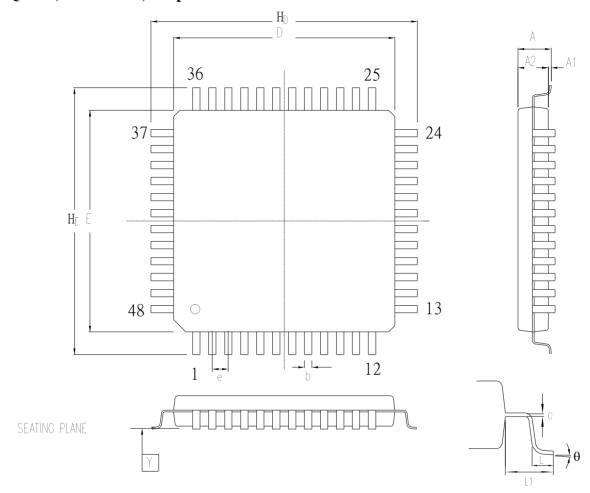
TSSOP20, 4.4 x 6.5mm



SYMBOL	DII	MENSION (MM)	V	DIMENSION (INCH)			
STREEL	MIN.	NDM.	MAX.	MIN.	N□M.	MAX.	
Α	-	-	1,20	-	-	0.047	
Al	0,05	-	0,15	200.0		0.006	
42	0.80	0.90	1,05	0.031	0.035	0.041	
E	4.30	4.40	4.50	0.169	0.173	0.177	
HE		6.40 BS	С	0.252 BSC			
D	6.40	6.50	6.60	0.252	0.256	0.260	
L	0.50	0.60	0.75	0.020	0.024	0.030	
Li		1.00 REF			0.039 RI	F	
ь	0.19	-	0.30	0.007	-	0.012	
e		0.65 BS	C		0.026 B:	2C	
С	0.09	-	0.20	0.004	-	0.008	
θ	0"	-	8"	0,	-	8*	
Y	0.	10 BASIC			0.004 BA	SIC	



LQFP48, 7x7x1.4mm, footprint 2.0mm



Controlling dimension: Millimeters

Symbol	Dime	ension i	n inch	Dimension in mm			
Symbol	Min	Nom	Max	Min	Nom	Max	
Α	_			_	_		
A 1	0.002	0.004	0.006	0.05	0.10	0.15	
A ₂	0.053	0.055	0.057	1.35	1.40	1.45	
b	0.006	0.008	0.010	0.15	0.20	0.25	
С	0.004	0.006	0.008	0.10	0.15	0.20	
D	0.272	0.276	0.280	6.90	7.00	7.10	
Е	0.272	0.276	0.280	6.90	7.00	7.10	
е	0.014	0.020	0.026	0.35	0.50	0.65	
Н₀	0.350	0.354	0.358	8.90	9.00	9.10	
H _∈	0.350	0.354	0.358	8.90	9.00	9.10	
L	0.018	0.024	0.030	0.45	0.60	0.75	
L ₁	_	0.039	_	_	1.00	_	
Y	_	_	0.004	_	_	0.10	
θ	0.	_	7	0.	_	7	



9. Ordering Information

Part No.	Shape	Туре	Remark
N588JP062/082/122/172/202/252/342	W, H	Wafer Form, Die Form	Blank, 16~24 I/O
N588JP062/082/122/172/202/252/342XXX	W, H	Wafer Form, Die Form	Pre-code
N588JP062A/082A/122A/172A/202A/252A/342A	Е	Package: SOP8 (150mil)	Blank, 2 I/O
N588JP062B/082B/122B/172B/202B/252B/342B	Е	Package: SOP14 (150mil)	Blank, 6 I/O
N588JP062F/082F/122F/172F/202F/252F/342F	Е	Package: TSSOP20 (4.4x6.5mm^2)	Blank, 12 I/O
N588JP062L/082L/122L/272L/202L/252L/342L	Е	Package: LQFP48 (7x7mm^2)	Blank, 16~24 I/O
N588JP06A/08A/12A/17A/20A/25A/34AXXX	Е	Package: SOP8 (150mil)	Pre-code, 2 I/O
N588JP06B/08B/12B/17B/20B/25B/34BXXX	Е	Package: SOP14 (150mil)	Pre-code, 6 I/O
N588JP06F/08F/12F/17F/20F/25F/34FXXX	Е	Package: TSSOP20 (4.4x6.5mm^2)	Pre-code, 12 I/O
N588JP06L/08L/12L/17L/20L/25L/34LXXX	Е	Package: LQFP48 (7x7mm^2)	Pre-code, 16~24 I/O



10. Revision History

Version	Date	Substantial Changes	Page
A1.0	Feb. 2020	First version release	All
A1.1	Feb. 2020	Update TSSOP20, LQFP48 PIN name	12, 13

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