EC200S-CN

Hardware Design

LTE Standard Module Series

Rev. EC200S-CN_Hardware_Design_V1.0

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About the Document

Revision History

Version	Date	Author	Description
1.0	2020-04-29	Vane WANG/ Simmons ZHOU	Initial

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1 Introduction

This document defines the EC200S-CN module and describes its air interface and hardware interface which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of EC200S-CN module. Associated with application note and user guide, customers can use EC200S-CN module to design and set up wireless applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating EC200S-CN module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

EC200S-CN is an LTE-FDD, LTE-TDD and GSM wireless communication module, which provides data connectivity on LTE-FDD, LTE-TDD, EDGE and GPRS networks. It also provides voice functionality for customers' specific applications. The following table shows the frequency bands of EC200S-CN module.

Table 1: Frequency Bands of EC200S-CN Module

Network Type	Bands
LTE-FDD	B1/B3/B5/B8
LTE-TDD	B34/B38/B39/B40/B41
GSM	900/1800 MHz

With a compact profile of 29.0 mm × 32.0 mm × 2.4 mm, EC200S-CN can meet almost all requirements for M2M applications such as automotive, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EC200S-CN is an SMD type module which can be embedded into applications through its 144-pin pads, including 80 LCC signal pads and 64 LGA pads.

2.2. Key Features

The following table describes the detailed features of EC200S-CN module.

Table 2: Key Features of EC200S-CN Module

Features	Description
Power Supply	Supply voltage: 3.4–4.5 V Typical supply voltage: 3.8 V
Transmitting Power	Class 4 (33 dBm ±2 dB) for EGSM900 Class 1 (30 dBm ±2 dB) for DCS1800 Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK Class 3 (23 dBm ±2 dB) for LTE-FDD bands Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	Support up to non-CA Cat 1 FDD and TDD Support 1.4/3/5/10/15/20 MHz RF bandwidth FDD: Max 10 Mbps (DL), Max 5 Mbps (UL) TDD: Max 7.5 Mbps (DL), Max 1 Mbps (UL)
GSM Features	**GPRS:** Support GPRS multi-slot class 12 Coding scheme: CS-1/CS-2/CS-3/CS-4 Max 85.6 kbps (DL), Max 85.6 kbps (UL) **EDGE:** Support EDGE multi-slot class 12 Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max 236.8 kbps (DL), Max 236.8 kbps (UL)
Internet Protocol Features	Support TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/FTPS/SSL/FILE/MQTT/MMS*/SMTP*/SMTPS* protocols Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connection
SMS	Text and PDU mode Point-to-point MO and MT SMS cell broadcast SMS storage: (U)SIM card currently
(U)SIM Interface	Support USIM/SIM card: 1.8 V, 3.0 V

Audio Features	Support one digital audio interface: PCM interface Support one analog audio input and one analog audio output GSM: HR/FR/EFR/AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface*	Used for audio function with external codec
USB Interface	Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480 Mbps Used for AT command communication, data transmission, software debugging, firmware upgrade Support USB serial drivers for: Windows 7/8/8.1/10, Linux 2.6–5.4, Android 4.x–9.x, etc.
UART Interfaces	**Main UART:** Used for AT command communication and data transmission Baud rates reach up to 921600 bps; 115200 bps by default Support RTS and CTS hardware flow control **Debug UART:** Used for the output of partial logs 115200 bps baud rate
SD Card Interface*	Support SD 3.0 protocol
WLAN Interface*	Support SDIO 3.0 interface for WLAN
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	NET_MODE and NET_STATUS used to indicate the network connectivity status
Antenna Interface	Main antenna interface (ANT_MAIN) 50 Ω impedance
Position Fixing	Support Wi-Fi Scan* and main antenna can be used
Physical Characteristics	Size: (29.0 ±0.15) mm × (32.0 ±0.15) mm × (2.4 ±0.2) mm Weight: approx. 4.3 g
Temperature Range	Operation temperature range: -35 to +75 °C[1)] Extended temperature range: -40 to +85 °C[2)] Storage temperature range: -40 to +90 °C
Firmware Upgrade	USB interface and DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1] Within operating temperature range, the module is 3GPP compliant.
2. [2] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of EC200S-CN and illustrates the major functional parts.

- Power management
- Baseband
- Flash
- Radio frequency
- Peripheral interfaces

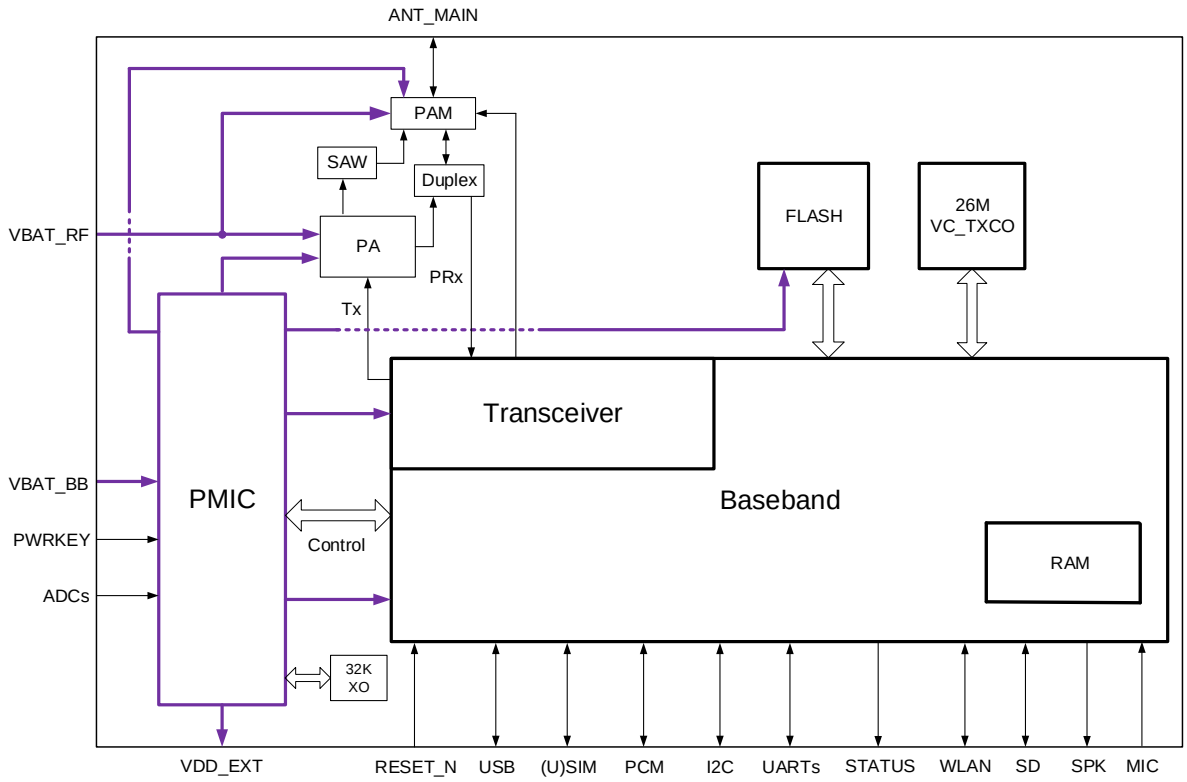


Figure 1: Functional Diagram

2.4. Evaluation Board

In order to help customers develop applications with EC200S-CN, Quectel provides an evaluation board (UMTS&LTE EVB), USB to RS-232 converter cable, earphone, antenna and other peripherals to control or test the module. For more details, please refer to ***document [4]***.

3 Application Interfaces

3.1. General Description

EC200S-CN is equipped with 80 LCC pins plus 64 LGA pins that can be connected to cellular application platform. The subsequent chapters will provide detailed descriptions of the following interfaces.

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces*
- Analog audio interfaces*
- SD card interface*
- WLAN interface*
- ADC interfaces
- Status indication
- FORCE_USB_BOOT interface

NOTE

"*" means under development.

3.2. Pin Assignment

The following figure shows the pin assignment of EC200S-CN module.

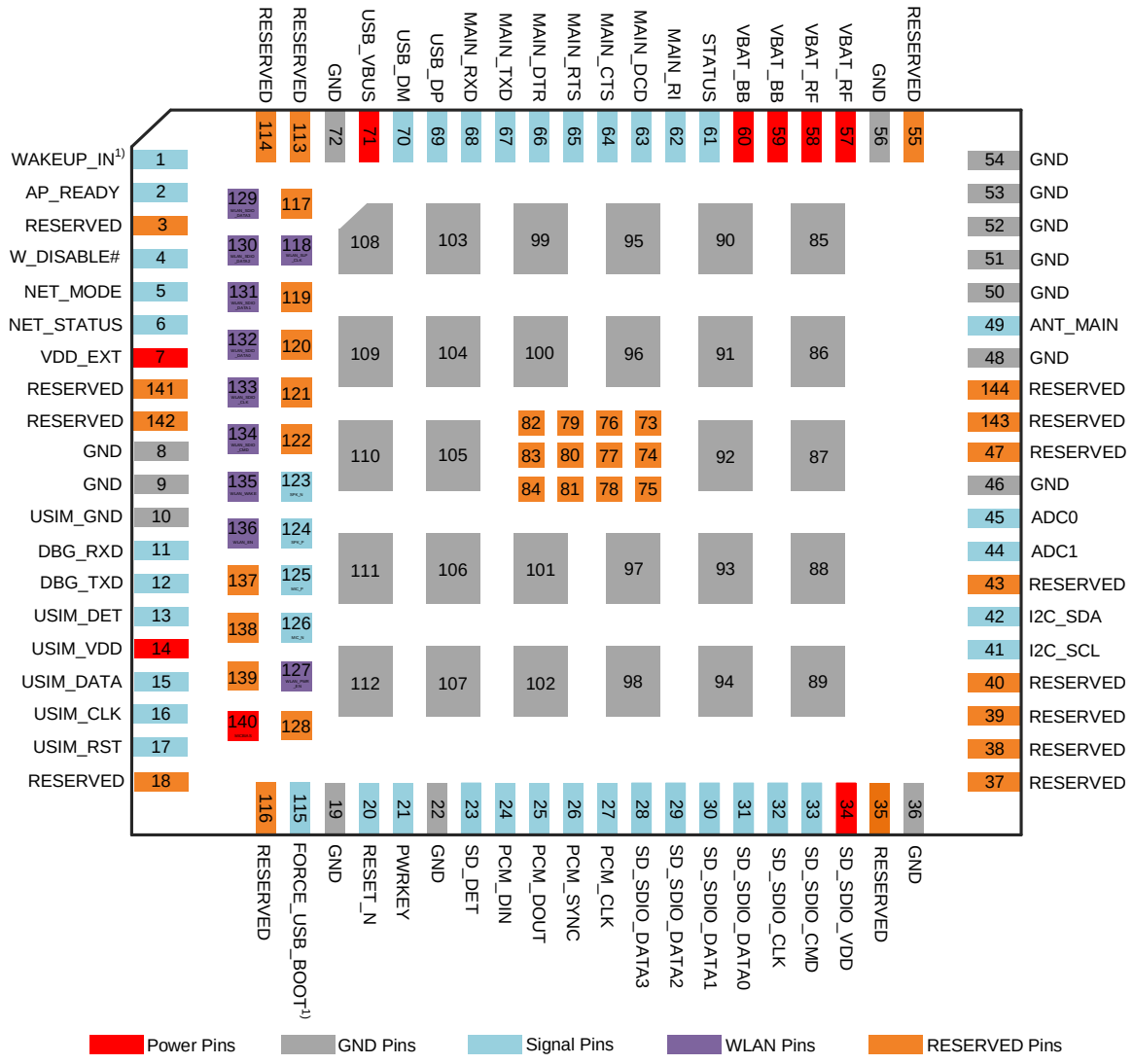


Figure 2: EC200S-CN Module Pin Assignment (Top View)

NOTES

1. 1) means pin FORCE_USB_BOOT cannot be pulled up before startup.
2. Unused and RESERVED pins are kept open, and all GND pins are connected to the ground network.
3. GND pins 85–112 should be connected to ground in the design. RESERVED pins 73–84 should not be designed in schematic and PCB decal, and should be served as a keepout area.
4. WLAN, SD card, PCM & I2C and analog audio interfaces are under development.

3.3. Pin Description

The following tables show the pin definition of EC200S-CN module.

Table 3: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output

Table 4: Pin Description

Power Supply Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for module's baseband part	Vmax = 4.5 V Vmin = 3.4 V Vnorm = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	57, 58	PI	Power supply for module's RF part	Vmax = 4.5 V Vmin = 3.4 V Vnorm = 3.8 V	It must be provided with sufficient current up to 1.8 A.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112		Ground		
Power Supply Output					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vnorm = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. If unused, keep it open.
Power On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	20	DI	Reset the module, low active	V_{IL}max = 0.5 V	If unused, keep it open.
PWRKEY	21	DI	Turn on/off the module	V_{IL}max = 0.5 V	VBAT power domain.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_MODE	5	DO	Indicate the module's network registration mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
NET_ STATUS	6	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
STATUS	61	OD	Indicate the module's operation status		An external pull-up resistor is required. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_DP	69	IO	USB differential data (+)		USB 2.0 compliant. Require differential impedance of 90 Ω. If unused, keep it open.
USB_DM	70	IO	USB differential data (-)		USB 2.0 compliant. Require differential impedance of 90 Ω. If unused, keep it open.
USB_VBUS	71	AI	USB connection detection	Vmax = 5.25 V Vmin = 3.0 V	Typical: 5.0 V If unused, keep it

				Vnorm = 5.0 V	open.
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		Specified ground for (U)SIM		Connect (U)SIM card connector GND.
USIM_DET	13	DI	(U)SIM card detection	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM_VDD	14	PO	Power supply for (U)SIM card	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM_DATA	15	IO	(U)SIM data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_CLK	16	DO	(U)SIM clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_RST	17	DO	(U)SIM reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:**	

				V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RI	62	DO	Ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_DCD	63	DO	Data carrier detection	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_CTS	64	DO	Clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_RTS	65	DI	Request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
MAIN_DTR	66	DI	Data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
MAIN_TXD	67	DO	Transmit data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_RXD	68	DI	Receive data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	11	DI	Debug receive data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
DBG_TXD	12	DO	Debug transmit data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
ADC Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC1	44	AI	General-purpose analog to digital converter	Voltage range: 0 V to VBAT_BB	If unused, keep it open.
ADC0	45	AI	General-purpose analog to digital converter	Voltage range: 0 V to VBAT_BB	If unused, keep it open.
PCM & I2C Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_DIN	24	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
PCM_DOUT	25	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
PCM_SYNC	26	IO	PCM data frame synchronization	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, it serves as an output signal. In slave mode, it is used as an input signal. If unused, keep it open.
PCM_CLK	27	IO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, it serves as an output signal. In slave mode, it is used as an input signal.
I2C_SCL	41	OD	I2C serial clock for external codec		An external 1.8 V pull-up resistor is required. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data for external codec		An external 1.8 V pull-up resistor is required. If unused, keep it open.

Analog Audio Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MICBIAS	140	PO	Bias voltage output for microphone		
MIC_P	125	AI	Microphone analog input (+)		
MIC_N	126	AI	Microphone analog input (-)		
SPK_P	124	AO	Analog audio differential output (+)		
SPK_N	123	AO	Analog audio differential output (-)		
SD Card Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_DET	23	DI	SD card detect		1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA3	28	IO	SD card SDIO data bit 3		1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA2	29	IO	SD card SDIO data bit 2		1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA1	30	IO	SD card SDIO data bit 1		1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA0	31	IO	SD card SDIO data bit 0		1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_CLK	32	DO	SD card SDIO clock		1.8/2.8 V power domain.
SD_SDIO_CMD	33	IO	SD card SDIO command		1.8/2.8 V power domain. If unused, keep it

					open.
SD_SDIO_VDD	34	PO	SD card SDIO power		1.8/2.8 V power domain. If unused, keep it open.
WLAN Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	118	DO	WLAN sleep clock		If unused, keep it open.
WLAN_PWR_EN	127	DO	WLAN power supply enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
WLAN_SDIO_DATA3	129	IO	WLAN SDIO data bit 3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
WLAN_SDIO_DATA2	130	IO	WLAN SDIO data bit 2	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
WLAN_SDIO_DATA1	131	IO	WLAN SDIO data bit 1	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
WLAN_SDIO_DATA0	132	IO	WLAN SDIO data bit 0	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
WLAN_SDIO_CLK	133	DO	WLAN SDIO clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
WLAN_SDIO_CMD	134	DO	WLAN SDIO command	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it

					open.
WLAN_WAKE	135	DI	Wake up the host (module) by an external Wi-Fi module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
WLAN_EN	136	DO	WLAN function enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
RF Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	49	IO	Main antenna		50 Ω impedance.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	1	DI	Wake up the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
AP_READY	2	DI	Application processor sleep state detection	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. In low voltage level, module can enter into airplane mode. If unused, keep it open.
FORCE_ USB_BOOT	115	DI	Force the module to enter emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Active high. It is recommended to reserve test points.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	3, 18, 35, 37–40,		Reserved		Keep these pins unconnected.

	43, 47, 55, 73–84, 113, 114, 116, 117, 119–122, 128, 137–139, 141–144

NOTE

"*" means under development.

3.4. Operating Modes

The following table briefly outlines the operating modes to be mentioned in the following chapters.

Table 5: Overview of Operating Modes

Modes	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** command or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. In this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the power management unit (PMU) shuts down the power supply, software goes inactive and the serial interfaces are not accessible. However, the VBAT_RF and VBAT_BB pins are still powered.	

3.5. Power Saving

3.5.1. Sleep Mode

EC200S-CN is able to reduce its current consumption to an ultra-low value in the sleep mode. The following section describes power saving procedures of EC200S-CN module.

3.5.1.1. UART Application

If the host communicates with module via UART interface, the following preconditions should be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR to high level.

The following figure shows the connection between the module and the host.

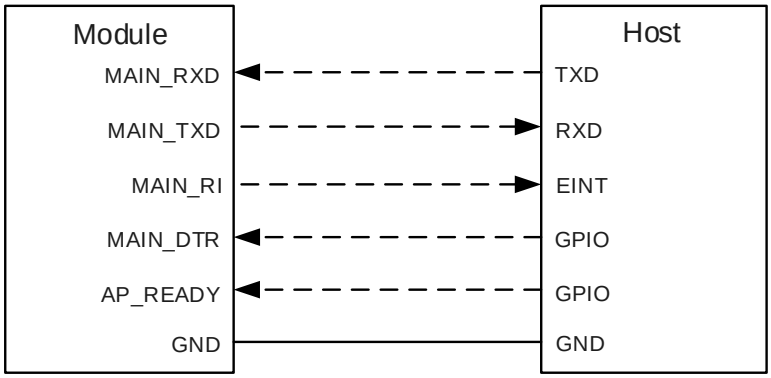


Figure 3: Sleep Mode Application via UART

- Driving MAIN_DTR to low level by host will wake up the module.
- When EC200S-CN has a URC to report, the URC will trigger the behavior of MAIN_RI pin. Please refer to ***Chapter 3.18*** for details about MAIN_RI behavior.

3.5.1.2. USB Application with USB Remote Wakeup Function*

If the host supports USB Suspend/Resume and remote wakeup functions, the following three preconditions must be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the MAIN_DTR is kept at high level or kept open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

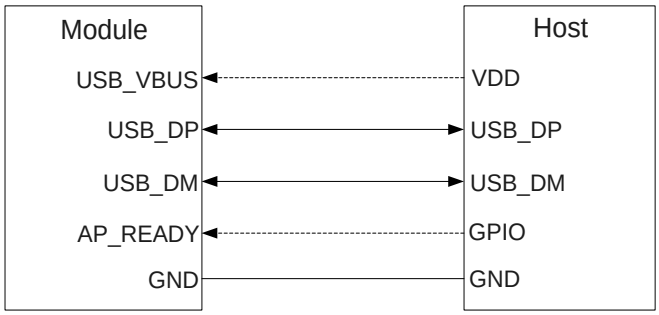


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to EC200S-CN through USB will wake up the module.
- When EC200S-CN has a URC to report, the module will send remote wakeup signals via USB bus so as to wake up the host.

NOTES

"*" means under development.

3.5.1.3. USB Application with USB Suspend/Resume and MAIN_RI Wakeup Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

There are three preconditions to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

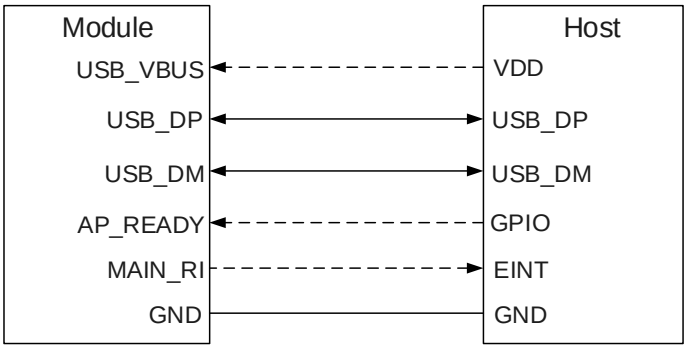


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to module through USB will wake up the module.
- When module has a URC to report, the URC will trigger the behavior of MAIN_RI pin.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB Suspend function, please disconnect USB_VBUS with additional control circuit to let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

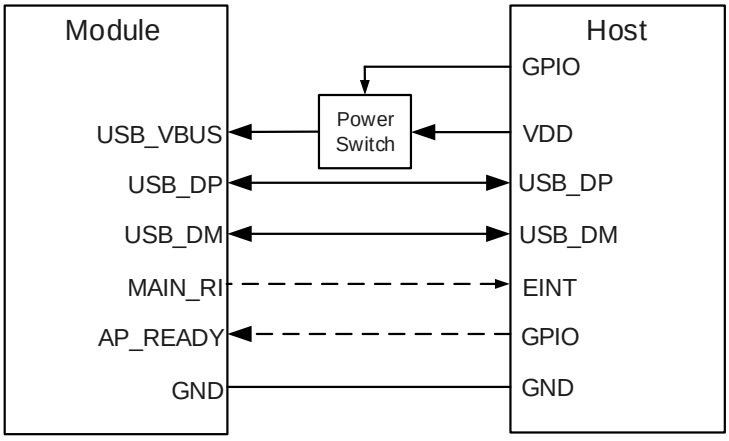


Figure 6: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default, and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving it to low level can make the module enter airplane mode.

Software:

AT+CFUN = <fun> command provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode; both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

3.6. Power Supply

3.6.1. Power Supply Pins

EC200S-CN provides four VBAT pins dedicated to connecting with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows the details of power supply and GND pins.

Table 6: Power Supply and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part	3.4	3.8	4.5	V
VBAT_BB	59, 60	Power supply for module's baseband part	3.4	3.8	4.5	V
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112	Ground	-	0	-	V

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.4 V to 4.5 V. Please make sure that the input voltage will never drop below 3.4 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

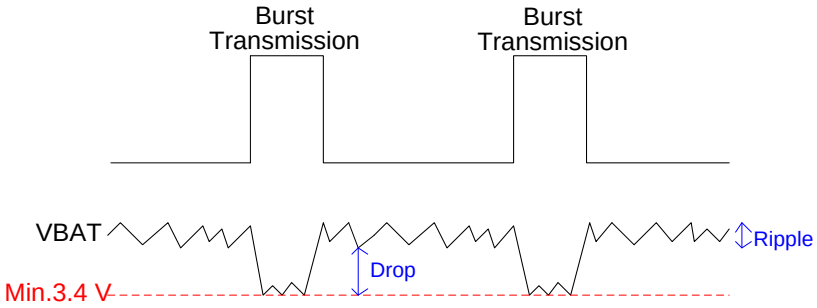


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 µF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1 mm; and the width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS diode of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. The following figure shows the star structure of the power supply.

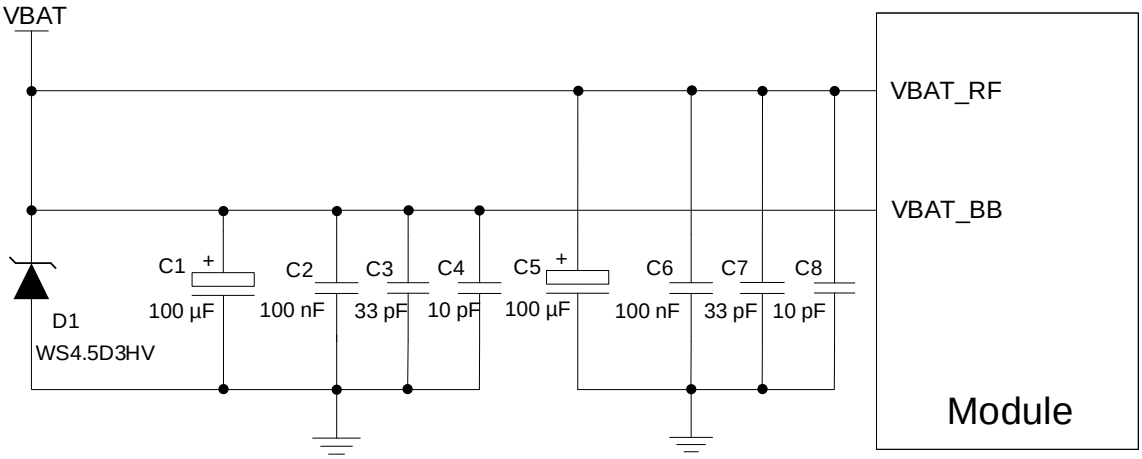


Figure 8: Star Structure of Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2.0 A at least to the module. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for 5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

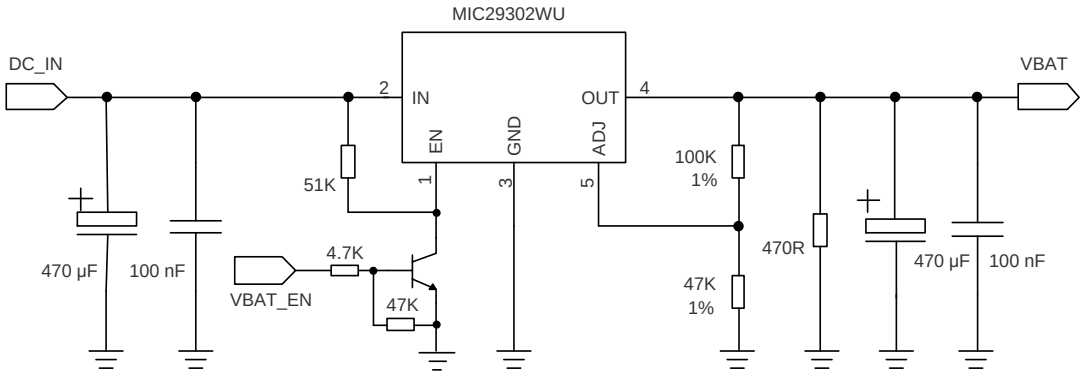


Figure 9: Reference Circuit of Power Supply

3.7. Power-on/off/Reset Scenarios

3.7.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 7: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	VBAT power domain

When EC200S-CN is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

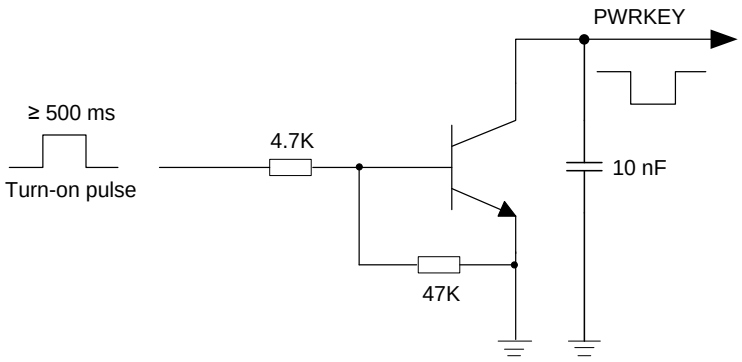


Figure 10: Reference Circuit of Turing on the Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

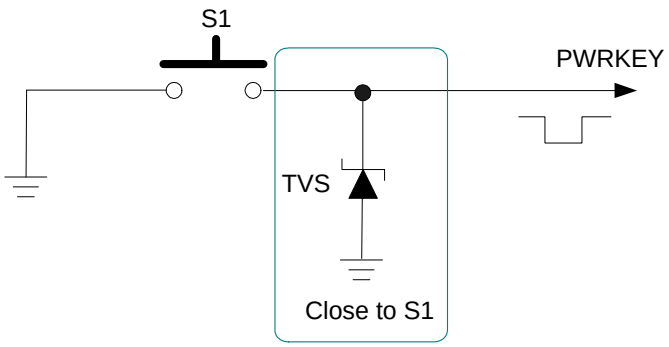


Figure 11: Reference Circuit of Turing on the Module Using Keystroke

The timing of turning on the module is illustrated in the following figure.

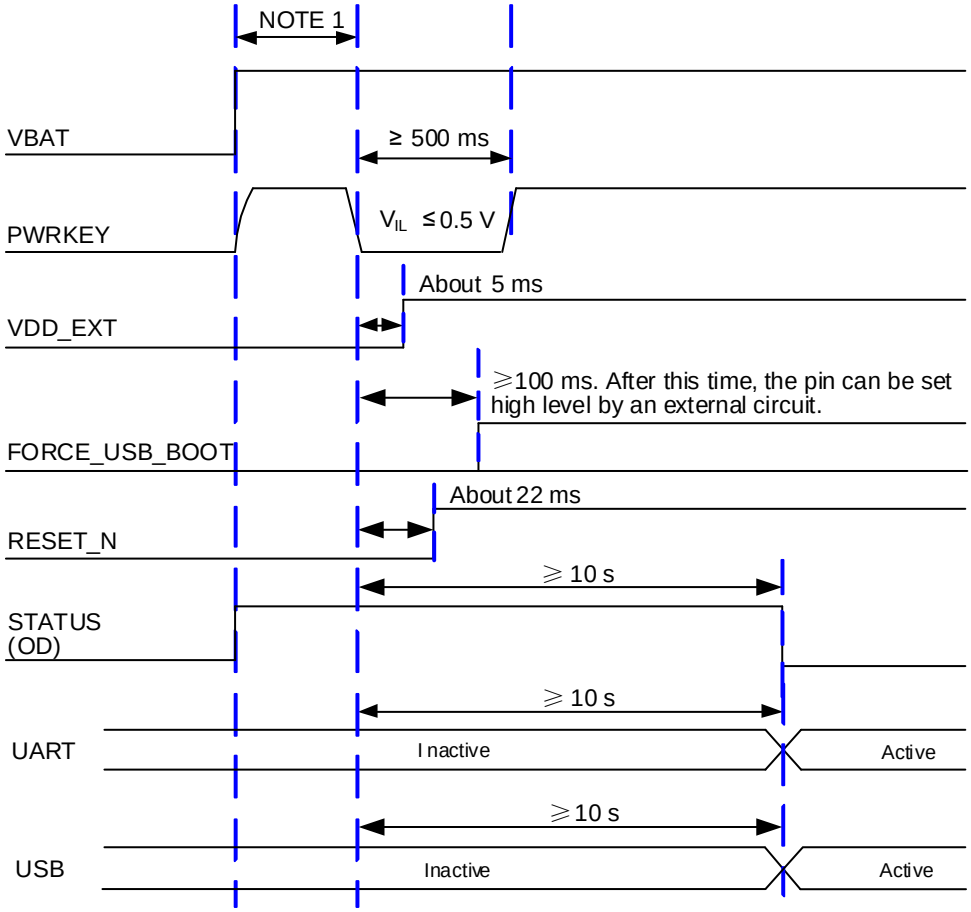


Figure 12: Timing of Turning on Module

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 4.7 kΩ resistor if module needs to be powered on automatically and shutdown is not needed.

3.7.2. Turn off Module

The following procedures can be used to turn off the module:

- Using the PWRKEY pin.
- Using **AT+QPOWD** command.

3.7.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650 ms, the module will execute power-down procedure after the PWRKEY is released. The timing of turning off the module is illustrated in the following figure.

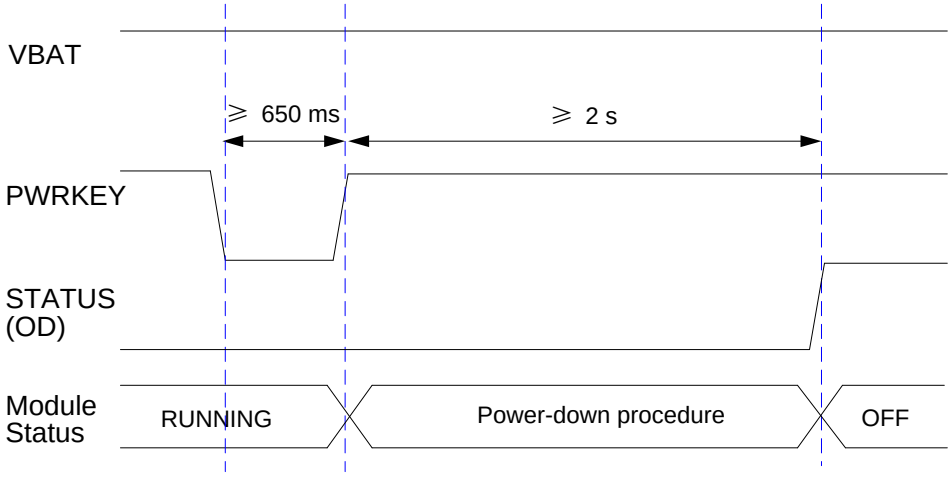


Figure 13: Timing of Turning off Module

3.7.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to the procedure of turning off the module via PWRKEY pin.

Please refer to ***document [2]*** for details about **AT+QPOWD** command.

NOTES

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turning off module with the AT command, please keep PWRKEY at a high level after the execution of the command. Otherwise, the module will turn itself back on after being shut down.

3.7.3. Reset the Module

The RESET_N pin can be used to reset the module. The module can be reset by pulling the RESET_N pin low for at least 300 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 8: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	1.8 V power domain

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

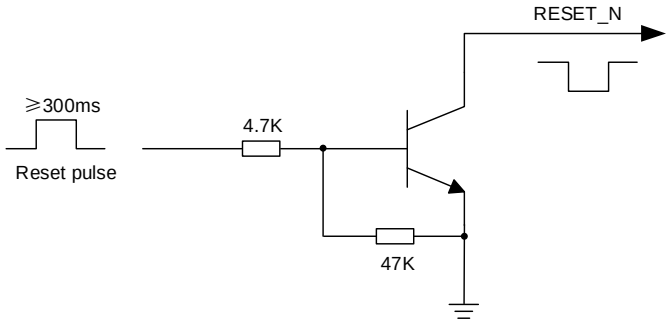


Figure 14: Reference Circuit of Resetting the Module by Using Driving Circuit

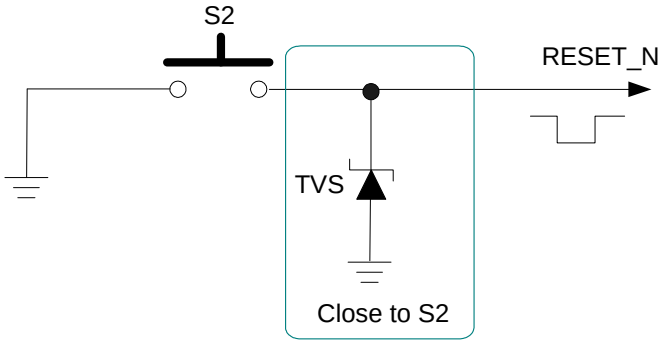


Figure 15: Reference Circuit of Resetting the Module by Using Keystroke

The timing of resetting module is illustrated in the following figure.

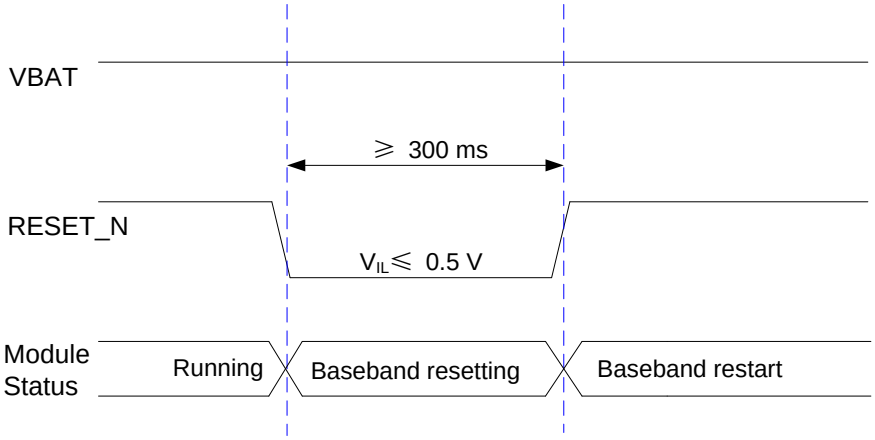


Figure 16: Timing of Resetting Module

NOTES

1. Please ensure that there is no large capacitance with the max value exceeding 10 nF on PWRKEY and RESET_N pins.
2. RESET_N only resets the internal baseband chip of the module and does not reset the power management chip.
3. It is recommended to use RESET_N only when failing to turn off the module by **AT+QPOWD** command or PWRKEY pin.

3.8. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 9: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_GND	10		Specified ground for (U)SIM	
USIM_DET	13	DI	(U)SIM card detection	1.8 V power domain. If unused, keep it open.
USIM_VDD	14	PO	Power supply for (U)SIM card	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.

USIM_DATA	15	IO	(U)SIM data
USIM_CLK	16	DO	(U)SIM clock
USIM_RST	17	DO	(U)SIM reset

EC200S-CN supports (U)SIM card hot-plug via the USIM_DET pin. The function supports low level and high level detections. By default, It is disabled, and can be configured via **AT+QSIMDET** command. Please refer to ***document [2]*** for details about the command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

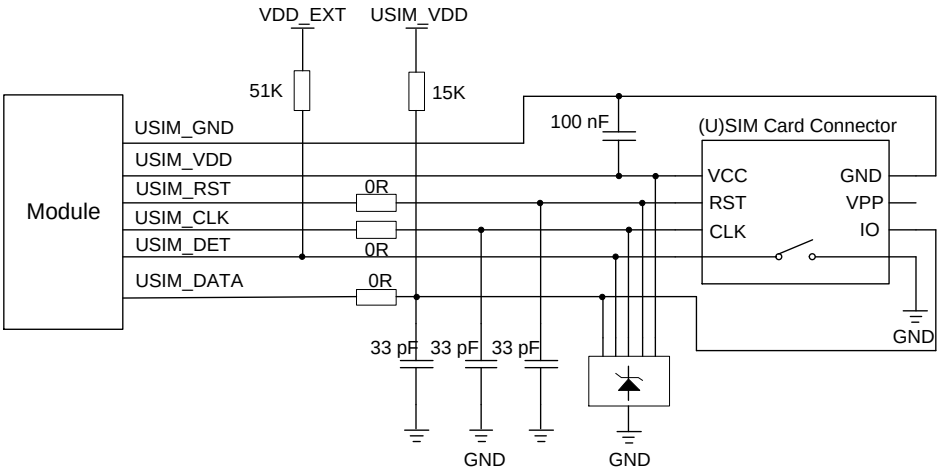


Figure 17: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

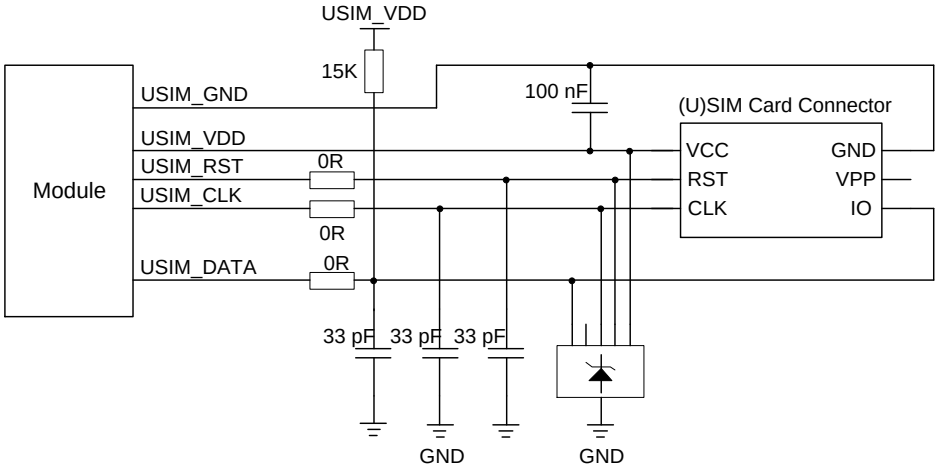


Figure 18: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in customers' applications, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length less than 200 mm as far as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential. If the ground is complete on customers' PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

3.9. USB Interface

EC200S-CN provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serves as a slave device and is used for AT command communication, data transmission, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 10: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	IO	USB differential data (+)	Require differential impedance of 90 Ω
USB_DM	70	IO	USB differential data (-)	Require differential impedance of 90 Ω
USB_VBUS	71	AI	USB connection detection	Typical 5.0 V
GND	72		Ground	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

It is recommended to reserve test points for debugging and firmware upgrade in customers' designs. The following figure shows a reference circuit of USB interface.

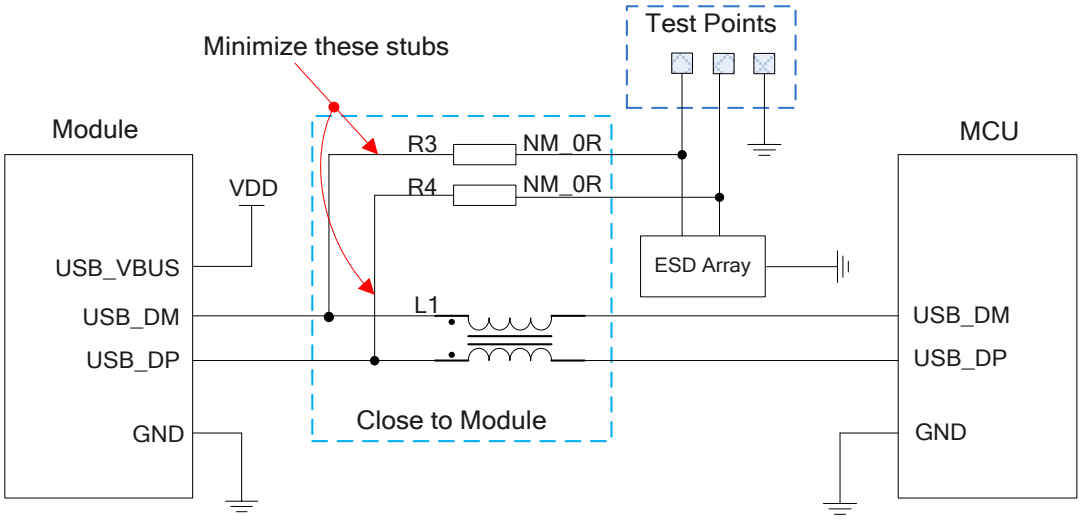


Figure 19: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1, R3 and R4 components must be placed close to the module, and also resistors R3 and R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Please pay attention to the selection of the ESD component on the USB data line. Its parasitic capacitance should not exceed 2 pF and should be placed as close as possible to the USB interface.

3.10. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps baud rates, and the default is 115200 bps. This interface is used for data transmission and AT command communication.
- The debug UART interface supports 115200 bps baud rate. It is used for the output of partial logs.

The following tables show the pin definition of main UART interface.

Table 11: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	62	DO	Ring indication	1.8 V power domain. If unused, keep it open.
MAIN_DCD	63	DO	Data carrier detection	
MAIN_CTS	64	DO	Clear to send	
MAIN_RTS	65	DI	Request to send	
MAIN_DTR	66	DI	Data terminal ready	
MAIN_TXD	67	DO	Transmit data	
MAIN_RXD	68	DI	Receive data	

Table 12: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	11	DI	Debug receive data	1.8 V power domain. If unused, keep it open.
DBG_TXD	12	DO	Debug transmit data	

The logic levels are described in the following table.

Table 13: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V

V_{OH}	1.35	1.8	V

The module provides a 1.8 V UART interface. A level translator should be used if the application is equipped with a 3.3 V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

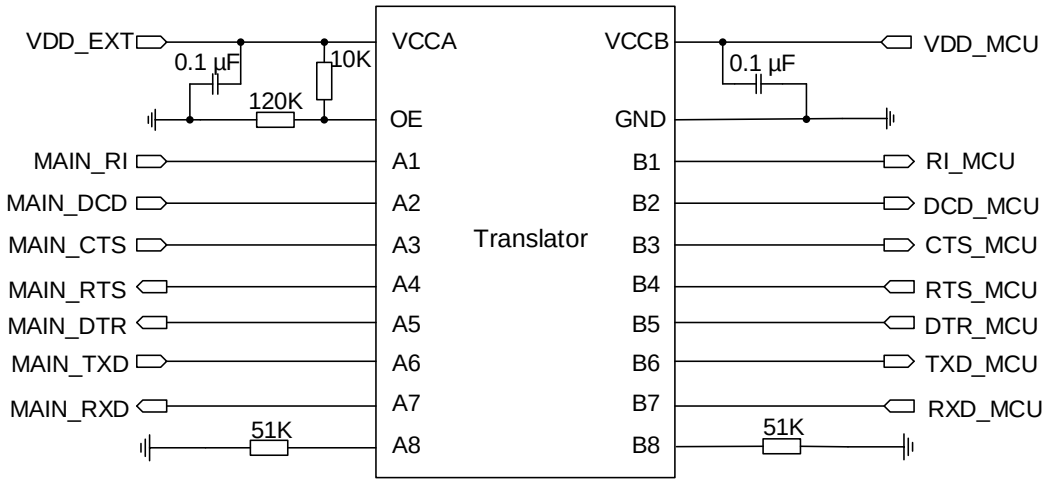


Figure 20: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, please refer to that of the circuits in solid lines, but please pay attention to the direction of connection.

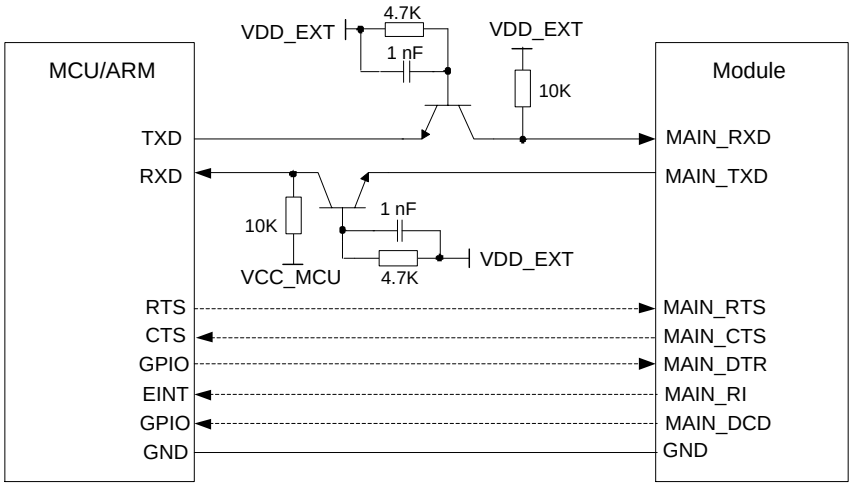


Figure 21: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.

3.11. PCM and I2C Interfaces*

EC200S-CN provides one Pulse Code Modulation (PCM) interface and one I2C interface.

EC200S-CN works as a master device pertaining to I2C interface.

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 14: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	24	DI	PCM data input	1.8 V power domain. If unused, keep it open.
PCM_DOUT	25	DO	PCM data output	1.8 V power domain. If unused, keep it open.
PCM_SYNC	26	IO	PCM data frame synchronization	1.8 V power domain. In master mode, it serves as an output signal. In slave mode, it is used as an input signal. If unused, keep it open.
PCM_CLK	27	IO	PCM clock	1.8 V power domain. In master mode, it serves as an output signal. In slave mode, it is used as an input signal. If unused, keep it open.
I2C_SCL	41	OD	I2C serial clock for external codec	An external 1.8 V pull-up resistor is required. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data for external codec	An external 1.8 V pull-up resistor is required. If unused, keep it open.

The following figure shows a reference design of PCM interface with external codec IC.

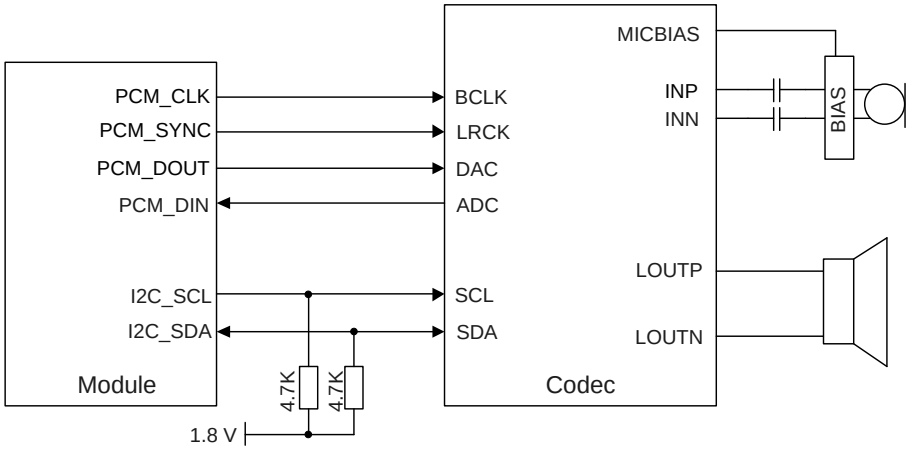


Figure 22: Reference Circuit of PCM Application with Audio Codec

NOTES

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuit on the PCM lines, especially for PCM_CLK.
2. "*" means under development.

3.12. Analog Audio Interfaces*

The module provides one analog input channel and one analog output channel.

Table 15: Pin Definition of Audio Interfaces

Audio channel	Pin Name	Pin No.	I/O	Description
AIN	MICBIAS	140	PO	Bias voltage output for microphone
	MIC_P	125	AI	Microphone analog input (+)
	MIC_N	126		Microphone analog input (-)
AOUT	SPK_P	124	AO	Analog audio differential output (+)
	SPK_N	123		Analog audio differential output (-)

- AIN channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- AOUT channels are differential output channels, which can be applied for output of receiver and handset.

3.12.1. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10 pF capacitor here is used for filtering out RF interference at DCS1800. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, customers would have to discuss with their capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required.

In order to decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces cannot be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

3.12.2. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure

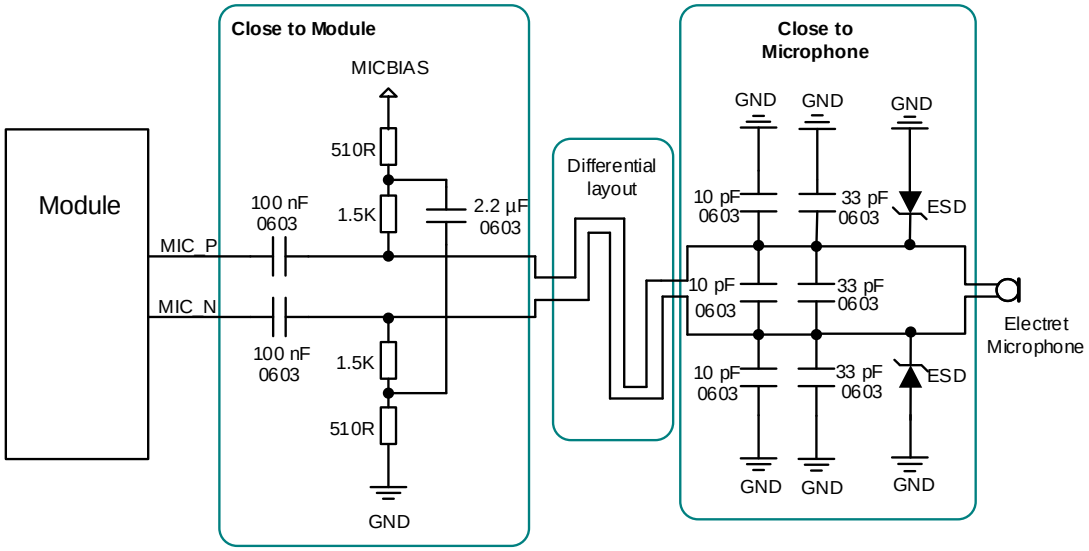


Figure 23: Reference Design for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD components used for protecting the MIC.

3.12.3. Receiver Interface Design

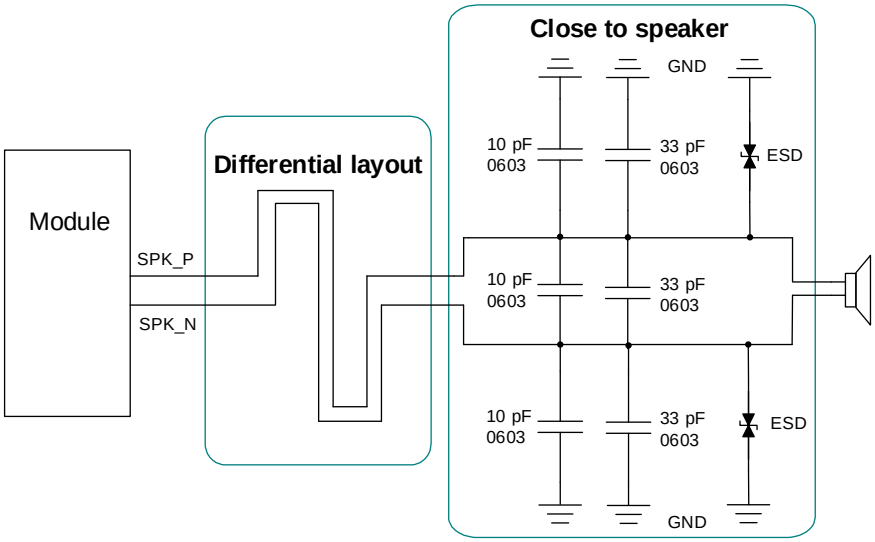


Figure 24: Reference Design for Receiver Interface

NOTE

"*" means under development.

3.13. SD Card Interface*

EC200S-CN provides an SD card interface, which complies with SD 3.0 specification.

The following table shows the pin definition of SD card interface.

Table 16: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_DET	23	DI	SD card detect	1.8/2.8 V power domain. If unused, keep it open.

SD_SDIO_DATA3	28	IO	SD card SDIO data bit 3	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA2	29	IO	SD card SDIO data bit 2	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA1	30	IO	SD card SDIO data bit 1	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA0	31	IO	SD card SDIO data bit 0	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_CLK	32	DO	SD card SDIO clock	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_CMD	33	IO	SD card SDIO command	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_VDD	34	PO	SD card SDIO power	1.8/2.8 V power domain. If unused, keep it open.

The following figure shows a reference design of SD card interface.

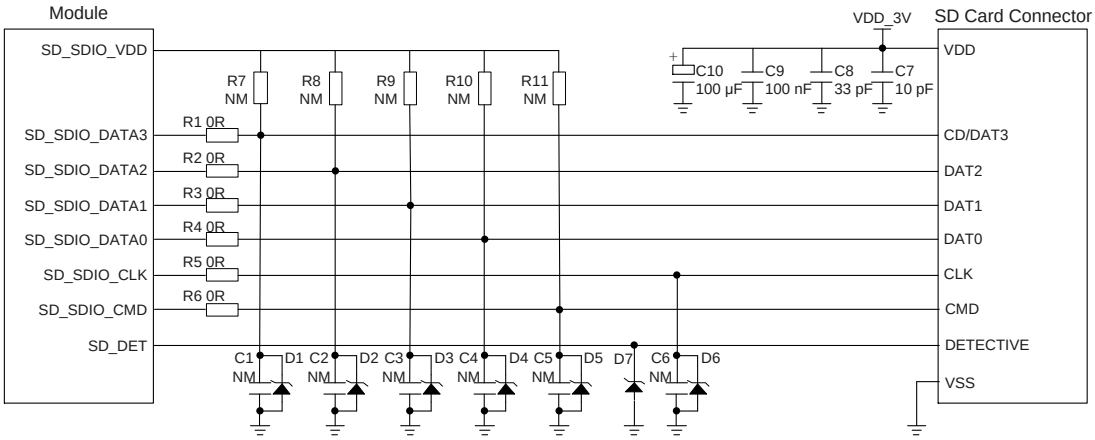


Figure 25: Reference Circuit of SD Card Interface

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- The voltage range of SD card power supply VDD_3V is 2.7–3.6 V and a sufficient current up to 0.8 A should be provided. As the maximum output current of SD_SDIO_VDD is 50 mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, resistors R7–R11 are needed to pull up the SDIO to SD_SDIO_VDD. Value of these resistors is among 10–100 kΩ and the recommended value is 100 kΩ. SD_SDIO_VDD should be used as the pull-up power.
- In order to adjust signal quality, it is recommended to add 0 Ω resistors R1–R6 in series between the module and the SD card. The bypass capacitors C1–C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.

- In order to offer good ESD protection, it is recommended to add a TVS diode on SD card pins near the SD card connector with junction capacitance less than 15 pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
  It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω (±10%).
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 15 pF.
- It is recommended to keep the traces of SD_SDIO_CLK, SD_SDIO_DATA[0:3] and SD_SDIO_CMD with equal length (the difference among them is less than 1mm) and the total routing length needs to be less than 50 mm.

NOTE

"*" means under development.

3.14. WLAN Interface*

EC200S-CN supports a SDIO 3.0 interface for WLAN.

The following table shows the pin definition of WLAN interface

Table 17: Pin Definition of WLAN Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SLP_CLK	118	DO	WLAN sleep clock	If unused, keep it open.
WLAN_PWR_EN	127	DO	WLAN power supply enable control	1.8 V power domain If unused, keep it open.
WLAN_SDIO_DATA3	129	IO	WLAN SDIO data bit 3	
WLAN_SDIO_DATA2	130	IO	WLAN SDIO data bit 2	
WLAN_SDIO_DATA1	131	IO	WLAN SDIO data bit 1	
WLAN_SDIO_DATA0	132	IO	WLAN SDIO data bit 0	
WLAN_SDIO_CLK	133	DO	WLAN SDIO clock	1.8 V power domain If unused, keep it open.
WLAN_SDIO_CMD	134	DO	WLAN SDIO command	1.8 V power domain

WLAN_WAKE	135	DI	Wake up the host (module) by an external Wi-Fi module	If unused, keep it open.
WLAN_EN	136	DO	WLAN function enable control	

As SDIO signals are very high-speed, in order to ensure the SDIO interface design meets SDIO 3.0 specification, please comply with the following principles:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal trace is 50 Ω ±10%.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the traces of WLAN_SDIO_CLK, WLAN_SDIO_DATA[0:3] and WLAN_SDIO_CMD with equal length (the difference among them is less than 1 mm) and the total routing length needs to be less than 50 mm.
- Make sure the adjacent trace spacing is 2 times of the trace width and bus capacitance is less than 15 pF.

NOTE

"*" means under development.

3.15. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. **AT+QADC=0** can be used to read the voltage value on ADC0 pin. **AT+QADC=1** can be used to read the voltage value on ADC1 pin. For more details about these AT commands, please refer to ***document [2]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 18: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description
ADC1	44	General-purpose analog to digital converter
ADC0	45	General-purpose analog to digital converter

The following table describes the characteristic of the ADC function.

Table 19: Characteristic of the ADC

Parameter	Min.	Typ.	Max.	Unit
ADC1 Voltage Range	0		VBAT_BB	V
ADC0 Voltage Range	0		VBAT_BB	V
ADC Resolution		12		bits

NOTE

It is recommended to use a resistor divider circuit for ADC application.

3.16. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two pins which are NET_MODE and NET_STATUS for network status indication. The following tables describe pin definition and logic level changes in different network status.

Table 20: Pin Definition of Network Connection Status/Activity Indication

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network registration mode	1.8 V power domain If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network activity status	1.8 V power domain If unused, keep it open.

Table 21: Working State of Network Connection Status/Activity Indication

Pin Name	Logic Level Changes	Network Status
NET_MODE	Always high	Registered on LTE network
	Always low	Others
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching

	Flicker slowly (1800 ms high/200 ms low)	Idle
	Flicker quickly (125 ms high/125 ms low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

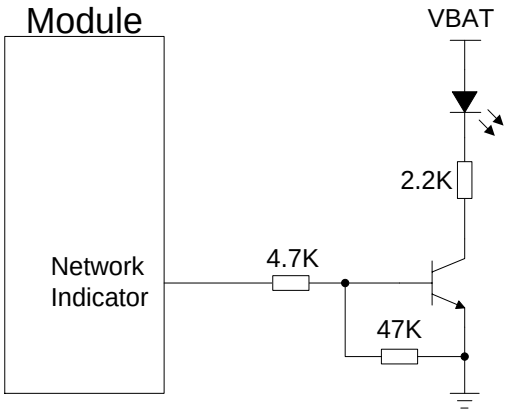


Figure 26: Reference Circuit of Network Status Indication

3.17. STATUS

The STATUS pin is an open drain output for module's operation status indication. It can be connected to a GPIO of DTE with a pulled-up resistor, or as an LED indication circuit as below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

Table 22: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	An external pull-up resistor is required. If unused, keep it open.

The following figure shows different circuit designs of STATUS, and customers can choose either one according to the application demands.

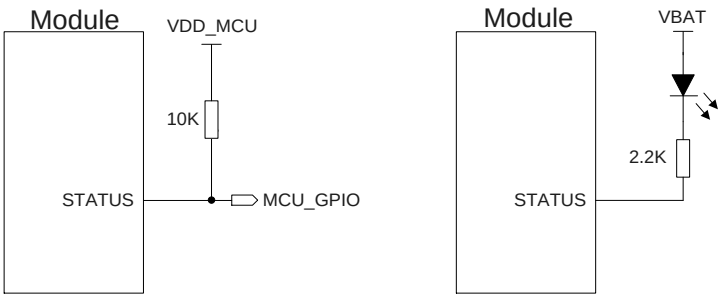


Figure 27: Reference Circuits of STATUS

NOTE

The status pin cannot be used as indication of module shutdown status when VBAT is removed.

3.18. Behaviors of the MAIN_RI

AT+QCFG="risignaltype","physical" can be used to configure MAIN_RI behaviors.

No matter on which port a URC is presented, the URC will trigger the behaviors of MAIN_RI pin.

NOTE

The URC can be outputted via UART port, USB AT port and USB modem port, which can be set by **AT+QURCCFG** command. The default port is USB AT port.

In addition, MAIN_RI behavior can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 23: Behaviors of the MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns

The MAIN_RI behavior can be changed via **AT+QCFG="urc/ri/ring"***. Please refer to ***document [2]*** for details.

NOTE

"*" means under development.

3.19. FORCE_USB_BOOT Interface

EC200S-CN provides a FORCE_USB_BOOT pin. Customers can pull up FORCE_USB_BOOT to 1.8 V before VDD_EXT is powered up, and the module will enter emergency download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 24: Pin Definition of FORCE_USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
FORCE_ USB_BOOT	115	DI	Force the module to enter emergency download mode	1.8 V power domain. Active high. It is recommended to reserve test points.

The following figure shows a reference circuit of FORCE_USB_BOOT interface.

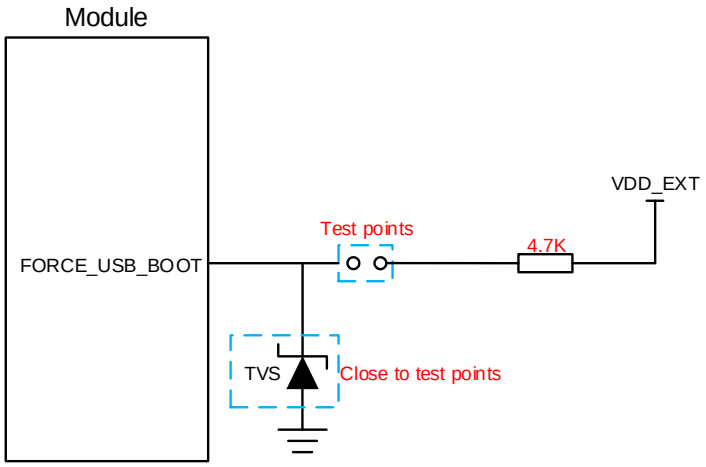


Figure 28: Reference Circuit of FORCE_USB_BOOT Interface

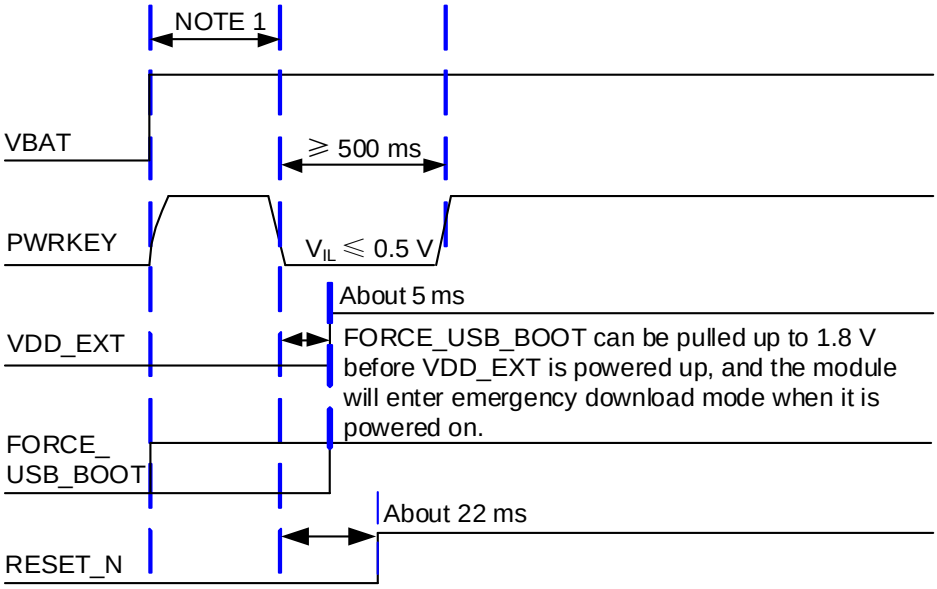


Figure 29: Timing Sequence for Entering Emergency Download Mode

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. When using MCU to control module to enter the emergency download mode, please follow the above timing sequence. It is not recommended to pull up FORCE_USB_BOOT to 1.8 V before powering up VBAT. Directly connect the test points as shown in ***Figure 28*** can manually force the module to enter download mode.

4 Antenna Interface

EC200S-CN provides a main antenna interface .The antenna port has an impedance of 50 Ω.

4.1. Main Antenna Interface

4.1.1. Pin Definition

The pin definition of main antenna is shown below.

Table 25: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	IO	Main antenna	50 Ω impedance

4.1.2. Operating Frequency

Table 26: Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-TDD B34	2010–2025	2010–2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz

LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2535–2675	2535–2675	MHz

4.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN pads is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

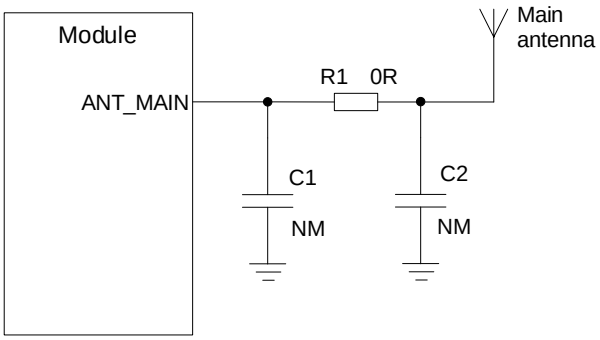


Figure 30: Reference Circuit of RF Antenna Interface

NOTE

Place the π-type matching components (R1&C1&C2) as close to the antenna as possible.

4.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the space between the RF trace and the ground (S). Microstrip and coplanar waveguide are typically used in RF layout to control characteristic impedance. The following figures are reference designs of microstrip or coplanar waveguide with different PCB structures.

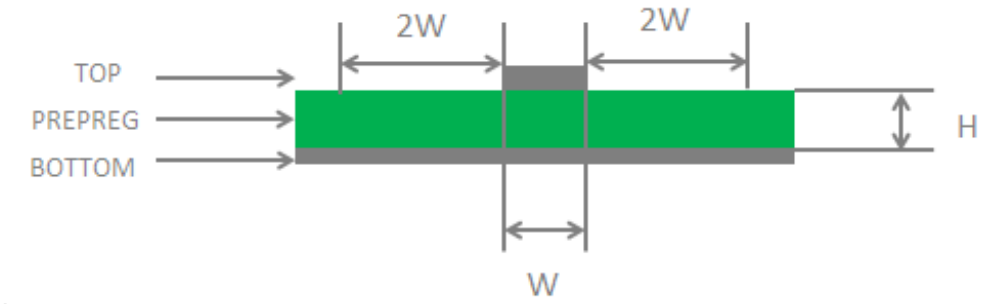


Figure 31: Microstrip Design on a 2-layer PCB

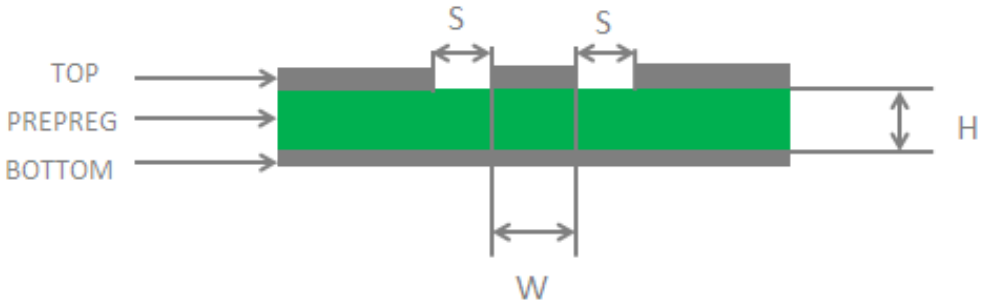


Figure 32: Coplanar Waveguide Design on a 2-layer PCB

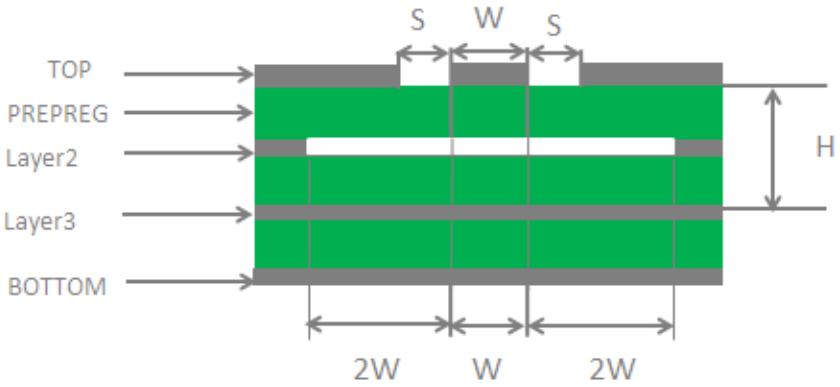


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

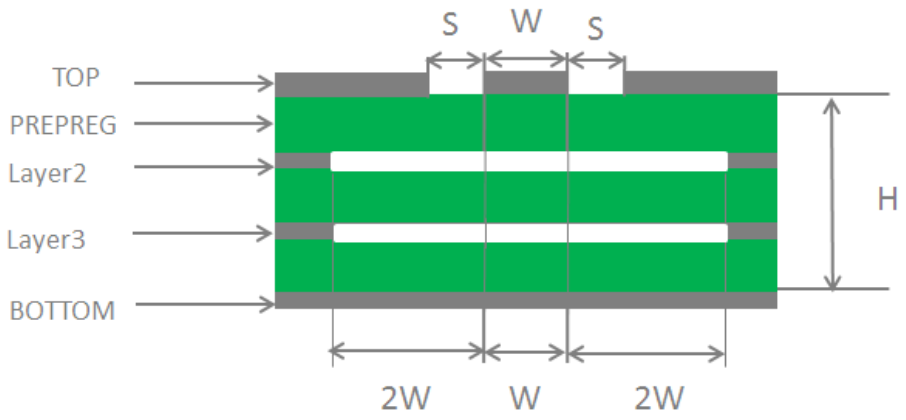


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedance of RF traces as 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).

For more details about RF layout, please refer to ***document [3]***.

4.2. Antenna Installation

4.2.1. Antenna Requirement

The following table shows the requirements on main antenna.

Table 27: Antenna Requirements

Type	Requirements
GSM/UMTS/LTE	VSWR: ≤ 2 Efficiency: > 30% Max input power: 50 W

	Input impedance: 50 Ω Cable insertion loss: < 1 dB (EGSM900, LTE-FDD B5/B8) Cable insertion loss: < 1.5 dB (DCS1800,, LTE B1/B3/B34/B39) Cable insertion loss: < 2 dB (LTE-TDD B38/B40/B41)

4.2.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by *Hirose*.

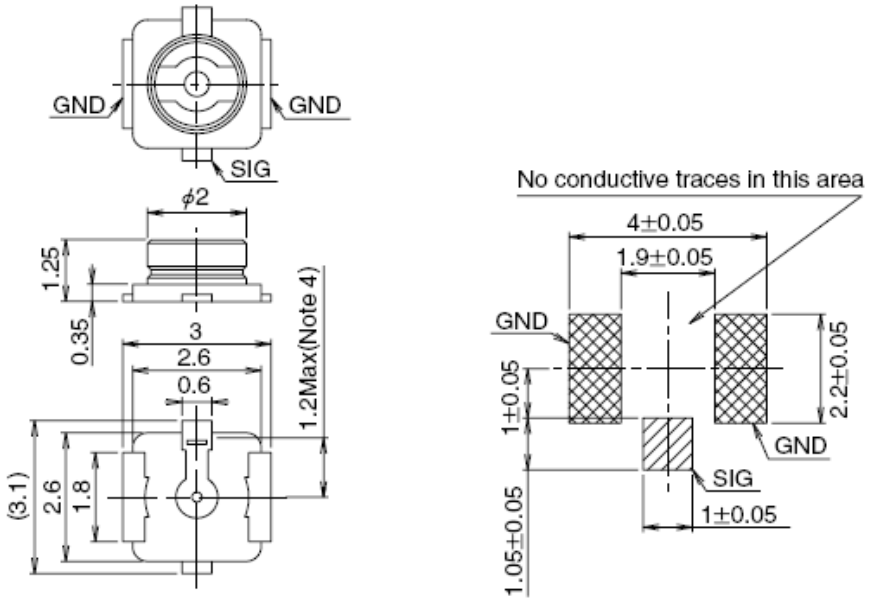


Figure 35: Dimensions of U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

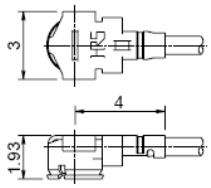
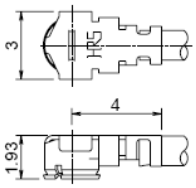
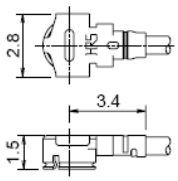
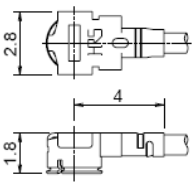
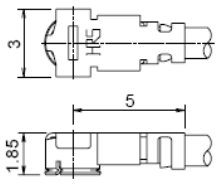
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 36: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

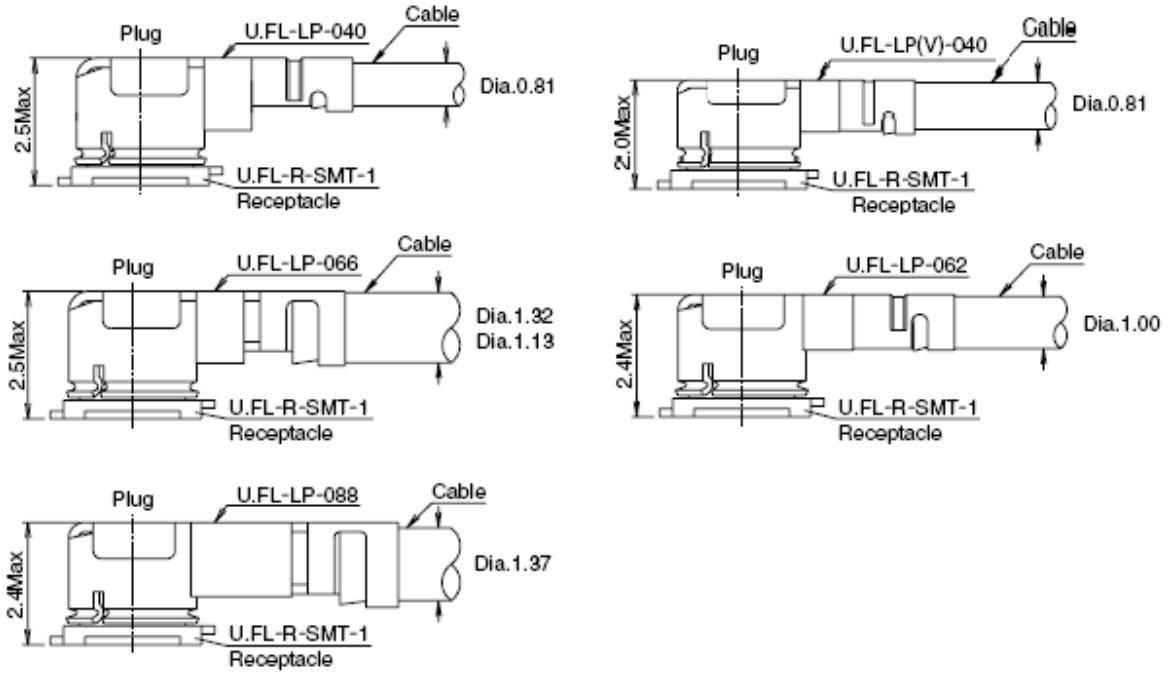


Figure 37: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

5 Electrical, Reliability and Radio Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 28: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

5.2. Power Supply Ratings

Table 29: The Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.4	3.8	4.5	V
	Voltage drop during burst transmission	Maximum power control level on EGSM900.			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900.		1.8	2.0	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

5.3. Operation and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 30: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range[1)]	-35	+25	+75	ºC
Extended Operation Range[2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operating temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

5.4. Current Consumption

The following table shows the current consumption of EC200S-CN will be supplemented in subsequent versions of this document.

Table 31: Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	13	μA
	Sleep state	**AT+CFUN=0** (USB disconnected)	0.704	mA
		EGSM900 @ DRX = 2 (USB disconnected)	1.498	mA
		EGSM900 @ DRX = 5 (USB disconnected)	1.030	mA
		EGSM900 @ DRX = 5 (USB suspend)	TBD	mA
		EGSM900 @ DRX = 9 (USB disconnected)	0.893	mA
		DCS1800 @ DRX = 2 (USB disconnected)	1.503	mA
		DCS1800 @ DRX = 5 (USB disconnected)	1.024	mA
		DCS1800 @ DRX = 5 (USB suspend)	TBD	mA
		DCS1800 @ DRX = 9 (USB disconnected)	0.880	mA
		LTE-FDD @ PF = 32 (USB disconnected)	1.734	mA
		LTE-FDD @ PF = 64 (USB disconnected)	1.203	mA
		LTE-FDD @ PF = 64 (USB suspend)	TBD	mA
		LTE-FDD @ PF = 128 (USB disconnected)	0.925	mA
		LTE-FDD @ PF = 256 (USB disconnected)	0.807	mA
		LTE-TDD @ PF = 32 (USB disconnected)	1.735	mA
		LTE-TDD @ PF = 64 (USB disconnected)	1.195	mA
		LTE-TDD @ PF = 64 (USB suspend)	TBD	mA
		LTE-TDD @ PF = 128 (USB disconnected)	0.931	mA

		LTE-TDD @ PF = 256 (USB disconnected)	0.790	mA
	Idle state	EGSM900 @ DRX = 5 (USB disconnected)	14.65	mA
		EGSM00 @ DRX = 5 (USB connected)	25.04	mA
		LTE-FDD @ PF = 64 (USB disconnected)	14.83	mA
		LTE-FDD @ PF = 64 (USB connected)	25.14	mA
		LTE-TDD @ PF = 64 (USB disconnected)	14.78	mA
		LTE-TDD @ PF = 64 (USB connected)	25.13	mA
	GPRS data transfer	EGSM900 4DL/1UL @ 32.07 dBm	246.5	mA
		EGSM900 3DL/2UL @ 32.02 dBm	462.2	mA
		EGSM900 2DL/3UL @ 30.98 dBm	603.5	mA
		EGSM900 1DL/4UL @ 29.46 dBm	667.7	mA
		DCS1800 4DL/1UL @ 29.73 dBm	190.2	mA
		DCS1800 3DL/2UL @ 29.65 dBm	348.2	mA
		DCS1800 2DL/3UL @ 28.22 dBm	438.7	mA
		DCS1800 1DL/4UL @ 26.32 dBm	485.4	mA
	EDGE data transfer	EGSM900 4DL/1UL @ 25.76 dBm	186.9	mA
		EGSM900 3DL/2UL @ 25.60 dBm	359.5	mA
		EGSM900 2DL/3UL @ 27.08 dBm	491.9	mA
		EGSM900 1DL/4UL @ 22.92 dBm	640.4	mA
		DCS1800 4DL/1UL @ 25.14 dBm	148.1	mA
		DCS1800 3DL/2UL @ 25.10 dBm	272.9	mA
		DCS1800 2DL/3UL @ 23.53 dBm	383.7	mA
		DCS1800 1DL/4UL @ 21.45 dBm	493.3	mA
	LTE data transfer	LTE-FDD B1 @ 22.98 dBm	542.1	mA
		LTE-FDD B3 @ 22.83 dBm	536.9	mA

		LTE-FDD B5 @ 22.82 dBm	491.8	mA
		LTE-FDD B8 @ 23.04 dBm	511.6	mA
		LTE-TDD B34 @ 22.63 dBm	271.2	mA
		LTE-TDD B38 @ 22.49 dBm	279.5	mA
		LTE-TDD B39 @ 22.59 dBm	262.0	mA
		LTE-TDD B40 @ 22.55 dBm	262.5	mA
		LTE-TDD B41 @ 22.51 dBm	275.2	mA
	GSM voice call	EGSM900 PCL = 5 @ 32.09 dBm	257.6	mA
		EGSM900 PCL = 12 @ 19.57 dBm	93.0	mA
		EGSM900 PCL = 19 @ 5.56 dBm	61.2	mA
		DCS1800 PCL = 0 @ 29.66 dBm	197.5	mA
		DCS1800 PCL = 7 @ 17.14 dBm	85.1	mA
		DCS1800 PCL = 15 @ 1.42 dBm	56.8	mA

5.5. RF Output Power

The following table shows the RF output power of EC200S-CN module.

Table 32: RF Output Power

Frequency	Max.	Min.
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots Tx mode, the maximum output power is reduced by 2.5 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

5.6. RF Receiving Sensitivity

The following table shows conducted RF receiving sensitivity of EC200S-CN module.

Table 33: Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
EGSM900	-108.5 dBm	NA	NA	-102 dBm
DCS1800	-108.5 dBm	NA	NA	-102 dBm
LTE-FDD B1 (10 MHz)	-98.0 dBm	NA	NA	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.0 dBm	NA	NA	-93.3 dBm
LTE-FDD B5 (10 MHz)	-97.5 dBm	NA	NA	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.0 dBm	NA	NA	-93.3 dBm
LTE-TDD B34 (10 MHz)	-97.5 dBm	NA	NA	-96.3 dBm
LTE-TDD B38 (10 MHz)	-97.5 dBm	NA	NA	-96.3 dBm
LTE-TDD B39 (10 MHz)	-97.5 dBm	NA	NA	-96.3 dBm
LTE-TDD B40 (10 MHz)	-97.5 dBm	NA	NA	-96.3 dBm
LTE-TDD B41 (10 MHz)	-96.5 dBm	NA	NA	-94.3 dBm

5.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatics discharge characteristics.

Table 34: Electrostatics Discharge Characteristics (25 ºC, 45% Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	TBD	TBD	kV
Main Antenna Interface	TBD	TBD	kV
Other Interfaces	TBD	TBD	kV

6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05 mm unless otherwise specified.

6.1. Mechanical Dimensions of the Module

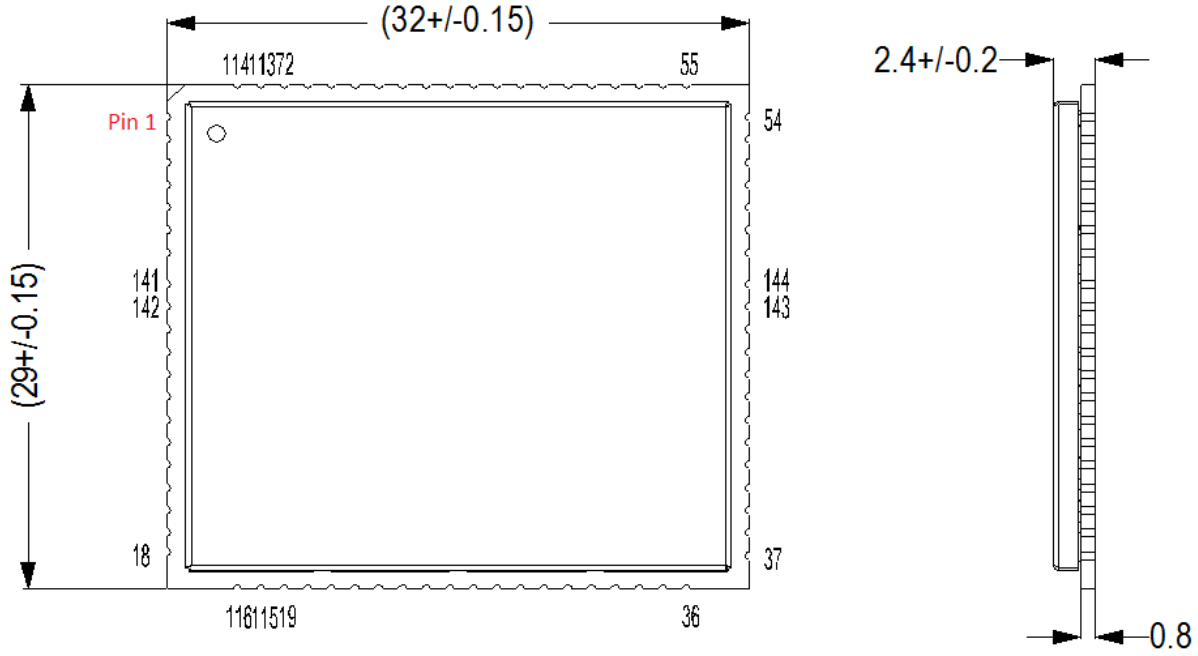


Figure 38: Module Top and Side Dimensions

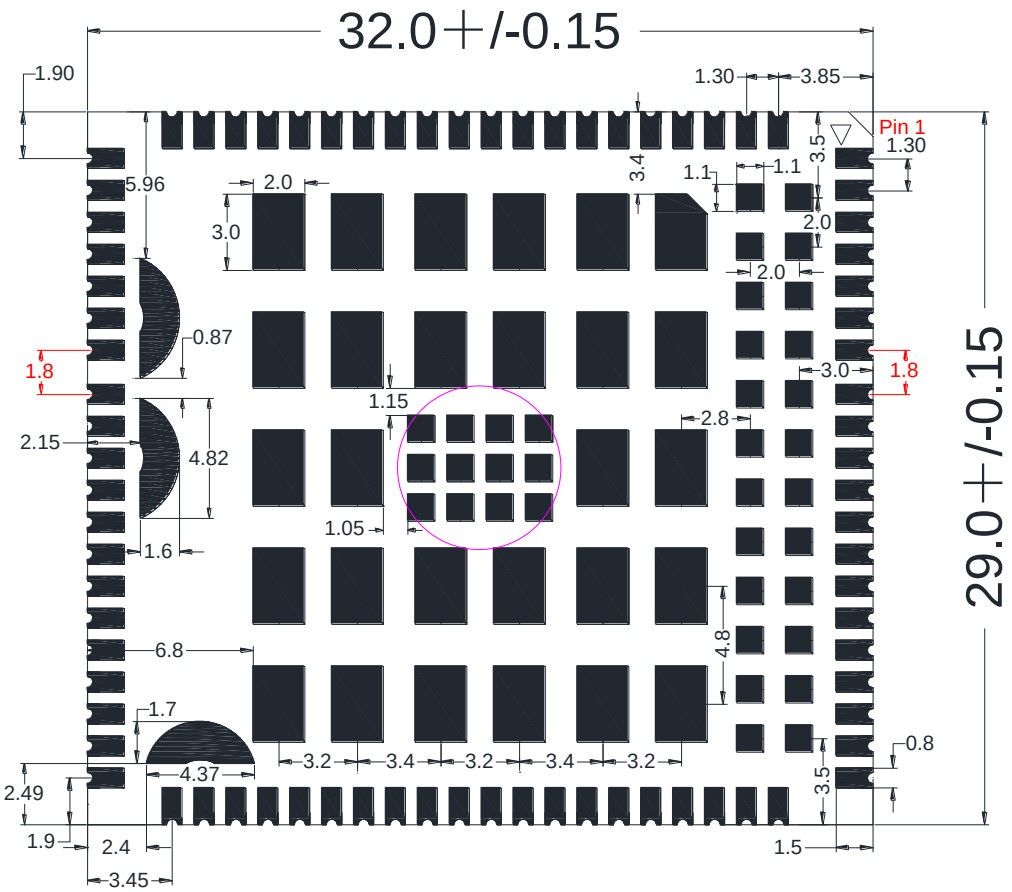


Figure 39: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

6.2. Recommended Footprint

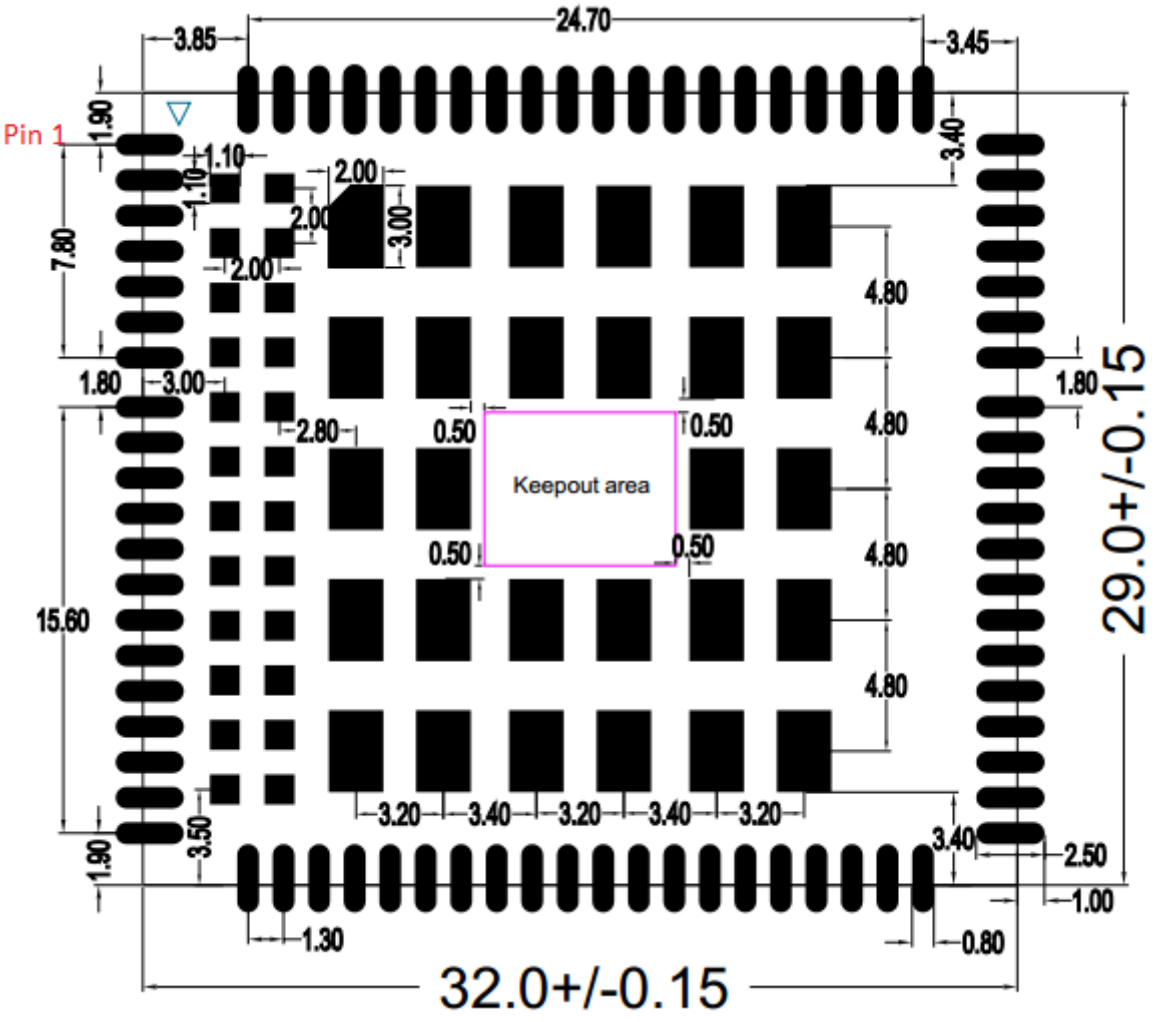


Figure 40: Recommended Footprint (Top View)

NOTES

1. The keepout area should not be designed.
2. For easy maintenance of the module, please keep about 3 mm between the module and other components in the host PCB.

6.3. Design Effect Drawings of the Module

Figure 41: Top View of the Module

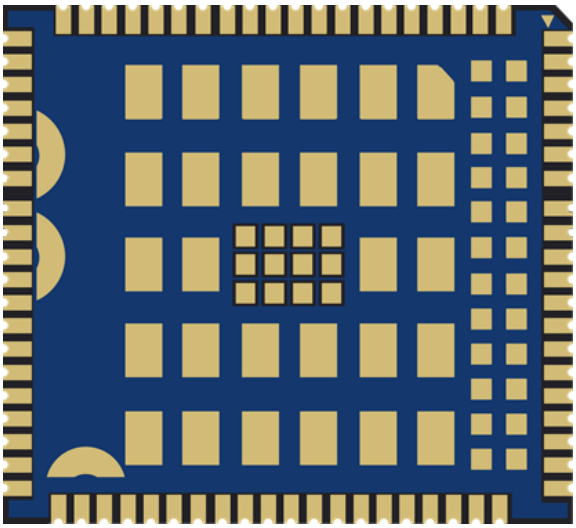


Figure 42: Bottom View of the Module

NOTE

These are renderings of EC200S-CN module. For authentic appearance, please refer to the module that you receive from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage

EC200S-CN is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35%–60%.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 24 hours in a plant where the temperature is 23 ±5 °C and relative humidity is below 60%. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 24 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10% (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTE

Please take the module out of the packaging and put it on high-temperature resistant fixtures before the baking. If shorter baking time is desired, please refer to *IPC/JEDEC J-STD-033* for baking procedure.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, please refer to ***document [1]***.

It is suggested that the peak reflow temperature is 238–246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

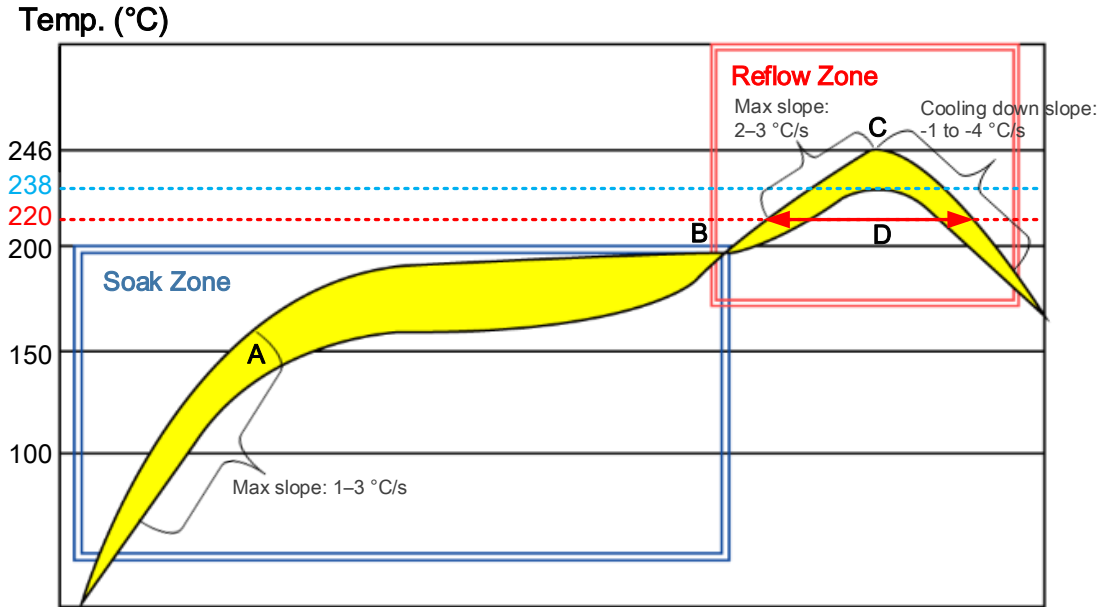


Figure 43: Reflow Soldering Thermal Profile

Table 35: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150°C and 200°C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 220 °C)	45–70 s
Max temperature	238–246 °C
Cooling down slope	-1 to -4 °C/s
Reflow Cycle	
Max reflow cycle	1

7.3. Packaging

EC200S-CN is packaged in tape and reel carriers. One reel is 11.88m long and contains 250 modules. The figure below shows the package details, measured in mm.

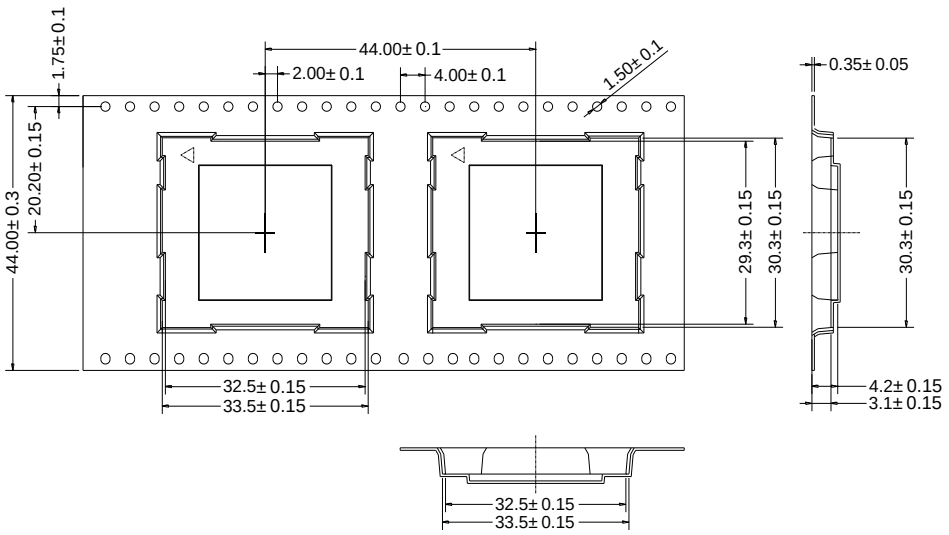


Figure 44: Tape Specifications

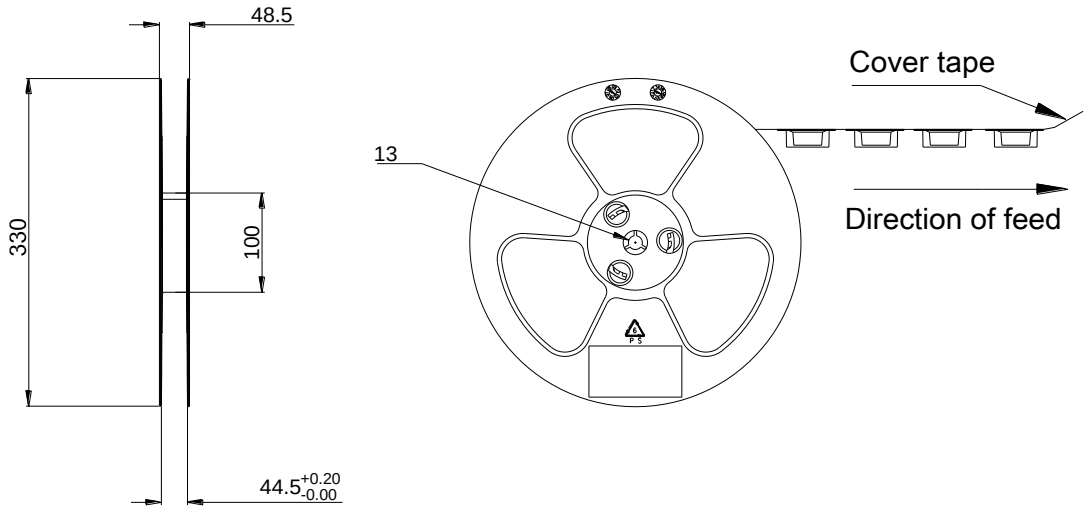


Figure 45: Reel Specifications

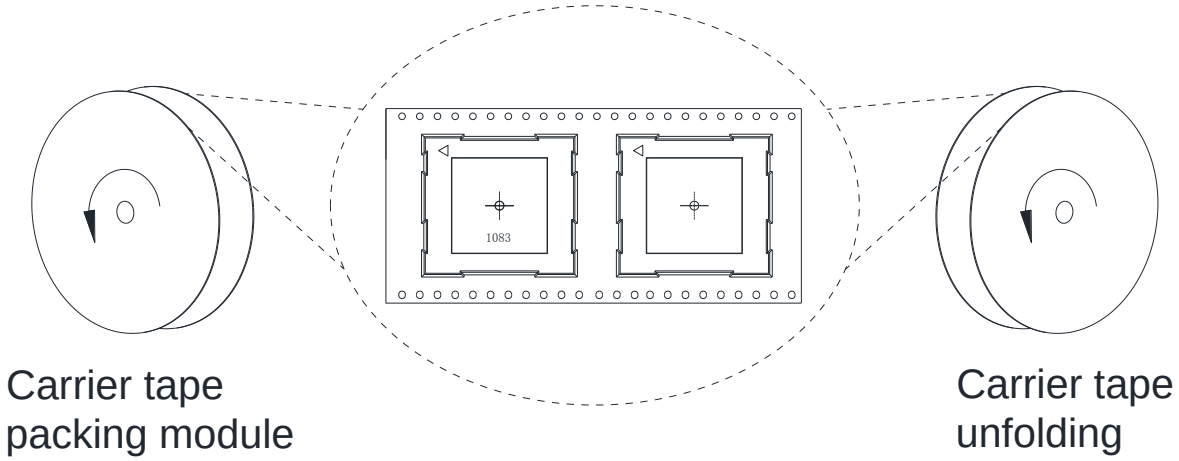


Figure 46: Tape and Reel Directions

8 Appendix A References

Table 36: Related Documents

SN	Document Name	Remark
[1]	Quectel_Module_Secondary_SMT_User_Guide	Module secondary SMT user guide
[2]	Quectel_EC200S-CN_AT_Commands_Manual	EC200S-CN AT commands manual
[3]	Quectel_RF_Layout_Application_Note	RF Layout application note
[4]	Quectel_UMTS&LTE_EVB_User_Guide	UMTS&LTE EVB user guide for UMTS&LTE modules

Table 37: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DL	Downlink
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
EGSM	Extended GSM900 Band (including standard GSM900 band)

ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP over SSL
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hyper Text Transfer Protocol
HTTPS	Hyper Text Transfer Protocol over Secure Socket Layer
LED	Light Emitting Diode
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MMS	Multimedia Messaging Service
MSL	Moisture Sensitivity Level
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PF	Paging Frame
PPP	Point-to-Point Protocol

PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SIMO	Single Input Multiple Output
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver &Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
$V_I$max	Absolute Maximum Input Voltage Value

V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WLAN	Wireless Local Area Network

9 Appendix B GPRS Coding Schemes

Table 38: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

10 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3 + 1 or 2 + 2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 39: GPRS Multi-slot Classes

Multi-slot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA

14	4	4	NA
15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

11 Appendix D EDGE Modulation and Coding Schemes

Table 40: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	Timeslot 1	Timeslot 2	Timeslot 4
CS-1	GMSK	/	9.05 kbps	18.1 kbps	36.2 kbps
CS-2	GMSK	/	13.4 kbps	26.8 kbps	53.6 kbps
CS-3	GMSK	/	15.6 kbps	31.2 kbps	62.4 kbps
CS-4	GMSK	/	21.4 kbps	42.8 kbps	85.6 kbps
MCS-1	GMSK	C	8.80 kbps	17.60 kbps	35.20 kbps
MCS-2	GMSK	B	11.2 kbps	22.4 kbps	44.8 kbps
MCS-3	GMSK	A	14.8 kbps	29.6 kbps	59.2 kbps
MCS-4	GMSK	C	17.6 kbps	35.2 kbps	70.4 kbps
MCS-5	8-PSK	B	22.4 kbps	44.8 kbps	89.6 kbps
MCS-6	8-PSK	A	29.6 kbps	59.2 kbps	118.4 kbps
MCS-7	8-PSK	B	44.8 kbps	89.6 kbps	179.2 kbps
MCS-8	8-PSK	A	54.4 kbps	108.8 kbps	217.6 kbps
MCS-9	8-PSK	A	59.2 kbps	118.4 kbps	236.8 kbps