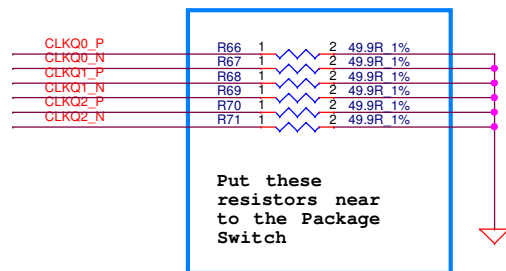
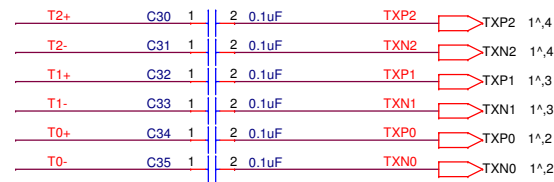


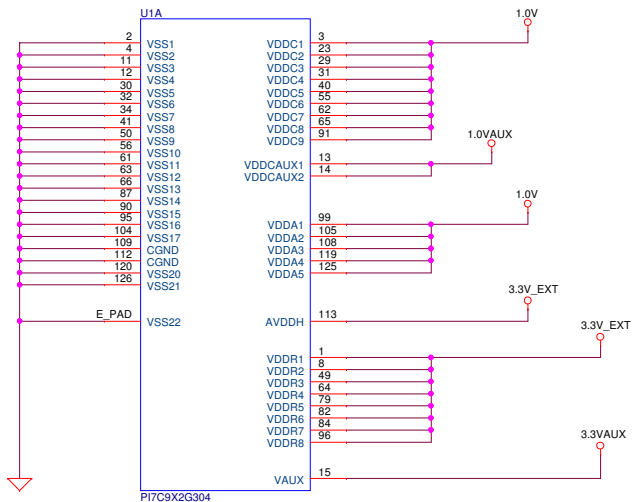
- # Notice #
1. If the reference clock input is HCSL type, it can be AC or DC coupling.
 2. If the 100MHz clock source is not in HCSL protocol (ex: LVPECL, LVDS , etc), Please refer to application note to add application circuit.

Clock Output Termination Resistors

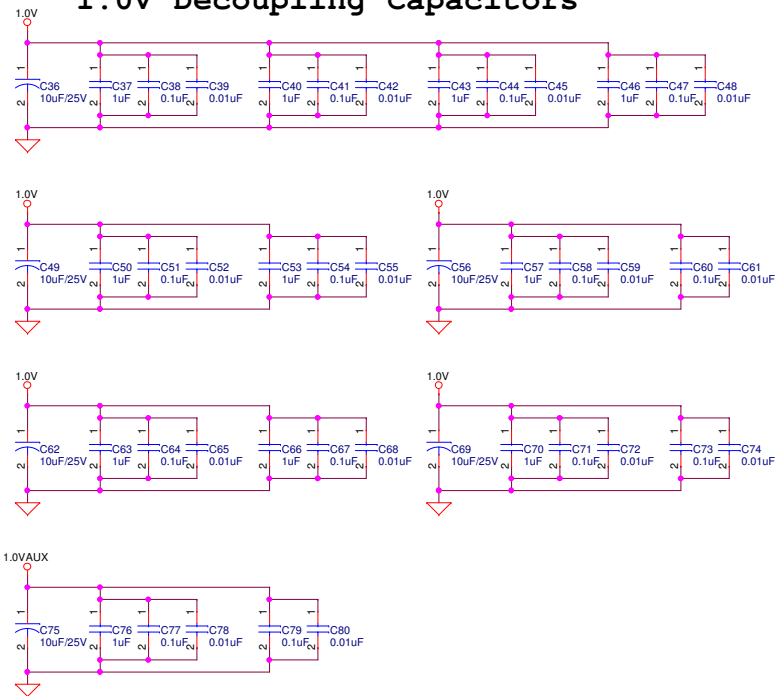


Tx AC Coupling Capacitors

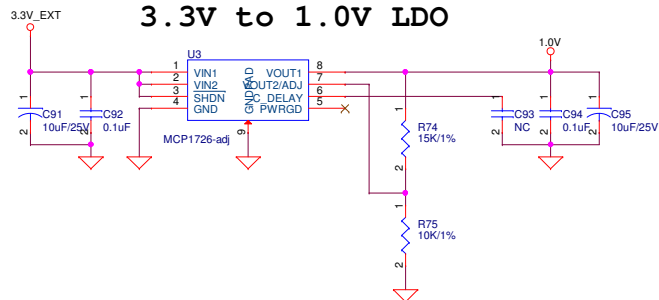




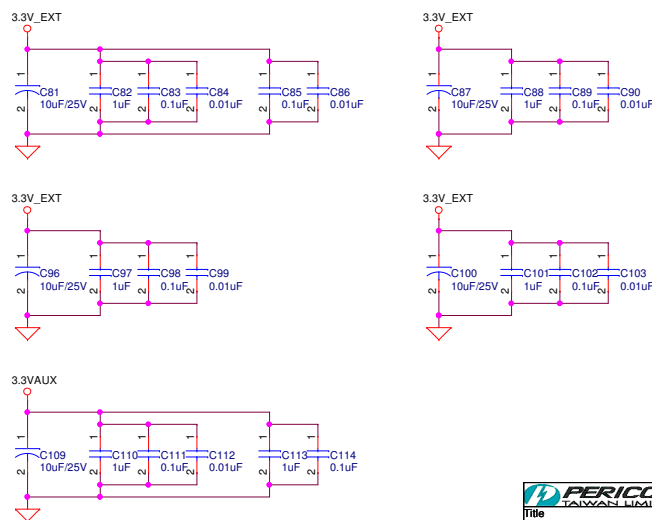
1.0V Decoupling Capacitors



3.3V to 1.0V LDO



3.3V Decoupling Capacitors



Standard Resistor Values
 10K 11K 12K 13K 15K 16K 18K
 20K 22K 24K 27K
 30K 33K 36K 39K
 43K 47K
 51K 56K
 62K 68K
 75K
 82K
 91K

$R1:R2=1.5:1$
 $V_{out}=V_{adj}\{(R1+R2)/R2\}$
 $V_{adj}=0.41V$
 value range for resistor R2
 is from 10 kΩ to 200 kΩ

