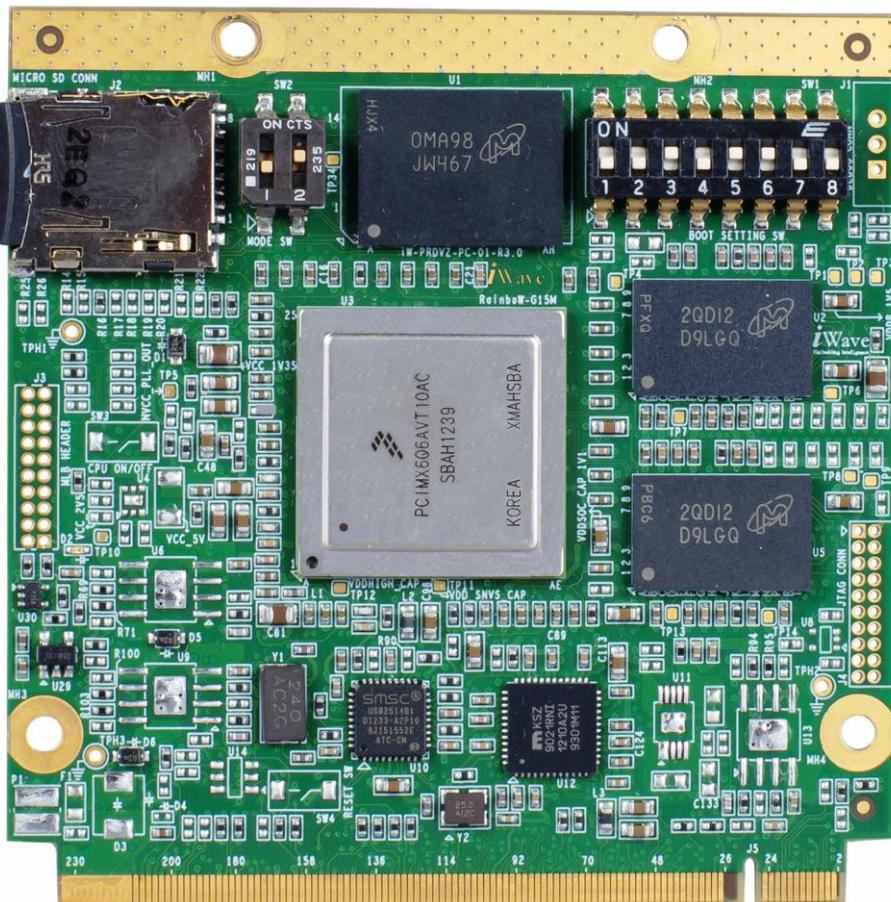


# iW-RainboW-G15M

## i.MX6 Qseven System On Module

### Hardware User Guide



**iWave**  
Embedding Intelligence

## Document Revision History

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## 1. INTRODUCTION

### 1.1 Purpose

This document is the Hardware User Guide for the i.MX6 Qseven System On Module based on the Freescale's i.MX6 Applications Processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX6 Qseven System On Module from a Hardware Systems perspective.

### 1.2 Qseven System On Module Overview

The Qseven concept is an off-the-shelf, multi-vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven modules have a standardized form factor of 70mm x70mm and have specified pin outs based on the high speed MXM system connector that has a standardized pin out regardless of the vendor. A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven module.

### 1.3 List of Acronyms

The following acronyms will be used throughout this document.

**Table 1: Acronyms & Abbreviations**

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BOM	Bill of Material
BPP	Bits Per Pixel
CAN	Controller Area Network
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR3	Double Data Rate 3
DSI	Display Serial Interface
eCSPI	Enhanced Configurable Serial Peripheral Interface
eMMC	Enhanced Multi Media Card
ESAI	Enhanced Serial Audio Interface
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output

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HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signal
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz
MIPI	Mobile Industry CPU Interface
MLB	Media Local Bus
MMC	Multi Media Card
NC	No Connect
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RGMII	Reduced Gigabit Media Independent Interface
ROM	Read-Only Memory
RTC	Real Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SOM	System On Module
SPDIF	Sony/Philips Digital Interconnect Format
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
TMDS	Transition Minimized Differential Signalling
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USBOTG	Universal Serial Bus On The Go

## 1.4 References

- i.MX6 Applications Processors Products Datasheet
- i.MX6 Applications Processor Reference Manual
- Qseven Specification Revision 1.2

## 1.5 Important Note

In this document, wherever i.MX6 CPU signal name is mentioned, it is followed as per below format.

- If CPU pin functionality name and CPU pad name is same, Signal name is mentioned as  
**“CPU\_Pad\_Name”**

**Example: SD3\_DATA2**

In this signal, functionality which we are using and CPU Pad name is **SD3\_DATA2**.

- If CPU pin functionality name and pad name is different, Signal name is mentioned as  
**“Functionality\_name (CPU\_Pad\_name)”**

**Example: UART3\_RTS (SD3\_RST)**

In this signal, **UART3\_RTS** is the functionality which we are using and **SD3\_RST** is the CPU Pad name.

- If CPU pin functionality is GPIO, Signal name is mentioned as  
**“GPIONumber\_FunctionalityDescription (CPU\_Pad\_name)”**

**Example: GPIO7\_0\_SD1\_CD(SD3\_DAT5)**

In this signal, **GPIO7\_0** is the GPIO number, **SD1\_CD** (SD1 card detect) is the functionality which we are using and **SD3\_DAT5** is the CPU pad name.

*Note: The above naming is not applicable for other signals which are not connected to CPU.*

## 2. i.MX6 SOM ARCHITECTURE AND DESIGN

This section provides detailed information about the i.MX6 Qseven SOM Features and Hardware architecture with high level block diagram. Also this section provides detailed information about Qseven edge connector & Expansion connector's pin assignment and usage.

### 2.1 i.MX6 Qseven SOM Block Diagram

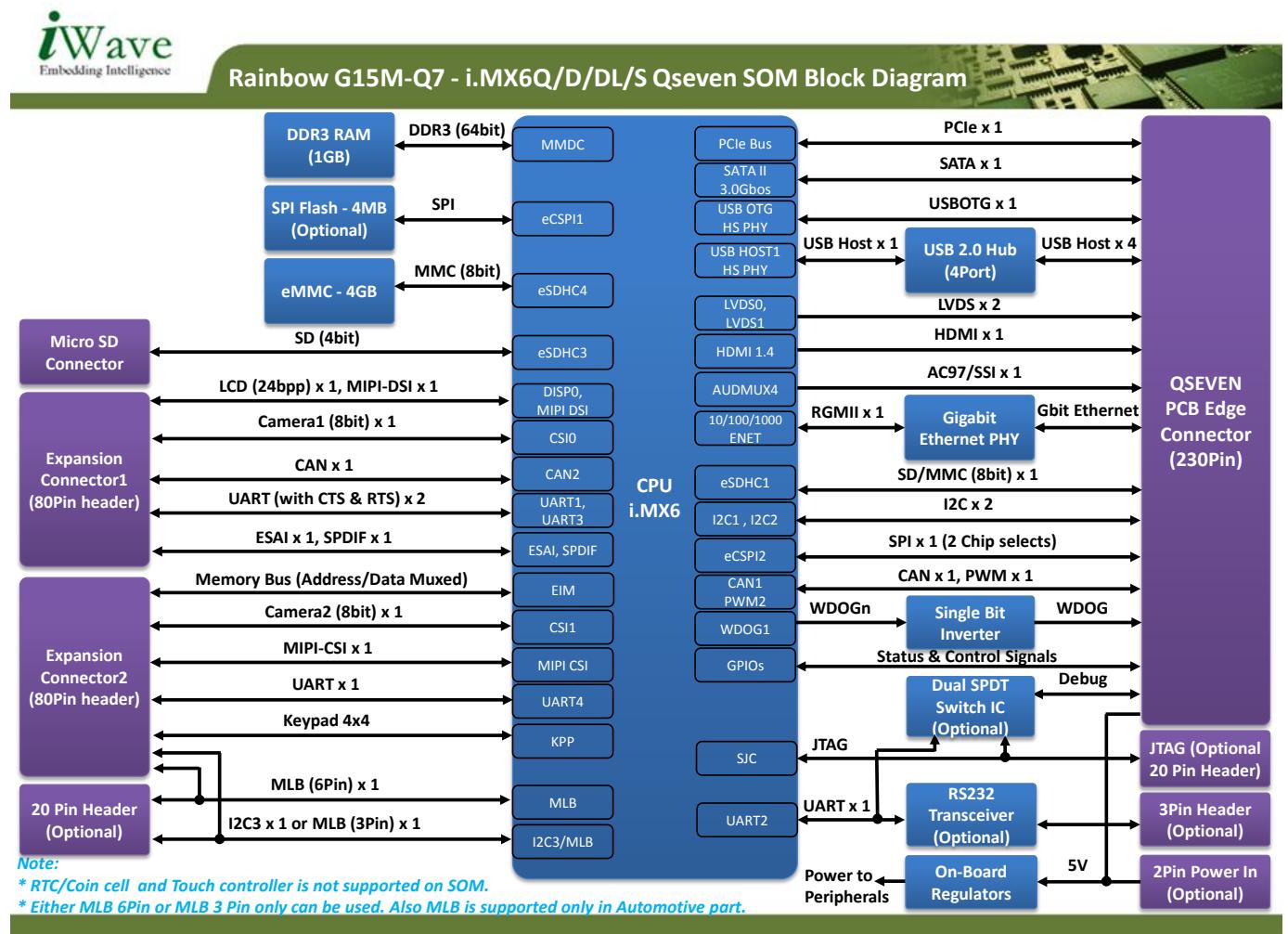


Figure 1: i.MX6 Qseven SOM Block Diagram

## 2.2 i.MX6 Qseven SOM Features

The i.MX6 Qseven SOM supports the following features.

### CPU

- Freescale's i.MX6 Quad/Dual/Solo ARM™ Cortex-A9 based CPU @ 1GHz/Core

### Boot Switches

- Boot Mode Settings Switch
- Boot Media Settings Switch

### Memory

- 1GB DDR3 RAM (Expandable)
- 4GB eMMC Flash (Expandable)
- Micro SD Slot
- SPI NOR Flash (Optional)

### Qseven PCB Edge Interfaces

- PCIe Gen2.0 (1 No.)
- SATA II (1 No.)
- USBOTG 2.0 (1 No.)
- USB Host 2.0 (4 Nos.) through On-SOM 1 to 4 port USB Hub
- LVDS (2 Nos.)
- HDMI 1.4 (1 No.)
- AC97/SSI Audio (1 No.)
- Gigabit Ethernet through On-SOM Gigabit Ethernet PHY (1 No.)
- SD/MMC (8bit)
- I2C (2 No.)
- SPI (1no. with 2 Chip selects)
- Debug UART (1 No.)
- CAN1 (1 No.)
- WDOG (1 No.)
- PWM (1 No.)

## Expansion Connector1 Interfaces

- LCD - 24bpp RGB (1 No.)
- MIPI-DSI (1 No.)
- Camera1 (8bit)
- UART1 (with CTS & RTS) (1 No.)
- UART3 (with CTS & RTS) (1 No.)
- ESAI (1 No.)
- SPDIF (1 No.)
- CAN2 (1 No.)

## Expansion Connector2 Interfaces

- Memory Bus (Address & Data Multiplexed)
- Camera2(8bit)
- MIPI-CSI (1 No.)
- UART4 (1 No.)
- 4x4 Keypad (1 No.)
- MLB (6pin) or MLB (3pin)

## Optional Features

- JTAG Header
- RS232 Debug UART Header(3Pin) - For Standalone operation
- 5V Power In connector (2Pin) - For Standalone operation
- 20Pin Header - MLB (6pin), MLB (3pin) or I2C3, GPIOs (2nos)

## General Specification

- Power Supply : 5V, 2A
- Temperature : -40°C to +85°C Industrial grade
- Form Factor : 70mm X 70mm (Qseven R1.2 Specification)

## 2.3 i.MX6 CPU

i.MX6 Qseven SOM is based on Freescale's i.MX6 Quad/Dual/Solo ARM™ Cortex-A9 core based CPU which can operate up to 1 GHz speed/core. i.MX6 CPU is Freescale's latest achievement in integrated multimedia application processors which is part of growing multimedia-focused products that offers high performance processing and are optimized for lowest power consumption. The simplified Block Diagram of i.MX6 CPU is shown below for your reference.

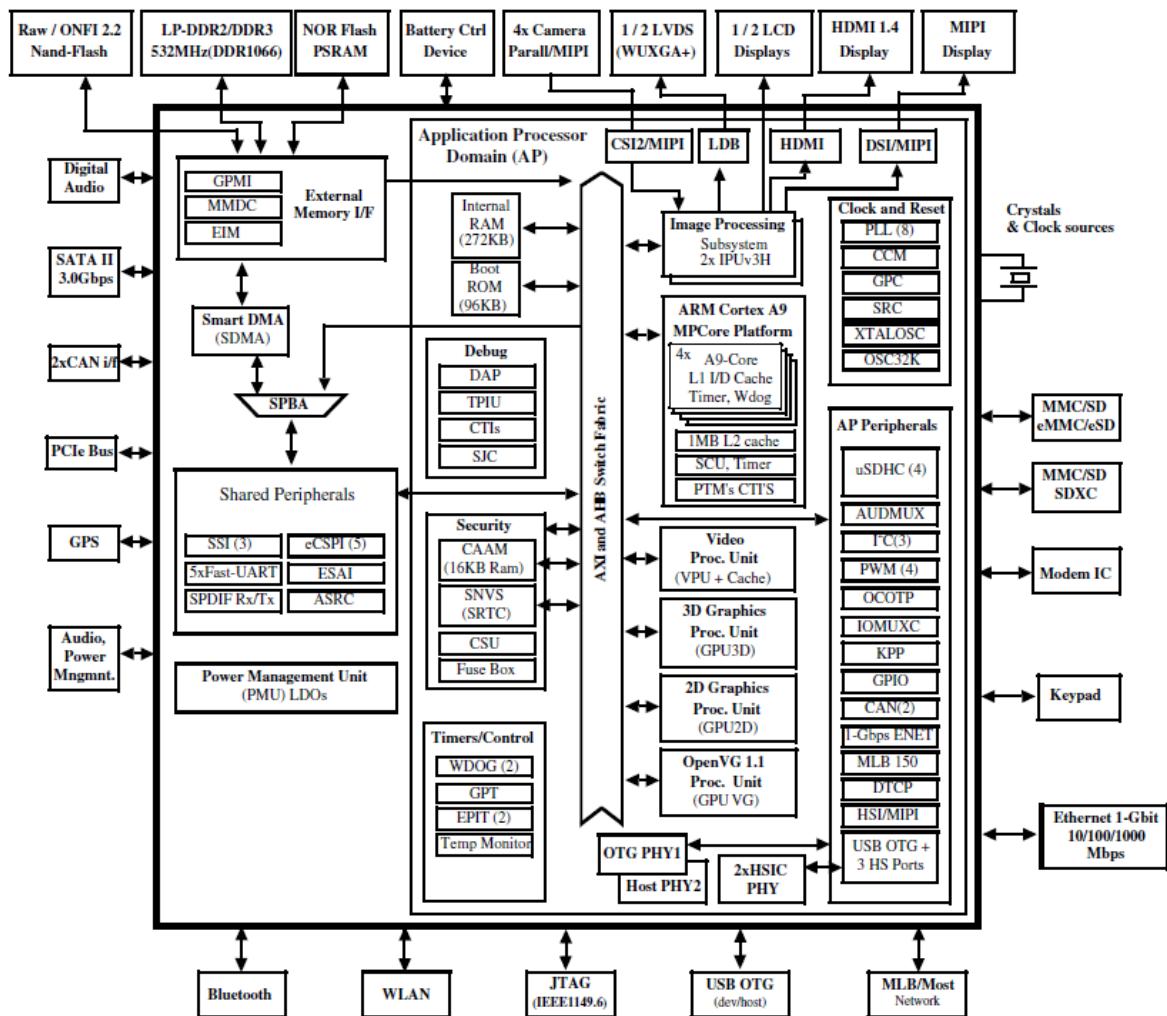


Figure 2: i.MX6 CPU Simplified Block Diagram

*Note: Please refer the latest i.MX6 Datasheet & Reference Manual from Freescale website for Electrical characteristics of i.MX6 Application CPU which may be revised from time to time.*

## 2.4 Boot Switches

i.MX6 CPU boot process begins at Power On Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. The i.MX6 Boot ROM code uses the state of the internal register **BOOT\_MODE [1:0]** as well as the state of various eFUSES and/or GPIO settings to determine the boot flow behaviour of the device.

i.MX6 Qseven SOM supports two Boot switches for selecting Boot Mode setting and Boot Media setting of i.MX6 CPU.

1. Boot Mode Setting Switch
2. Boot Media Setting Switch

### 2.4.1 Boot Mode Switch

i.MX6 Qseven SOM supports two positions Boot Mode Switch (SW2) which is physically located in the top of the PCB. This switch is used to select the boot mode setting of i.MX6 CPU as explained in the below table.

**Table 2: Boot Mode Settings Truth Table**

Boot Mode Setting On i.MX6 SOM	Description	SW2 (2 Position Switch)		
		POS1	POS2	Image
Internal Boot Mode <b>(Default)</b>	In this mode, i.MX6 boot media is selected by GPIO Pin's settings	OFF	ON	
Boot From eFuses	In this mode, i.MX6 boot media is selected by i.MX6 eFUSE settings <i>Note: i.MX6 eFuse setting is NOT modified by iWave from silicon shipped value.</i>	OFF	OFF	
Serial Downloader Mode	In this mode, i.MX6 boot device can be Programmed through its USB OTG interface using MFG Tool	ON	OFF	
ON – High		OFF - Low		

## 2.4.2 Boot Media Switch

i.MX6 Qseven SOM supports Eight positions Boot Media Switch (SW1) which is physically located in the top of the PCB. This switch is used to select the boot media of i.MX6 CPU if i.MX6 CPU boot mode is selected as Internal Boot Mode. i.MX6 Qseven SOM supports different boot media options for booting i.MX6 CPU as explained in the below table.

**Table 3: Boot Media Settings Truth Table**

Boot Media Setting On i.MX6 SOM	SW1 (8 Position Switch)								Image
	POS1	POS2	POS3	POS4	POS5	POS6	POS7	POS8	
SD4 - 8bit eMMC <b>(Default)</b>	OFF	ON	ON	ON	ON	OFF	ON	OFF	
SD3 - 4bit Micro SD	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	
eCSPI1 - SPI Flash <b>(Optional)</b>	ON	ON	OFF	X	X	X	X	X	
SD1 - 4bit (Through Qseven Edge)	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	
SD1 - 8bit MMC (Through Qseven Edge)	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	
SATA - 3Gbps (Through Qseven Edge)	OFF	ON	OFF	OFF	OFF	X	X	X	
ON - High			OFF - Low					X - Don't Care	

## 2.5 Memory

### 2.5.1 DDR3 SDRAM

i.MX6 Qseven SOM uses four 256MB DDR3 SDRAM ICs to support a total on board RAM memory of 1GB (expandable). These devices will operate at 1.5V voltage level. The DRAM calibration resistor used on Qseven SOM is 240 Ohm 1% resistor. A pair of DDR3 IC is physically located on either side of the Qseven SOM.

### 2.5.2 eMMC Flash Memory

i.MX6 Qseven SOM supports 4GB eMMC (expandable) memory as default boot device. Also eMMC Flash can be used for Mass storage. eMMC is directly connected to the eSDHC Port 4 (SD4) of the i.MX6 CPU and operating under 3.3V Voltage level. The eMMC flash memory is physically located on top of the Qseven SOM.

### 2.5.3 Micro SD Slot

i.MX6 Qseven SOM supports Micro SD slot to connect Micro SD card for Mass storage also can be used as Boot device. Micro SD Card Connector (J2) is directly connected to the eSDHC Port 3 (SD3) of the i.MX6 Applications CPU. It supports card detect feature. The main power to Micro SD Card Connector is 3.3Voltage. Micro SD Connector is physically located on top of the Qseven SOM as shown below.

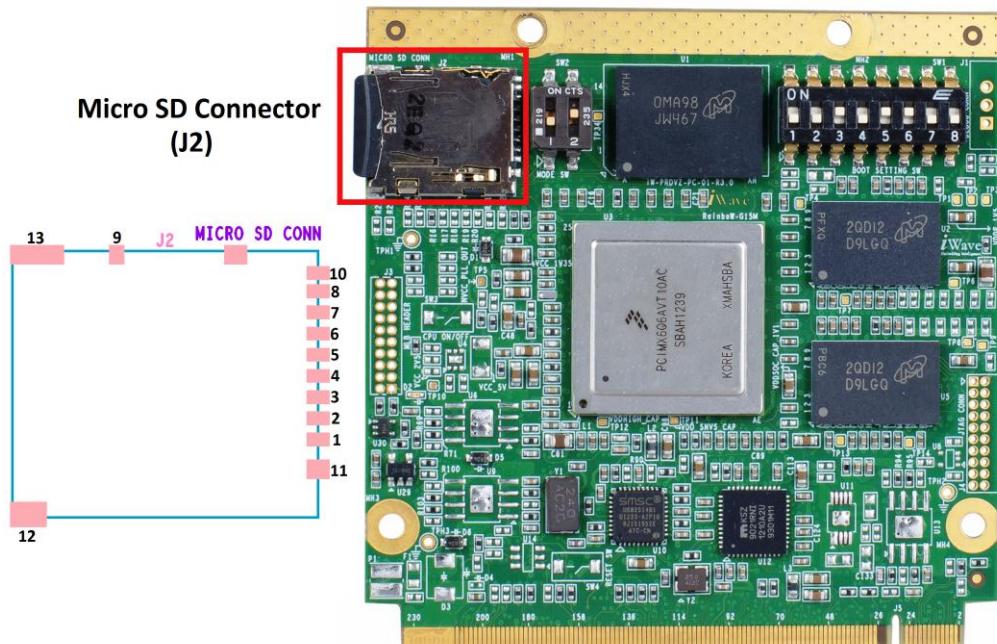


Figure 3: Micro SD Slot

**Table 4: Micro SD Connector Pin Assignment**

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	SD3_DATA2	Input / Output	3.3V CMOS	SD3 Data Line (Bit2)
2	SD3_DATA3	Input / Output	3.3V CMOS	SD3 Data Line (Bit3)
3	SD3_CMD	Input / Output	3.3V CMOS/ 10K Pull-up	SD3 Command Response
4	VCC_3V3	Power	3.3V	Card Supply Voltage
5	SD3_CLK	Output	3.3V CMOS	SD3 Clock
6	VSS	Power	0V	Ground
7	SD3_DATA0	Input / Output	3.3V CMOS	SD3 Data Line (Bit0)
8	SD3_DATA1	Input / Output	3.3V CMOS	SD3 Data Line (Bit1)
9	GPIO7_1_SD3_CD (SD3_DAT4)	Input	3.3V CMOS/ 10K Pull-up	SD3 Card Detect

#### 2.5.4 SPI NOR Flash Memory (Optional)

The i.MX6 Qseven SOM supports SPI NOR Flash and it can be used as Boot Device. This device operates under 3.3 Voltage level. This is the optional feature and will not be populated in default configuration. The below table provides the SPI Flash circuit BOM which can be used to mount the SPI Flash in i.MX6 Qseven SOM and check the functionality.

**Table 5: SPI NOR Flash - BOM**

Sl. No.	Part Description	Part Number	Identifier	Package	Quantity
1	16M SPI Flash Memory	SST25VF016B-50-4I-S2AF	U15	8-SOIC	1
2	RES 10.0K OHM 1/16W 5%	RC0402JR-0710KL	R9, R10,162	0402	3
3	CAP CER 10UF 10V X5R	C1608X5R1A106M	C4	0603	1
4	CAP CERAMIC .1UF 10V X5R	CC0402KRX5R6BB104	C12	0402	1

*Note: For i.MX6 SOM Silkscreen identifier details, refer APPENDIX I*

## 2.6 Qseven PCB Edge Connector

Qseven PCB edge connector has standard pin out as per Qseven Specification 1.20. The interfaces which are available at Qseven edge connector are listed below.

- **PCIe interface**

Qseven Edge connector has one PCI Express v2.0 lane. PCI express (Gen 2.0) dual mode complex supporting Root complex operations and Endpoint operations.

- **SATA interface**

Qseven Edge connector has one SATA II interface with speed up to 3.0 Gbps. This can be used to interface with different Hard disk drives. Also booting from SATA is supported.

- **USB OTG interface**

Qseven Edge connector has one High Speed USB 2.0 OTG port up to 480 Mbps using i.MX6 integrated High Speed USB PHY. Also in Serial Download Boot Mode, this interface can be used to program the i.MX6 CPU boot device using MFG Tool.

- **USB Host interface**

Qseven Edge connector has four High Speed (HS) USB 2.0 host. To support 4 USB hosts, the i.MX6 Qseven SOM uses 1 to 4 port USB hub “USB2514Bi” on SOM .This USB hub is interfaced with i.MX6 using i.MX6 integrated High Speed USB Host PHY.

- **LVDS interface**

Qseven Edge connector has two independent LVDS interfaces which are connected to LVDS0 & LVDS1 port of i.MX6 CPU. i.MX6 supports one LVDS port of up to 165 Mpixels/sec or two ports of up to 85 Mpixels/sec per port

- **HDMI interface**

Qseven Edge connector has one HDMI 1.4 port. HDMI is capable of transferring uncompressed video, audio and data using a single cable. The video pixel rates are typically from 25 MHz up to 297 MHz (4k x 2k and 3Dvideo modes), but HDMI can support higher rates up to 340MHz.

- **Audio interface**

Qseven Edge connector has one port AC'97 up to 1.4 Mbps, audio interface. This is supported using i.MX6's AUDMUX4- SSI interface. Also the same pins can be used as SSI interface.

- **Gigabit Ethernet interface**

Qseven Edge connector has one Gigabit Ethernet interface. To support Gigabit Ethernet, the i.MX6 Qseven SOM uses Gigabit Ethernet PHY “KSZ9021RNI” which works in 2.5V IO voltage level. This PHY is interfaced with i.MX6 using RGMII interface.

- **SD/MMC interface**

Qseven Edge connector has one 8bit SD/MMC interface using i.MX6 eSDHC1 interface along with Card Detect, Writ Protect and Power Enable pins using i.MX6 GPIOs.

- **I2C interface**

Qseven Edge connector has two I2C channels which can work up to 400 kbps.

- **SPI interface**

Qseven Edge connector has one SPI interface with two chip selects. This is supported using i.MX6's eCSPI2 interface which can work up to 66 Mbps write & 31Mbps read.

- **Debug UART interface**

Qseven Edge connector has JTAG and UART2 interface for debugging purpose. Since both interface pins are multiplexed in Qseven specification, only debug UART option is provided at Qseven edge connector in i.MX6 Qseven SOM.

- **CAN interface**

Qseven Edge connector has one CAN interface. This is supported using i.MX6's FLEXCAN1 interface which can work up to 1 Mbps speed.

- **WDOG interface**

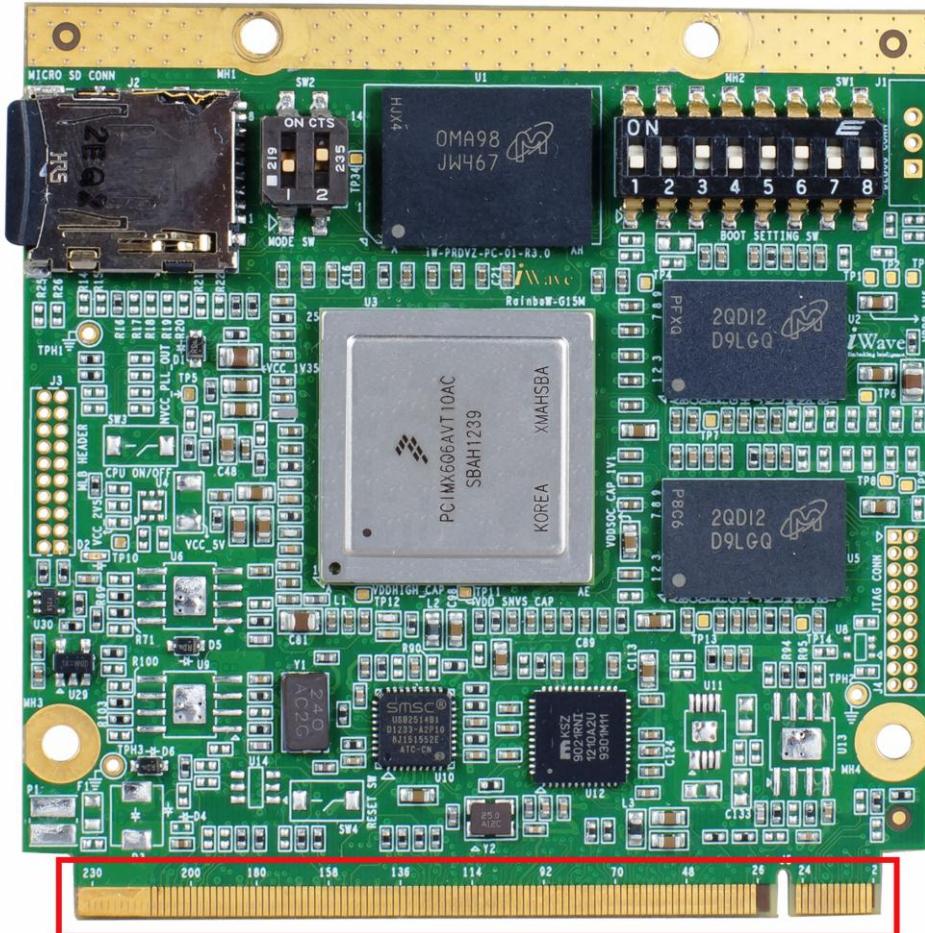
Qseven Edge connector supports Watchdog trigger input and event indicator output.

- **PWM interface**

Qseven Edge connector supports PWM interface which can be used to control the brightness of the LVDS LCD backlight.

- **UART Interface (Optional)**

Qseven Edge connector optionally supports UART interface as per Qseven Specification R2.0. This is supported using i.MX6's UART5 interface which can work up to 4Mbps speed.



**Qseven PCB Edge Connector (J5)**

**Top Side**



**Bottom Side**

**Figure 4: Qseven PCB Edge Connector**

Number of Pins	- 230
Connector Part	- Not Applicable (On Board PCB Edge connector)
Mating Connector	- AS0B326-S78N-7F from FOXCONN or 88882-2D0K from Aces

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**Table 6: 230-Pin PCB Edge Connector Pin Assignment**

Pin No.	Edge Connector Pin Name	Signal Name	Signal Type	Voltage Level/Termination	Description
1	GND1	GND	Power	0V	Ground
2	GND2	GND	Power	0V	Ground
3	GBE_MDI3-	GPHY_DTXRXM	Input/Output	Differential/On-PHY Termination	Gigabit Ethernet MDI differential pair 3 negative
4	GBE_MDI2-	GPHY_CTXRXM	Input/Output	Differential/On-PHY Termination	Gigabit Ethernet MDI differential pair 2 negative
5	GBE_MDI3+	GPHY_DTXRXP	Input/Output	Differential/On-PHY Termination	Gigabit Ethernet MDI differential pair 3 positive
6	GBE_MDI2+	GPHY_CTXRXP	Input/Output	Differential/On-PHY Termination	Gigabit Ethernet MDI differential pair 2 positive
7	LINK100#	GPHY_LINK_LED2	Output	3.3V CMOS	100Mbps Ethernet Link status LED. <i>Note: Same signal is also connected to Qseven edge connector 8<sup>th</sup> &amp; 13<sup>th</sup> pins. So use only in one place.</i>
8	GBE_LINK1000#	GPHY_LINK_LED2	Output	3.3V CMOS	Gigabit Ethernet Link status LED. <i>Note: Same signal is also connected to Qseven edge connector 7<sup>th</sup> &amp; 13<sup>th</sup> pins. So use only in one place.</i>
9	GBE_MDI1-	GPHY_BTXRXM	Input/Output	Differential/On-PHY Termination	Gigabit Ethernet MDI differential pair 1 negative
10	GBE_MDIO-	GPHY_ATXRXM	Input/Output	Differential/On-PHY Termination	Gigabit Ethernet MDI differential pair 0 negative

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11	GBE_MDI1+	GPHY_BTXRXP	Input/ Output	Differential/ On-PHY Termination	Gigabit Ethernet MDI differential pair 1 positive
12	GBE_MDI0+	GPHY_ATXRXP	Input/ Output	Differential/ On-PHY Termination	Gigabit Ethernet MDI differential pair 0 positive
13	GBE_LINK#	GPHY_LINK_LED2	Output	3.3V CMOS	Gigabit Ethernet Link status LED. <i>Note: Same signal is also connected to Qseven edge connector 7<sup>th</sup> &amp; 8<sup>th</sup> pins. So use only in one place.</i>
14	ACT#	GPHY_ACTIVITY_LED 1	Output	3.3V CMOS	Gigabit Ethernet Activity status LED
15	GBE_CTREF	VAVDDH_GPHY	Power Out	3.3V	Reference voltage for Gigabit Ethernet magnetics centre tap.
16	SUS_S5#/GPIO	EIM_WAIT	Output	3.3V CMOS	S5 State is not supported. EIM_WAIT signal is connected to this pin for GPIO purpose through resistor and default populated. <i>Note: EIM_WAIT signal is always connected to Expansion connector2 40<sup>th</sup> pin also.</i>
17	WAKE#/GPIO	GPIO6_10_WAKE(NA NDF_RBO)	Input	3.3V CMOS	External system wake event
18	SUS_S3#/GPIO	GPIO5_2_HDMI_CEC (EIM_A25)	Output	3.3V CMOS/ 10K Pull-up	S3 State is not supported. <i>Note: Optionally HDMI_CEC is connected to this pin through resistor and default not populated.</i> <i>Note: HDMI_CEC is also connected to Qseven edge connector 124<sup>th</sup> pin and</i>

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					<i>Expansion connector2 62<sup>nd</sup> pin through resistors and default both populated.</i>
19	SUS_STAT#/GPIO	GPIO6_9_SUS_STAT(NANDF_WP_B)	Output	3.3V CMOS	Suspend Status
20	PWRBTN#	ON_OFF	Input	3.3V CMOS/ 10K Pull-up	PWRBTN# is not supported. This pin is connected to i.MX6 CPU's ON_OFF pin through resistor and default populated.
21	SLP_BTN#/GPIO	GPIO3_31_SLP_BTN(EIM_D31)	Input	3.3V CMOS	Sleep button
22	LID_BTN#/GPIO	NC	NC	NC	NC
23	GND3	GND	Power	0V	Ground
24	GND4	GND	Power	0V	Ground
25	GND5	GND	Power	0V	Ground
26	PWRGIN/GPIO 5V CMOS INPUT	SOMPWR_EN	Input	5V CMOS/ 10K Pull-up	Active high Enable signal for SOM Power.
27	BATLOW#/GPIO	GPIO3_23_BATLOW(EIM_D23)	Input	3.3V CMOS	Battery low indication.
28	RSTBN#	RSTBN	Input	3.3V CMOS/ 10K Pull-up	Active low Reset button input to CPU.
29	SATA0_TX+	SATA_TXP	Output	Differential/ 0.1uF AC Coupling (C314)	SATA0 Transmit Output differential positive.
30	SATA1_TX+	NC	NC	NC	NC
31	SATA0_TX-	SATA_TXM	Output	Differential/ 0.1uF AC Coupling (C315)	SATA0 Transmit Output differential negative.
32	SATA1_TX-	NC	NC	NC	NC
33	SATA_ACT#	GPIO4_10_SATA_AC T(KEY_COL2)	Output	3.3V CMOS	SATA command Activity line.
34	GND6	GND	Power	0V	Ground

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35	SATA0_RX+	SATA_RXP	Input	Differential/ 0.1uF Coupling (C316) & 100E parallel termination between Pair	AC	SATA0	Receive differential positive.	Input
36	SATA1_RX+	NC	NC	NC	NC	NC	NC	NC
37	SATA0_RX-	SATA_RXM	Input	Differential/ 0.1uF Coupling (C317) & 100E parallel termination between Pair	AC	SATA0	Receive differential negative.	Input
38	SATA1_RX-	NC	NC	NC	NC	NC	NC	NC
39	GND7	GND	Power	0V	Ground			
40	GND8	GND	Power	0V	Ground			
41	BIOS_DISABLE#/ BOOT_ALT#	NC	NC	NC	NC	NC	NC	NC
42	SDIO_CLK#	SD1_CLK	Output	3.3V CMOS	SD/MMC card clock			
43	SDIO_CD#	GPIO7_0_SD1_CD(SD 3_DAT5)	Input	3.3V CMOS	SD/MMC card Detect pin			
44	SDIO_LED	GPIO6_7_SD1_LED(N ANDF_CLE)	Output	3.3V CMOS	SD/MMC card indication LED			
45	SDIO_CMD	SD1_CMD	Input/ Output	3.3V CMOS	SD/MMC card Command line			
46	SDIO_WP	GPIO6_11_SD1_WP( NANDF_CS0)	Input	3.3V CMOS	SD/MMC card Write Protect pin			
47	SDIO_PWR#/ GPIO	GPIO6_14_SD1_PWR (NANDF_CS1)	Output	3.3V CMOS	SD/MMC card Power Enable pin			
48	SDIO_DAT1	SD1_DAT1	Input/ Output	3.3V CMOS	SD/MMC card Data Line (Bit1)			
49	SDIO_DAT0	SD1_DAT0	Input/ Output	3.3V CMOS	SD/MMC card Data Line (Bit0)			

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50	SDIO_DAT3	SD1_DAT3	Input/ Output	3.3V CMOS	SD/MMC card Data Line (Bit3)
51	SDIO_DAT2	SD1_DAT2	Input/ Output	3.3V CMOS	SD/MMC card Data Line (Bit2)
52	SDIO_DAT5	SD1_DAT5(NANDF_D 1)	Input/ Output	3.3V CMOS	SD/MMC card Data Line (Bit5)
53	SDIO_DAT4	SD1_DAT4(NANDF_D 0)	Input/ Output	3.3V CMOS	SD/MMC card Data Line (Bit4)
54	SDIO_DAT7	SD1_DAT7(NANDF_D 3)	Input/ Output	3.3V CMOS	SD/MMC card Data Line (Bit7)
55	SDIO_DAT6	SD1_DAT6(NANDF_D 2)	Input/ Output	3.3V CMOS	SD/MMC card Data Line (Bit6)
56	RSVD	GPIO3_22_RGMII_RS T(EIM_D22)	Input/ Output	3.3V CMOS	General purpose I/O
57	GND9	GND	Power	0V	Ground
58	GND10	GND	Power	0V	Ground
59	HDA_SYNC	AUD4_TXFS(SD2_DA T1)	Output	3.3V CMOS	Audio Transmit frame synchronization line
60	SMB_CLK	I2C2_SCL(KEY_COL3)	Output	3.3V CMOS/ 4.7K Pull-up	I2C2 clock signal
61	HDA_RST#/ GPIO	GPIO1_11_HDA_RST (SD2_CMD)	Output	3.3V CMOS	Audio reset
62	SMB_DAT	I2C2_SDA(KEY_ROW 3)	Input/ Output	3.3V CMOS/ 4.7K Pull-up	I2C2 Data signal
63	HDA_BITCLK	AUD4_TXC(SD2_DAT 3)	Output	3.3V CMOS	Audio Transmit Clock line
64	SMB_ALERT#	GPIO1_10_SMB_ALE RT(SD2_CLK)	Input	3.3V CMOS	System Management Bus Alert input.
65	HDA_SDI	AUD4_TXD(SD2_DAT 2)	Input	3.3V CMOS	Audio Transmit data line <b>Note: Make sure to enable AUDMUX_PDCR4 register's 12<sup>th</sup> bit (TXRXEN) in i.MX6 to make this pin as receive</b>
66	I2C_CLK	I2C1_SCL(EIM_D21)	Output	3.3V CMOS/ 4.7K Pull-up	I2C1 Clock signal

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67	HDA_SDO	AUD4_RXD(SD2_DAT0)	Output	3.3V CMOS	Audio Receive data line <b>Note:</b> Make sure to enable AUDMUX_PDCR4 register's 12 <sup>th</sup> bit (TXRXEN) in i.MX6 to make this pin as transmit
68	I2C_DAT	I2C1_SDA(EIM_D28)	Input/Output	3.3V CMOS/4.7K Pull-up	I2C1 Data signal
69	THRM#/ GPIO	NC	NC	NC	NC
70	WDTRIG#	GPIO6_8_WDTRIG(N ANDF_ALE)	Input	3.3V CMOS	Watchdog trigger signal
71	THRMTRIP#/ GPIO	NC	NC	NC	NC
72	WDOUT	WDOG_B(GPIO_9)	Output	3.3V CMOS	Watchdog event indicator Output. <i>Note:</i> WDOG_B(GPIO_9) signal is connected to this pin through inverter. <i>Note:</i> WDOG_B(GPIO_9) signal is optionally connected to Expansion connector1 8 <sup>th</sup> pin (as E8AI_FSR) through resistor and default not populated.
73	GND11	GND	Power	0V	Ground
74	GND12	GND	Power	0V	Ground
75	USB_P7-	NC	NC	NC	NC
76	USB_P6-	NC	NC	NC	NC
77	USB_P7+	NC	NC	NC	NC
78	USB_P6+	NC	NC	NC	NC
79	USB_6_7_OC#	NC	NC	NC	NC
80	USB_4_5_OC#	USB_4_5_OC	Input	3.3V CMOS	Over current sense for USB port 4 & 5
81	USB_P5-	NC	NC	NC	NC
82	USB_P4-	USB_HUBP4_DM	Input/Output	Differential	USB Host Port4 Data negative
83	USB_P5+	NC	NC	NC	NC

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84	USB_P4+	USB_HUBP4_DP	Input/ Output	Differential	USB Host Port4 Data Positive
85	USB_2_3_OC#	USB_2_3_OC	Input	3.3V CMOS	Over current sense for USB port 2 & 3
86	USB_0_1_OC#	USB_0_1_OC	Input	3.3V CMOS	Over current sense for USB port 0 & 1
87	USB_P3-	USB_HUBP3_DM	Input/ Output	Differential	USB Host Port3 Data negative
88	USB_P2-	USB_HUBP2_DM	Input/ Output	Differential	USB Host Port2 Data negative
89	USB_P3+	USB_HUBP3_DP	Input/ Output	Differential	USB Host Port3 Data Positive
90	USB_P2+	USB_HUBP2_DP	Input/ Output	Differential	USB Host Port2 Data Positive
91	USB_CC	GPIO2_25_USB_CC(E IM_OE)	Input	3.3V CMOS	USB client connect
92	USB_ID	USBOTG_ID(ENET_R X_ER)	Input	3.3V CMOS	USB OTG ID to identify Host & device
93	USB_P1-/OTG-	USB_OTG_DN	Input/ Output	Differential	USB OTG Data negative
94	USB_P0-	USB_HUBP1_DM	Input/ Output	Differential	USB Host Port1 Data negative
95	USB_P1+/OTG+	USB_OTG_DP	Input/ Output	Differential	USB OTG Data Positive
96	USB_P0+	USB_HUBP1_DP	Input/ Output	Differential	USB Host Port1 Data Positive
97	GND13	GND	Power	0V	Ground
98	GND14	GND	Power	0V	Ground
99	LVDS_A0+	LVDS0_TX0_P	Output	LVDS	LVDS primary channel differential pair0 positive
100	LVDS_B0+	LVDS1_TX0_P	Output	LVDS	LVDS secondary channel differential pair0 positive
101	LVDS_A0-	LVDS0_TX0_N	Output	LVDS	LVDS primary channel differential pair0 negative
102	LVDS_B0-	LVDS1_TX0_N	Output	LVDS	LVDS secondary channel differential pair0 negative

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103	LVDS_A1+	LVDS0_TX1_P	Output	LVDS	LVDS primary channel differential pair1 positive
104	LVDS_B1+	LVDS1_TX1_P	Output	LVDS	LVDS secondary channel differential pair1 positive
105	LVDS_A1-	LVDS0_TX1_N	Output	LVDS	LVDS primary channel differential pair1 negative
106	LVDS_B1-	LVDS1_TX1_N	Output	LVDS	LVDS secondary channel differential pair1 negative
107	LVDS_A2+	LVDS0_TX2_P	Output	LVDS	LVDS primary channel differential pair2 positive
108	LVDS_B2+	LVDS1_TX2_P	Output	LVDS	LVDS secondary channel differential pair2 positive
109	LVDS_A2-	LVDS0_TX2_N	Output	LVDS	LVDS primary channel differential pair2 negative
110	LVDS_B2-	LVDS1_TX2_N	Output	LVDS	LVDS secondary channel differential pair2 negative
111	LVDS_PPEN/ GPIO	GPIO2_4_LVDS_PPE N(NANDF_D4)	Output	3.3V CMOS	LVDS LCD panel power enable control.
112	LVDS_BLEN/ GPIO	GPIO2_5_LVDS_BLE N(NANDF_D5)	Output	3.3V CMOS	LVDS LCD panel Backlight enable control.
113	LVDS_A3+	LVDS0_TX3_P	Output	LVDS	LVDS primary channel differential pair3 positive
114	LVDS_B3+	LVDS1_TX3_P	Output	LVDS	LVDS secondary channel differential pair3 positive
115	LVDS_A3-	LVDS0_TX3_N	Output	LVDS	LVDS primary channel differential pair3 negative
116	LVDS_B3-	LVDS1_TX3_N	Output	LVDS	LVDS secondary channel differential pair3 negative
117	GND15	GND	Power	0V	Ground
118	GND16	GND	Power	0V	Ground
119	LVDS_A_CLK+	LVDS0_CLK_P	Output	LVDS	LVDS primary channel differential clock positive.
120	LVDS_B_CLK+	LVDS1_CLK_P	Output	LVDS	LVDS secondary channel differential clock Positive.
121	LVDS_A_CLK-	LVDS0_CLK_N	Output	LVDS	LVDS primary channel differential clock Negative.

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122	LVDS_B_CLK-	LVDS1_CLK_N	Output	LVDS	LVDS secondary channel differential clock negative.
123	LVDS_BLT_CTRL/ GP_PWM_OUT0/ PWM0	PWM2_PWM0(GPIO _1)	Output	3.3V CMOS	LVDS LCD Panel backlight brightness control. <i>Note: Optionally same signal is connected to Qseven edge connector 194<sup>th</sup> &amp; 196<sup>th</sup> pins (as PWM2) and Expansion connector1 12<sup>th</sup> pin (as ESDI_SCKR) through resistors.</i>
124	RSVD_1	GPIO5_2_HDMI_CEC (EIM_A25)	Input/ Output	3.3V CMOS	HDMI CEC bus. <i>Note: Optionally GPIO5_2_HDMI_CEC(EIM_A 25) is connected to Qseven edge connector 18<sup>th</sup> pin and Expansion connector2 62<sup>nd</sup> pin through resistors and both default populated.</i>
125	LVDS_DID_DAT/ GP_I2C_DAT	I2C1_SDA(EIM_D28)	Input/ Output	3.3V CMOS/ 4.7K Pull-up	I2C1 Data signal
126	LVDS_BLC_DAT	I2C1_SDA(EIM_D28)	Input/ Output	3.3V CMOS/ 4.7K Pull-up	I2C1 Data signal
127	LVDS_DID_CLK/ GP_I2C_CLK	I2C1_SCL(EIM_D21)	Output	3.3V CMOS/ 4.7K Pull-up	I2C1 Clock signal
128	LVDS_BLC_CLK	I2C1_SCL(EIM_D21)	Output	3.3V CMOS/ 4.7K Pull-up	I2C1 Clock signal
129	CANO_TX	CAN1_TX(GPIO_7)	Output	3.3V CMOS	CAN channel one TX line
130	CANO_RX	CAN1_RX(KEY_ROW 2)	Input	3.3V CMOS	CAN channel one RX line
131	SDVO_BCLK+/ TMDS_CLK+	HDMI_CLKP	Output	TMDS	HDMI differential clock positive
132	SDVO_INT+	NC	NC	NC	NC
133	SDVO_BCLK-// TMDS_CLK-	HDMI_CLKM	Output	TMDS	HDMI differential clock negative
134	SDVO_INT-	NC	NC	NC	NC

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135	GND17	GND	Power	0V	Ground
136	GND18	GND	Power	0V	Ground
137	SDVO_GREEN+/ TMDS_LANE1+	HDMI_D1P	Output	TMDS	HDMI differential data1 positive
138	SDVO_FLDSTALL+	NC	NC	NC	NC
139	SDVO_GREEN-// TMDS_LANE1-	HDMI_D1M	Output	TMDS	HDMI differential data1 negative
140	SDVO_FLDSTALL-	NC	NC	NC	NC
141	GND19	GND	Power	0V	Ground
142	GND20	GND	Power	0V	Ground
143	SDVO_BLUE+/ TMDS_LANE0+	HDMI_D0P	Output	TMDS	HDMI differential data0 positive
144	SDVO_TVCLKIN+	NC	NC	NC	NC
145	SDVO_BLUE-// TMDS_LANE0-	HDMI_D0M	Output	TMDS	HDMI differential data0 negative
146	SDVO_TVCLKIN-	NC	NC	NC	NC
147	GND21	GND	Power	0V	Ground
148	GND22	GND	Power	0V	Ground
149	SDVO_RED+/ TMDS_LANE2+	HDMI_D2P	Output	TMDS	HDMI differential data2 positive
150	SDVO_CTRL_DA/ HDMI_CTRL_DA	I2C2_SDA(KEY_ROW 3)	Input/ Output	3.3V CMOS/ 4.7K Pull-up	I2C2 Data signal
151	SDVO_RED-// TMDS_LANE2-	HDMI_D2M	Output	TMDS	HDMI differential data2 negative
152	SDVO_CTRL_CK/ HDMI_CTRL_CK	I2C2_SCL(KEY_COL3)	Output	3.3V CMOS/ 4.7K Pull-up	I2C2 Clock signal
153	HDMI_HPD#	HDMI_HPD	Input	3.3V CMOS	HDMI Hot Plug Detect
154	DP_HPD#	NC	NC	NC	NC
155	PCIE_CLK_REF+	PCIe_REFCLK_DP	Output	Differential	PCIe differential reference clock positive
156	PCIE_WAKE#	GPIO2_6_PCIE_WAK E(NANDF_D6)	Input	3.3V CMOS	PCIe interface wake up signal
157	PCIE_CLK_REF-	PCIe_REFCLK_DN	Output	Differential	PCIe differential reference clock negative
158	PCIE_RST#	GPIO2_7_PCIE_RST( NANDF_D7)	Output	3.3V CMOS	PCIe Reset.

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159	GND23	GND	Power	0V	Ground
160	GND24	GND	Power	0V	Ground
161	PCIE3_TX+	NC	NC	NC	NC
162	PCIE3_RX+	NC	NC	NC	NC
163	PCIE3_TX-	NC	NC	NC	NC
164	PCIE3_RX-	NC	NC	NC	NC
165	GND25	GND	Power	0V	Ground
166	GND26	GND	Power	0V	Ground
167	PCIE2_TX+	NC	NC	NC	NC
168	PCIE2_RX+	NC	NC	NC	NC
169	PCIE2_TX-	NC	NC	NC	NC
170	PCIE2_RX-	NC	NC	NC	NC
171	EXCD0_PERST#/UART0_TX	KEY_COL1	Output	3.3V CMOS	<p>Default NC</p> <p><i>Note: Optionally UART5 TX signal (CPU Pin name: KEY_COL1) is connected to this pin through resistor R350 and default not populated.</i></p> <p><i>Note: KEY_COL1 is always connected to Expansion connector2 11<sup>th</sup> pin.</i></p>
172	EXCD1_PERST#/UART0_RTS#	CAN2_RX(KEY_ROW4)	Output	3.3V CMOS	<p>Default NC</p> <p><i>Note: Optionally UART5 RTS signal (CPU Pin name: CAN2_RX) is connected to this pin through resistor R348 and default not populated.</i></p> <p><i>Note: CAN2_RX is always connected to Expansion connector1 78<sup>th</sup> pin.</i></p>
173	PCIE1_TX+	NC	NC	NC	NC
174	PCIE1_RX+	NC	NC	NC	NC
175	PCIE1_TX-	NC	NC	NC	NC
176	PCIE1_RX-	NC	NC	NC	NC

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177	EXCDO_CPPE#/UART0_RX	KEY_ROW1	Input	3.3V CMOS	<p>Default NC</p> <p><i>Note: Optionally UART5_RX signal (CPU Pin name: KEY_ROW1) is connected to this pin through resistor R351 and default not populated.</i></p> <p><i>Note: KEY_ROW1 is always connected to Expansion connector2 7<sup>th</sup> pin.</i></p>
178	EXCD1_CPPE#/UART0_CTS#	CAN2_TX(KEY_COL4)	Input	3.3V CMOS	<p>Default NC</p> <p><i>Note: Optionally UART5_CTS signal (CPU Pin name: CAN2_TX) is connected to this pin through resistor R349 and default not populated.</i></p> <p><i>Note: CAN2_TX is always connected to Expansion connector1 79<sup>th</sup> pin.</i></p>
179	PCIE0_TX+	PCIe_TXP	Output	Differential / 0.1uF AC Coupling (C320)	PCIe differential transmit line positive
180	PCIE0_RX+	PCIe_RXP	Input	Differential	PCIe differential receive line positive
181	PCIE0_TX-	PCIe_TXM	Output	Differential / 0.1uF AC Coupling (C321)	PCIe differential transmit line negative
182	PCIE0_RX-	PCIe_RXM	Input	Differential	PCIe differential receive line negative
183	GND27	GND	Power	0V	Ground
184	GND28	GND	Power	0V	Ground
185	LPC_AD0	NC	NC	NC	NC
186	LPC_AD1	NC	NC	NC	NC

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187	LPC_AD2	NC	NC	NC	NC
188	LPC_AD3	NC	NC	NC	NC
189	LPC_CLK	NC	NC	NC	NC
190	LPC_FRAME#	NC	NC	NC	NC
191	SERIRQ	NC	NC	NC	NC
192	LPC_LDRQ#	NC	NC	NC	NC
193	VCC_RTC	VRTC_3V0	Power	3V	RTC battery voltage Input. This pin is connected to CPU RTC Power Input (VDD_SNVS_IN) through schottky diode and default populated.
194	SPKR/ PWM1	PWM2_PWMO(GPIO_1)	Output	3.3V CMOS	<p>Default NC</p> <p><i>Note:</i></p> <p><i>PWM2_PWMO(GPIO_1)</i> is optionally connected to this pin through resistor and default not populated</p> <p><i>Note:</i> Same signal is also connected to Qseven edge connector 123<sup>rd</sup> &amp; 196<sup>th</sup> pins (as PWM2) and Expansion connector1 12<sup>th</sup> pin (as ESAI_SCKR) through resistors.</p>
195	FAN_TACHO_IN/ GP_TIMER_IN	GPIO6_16_FAN_CRT L(NANDF_CS3)	Input	3.3V CMOS	Fan tachometer input
196	FAN_PWMOUT/ GP_PWM_OUT1	PWM2_PWMO(GPIO_1)	Output	3.3V CMOS	<p>Default NC</p> <p><i>Note:</i></p> <p><i>PWM2_PWMO(GPIO_1)</i> is optionally connected to this pin through resistor and default not populated</p> <p><i>Note:</i> Same signal is also connected to Qseven edge connector 123<sup>rd</sup> &amp; 194<sup>th</sup> pins</p>

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					<i>(as PWM2) and Expansion connector1 12<sup>th</sup> pin (as ESDI_SCKR) through resistors.</i>
197	GND29	GND	Power	0V	Ground
198	GND30	GND	Power	0V	Ground
199	SPI_MOSI	eCSPI2_MOSI(CSIO_DA AT9 )	Input/ Output	3.3V CMOS	SPI Master Out Slave In
200	SPI_CS0#	eCSPI2_SS0(CSIO_DA T11)	Output	3.3V CMOS	SPI chip select 0
201	SPI_MISO	eCSPI2_MISO(CSIO_DA AT10)	Input/ Output	3.3V CMOS	SPI Master In Slave Out
202	SPI_CS1#	eCSPI2_SS1(EIM_LBA )	Output	3.3V CMOS	SPI chip select 1
203	SPI_SCK	eCSPI2_SCLK(CSIO_DA AT8)	Output	3.3V CMOS	SPI clock output
204	MFG_NC4/ JTAG_TRST#/ GPIO For JTAG/ UART	JTAG_TRSTB	Input	3.3V CMOS	JTAG Reset Input
205	VCC_5V_SB	NC	NC	NC	NC
206	VCC_5V_SB	NC	NC	NC	NC
207	MFG_NC0/ JTAG_TCK	JTAG_TCK	Input	3.3V CMOS	JTAG Test Clock
208	MFG_NC2/ JTAG_TDI/ UART_RX	JTDI_RX	Input	3.3V CMOS	Debug UART RX data line UART2_RXD(EIM_D27) is connected to this pin through resistor and default populated <i>Note: Optionally JTAG_TDI is connected to this pin through resistor and default not populated</i>
209	MFG_NC1/ JTAG_TDO/ UART_TX	JTDO_UTX	Output	3.3V CMOS	Debug UART TX data line. UART2_RXD(EIM_D26) is connected to this pin

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					through resistor and default populated <i>Note: Optionally JTAG_TDO is connected to this pin through resistor and default not populated</i>
210	MFG_NC3/ JTAG_TMS	JTAG_TMS	Input	3.3V CMOS	JTAG Test Mode Select
211	VCC	VCC_5V	Power	5V	Input Supply Voltage
212	VCC	VCC_5V	Power	5V	Input Supply Voltage
213	VCC	VCC_5V	Power	5V	Input Supply Voltage
214	VCC	VCC_5V	Power	5V	Input Supply Voltage
215	VCC	VCC_5V	Power	5V	Input Supply Voltage
216	VCC	VCC_5V	Power	5V	Input Supply Voltage
217	VCC	VCC_5V	Power	5V	Input Supply Voltage
218	VCC	VCC_5V	Power	5V	Input Supply Voltage
219	VCC	VCC_5V	Power	5V	Input Supply Voltage
220	VCC	VCC_5V	Power	5V	Input Supply Voltage
221	VCC	VCC_5V	Power	5V	Input Supply Voltage
222	VCC	VCC_5V	Power	5V	Input Supply Voltage
223	VCC	VCC_5V	Power	5V	Input Supply Voltage
224	VCC	VCC_5V	Power	5V	Input Supply Voltage
225	VCC	VCC_5V	Power	5V	Input Supply Voltage
226	VCC	VCC_5V	Power	5V	Input Supply Voltage
227	VCC	VCC_5V	Power	5V	Input Supply Voltage
228	VCC	VCC_5V	Power	5V	Input Supply Voltage
229	VCC	VCC_5V	Power	5V	Input Supply Voltage
230	VCC	VCC_5V	Power	5V	Input Supply Voltage

## 2.7 Expansion Connectors

Qseven edge connector pull-out only a selected set of interfaces as per Qseven standard. All the effort is made in i.MX6 Qseven SOM design, to provide maximum interfaces of i.MX6 CPU to the carrier board by adding two Expansion connectors. Following section provides details about supported interfaces in the Expansion connectors.

### 2.7.1 Expansion Connector1

Expansion connector1 supports following interfaces:

- **Parallel LCD Interface:**

Expansion connector1 provides 24bpp RGB parallel LCD interface along with control signals. i.MX6 CPU parallel LCD interface supports up to 220Mpixels/sec.

- **MIPI-DSI**

Expansion connector1 provides MIPI-DSI two lane which supports 1 Gbps.

- **Camera interface**

Expansion connector1 provides one 8bit parallel camera interface (CSI0) along with required control signals.

- **UART interfaces**

Expansion connector1 provides two UART interfaces of up to 4.0 Mbps speed (UART1 & UART3) with TXD, RXD, CTS and RTS signals.

- **ESAI**

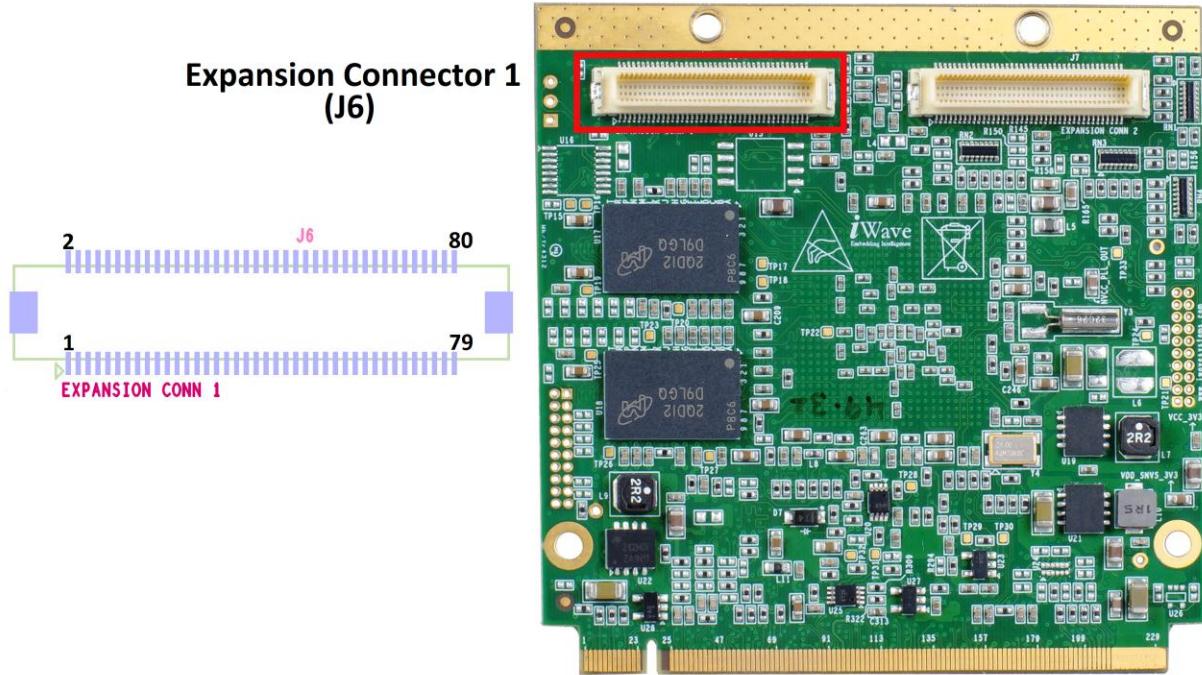
Expansion connector1 provides one Enhanced Serial Audio Interface (ESAI). This interface will work up to 1.4 Mbps.

- **SPDIF**

Expansion connector1 also provides one Sony Phillips Digital Interface (SPDIF) for audio.

- **CAN interface**

Expansion connector1 provides one controller area network (CAN) interface. This is supported using i.MX6's FLEXCAN2 interface up to 1 Mbps speed.



**Figure 5: Expansion Connector1**

Number of Pins - 80

Connector Part Number- DF17(2.0)-80DP-0.5V(57)

Mating Connector - DF17(3.0)-80DS-0.5V(57) from Hirose

**Table 7: Expansion Connector1 Pin Assignment**

Pin No	Signal Name	Signal Type	Voltage Level/Termination	Description
1	GND	Power	0V	Ground
2	DISP0_DAT23	Output	3.3V CMOS	LCD Data 23 (Red Data 7)
3	ESAI_TX5_RX0(GPIO_8)	Input/Output	3.3V CMOS	ESAI Serial Transmit5/Receive0 Data
4	DISP0_DAT22	Output	3.3V CMOS	LCD Data 22 (Red Data 6)
5	ESAI_TX4_RX1(ENET_TXD0)	Input/Output	3.3V CMOS	ESAI Serial Transmit4/Receive1 Data
6	DISP0_DAT18	Output	3.3V CMOS	LCD Data 18 (Red Data 2)
7	ESAI_TX2_RX3(ENET_TXD1)	Input/Output	3.3V CMOS	ESAI Serial Transmit2/Receive3 Data
8	ESAI_FSR(GPIO_9)	Input/Output	3.3V CMOS	<p>Default NC.</p> <p><i>Note: ESAI_FSR(GPIO_9) is optionally connected to this pin through resistor and default not populated.</i></p> <p><i>Note: ESAI_FSR(GPIO_9) is also connected to Qseven edge connector 72<sup>nd</sup> pin (as WDOG) through resistor option and default populated.</i></p>
9	ESAI_TX3_RX2(ENET_TX_EN)	Input/Output	3.3V CMOS	ESAI Serial Transmit3/Receive2 Data
10	ESAI_HCKR(GPIO_3)	Input/Output	3.3V CMOS	<p>Default NC.</p> <p><i>Note: ESAI_HCKR(GPIO_3) is optionally connected to this pin through resistor and default not populated.</i></p> <p><i>Note: ESAI_HCKR(GPIO_3) is also connected to Expansion connector2 2<sup>nd</sup> pin (as MLB_CLK) using resistor and default populated.</i></p>
11	ESAI_TX1(GPIO_18)	Output	3.3V CMOS	ESAI Serial Transmit1 Data

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12	PWM2_PWMO(GPIO_1)	Input	3.3V CMOS	Default NC. <i>Note: PWM2_PWMO(GPIO_1) is optionally connected to this pin (as ESAI_RX_CLK) through resistor and default not populated.</i> <i>Note: PWM2_PWMO(GPIO_1) is also connected to Qseven edge connector 123<sup>rd</sup>, 194<sup>th</sup> &amp; 196<sup>th</sup> pins and Expansion connector1 19<sup>th</sup> Pin through resistors.</i>
13	ESAI_TX0(GPIO_17)	Output	3.3V CMOS	ESAI Serial Transmit0 Data
14	ESAI_SCKT(ENET_CRS_DV)	Input/ Output	3.3V CMOS	ESAI Transmitter Serial Clock
15	SPDIF_IN1(GPIO_16)	Input	3.3V CMOS	SPDIF input line
16	ESAI_FST(ENET_RXD1)	Input/ Output	3.3V CMOS	ESAI Frame Sync for Transmitter
17	SPDIF_OUT1(GPIO_19)	Output	3.3V CMOS	SPDIF output line
18	ESAI_HCKT(ENET_RXD0)	Input/ Output	3.3V CMOS	ESAI High Frequency Clock for Transmitter
19	PWM2_PWMO(GPIO_1)	Output	3.3V CMOS	PWM2 output <i>Note: PWM2_PWMO(GPIO_1) is optionally connected to this pin through resistor and default not populated.</i> <i>Note: PWM2_PWMO(GPIO_1) is also connected to Qseven edge connector 123<sup>rd</sup>, 194<sup>th</sup> &amp; 196<sup>th</sup> pins and Expansion connector1 12<sup>th</sup> Pin through resistors.</i>
20	DISP0_DAT17	Output	3.3V CMOS	Parallel LCD Data17 (Red Data1)
21	DISP0_DAT14	Output	3.3V CMOS	Parallel LCD Data14 (Green Data6)
22	DISP0_DAT12	Output	3.3V CMOS	Parallel LCD Data12 (Green Data4)
23	DISP0_DAT9	Output	3.3V CMOS	Parallel LCD Data9 (Green Data1)
24	DISP0_DAT7	Output	3.3V CMOS	Parallel LCD Data7 (Blue Data7)
25	DISP0_DAT5	Output	3.3V CMOS	Parallel LCD Data5 (Blue Data5)
26	DISP0_DAT0	Output	3.3V CMOS	Parallel LCD Data0 (Blue Data0)

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27	GND	Power	0V	Ground
28	DISP0_DAT3	Output	3.3V CMOS	Parallel LCD Data3 (Blue Data 3)
29	DISP0_DAT10	Output	3.3V CMOS	Parallel LCD Data10 (Green Data2)
30	DISP0_DAT4	Output	3.3V CMOS	Parallel LCD Data4 (Blue Data 4)
31	DISP0_DAT13	Output	3.3V CMOS	Parallel LCD Data13 (Green Data5)
32	GND	Power	0V	Ground
33	DISP0_DAT21	Output	3.3V CMOS	Parallel LCD Data21 (Red Data5)
34	DISP0_DAT16	Output	3.3V CMOS	Parallel LCD Data16 (Red Data0)
35	DISP0_DAT20	Output	3.3V CMOS	Parallel LCD Data20 (Red Data4)
36	DISP0_DAT19	Output	3.3V CMOS	Parallel LCD Data19 (Red Data3)
37	GND	Power	0V	Ground
38	DISP0_DAT11	Output	3.3V CMOS	Parallel LCD Data11 (Green Data3)
39	GND	Power	0V	Ground
40	DISP0_DAT6	Output	3.3V CMOS	Parallel LCD Data6 (Blue Data6)
41	DISP0_DAT2	Output	3.3V CMOS	Parallel LCD Data2 (Blue Data2)
42	GND	Power	0V	Ground
43	DISP0_DAT1	Output	3.3V CMOS	Parallel LCD Data1 (Blue Data1)
44	GND	Power	0V	Ground
45	DISP0_DAT8	Output	3.3V CMOS	Parallel LCD Data8 (Green Data0)
46	DSI_D1P	Output	Differential	MIPI DSI differential data1 positive
47	DISP0_DAT15	Output	3.3V CMOS	Parallel LCD Data15 (Green Data7)
48	DSI_D1M	Output	Differential	MIPI DSI differential data1 negative
49	GND	Power	0V	Ground
50	UART1_TXD(SD3_DAT7)	Output	3.3V CMOS	UART1 Transmit data line
51	UART1_RTS(EIM_D20)	Input	3.3V CMOS	UART1 RTS input
52	UART1_RXD(SD3_DAT6)	Input	3.3V CMOS	UART1 Receive data line
53	UART1_CTS(EIM_D19)	Output	3.3V CMOS	UART1 CTS output
54	GND	Power	0V	Ground
55	DSI_CLKOP	Output	Differential	MIPI DSI differential clock positive
56	DSI_DOP	Output	Differential	MIPI DSI differential data Positive
57	DSI_CLKOM	Output	Differential	MIPI DSI differential clock negative
58	DSI_DOM	Output	Differential	MIPI DSI differential data negative
59	GND	Power	0V	Ground
60	UART3_RXD(EIM_D25)	Input	3.3V CMOS	UART3 Receive data line
61	UART3_RTS(SD3_RST)	Input	3.3V CMOS	UART3 RTS input
62	UART3_CTS(EIM_D30)	Output	3.3V CMOS	UART3 CTS output

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63	UART3_TXD(EIM_D24)	Output	3.3V CMOS	UART3 Transmit data line
64	CLKO(GPIO_0)	Output	3.3V CMOS	General purpose configurable clock from CPU
65	CSI0_PIXCLK	Input	3.3V CMOS	Camera0 PIXCLK
66	CSI0_HSYNC	Input	3.3V CMOS	Camera0 HSYNC
67	CSI0_DATA_EN	Input	3.3V CMOS	Camera0 data enable
68	CSI0_VSYNC	Input	3.3V CMOS	Camera0 VSYNC
69	CSI0_DAT12	Input	3.3V CMOS	Camera0 data bit0
70	CSI0_DAT13	Input	3.3V CMOS	Camera0 data bit1
71	CSI0_DAT14	Input	3.3V CMOS	Camera0 data bit2
72	CSI0_DAT15	Input	3.3V CMOS	Camera0 data bit3
73	CSI0_DAT16	Input	3.3V CMOS	Camera0 data bit4
74	CSI0_DAT18	Input	3.3V CMOS	Camera0 data bit6
75	CSI0_DAT19	Input	3.3V CMOS	Camera0 data bit7
76	CSI0_DAT17	Input	3.3V CMOS	Camera0 data bit5
77	DIO_DISP_CLK	Output	3.3V CMOS	Parallel LCD Clock
78	CAN2_RX(KEY_ROW4)	Input	3.3V CMOS	CAN channel2 Receive line <i>Note: Optionally same signal is connected to Qseven edge connector 172<sup>th</sup> pin (as UART5_RTS) through resistor and default not populated.</i>
79	CAN2_TX(KEY_COL4)	Output	3.3V CMOS	CAN channel2 Transmit line <i>Note: Optionally same signal is connected to Qseven edge connector 178<sup>th</sup> pin (as UART5_CTS) through resistor and default not populated.</i>
80	GND	Power	0V	Ground

## 2.7.2 Expansion Connector2

Expansion connector2 supports following interfaces:

- **External Memory Bus**

Expansion connector2 provides Data/Address multiplexed memory bus. This bus can handle the interface to memory devices which are external to the SOM.

- **Camera interface**

Expansion connector2 provides one 8bit camera interface (CSI1) along with required control signals.

- **MIPI-CSI**

Expansion connector2 provides one MIPI CSI-2 serial camera port, supporting up to 1000 Mbps/lane in 1/2/3-lane mode and up to 800 Mbps/lane in 4-lane mode.

- **UART Interface**

Expansion connector2 provides one UART interfaces of up to 4.0 Mbps speed (UART4) with TXD & RXD signals.

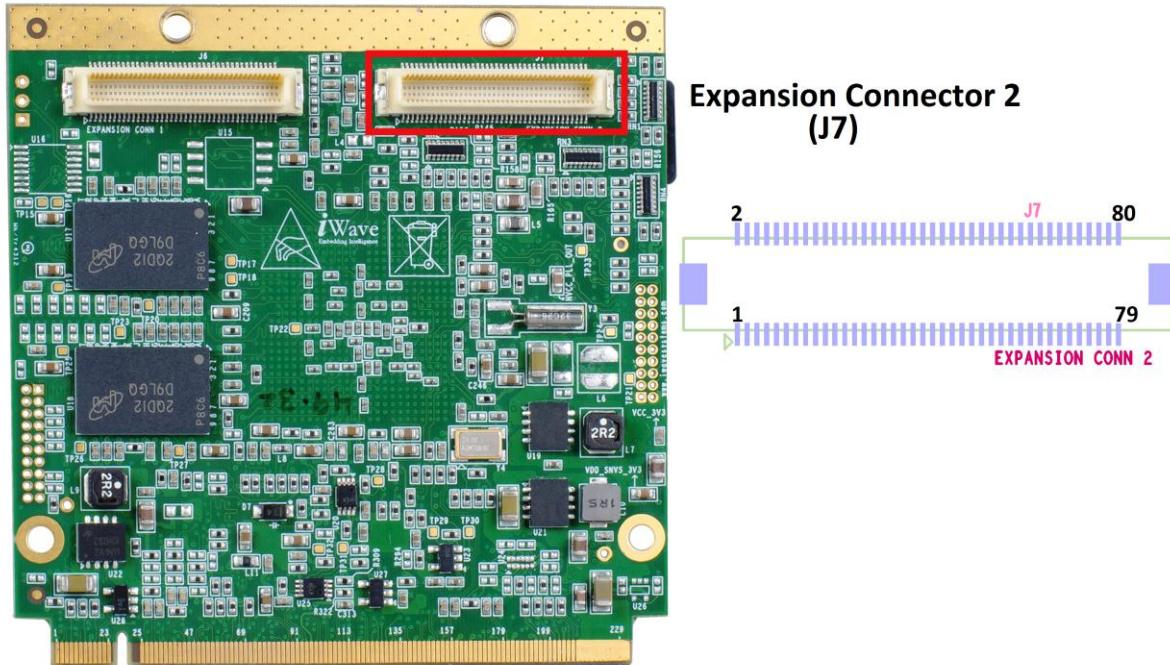
- **4x4 Keypad**

Expansion connector2 provides general purpose 4x4 keypad interface.

- **MLB**

Expansion connector2 provides MLB 6pin differential or 3Pin single ended interface. MLB provides interface to MOST Networks (150Mbps) with DTCP cipher accelerator. Either MLB 6pin or 3pin only can be used at a time. If 3Pin MLB is not used, same pin can be used as I2C3 interface.

*Note: MLB interface will be available only with automotive i.MX6 CPU part*



**Figure 6: Expansion Connector2**

Number of Pins - 80

Connector Part Number- DF17(2.0)-80DP-0.5V(57)

Mating Connector - DF17(3.0)-80DS-0.5V(57) from Hirose

**Table 8: Expansion Connector2 Pin Assignment**

Pin No	Signal Name	Signal Type	Voltage Level/Termination	Description
1	MLB_DN/MLBDAT(GPIO_2)	Input/Output	3.3V CMOS	MLB single ended data. <i>Note: Optionally MLB differential data negative also connected to this pin through resistor option and default not populated.</i>
2	MLBCLK/MLB_CP	Input	3.3V CMOS	MLB single ended clock. <i>Note: Optionally MLB differential clock positive also connected to this pin through resistor option and default not populated.</i> <i>Note: Optionally MLBCLK is connected to Expansion connector1 10<sup>th</sup> pin (as ESAI_HCKR) through resistor and default not populated.</i>
3	SD4_DAT2 / MLB_DP	Input/Output	3.3V CMOS	PWM4 or GPIO. <i>Note: Do Not Use this Pin in Carrier Board if i.MX6 Qseven SOM supports eMMC Flash as this signal is used for on-SOM eMMC Flash Interface.</i> <i>Note: Optionally MLB differential data positive connected to this pin through resistor option and default not populated.</i>
4	MLB_CN/ MLBSIG(GPIO_6)	Input	3.3V CMOS	MLB single ended signal line. <i>Note: Optionally MLB differential clock negative also connected to this pin through resistor option and default not populated.</i>
5	GND	Power	0V	Ground
6	GND	Power	0V	Ground
7	KEY_ROW1	Output	3.3V CMOS	Keypad Row1 <i>Note: Optionally same signal is</i>

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				<i>connected to Qseven edge connector 177<sup>th</sup> pin (as UART5_RX) through resistor and default not populated.</i>
8	KEY_ROW5(CSIO_DAT5)	Output	3.3V CMOS	Keypad Row2
9	KEY_ROW6(CSIO_DAT7)	Output	3.3V CMOS	Keypad Row3
10	KEY_ROW7(GPIO_5)	Output	3.3V CMOS	Keypad Row4
11	KEY_COL1	Input	3.3V CMOS	Keypad Column1 <i>Note: Optionally same signal is connected to Qseven edge connector 171<sup>th</sup> pin (as UART5_TX) through resistor and default not populated.</i>
12	KEY_COL5(CSIO_DAT4)	Input	3.3V CMOS	Keypad Column2
13	KEY_COL6(CSIO_DAT6)	Input	3.3V CMOS	Keypad Column3
14	KEY_COL7(GPIO_4)	Input	3.3V CMOS	Keypad Column4
15	GND	Power	0V	Ground
16	GND	Power	0V	Ground
17	EIM_DA1	Input/ Output	3.3V CMOS	EIM Data & address line 1
18	EIM_DA0	Input/ Output	3.3V CMOS	EIM Data & address line 0
19	EIM_DA3	Input/ Output	3.3V CMOS	EIM Data & address line 3
20	EIM_DA2	Input/ Output	3.3V CMOS	EIM Data & address line 2
21	EIM_DA5	Input/ Output	3.3V CMOS	EIM Data & address line 5
22	EIM_DA4	Input/ Output	3.3V CMOS	EIM Data & address line 4
23	EIM_DA7	Input/ Output	3.3V CMOS	EIM Data & address line 7
24	EIM_DA6	Input/ Output	3.3V CMOS	EIM Data & address line 6
25	EIM_DA9	Input/ Output	3.3V CMOS	EIM Data & address line 9

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26	EIM_DA8	Input/ Output	3.3V CMOS	EIM Data & address line 8
27	EIM_DA11	Input/ Output	3.3V CMOS	EIM Data & address line 11
28	EIM_DA10	Input/ Output	3.3V CMOS	EIM Data & address line 10
29	EIM_DA13	Input/ Output	3.3V CMOS	EIM Data & address line 13
30	EIM_DA12	Input/ Output	3.3V CMOS	EIM Data & address line 12
31	EIM_DA15	Input/ Output	3.3V CMOS	EIM Data & address line 15
32	EIM_DA14	Input/ Output	3.3V CMOS	EIM Data & address line 14
33	GND	Power	0V	Ground
34	GND	Power	0V	Ground
35	EIM_RW	Output	3.3V CMOS	EIM Read/Write Enable
36	EIM_CS0	Output	3.3V CMOS	EIM Chip Select0
37	EIM_BCLK	Output	3.3V CMOS	EIM Burst Clock
38	EIM_CRE(NANDF_CS2)	Output	3.3V CMOS	EIM Memory Register Set
39	EIM_EB1	Output	3.3V CMOS	EIM Enable Byte1
40	EIM_WAIT	Input	3.3V CMOS	EIM Ready/Busy/Wait
41	DIO_PIN4	Output	3.3V CMOS	Parallel LCD Contrast control <i>Note: If Parallel LCD is not used, this pin can be configured as AUD6_RXD.</i>
42	EIM_EB0	Output	3.3V CMOS	EIM Enable Byte0
43	DIO_PIN3	Output	3.3V CMOS	Parallel LCD Vsync <i>Note: If Parallel LCD is not used, this pin can be configured as AUD6_TXFS.</i>
44	DIO_PIN2	Output	3.3V CMOS	Parallel LCD Hsync <i>Note: If Parallel LCD is not used, this pin can be configured as AUD6_TXD.</i>

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45	DIO_PIN15	Output	3.3V CMOS	Parallel LCD Data Enable (DRDY) <i>Note: If parallel LCD is not used, this pin can be configured as AUD6_TXC.</i>
46	GND	Power	0V	Ground
47	GND	Power	0V	Ground
48	CSI1_D[13](EIM_A18)	Input	3.3V CMOS	Camera1 data bit1
49	CSI1_D[12](EIM_A17)	Input	3.3V CMOS	Camera1 data bit0
50	CSI1_D[15](EIM_A20)	Input	3.3V CMOS	Camera1 data bit3
51	CSI1_D[14](EIM_A19)	Input	3.3V CMOS	Camera1 data bit2
52	CSI1_D[17](EIM_A22)	Input	3.3V CMOS	Camera1 data bit5
53	CSI1_D[16](EIM_A21)	Input	3.3V CMOS	Camera1 data bit4
54	CSI1_D[18](EIM_A23)	Input	3.3V CMOS	Camera1 data bit6
55	CSI1_D[19](EIM_A24)	Input	3.3V CMOS	Camera1 data bit7
56	CSI1_HSYNC(EIM_EB3)	Input	3.3V CMOS	Camera1 HSYNC
57	CSI1_VSYNC(EIM_D29)	Input	3.3V CMOS	Camera1 VSYNC
58	CSI1_PIXCLK(EIM_A16)	Input	3.3V CMOS	Camera1 PIXCLK
59	GND	Power	0V	Ground
60	GND	Power	0V	Ground
61	CSI_CLKOP	Input	Differential	MIPI CSI differential clock positive
62	GPIO5_2_HDMI_CEC(EIM_A25)	Input/Output	3.3V CMOS	HDMI CEC <i>Note: Optionally HDMI_CEC is connected to Qseven edge connector 18<sup>th</sup> and 124<sup>th</sup> pins through resistors.</i>
63	CSI_CLK0M	Input	3.3V CMOS	MIPI CSI differential clock negative
64	UART4_TXD(KEY_COL0)	Output	3.3V CMOS	UART4 Transmit data line
65	CSI_D0P	Input	Differential	MIPI CSI differential data0 positive
66	MLB_SP	Output	LVDS	Default NC. <i>Note: Optionally connected to MLB differential signal Positive through resistor and default not populated.</i>
67	CSI_D0M	Input	Differential	MIPI CSI differential data0 negative
68	UART4_RXD(KEY_ROW0)	Input	3.3V CMOS	UART4 Receive data line
69	CSI_D1P	Input	Differential	MIPI CSI differential data1 positive

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70	MLB_SN	Output	LVDS	Default NC. <i>Note: Optionally connected to MIPI CSI differential signal negative through resistor and default not populated.</i>
71	CSI_D1M	Input	Differential	MIPI CSI differential data1 negative
72	SD4_DAT1	Input/ Output	3.3V CMOS	General Purpose I/O. <i>Note: Do Not Use this Pin in Carrier Board if i.MX6 Qseven SOM supports eMMC Flash as this signal is used for On-SOM eMMC Flash Interface.</i>
73	CSI_D2P	Input	Differential	MIPI CSI differential data2 positive
74	CLK2_p	Output	Differential	General purpose high speed differential clock2 positive from i.MX6.
75	CSI_D2M	Input	Differential	MIPI CSI differential data2 negative
76	CLK2_n	Output	Differential	General purpose high speed differential clock2 negative from i.MX6.
77	GND	Power	0V	Ground
78	GND	Power	0V	Ground
79	CSI_D3P	Input	Differential	MIPI CSI differential data3 positive
80	CSI_D3M	Input	Differential	MIPI CSI differential data3 negative

## 2.8 Optional Features

i.MX6 Qseven SOM supports below mentioned Optional Features which can be used if required but default not populated.

- JTAG Header
- RS232 Debug UART Header(3Pin) - For Standalone operation
- 5V Power In Connector (2Pin) - For Standalone operation
- 20Pin Header - MLB (6pin), MLB (3pin) or I2C3, GPIO

### 2.8.1 JTAG Header

A customized 20-pin ARM JTAG connector is available in i.MX6 Qseven SOM for Debug purpose. 3.3V reference power is provided to pin 1 of the connector to allow JTAG tool to automatically configure the logic signals for the right voltage. JTAG connector is physically located on top of the SOM. This is the optional feature and will not be populated in default configuration.

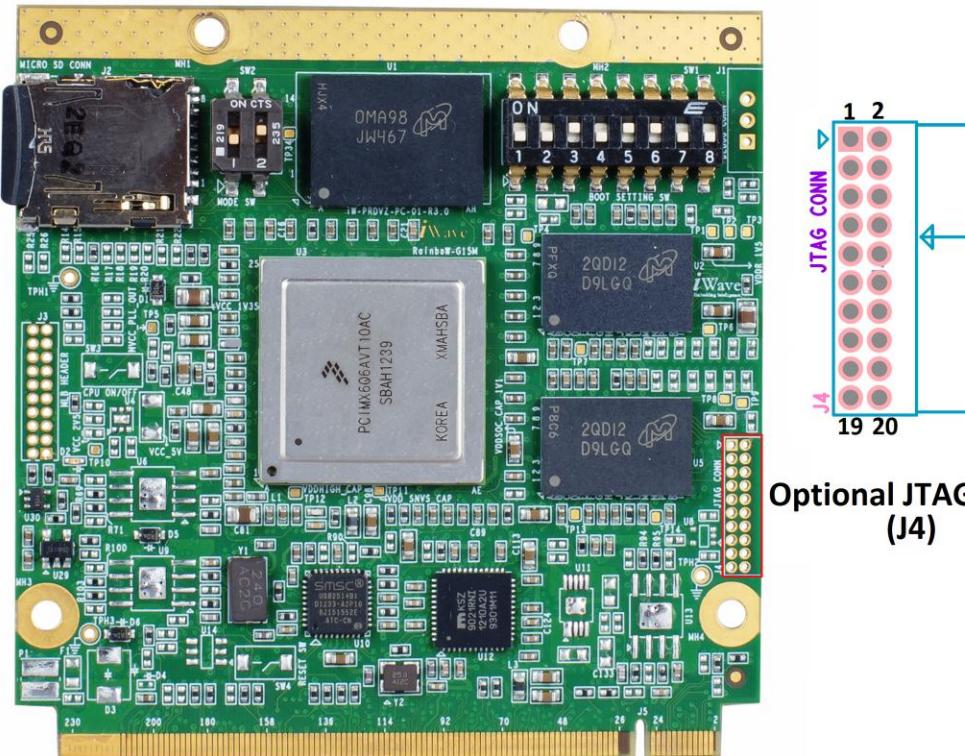


Figure 7: JTAG Connector

Table 9: JTAG Header Pin Assignment

Pin No	Signal Name	Signal Type	Voltage Level/Termination	Description
1	VCC_3V3	Power	3.3V	VREF Supply Voltage
2	VCC_3V3	Power	3.3V	Supply Voltage
3	JTAG_TRSTB	Input	3.3V CMOS	JTAG Test Reset signal
4	GND	Power	0V	Ground
5	JTAG_TDI	Input	3.3V CMOS	JTAG Test data input
6	GND	Power	0V	Ground
7	JTAG_TMS	Input	3.3V CMOS	JTAG Test mode select
8	GND	Power	0V	Ground
9	JTAG_TCK	Input	3.3V CMOS	JTAG Test Clock
10	GND	Power	0V	Ground
11	RTCK	Output	3.3V CMOS/ 10K Pull-down	Not used
12	GND	Power	0V	Ground
13	JTAG_TDO	Output	3.3V CMOS	JTAG Test Data output
14	GND	Power	0V	Ground
15	JTAG_RESETB	Input	3.3V CMOS	Reset Signal
16	GND	Power	0V	Ground
17	DBGRQ	Input	3.3V CMOS/ 10K Pull-up	Not used
18	GND	Power	0V	Ground
19	DBGACK	Output	3.3V CMOS/ 10K Pull-down	Not used
20	GND	Power	0V	Ground

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The below table provides the JTAG Circuit BOM which can be used to mount the JTAG in i.MX6 Qseven SOM and use it.

**Table 10: JTAG Header - BOM**

Sl. No.	Part Description	Part Number	Identifier	Package	Quantity
1	CONN HEADER .05" 20PS DL PCB R/A	GRPB102MWCN-RC	J4	20Pin TH	1
2	IC BUFFER TRI-ST ULP N- INV SC705	NC7SP125P5X	U8	8-Lead SC70	1
3	RES 0.0 OHM 1/16W	RC0402JR-070RL	R62,R233	0402	2
4	RES 10.0K OHM 1/16W 5%	RC0402JR-0710KL	R77, R91, R238, R240, R244, R258, R269	0402	3
5	CAP CERAMIC .1UF 10V X5R	CC0402KRX5R6BB104	C101	0402	1
6	CONN HEADER .050" 20PS DL PCB AU	LPPB102CFFN-RC	Mating connector for J4	NA	1

*Note: For i.MX6 SOM Silkscreen identifier details, refer **APPENDIX I***

## 2.8.2 Debug UART Header

A 3pin UART2 connector (J1) can be used for Debug purpose. This UART connector supports only Serial data input and serial data output signals in RS232 level. This 3-Pin Debug UART Connector is physically located on top of the SOM. This is the optional feature and will not be populated in default configuration.

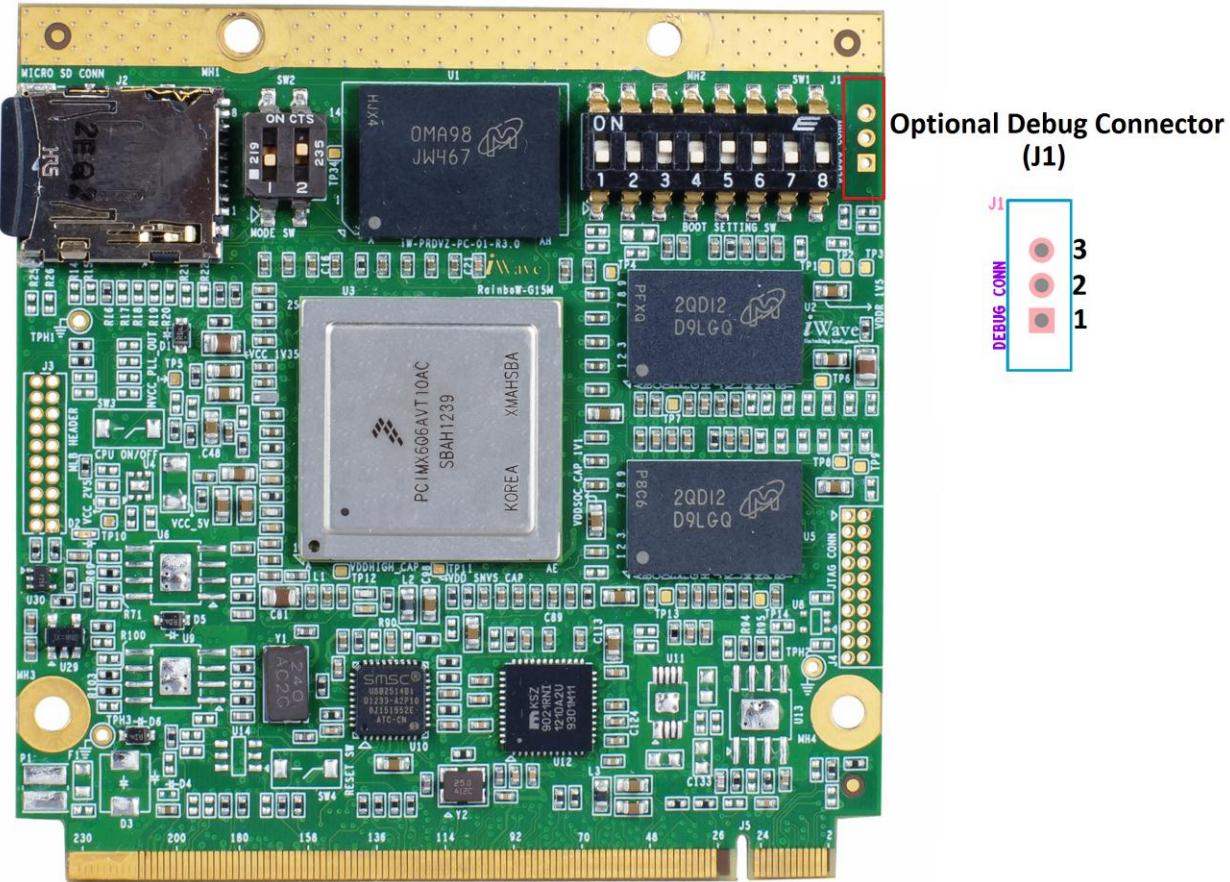


Figure 8: UART Connector

Table 11: Debug UART Header Pin Assignment

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground
2	UART2_TXD(EIM_D26)	Output	RS232 Level	Transmit data
3	UART2_RXD(EIM_D27)	Input	RS232 Level	Receive data

# i.MX6 Qseven System On Module Hardware User Guide

The below table provides the Debug UART circuit BOM which can be used to mount the Debug UART in i.MX6 Qseven SOM and use it.

**Table 12: Debug UART Header - BOM**

Sl. No.	Part Description	Part Number	Identifier	Package	Quantity
1	IC RS232 DRVR/RCVR	MAX3232IPWR	U16	16-TSSOP	1
2	CONN HEADER 3POS 2MM R/A	35363-0360	J1	3Pin TH	1
3	RES 0.0 OHM 1/16W	RC0402JR-070RL	R187, R12	0402	2
4	CAP CERAMIC .1UF 10V X5R	CC0402KRX5R6BB104	C1,C2,C3, C5,C160	0402	5
5	CAP CER 10UF 10V X5R	C1608X5R1A106M	C165	0603	1
6.	CONN RECEPTACLE HOUSING 3POS 2MM	35507-0300 (from Molex)	Mating connector for J1	NA	1

*Note: For i.MX6 SOM Silkscreen identifier details, refer APPENDIX I*

*Note: If On-SOM Debug UART Header is mounted, make sure to not use Debug UART connection in Qseven Edge connector because both are sharing the same signals. To isolate Debug UART signal connection to Qseven Edge connector, remove resistors R314 & R316 in i.MX6 SOM.*

### 2.8.3 Power IN Connector

i.MX6 Qseven SOM will work with +5V power input from Qseven Edge connector. Optionally SOM can be Power Up using Power IN Header (P1) for standalone purpose. Power connector P1 is the optional feature and will not be populated in default configuration.

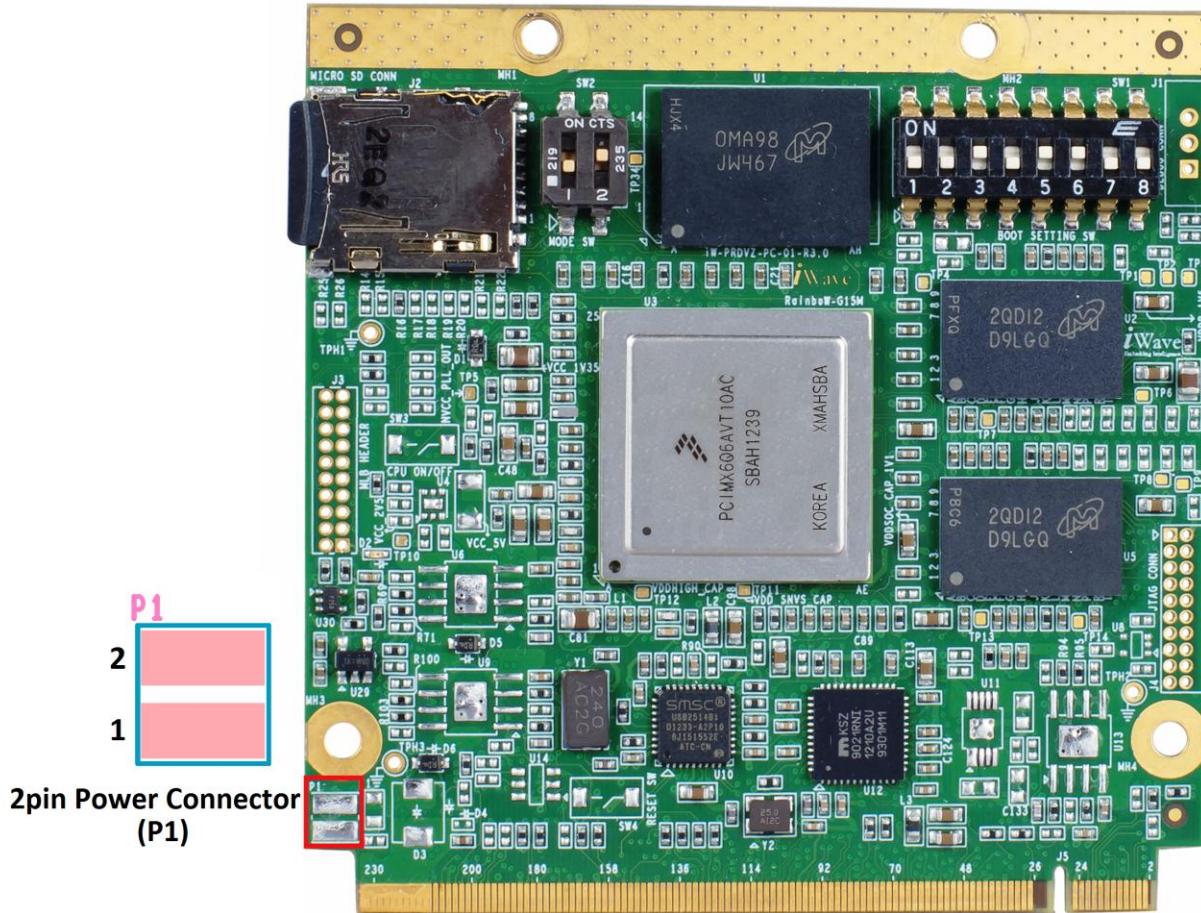


Figure 9: 2Pin Power connector

Table 13: 2pin Power Connector

Pin No	Signal Name	Signal Type	Voltage Level / Termination	Description
1	VCC_IN	Power	5V Power	5V Input Power
2	GND	Power	GND	Ground

# i.MX6 Qseven System On Module Hardware User Guide

The below table provides the power IN circuit BOM which can be used to mount power IN circuit for standalone i.MX6 Qseven SOM power up.

**Table 14: Power IN Connector - BOM**

Sl. No.	Part Description	Part Number	Identifier	Package	Quantity
1	CONN HEADER VERT 2CKT 2.5MM	0099990986	P1	2Pin TH	1
2	FUSE FAST 24VDC 3A	SF-0603F300-2	F1	0603	1
3	DIODE SCHOTTKY 4A 40V SMB	SSB44-E3/52T	D3	SMB	1
4	TVS ESD PROT ULT LOW CAP SOD-923	ESD9L5.0ST5G	D4	SOD-923	1
5	CAP CERAMIC .1UF 10V X5R	CC0402KRX5R6BB104	C150	0402	1
6	CAP CER 1.0UF 10V X5R 10%	C1005X5R1A105K	C151	0402	1
7	CAP CER 10UF 10V X5R	C1608X5R1A106M	C310	0603	1
8	CAP CER 100UF 6.3V X5R	GRM31CR60J107ME39L	C308	1206	1
9	CONN HOUSING 2POS 2.5MM SHROUD	0050375023	Mating connector for P1	NA	1
10	CONN FEMALE 22-28AWG 2.5MM TIN	0008701039	Mating connector crimp pin	NA	2

*Note: For i.MX6 SOM Silkscreen identifier details, refer APPENDIX I*

## 2.8.4 20 Pin Optional Header

i.MX6 Qseven SOM supports 20 pin MLB header to support MLB expansion. This is the optional feature and will not be populated in default configuration.

Number of Pins - 20

Connector Part Number- GRPB102VWVN-RC

Mating Connector - LPPB102CFNN-RC from Sullins Connector Solutions

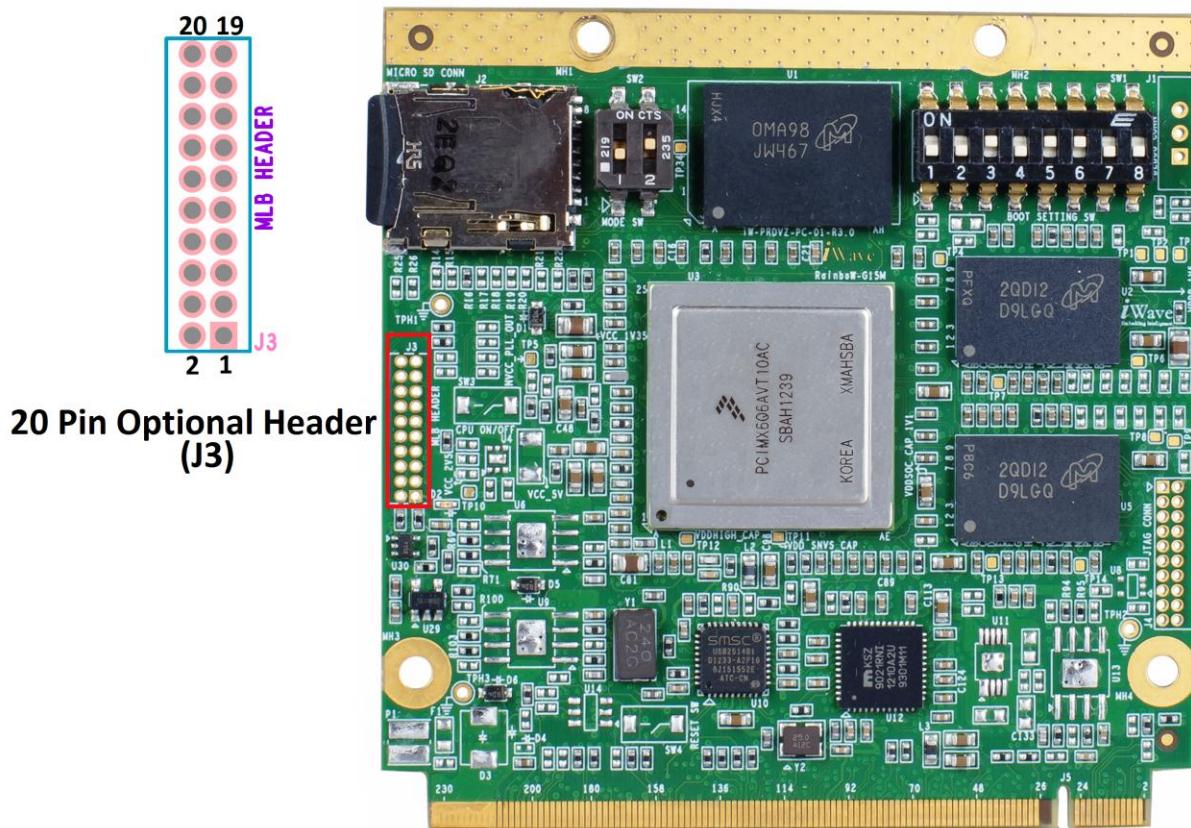


Figure 10: 20Pin Optional Header

**Table 15: 20Pin Optional Header Pin Assignment**

Pin No	Signal Name	Signal Type	Voltage Level / Termination	Description
1	VCC_3V3	Power	3.3V	Supply voltage
2	VCC_3V3	Power	3.3V	Supply voltage
3	MLB_DP	Input/Output	LVDS	Media Local Bus differential data line positive
4	UART3_CTS(EIM_D30)	Output	3.3V CMOS	UART3 Clear to Send
5	MLB_DN	Input/Output	LVDS	Media Local Bus differential data line negative
6	UART3_RTS(SD3_RST)	Input	3.3V CMOS	UART3 Request to Send
7	GND	Power	0V	Ground
8	CLK2_p	Output	LVDS	General purpose high speed differential clock2 positive
9	MLB_CP	Output	LVDS	Media Local Bus differential clock line positive
10	CLK2_n	Output	LVDS	General purpose high speed differential clock2 negative
11	MLB_CN	Output	LVDS	Media Local Bus differential clock line negative
12	GND	Power	0V	Ground
13	GND	Power	0V	Ground
14	MLBDAT(GPIO_2)	Input/Output	3.3V CMOS	Media Local Bus single ended data line
15	MLB_SP	Output	LVDS	Media Local Bus differential signal line positive
16	ESAI_HCKR(GPIO_3)	Output	3.3V CMOS	Media Local Bus single ended clock line
17	MLB_SN	Output	LVDS	Media Local Bus differential signal line negative
18	MLBSIG(GPIO_6)	Output	3.3V CMOS	Media Local Bus single ended signal line
19	GND	Power	0V	Ground
20	GND	Power	0V	Ground

*Note: All the signals in this connector are going to Expansion connectors also and so provide care while using this connector.*

## 3. ELECTRICAL SPECIFICATION

### 3.1 i.MX6 Qseven SOM Power Input Requirement

i.MX6 Qseven SOM is designed to be driven with a single +5V input power rail (VCC) from Qseven Edge connector. Optionally we can use On-SOM Power In connector to feed +5V to SOM which can be used ONLY for standalone power up.

Additionally, two optional power rails are specified in Qseven Specification to provide a +5V standby voltage and +3V RTC supply voltage.

i.MX6 Qseven SOM doesn't support +5V standby voltage (VCC\_5V\_SB) input because ARM core CPUs doesn't support Standby functionality. In i.MX6 SOM, VCC\_5V\_SB input from Qseven is not used.

The below table provides the Power Input Requirement of i.MX6 Qseven SOM.

**Table 16: i.MX6 Qseven SOM Power Requirement**

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC	4.75V	5V	5.25V	±50mV
2	VCC_5V_SB	NC	NC	NC	NC
3	VCC_RTC	2.8V	3V	3.3V	±20 mV

i.MX6 CPU's RTC module takes high current around 275mA as per i.MX6 datasheet. So there is a chance that RTC battery may drain very soon. The below table provides the RTC Circuit BOM which can be used to isolate the RTC functionality in i.MX6 Qseven SOM.

**Table 17: RTC Circuit - BOM**

Sl. No.	Part Description	Part Number	Identifier	Package	Quantity
1	DIODE SCHOTTKY 1A 20V SOD-323	NSR0320MW2T1G	D6	SOD-323	1

*Note: For i.MX6 SOM Silkscreen identifier details, refer APPENDIX I*

## 3.2 i.MX6 Qseven SOM Power Input Sequencing

i.MX6 Qseven SOM Power Input sequence requirement is explained below.

### Power Up Sequence:

- VCC\_RTC must come up at the same time or before VCC comes up.
- PWGIN must be active at the same time or after VCC comes up.

### Power Down Sequence:

- PWGIN must be inactive at the same time or before VCC goes down.
- VCC must go down at the same time or before VCC\_RTC goes down.

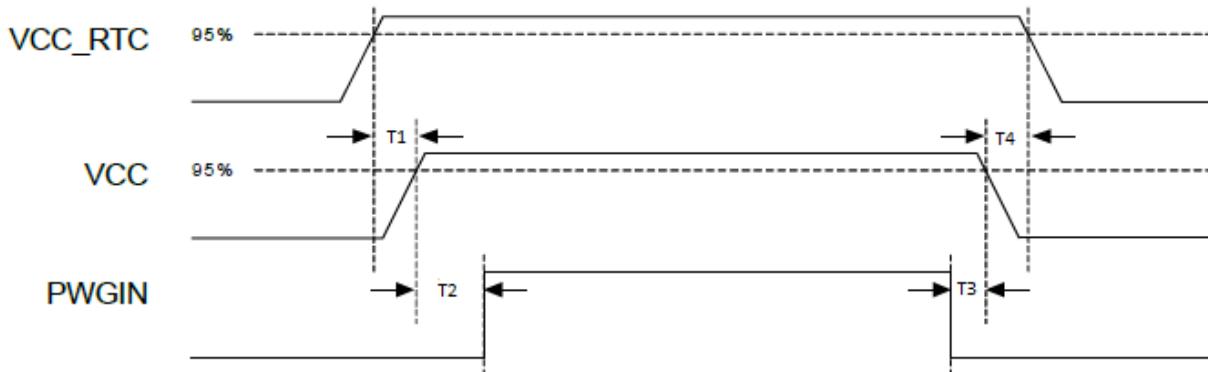


Figure 11: Qseven SOM Power Sequence

Table 18: Power Sequence Timing

Item	Description	Value
T1	VCC_RTC rise time to VCC rise time	$\geq 0$ ms
T2	VCC rise time to PWGIN rise time	$\geq 0$ ms
T3	PWGIN fall time to VCC fall time	$\geq 0$ ms
T4	VCC fall time to VCC_RTC fall time	$\geq 0$ ms

### 3.3 i.MX6 Qseven SOM Power Consumption

i.MX6 Qseven SOM Power consumption is measured in iWave's RainboW-G15D-i.MX6 Qseven Development Platform while running different power scripts in Linux 3.0.35 Kernel without enabling/implementing any Power Management feature.

**Table 19: i.MX6 Qseven SOM Power Consumption Report**

SI No.	Power Script	Power Script Operation	I <sub>max(A)</sub> @5V Input
1	Playing Video	LVDS - Run the VGA video (akiyo.mp4) on LVDS using VPU Decoder library	0.57
		HDMI - Run the 1080p video (fast.mov) on HDMI using Gstreamer application	0.67
2	Playing Audio	Run the MP3 file using Gplay Application on AC97 Audio Out	0.65
3	Playing 3D Graphics Demo	3D Gaming Bench Mark - Run the OpenGL Graphics application on LVDS	0.78
4	Dhrystone	Run the dry2 application	1
5	Maximum Power Test	Run all the below applications in parallel, 1. Run the VGA video (akiyo.mp4) on HDMI using GStreamer application 2. Run the VGA video (akiyo.mp4) and OpenGL Graphics application on LVDS alternatively. 3. Run the Ethernet ping test on back ground 4. Transfer the files between USB and Micro SD 5. Run the MP3 file using Gplay Application on AC97 Audio Out 6. Run the dry2 application on back ground	1.45
		Run all the above application with below one change, Instead of VGA Video run 1080p video (fast.mov) on HDMI using GStreamer application	1.62

*Note: Power Consumption is measured in particular condition and it may vary platform to platform based on board configuration. Depending upon board configuration, overall system design and cooling mechanism, customer may need to choose the appropriate heat solution.*

*iWave's i.MX6 Qseven Development platform uses the below Heat Sink Part,*

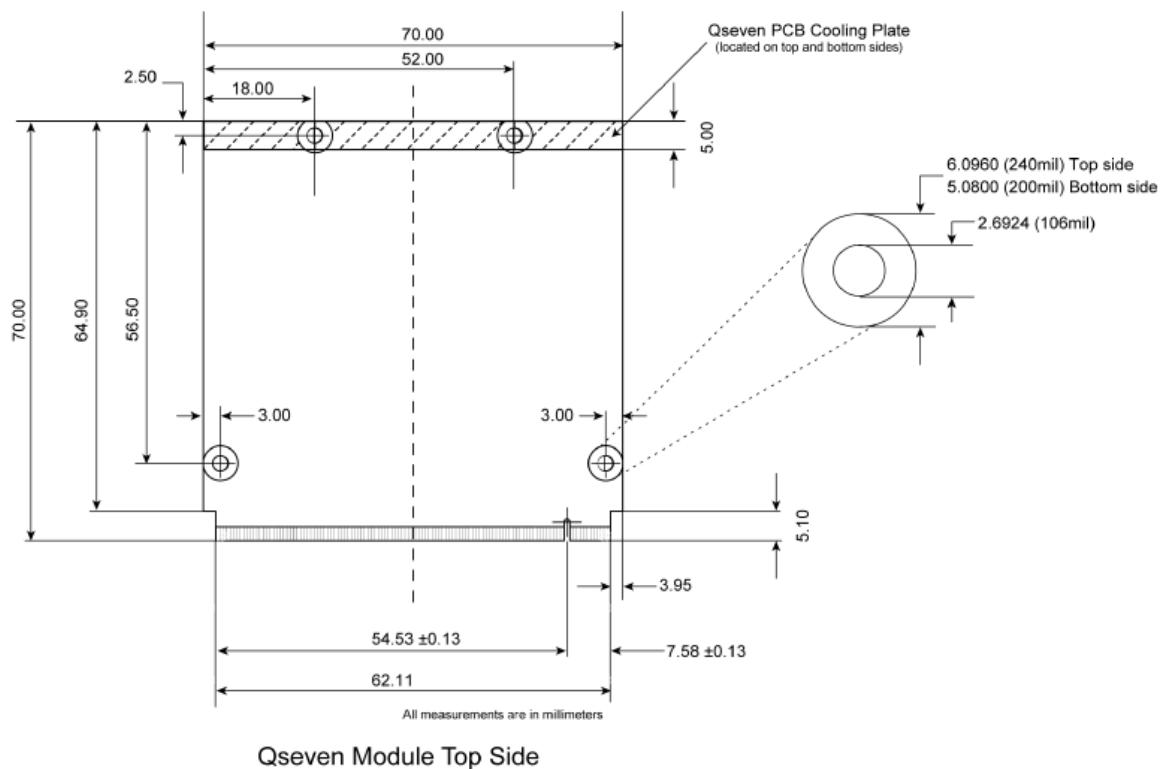
*Part Number : APF19-19-13CB/A01*

*Manufacturer : CTS Thermal Management Products*

## 4. MECHANICAL SPECIFICATION

### 4.1 Qseven SOM Mechanical Dimensions

i.MX6 Qseven SOM is fully compatible with Qseven specification Revision 1.2. The size of the PCB will be 70 mm x 70 mm x 1.2mm as per Qseven Specification. Qseven SOM mechanical dimension is shown below. Please refer the Qseven Specification Revision 1.2 for more details.



**Figure 12: Mechanical dimension of Qseven SOM**

*Note: The Qseven PCB cooling plate shown above is to be used as a cooling interface between the Qseven module and the application specific cooling solution.*

## 4.2 Expansion Connector's Placement

i.MX6 Qseven SOM has two Expansion connectors to provide more interfaces to carrier card along with standard pin out Qseven edge connector. Please see the below figure for the mechanical placement detail of Qseven mating connector and two expansion connector's mating connector in custom carrier board.

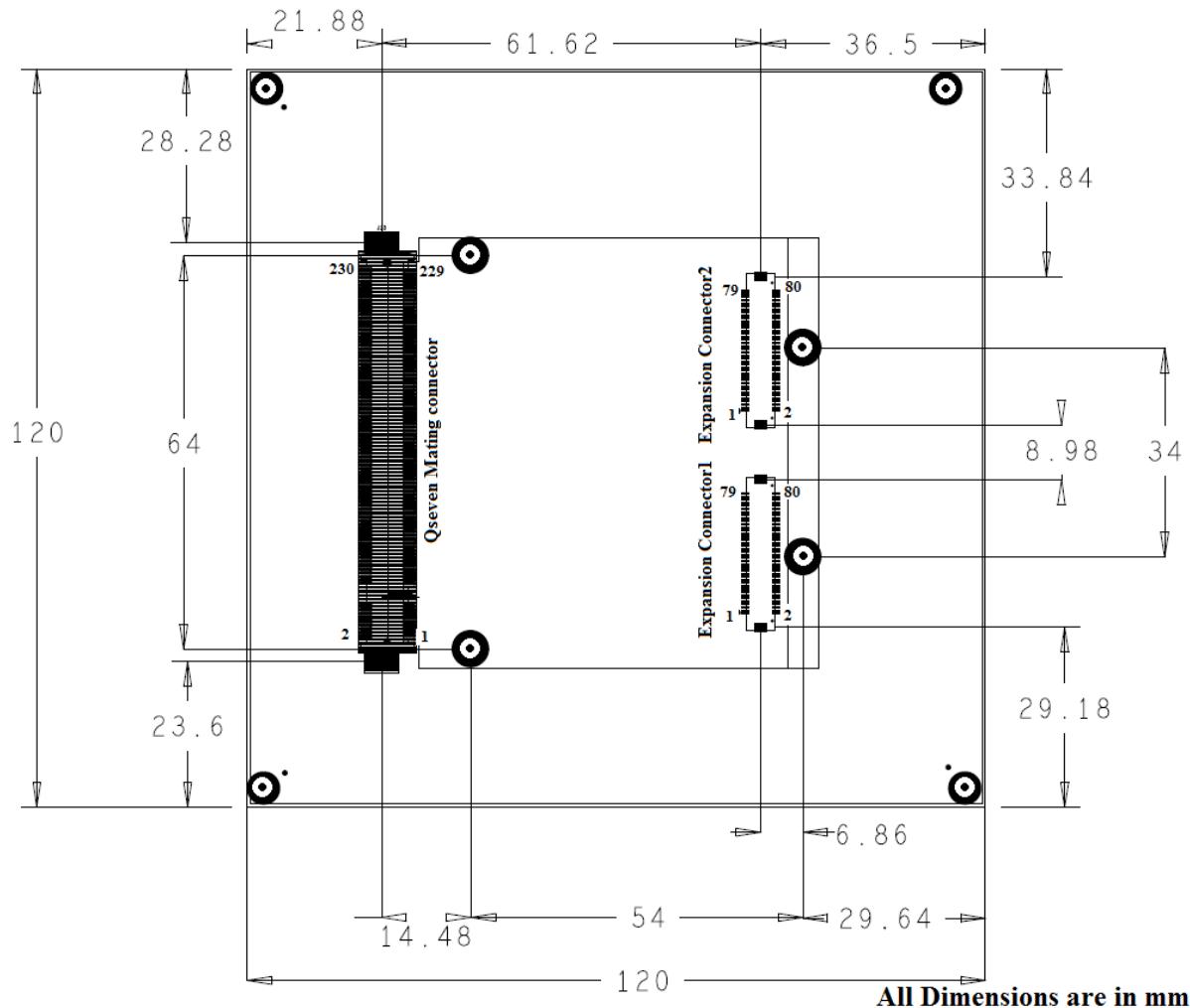
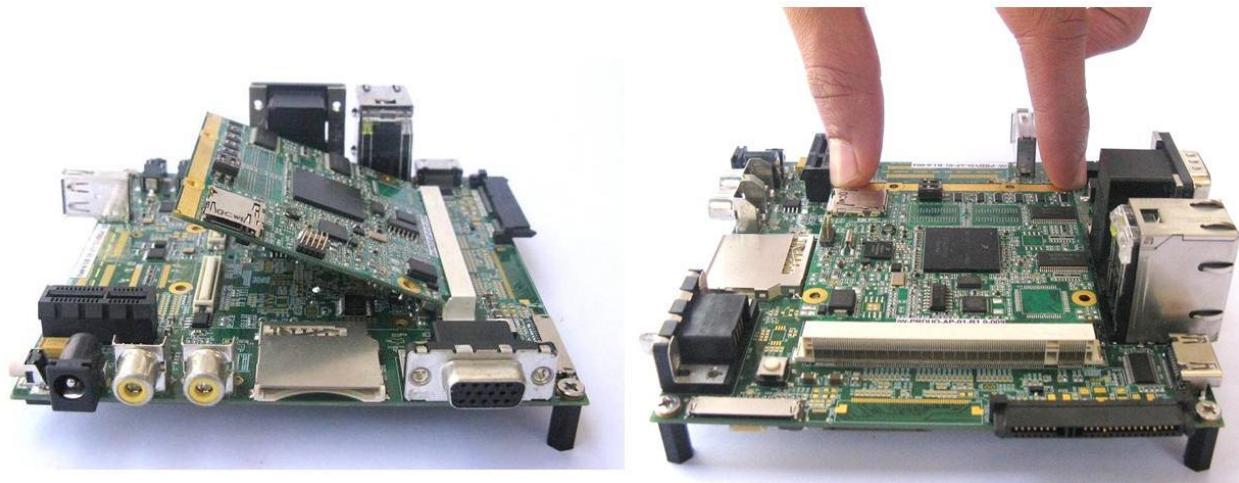


Figure 13: Connectors placement details in carrier card

Note: The above example shows the mechanical placement details of Qseven PCB Edge mating connector, two expansion connector's mating connector and Qseven SOM's mating mounting holes in iWave's Nano-ITX form factor (120mm x 120mm) Generic Qseven carrier board.

## 4.3 Guidelines to insert the Qseven SOM into Carrier board

- Make sure that the carrier board is completely powered off.
- Insert the Qseven module in to the MXM connector at an angle of 45° as shown below in the first photo.
- Check the Notch position of Qseven module is proper while inserting.
- Once the Qseven module is inserted to the MXM connector properly, press the board vertically down as shown below (in the second photo), such that the board is fixed firmly into the expansion connectors.



**Figure 14: Qseven Module Insertion procedure**

*Note: Photo shown above is for only reference and not exactly represents i.MX6 Qseven SOM*

## 5. SOM NUMBERING & REVISION

### 5.1 i.MX6 Qseven SOM Numbering

In all i.MX6 Qseven production SOMs, unique number is pasted as a label with Barcode readable format on the bottom side of SOM as shown below.

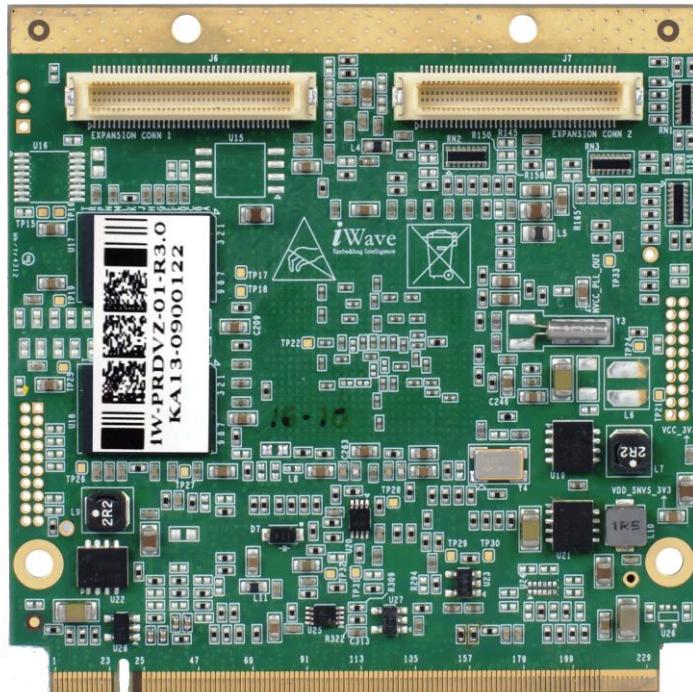


Figure 15: Production SOM Labelling

In the Label, the SOM numbering is mentioned in two rows as explained below,

**iW-PRDVZ-01-Rx.y**

**iW-PRDVZ-01-R** – Fixed characters represents iWave's i.MX6 Qseven SOM

**x** – Running number represents SOM revision (2- Proto SOM, 3 - Production SOM)

**y** – Running number represents SOM Assembly Configuration

**AANN-NNNNNNN**

**AA** – Running character represents Manufacturing code

**NN-NNNNNNN** – Running number represents SOM Unique Number

*Note: i.MX6 Qseven Proto SOMs (R2.0) and first batch R3.2 SOMs did not have the above label and can be identified with number "iW-PRDVZ-AP-01-R2.0/R3.2-NNN" which was pasted on Top side of the SOM*

## 5.2 i.MX6 Qseven SOM Revision History

i.MX6 Qseven Production version SOM is fully Hardware & Software compatible with Proto SOM minor updates as explained below.

**Table 20: SOM Revision History**

Sl. No.	Change Description	i.MX6 Proto SOM (R2.0)	i.MX6 Production SOM (R3.0)
PCB Changes			
1	Qseven Edge Connector 16 <sup>th</sup> Pin connection	This pin is pulled up with 10K	This pin is connected to EIM_WAIT signal for GPIO purpose through resistor and default populated.
2	Qseven Edge Connector 124 <sup>th</sup> Pin connection	This pin is connected to DISP0_DAT2 signal as General purpose I/O through resistor and default populated.	This pin is connected to GPIO5_2_HDMI_CEC(EIM_A25) signal for HDMI CEC functionality through resistor and default populated. This option is added to make i.MX6 SOM compatible with Qseven R2.0 specification.
3	Qseven Edge Connector 171 <sup>st</sup> Pin connection	NC	This pin is optionally connected to UART5 TX signal (CPU Pin name: KEY_COL1) through resistor and default not populated. This option is added to make i.MX6 SOM compatible with Qseven R2.0 specification.
4	Qseven Edge Connector 172 <sup>nd</sup> Pin connection	NC	This pin is optionally connected to UART5 CTS signal (CPU Pin name: KEY_ROW4) through resistor and default not populated. This option is added to make i.MX6 SOM compatible with Qseven R2.0 specification.
5	Qseven Edge Connector 177 <sup>th</sup> Pin connection	NC	This pin is optionally connected to UART5 RX signal (CPU Pin name: KEY_ROW1) through

			resistor and default not populated. This option is added to make i.MX6 SOM compatible with Qseven R2.0 specification.
6	Qseven Edge Connector 178 <sup>th</sup> Pin connection	NC	This pin is optionally connected to UART5 RTS signal (CPU Pin name: KEY_COL4) through resistor and default not populated. This option is added to make i.MX6 SOM compatible with Qseven R2.0 specification.
7	SATA RX differential pair termination	No Termination	100E parallel termination is added between SATA RX differential pairs and default populated
<b>Assembly Configuration Changes</b>			
8	Default Boot Media	Micro SD Card <i>Note: eMMC Flash is not populated.</i>	eMMC Flash <i>Note: eMMC Flash &amp; Micro SD connector is populated.</i>
9	i.MX6 CPU LDO Mode	Supports only CPU LDO Enable Mode by providing 1.35V to i.MX6 CPU's power pins VDDARM_IN & VDDSOC_IN. This is done by mounting R103 resistor value to 16.2K (1% Tolerance, 0402 package). <i>Note: Software change is also required between LDO bypass mode and LDO Enable Mode.</i>	Supports only CPU LDO Bypass Mode by providing 1.275V to i.MX6 CPU's power pins VDDARM_IN & VDDSOC_IN. This is done by mounting R103 resistor value to 14.3K (1% Tolerance, 0402 package). <i>Note: Software change is also required between LDO bypass mode and LDO Enable Mode</i>
10	SATA Transmit & Receive pair AC coupling	No AC coupling	0.01uF AC coupling in SATA transmit and Receive pair signals
11	PCIe Reference clock pair AC coupling	0.1uF AC coupling in PCIe Reference clock pair signals	No AC coupling
12	RTC Battery connection	VCC_RTC from Qseven is connected to i.MX6 CPU's RTC	VCC_RTC from Qseven is connected to i.MX6 CPU's RTC

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		Power Input pin VDD_SNVS_IN through OE resistor	Power Input pin VDD_SNVS_IN through Schottky diode
13	SPDT switch to select Debug UART & JTAG in Qseven Edge connector	SPDT Switch is populated to select Debug UART & JTAG on the fly.	SPDT switch is not populated and directly Debug UART is connected to Qseven connector

*Note: Assembly configuration of i.MX6 Qseven SOM may change without prior notice. Contact iWave for latest assembly configuration.*

## 6. APPENDIX I

### 6.1 i.MX6 Qseven SOM Silk Screen

i.MX6 Qseven SOM's PCB silkscreen top view and bottom view with Optional Feature's Identifier highlighted are shown in the below Figures. This will be useful while mounting the Optional Features in i.MX6 Qseven SOM.



Figure 16: Silk Screen Top View

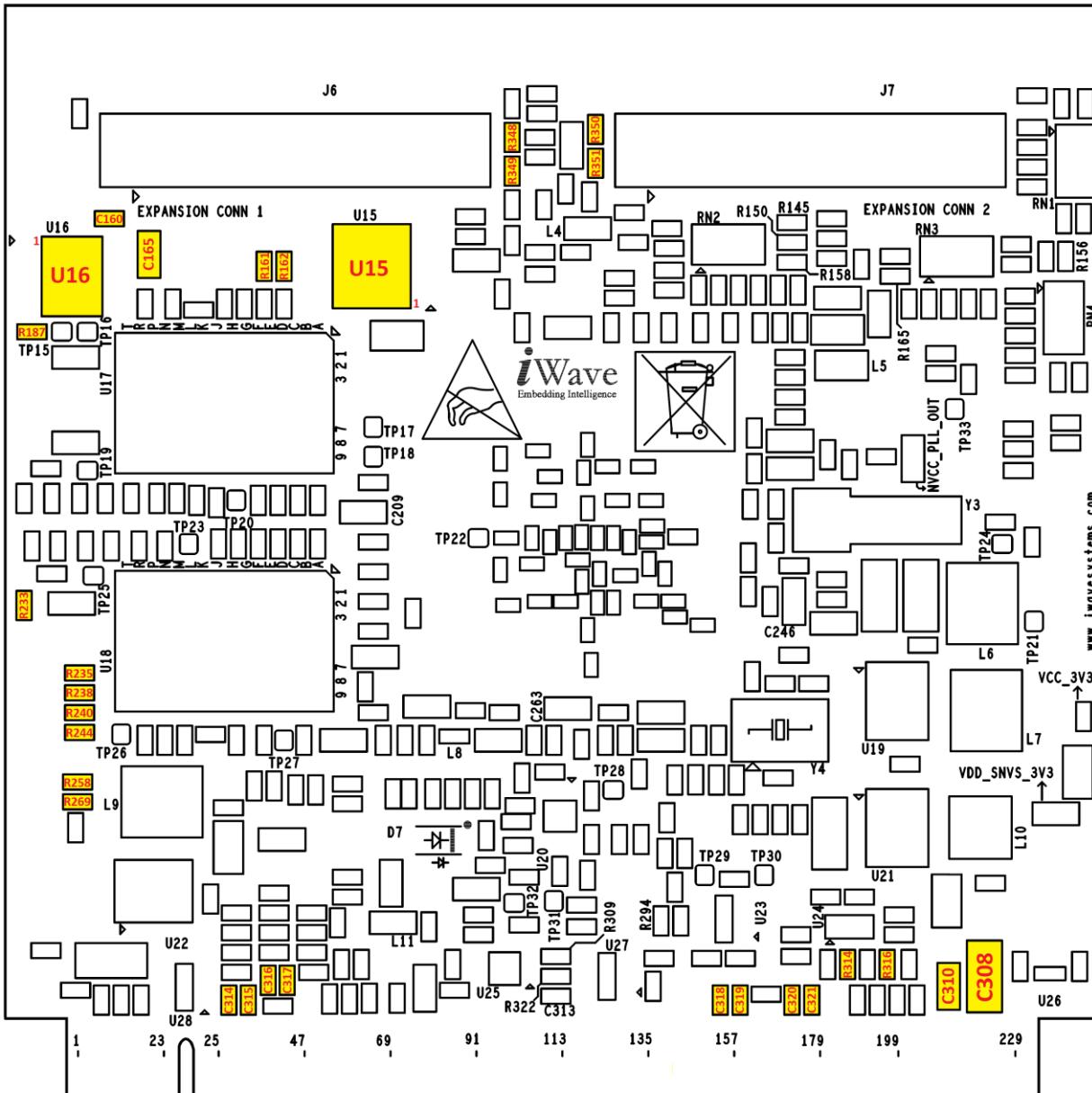


Figure 17: Silk Screen Bottom View

## 7. APPENDIX II

### 7.1 i.MX6 Qseven SOM Development Platform

iWave supports Generic Qseven Carrier Board which is targeted for quick validation of high performance Qseven compatible CPU modules. Being a Nano-ITX form factor with 120mmx120mm size, the carrier board is highly packed with all necessary interfaces & on-board connectors to validate complete Qseven supported features.

iWave supports RainboW-G15D - i.MX6 Qseven Development Platform with i.MX6 Qseven SOM and Generic Qseven Carrier board for complete validation of i.MX6 SOM functionality with complete BSP support. For more details on i.MX6 Qseven SOM Development platform, visit the below URL of iWave Website.

<http://www.iwavesystems.com/product/development-platform/i-mx6-q7-development-kit-18/i-mx6-q7-development-kit.html>

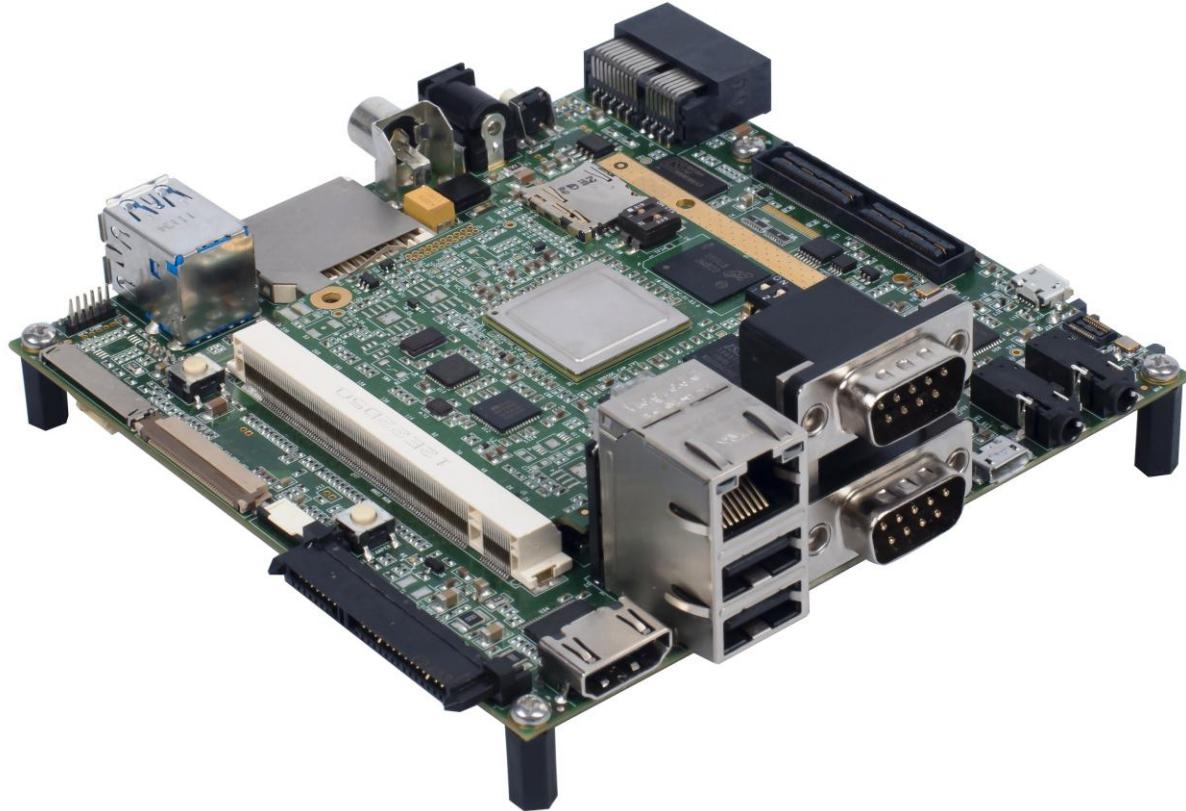


Figure 18: i.MX6 Development Platform