PI7C9X20404GP / PI7C9X20505GP / PI7C9X20508GP / PI7C9X20303SL / PI7C9X20404SL / PI7C9X20303UL / PI7C9X2G303EL / PI7C9X2G404EL / PI7C9X2G303UL / PI7C9X2G304SL / PI7C9X2G304SL / PI7C9X442SL / PI7C9X440SL
PCI Express® Packet Switch / Swidge
SMBus Programming Guide

1. Introduction

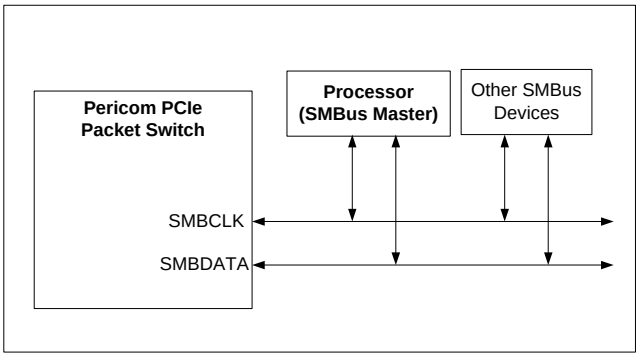
The Pericom PCIe® Packet Switches provide the System Management Bus (SMBus), a two-wire interface through which a simple device can communicate with the rest of the system. The SMBus interface on the packet switches is a bi-directional slave interface. It can receive data from the SMBus master or send data to the master. The interface allows full access to the configuration registers in the offset 00h to FFh range. A SMBus master, such as the processor or other SMBus devices, can read or write to every RW configuration register (read/write register) in the accessible range. In addition, the RO and HwInt registers (read-only and hardware initialized registers) that can be auto-loaded by the EEPROM interface can also be read and written by the SMBus interface. This feature allows increases in the system expandability and flexibility in system implementation.

2. SMBus Interface

The SMBus interface on the packet switches consists of one SMBus clock pin (SMBCLK), a SMBus data pin (SMBDATA), and 3 SMBus address pins (GPIO[5:7]). The SMBus clock pin provides or receives the clock signal. The SMBus data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The SMBus address pins determine the address to which the packet switch responds to. The SMBus address pins generate addresses according to the following table:

Table 2-1 SMBus Address Pin Configuration

BIT	SMBus Address
0	GPIO[5]
1	GPIO[6]
2	GPIO[7]
3	1
4	0
5	1
6	1



SMBus Implementation

3. Guideline for Programming SMBus

The SMBus commands are issued by the SMBus of the south bridge of the chipset. This guide uses the south bridge of Intel ICH7 family as an example and demonstrates step-by-step how to write and read the content of the configuration register, “Offset 00h – Vendor ID”.

Please refer to the chapter related SMBus Controller Registers in Intel Chipset Datasheet.

3.1. Write Operation

Write Word Protocol (PEC disabled):

S + Slave Address[6:0] + 0 (Wr) + A + 0000_1000 + A + Offset[7:0] + A + Port[7:0] + A + P

S + Slave Address[6:0] + 0 (Wr) + A + 0000_1000 + A + Data[7:0] + A + Data[15:8] + A + P

Slave Address[6:0]: SMBus Address
Offset[7:0]: Configuration Register Offset
Port[7:0]: Port Number
  For GENI/GENII packet switch
    0... upstream port 1
    1... downstream port 1
    2... downstream port 2
    3... downstream port 3
    4... downstream port 4

For Swidge,
    0... upstream port 1

1... downstream port 1
2... downstream port 2
4... func 0
5... func 1
6... func 2

The following steps are used to set the "Offset" and "Port" values:
- Write “00001000b” to HST_CMD (Host Command Register)
- Write “11010000b” to XMIT_SLVA (Transmit Slave Address Register)
  bit 7:1 - SMBUS Address
  bit 0 - Direction of the host transfer
  0=Write
  1=Read
- Write “00000000b” to HST_D0 (Host Data 0 Register) to
  This value is used to set "Offset[7:0]”. Because we are writing to “Vendor ID” (offset 00h), the value is filled with 0’s.
- Clear SMBus interface’s status by writing “ffh” to HST_STS (Host Status Register).
- Write “01001100b” to HST_CNT (Host Control Register)
  Please refer to the datasheet of the south bridge to for detail information of the HST_CNT Register.
- Read HST_STS (Host Status Register) to check whether this transaction is completed or not
  bit 0 - HOST_BUSY
  bit 1 - INTR
  bit 2 - DEV_ERR
  If "bit 1=1", this transaction is completed successfully.
  If "bit 2=1", an error has occurred in this transaction.

Repeat the steps below to write data to the register you want to change
- Write “00001000b” to HST_CMD(Host Command Register)
- Write “11010000b” to XMIT_SLVA (Transmit Slave Address Register)
  bit 7:1 - SMBUS Address
  bit 0 - Direction of the host transfer
- Write “0x34” to HST_D0 (Host Data 0 Register)
  This value is used to set "Data[7:0]. Suppose we are changing the Vendor ID to “0x1234”, the value is set to “0x34”.
- Write “0x12” to HST_D1 (Host Data1 Register)
  This value is used to set "Data[15:8]. Suppose we are changing the Vendor ID to 0x1234, the value is set to” 0x12”.
- Clear SMBus interface’s status by writing “ffh” to HST_STS (Host Status Register).
- Write “01001100b” to HST_CNT (Host Control Register)
  Please refer to the datasheet of the south bridge to for detail information of the HST_CNT Register.
- Read HST_STS (Host Status Register) to check whether this transaction is completed or not
  bit 0 - HOST_BUSY
  bit 1 - INTR
  bit 2 - DEV_ERR
  If "bit 1=1", this transaction is completed successfully.
  If "bit 2=1", an error has occurred in this transaction.

3.2. Read Operation

Read Word Protocol (PEC disabled):
S + Slave Address[6:0] + 0(Wr) + A + 0000_1000 + A + Offset[7:0] + A + Port[7:0] + A + P
S + Slave Address[6:0] + 0(Wr) + A + 0000_1000 + A + S + Slave Address[6:0] + 1(Rd) + A + Data[7:0] + A + Data[15:8] + A + P

Slave Address[6:0]: SMBus Address
Offset[7:0]: Configuration Register Offset
Port[7:0]: Port Number
For GENI/GENII packet switch
0... upstream port 1
1... downstream port 1
2... downstream port 2
3... downstream port 3
4... downstream port 4

For Swidge,
0... upstream port 1
1... downstream port 1
2... downstream port 2
4... func 0
5... func 1
6... func 2

The following steps are used to set the "Offset" and "Port" values:
- Write “00001000b” to HST_CMD (Host Command Register)
- Write “11010000b” to XMIT_SLVA (Transmit Slave Address Register)
  bit 7:1 - SMBUS Address
  bit 0 - Direction of the host transfer
- Write “00000000b” to HST_D0 (Host Data 0 Register)
  This value is used to set "Offset[7:0]. Because we are reading the VendorID (offset 00h), the value is filled with 0’s.
- Clear SMBus interface’s status by writing “ffh” to HST_STS (Host Status Register).

- Write “01001100b” to HST_CNT (Host Control Register)
  Please refer to the datasheet of the south bridge for detail information of the HST_CNT Register.
- Read HST_STS (Host Status Register) to check whether this transaction is completed or not
  bit 0 - HOST_BUSY
  bit 1 - INTR
  bit 2 - DEV_ERR
  If "bit 1=1", this transaction is completed successfully.
  If "bit 2=1", an error has occurred in this transaction.

Repeat the steps below to read the value from the register

- Write “00001000b” to HST_CMD (Host Command Register)
- Write “11010001b” to XMIT_SLVA (Transmit Slave Address Register)
  bit 7:1 - SMBUS Address
  bit 0 - Direction of the host transfer
  0 = Write
  1 = Read
- Clear SMBus interface’s status by writing “ffh” to HST_STS (Host Status Register).
- Write “01001100b” to HST_CNT (Host Control Register)
  Please refer to the datasheet of the south bridge for detail information of the HST_CNT Register.
- Read HST_STS (Host Status Register) to check whether this transaction is completed or not
  bit 0 - HOST_BUSY
  bit 1 - INTR
  bit 2 - DEV_ERR
  If "bit 1=1", this transaction is completed successfully.
  If "bit 2=1", an error has occurred in this transaction.
- After checking that bit 1 = 1 in the HST_STS Register, read HST_D0 and HST_D1 to get bit [7:0] and bit [15:8] of the Vendor ID Register.