PI7C9X2G404SLB/ PI7C9X2G304SLB/ PI7C9X2G404ELB/PI7C9X2G304ELB/PI7C9X2G303ELB PCI Express Gen2 Packet Switch: Errata

INTRODUCTION

This Errata document is created based upon the compatibility test results of PIC9X2G404SLB/PI7C9X2G304SLB/PI7C9X2G404ELB/PI7C9X2G304ELB/PI7C9X2G303ELB with 10 PCIe devices (including Gen1 WiFi, Gen2 USB 3.0, and SATA 6.0) on 6 PCIe Gen2 platforms (Intel X38, G45, P55, P45, X48 and X58).

DOCUMENT REVISION HISTORY

DATE	REVISION	DESCRIPTION
1/17/2014	1.1	New Errata document
7/8/2015	1.2	Add E4
7/22/2015	1.3	Add E5

SILICON REVISION

DATE	REVISION ID	DESCRIPTION
8/01/2013	05h	PI7C9X2G404SLB silicon

SUMMARY OF ERRATA

ERRATA #	DESCRIPTION	STATUS
E1	Incorrect DWNRST_L behavior with hot plug-in	Workaround available
E2	Unable to change rate from GEN1 to GEN2 with nVidia chipset	Workaround available
E3	Malfunction Due to Incorrect Lane and Polarity Inversion Configuration in PI7C9X2G304SLB/PI7C9X2G304ELB	Workaround available
E4	Incorrectly Implemented Bridge Mapping of INTx Virtual Wires	Workaround availiable
E5	ACS P2P Request Redirect Is Not Functional	Workaround available

E1: Incorrect DWNRST_L behavior with hot plug-in

Problem:
In normal operations, the DWNRST_L signal is asserted when an end device is plugged into the downstream port of the switch. Instead, the DWNRST_L signal is asserted when the end device is plugged out of the downstream port of the switch. It may cause the end device to malfunction if the end device does not have power-on-reset implementation and needs the DWNRST_L signal to operate normally.

Workaround:
The application board could add extra logic to provide RESET signal to the end device when it is plugged into the downstream port of the switch.

Status:
No fixes for this issue are planned in the next revision of silicon.

E2: Unable to change rate from GEN1 to GEN2 with nVidia chipset

Problem:
The nVidia chipset does not allow the attached device (i.e. this packet switch) to originate request for GEN1 to GEN2 change rate. The only possible way to link at GEN2 is when nVidia chipset initiates the change. The link remains in GEN1 only if the device triggers the change rate.

Workaround:
There is an option bit defined in this packet switch to turn off the commencement of the change rate. Therefore, the chip can successfully link with X58/nVidia at GEN2 rate. When the application is an embedded system, the option bit can be disabled through SMBUS before link training.

Status:
No fixes for this issue are planned in the next revision of silicon.

E3: Malfunction Due to Incorrect Lane and Polarity Inversion Configuration in PI7C9X2G304SLB/PI7C9X2G304ELB

Problem:

This issue only occurs when the x2 upstream port's lanes are reversed and one of these two lanes' polarity is reversed and the other is not reversed. In the real applications, the possibility of x2 lanes reversal is very low. Therefore, we expect that this issue is very unlikely to occur.

This happens because the device detects the polarity of each and every lane first and sets the PHY RX polarity. After lane polarity is determined, the device then detects the sequence of the lanes via Link negotiation procedure, and swaps the lanes internally is the lanes are reversed. At this step, the polarity information is swapped and not detected again. This results in incorrect polarity information for the x2 port's lane.

Workaround:

In embedded systems, designers are allowed to reverse x2 upstream port’s lanes, reverse two lanes’ polarity or reverse x2 upstream port’s lanes and two lanes’ polarity at the same time. But please be advised not to implement this configuration: reversal of x2 upstream port’s lanes, and reversal of one of these two lanes’ polarity and no reversal for the other lane.

Status:

No fixes for this issue are planned in the next revision of silicon.

E4: Incorrectly Implemented Bridge Mapping of INTx Virtual Wires

Problem:

Per PCIe specification, virtual and actual PCI to PCI Bridges map the virtual wires of the primary side to the wires of secondary side of the Bridge, based on the Device Number of the Device on the secondary side of the Bridge, as shown in the table below.

Device Number for Device on Secondary Side of Bridge	INTx Virtual Wire on Secondary Side of Bridge	Mapping to INTx Virtual Wire on Primary Side of Bridge
0,4,8,12,20,24,28	INTA	INTA
	INTB	INTB
	INTC	INTC
	INTD	INTD
1,5,9,13,17,21,25,29	INTA	INTB
	INTB	INTC
	INTC	INTD
	INTD	INTA
2,6,10,14,18,22,26,30	INTA	INTC
	INTB	INTD
	INTC	INTA
	INTD	INTB
3,7,11,15,19,23,27,31	INTA	INTD
	INTB	INTA
	INTC	INTB
	INTD	INTC

As the Packet Switch can be logically viewed as two-level cascaded multiple virtual PCI-to-PCI Bridges, where one upstream-port Bridge sits on all downstream-port Bridges, it should follow the INTx mapping rule. However, in our implementation, our switch device maps the virtual wires based on the Device Number of the Bridge. When the Device Number of the upstream port of the Packet Switch is assigned to '0', no issues are experienced. However, if the Device Number is assigned to a number other than '0', the Packet Switch will map INTx twice on both upstream and downstream port sides. This behavior of two times of mapping causes system to have non-functional INTx service due to incorrect INTx routing.

Workaround:

BIOS/Firmware needs to modify the INTx routing table when Device Number of the upstream port of the Packet Switch is assigned to a number other than '0'.

Status:

It will be fixed in the revision of silicon.

E5: ACS P2P Request Redirect Is Not Functional

Problem:
When ACS P2P Request Redirect function is enabled by setting ACS Capability Register (CFG Offset 224h, bit 18) and bandwidth between upstream port and downstream port is not balanced, packets are queued in the internal buffer of packet switch until CLPD pkt.

Workaround:
1. Do not enable ACS P2P Request Redirect function.
2. If ACS is enabled, the packet switch needs to operate under store & forward mode for forwarding packet.

Status:
No fixes for this issue are planned in the next revision of silicon.