

# PI7C9X2G304SL PCI Express Packet Switch Evaluation Board User's Manual

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3545 North 1<sup>ST</sup> Street, San Jose, CA 95134

Telephone: 1-800-435-2336 FAX: 408-435-1100

Website: http://www.pericom.com



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#### **REVISION HISTORY**

Date	Revision Number	Description	
08/20/2010	1.0	Preliminary User's Manual	
10/4/2010 1.1 Updated Figure 1.1 PI7C9X2G30		Updated Figure 1.1 PI7C9X2G304SL Evaluation	
		Board Front View (PCB ver. 2.0) and Section 2 Initial	
		Setup	
		Removed Section 3.2 Push-Button Switch	
8/12/2011	1.2	Updated to RDK	
6/14/2013	1.3	Updated Product Features	



#### 1. General Information

The PI7C9X2G304SL Evaluation board is built on the PI7C9X2G304SL, a 3-port 4-lane PCI Express Gen2 Packet Switch. The Evaluation board is a rapid and complete solution for software and hardware development with low risk and fast time-to-market. The Evaluation board allows the upstream port of the PI7C9X2G304SL packet switch to be directly plugged into a x2 PCI Express slot on a system board. The downstream slots of the Evaluation board allow connections to two other x1 PCI Express end devices.

#### 1.1. PI7C9X2G304SL Features

- 4-lane PCI Express Gen 2 Switch with 3 PCI Express ports
- Supports "Cut-through" (Default) as well as "Store and Forward" mode for packet switching
- Peer-to-peer switching between any two downstream ports
- 150 ns typical latency for packet routed through Switch without blocking
- Integrated reference clock for downstream ports
- Strapped pins configurable with optional EEPROM or SMBus
- SMBus interface support
- Compliant with System Management (SM) Bus, Version 1.0
- Compliant with PCI Express Base Specification Revision 2.1
- Compliant with PCI Express CEM Specification Revision 2.0
- Compliant with PCI-to-PCI Bridge Architecture Specification Revision 1.2
- Compliant with Advanced Configuration Power Interface (ACPI) Specification
- Advanced Power Saving
- Supports Isochronous Traffic
- Supports up to 512-byte maximum payload size
- Programmable driver current and de-emphasis level at each individual port
- Support Access Control Service (ACS) for peer-to-peer traffic
- Support Address Translation (AT) packet for SR-IOV application
- Support OBFF and LTR
- Low Power Dissipation: 650 mW typical in L0 normal mode
- Industrial Temperature Range -40° to 85°C
- 128-pin LQFP 14mm x 14mm package

#### 1.2. PI7C9X2G304SL Evaluation board Features

- PI7C9X2G304SL in 128-pin LQFP 14mm x 14mm package
- Supports one x1 or x2 upstream PCI Express port
- Supports two x1 downstream PCI Express slot connectors
- Manual push-button MREST# capability
- LED indicators for visual inspection
- Uses ATX hard disk power connector to supply power to the packet switch and the connected add-in cards



# 1.3. Evaluation board Front View

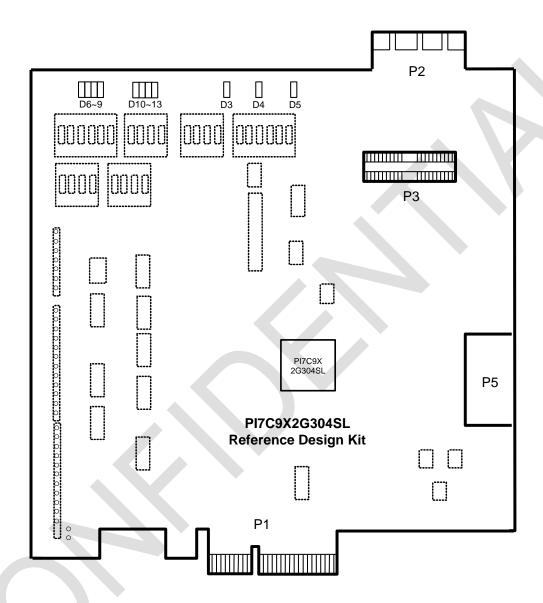
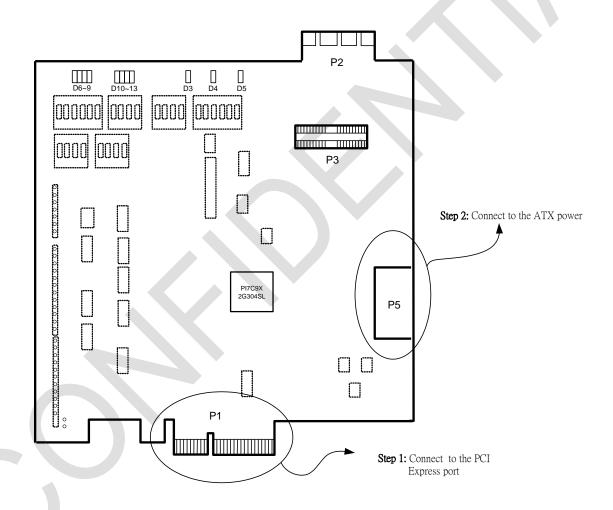


Figure 1-1 PI7C9X2G304SL Evaluation board Front View



# 2. Initial Setup

- Step 1. Connect the upstream PCI Express connector (P1) of the Evaluation board to the PCI Express slot on the Root Complex. The Evaluation board should be connected to the Root Complex before it is connected to the ATX power.
- Step 2. Connect the ATX power cord from an external power source to the ATX power connector of the Evaluation board. The Evaluation board does not get its power from the PCI Express slot, and it requires external ATX power to function.





### 3. On-Board LED Indicators and Connectors

#### 3.1. LED Indicators

The Evaluation board provides a number of LED indicators to conveniently display the status of the output signals. The name and function of each of the indicator is listed and explained in the table below.

**Table 3-1 LED Indicator Description** 

LED Location	Name	Function	Description
D3	3.3VAUX	3.3V Auxiliary Power	Indicates the status of the 3.3V auxiliary power supply. The indicator is active-high.
D4	12VCC_EXT	12V Power	Indicates the status of the 12V external power supply. The indicator is active-high.
D5	3.3V_EXT	3.3V Power	Indicates the status of the 3.3V external power supply. The indicator is active-high.
D6 to D9	LANEACT0 to LANEACT3	Reserved	
D10 to D13	L3_BIST_ERR to L0_BIST_ERR	Reserved	



#### 3.2. Connector Ports and Power Connector

The Evaluation board provides two downstream PCI Express ports to enable connections to various end devices. The Evaluation board uses an ATX hard disk power connector to supply power to the packet switch and the connected add-in cards

**Table 3-2 Connector Port Function** 

Port	Function
P1	x1 or x2 upstream PCI Express port.
	Connects to the Root Complex
P2	x1 downstream PCI Express port1.
	Connects to a PCI Express end device
P3	x1 downstream PCI Express port2.
	Connects to a PCI Express end device
P5	ATX hard disk power connector