PI7C9X2G404SL / PI7C9X2G304SL / PI7C9X2G404EL / PI7C9X2G304EL / PI7C9X2G303EL
SlimLine™ / UltraLo™ PCI Express® Gen2 Packet Switch Guidelines

1. Introduction
This application note provides a concise and practical guide for the board designers to easily incorporate the Pericom SlimLine / UltraLo PCI Express Gen2 Packet Switches in their designs. This document includes design outlines, layout cautions and application reminders, which can help the designers to achieve optimal performance in their systems.

2. Differential Impedance
For microstrip traces, an impedance target of 85Ω with a max 20% impedance tolerance is desired for 6-layer printed circuit board stackups.
For stripline traces, an impedance target of 85Ω with a max 15% impedance tolerance is desired for 6-layer printed circuit board stackups.

3. Single-Ended Impedance
For microstrip traces, an impedance target of 50Ω with a max 15% impedance tolerance is desired for 6-layer printed circuit board stackups.
For stripline traces, an impedance target of 50Ω with a max 15% impedance tolerance is desired for 6-layer printed circuit board stackups.

4. Differential Pair Length Restrictions
Trace routing lengths from a chipset to a connector (microstrip and stripline) are limited to 5 inches.

5. Stitching Via
When traces change layers, stitching vias must be used. Stitching vias should be placed as close as possible to the differential pair signal vias (<=100mils).

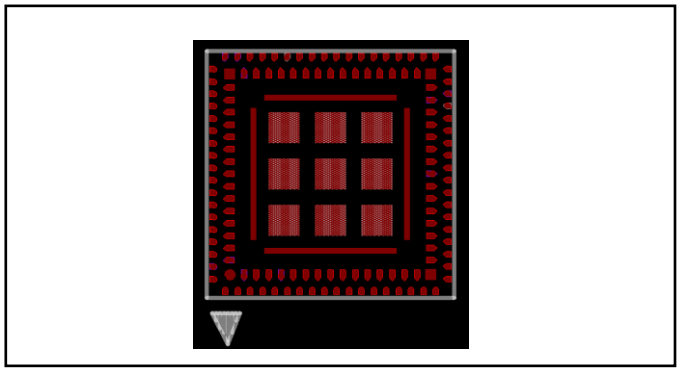
6. Edge Finger Design
The reference planes on the inner layers should be removed immediately under the gold finger areas that exist on the outer layers of the PCB. The planes should be removed along the entire length of the edge finger component that contains PCI Express differential pair signal traces. This removal of the reference planes should be restricted to the actual area of the edge fingers only and not extend out to the trace routing area.

7. Via Usage
A maximum of Zero (0) via pair may be used on each TX differential pair of a system board.
A maximum of two (2) via pairs may be used on each RX differential pair of a system board.

8. Capacity Effect Removal
The reference planes on the inner layers should be removed immediately under the chip pin, AC capacitor and slot solder spots along the differential pair signal traces.

9. aQFN Center Metal Pad Layout Guidelines
The aQFN package (used by PI7C9X2G404EL/ 304EL/ 303EL) has a center metal pad on the underside of the part, typically for grounding and heat conduction. It's this center metal pad that makes this form factor so difficult to use.

This is an example of recommended practice. The basic idea is to have a lower quantity of solder over a broader area. This reduces thickness in the center and other problems associated with large paste, such as outgassing and spattering. This will give good solder distribution and avoid high-centering or outgassing problems.



Note: This illustration refers to the aQFN package of PI7C9X2G404EL/ 304EL/ 303EL.

10. Differential Signal (Tx/Rx) Layout Guidelines
PCI Express is a dual simplex point-to-point serial differential low-voltage interconnect. The bit rate is 2.5 G bit/sec/lane/direction at introduction. The signal is

8b/10b encoded with an embedded clock. Each lane consists of two pairs of differential signals. Differential trace impedance target of 100Ohm with a tolerance of 15% or better is desired. Tight coupling within the differential pair and increased spacing to other differential pairs helps to minimize crosstalk and EMI. If possible, Tx and Rx differential pairs should route alternately on the same layer (Tx pair next to a Rx pair rather than another Tx pair) to help minimize FEXT.

AC coupling capacitors of 100 nF should be placed at the same location (as close as possible) and should not be staggered from one trace to the other within the pair. While size 0603 capacitors are acceptable, size 0402 capacitors are strongly encouraged. C-packs are not allowed for AC coupling capacitors. The exact same package size of capacitor should be used for each signal in a differential pair. Pad sizes for each of the capacitors should be minimized. The “breakout” into and out of the capacitors should be symmetrical for both signal traces in a differential pair.

From our experience, the high-speed transmission line design is very important and a good transmission line design is a critical factor to achieve good signal quality. If the PCB design can be further improved, especially the traces of the TX and RX of the PCIe lanes, and the reference clock, the overall system stability should be improved.

Breakout Areas near a device package that resulted in “neck-downs” and decreased spacing should be limited to no more than 500 mils in lengths. The necking-down should be done symmetrically on both nets of the differential pair. Breakout sections require special attention to minimize crosstalk.

Test points and probing structures may impact the loss and jitter budgets. If possible, test points and probe structures should not introduce stubs on the differential pairs.

11. Reference Clock Input Pairs

The reference clock input pins connect to external 100MHz differential clock. The signal must match to LVPECL or HCSL spec.

A 100nF capacitor should be placed between the clock source and the packet switch. The purpose of this capacitor is to achieve AC coupling. This AC Coupling ensures the Packet Switch is compatible with the differential clock signals regardless the type of the clock. The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered.

12. VGA Support

The SlimLine / UltraLo packet switches support VGA function in all downstream ports. If the system needs to support a VGA chip, The VGA Enable bit in the Bridge Control register (offset 3Ch) is used to control the behaviors to both the VGA frame buffer addresses and to the VGA register addresses. When a VGA compatible device is located at downstream port of the packet switch, the VGA Enable bit must be set. When set, the packet switch will positively decode and forward memory accesses to VGA frame buffer addresses and I/O accesses to VGA registers from the upstream port to the downstream port and block forwarding of these same accesses from the downstream port to the upstream port.

The packet switches implements VGA Enable bit in the Bridge Control register as read-write bit for Port 1 and Port 2.

13. GPIO Control

The SlimLine / UltraLo packet switch provides GPIO pins, which can be programmed as either input or output pins through configuration registers. The user has the ability to monitor the input/output status or control the output signals by reading or writing the corresponding GPIO registers. After the packet switch is powered up, the GPIO pins are set to be input pins by default. Following is a block diagram for illustrating the GPIO pins and the associated control registers.

13.1. Output Operation

For GPIO to act as output pins, the user has to make sure the bus is in tri-state (no other master is driving it) before enabling the output buffer to avoid any possible bus contentions. First, the user puts the desired output status in the GPIO output register, and then sets low to the GPIO O/P enable register. So the output signal will be observed in the GPIO pins immediately.

13.2. Input Operation

To check the input/output status of GPIO pin, the output buffer has to be turned off by setting high to the GPIO Output Enable Register. This will prevent the signal driving by the chip from being read back. After disabling the output buffer, any signal status change in the GPIO pin will be reflected in the input bits of GPIO

registers. The values can be captured through Configuration Read Command.

13.3. Example

1) To program GPIO as output pin and drive high off the chip
  Step 1: Write "1" into GPIO output bit of register, which is at D8H
  Step 2: Write "1" into GPIO output enable bit of register, which is at D8H
2) To program GPIO as input pin
  Step 1: Write "0" into GPIO output enable bit of register, which is at D8H
  Step 2: Read value from GPIO input bit of register, which is at D8H

14. SM-BUS

The SlimLine / UltraLo packet switches support the SMBus function. The SMBus address can be configured by GPIO[5:6:7]. The address is 1101XXX_b. Bit 0 is used to indicate R/W. Bit 1, 2, and 3 corresponds to GPIO[5], GPIO[6], and GPIO[7]. The Packet Switch supports only the Host Command (08H/03H). The 03H command is only used to terminate the command that is currently being executed.
Host command 08H used in Read or Write.

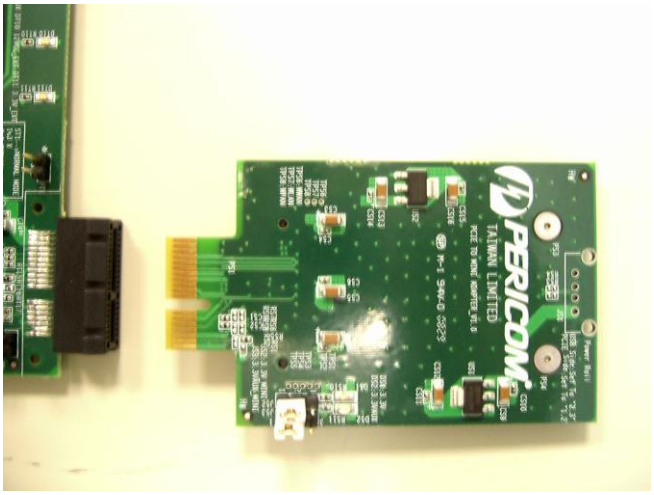
To complete a single SMBus read/write operation, two separate SMBus commands must be issued separately in two cycles. The low byte of the first command represents register offset. The high byte represents the port number. The second command represents the data used for the operation.

15. PRSNTx# Pin

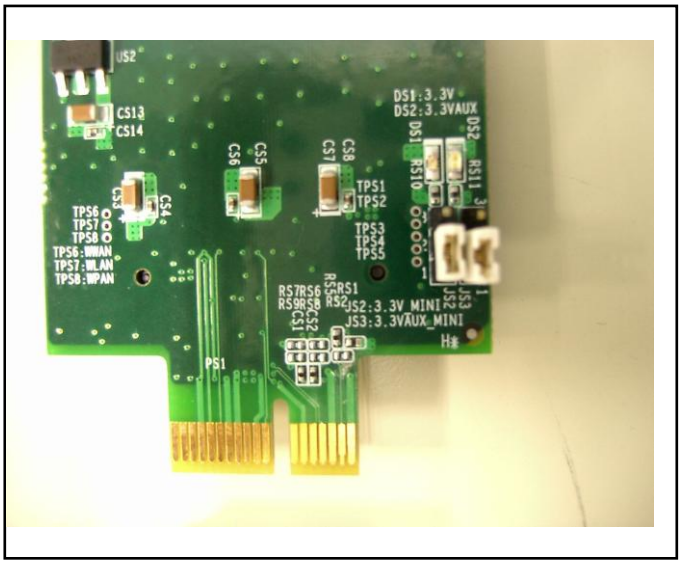
When the SlimLine / UltraLo packet switches are connected to slots, the PRSNTx# pins must be connected to the slots' PRSNT# pins and pull-up resisters of 5.1K ohm, so that the presence of the cards can be detected. When slot is empty, the power saving function is enabled.
If the packet switch is used without the slot, the **PRSNTx# must be pulled low** with a 1K ohm resistor. In this case, power saving is never enabled.

16. PCI Express to Mini PCI Express Adaptor

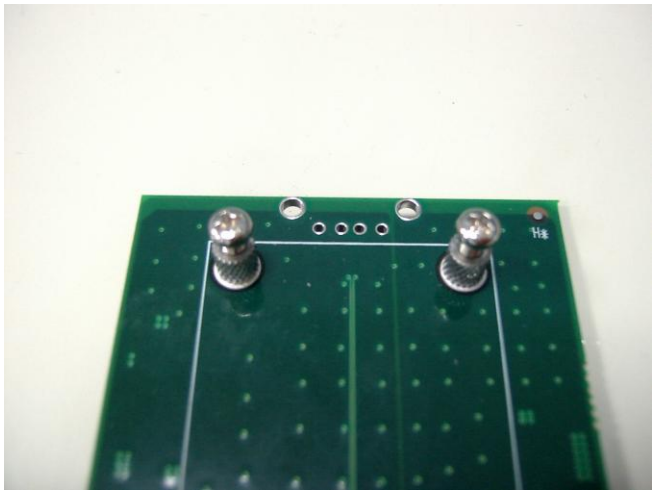
The evaluation board may come with an optional PCI Express to Mini PCI Express adaptor to facilitate the testing of an endpoint device in PCI Express Mini Card form factor. The following instruction describes how to connect such device to the adaptor and the adaptor to the evaluation board.



PCI Express to Mini PCI Express Adaptor

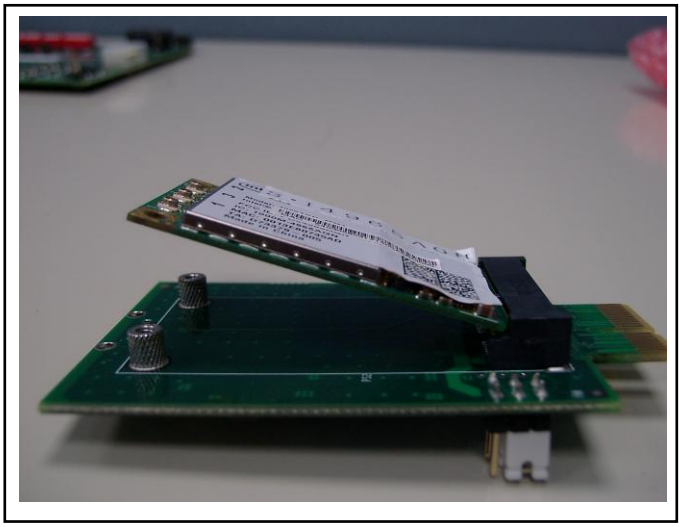


Step 1: Make sure jumpers JS2 and JS3 are set properly: jumper pin 2 and pin 3 should be strapped.

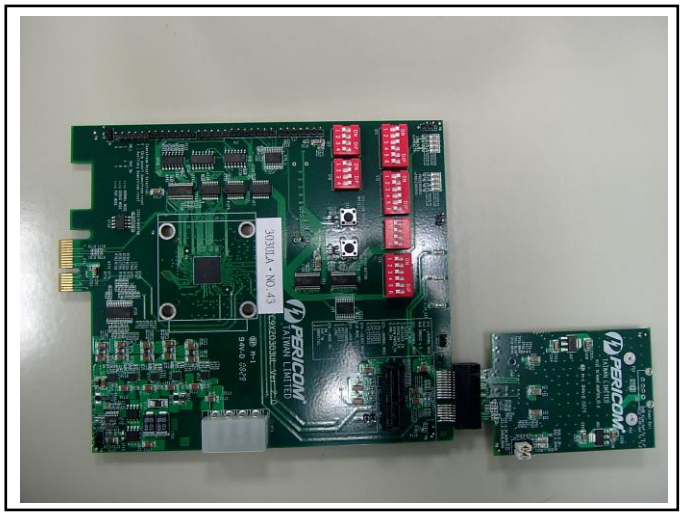


Step 2: Remove the screws on the front side of the adaptor.

Step 4: Fasten the screws and secure the Mini PCI Express Card device.



Step 3: Insert a Mini PCI Express Card device.



Step 5: Plug the adaptor to the evaluation board's downstream port.