Post lab 6. Please answer the following questions about the ADC and DAC, and submit your source code.

1. Consider a system where the DAC is updated every 4us (250 kHz) with a value from a 200-element wave table containing a single cycle of a waveform. What would be the frequency of the output wave?

In order to complete the waveform we would nee 200 samples per cycle. This results in 250 kHz/200 samples which gives us a frequency of 1250 Hz or 1.25 KHz.

2. Consider that the ADC in 12-bit mode divides the input voltage range (0-3V) into 4096 steps (where 0V is 0, and 3V is 4095).
    a. What is the voltage/measurement resolution (how much does the voltage change per bit) of the ADC?

Resolution is calculated using voltage range / steps so we would have 3/4096 which gives us a resolution of 0.0007324 V/step.

    b. What would be the ADC output value (nearest integer) if the input voltage was 1.75V?

The ADC output value would be 1.75/0.0007324 which gives us a value of 2387.