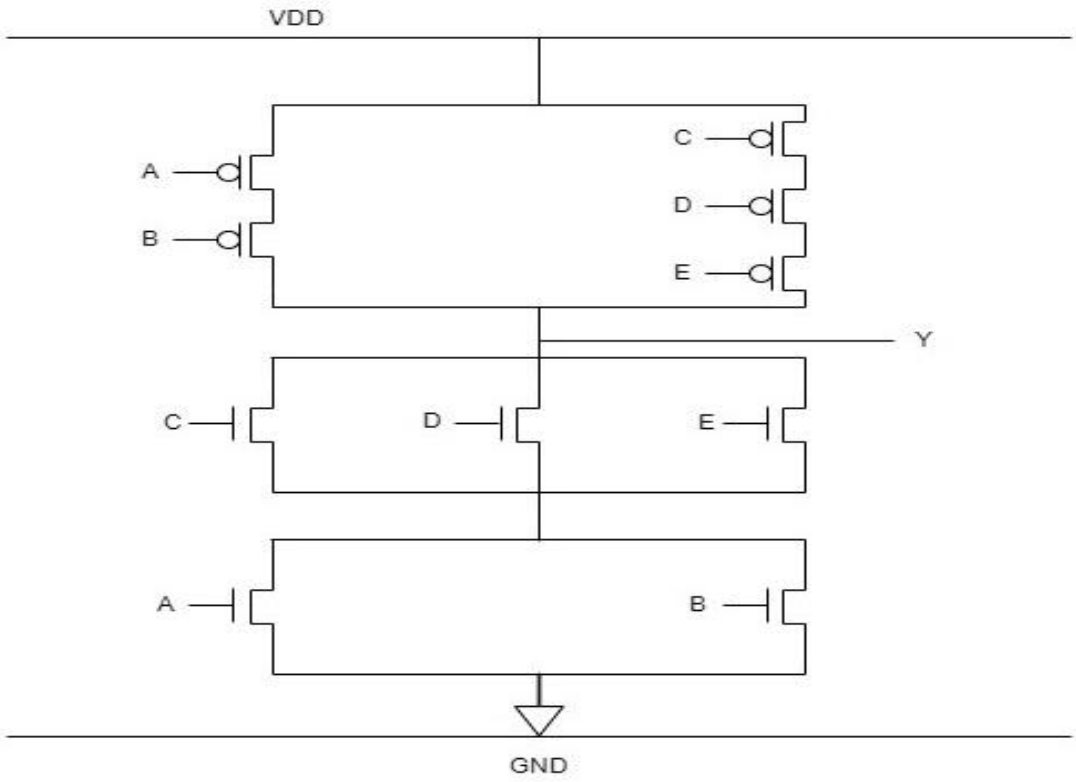
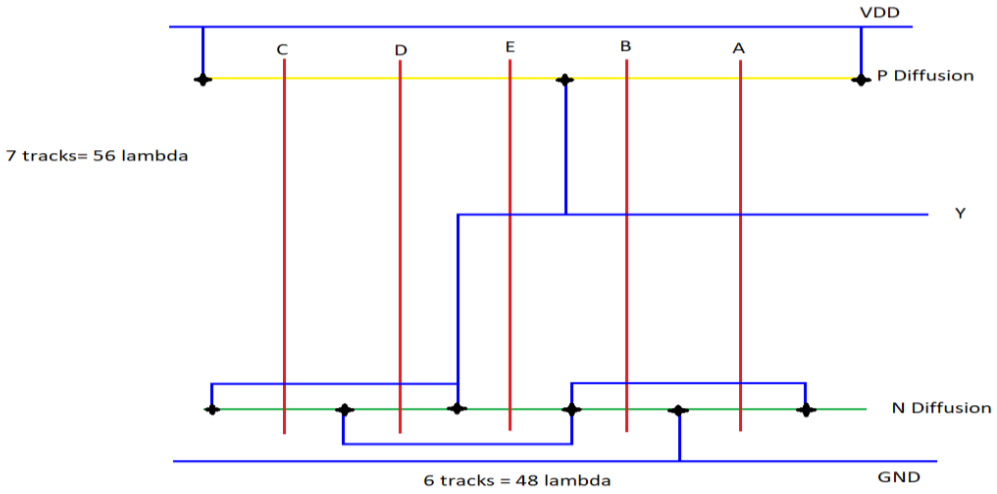
Assignment-1

Given 5 input function: $\overline{(A+B)(C+D+E)}$

Transistor level CMOS logic diagram:



Stick Diagram with area estimation:



Total estimated area:

Vertically 7 tracks = 7 X 8 λ =56 λ

Horizontally 7 tracks = 6 X 8 λ =48 λ

Total area =56 λ X 48 λ

Gate level module:

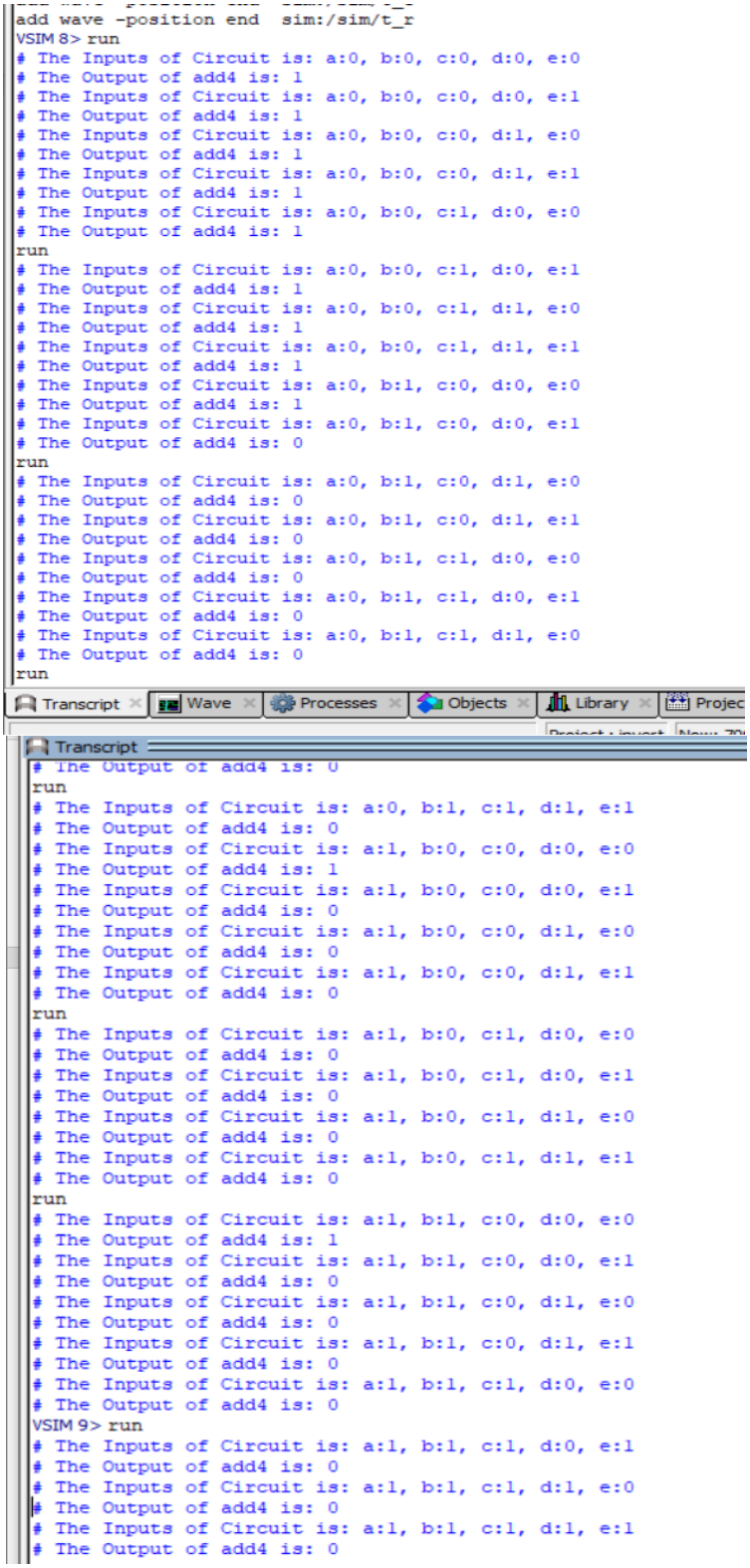
```
module invert(a,b,c,d,e,r);
input a,b,c,d,e;
output r;
wire p,q;
or (p,a,b);
or (q,c,d,e);
nand(r,p,q);
endmodule
```

Transistor level module:

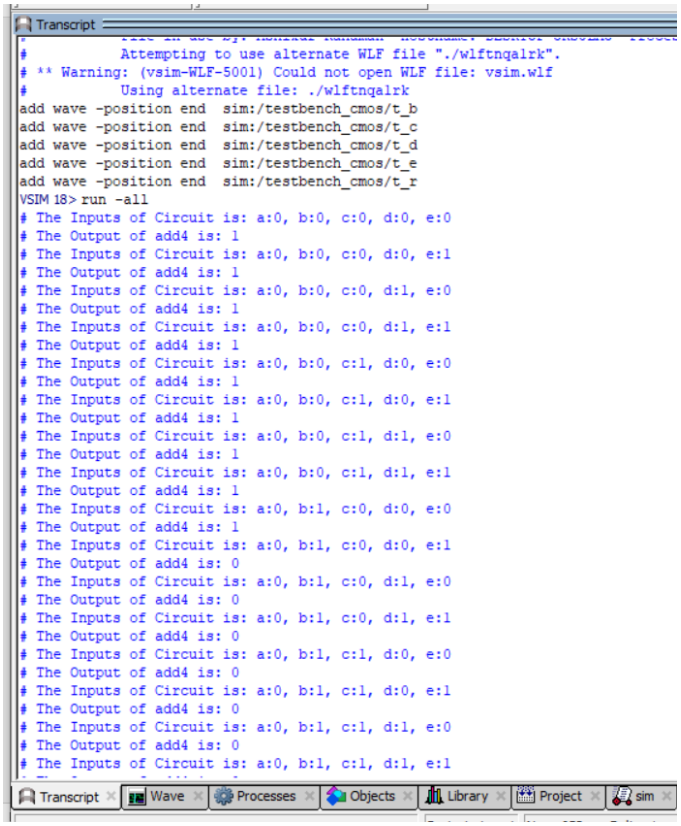
```
module transistor_level(a,b,c,d,e,out);
input a,b,c,d,e;
output out;
wire PD1,PD2,PD3,ND1,out;

pmos ( PD1, 1, a);
pmos ( out, PD1, b);
pmos ( PD2, 1, c);
pmos ( PD3, PD2, d);
pmos ( out, PD3, e);

nmos ( out, ND1, c);
nmos ( out, ND1, d);
nmos ( out, ND1, e);
nmos ( ND1, 0, a);
nmos ( ND1, 0, b);
endmodule
```

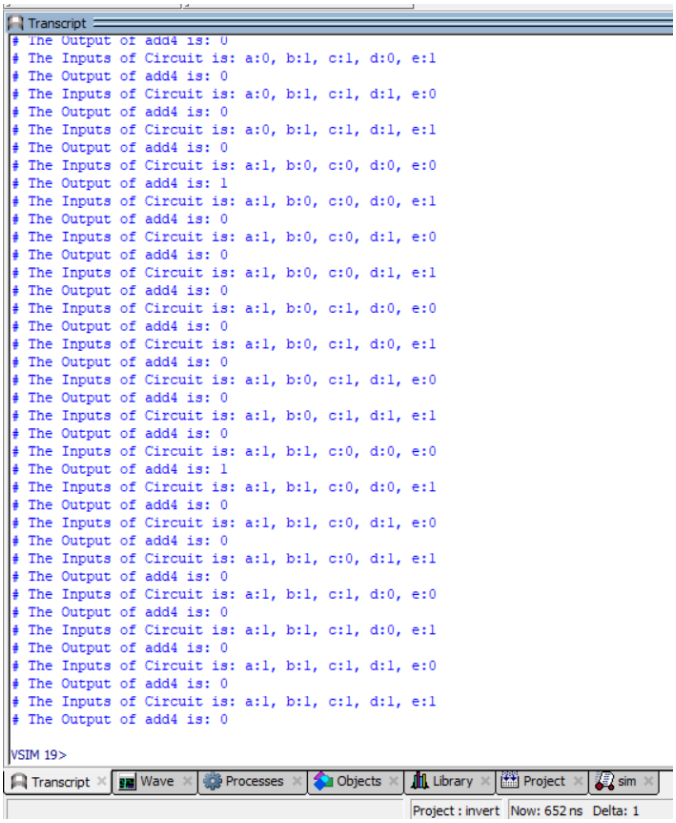
Questa output for all 32 possible combinations (for gate level and transistor level the outputs are same)

Gate level:

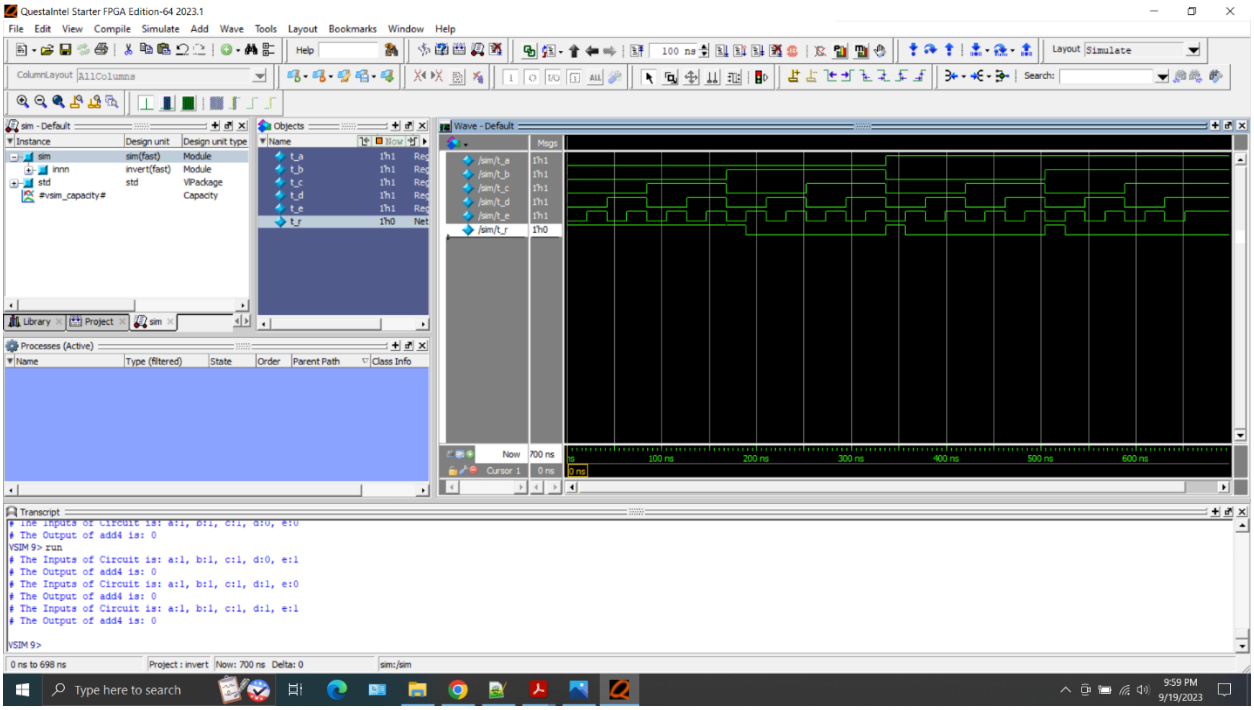


Transistor level:





Wave form of gate level:



Wave form of transistor level: