School of Computing and Informatics

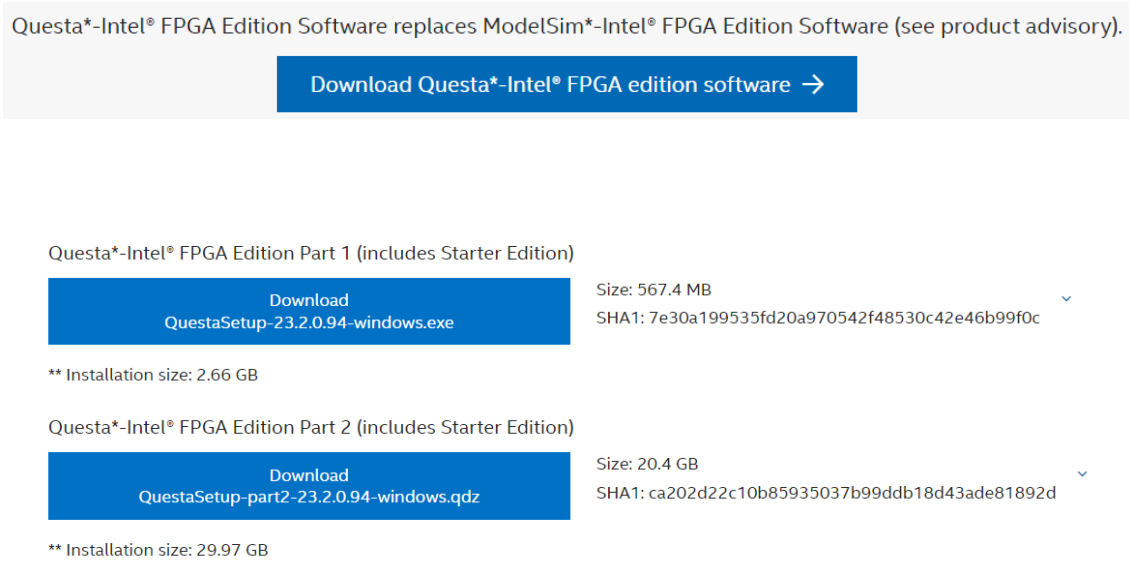
CSCE 585 – VLSI Design – Fall 2023

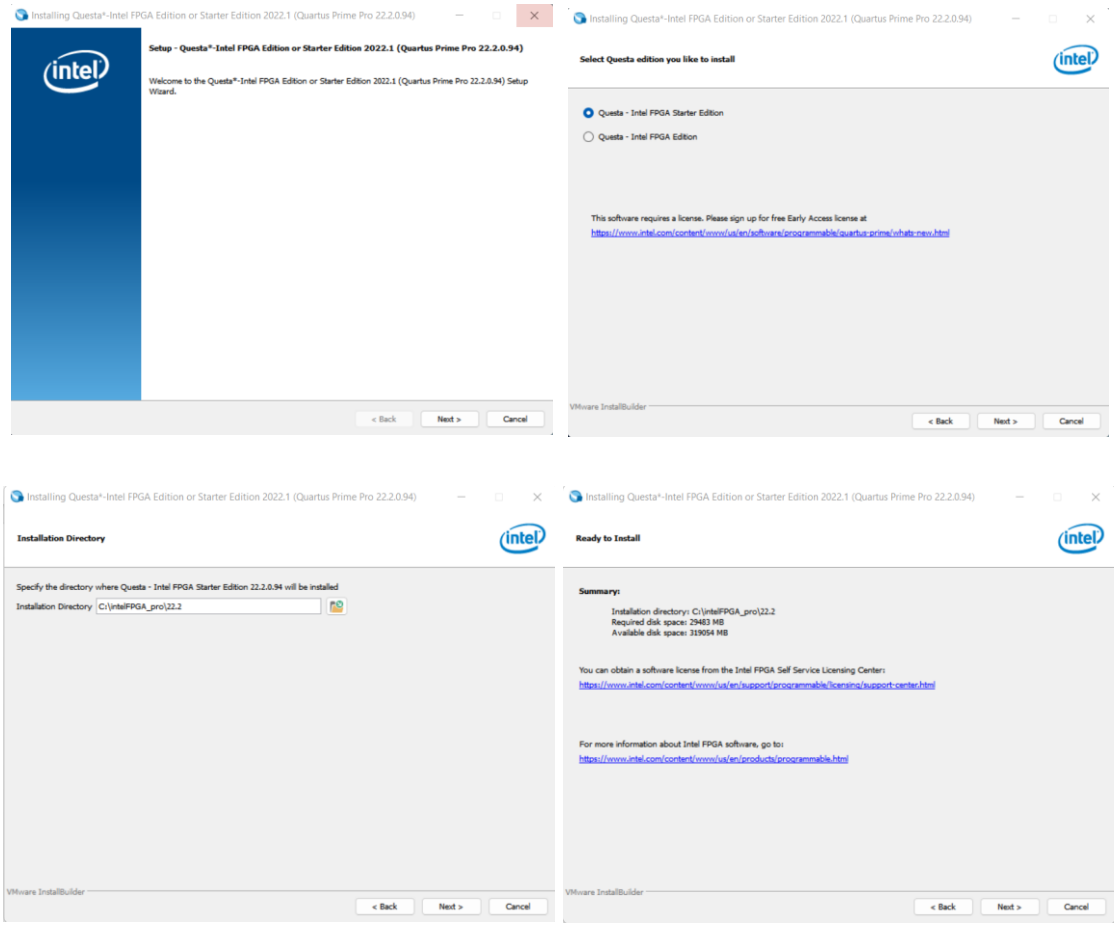
Computer Assignment 1

In this assignment, you will get familiar with Verilog coding and HDL simulation using Siemens EDA Questa (Modelsim). You start by installing/running Questa, writing an HDL code, and simulating the hardware description of a simple function. You then receive the RTL design of a simple MIPS processor and modify its arithmetic and logic unit (ALU) to add a new instruction.

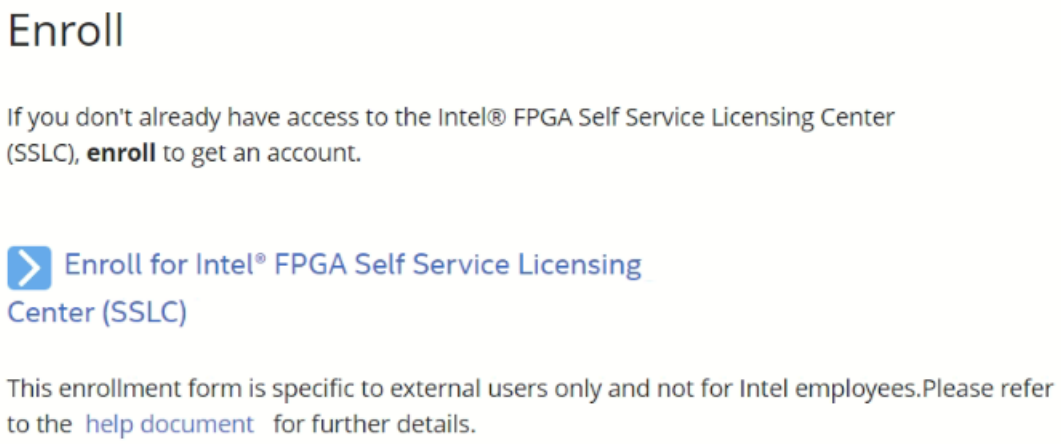
a) Download and install the **free starter edition of Questa** from Intel website:

https://www.intel.com/content/www/us/en/software/programmable/quartus-prime/questa-edition.html





Obtain a free starter license from:
https://fpgasupport.intel.com/Licensing/license/index.html



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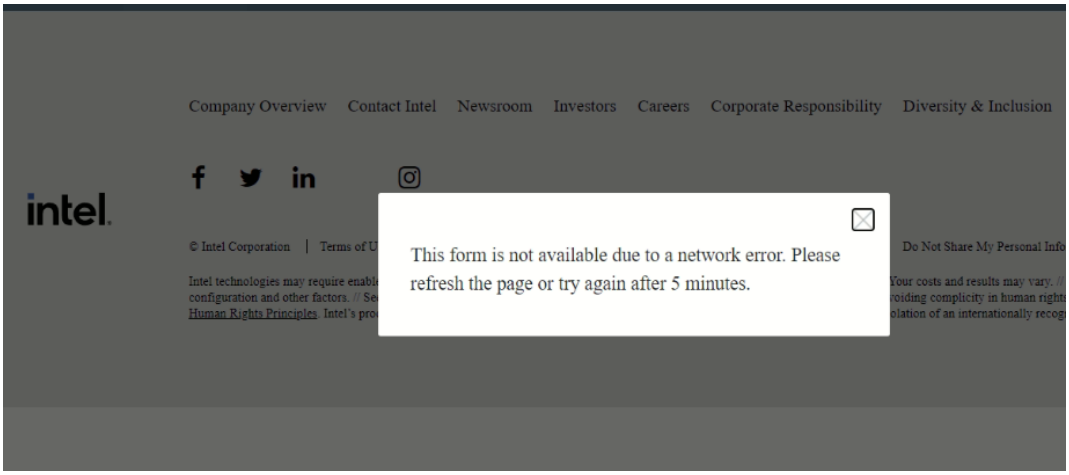
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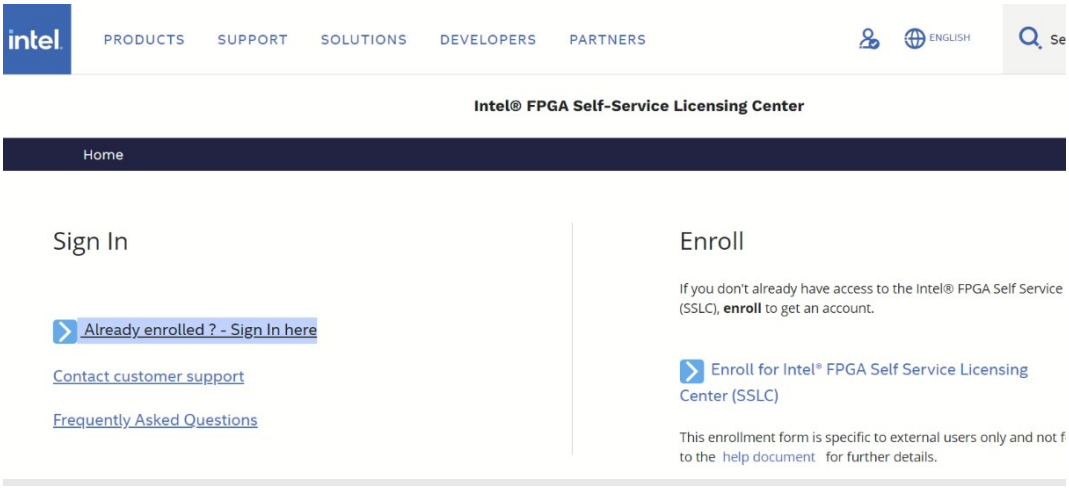
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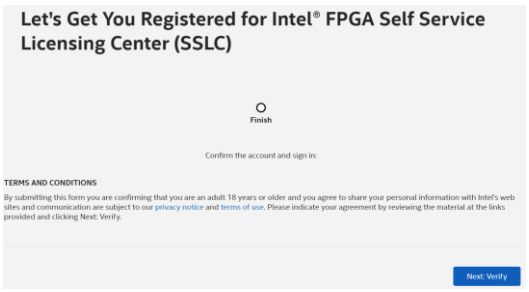
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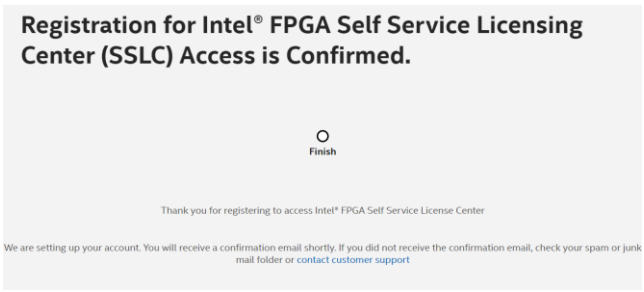
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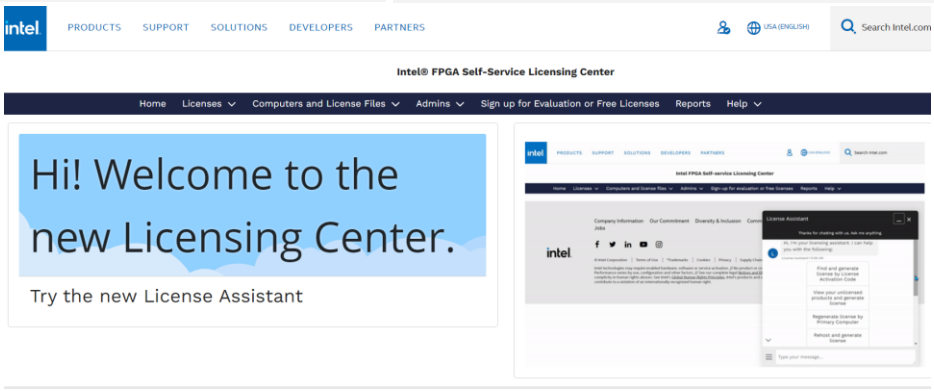
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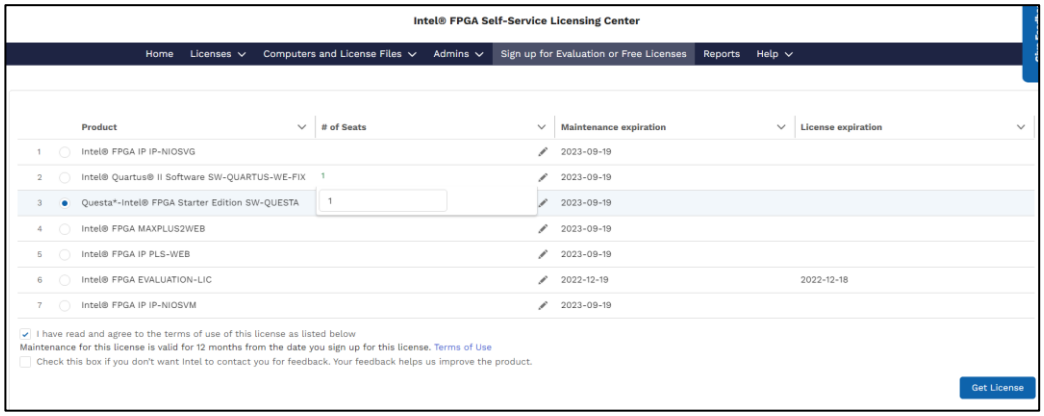
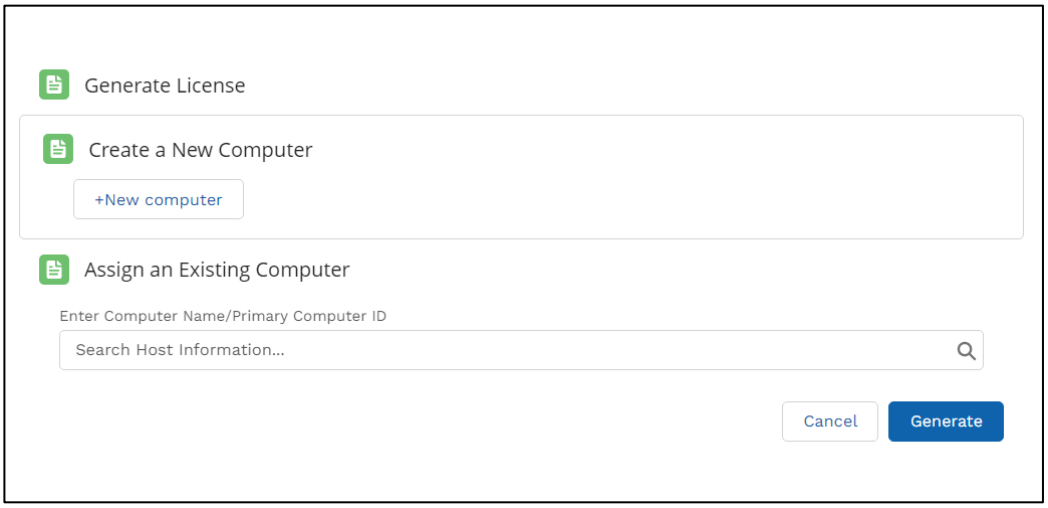
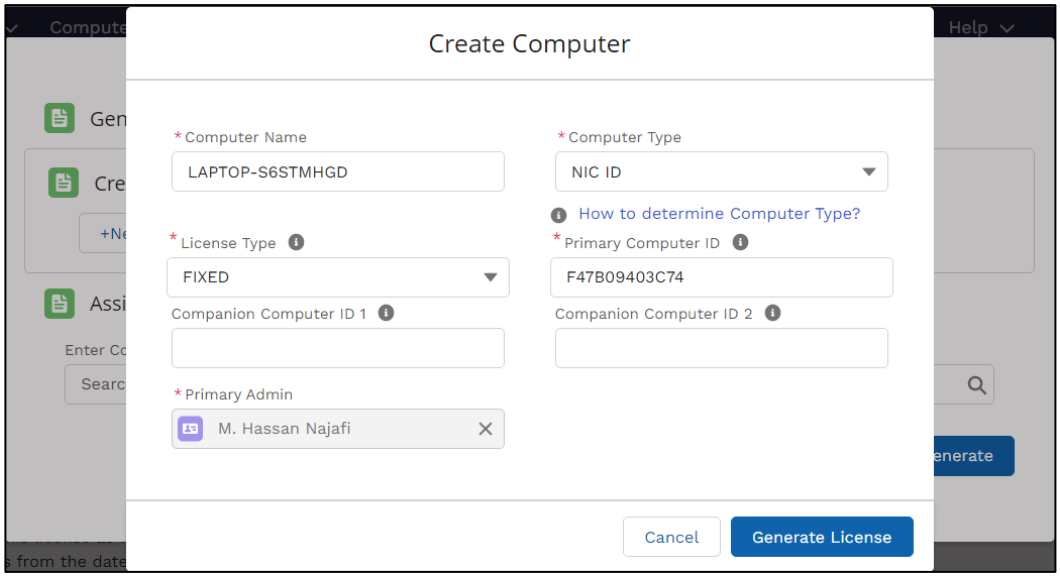
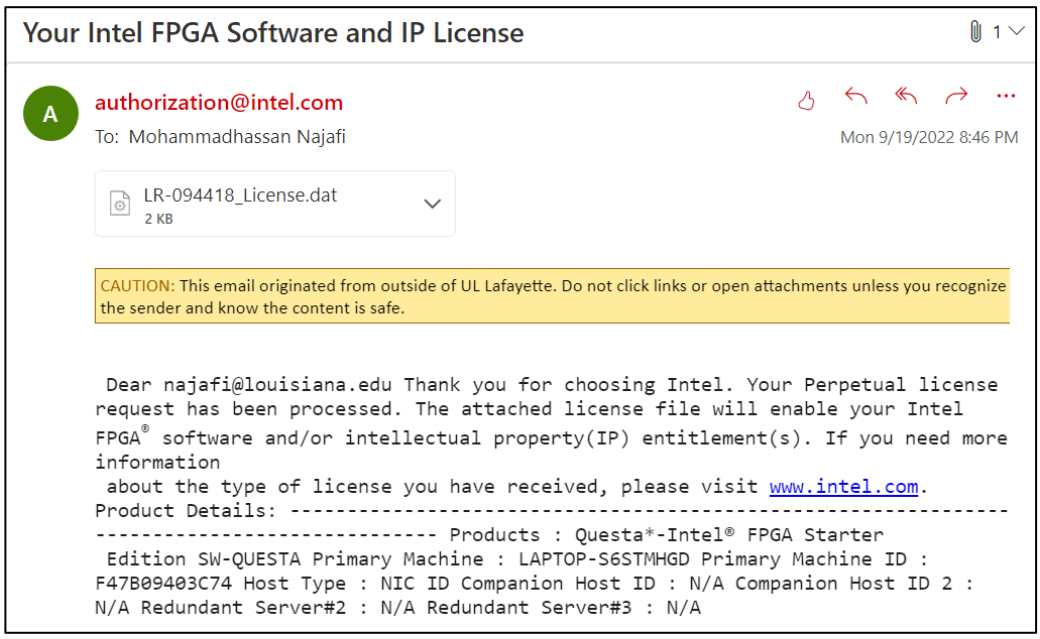






Your network interface card (NIC) ID can be found by “ipconfig /all” in command prompt.



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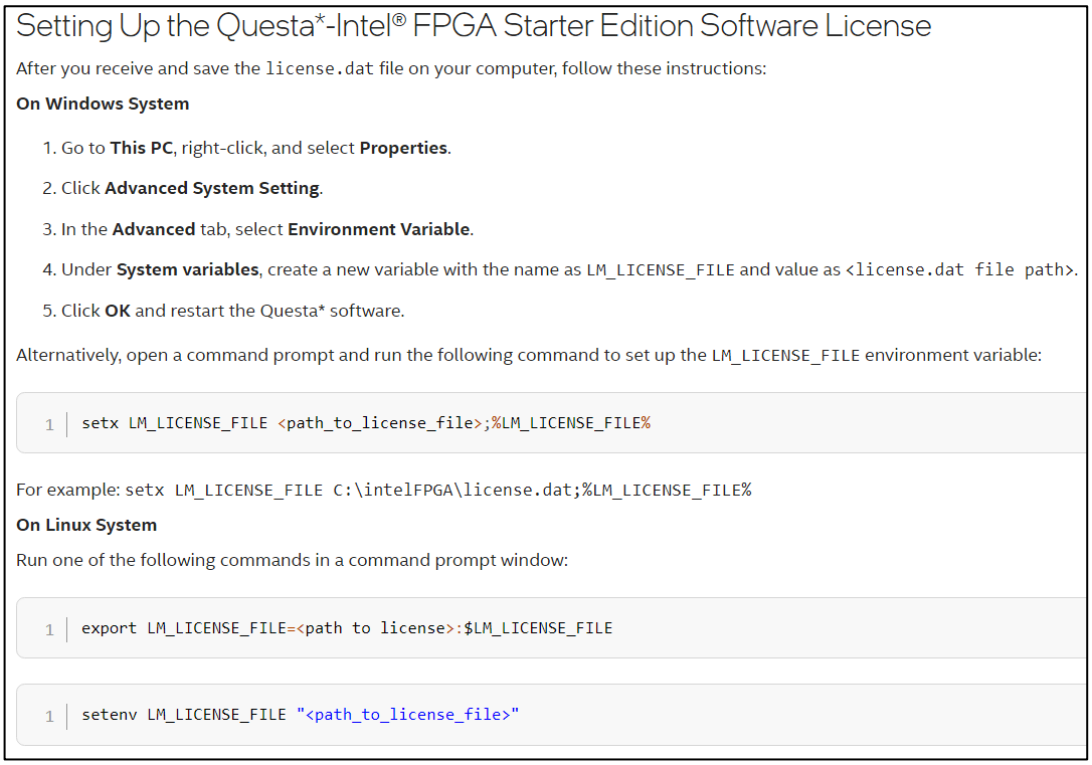
Download your license to your Questa installation folder and add its address to your system variables as a LM_LICENSE_FILE variable:

https://www.intel.com/content/www/us/en/docs/programmable/683472/22-1/and-software-license.html



Setting Up the Questa*-Intel® FPGA Starter Edition Software License

After you receive and save the `license.dat` file on your computer, follow these instructions:

On Windows System

1. Go to **This PC**, right-click, and select **Properties**.
2. Click **Advanced System Setting**.
3. In the **Advanced** tab, select **Environment Variable**.
4. Under **System variables**, create a new variable with the name as `LM_LICENSE_FILE` and value as `<license.dat file path>`.
5. Click **OK** and restart the Questa* software.

Alternatively, open a command prompt and run the following command to set up the `LM_LICENSE_FILE` environment variable:

```
1 | setx LM_LICENSE_FILE <path_to_license_file>;%LM_LICENSE_FILE%
```

For example: `setx LM_LICENSE_FILE C:\intelFPGA\license.dat;%LM_LICENSE_FILE%`

On Linux System

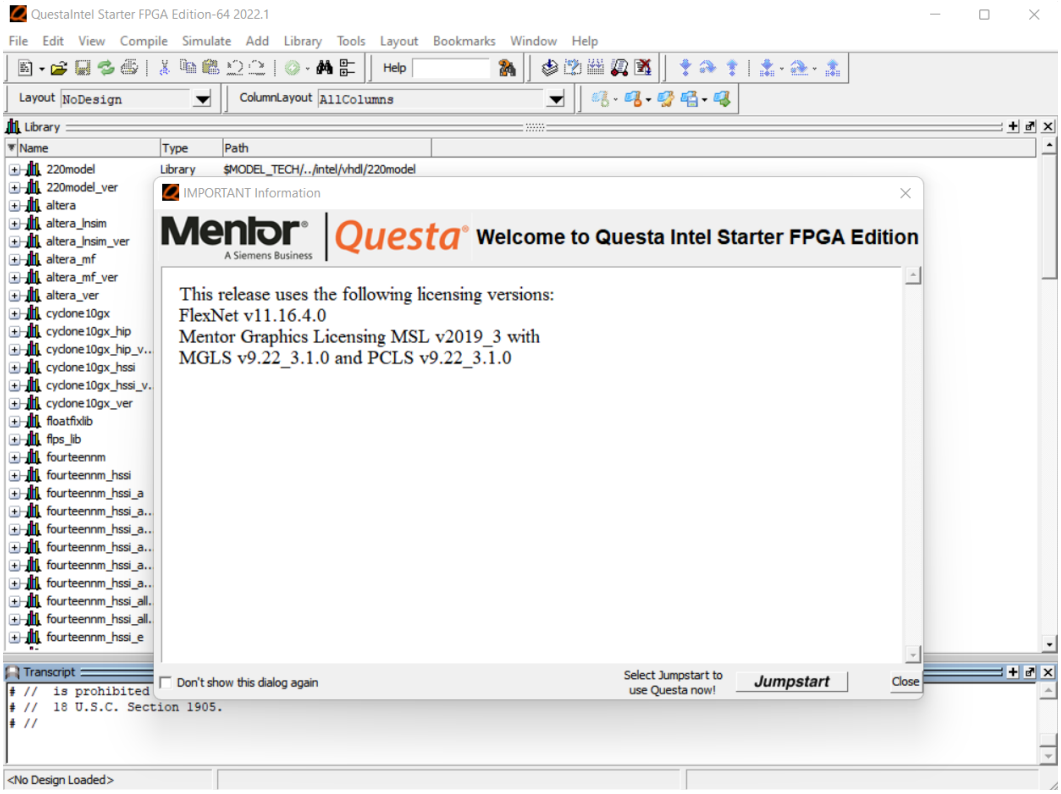
Run one of the following commands in a command prompt window:

```
1 | export LM_LICENSE_FILE=<path to license>:$LM_LICENSE_FILE
```

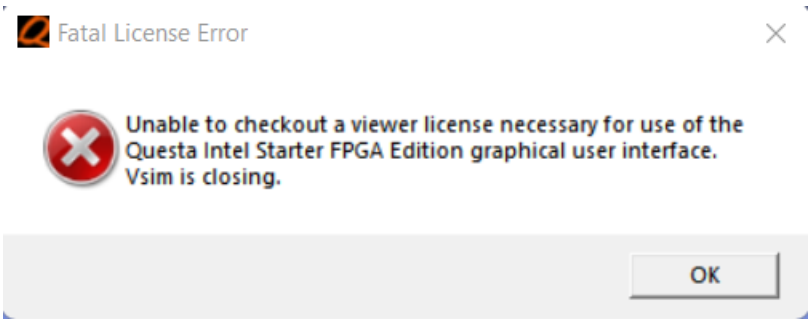
```
1 | setenv LM_LICENSE_FILE "<path_to_license_file>"
```

Confirm Questa and its license are installed correctly by running vsim.exe:

C:\intelFPGA_pro\23.2\questa_fse\win64\vsim.exe



- Note that by requesting "1 license seat" you can only run <u>one Questa window</u>. So, make sure you close the previous Questa window before running a new one to prevent the following error:



b) You can also use the **Windows machines in the SWAMP lab** (3rd floor – Oliver Hall) to run Questa if you don't have a Windows system or enough space on your computer.

Let the instructor know <u>by Sep 15</u> if you have any issue in installing or running Questa.

c) Install **Notepad++** or another editor for editing your Verilog codes.

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1. A) Sketch a **transistor-level schematic** for a CMOS logic gate implementing the following 5-input function: $\boldsymbol{Y = \overline{(A + B) \cdot (C + D + E)}}$. Sketch a stick diagram for the function. Estimate the area from the stick diagram (consider a length of $8\boldsymbol{\lambda}$ for each wire track).

   B) Write a **gate level** and a **transistor-level** Verilog module for this function. Verify correct functionality of the two implemented modules (Gate-level and Transistor-level) for **all 32 possible combinations** of the inputs with a **testbench** and **HDL simulation** using Questa. <u>Put your modules, testbench, Questa log output, and a screenshot of the Questa wave output in a separate folder.</u>

2. In class, we discussed the functionality of a simple **MIPS** processor and described the implemented instructions inside its ALU. Now we want to modify the arithmetic unit of the simple MIPS processor and add another instruction. We add the **XOR** instruction to the ALU of the processor (for this you need to modify ALU to add one new opcode [*just modify **alu** and **alucontrol** modules in the mips.v file*] to be able to execute programs including XOR instruction). Simulate the modified design with Questa and verify the functionally of processor. Automatic simulation and verification with the TCL script that we saw in the class can help you with fast simulation using Questa.

XOR -- *Bitwise exclusive or*

Description:	Exclusive ors two registers and stores the result in a register
Operation:	$d = $s ^ $t; advance_pc (4);
Syntax:	xor $d, $s, $t
Encoding:	`0000 00ss ssst tttt dddd d--- --10 0110`

As can be seen in *mipstest.v* and *mipstest_xor.v* testbench files, to verify correct functionality of the MIPS processor, the data at address **EE** of memory after running the original Fibonacci program (*fib.dat*) must be **8'h0D** and after running the modified Fibonacci program (*fib_xor.dat*) which includes an XOR instruction must be **8'hF2**.

Please put the following files in a separate folder:

1. Upload you MIPS project folder. This should include your modified *mips.v* file which supports XOR instruction (name the new modified file *mips_xor.v*)

2. Catch the moment that the output of the program is written at memory address 238 (or 8'hEE) in Questa wave window (hint: you can track /top/dut/memwrite signal). Verify that the "writedata" signal has the expected output (8'h0D or 8'hf2). Take two screenshots from the wave window of Questa, one for the original operation of MIPS with *fib.dat* and the other for the modified MIPS with *fib_xor.dat*.

4. Upload your results on Moodle as *LASTNAME_ULID.zip*