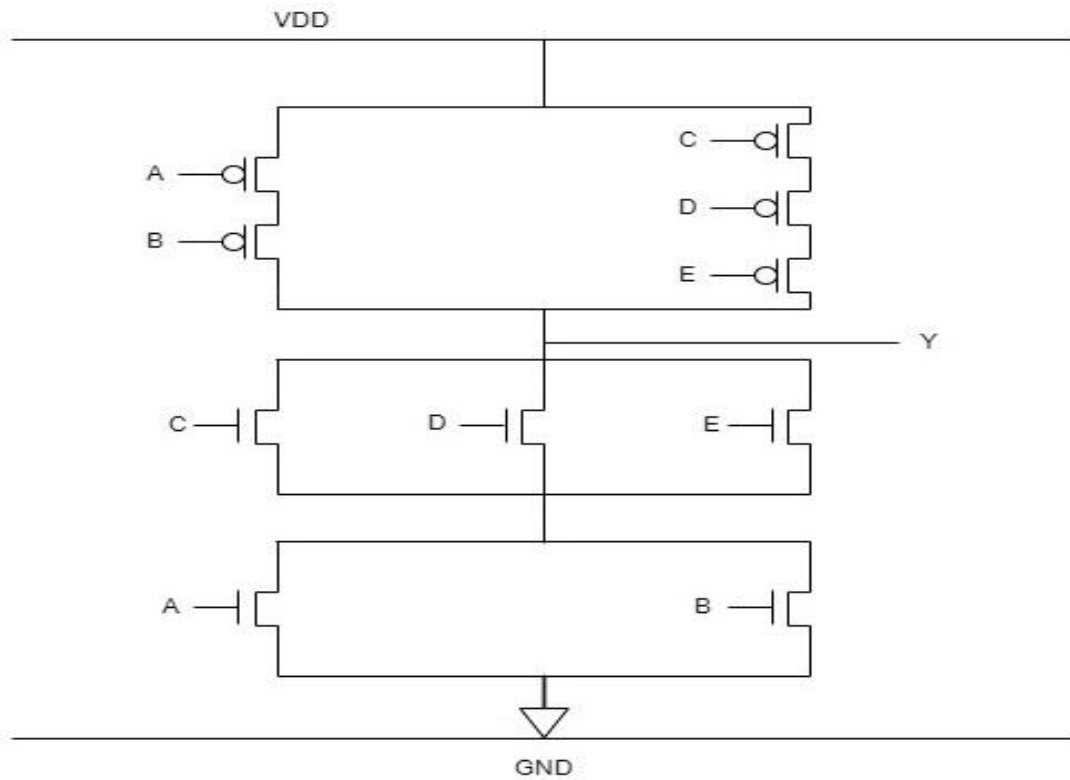


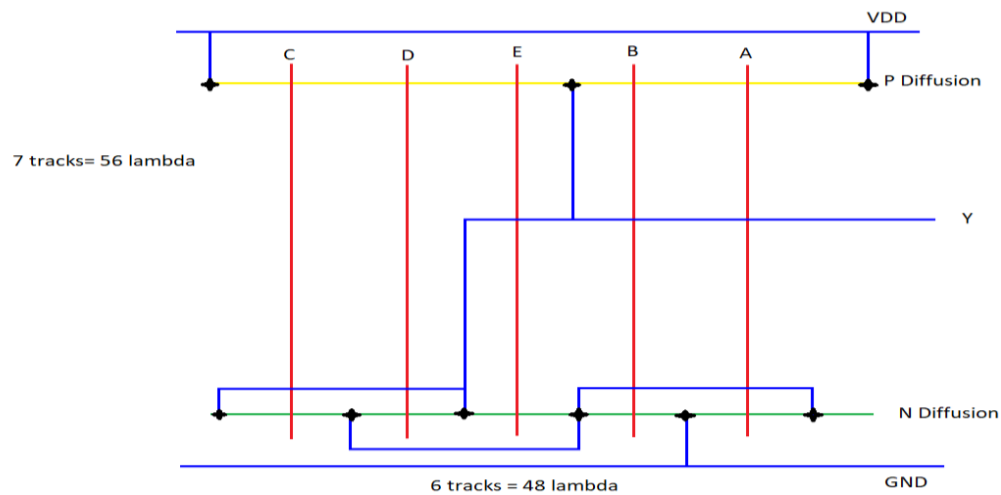
## Assignment-1

Given 5 input function:  $\overline{(A + B)(C + D + E)}$

Transistor level CMOS logic diagram:



Stick Diagram with area estimation:



Total estimated area:

Vertically 7 tracks =  $7 \times 8 \lambda = 56 \lambda$

Horizontally 7 tracks =  $6 \times 8 \lambda = 48 \lambda$

Total area =  $56 \lambda \times 48 \lambda$

Gate level module:

```
1  module invert(a,b,c,d,e,r);
2  input a,b,c,d,e;
3  output r;
4  wire p,q;
5  or (p,a,b);
6  or (q,c,d,e);
7  nand(r,p,q);
8  endmodule
9
```

Transistor level module:

```
1  module transistor_level(a,b,c,d,e,out);
2  input a,b,c,d,e;
3  output out;
4  wire PD1,PD2,PD3,ND1,out;
5
6  pmos ( PD1, 1, a);
7  pmos ( out, PD1, b);
8  pmos ( PD2, 1, c);
9  pmos ( PD3, PD2, d);
10 pmos ( out, PD3, e);
11
12 nmos ( out, ND1, c);
13 nmos ( out, ND1, d);
14 nmos ( out, ND1, e);
15 nmos ( ND1, 0, a);
16 nmos ( ND1, 0, b);
17 endmodule
18
```

Questa output for all 32 possible combinations (for gate level and transistor level the outputs are same)

Gate level:

```
add wave -position end sim:/sim/t_r
VSIM 8> run
# The Inputs of Circuit is: a:0, b:0, c:0, d:0, e:0
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:0, d:0, e:1
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:0, d:1, e:0
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:0, d:1, e:1
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:1, d:0, e:0
# The Output of add4 is: 1
run
# The Inputs of Circuit is: a:0, b:0, c:1, d:0, e:1
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:1, d:1, e:0
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:1, d:1, e:1
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:1, c:0, d:0, e:0
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:1, c:0, d:0, e:1
# The Output of add4 is: 0
run
# The Inputs of Circuit is: a:0, b:1, c:0, d:1, e:0
# The Output of add4 is: 0
# The Inputs of Circuit is: a:0, b:1, c:0, d:1, e:1
# The Output of add4 is: 0
# The Inputs of Circuit is: a:0, b:1, c:1, d:0, e:0
# The Output of add4 is: 0
# The Inputs of Circuit is: a:0, b:1, c:1, d:0, e:1
# The Output of add4 is: 0
# The Inputs of Circuit is: a:0, b:1, c:1, d:1, e:0
# The Output of add4 is: 0
run
# The Output of add4 is: 0
run
# The Inputs of Circuit is: a:0, b:1, c:1, d:1, e:1
# The Output of add4 is: 0
# The Inputs of Circuit is: a:1, b:0, c:0, d:0, e:0
# The Output of add4 is: 1
# The Inputs of Circuit is: a:1, b:0, c:0, d:0, e:1
# The Output of add4 is: 0
# The Inputs of Circuit is: a:1, b:0, c:0, d:1, e:0
# The Output of add4 is: 0
# The Inputs of Circuit is: a:1, b:0, c:0, d:1, e:1
# The Output of add4 is: 0
run
# The Inputs of Circuit is: a:1, b:0, c:1, d:0, e:0
# The Output of add4 is: 0
# The Inputs of Circuit is: a:1, b:0, c:1, d:0, e:1
# The Output of add4 is: 0
# The Inputs of Circuit is: a:1, b:0, c:1, d:1, e:0
# The Output of add4 is: 0
# The Inputs of Circuit is: a:1, b:0, c:1, d:1, e:1
# The Output of add4 is: 0
run
# The Inputs of Circuit is: a:1, b:1, c:0, d:0, e:0
# The Output of add4 is: 1
# The Inputs of Circuit is: a:1, b:1, c:0, d:0, e:1
# The Output of add4 is: 0
# The Inputs of Circuit is: a:1, b:1, c:0, d:1, e:0
# The Output of add4 is: 0
# The Inputs of Circuit is: a:1, b:1, c:0, d:1, e:1
# The Output of add4 is: 0
# The Inputs of Circuit is: a:1, b:1, c:1, d:0, e:0
# The Output of add4 is: 0
VSIM 9> run
# The Inputs of Circuit is: a:1, b:1, c:1, d:0, e:1
# The Output of add4 is: 0
# The Inputs of Circuit is: a:1, b:1, c:1, d:1, e:0
# The Output of add4 is: 0
# The Inputs of Circuit is: a:1, b:1, c:1, d:1, e:1
# The Output of add4 is: 0
```

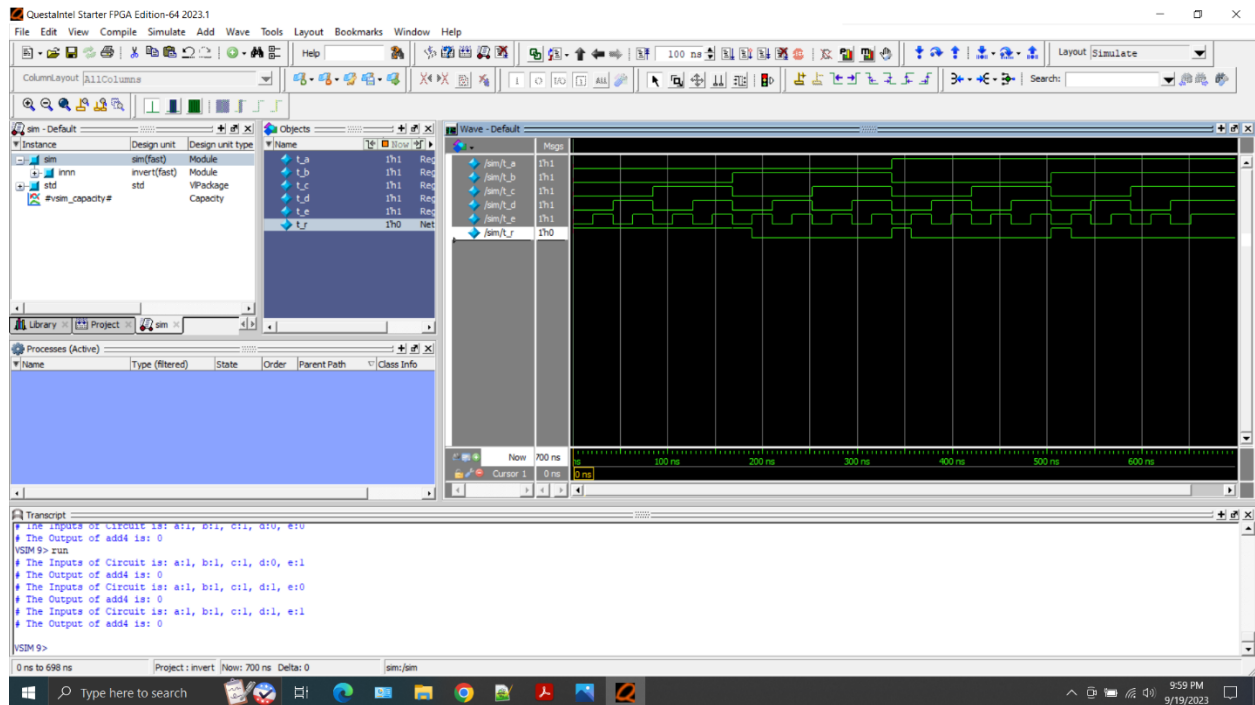
```

Transcript
# Attempting to use alternate WLF file "./wlfmgqlark".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
# Using alternate file: ./wlfmgqlark
add wave -position end sim:/testbench_cmos/t_b
add wave -position end sim:/testbench_cmos/t_c
add wave -position end sim:/testbench_cmos/t_d
add wave -position end sim:/testbench_cmos/t_e
add wave -position end sim:/testbench_cmos/t_r
VSIM i8> run -all
# The Inputs of Circuit is: a:0, b:0, c:0, d:0, e:0
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:0, d:0, e:1
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:0, d:1, e:0
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:0, d:1, e:1
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:1, d:0, e:0
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:1, d:0, e:1
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:1, d:1, e:0
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:0, c:1, d:1, e:1
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:1, c:0, d:0, e:0
# The Output of add4 is: 1
# The Inputs of Circuit is: a:0, b:1, c:0, d:0, e:1
# The Output of add4 is: 0
# The Inputs of Circuit is: a:0, b:1, c:0, d:1, e:0
# The Output of add4 is: 0
# The Inputs of Circuit is: a:0, b:1, c:0, d:1, e:1
# The Output of add4 is: 0
# The Inputs of Circuit is: a:0, b:1, c:1, d:0, e:0
# The Output of add4 is: 0
# The Inputs of Circuit is: a:0, b:1, c:1, d:0, e:1
# The Output of add4 is: 0
# The Inputs of Circuit is: a:0, b:1, c:1, d:1, e:0
# The Output of add4 is: 0
# The Inputs of Circuit is: a:0, b:1, c:1, d:1, e:1
# The Output of add4 is: 0

```

Project : invert	Now: 652 ns	Delta: 1
------------------	-------------	----------

Wave form of gate level:



Wave form of transistor level:

