Modular Design in Bluespec Using Asim / AWB

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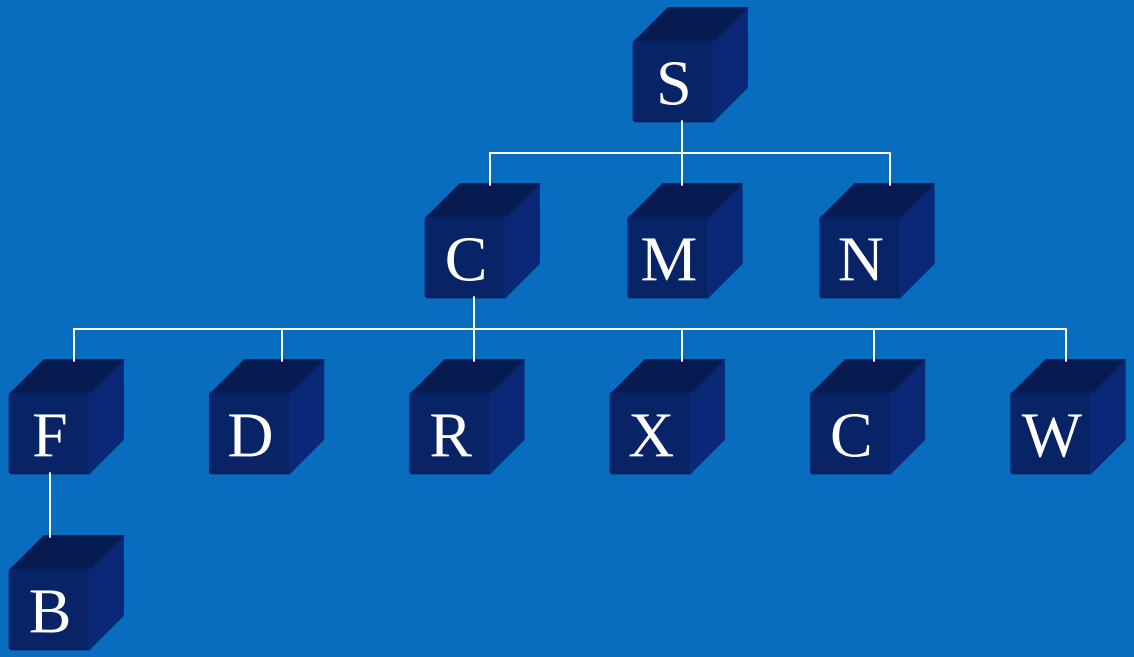
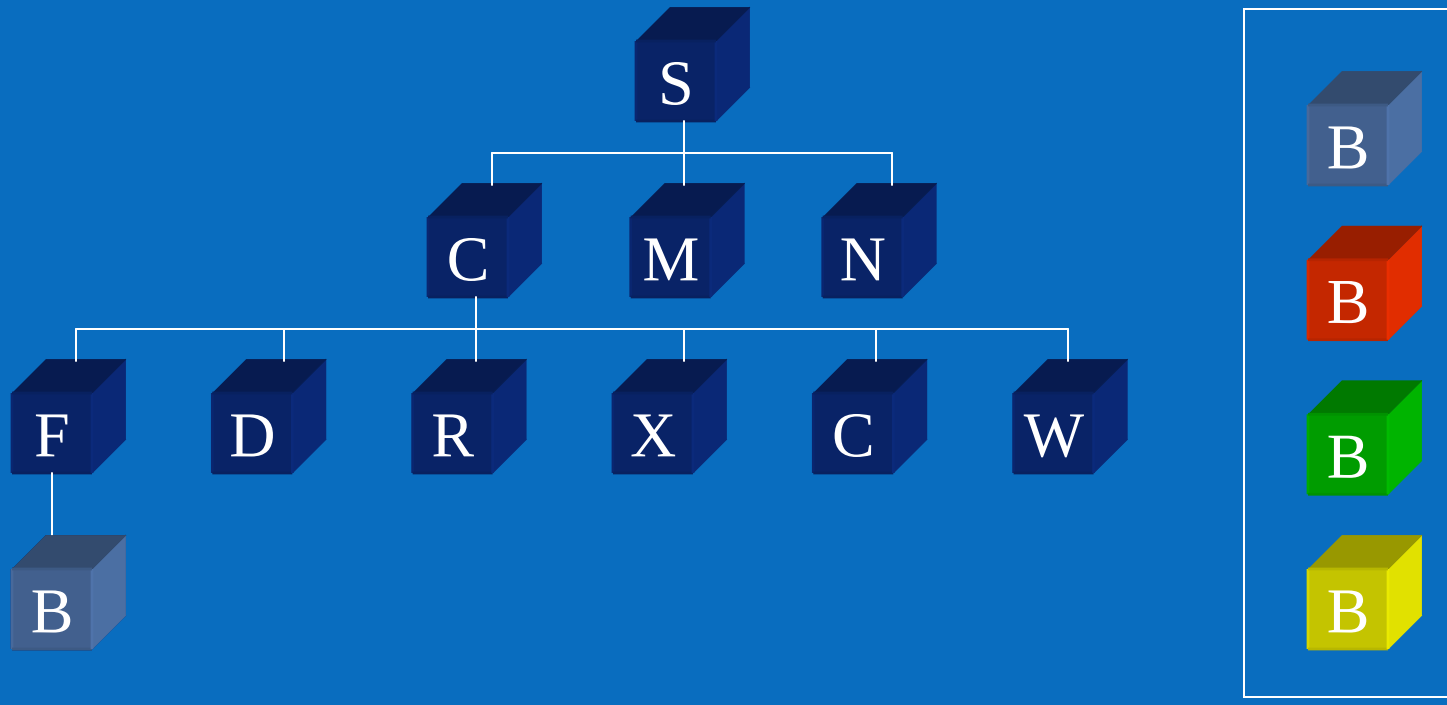
Why modularity?

- Speed of development
- Shared components between products
- Reuse across generations
- Improved fidelity
- Incremental refinement
- Facilitates area/speed trade-offs
- Architectural experimentation
- Factorial development and evaluations
- Sharing

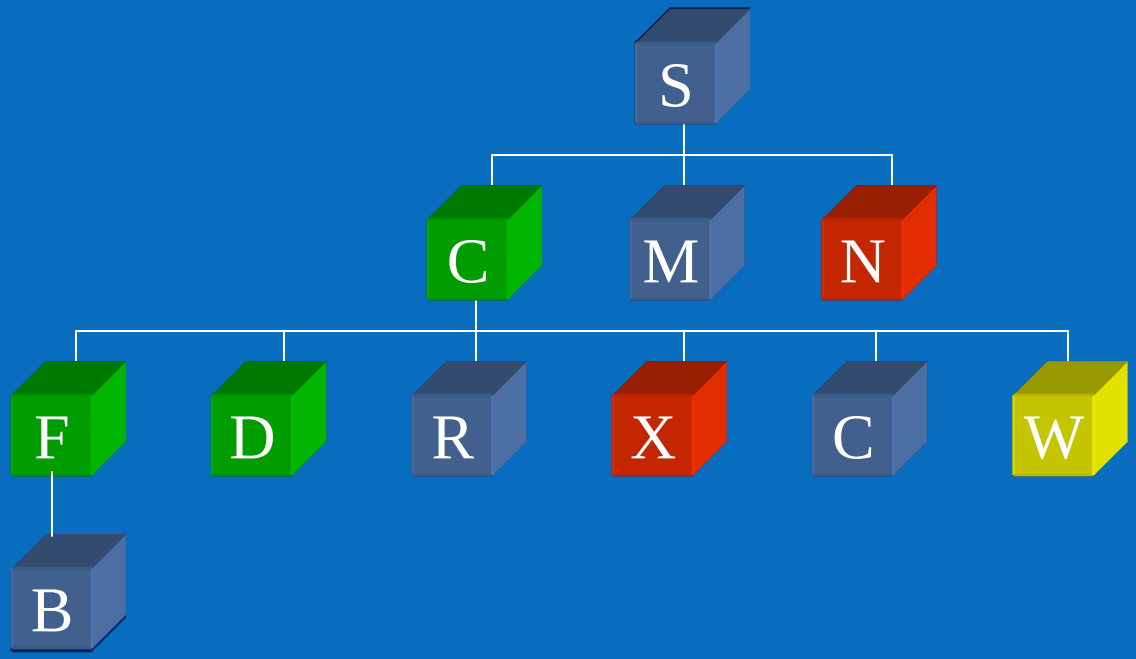
ASIM Module Hierarchy

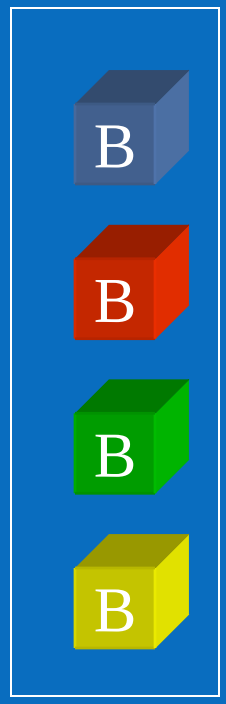


ASIM Module Selection

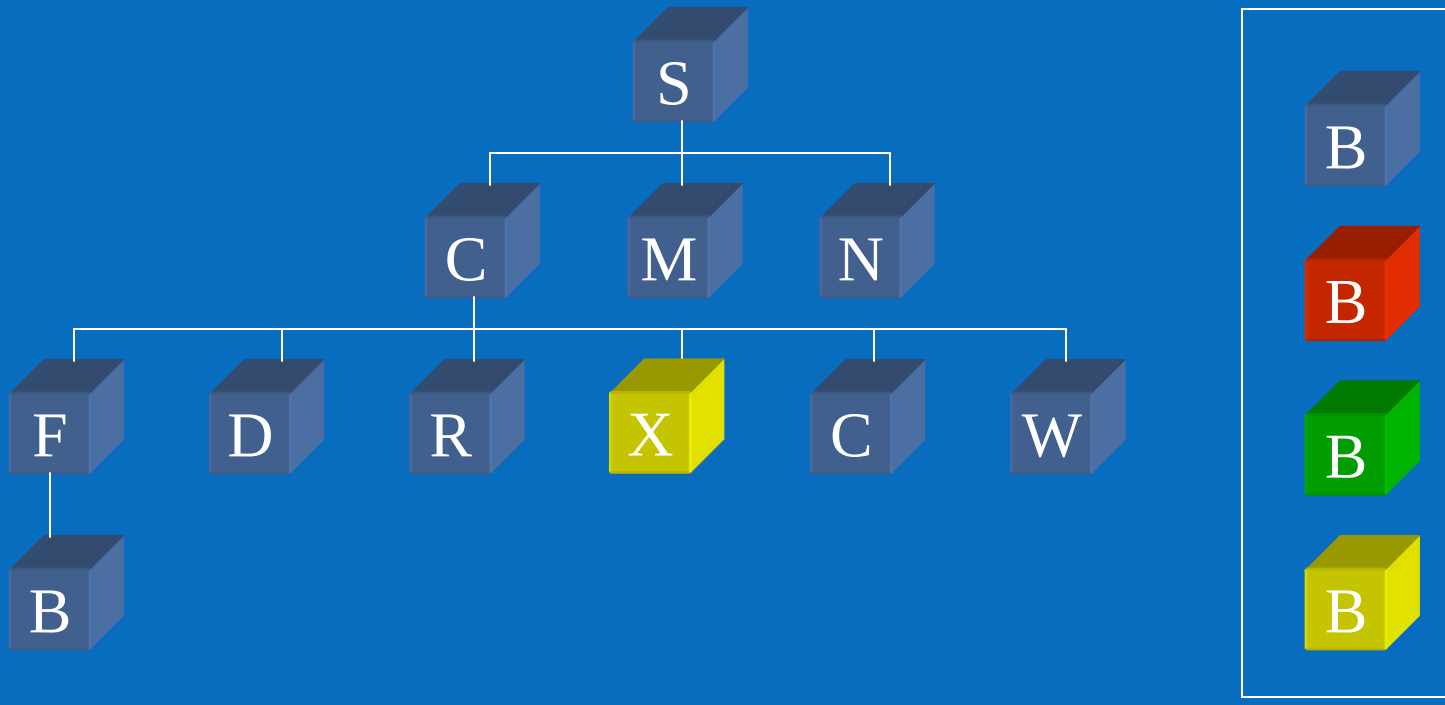


Module Selection

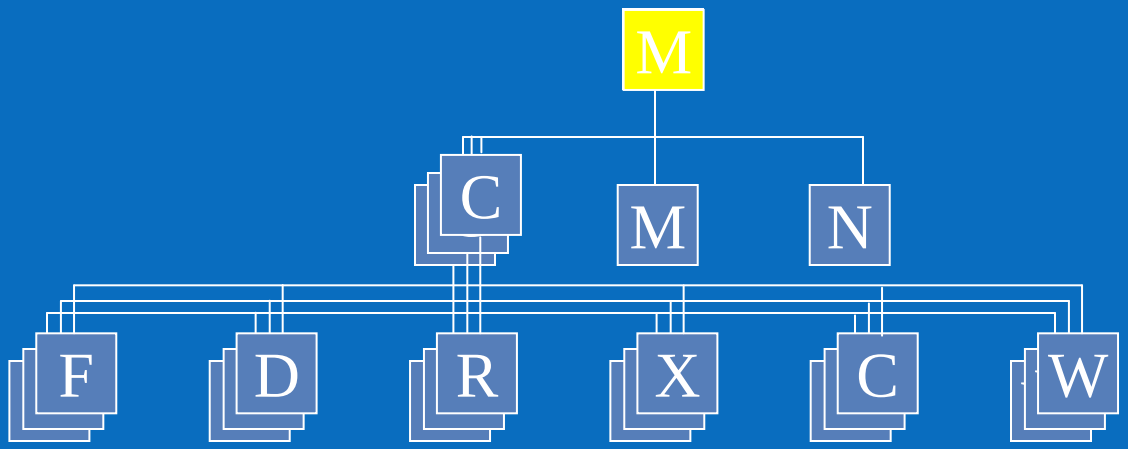




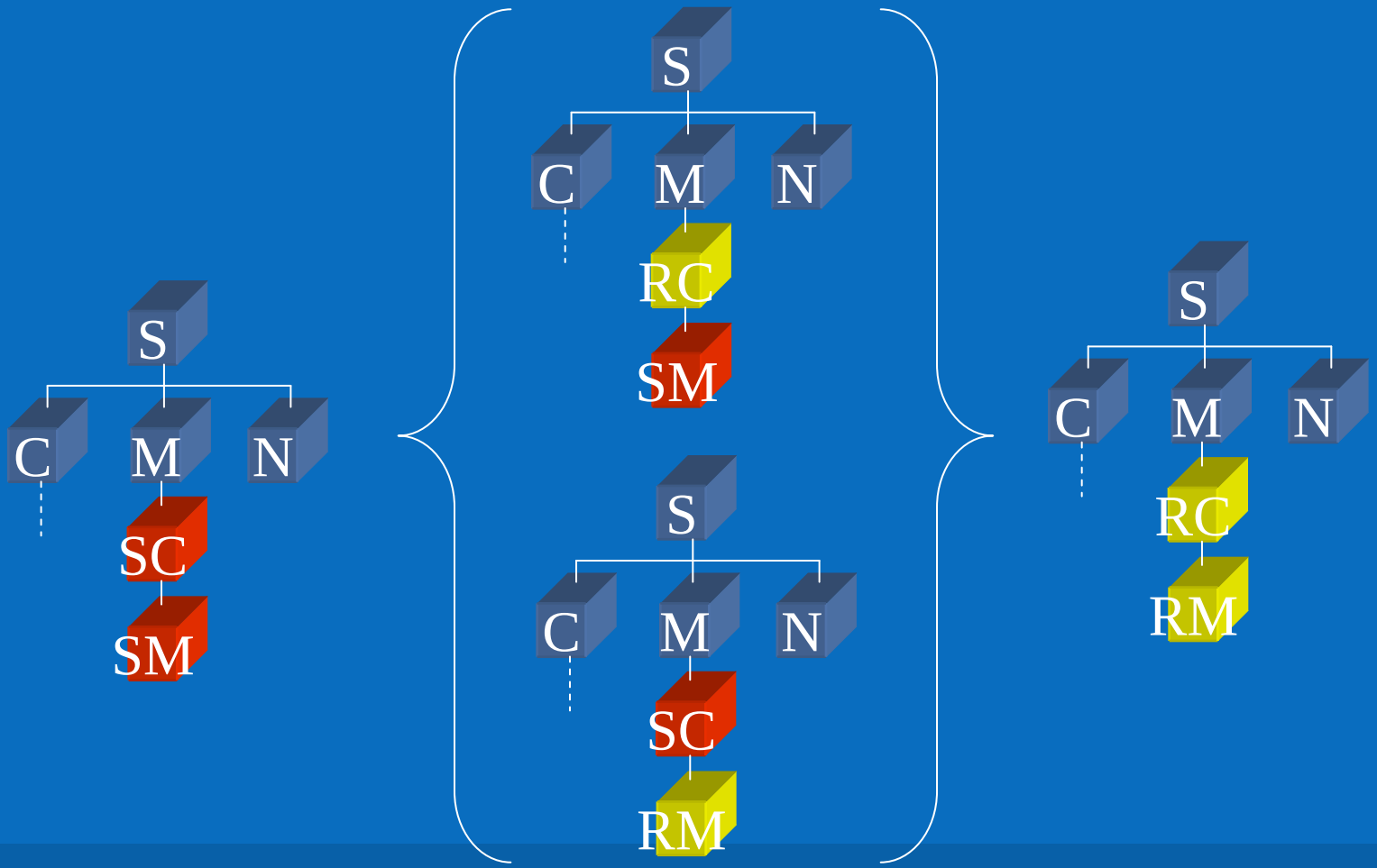
Module Replacement



Module Instantiation



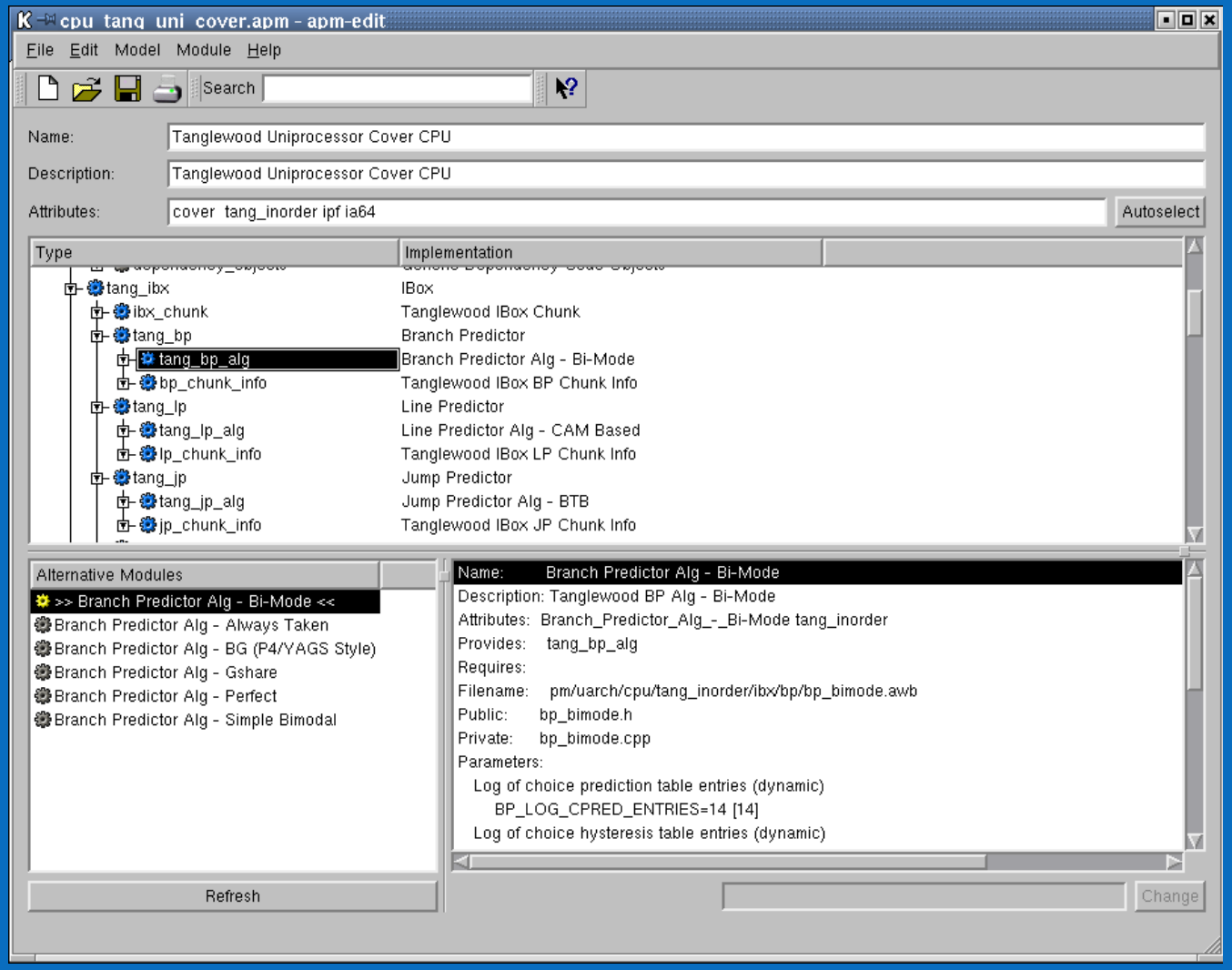
Factorial Coding / Experiments



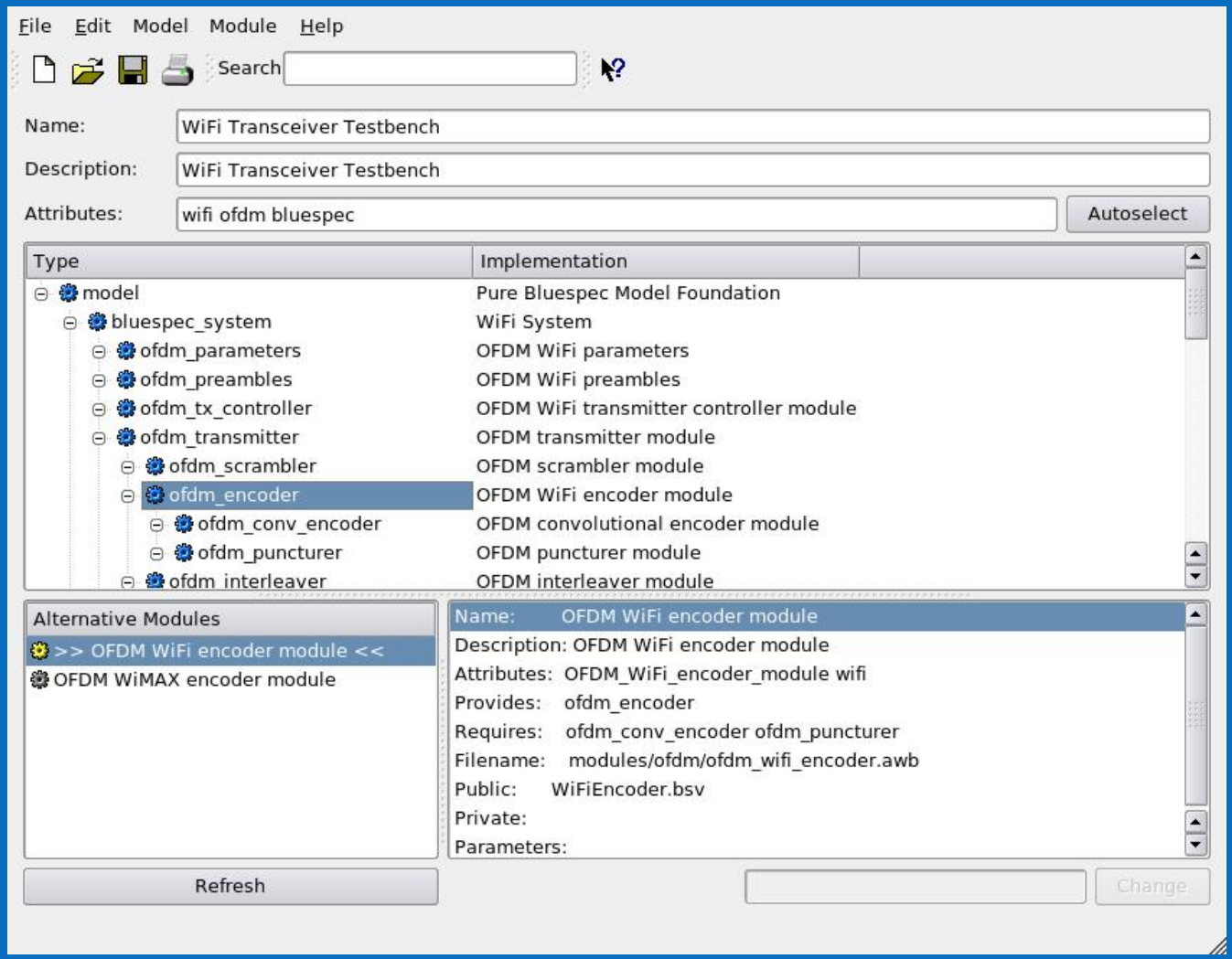
Module Description (.awb file)

```
%name SMIPS R10K Superscalar Decode Stage

%desc SMIPS R10K Superscalar Decode Stage

%attributes s10k smips hasim


%provides hasim_pipe_decode

%requires hasim_rob hasim_branch_pred


%public Decode.bsv
```

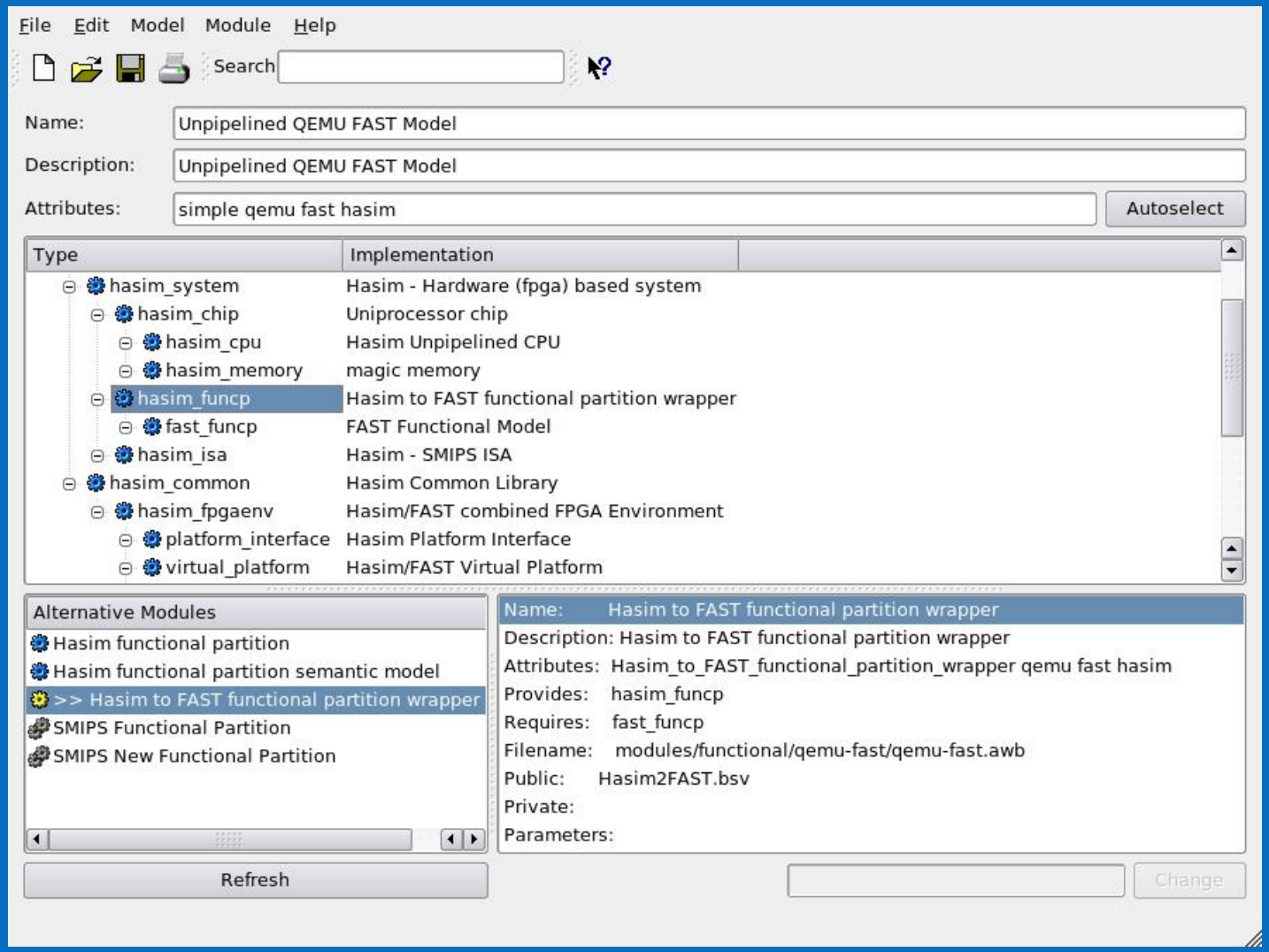
(H)ASIM Module Hierarchy



(H)ASIM Module Hierarchy



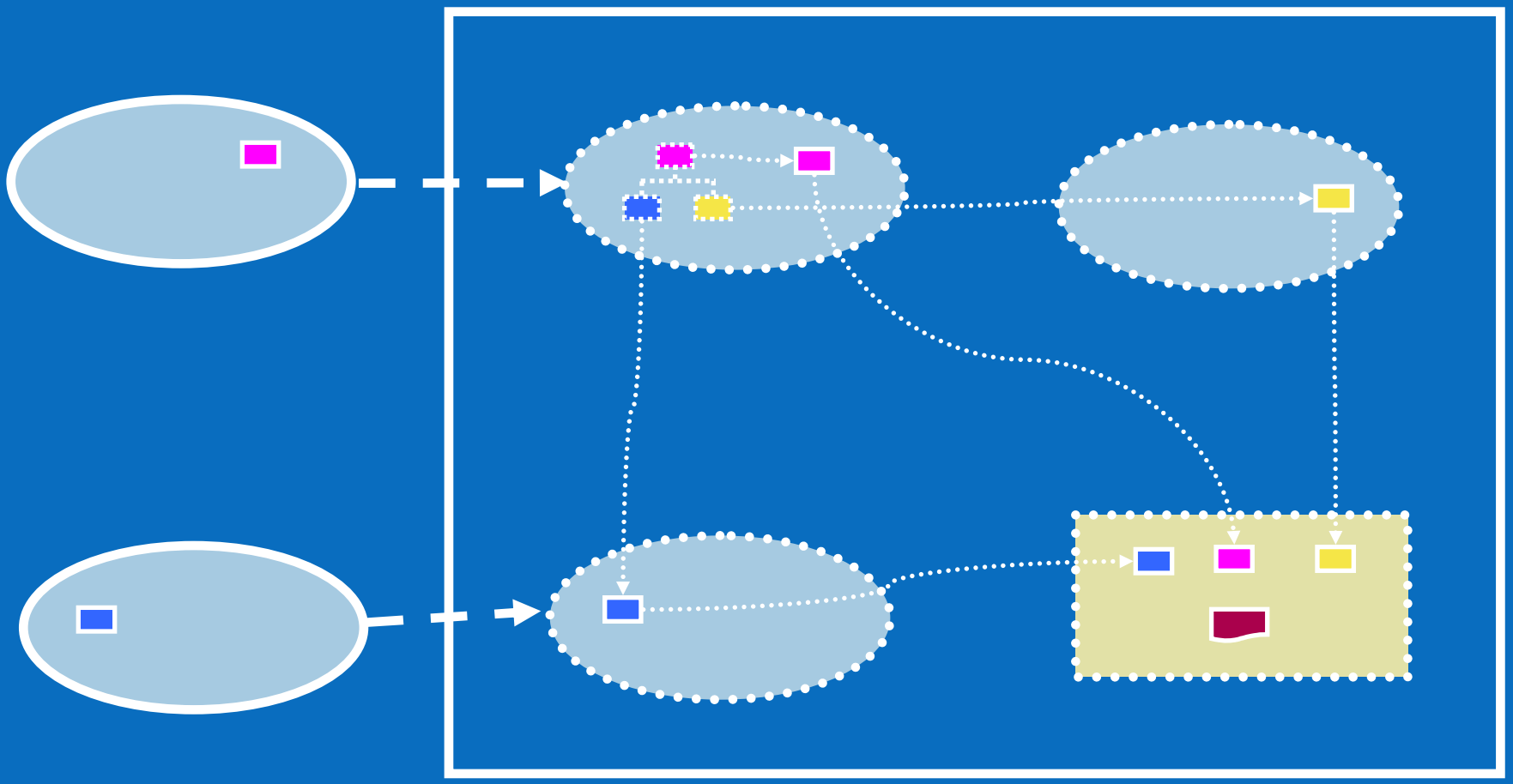
(H)ASIM Module Hierarchy



Module Interfaces

- Plumbing Modules
- Algorithm Modules
- Message Modules
- Library Modules

AWB Operation



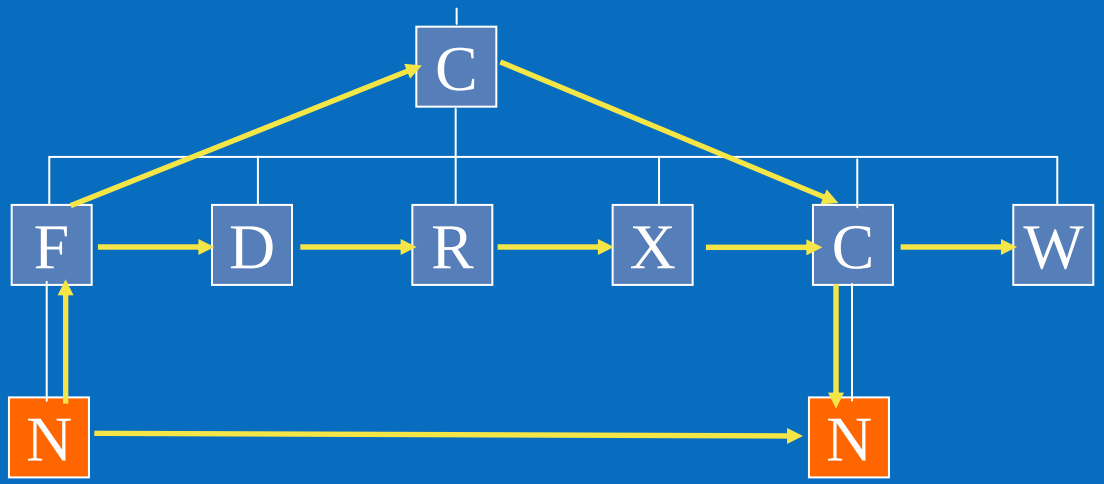
Repositories

Workspace

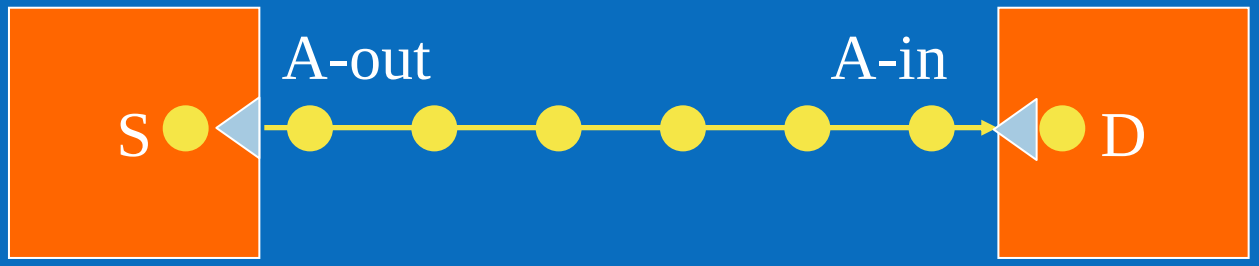
Build Features

- Model level parameter specification
- Automatic Makefile creation from templates (L2)
- Bluespec module dependence analysis
- Easy to specify synthesis boundaries (L3a)
- Support for parallel builds (L3b)
- Allows BDPI and Verilog modules (L7)
- Support for hybrid hardware/software modules
- Targets bitfile, iverilog, Bluesim

Communication: A modularity speedbump



Soft Connections: Flattening the speedbumps



Soft Connections

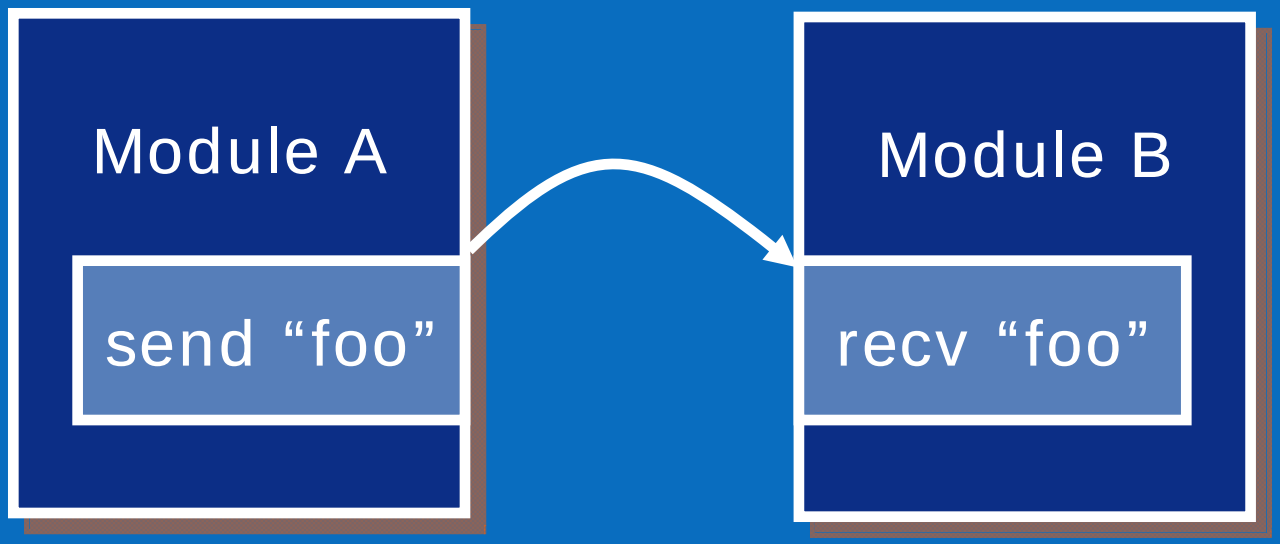
- Use “ModuleCollect” to collect connection names:

```
let my_con <- mkConnection_Send(“dec_to_exe”);
```

- Use static elaboration to find/join ends. Pseudo-code:

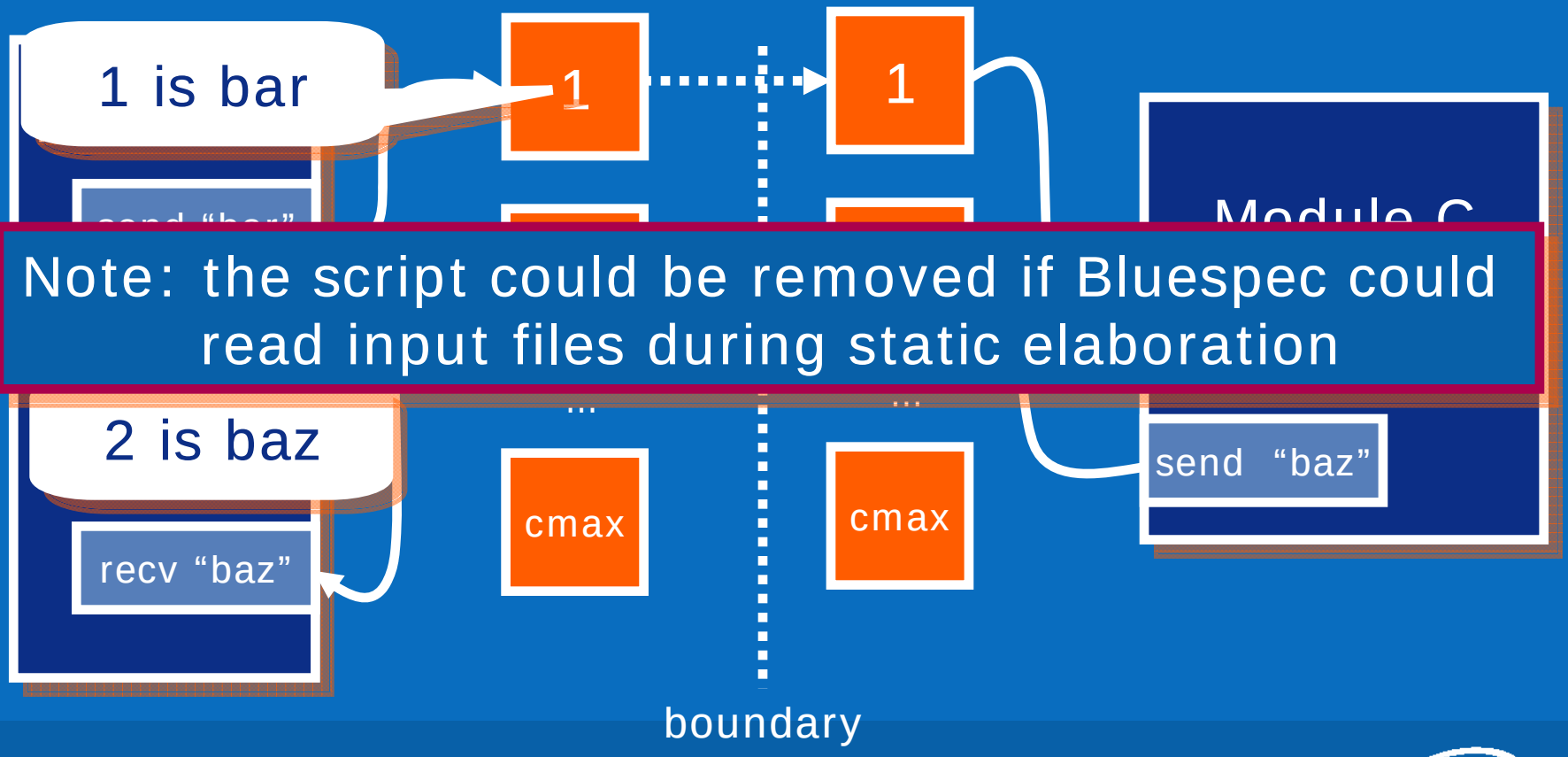
```
let cons <- getCollection(toplevel);                    //Get the connections
match {.sends, .recs} = splitConnections(ld);    //Split into sends, recs
match {.dang_sends, .dang_recs, .cncts} = groupByName(sends, recs);
foreach {.send, rec} in cncts
       mkConneciton(send, rec);
if (dang_sends != nil || dang_recs != nil)
       error “Dangling Connections at top level!
```

Connections



Connections Across Synthesis Boundaries (L3)

4. Use the previous scheme to connect as normal



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Soon...

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