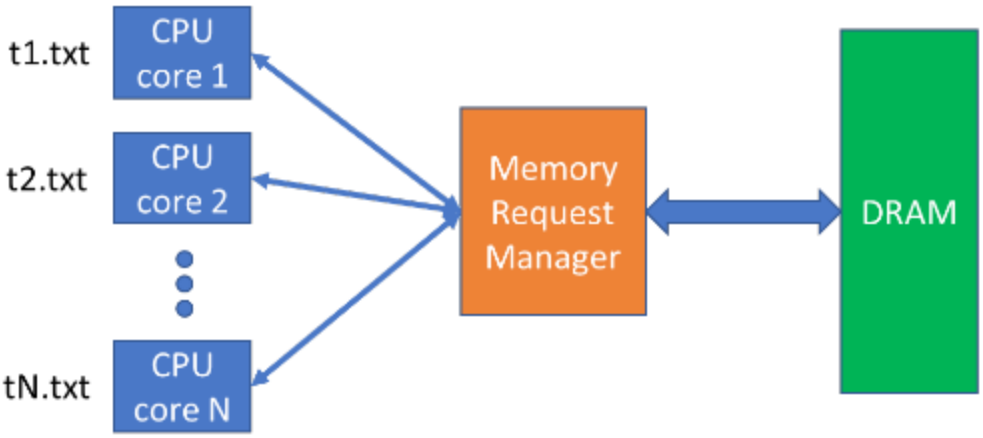

1. Extend your earlier MIPS simulator (with DRAM timings) to the multicore scenario. Your objective is to implement the Memory Request Manager in such a way that the instruction throughput (total number of instructions completed by the whole system in a given period, say from Cycle 0 to Cycle M) is maximised.

   What is expected:
   1. Implementation of the memory request manager
   2. Logic used by the memory manager (if there are multiple requests waiting, which one will it choose?)
      a. The memory manager can remember past history, **if needed,** to make its decision (similar to branch prediction where the past behaviour of branches is used to predict the current branch direction)
      b. ThroughPut should be maximized
2. Estimate the delay (in clock cycles) of your own Memory Request Manager algorithm and incorporate it into your timing model. Justify the estimation. Remember this is an estimate. You don't have to design the entire manager hardware.
   a. Memory manager needs some cycles to decide which request should be sent to DRAM next. This might cause delays to overall execution. Provide the delay caused by memory manager and its impact on overall execution. Total cycles your program takes includes memory manager delays also.