Some common mistakes identified during Assignment-4 demos

1. Using Non-blocking memory is required
2. Finite wait buffer (size can be any finite value, the reason for chosen finite value should be justifiable with experimental analysis)
3. 2 instructions trying to write to registers in same cycle -> Page 247 of textbook
4. Lw $t2, 1000($t0)
   Addi $t0, $t1, 10

   These 2 are independent instructions. Some students implemented them as dependent assuming add will change t0 content in next cycle which will change address value of load instr.

   Lw instruction has already computed the memory address value it has to access in cycle i by reading out register t0. In cycle i+1, addi instruction can change value of t0.
5. Design Choice: understand that the design choice should be to solve broader problem. Design choice is not an excuse to limit your solution to minimalistic implementation.
6. IPC, tradeoff of starvation with cycle analysis - actually causes major issue. -> ignore for assignment-4