| Digital Design and Computer Architecture: Lab Report | | |
|---|---|---|
| Lab 6: Testing the ALU | | |
| Date | | Grade |
| Names | | |
| | | Lab session / lab room |
| | | |

**You have to submit this report via Moodle.**

**Use a zip file or tarball that contains the report and all other files you used for the report, i.e., the entire Verilog project folder and/or all schematics you drew. If any files are missing, it may negatively impact your grade. No shortcuts/links will be accepted.**

**Only one of the members of each group should submit. All members of the group will get the same grade.**

**The name of the submitted file should be *Lab1_LastName1_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the last names of the members of the group.**

**The deadline for the report is a hard deadline and it will not be extended.**

## Exercise 1. Designing a Testbench for the FSM of Lab 4

In the manual, you learned how to design a testbench for a combinational circuit (the ALU).

In this exercise, you will design a simple testbench for the FSM from Lab 4.

You need to use the testbench to pass the inputs to the unit under test (UUT) — in this case, your FSM — and observe and verify the state transitions (current state and next state) in the waveforms. You do not need to specify the golden model result and compare it with your FSM output through the testbench.

**Note: Enable and disable the reset signal during the initialization phase. You also need to pass the clock signal to the FSM module.**

In your submission, include:

- Your testbench Verilog code;
- Your FSM codes from Lab 4;
- Your input file;
- A print-screen of your state transitions in the waveforms for the case when you set the ***right*** signal equal to logic-1.

## Feedback

If you have any comments about the exercises (e.g., related to mistakes in the text, the difficulty level, or anything else that will help us improve them), please submit them through Moodle, using the corresponding “Lab 6: Feedback” form:

https://moodle-app2.let.ethz.ch/mod/feedback/view.php?id=899257