Digital Design and Computer Architecture: Lab Report		
Lab 8: Full System Integration (Session I)		
Date		Grade
Names		
		Lab session / lab room

You have to submit this report via Moodle.

Use a zip file or tarball that contains the report and all other files you used for the report, i.e., the entire Verilog project folder and/or all schematics you drew. If any files are missing, it may negatively impact your grade. No shortcuts/links will be accepted.

Only one of the members of each group should submit. All members of the group will get the same grade.

The name of the submitted file should be *Lab1_LastName1_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the last names of the members of the group.

The deadline for the report is a hard deadline and it will not be extended.

Exercise 1

Which MIPS instructions do you think would produce wrong outputs if the ControlUnit signal *RegWrite* is *'stuck at 0'*, i.e., *RegWrite* always has the value 0? In other words, which MIPS instructions depend on the control signal *RegWrite*?

Exercise 2

Explain why a 6-bit address is enough for the instruction and data memory. *(Hint: think about the size of the memory.)*

Exercise 3

As you might have noticed, there are three different counters used in this lab. One is present in the *snake_patterns.asm* file, the second is in the clock_div module, and the third is the `DispCount` signal for the 7-segment display. Explain the functions of each of these three counters/dividers in a sentence or two each.

Feedback

If you have any comments about the exercises (e.g., related to mistakes in the text, the difficulty level, or anything else that will help us improve them), please submit them through Moodle, using the corresponding "Lab 8.1: Feedback" form:

https://moodle-app2.let.ethz.ch/mod/moodleoverflow/view.php?id=903195