Digital Design and Computer Architecture: Lab Report		
Lab 3: Verilog for Combinational Circuits		
Date		Grade
Names		
		Lab session / lab room

You have to submit this report via Moodle.

Use a zip file or tarball that contains the report and all other files you used for the report, i.e., the entire Verilog project folder and/or all schematics you drew. If any files are missing, it may negatively impact your grade. No shortcuts/links will be accepted.

Only one member from each group should submit the report. All members of the group will get the same grade.

The name of the submitted file should be *Lab3_LastName1_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the last names of the members of the group.

The deadline for the report is a hard deadline and it will not be extended.

Exercise 1. Turning off the Redundant Displays (1.5 Pts)

If you do not like seeing all 7-segment displays showing the same number four times you may want to turn off the three extra 7-segment displays. They can be disabled by connecting their activation input to logic-1 (note that the activation input is active-low). In order to achieve this, you can add a new 4-bit output AN[3:0] into your top module and assign logic-1 to AN[1], AN[2] and AN[3], and logic-0 to AN[0].

At this point, you need to update the constraints file in order to map these new output signals to the activation pins on the board.

Do this by adding the following lines to your constraints file:

```
set_property PACKAGE_PIN U2 [get_ports {AN[0]}]
set_property PACKAGE_PIN U4 [get_ports {AN[1]}]
set_property PACKAGE_PIN V4 [get_ports {AN[2]}]
set_property PACKAGE_PIN W4 [get_ports {AN[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {AN}]
```

You can name the new output as you prefer. Just be careful to be consistent with your choice when updating the constraints file. After this little tweak, generate the programming file again and reprogram the board. You should now see only the right-most 7-segment display on.

Exercise 2. Choosing a Specific Display (1.5 Pts)

Change your design of Exercise 1, so that you can select which 7-segment display to turn on. Design a decoder that 1) receives two inputs from two switches on the board and 2) based on them, activates only one of the 7-segment displays.

Feedback

If you have any comments about the exercises (e.g., related to mistakes in the text, the difficulty level, or anything else that will help us improve them), please submit them through Moodle, using the corresponding "Lab 3: Feedback" form:

https://moodle-app2.let.ethz.ch/mod/feedback/view.php?id=888009