Germanium Core

Lilly Anderson

January 14, 2024

Contents

Introduction

This is the GeCo (Germanium Core) architectural specification v0.1 Rev 2.0. This gives information on the hardware expectations of a valid GeCo implementation.

0.1 Goals

- Symmetric Multi-Processing
- Variable instruction length (16, 32, and 64 bit sizes)
- Software managed address translation
- Memory mapped IO

1 16 Bit Encodings

This section describes compressed instruction encodings for GeCo to help reduce binary sizes. We will use "CGC" to refer to 16 bit encodings in general.

1.1 Overview

CGC is used to compress a few different kinds of instructions, specifically common types of instructions, such as stack, thread, and global relative accesses, loading immediates, arithmetic operations, jumping, and branching. It supports 4 different encodings.

-

2 32 Bit Encodings

3 64 Bit Encodings

4 Instructions

5 Registers

The GeCo processors support 31 different general purpose registers, and 1 register doubling as a scratch, and no-access register. There are also 256 CSR (Control/Status Register) addresses.

5.1 Definitions

Term	Read	Write
RAWA	Any	Any
RAWI	Any	Ignored
RAWL	Any	Legal

5.2 Main Registers

Main registers are intended to be used for general processing.

Register ID	Name	Use
0b00000	Zero/Scratch	Will read zero[1]
0b00001	Frame pointer	Points to the start of the frame
0b00010	Stack pointer	Current position in the stack
0b00011	Stack base	Start of the stack in memory
0b00100	Global pointer	Points to the global storage region
0b00101	Thread pointer	Points to the thread storage region
0b00110	Return address	Stores where to return to after a jump
0b00111-0b11111	gp0-gp24	General purpose, any use

5.3 Control/Status Registers

Contro/Status Registers are used to control aspects of the processor, or query the status of different parts of the processor.

5.3.1 CSR Listing

Address	Bits	Name	Access	Minimum Mode	Section
0x000000	64	scause	RAWI	Supervisor	7.2
0x000001	64	strap	RAWA	Supervisor	7.2
0x000002	64	sret	RAWA	Supervisor	7.2
0x000003	64	sscratch	RAWA	Supervisor	7.2
0x010000	64	memmode	RAWL	Supervisor	8
0x010014	64	memscratch	RAWA	Supervisor	8

6 Traps

On a GeCo system traps serve to help handle internal errors, and external devices.

[1] It can be read/write if the trap bit in the processor flags is set, it's state must be consistent accross traps

6.1 Overview

To provide proper access to external devices, and internal error handling, GeCo provides traps as they come in. These traps can occur due to several reasons, and can be mapped to different values.

Source	Number	Reason
External (1)	0x00	MSI
External (1)	0x02	Timer
External (1)	0x04	External device
Internal (0)	0x00	Misaligned instruction
Internal (0)	0x02	Misaligned read
Internal (0)	0x04	Misaligned write
Internal (0)	0x06	Invalid instruction address
Internal (0)	0x08	Invalid read address
Internal (0)	0x0A	Invalid write address
Internal (0)	0x0C	Instruction page fault
Internal (0)	0x0E	Read page fault
Internal (0)	0x10	Write page fault

6.2 CSRs

To allow for changing the device's state for traps there are several CSRs provided by GeCo. These CSRs can manage the trap handler address, the trap cause, the MSI source, and return address.

6.2.1 strap

Supervisor trap, or "strap", is a CSR used to control the virtual address of the trap handler, if virtual addressing is disabled then this address will be treated as physical.

Bit(s)	Name	Use
0..62	Strap Vaddr	Lower 63 bits of the trap handler's address
63	Strap On	Enables trapping[1]

6.3 Core Communication Device

The CCD (Core Communication Device) can be used to alert other cores of new events, this acts similarly to an MSI but may be implicitly triggered by the processor, or may have implicit reactions. This device can be used to send IPIs, send remote fences, and change the state of other cores.

[1] If a trap occurs and the strap.on bit is not set, then the core may repeatedly trap until powered down, halt execution but remain powered on, or it can power down that core, if every core in a chip is powered down then the entire system must power down. Regardless of if it shuts the core down, if other cores exist the CCD (specified in 7.3) must be notified

6.3.1 Layout

The CCD provides different regions, each region contains registers used for controlling the other cores, or the local core. It is split into 2 regions, the Core Control region (CCR), and the Core Local Buffer region (CLB). The CCR must always be provided at physical address 0x2000, and take up 0x2000 bytes. The CLB must be provided at physical address 0x1000, and take up 0x1000 bytes.

Core Control Region Layout

Byte	Size	Name	Use
0x0	2	Core 0 Control	Used to send a signal to the core[1]
...	...	...	...
0x1FF8	2	Core 4095 Control	Used to send a signal to the core[1]

7 Virtual Addressing

[1] If a core is not associated with that register, nothing should happen