

# Wells Fargo Challenge – Phase 3

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## 1 Final Circuit Execution and Output Validation

We first begin with mathematical analysis of an ideal mid-circuit measurement circuit and prove the equivalence for our proposed solution using mid-circuit measurement.

### Mathematical Modeling for the Conditional Evolution of Ideal Mid-Circuit Measurement Logic

Let the two data qubits both be prepared in the same state  $|x_0\rangle = \alpha|0\rangle + \beta|1\rangle$ , with  $|\alpha|^2 + |\beta|^2 = 1$ , and the ancilla qubit in  $|0\rangle$ . The joint input is  $|\Psi_{in}\rangle = |x_0\rangle_1 \otimes |x_0\rangle_2 \otimes |0\rangle_3$ . As an example, we use the below entangling unitary:

$$U = \text{CNOT}_{1 \rightarrow 3} \text{CNOT}_{1 \rightarrow 2} (H_1 \otimes I_2 \otimes I_3), \quad (1)$$

where H is the Hadamard gate.

After the first application of  $U$ ,

$$|\Psi_1\rangle = U |x_0, x_0, 0\rangle \quad (2)$$

$$= \text{CNOT}_{1 \rightarrow 3} \text{CNOT}_{1 \rightarrow 2} (H(|x_0\rangle) \otimes |x_0\rangle \otimes |0\rangle), \quad (3)$$

$$= \text{CNOT}_{1 \rightarrow 3} \text{CNOT}_{1 \rightarrow 2} \frac{\alpha|+\rangle + \beta|-\rangle}{\sqrt{2}} |x_0\rangle |0\rangle, \quad (4)$$

$$= \text{CNOT}_{1 \rightarrow 3} \text{CNOT}_{1 \rightarrow 2} (c_0|0\rangle + c_1|1\rangle)_1 |x_0\rangle_2 |0\rangle_3, \quad (5)$$

$$= c_0|0, x_0, 0\rangle + c_1|1, \tilde{x}_0, 1\rangle. \quad (6)$$

where  $c_0 = \frac{\alpha+\beta}{\sqrt{2}}$ ,  $c_1 = \frac{\alpha-\beta}{\sqrt{2}}$ , and  $|\tilde{x}_0\rangle = X|x_0\rangle = \alpha|1\rangle + \beta|0\rangle$ . A measurement of qubit 3 yields  $y_1 \in \{0, 1\}$ , projecting qubits 1–2 to

$$(q_1, r_1) = \begin{cases} (0, x_0), & y_1 = 0, \\ (1, \tilde{x}_0), & y_1 = 1. \end{cases} \quad (7)$$

For each round, we reset qubit 3 to  $|0\rangle$  and reapply  $U$ . For the generic expression for the output at round  $n$ , based on input  $(q_{n-1}, r_{n-1})$ :

$$|\Psi_n\rangle = U |q_{n-1}, r_{n-1}, 0\rangle \quad (8)$$

$$= \frac{1}{\sqrt{2}} (|0\rangle + (-1)^{q_{n-1}} |1\rangle)_1 |r_{n-1}\rangle_2 |0\rangle_3, \quad (9)$$

$$= \frac{1}{\sqrt{2}} (|0, r_{n-1}, 0\rangle + (-1)^{q_{n-1}} |1, \tilde{r}_{n-1}, 1\rangle), \quad (10)$$

so, the evolution of the first two qubits based on evolution of qubit 3 can be given as follows:

$$(q_n, r_n) = \begin{cases} (0, r_{n-1}), & y_n = 0, \\ (1, \tilde{r}_{n-1}), & y_n = 1. \end{cases} \quad (11)$$

**Deferred-Measurement Implementation and Equivalence Proof:** The *deferred measurement principle* states that any quantum circuit with intermediate measurements and classical feed-forward can be rewritten as a fully coherent unitary circuit by deferring all measurements to the end and replacing conditional operations with coherent control.

Regarding our problem statement, consider the ancilla registers  $E_1, \dots, E_n$ , each initialized to  $|0\rangle$ . For each round  $k = 1, \dots, n$ , perform:

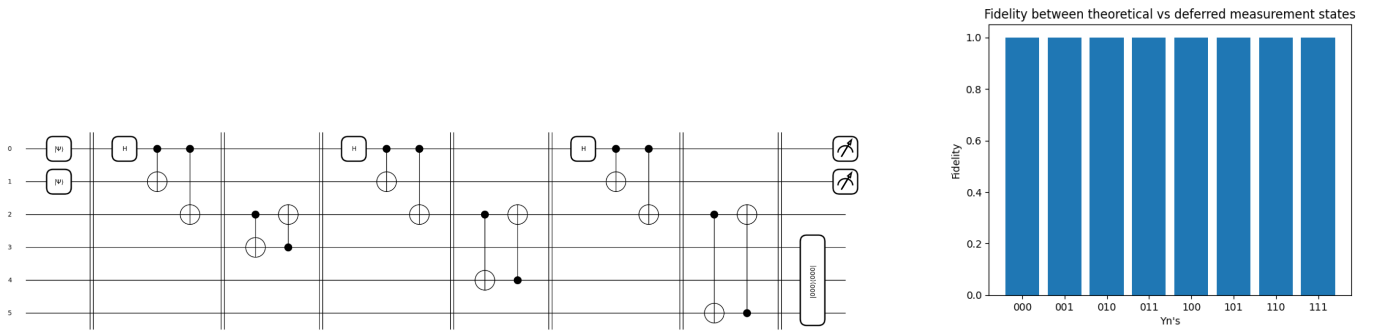
$$U_{123}(|q_{k-1}, r_{k-1}\rangle \otimes |0\rangle_3) = |q'_k, r'_k\rangle_{1,2} \otimes |q_k\rangle_3, \quad (12)$$

$$\text{CNOT}_{3 \rightarrow E_k} : |q_k\rangle_3 |0\rangle_{E_k} \mapsto |q_k\rangle_3 |q_k\rangle_{E_k}, \quad (13)$$

$$\text{CNOT}_{E_k \rightarrow 3} : |q_k\rangle_3 |q_k\rangle_{E_k} \mapsto |0\rangle_3 |q_k\rangle_{E_k}. \quad (14)$$

After  $n$  rounds, qubits 1–2 are in the same conditional state  $(q_n, r_n)$ , while ancillas store  $(y_1, \dots, y_n)$  coherently. A final projection of  $\{E_k\}$  based on the input  $\{y_i\}$  recovers the conditional evolution outcomes for qubits 1–2.

**Proof of equivalence:** We now show that, at round  $n$ , replacing the mid-circuit measure–reset on qubit 3 by the ancilla-driven CNOT sequence on  $E_n$  reproduces exactly same results as given in (11). For the round  $n$ , starting from input



(a) Deferred measurement circuit for  $y_1y_2y_3 = 001$

(b) Validation of output fidelity for  $n = 3$  across all possible  $Y_n(y_1y_2y_3)$ .

Figure 1: Deferred measurement circuit and associated analysis results.

$|q_{n-1}, r_{n-1}, 0\rangle_{123}$ , the application of unitary can be given as:

$$U_{123} : |q_{n-1}, r_{n-1}, 0\rangle \mapsto \frac{1}{\sqrt{2}} \left( |0, r_{n-1}, 0\rangle + (-1)^{q_{n-1}} |1, \tilde{r}_{n-1}, 1\rangle \right) = |\Psi_n\rangle_{123}.$$

The deferred circuit introduces  $|0\rangle_{E_n}$  and performs the below CNOTs:

$$\text{CNOT}_{3 \rightarrow E_n} : |\Psi_n\rangle_{123} |0\rangle_{E_n} \mapsto \frac{1}{\sqrt{2}} \left( |0, r_{n-1}, 0\rangle |0\rangle_{E_n} + (-1)^{q_{n-1}} |1, \tilde{r}_{n-1}, 1\rangle |1\rangle_{E_n} \right).$$

$$\text{CNOT}_{E_n \rightarrow 3} : |x\rangle_3 |y\rangle_{E_n} \mapsto |0\rangle_3 |y\rangle_{E_n},$$

This yields an outcome

$$\frac{1}{\sqrt{2}} \left( |0, r_{n-1}, 0\rangle |0\rangle_{E_n} + (-1)^{q_{n-1}} |1, \tilde{r}_{n-1}, 0\rangle |1\rangle_{E_n} \right).$$

Now qubit 3 is reset to  $|0\rangle$ , and  $E_n$  coherently holds the bit  $y_n$ .

If one now *measures* the ancilla  $E_n$  in the computational basis, the post-measurement joint state of qubits 1–2 is

$$(q_n, r_n) = \begin{cases} (0, r_{n-1}), & y_n = 0, \\ (1, \tilde{r}_{n-1}), & y_n = 1. \end{cases} \quad (15)$$

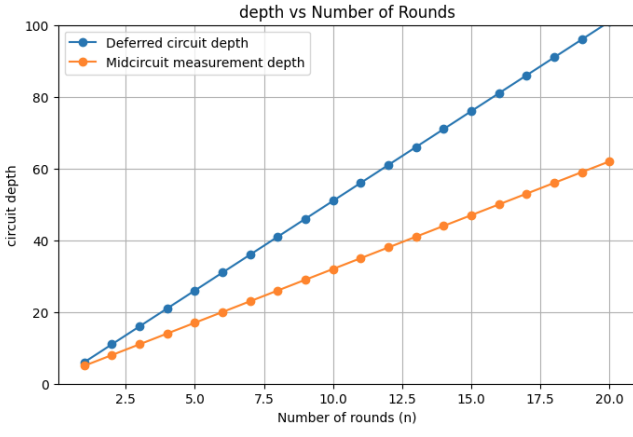
exactly as in the mid-circuit protocol.

Commutation ensures the future rounds match. Since  $E_n$  is an independent register, all future unitaries  $U_{123}$  commute with  $\text{CNOT}_{3 \rightarrow E_n}$  and  $\text{CNOT}_{E_n \rightarrow 3}$ . Thus subsequent rounds see the same input  $|q_n, r_n, 0\rangle_3$  and reproduce the identical conditional evolution on qubits 1–2. The circuit implementation for deferred measurement logic is given in Fig. 1a. Fig. 1b gives the fidelity plot for  $n = 3$  for all possible combinations of  $y_1y_2y_3$  on Aer simulator (both of these plots are implemented in approach.ipynb file in github. ). It can be seen that fidelity remains 1 and matches theoretical predictions, demonstrating that the deferred measurement implementation preserves the conditional evolution.

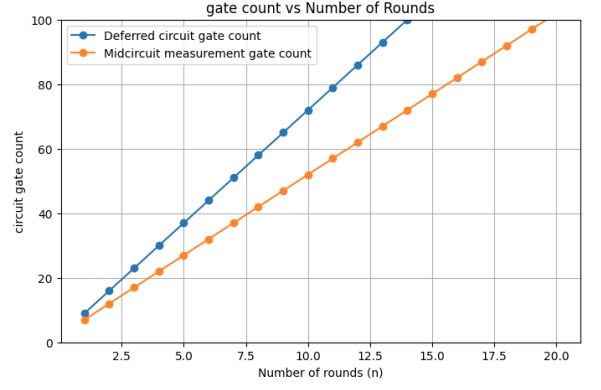
## 2 Performance and Scalability Benchmarks

All results in this section are performed using the ionq simulator, with the noise model configured as an Aria-1 to reflect realistic hardware behavior.

The proposed deferred measurement circuit design is benchmarked for fidelity decay, depth, gate count, memory overhead, and qubit reuse efficiency as the number of rounds  $n$  increases. The additional ancilla registers and coherent control operations add overhead compared to mid-circuit measurement but maintain practical fidelity and modularity for moderate depths.



(a) Circuit depth as a function of  $n$ .



(b) Gate count scaling with  $n$ .

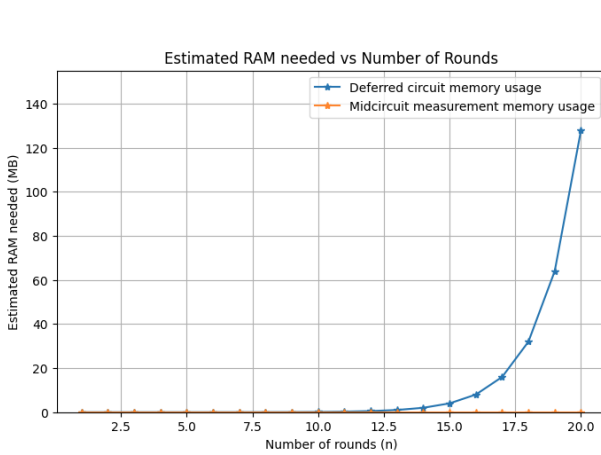
Figure 2: Circuit complexity trends: depth and gate count measured on the Aer simulator with an Aria-1 noise model.

Figure 2a and Figure 2b illustrate how the circuit depth and total gate count grow linearly with increasing  $n$ . This is due to the extra coherent control operations and ancilla management required to emulate measurement-conditioned feedback without explicit mid-circuit resets. These trends show that the overhead remains manageable for small to mid-scale circuits.

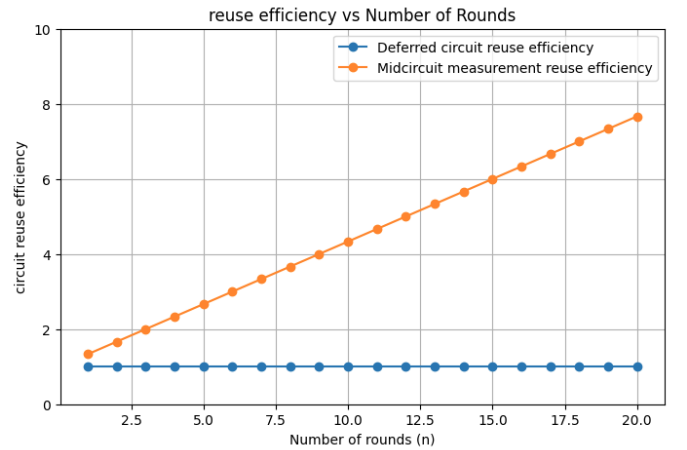
Figure 3a presents the scaling of memory usage as more ancilla registers are added to store intermediate measurement outcomes coherently. While this increases the circuit's memory footprint, it demonstrates the trade-off between hardware constraints (e.g., lacking fast qubit reset) and the modularity offered by the deferred measurement approach.

Figure 3b shows the qubit reuse efficiency with respect to  $n$ . As  $n$  increases, more ancillas are needed, but the deferred design maintains conditional evolution without mid-circuit resets. This makes it valuable for architectures where repeated measurement and reset operations are slow, noisy, or unavailable.

Overall, these benchmarks confirm that the deferred measurement circuit provides a flexible, hardware-compatible alternative to direct mid-circuit measurement, with acceptable resource overhead for moderate circuit depths and round numbers.



(a) Memory load vs.  $n$ .



(b) Qubit reuse efficiency vs.  $n$ .

Figure 3: Resource scaling: memory and qubit reuse metrics obtained on the Aer simulator (Aria-1 noise replica).

### 3 Connection to Real-World Feedback Systems

The proposed deferred measurement design provides a flexible framework for implementing feedback-controlled quantum operations when mid-circuit measurement and reset are limited or noisy. By coherently storing intermediate measurement outcomes in redundant ancilla registers, the design enables fault-tolerant measurement strategies that can detect and correct errors through majority voting over ancilla states, as discussed in further section.

In addition, the circuit naturally supports iterative update loops, allowing the conditional logic to mimic real-time feedback mechanisms common in quantum error correction protocols and adaptive control. This modular approach can be extended to emerging applications in quantum sensing, where precise and adaptive measurements improve sensitivity,

or in variational quantum algorithms and quantum machine learning tasks that benefit from measurement-conditioned parameter updates.

By balancing ancilla overhead and coherent control, this architecture bridges the gap between theoretical feedback schemes and practical constraints of near-term quantum hardware.

## 4 Error Analysis and Mitigation

To evaluate the robustness of the deferred measurement design, we simulated its behavior using the `ionq_simulator` backend, which emulates the longer coherence times and native support for deferred measurement characteristic of trapped-ion devices. Unlike an ideal simulator, `ionq_simulator` always includes realistic noise effects, providing a more representative benchmark for hardware performance.

To further analyze noise resilience, we incorporated an additional Aria-1 noise model, approximated by a simple depolarizing channel with representative error rates:

$$\text{ry} : p = 0.0005, \quad \text{rxx} : p = 0.0133.$$

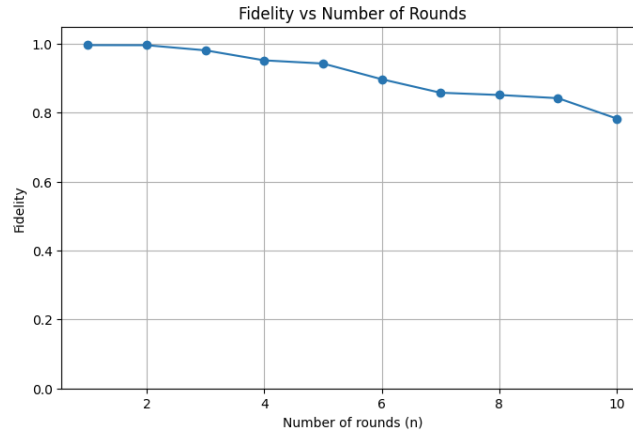


Figure 4: Fidelity of the deferred circuit on `ionq_simulator` with a simulated Aria-1 noise model.

As shown in Figure 4, the fidelity gradually declines with increasing  $n$ , consistent with the expectation that repeated entangling operations and ancilla management amplify the effects of noise.

Beyond noise, simulator constraints such as state vector truncation or the absence of dynamic control flow can challenge the accuracy of conditional evolution. We mitigated these issues by coherently encoding measurement outcomes into dedicated ancilla registers and verifying correct conditional branches through classical post-processing. Robust control sequences and explicit CNOT structures ensure that gate errors do not propagate uncontrollably through the feedback loop.

## 5 Reflections and Potential Extensions

This measurement-conditioned circuit architecture generalizes naturally to a range of larger and more complex quantum systems. One clear extension is scaling to deeper feedback loops and larger qubit registers. By adding multiple ancilla qubits, we can coherently encode more measurement outcomes, providing greater redundancy that helps mitigate noise and decoherence.

For example, consider a control qubit  $q_1 = \alpha|0\rangle + \beta|1\rangle$ , a data qubit  $q_2$ , and an ancilla register  $A = \{a_1, \dots, a_m\}$  initialized in  $|0^{\otimes m}\rangle$ . Applying the unitary

$$U = \left( \prod_{j=1}^m \text{CNOT}_{1 \rightarrow a_j} \right) \cdot \text{CNOT}_{1 \rightarrow 2} \cdot H_1$$

produces the entangled state

$$|\Psi_1\rangle = c_0|0, x_0, 0^{\otimes m}\rangle + c_1|1, \tilde{x}_0, 1^{\otimes m}\rangle, \quad c_0 = \frac{\alpha + \beta}{\sqrt{2}}, \quad c_1 = \frac{\alpha - \beta}{\sqrt{2}}.$$

In this configuration, only  $y = 0^m$  or  $y = 1^m$  occur with non-zero probability, enabling majority voting across the ancilla

register to detect or correct single-qubit noise events. This highlights how the deferred measurement scheme can be adapted to incorporate error correction features in larger systems.

In the future, combining this scheme with classical control logic could enable dynamic updates to unitary operations in response to intermediate outcomes, bridging the gap between measurement-based quantum computing and hybrid quantum-classical feedback loops found in high-frequency trading or adaptive portfolio strategies.

Together, these extensions demonstrate that the deferred measurement design is inherently scalable and adaptable to a range of practical and advanced quantum applications.

## Conclusion

We demonstrated a deferred measurement protocol with multiple ancilla qubits, verified its equivalence to mid-circuit measurement, and validated its robustness under noise. The results indicate practical feasibility for feedback-enabled quantum systems and open pathways for extensions in error correction and adaptive computation.

**Supporting materials** including source code and circuit files are submitted separately on github: [Github link](#).

## References

- [1] Y. Gurevich and A. Blass, “Quantum circuits with classical channels and the principle of deferred measurements,” Jul. 17, 2021, arXiv: arXiv:2107.08324. doi: 10.48550/arXiv.2107.08324.
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